Bidirectional Dual Active Bridge Converter for Energy Storage Applications

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Preface

This thesis constitutes the last part of a master's degree in Energy within the theme group electric power engineering at the University of Bergen (UiB), in association with the Western University of applied sciences(HVL). The work has been carried out over two semesters, autumn 2021 and spring 2022

The laboratory space and equipment used were provided by the Western Norway University of Applied Sciences, Faculty of Engineering and Science.

I hereby declare that this thesis is titled "*Bidirectional Dual Active Bridge Converter for Energy Storage Applications,*", and the work presented in it is my own.

Martin Thormodsæter Ramsdal   Date

Acknowledgment

Abstract

Harnessing energy through wind turbines and photovoltaic systems has increased in demand over the last decades. One major downside of these renewable energy resources is their fluctuating nature, as they cannot produce power on demand. A standard solution to overcome this problem is to use energy storage in conjunction with renewable energy resources to maintain a smooth and continuous power flow to the load. Energy storage applications such as battery packs and supercapacitors are the most common and economical solutions. However, they require a bidirectional DC to DC converter to adjust and regulate the voltage levels in both directions.

In this thesis, a simulation model in Matlab®/Simulink® and a hardware prototype of an isolated bidirectional DC/DC converter have been designed with Dual Active Bridge topology. Both systems have been implemented with single-phase shift modulation to regulate the output power and direction of power flow of the converter. The functionality and efficiency of the simulation model and hardware prototype results have been analyzed and compared. Power losses in the hardware prototype have been estimated based on the power results from the results gathered in the lab.

Sammendrag

Etterspørselen av energi gjennom vindturbiner og solcelleanlegg har økt i de siste tiårene. En stor ulempe ved disse fornybare energiressursene er deres fluktuerende natur, siden de ikke kan produsere kraft på forespørsel. En standardløsning for å overvinne dette problemet er å bruke energilagring i forbindelse med fornybare energiressurser for å opprettholde en jevn og kontinuerlig kraftstrøm til lasten. Energilagringsapplikasjoner som batteripakker og superkondensatorer er de vanligste og mest økonomiske løsningene. Imidlertid krever de en toveis DC til DC-omformer for å justere og regulere spenningsnivåene i begge retninger.

I denne oppgaven er en simuleringsmodell i Matlab®/Simulink® og en maskinvareprototype av en isolert toveis DC/DC-omformer designet med Dual Active Bridge-topologi. Begge systemene har blitt implementert med Single Phase Shift modulasjon for å regulere utgangseffekten og retningen på strømstrømmen til omformeren. Funksjonaliteten og effektiviteten til simuleringsmodellen og maskinvareprototyperesultatene har blitt analysert og sammenlignet. Strømtap i maskinvareprototypen er estimert basert på effektresultatene fra resultatene samlet i laboratoriet.

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Listings

Acronyms

RMS Root-Mean-Square. 13

SDGs Sustainable Development Goals. 1

SPS Single Phase Shift. 3, 13, 25, 27, 53, 63, 64, 69

TRI Triangular. 13

ZCS Zero-Current-Switching. 13, 21

ZVS Zero-voltage-Switching. 21, 22, 58, 67

Chapter 1

Introduction

1.1 Background

The demand for sustainable energy has never been higher. Moreover, to reach the Sustainable Development Goals (SDGs)[8], more electrical power has to come from renewable energy sources such as wind and solar, which are mainly acquired through wind turbines and photovoltaic solar panels[22]. One major downside of these renewable energy resources is their fluctuating nature, as they cannot produce power on demand[22]. A standard solution to overcome this problem is to use energy storage in conjunction with renewable energy resources to maintain a smooth and continuous power flow to the load [16]. The most common and economical energy storage devices in the medium-power range are batteries and supercapacitors [3]. Whereas DC/AC converter is required to integrate the energy system into the power grid, a bidirectional DC/DC converter adjusts and regulates the voltage levels. Figure 1.1 shows an illustration of how these systems could be implemented into the power grid.
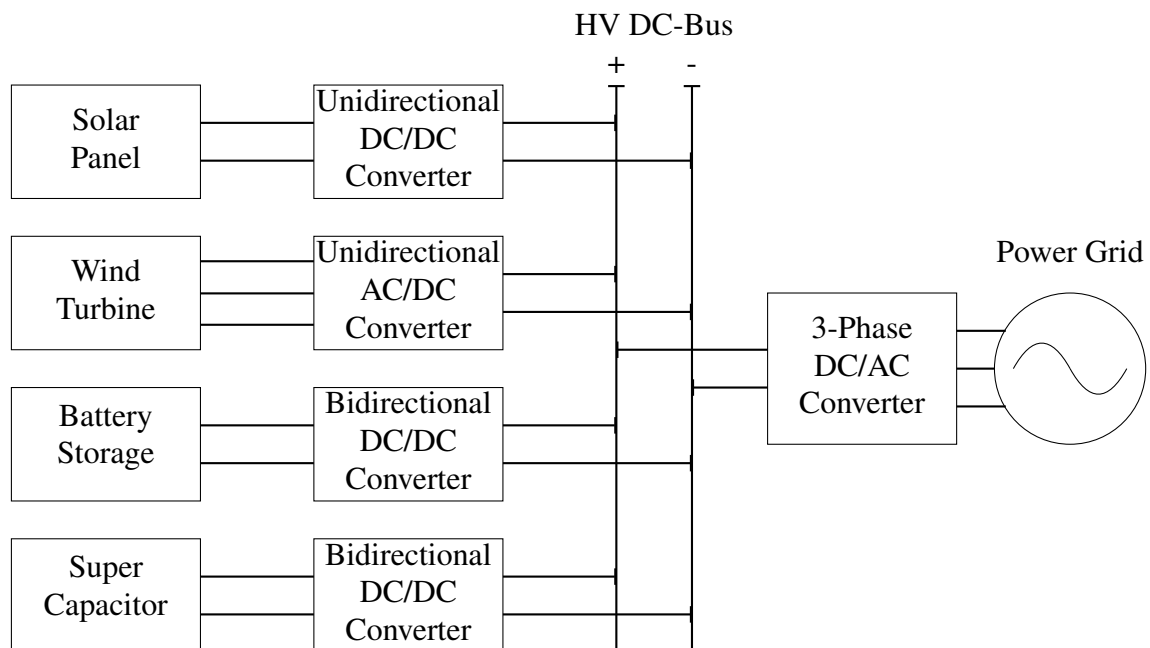
Figure 1.1: Illustration of High-voltage DC-bus implementation into the power grid

1.2 Previous Work

Bidirectional DC/DC converters and the Dual Active Bridge Converter are not new within the field of power electronics. Therefore, substantial research has been done to improve their efficiency, power density, and overall functionality. Some work has been done on bidirectional DC/DC converter here at Western Norway University of Applied Science, associated with the University of Bergen. Most recently, two theses were finalized in June of 2021;

- Bidirectional DC-DC Converter For Charging Batteries of Electric Vehicles By Fredrik Storebø [32]. This thesis presented the functionality and operation of an isolated bidirectional dc-dc converter for use with battery applications.

- DC-DC Converter for Supercapacitor as DC-bus Stabilization Element by Marius Reigstad [26]. This thesis presented an isolated bidirectional DC-DC converter simulation integrated with a supercapacitor model.

One aspect of this thesis which will be prevalent in the later chapter is the use of power modules, which recently have been developed at HVL. They have been designed by assistant prof. Eirik Haustveit and assistant prof. Vegard Steinsland, and assembled by Steffen Troy.

1.3 Stating the Problem

Power electronics systems such as converters are indispensable in the modern sustainable world, as they function as an enabling technology. Enabling energy sustainability through areas such as; harnessing energy from renewable sources, implementing energy storage, increasing efficiency of transmitting, and increasing efficiency of electricity consumption [22]. The Dual Active Bridge converter also referred to as a DAB converter, is a popular bidirectional DC/DC converter for medium to high power applications. Its design is ideal for energy storage applications because of its power density, cost, weight, galvanic isolation, high-voltage conversion ratio, and reliability [16]. However, the high complexity of control still offers more to be achieved regarding efficiency and power density.

When discussing and utilizing power electronic systems, high efficiency and high power density are the most central aspects. To make the overall system economically feasible, it needs to have as little energy loss as possible and a high energy density, reducing the size and weight of the application. The focus of this thesis is the efficiency of the DAB converter, which is the ratio of power output by the input power, as shown in eq. 1.1[22].

$$\eta = \frac{P_{out}}{P_{in}} \qquad \forall \qquad 0 \leq \eta \leq 1 \tag{1.1}$$

For the last decades, where computing power has increased exponentially, more academic research on power electronics has been done exclusively with simulation tools. Consequently, more complex ideas are presented and discussed solely by their mathematical principles and not realized through hardware prototypes. Prototypes with design-specific hardware are essential to validate the results from the domain-specific simulation tools, and this juxtaposition is crucial to confirm or deny the simulation and theoretical results.

1.4   Objective

This thesis aims to design and evaluate the use of a phase-shifted high switching frequency Dual Active Bridge converter, where galvanic isolation is achieved through a high-frequency transformer. A computer simulation and hardware prototype of the converter will be designed and evaluated using the same switching strategy to compare and analyze their functionality and efficiency.

- Develop a simulation in model in Matlab/Simulink of a DAB converter with single phase-shift modulation.

- Develop a hardware prototype of a DAB converter and implement single phase-shift modulation.

- Compare the simulation model's functionality, power transfer, and efficiency with the hardware prototype of the converter.

1.5   Structure

This thesis is organized into six chapters, introduction, theory, method, results, discussion and conclusion. Finally the the appendix presents supplementary information.

2. **Theory**: This chapter presents relevant theoretical principles regarding the thesis. The DAB converter's central elements and features that would help the reader will be explained. First, the working principles of bidirectional DC/DC converters are presented, including all the elements required to construct a DAB converter. The functionality of the DAB converter is the core of the chapter, with relevant theory on sections such as SPS (Single Phase Shift) modulation, power losses, and soft-switching. Lastly, the microcontroller and domain-specific software which have been utilized are introduced.

3. **Method**: This chapter will display how the simulation model in Matlab/Simulink and the hardware prototype of the DAB converter were designed. It starts with parameter selection and design of the high-frequency transformer. Then the simulation model is presented with its associated source code. Next, the microcontroller, which is responsible for the operation and signal creation for the hardware converter prototype, is described. Then the following section presents the complete design of the hardware prototype of the converter, including the interface card design, integration of the power modules, and component selection. Finally, the laboratory test setup for the DAB converter is presented and explained.

4. **Results**: This chapter displays all the results gathered throughout the thesis. Results from the Matlab/Simulink simulation model and the hardware prototype of the DAB converter are presented beside each other to highlight their functionality with SPS modulation and bidirectional power flow. Then more power-specific results are showcased, such as output voltage levels and efficiency.

5. **Discussion**: In this chapter, the results from the simulation model and the hardware prototype are analyzed and discussed. Efficiencies from different configurations are compared, power losses are estimated, and the limits of the converter are examined.

6. **Conclusion**: This chapter summarizes the thesis and highlights the paper's main findings

and relevant discussions.

- **Appendix**: The appendix includes extensive information which was termed unnecessary to present in the main body of the paper.

    A Submodels from the Matlab/Simulink model.

    B Schematics and PCB layout

    C Datasheets of essential components.

    D Source code.

    E Laboratory test Equipment.

    F Supplementary results.

Chapter 2

Theory

This chapter presents the relevant theory and domain-specific software tools for this thesis. First, an overview of the operation of DC/DC converters, focusing on bidirectional power flow and the systems required for such operations are presented in 2.1. Then in section 2.2, a detailed description of the dual active bridge converter is presented, including its topology, working principles, and single phase shift modulation. The power losses related to the DAB converter are presented in section 2.3, before zero-voltage switching are explained in section 2.4. Finally, the software and microcontroller used in the project are introduced in section 2.5.

2.1 Bidirectional DC/DC Power Converter

Power converters are the systems for changing electrical energy from one form to another. A DC-to-DC converter is responsible for either stepping opp or down a DC (Direct Current) input voltage to a regulated DC (Direct Current) output voltage. As presented in chapter 1, several power electronics applications used in energy sustainability, such as harnessing solar and wind energy and energy storage, require a DC/DC converter[13]. As the name implies, a bidirectional converter can transfer power in both directions of the converter and is therefore suitable for energy storage applications to charge and discharge the stored energy [22]. The same operation could be accomplished by using two unidirectional converters. However, this world significantly increases the size of the converter system[16].
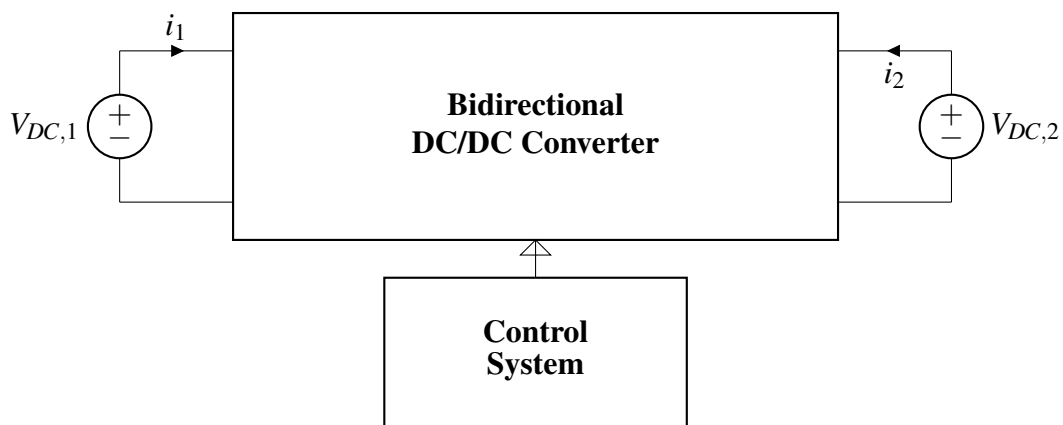
Figure 2.1: Bidirectional DC/DC converter system

Figure 2.1 shows a representation of a bidirectional DC/DC converter where the power flow can either be from $V_{DC,1}$ to $V_{DC,2}$ or vise versa. Which of these two modes the converter operates in is determined by controlling a set of electrical switches and is often referred to as either "forward" or "backward" mode[16]. The converters are generally divided into two groups of configuration, either non-isolated or isolated [13].

2.1.1 Non-Isolated Bidirectional DC/DC Converter

A NBDC (Non-isolated bidirectional DC/DC) converter transfers the power without any electrical separation between each power side. This topology reduces the overall dimensions of the converter compared with its isolated counterpart and is, therefore, more suitable for applications where size and weight are a considerable concern[16]. The NBDC converters are also not influenced negatively by EMI (Electromagnetic Interference) since they do not require any magnetic components. EMI introduces electromagnetic fields, which can hinder communication systems in the circuit and may prevent electronic equipment from functioning efficiently[18]. On the other hand, this structure becomes impractical since it is difficult to achieve high voltage conversion ratios in such converters, which can be achieved with a transformer [29].

2.1.2 Isolated Bidirectional DC/DC Converter

An IBDC (isolated bidirectional DC/DC) converter consists of electrical separation between the primary and secondary sides, and is often referred to as galvanic isolation. Galvanic isolation is a means of preventing DC and unwanted AC currents between two parts of a system while allowing signal and power transfer between the two parts[16]. The result is a extra level of security now that each side has its ground reference, limiting the interference each side will have on the other. Personal safety and the protection of sensitive loads are often required in electrical systems, and hence isolation in converters is often mandatory[16]. The most utilized way of achieving isolation is through a magnetic transformer. The transformer also offers another degree of freedom to the voltage gain, simply by the number of winding turns on each side, which will further be discussed in section 2.1.5.
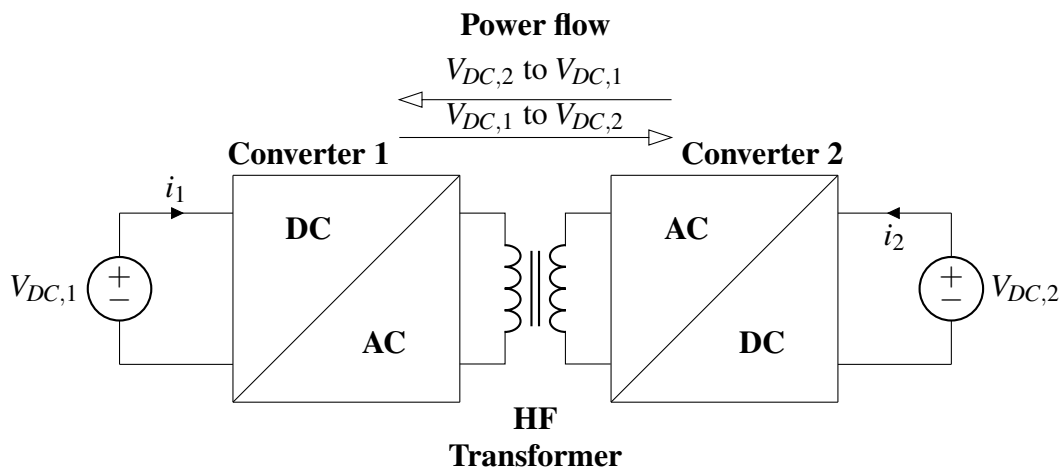
Figure 2.2: Outline of an IBDC with power flow indications

Using transformers in a DC/DC converter system increases the complexity of the converter.

It is necessary for the topology to convert the signal from DC to AC and back to DC after it has passed through the transformer since a transformer can only transfer power in the form of AC[22][2]. The conversion is achieved using electrical switches and referred to as a rectifier of the conversion is from AC to DC, and an inverter if it is from DC to AC. Both conversions can be achieved through the same physical structure and determined by the operation of the electrical switches.

2.1.3 Inverter and Rectifier

Whereas the DC/DC converter is utilized to step up or down the amplitude of a DC signal, inverters' and rectifiers' function is to change the form of the signal, either from DC (Direct Current) to AC (Alternating Current) or vice versa [22]. An IBDC converter consists of two power converters, where both must function as either an inverter or rectifier, dependent on which mode the IBDC converter operates in, as shown in figure 2.2. This mirrored topology is one of the reasons that a full-bridge topology is often used for IBDC converters[1].

Full bridge topology

A full bridge topology uses four electrical switches (Q_{1-4}), as shown in figure 2.3, and is controlled either with bi-polar or uni-polar voltage switching. Bi-polar switching uses two complementary PWM (Pulse With Modulation) signals to control one high side and the low side transistor on each leg of the bridge. Hence the two signals are referred to as S14 and S23. With bi-polar switching, the output voltage will vary between $+V_{DC}$ and $-V_{DC}$ determined by which of the two sets of transistors are on. Uni-polar switching can control the high side transistors separately and can therefore also reach an output voltage level of zero, as well as $+V_{DC}$ and $-V_{DC}$.

A disadvantage of using the full bridge topology is that the driver circuit becomes even more complex since four switches need to be controlled at any given time. Because of the high number of electrical switches, these converters are primarily utilized in advanced high power systems[13]. Most of the losses in a bride circuit are the switching losses. However, the topology offers substantially better efficiencies than alternative typologies, especially when utilizing soft switching, which is presented later in section 2.4.
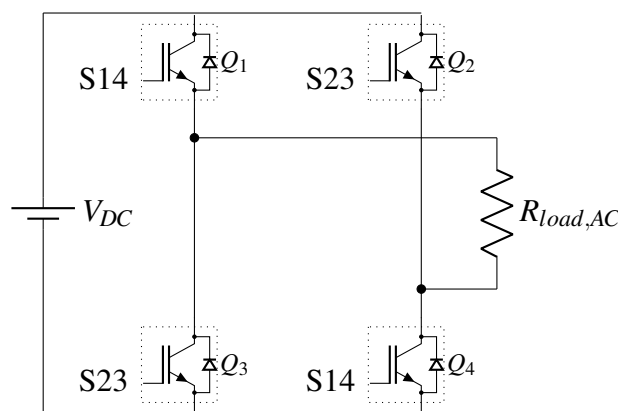
Figure 2.3: Full bridge inverter with bi-polar voltage switching

Dead-time

A crucial aspect when using a full bridge configuration is implementing dead-time between each leg of the bridge. The two sets of switches turn on or off momentarily in an ideal full bridge operation. However, these switches use a small amount of time for this operation which causes a window where both transistors in the same leg are on. This can cause a shoot-through current where the current flows directly to ground and bypasses the load [20]. This phenomenon would most likely destroy the transistors if not terminated immediately. Therefore a short period is implemented where all four switches are off simultaneously and referred to as the dead-time[22].

2.1.4   Power transistors

Power transistors function as electrical switches and are the building blocks of all electronics. They consist of semiconducting material, which allows them to be either conductors or insulators, decided by an external signal [22]. For most power converters that require high frequencies, the choice of power transistors falls on either MOSFETs or IGBTs because of their rapid switching capabilities. MOSFETs can turn on and off the fastest and is therefore utilized in application with the highest frequencies. IGBTs have better on-state characteristics because they can utilize conductivity modulation, which reduces on-state losses [24], and hence have better overall efficiency.

2.1.5   High-frequency transformer

The high-frequency transformer is an essential piece of equipment in IBDC converters and is the conventional method to realize galvanic isolation. The transformer should achieve this while transferring the power as efficiently and instantaneously as possible [33]. The reason that the HF transformer is considered superior to a low-frequency transformer in power converters is that for any given power rating, the higher the frequency, the smaller the transformer and filter components can be, which severely reduces the overall size of the converters [22].

Energy Transfer

Transformers transfer energy by means of electromagnetic induction and consist of a magnetic core and two independent windings (primary and secondary)[24]. An ideal transformer should not store any energy, and the energy is transferred instantaneously from one side to the other. In practice, there is energy stored in two areas; leakage inductance (L_K) which is the energy stored in the non-magnetic regions of the transformer, and mutual inductance (L_M) which represents energy stored in the finite permeability of the magnetic core[33]. Transformers consist of two tightly coupled winding where almost all of the flux produced by one winding links to the other winding[22].
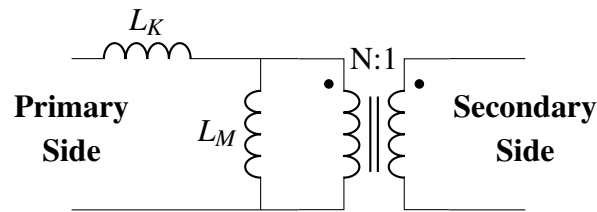
Figure 2.4: Transformer equivalent with leakage and mutual inductance

Design considerations

Transformer design is a central part of power electronics and is yet another converter aspect that can be adapted and designed for optimal power transfer. In a power supply design, transformers and inductors are significant contributors to size, and increasing the operating frequency reduces their size. However, increasing the switching frequency will increase the hysteresis and eddy current losses in the core of the transformer, as well as the winding losses[33]. Skin effect is an important consideration when designing an HF transformer. At high frequencies, the current through the copper winding is "pushed" to the surface of the conductor; and consequently, a smaller effective current-carrying cross-section area is utilized[30][15].

The material used for the magnetic core in the transformer (iron, ferrite, etc.) has a specific characteristic called saturation flux density. As the current through the windings increases, the magnetic field intensity also increases[24]. Saturation is the maximum value of flux density the material can reach. It occurs when the applied ampere-turns generate more magnetic flux than the core can handle[33].

2.2 Dual Active Bridge Converter

The DAB (Dual Active Bridge) is a bidirectional DC/DC converter with galvanic isolation from a high-frequency transformer. It was first introduced in the paper [7], by R.W. De Doncke in 1988. Following this introduction, several papers were published based on the performance of the high-power-density DC-to-DC converter with single-phase dual active bridge topology[17]. The converter had desirable features such as low device and component stresses, small filter components, low switching losses, high-power density, high efficiency, and the ability to operate with bidirectional power flow [17]. These features raptly established the DAB converter as one of the most popular IBDC converters for medium to high power applications and one of the preferred converters for energy storage applications [6]. The DAB utilizes eight controllable power transistors, which require a particular focus on the control and design of the converter to overcome the disadvantages such as switching losses [13].

2.2.1 Topology

The DAB converter topology consists of identical primary and secondary sides, isolated by a high-frequency transformer as shown in figure 2.5. Each side comprises four transistors in a full-bridge topology and a DC-link capacitor. Due to the symmetry of the converter, it is capable of bidirectional power flow and, therefore often selected for energy storage applications[12]. The DAB can also function with half-bridges and push-pull typologies. However, a full bridge allows for the best converter utilization due to that only this topology can generate zero output voltage and therefore enables the use of improved modulation schemes with soft-switching, which is critical for high-efficiency[19].
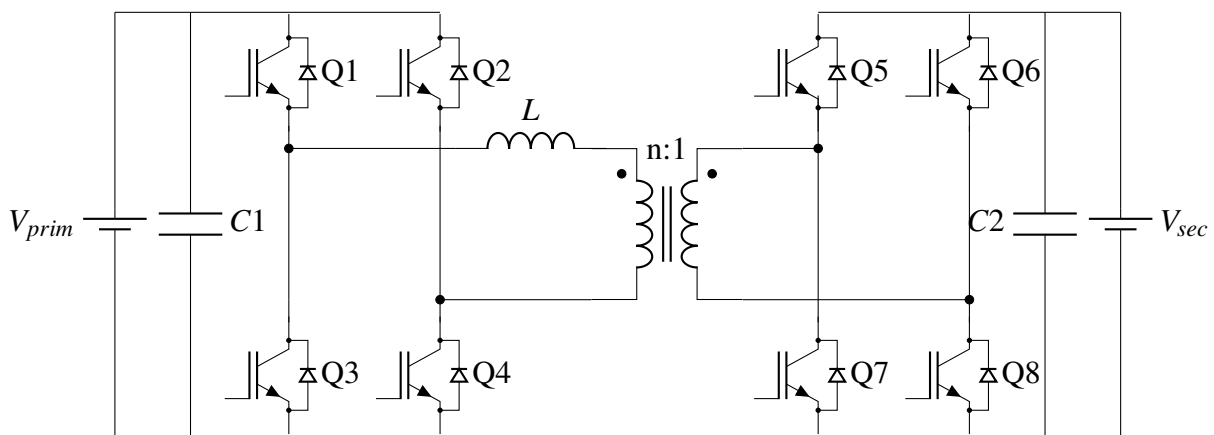
Figure 2.5: Basic topology of a Dual Active Bridge Converter

In figure 2.5, V_{prim} and V_{sec} represents the primary and secondary DC bus-link of the converter. The inductor (L) is the sum of leakage inductance in the transformer and external inductance necessary for substantial energy transfer. The inductor can be placed on either side of the transformer, but it is positioned on the high-voltage side in most applications due to the lower occurring current[19]. Q1 through Q8 are the transistors that work as controllable electrical switches in the converter to form the two full bridge configurations.

2.2.2 Working Principles

A few working principles govern the functionality of the DAB, such as how power can flow between two AC sources, which enables the use of a transformer, and secondly, how AC signals are generated in the form of square waves from stable DC sources.

Power flow between two AC sources

As stated several times in this thesis, the DAB converter is a DC to DC converter that utilizes AC power to transfer energy from one source to another though a transformer. These principles will be explained in more detail to understand how energy can be transferred and how the direction of the power flow is changed by controlling the phase between the two sources. The starting point for this is the AC power flow between the two sources V_1 And V_2 through an inductor as shown in figure 2.6, where θ_1 and θ_2 represent the phases of each source.
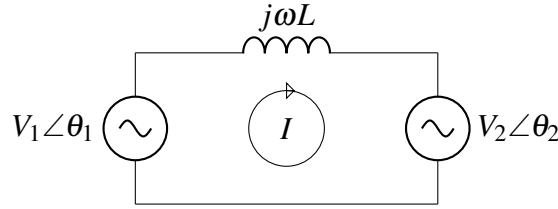
Figure 2.6: circuit of power flow between two AC sources

The average power transferred from one source to the other is determined by the current loop in figure 2.6 which is represented by a phasor in eq. 2.1

$$\bar{I} = \frac{V_1 \angle \theta_1 - V_2 \angle \theta_2}{j\omega L} \tag{2.1}$$

From there, current can be represented in the time domain with reference to V_1, such that $\theta_1 = 0$ and consequently the phase between the sources is θ_2. The current can then be represented in the time domain as shown in eq. 2.2

$$I(t) = \frac{V_1}{\omega L} sin(\omega t) - \frac{V_2}{\omega L} sin(\omega t - \theta_2) \tag{2.2}$$

The power on the secondary side can therefore be expressed as eq. 2.3 as a result of Joule's Law [24].

$$P_2(t) = V_2(t) \cdot I(t) = V_2 \cdot cos(\omega t - \theta_2)[\frac{V_1}{\omega L} Sin(\omega t) - \frac{V_2}{\omega L} Sin(\omega t - \theta_2)] \tag{2.3}$$

Averaging the power over one period, represented as Ts, results in a much simpler equation and is left with eq. 2.4, which after some mathematical manipulations yields eq. 2.5.

$$P_{2,average} = \frac{1}{T_S} \int_0^{T_S} P_2(t) dt \tag{2.4}$$

$$P_{2,sine} = \frac{V_1 V_2}{\omega L} Sin\theta_2 \tag{2.5}$$

This representation concludes that the phase (θ_2) governs power flow in this topology, such that if θ_2 is positive, then energy will flow from V_1 to V_2. If θ_2 is negative, power flows in the opposite direction. This power transfer is only possible because of the inductance between the two sources. Power transfer in a DAB converter occurs in a similar manner where the AC signals are two high-frequency square waves are created in the primary and secondary full bridge on each side of the transformer. Eq. 2.5 describes the power flow between two sine wave sources[27]. The DAB converter utilizes square waves instead of sine waves, but the same principles are at work.

$$\left| \begin{array}{ll} \theta_2 > 0 \rightarrow & \text{Power flow from } V_1 \text{ to } V_2 \\ \theta_2 < 0 \rightarrow & \text{Power flow from } V_2 \text{ to } V_1 \end{array} \right.$$

Table 2.1: Power flow between two AC sources

Two active bridges and a transformer

Including a transformer ensures the galvanic isolation between the two sides and introduces leakage inductance, which is prevalent in the transformer. This inductance can now represent the energy inductance required for the AC power energy transfer. However, if the inductance is insufficient, an inductor is placed in series with the transformer. The transformer also introduces turn ratio of the winding as a value of n, shown in Eq. 2.6.

$$n = \frac{V_{prim}}{V_{sec}} \tag{2.6}$$

As the name of the converter implies, the DAB consists of the two active bridges, which referees to a controllable full bridge as presented in section 2.1.3. Their function is to generate two complementary high-frequency square waves, which can be phase-shifted with respect to each other. The frequency of the two AC signals results from the switching frequency of the two full bridges and is therefore often referred to as the switching frequency.
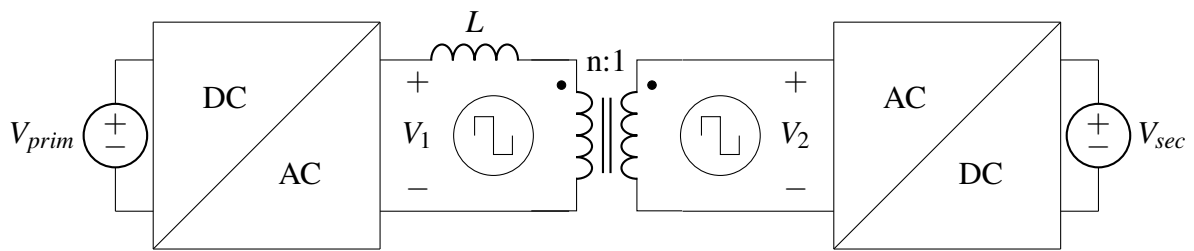
Figure 2.7: Basic structure of the bidirectional dual active bridge converter

Figure 2.7 is an equivalent system of the dual active bridge which will be used to derive the final power equation for the converter. V_1 and V_2 are the voltages of the two high-frequency square waves, which have been inverted by the two DC buses, V_{prim} and V_{sec}, respectively. The ultimate voltage and current over the inductor govern the power flow in the converter, and the inductance, represented by L, is the sum of leakage inductance in the transformer and any external series inductance. The concept is that applied square waves to the bridges create a voltage differential across the energy transfer inductance and direct its stored energy.

2.2.3   Single Phase Shift Modulation

The DAB converter has a simplistic topology, although the high number of controllable switches requires a strategy to govern the phase shift ratio between the two square waves and hence the power flow of the converter. The switching strategies are called PSM (Phase Shift Modulation) techniques and are how the two AC signals and phase shift are used to transfer the power, and adjust the voltage levels. Subsequently, the modulation techniques' objectives is to reduce power losses while maintaining a smooth output signal.

The most simplistic and common modulation technique used in the DAB converter is the SPS (Single Phase Shift) modulation. It consists of two complementary square waves where both constantly have a 50% duty-cycle and constant switching frequency. SPS modulation has the highest achievable power flow of the modulation techniques, however, it has two notable drawbacks. Firstly, it encounters a high RMS transformer current, hence larger conduction losses, and secondly, a limited operating range where it can utilize zero voltage switching [28]. Nevertheless, SPS modulation is the PSM technique that is most straightforward to implement and therefore selected for this project. Similarly, as eq. 2.5 was determined in section 2.2.2, the average output value of two square waves instead of sine waves can be shown as in eq. 2.7. V_1 and V_2 are the voltage levels of the two square waves, both operations with a switching frequency of f_{sw}, and phase-shifted to each other by δ.

$$P_{2,sqaure} = \frac{V_1 \cdot V_2}{2 \cdot \pi^2 \cdot f_{sw} \cdot L} \delta(\pi - \delta) \qquad \forall \qquad -\frac{\pi}{2} \leq \delta \leq \frac{\pi}{2} \tag{2.7}$$

Other modulation techniques

The more complex modulation techniques are used to further reduce the power losses and increase the soft-switching operating range[19]. Two other modulation techniques are presented below. Dual-phase shift which is an extension of the Single phase shift, and Triangular modulation which employs duty-cycle variations.

- DPS (Dual-Phase Shift) modulation uses two-phase shift ratios. One phase shift ratio between the primary and secondary side of the transformer, just as SPS modulation, and one phase shift ratio between the gate signals of the diagonal devices on one of the bridges. DPS modulation can effectively reduce current stress and broaden the range of soft switching[5]. This increase in operational freedom does increase the complicity of the operation. The power transfer is equal to SPS modulation and presented in eq. 2.20.

- TRI (Triangular) modulation utilizes uni-polar switching on both full bridges, as mentioned in 2.1.3. The result is a three-level switched voltage waveform with duty cycle modulation. This modulation technique can utilize Zero-Current-Switching and have a reduced RMS transformer current. However, this modulation has limited achievable power flow, and calculated as shown in eq. 2.8[11]

$$P_{max}^{tri} = \frac{n^2 V_2^2 (V_1 - nV_2)}{4 f_{sw} L_{tot} V_1} \tag{2.8}$$

Gate signals for single phase shift modulation

The two bridges are operated by eight switching signals, which control the transistors Q_{1-8}, shown in figure 2.5. The transistors are divided into pairs that operate with the same switching cycles and in complementary modes for the full bridge configuration. These pairs are; Q14 and Q23 on the primary bridge and Q58 and Q67 on the secondary bridge. They all operate with a 50% duty cycle with a cycle period of T_S, which can be calculated from the switching frequency as shown in Eq. 2.9. Figure 2.8 shows a representation of the four gate signals where δ is the phase shift between the two bridges.

$$T_s = \frac{1}{f_{sw}} \tag{2.9}$$
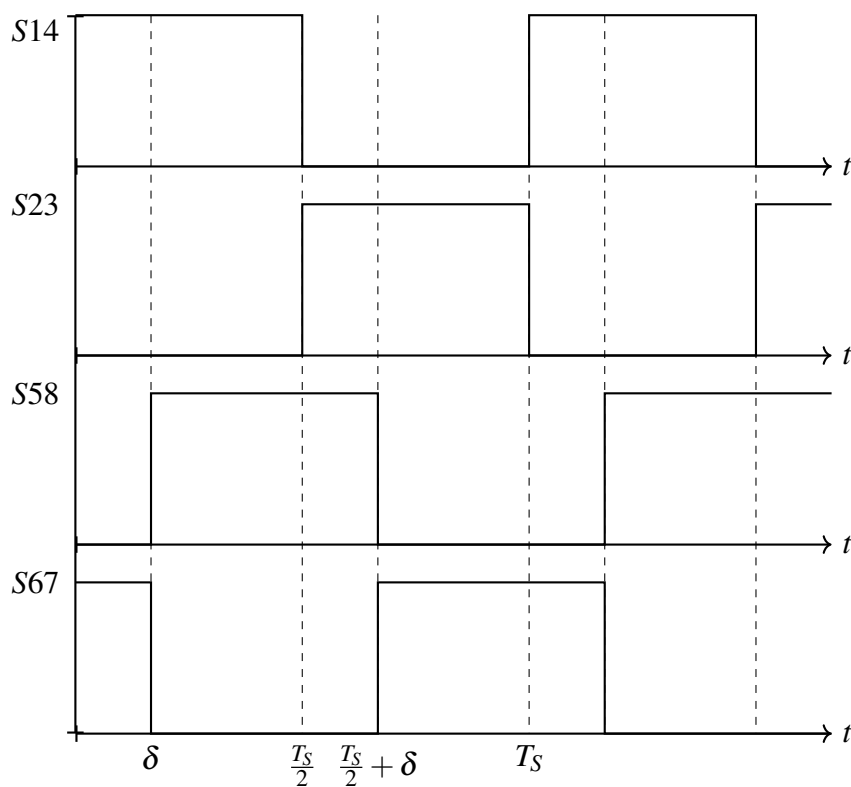
Figure 2.8: Gate signals for SPS modulation

Inductor characteristics

It is the current though the inductor which governs the power flow in the converter and is a result of the two voltages V_1 and V_2, where δ is the phase shift between them and are a result of the switching sequence from figure 2.8. The inductor voltage is a function of the rate of current change through it and its self-inductance[22], expressed in eq. 2.10. The dynamics over the inductor, V_L, can therefore be divided into four intervals according to the values of V_1 and V_2 as shown in figure 2.9, and mathematically described in eq. 2.11.

$$L\frac{di_L(t)}{dt} = V_L(t) \tag{2.10}$$

$$L\frac{di_L(t)}{dt} = V_1(t) - V_2(t) \qquad \forall \qquad 0 < t < \frac{T_S}{2} \tag{2.11}$$
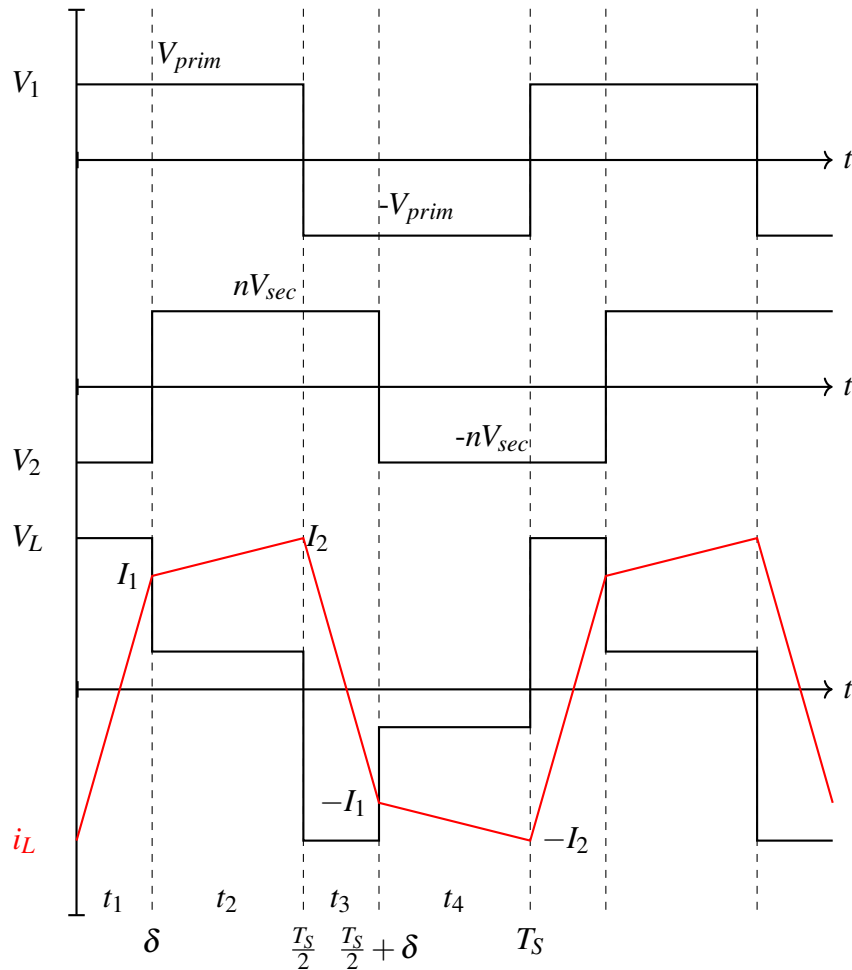
Figure 2.9: A representation of the waveforms using SPS modulation in the DAB converter

Furthermore, the symmetry in the inductor current waveform allows for power flow analysis to be developed only using one half switching period, $\frac{T_s}{2}$. Hence divided into only two intervals, one before the phase shift and one after, resulting in eq. 2.12 and eq.2.13.

$$L\frac{I_1 + I_2}{\delta} = V_{prim} + nV_{sec} \qquad \forall \qquad 0 \leq t \leq \delta \qquad (2.12)$$

$$L\frac{I_2 - I_1}{\frac{T_S}{2} - \delta} = V_{prim} - nV_{sec} \qquad \forall \qquad \delta \leq t \leq \frac{T_S}{2} \qquad (2.13)$$

There are two sets of instantaneous inductor current values, I_1 and I_2, and occur when V_1 and V_2 change their polarity from negative to positive. This is shown in figure 2.9 and are calculated by solving for the currents in eq. 2.12 and eq. 2.13. These values are important when estimating losses in the converter in section 2.3 as they are the highest values of the inductor current.

$$I_1 = \frac{(V_{prim} + nV_{sec})\delta - (V_{prim} - nV_{sec})(\frac{T_S}{2} - \delta)}{2 \cdot L} \qquad (2.14)$$

$$I_2 = \frac{(V_{prim} + nV_{sec})\delta + (V_{prim} - nV_{sec})(\frac{T_S}{2} - \delta)}{2 \cdot L} \qquad (2.15)$$

Power values on the secondary side

Since the output values can be indicated from which directing the power flows in the bidirectional converter. This representation of the output values presents the values on the secondary side, referring to figure 2.5. The output current is the rectified waveform of the inductor current and is shown in figure 2.10. The average of the output current is the outcome of taking the integral over one-half cycle ($\frac{T_s}{2}$) of the waveform, which results in eq. 2.16.
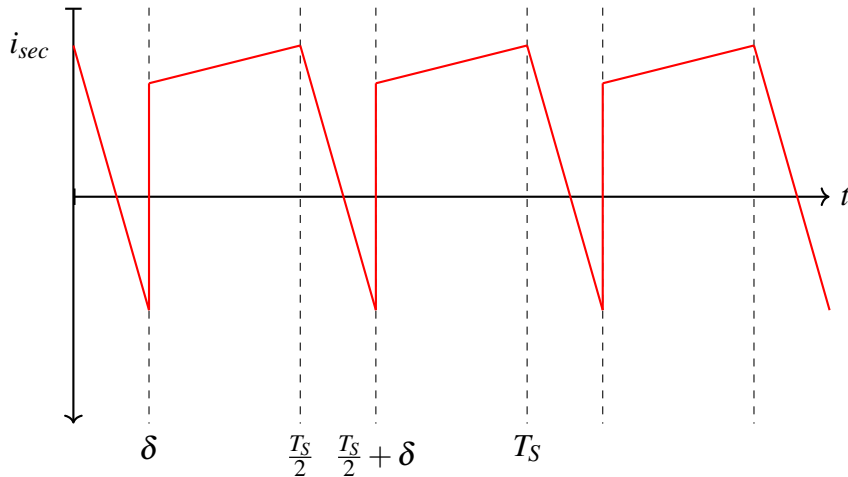
Figure 2.10: Output current

$$I_{sec} = \frac{nV_{prim}}{L \cdot F_{sw}}\delta(1 - \frac{\delta}{T_S/2}) \qquad \forall \qquad -\frac{\pi}{2} \leq \delta \leq \frac{\pi}{2} \qquad (2.16)$$

$$P_{out} = \frac{V_{sec}}{I_{sec}} \tag{2.17}$$

To simplify, the phase-shift variable, D, is introduced in eq. 2.18. Combining this with eq. 2.17 results in the output power as a function of the voltage on the primary and secondary sides, and the phase shift variable in eq. 2.19

$$D = \frac{\delta}{T_s/2} \tag{2.18}$$

$$P_{out} = \frac{n \cdot V_{sec} \cdot V_{prim}}{2 \cdot L \cdot f_{sw}} D(1-D) \qquad \forall \qquad -0.5 \leq D \leq 0.5 \tag{2.19}$$

The maximum power transferred can then be derived from the fact that the larges phase shift is when $|D| = 0.5$, hence eq. 2.20

$$P_{max} = \frac{n \cdot V_{sec} \cdot V_{prim}}{8 \cdot L \cdot f_{sw}} \tag{2.20}$$

The phase shift for any required power transfer less than maximum is possible to achieve by rearranging eq. 2.19 and is given in 2.21 solving for the phase shift value.

$$D = \frac{1}{2}(1 - \sqrt{1 - \frac{8 \cdot f_{sw} \cdot L \cdot |P|}{n \cdot V_{prim} \cdot V_{sec}}}) \qquad \forall \qquad P < |P_{MAX}| \tag{2.21}$$
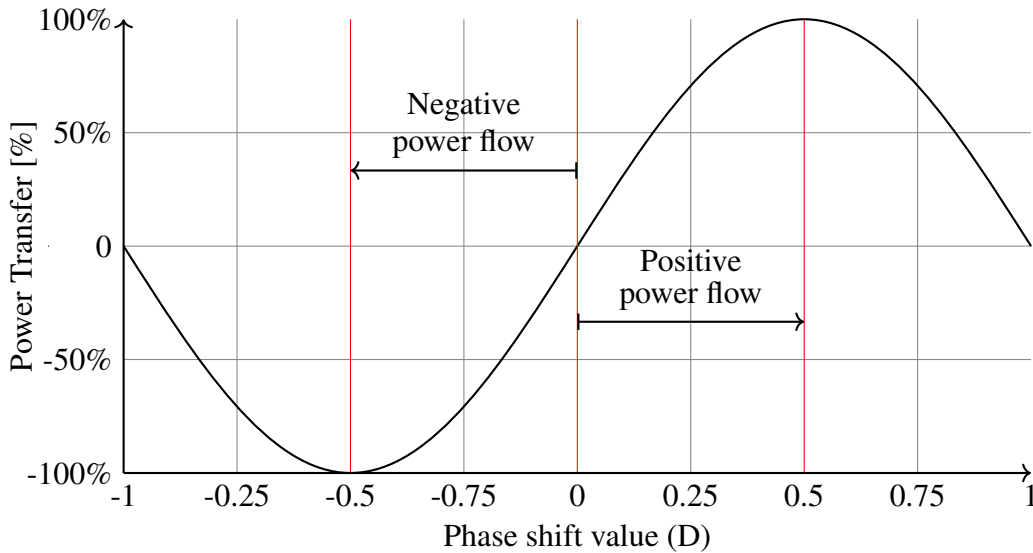
Figure 2.11: Power transfer characteristics according to phase-shift value

2.3   Power Losses

This section will present the most dominant power losses in the DAB converter. Power losses are the unwanted electric energy that is dissipated in the circuit when operating and is one of the main concerns when designing any power converter. In the DAB converter the losses can be classified into three categories; switching losses [34], conduction losses[1] and magnetic losses[25].

Heat is a significant concern for electrical and magnetic components, and their operating temperature is often the limiting factor set by the manufacturer. If the temperature of essential components becomes too high, the efficiency will descend rapidly and break down entirely in the worst case[25]. The following equations assume that the components operate within their temperature limits and are cooled by a heat sink if necessary.

2.3.1   Switching Losses

Switching losses occur in each of the eight transistors when they transition from one state to another, either when they turn on or turn off [9]. Therefore, the losses depend on the DAB converter's type of semiconductor device. As mentioned in section 2.1.4, the standard transistor used in these power converters are either MOSFETs or IGBTs and in this project, all the transistors are IGBTs. During switching, each transistor is exposed to voltage and current simultaneously, resulting in power dissipation, and referred to as switching losses. The waveform in figure 2.12 is a simplified view of the switching transient of one transistor for both turn-on and turn-off.
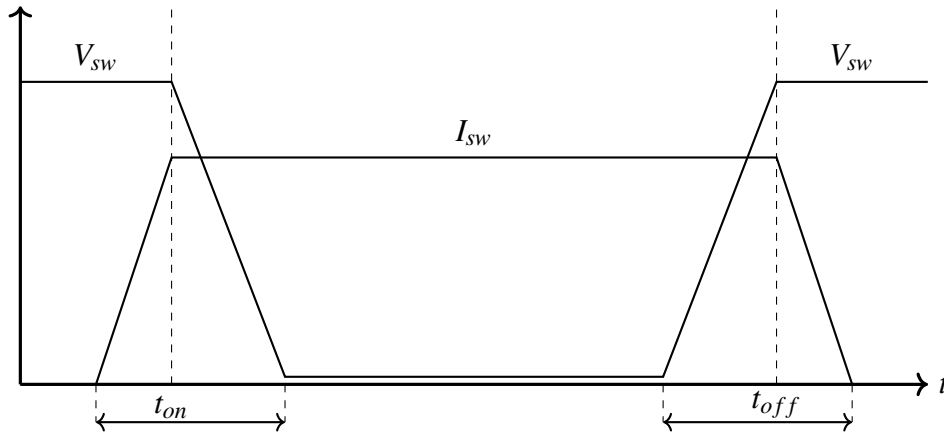
Figure 2.12: Simplified waveforms of switch turn-on and turn-off transient

Switching losses over one transistor for one switching transient is calculated using eq. 2.22,

$$P_{sw} = \frac{1}{2} \cdot V_{sw} \cdot I_{sw} \cdot (t_{on} + t_{off}) \cdot f_{sw} \tag{2.22}$$

where V_{sw} and I_{sw} is the voltage and current over the transistor during switching, with reference from collector to emitter. The time intervals t_{on} and t_{off} are the time for the transistor to turn ON and OFF, which is detailed in the datasheet of the transistor. Finally, the switching frequency that the transistors are operating with is f_{sw}

These values can further be determined from the transistor on each bridge, determined from the switching waveforms in figure 2.8 and 2.9 as well as the topology in figure 2.5. The

voltages over the transistors is V_{prim} on the primary, and V_{sec} on the secondary bridge. The current during the switching sequence will on the primary side be I_2, and in the secondary bridge at I_1/n. eq. 2.22 can be further derived to calculate the switching losses in the DAB converter with voltages and currents already determined, as shown in 2.23. These calculations are derived from [34] and [1].

$$P_{sw,total} = 2 \cdot (V_{prim} \cdot I_2 + V_{sec} \cdot \frac{I_1}{n}) \cdot (t_{on} + t_{off}) \cdot f_{sw} \tag{2.23}$$

2.3.2 Conduction Losses

Conduction losses are the continuous losses when the transistor is conducting. Also referred to as the on-state losses, these are losses related to the internal resistance of the transistors as well as the voltage drop across the anti-parallel diode. These calculations are derived from [1] and [12] where the losses over the switch can be calculated from eq. 2.24 and over the diode in eq. 2.25.

$$P_{con,sw} = I_{sw,rms}^2 \cdot R_{sw,on} \tag{2.24}$$

$$P_{con,diode} = I_{diode,rms} \cdot V_{diode} \tag{2.25}$$

The value $R_{sw,on}$ is the average on-state ohmic resistance over the transistor, and V_{diode} is the forward voltage drop over the anti-parallel diode. The two currents $I_{sw,rms}$ and $I_{diode,rms}$ are the RMS currents through and calculated from the inductor current waveform 2.9. Both the currents are estimated using 2.26 and 2.27 from the currents over the inductor in 2.14 and 2.15. I_0 is the instantaneous current at the end of the dead-time interval 2.13, and depends on the driver circuit for the transistors.
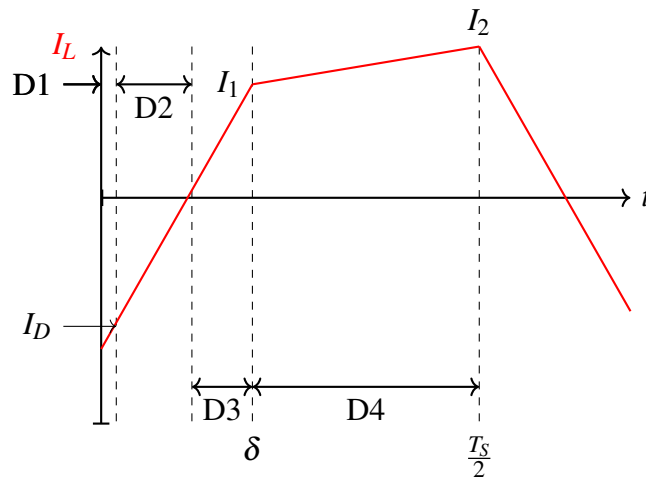
Figure 2.13: Conduction time intervals of the inductor current

D_1 is the time interval of the dead-time from the switching

$$I_{D,rms} = \sqrt{\frac{D_1}{3}(I_0^2 + I_0 \cdot I_1 + I_1^2)} \tag{2.26}$$

$$I_{sw,rms} = \sqrt{\frac{D_2}{3} + I_1^2 \frac{D_3}{3} I_\delta^2 + \frac{D_4}{3}(I_0^2 + I_0 \cdot I_1 + I_1^2)} \tag{2.27}$$

2.3.3 Magnetic Losses

Magnetic losses include all power losses related to the high-frequency transformer and the series inductor in the converter. The losses have been divided into two subsequent categories; core losses and copper losses. The magnetizing current plays only a minor role in the transformer losses[25]. The inductor is also a magnetic component which will experience losses[23].

Core losses

Core losses in a transformer occur because of the alternating magnetic flux in the core and combine hysteresis loss and eddy current losses. These values can be measured for a given core and calculated using Steinmetz's equation[35]. However, typically the core losses are estimated using the product of core loss per unit of volume P_v, and the core volume V_E shown in eq. 2.28. These values are given in the datasheet of the core material[25].

$$P_{core,loss} = P_v \cdot V_E \tag{2.28}$$

Copper losses

Copper losses or winding losses are the heat losses in the windings because of their ohmic resistance[25]. The copper losses from inductors can be calculated in the same fashion using the ohmic resistance from the indicator winding [23].

$$P_{copper,loss} = I_{prim\ rms}^2 \cdot R_{prim} + I_{sec\ rms}^2 \cdot R_{sec} \tag{2.29}$$

2.4   Zero Voltage Switching

A important advantage of the DAB converter is its natural capability of soft switching in the form of ZVS (Zero-voltage-Switching). In the first adaptation of the DAB converter in 1991, soft switching was prevalent and paramount factor to minimize losses. The converter is shown to be suitable for high power-density high power applications, and while operating with soft-switching, the converter can have a decrease in power losses at high switching frequency[7]. Hence, reducing the weight and size of the converter while maintaining a high power density. Soft-switching is realized by forcing either the current or voltage to zero while the switching of the transistors occurs.

In the previous section 2.3, it was presented that a major part of the losses in the DAB converter or any other bridge converter is the switching losses, primarily because of the high switching frequencies that this converter operates on. The switching transient that was shown in figure 2.12 presents the overlapping voltage and current values at the moment when the switching occurs. This situation is what is referred to as hard-switching [24]. Forcing either the voltage or the current to zero at this moment will result in the elimination of the switching power losses for that switch. This occurrence is referred to as either ZVS or ZCS, depending on which value is forced to zero. All switches in the DAB converter may work in ZVS, or ZCS [21]. However, ZCS is achieved through control and therefore prevents the use of phase-shift modulation, while ZVS is achieved through topology.

2.4.1   ZVS in a DAB Converter

How ZVS occurs in the DAB converter is describes in detail in [25] and analyzed in [10] and [31]. The principle of the natural ZVS phenomenon of the converter comes from the fact that there is a short dead-time where the inductor-stored energy discharges the output capacitance in the transistors. The result is that voltage over the transistors is held close to zero before they are turned on.

The critical detail is that each transistor consists of an anti-parallel diode and a capacitor. The transistors is defined as Q_{1-8} according to figure 2.5, and the time intervals as t_{1-4}, according to figure 2.12. Figures for this is shown in [25].

At the switching instance from t_1 to t_2, Q_1 and Q_2 continue to conduct wheres Q_6 and Q_7 turn off, and Q_6 and Q_6 turn on. At this moment, there is a time period where all four Q_{5-8} are off, and the energy stored in the inductor circulates current, which discharges the capacitors across Q_5 and Q_8 to zero, and charges the capacitors across Q_6 and Q_7 to V_{sec}. After these capacitors have been charged and discharged, the current will continue to flow through the anti-parallel diode in Q_5 and Q_8, and the voltage across these transistors will be clamped to zero. They then turn on with zero voltage which can drastically reduce the switching losses.

The same event occur at the switching period from t_2 to t_3, where Q_1 and Q_2 turn-off while Q_2 and Q_3. Hence, Q_2 and Q_3 turn-on with ZVS.

Energy required for ZVS

The energy stored in the series inductor can be expressed in eq. 2.30, which will then charge and discharge the capacitive energy in the transistor as expressed in eq. 2.31.

$$E_L = \frac{1}{2}LI_L^2 \tag{2.30}$$

$$E_C = \frac{1}{2}C_T V_T^2 \tag{2.31}$$

Here C_T is the output capacitance of the transistor and found in the datasheet, and V_T indicated the voltage over the transistor. By combining eq. 2.30 an eq. 2.31, the minimum inductor current required to achieve soft switching is expressed in eq. 2.32.

$$I_{l,min} = \sqrt{\frac{C_T V_T^2}{L}} \tag{2.32}$$

Voltage ratio to achieve ZVS

One of the conditions for ZVS to occur in both bridges in the DAB is that I_1 is equal to I_2, both defines in section 2.2.3. This is only true when the voltage ratio (M), expressed as shown in eq. 2.33, is equal to 1.

$$M = \frac{nV_{sec}}{V_{prim}} \tag{2.33}$$

2.5   Microcontroller and Software Tools

In this section, the microcontroller and software tools are presented. All the software has been applied using a personal computer with an x64bit-based windows 11 system.

2.5.1   MathWorks Matlab®& Simulink® v9.10

Matlab, an abbreviation for MATrix LABoratory, is a mathematics-based computing language that integrates computation, visualization, and programming into one environment. Simulink exists within the Matlab system and is used more for graphical modeling, simulating, and analyzing multi-domain dynamical systems. The required Matlab libraries are also listed.

- MATLAB R20212a

- Simulink Control Design

- STM32 embedded target for Matlab and Simulink

- Simcape electrical

- Simulink coder

- Embedded coder

- Target support package - STM32 adapter

2.5.2   KiCad v5.1.10_1

KiCad is an open-source programming tool used for electronic design automation. The software features several EDA aspects, from hierarchical schematic structure to design of the electronic circuits to PCB (Printed Circuit Board) layout. KiCad has integrated footprints for components and can create Gerber files for PCB production.

2.5.3   STMicroelectronics STM32

The microcontroller used for this project is the STM32 Nucleo-64 development board from STMicroelectronics with an STM32L476RG MCU (Microcontroller Unit). It has an integrated ST-LINK/V2-1 programmer and therefore requires no separate probe. The Nucleo board is a low-cost and easy-to-use development platform used to evaluate and start development with an STM32 microcontroller quickly. Two STMicroelectronics environments are required to program the microcontroller. The initialization code generator or STMCubeMX and the Integrated Development Environment (STMCubeIDE).

STM32CubeMX v6.3.0

The CubeMX software system is a graphical tool that allows for the simple configuration of the STM32 microcontrollers and microprocessors and initializes the C code generation.

STM32CubeIDE v1.7.0

The Integrated Development Environment for the STM32 is a development platform with peripheral configuration, code generation, code compilation, and debug features. The code configuration generated from the MX system is automatically generated in the IDE, where the code can further be developed. After compiling, the code is uploaded to the microcontroller through the ST-Link.

Chapter 3

Methods

This chapter will describe the methods used during the development and testing of the bidirectional DAB converter presented in this thesis. The purpose is to clearly explain each part that led to the results presented in chapter 4.

Section 3.1 present some overall design considerations such as the parameters selection, the transistor power module, and the high-frequency transformer design. In section 3.2 the Matlab/Simulink model used to simulate the concept of the bidirectional DAB converter is presented. In section 3.3 the Nucleo-64 STM32L476 microcontroller which is used to produce the required gate signals to the power modules is presented. Both the software and hardware consideration required to use this microcontroller and create the correct SPS modulation are describes in detail. The following section 3.4 addresses the full design and creation of a functioning hardware bidirectional DAB converter. A PCB interface card is designed with the current and voltage measurement circuit and used to integrate the power modules, HF transformer, and all the other electrical components. In section 3.5, the laboratory test setup of the hardware prototype is laid out in detail.

3.1 Design Considerations

3.1.1 Parameter Selection

Various parameters have to be selected in the design process of the DAB converter. Some values were already established at the beginning of this project because of the IGBTs implemented in the power modules. However, most were either decided as an initial set of suitable values or calculated to fit the specification of the converter. The values provided under in table 3.1 are the most fundamental parameters when designing a DAB converter, and the choices for each will be explained in detail in this section.

Name	Symbol	Value
Nominal Power	P_{nom}	800 W
Primary Voltage	V_{prim}	200 V
Secondary Voltage	V_{sec}	200 V
Rated Output Current	I_{sec}	4 A
Restive load	R_{load}	50 Ω
Switching Frequency	f_{sw}	10 kHz
Transformer turn ratio	n	1:1
Power transfer inductance	L	625 µH
Primary capacitance	C_{prim}	150 µF
Secondary capacitance	C_{sec}	150 µF

Table 3.1: System specifications for DAB converter model

Output values

The maximum output power was preliminary set to be 800 watt with an maximum output voltage of 200V and a current of 4A. The hardware prototype was designed according to these parameters. Referring back to section 2.2.3, the converter operates at its limits when the phase shift value, D, is at ±0.5, which results in an load resistance of 50Ω

$$R_{load} = \frac{V_{sec,max}^2}{P_{Rated}} = 50\Omega \tag{3.1}$$

The voltage and current on the secondary side will vary dependent on the phase-shift value D, so I_{sec} will be obtained using eq. 3.2, and subsequently, V_{sec} will be calculated using 3.3.

$$I_{sec} = \frac{V_{prim}}{2 \cdot n \cdot L \cdot f_{sw}} D(1-D) \tag{3.2}$$

$$V_{sec} = I_{sec} \cdot R_{load} \tag{3.3}$$

Turn-ratio

The turn ratio is the ratio of winding turns on each side of the transformer and determines the relationship between the voltage levels on each side. For this project, the goal is to design a

function DAB converter with SPS modulation. Hence the voltage levels on each side are not a critical part of the power transfer and were chosen for simplicity to be equal.

$$n = \frac{V_{prim}}{V_{sec}} = 1 \tag{3.4}$$

Power transfer inductance

The importance of inductance in the DAB and other converters was stated in section 2.2.2. This value is the sum of the transformer leakage inductance and any additional inductance placed at the primary or secondary side of the transformer and is the inductance required for the necessary energy transfer in the converter. The inductance required for the maximum power transfer according to Eq. 2.20 is calculated in Eq. 3.5.

$$L = \frac{n \cdot V_{prim} \cdot V_{sec}}{8 \cdot P_{max} \cdot f_{sw}} = 625\mu H. \tag{3.5}$$

This induction value will also be the suitable inductance to archive soft switching in both the full bridges, as described in section 2.4.

Filter capacitors

To further smooth the voltage through the load and the converter, there is placed a capacitor in parallel with the input and output sources as shown in figure 2.5, section 2.2.1 and works because the voltage across the capacitor cannot change instantaneously[24]. The filter capacitors are utilized to lower the voltage ripple of the converter to an acceptable level.

A minimum value for the filter capacitors were calculated from eq.3.6, which was derived using the output current waveform presented in section 2.2.3, figure 2.10. ΔQ is the energy which the filter capacitors need to absorb in order to smooth the output current to acceptable levels.

$$\Delta Q = \frac{V_{prim} \cdot D^2}{4 \cdot L \cdot n \cdot f_{sw}^2}[(1-D) + \frac{D^2}{4}] \tag{3.6}$$

The voltage ripple is at its max when the phase shift value is at its highest value at D=0.5, which results in eq. 3.7, which determines the capacitance in the filter capacitors.

$$C_{sec} = C_{prim} = \frac{\Delta Q}{2\Delta V_{prim}} = 150\mu F \tag{3.7}$$

3.1.2   Power Module and Transistor

The power module was designed and produced at the Western Norway University of Applied Science before starting this project. These modules are designed for medium voltage direct current applications with several built-in systems such as interlock delay time calibration and integrated signal receivers circuit. Interlock delay time modifies the input signals in such a way that dead-time is prevalent in the switching sequence. They have been designed by assistant prof. Eirik Haustveit and assistant prof. Vegard Steinsland, and assembled by Steffen Troy. The full overview of the schematic of the power module can be found in the appendix B. However, the schematic of the transistor layout is shown in figure 3.1 since it shows how the transistors are put together with its driver circuit and output ports, which are critical for the interface construction which comes later in section 3.4.
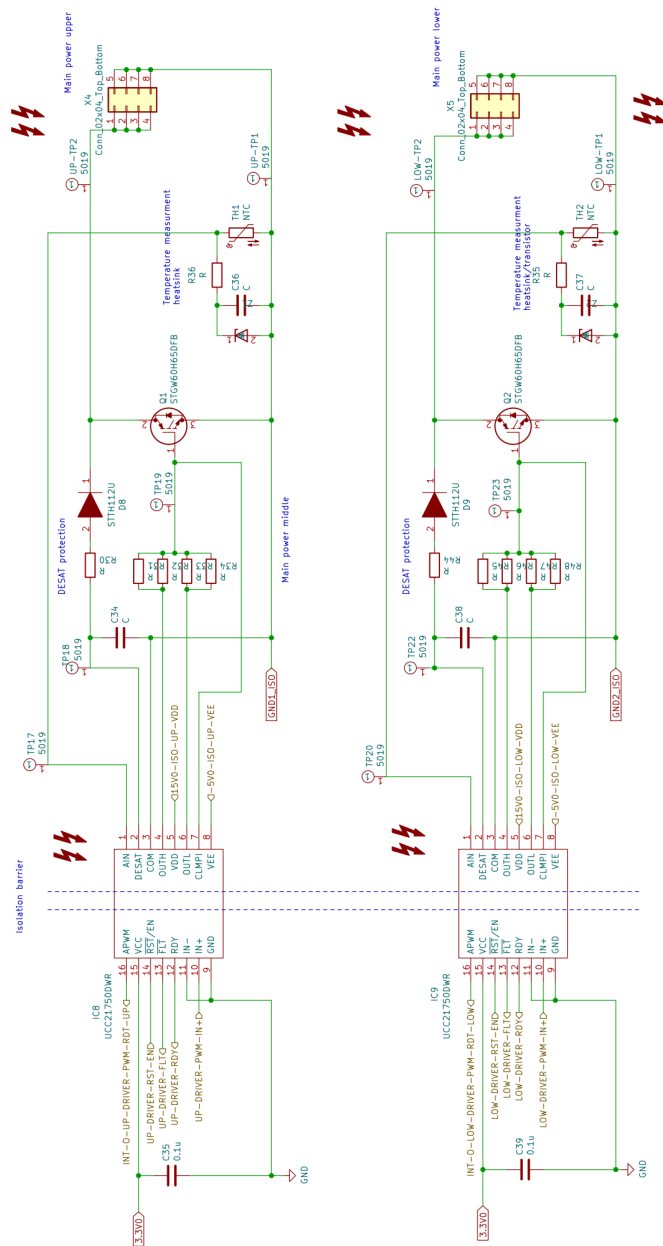
Figure 3.1: Schematic overview of the power module

IGBTs

Each module consists of two power transistors and their required driver circuit in the configuration shown in figure 3.1. The transistor is a IGBT **STGW60H65DFB**, and some of its important specifications are listed under in table 3.2. The full datasheet is found in the appendix C.

Parameter	Symbol	Typical Value
Collector-emitter saturation voltage	$V_{CE(sat)}$	1.60 V
Maximum junction temperature	T_J	175 C
Forward on-voltage	V_F	2 V
Max collector current	$I_{C,max}$	60 A
Switching frequency	f_{sw}	<20 kHz

Table 3.2: Selected IGBT specifications

Switching frequency

The switching frequency is one of the most limiting factors for this project and was early decided to be 10kHz. The operating area for this IGBT is from 1kHz to 100 kHz, referring to figure 3.2. However, this is at the optimal condition, and switching at any frequency over 20kHz would increase the stress on the device and driver circuit. Higher values would reduce the size of the transformer, as mentioned in section 2.1.5. Nevertheless, it would not limit any part of this prototype and testing, so a 10 kHz frequency was decided as a suitable value.

$$f_{sw} = \frac{1}{T_s} = 10 \, kHz \tag{3.8}$$
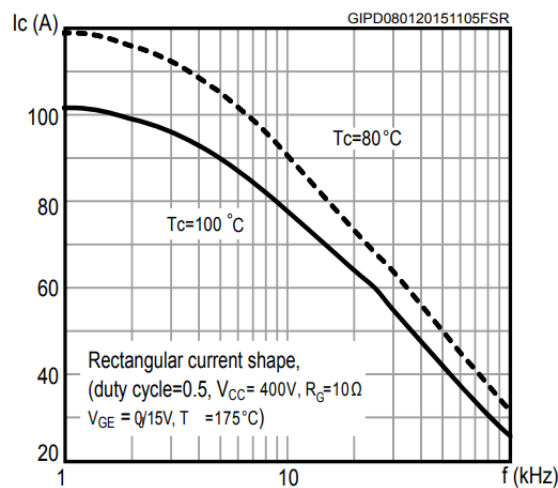
Figure 3.2: Collector current vs. switching frequency figure from IGBT datasheet

Physical model of the power module

Figure 3.3 and 3.4 shows the physical prototype of the power module. The connections in the blue square are the three power cables for the module; one connected to ground and two connected to the positive and negative sides of a 15V DC power supply. The white Ethernet cable in the green square transfers the PWM signals from the microcontroller, which controls the gate signal of the two IGBTs. The transistors are attached to the heat sinks, and the red squares highlight their collector and emitter ports.

Figure 3.3: Side view of the power module
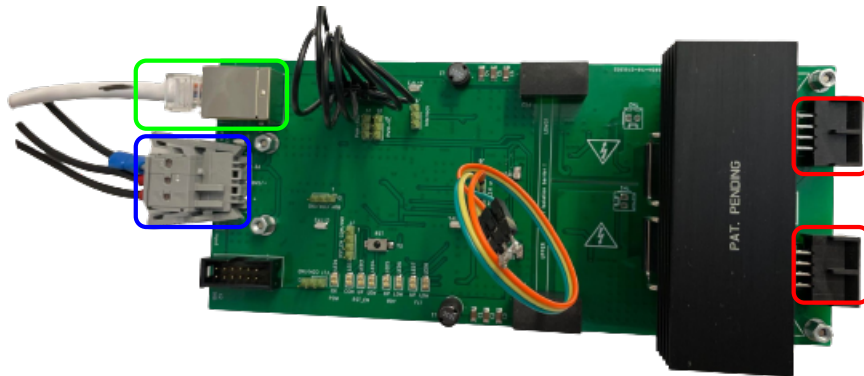
Figure 3.4: top view of the power module

3.1.3   High-Frequency Transformer Design

The HF transformer for the DAB converter was built for this project from the ground up. The first deciding factor is to select a material, bobbin, and core structure that suit the application. Then the number of winding turns on each side can be calculated before, and finally, the wire thickness is designed to accommodate for skin effect and current handling capabilities.

Magnetic Core Material

The transformer size was already selected because of inventory; this included the accessories that fit the core, known as the winding bobbin. It is designed to be used with an E-E core, so the first step is to select a material to fit this bobbin. The ETD 49/25/16 was chosen with the SIFERRIT material N87. One key note in is that the material does not reach its saturation flux density, which for the selected material is around 350 milliTesla, as shown in figure 3.5. Ferrite cores have high electrical resistivity, which reduces the eddy current losses so much that they can be neglected. The only core losses left are the hysteresis loss, which is one of the main reasons this material is used for frequencies from 10kHz and higher. The datasheet for the bobbin, core dimensions, and SIFERRIT N87 material can be found in appendix C.
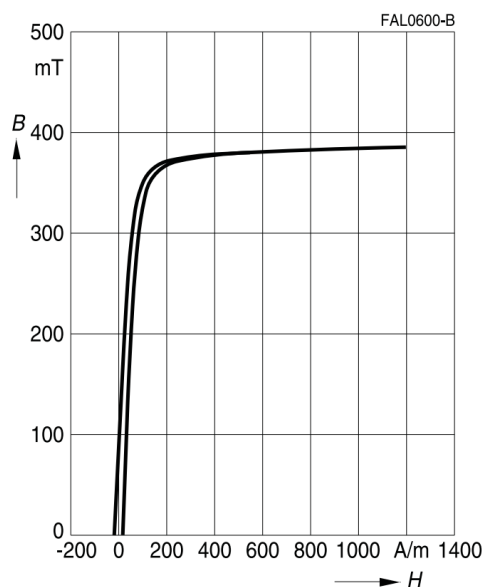
Figure 3.5: Dynamic magnetization curves of N87 material

Number of turns and wire thickness

The turn ratio has been set to 1:1 from section 3.1.1, so each side of the transformer will have the same number of turns. The number of turns are selected to ensures that the transformer does not go into saturation when operating and is calculated accordingly to eq. 3.9[14]. Ae is the effective magnetic cross-section area of $209mm^2$, and B_{max} is the maximum expected to change in flux density which was chosen to be 240mT. The transformer was created with 100 turns on each side of the transformer. The material properties are found in appendix C.

$$N = \frac{V_{prim}}{4 \cdot B_{max} \cdot f_{sw} \cdot Ae} \approx 100 \; turns \tag{3.9}$$

Wire thickness

The thickness of the wire is chosen for two reasons; to fill the transformer area as much as possible in order to mitigate losses, and to handle the maximum current trough the transformer[24][33].

As explained in section 3.1.3, the transformer need to be design to eliminate skin effect as much as possible. To ensure that the current density in the conducting wire is homogeneous throughout the whole cross-section, the skin dept, δ is calculated using an approximation for copper wires in eq. 3.10[24].

$$\delta(mm) = \frac{72}{\sqrt{f_{sw}}} = \frac{72}{\sqrt{10 \cdot 10^3}} = 0.72mm \tag{3.10}$$

The diameter required for the copper wire is therefor twice the length of the skin dept.

$$Wire\ thickness \longrightarrow 2 \cdot \delta = 2 \cdot 0.72mm \approx 1.5mm. \tag{3.11}$$

The available wire thickness was a 0.5mm copper wire. However, this thickness would be too thin to conduct the required current and would not fill the window area of the converter bobbin. This would result in higher power losses in the transformer. Three wires were therefore twinned in parallel, increasing the transformer's current-carrying capabilities.

Construction of the transformer

The first step of the construction process was to cut and twist the wires at length required for both sides. The inner winding is first implemented with start and endpoints on the same side of the transformer, then a thin layer of voltage isolating tape is placed on the outer side of the wires. The outer winding is twisted around the bobbin before the E-E core is placed around and locked in place by metallic strips. The final product of the transformer is shown in figure 3.6.

Figure 3.6: Constructed high-frequency transformer

3.2   DAB Converter Model in Matlab/Simulink

The simulation model of the DAB converter has been designed within Simulink, a MATLAB-based graphical programming environment. The simulations are used to showcase the principles behind the converters and to compare them with the results from the hardware prototype, which is presented in section 3.4. Standard component from the Simscape electrical library was utilized for all simulation models (section 2.5). Figure 3.7 shows an overview of the Simulink model, which is divided into three parts; the DAB converter topology, Signal generation, and Scope. Each part will be described in detail in the following sections.
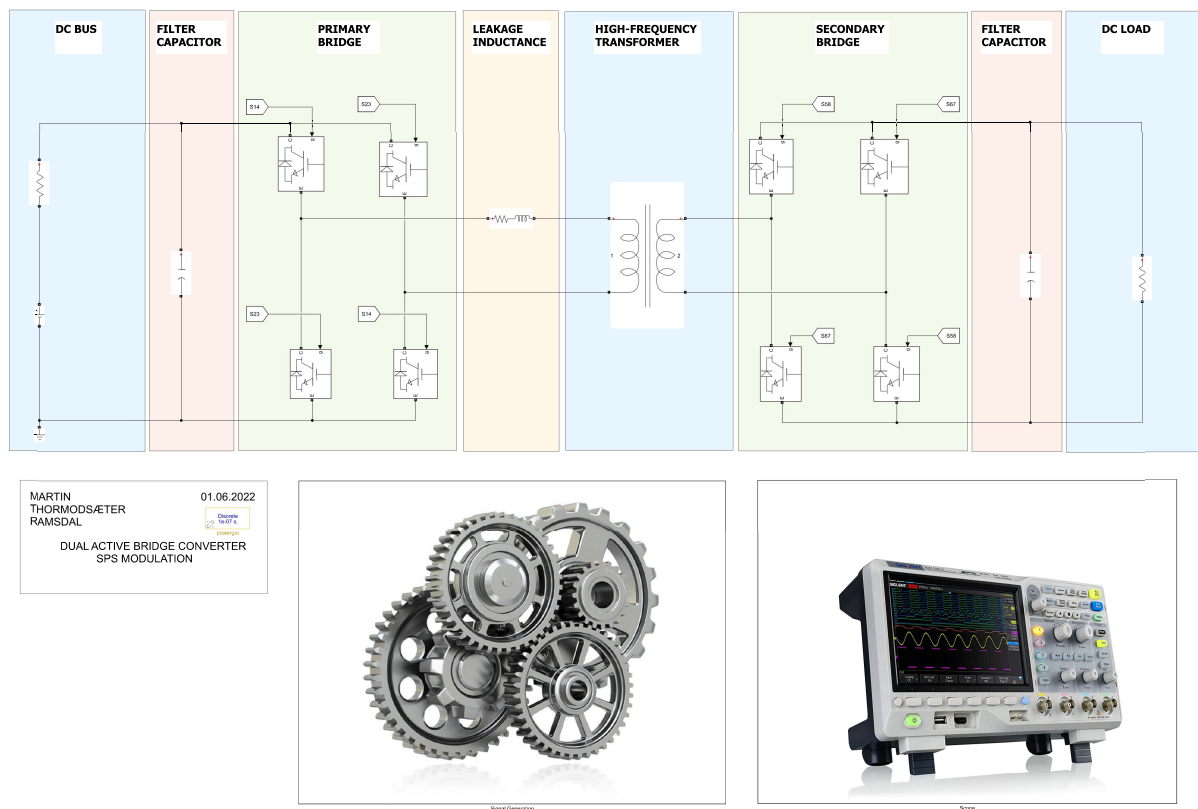
Figure 3.7: Overview of the simulation model in Matlab/Simulink

3.2.1   DAB Converter Topology and Parameters

The design is based on the topology presented in figure 2.5, section 2.2. However, the secondary source has been replaced with a resistive load. Because of this, the model will not function as a bidirectional converter, but the mirrored topology will still represent the bidirectional functionality of the load and source that were switched. Each side has a filter capacitance and a full bridge composed of four IGBTs with anti-parallel diodes. The transformer is a linear transformer with the turn-ratio of 100:100, where all the leakage inductance is modelled using a series inductor on the primary side. The values calculated and selected in section 3.1.1 have been used in the Simulink model. However, some specific values were either chosen to standard, zero, or values that could be measured from the prototype. The copper winding re-

sistance from the specific HF transformer and inductor, presented in section 3.1.3 and 3.4, was measured using a multimeter and embedded in the simulation model. The resistance is 0.875 Ω for the transformer and 0.125 Ω for the inductor.

3.2.2 Control and Signal Generation subsystem

The signal generation subsystem task is to produce the four PWM gate signals to the IGBTs, and ensure the correct phase shift between the two square waves. These signals were produced using pulse generators set with a period $100\mu s$, which would result in a switching frequency of 10kHz. The phase delay for the secondary bridge was also implemented as an initial value decided by the script, presented in 3.2.4. The phase shift value, expressed as D, was used as the input value and could be chosen between 0 and 0.5 since only uni-directional power flow is implemented. Discrete variable time delay blocks are implemented to achieve the desired phase shift between the square wave signals. The PID and signal generator subsystems are found in Appendix A.

dead-time implementation

The dead-time had to be equal to what the power modules would implement in the hardware prototype. Since the dead time circuit was already implemented in the power modules, this needed to be transferred correctly to the simulation. The dead-time implemented was $4.5\mu s$, which required each square wave to be generated with a pulse width of 45.5% of the period.

PID controller

Instead of using the input directly from Matlab script, a PID controller was implemented such that the phase shift could be determined from a reference voltage, current, or power. However, since the measurement circuits could not be realized, neither could this control system. Therefore, no more work was done in this subsystem of the simulation.
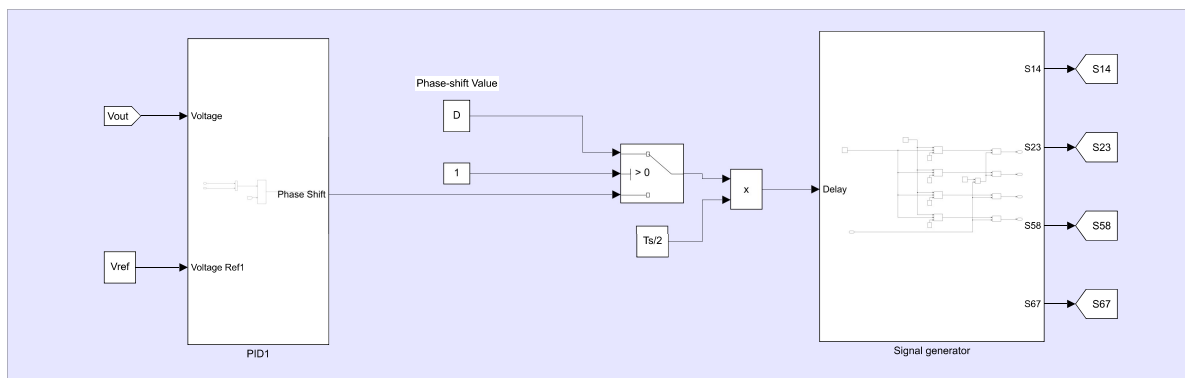
Figure 3.8: Control subsystem

3.2.3   Scope

The scope subsystem has three purposes for the simulation. Firstly, it gathers all the relevant measured signals from the simulation through a multi-meter block. The setup is designed to choose which values are desirable to see and arranged in four groups; voltage, current, gate signals, and power. The second purpose is to implement simple calculations to acquire values such as input and output power and efficiency. The last aspect of this subsystem is to direct average values back to the workplace for comparison and calculations.
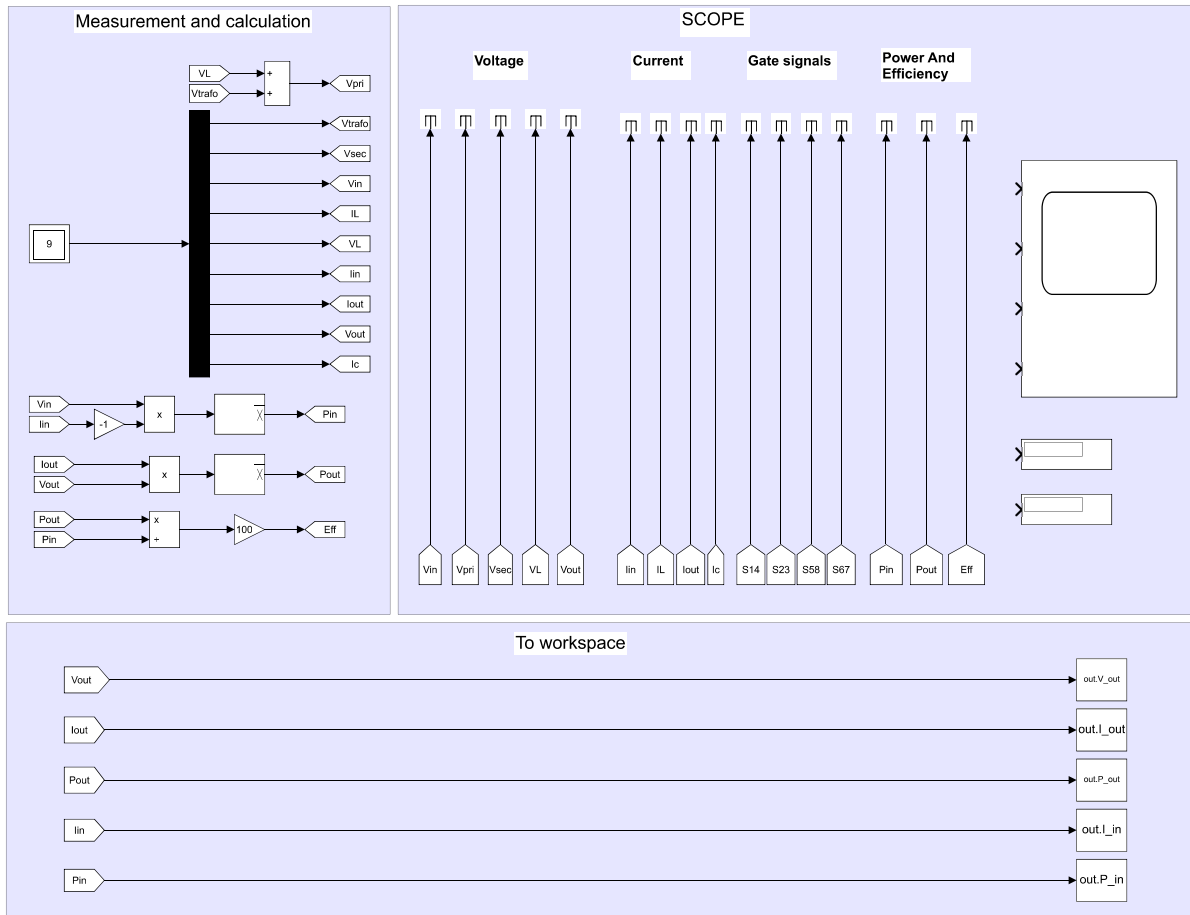
Figure 3.9: Scope simulation subsystem

3.2.4 Script

In the Matlab script, shown in listing 3.1, the main objective was to initialize the values in the Simulink model and then run the simulation. The script also calculates some reference values, based on the equation presented in chapter 2, to compare with the simulation results.

Listing 3.1: Matlab script

```matlab
1 %% Dual Active bridge configuration
2 clear
3 clc
4 close all
5
6 %Set values
7 Sample=1e-7;    %Sample time
8 Rload=50;       %Ohmic load
9 Vin=200;        %Input voltage (DC)
10
11 Cfilter=150e-6; %Filter capacitance
12 L=625e-6;       %Series inductance
13 W1=100;         %Winding turns primary, transformer
14 W2=100;         %Winding turns secondary, transformer
15 n=W2/W1;        %turn-ratio
16 fsw=10e3;       %Switching frequency
17 Ts=1/fsw;       %Period
18
19 D=0.5;           %Phase-shift Value (Between -0.5 and 0.5)
20
21 phase_shift=D*Ts/2;
22
23 Vref=200;  %Reference voltage
24 Iref=4;    %Reference current
25
26 sim('Function_DAB2');
27
28 %Calculations for reference
29 I_out_calculated=(Vin*D*(1-D))/(2*n*L*fsw)
30 V_out_calculated = Rload*I_out_calculated
31 P_out_caluclated=V_out_calculated*I_out_calculated
32
33 I_1 = ((Vin+n*V_out_calculated)*phase_shift - (Vin-n*V_out_calculated)*(Ts
    /2 - phase_shift))/(2*L)
34 I_2 = ((Vin+n*V_out_calculated)*phase_shift + (Vin-n*V_out_calculated)*(Ts
    /2 - phase_shift))/(2*L)
35
36 %Values from simulation
37 I_in_avg=ans.I_in
38 I_out_avg=ans.I_out
39 V_out_avg=ans.V_out
40 P_in_avg=ans.P_in
41 P_out_avg=ans.P_out
42
43 %Efficiency
44 eta_simulated= P_out_avg/P_in_avg
```

3.3 Microcontroller

A MCU (Microcontroller Unit) is an integrated circuit used to dictate the control and operation in an embedded system[4]. The microcontroller is built around its CPU and usually includes at least memory, timers, and input/output ports. For this project, the MCU was used to generate the square wave PWM signals and the controllable phase shift between the two full bridges. MCUs come in all different sizes and power for different applications. The Nucleo-64 STM32L476 from ST-microelectronics was used for this project.

3.3.1 Nucleo-64 STM32L476

There are several STM32 microcontroller boards, and this project utilizes the Nucleo series, more specifically the Nucleo-64 STM32L476, shown in figure 3.10. This board has a built-in programmer and internal PWM signal, which are the main reason for selecting this specific microcontroller since it requires no external signals or ST-link. There is a series of software required for the setup and operation of the controller, which will be discussed in the following sections.

3.3.2 STM32CubeMX

The CubeMX software is used for STM32 microcontroller and microprocessor selection and utilizes a graphical interface for the configuration of controller elements such as pin-out, internal clock, timers, and ADCs. The CubeMX generates the C initialization code project, which is directed to the selected project manager tool-chain, the STM32CubeIDE. The Nucleo-64 STM32L476 STbord can be selected within the interface, which automatically sets the standard pins and clock configuration according to the CPU and board connections. Figure 3.11 shows the pin-out connections as displayed in the CubeMX software.
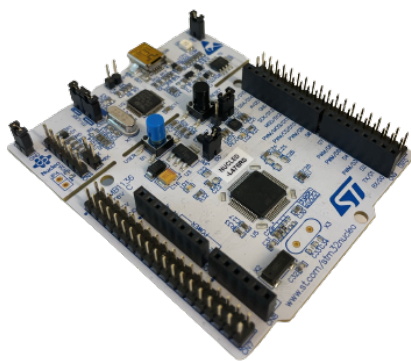
Figure 3.10: Nucleo-64 STM32L476
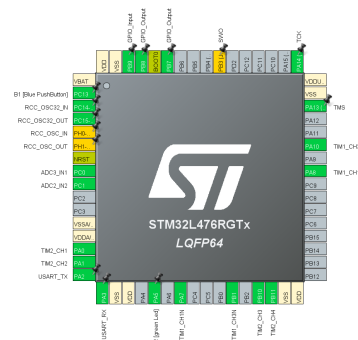
Figure 3.11: Pin-out view of the MCU

Internal clock and Timers

The timers were the most crucial part of the microcontroller for this project as they were used to generate the square waves PWM signals for all eighth IGBTs, as well as the controllable phase-shift between the two bridges. For this project, timer one was used with PWM signals generated from channel 1 for the primary and channel 3 for the secondary bridge. The inverse signal was also required for the second leg of each bridge. Table 3.3 shows the four output signals and associated output pin on the MCU.

TIM1_CH1	PA8	TIM1_CH3	PA10
TIM1_CH1N	PA7	TIM1_CH3N	PB1

Table 3.3: Timer channels and associated pin-out ports

The signal needed to have the correct frequency of 10kHz, a duty-cycle of 50%, and the ability to phase-shift compared to each other. This is accomplished using the center-aligned counter mode, with a Prescaler set to 19, and ARR (Automated Reload Register) set as 49, and an internal clock set to 20MHz. The frequency is den determined by the equation 3.12. The extra two are in the denominator because of the center aliened mode, which in essence doubles the count. Both the ARR and Prescaler start from 0.

$$SwichingFrequency = \frac{Internal\ clock}{Prescaler \cdot ARR \cdot 2} = 10\ kHz \tag{3.12}$$

The programmable phase shift of the PWM signals was achieved by using Asymmetric mode on the two center-aligned PWM signals. The duty cycle and the phase shift are determined by a pair of CCRx registers, where one register controls the PWM during up-counting, the second during down-counting so that PWM is adjusted every half PWM cycle.

OC1REFC is controlled by TIM1_CCR1 and TIM1_CCR2

OC3REFC is controlled by TIM1_CCR3 and TIM1_CCR4

Figure 3.12 shows a representation of the timer sequence, and how the two square waves are generated from the control of the CCRx register. For simplicity, the ARR has been set to 5 instead of 49 in the figure.
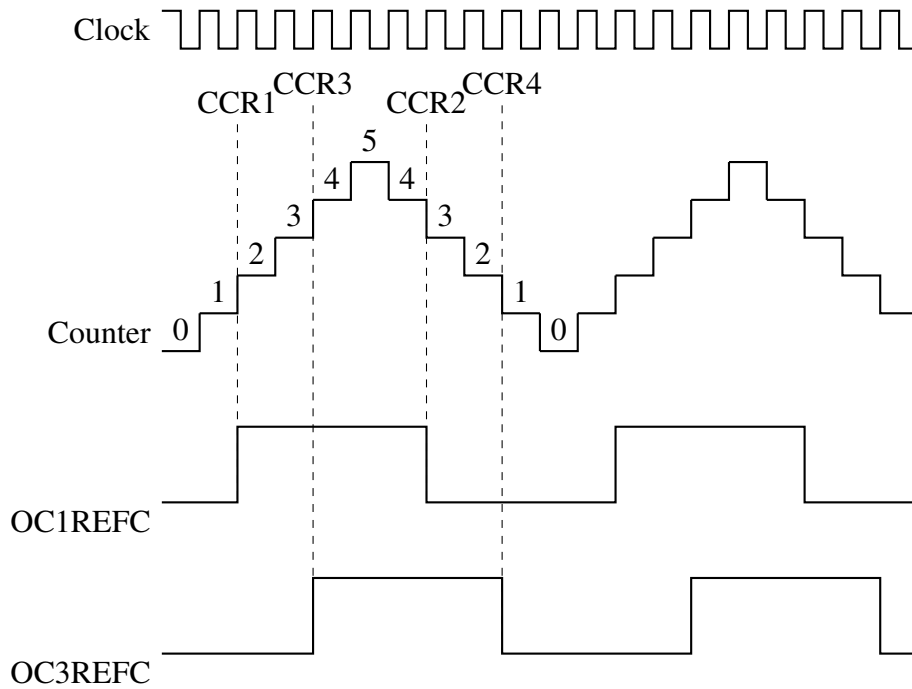
Figure 3.12: clock, counter and channel sequence

In the example referring to figure 3.12, where CCR1 is 2, CCR2 is 4, CCR3 is 3 and CCR4 is 1. The result is a phase-shift of the two output signals to be as eq.3.13. Because of the permanent 50% duty cycle, the down counting value is always a fixed value behind each up-counting. Combining this with the fact that only one of the brides requires to be shifted limits the phase shift control to only one CCRx value, specifically the CCR1. Setting CCR3 to be 25 would implement the range of phase shift where CCR1 as 0 would result in the phase shift of D=0.5, and a CCR1 value of 50 would result in the phase shift of D=-0.5.

$$D = \frac{CCR3 - CCR1}{ARR} = 0.4 \tag{3.13}$$

Code from CubeMX

The critical code section generated from the CubeMX is the main file and initializing of configurations such as the timers. The code in listing 3.2 is a constricted part of the initializing of timer 1 and the four channels. Some parts of the code have been cut out, and the whole main file is uploaded to GITHUB with a link found in appendix D.

Listing 3.2: Timer initialization

```
1  static void MX_TIM1_Init(void)
2  {
3    htim1.Instance = TIM1;
4    htim1.Init.Prescaler = 20-1;
5    htim1.Init.CounterMode = TIM_COUNTERMODE_CENTERALIGNED1;
6    htim1.Init.Period = 50-1;
7    htim1.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
8    htim1.Init.RepetitionCounter = 0;
9    htim1.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_ENABLE;
10   sClockSourceConfig.ClockSource = TIM_CLOCKSOURCE_INTERNAL;
11   sMasterConfig.MasterOutputTrigger = TIM_TRGO_OC1REF;
12   sMasterConfig.MasterOutputTrigger2 = TIM_TRGO2_OC3REF;
13   sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_ENABLE;
14   sConfigOC.OCMode = TIM_OCMODE_ASSYMETRIC_PWM1;
15   sConfigOC.Pulse = 25;
16   sConfigOC.OCPolarity = TIM_OCPOLARITY_HIGH;
17   sConfigOC.OCNPolarity = TIM_OCNPOLARITY_HIGH;
18   sConfigOC.OCFastMode = TIM_OCFAST_DISABLE;
19   sConfigOC.OCIdleState = TIM_OCIDLESTATE_RESET;
20   sConfigOC.OCNIdleState = TIM_OCNIDLESTATE_RESET;
21   /* TIM1 Start. */
22           while ((&htim1)->State == HAL_TIM_STATE_BUSY) {
23           }
24           /* Enable the PWM output 1. */
25           HAL_TIM_PWM_Start(&htim1,TIM_CHANNEL_1);
26           /* Enable the complementary PWM output 1. */
27            HAL_TIMEx_PWMN_Start(&htim1,TIM_CHANNEL_1);
28           while ((&htim1)->State == HAL_TIM_STATE_BUSY) {
29           }
30       /* Enable the PWM output 3. */
31            HAL_TIM_PWM_Start(&htim1,TIM_CHANNEL_3);
32          /* Enable the complementary PWM output 3. */
33           HAL_TIMEx_PWMN_Start(&htim1,TIM_CHANNEL_3);
34   HAL_TIM_MspPostInit(&htim1);
35  }
```

3.3.3 STM32CubeIDE

The next section of software required for the microcontroller is the Cube Integrated development environment, or CubeIDE, which is the development tool for integrating the CubeMX code and further programming, peripheral configuration, and compiling and debugging for the STM32 microcontroller and microprocessor. The CubeIDE is also the connection between the software and the microcontroller, so it uploads the code through the ST-link on the STM board. The listing underneath in listing 3.3 is a section of the main file from the CubeIDE, which shows, among other things, the initialization of the configuration. However, it includes the while loop, which runs the step function that controls the CCRx values. The step function will be discussed in more detail in the following section.

Listing 3.3: Main function

```
1  int main(void){
2    /* MCU Configuration---------*/
3    HAL_Init();
4    /* Configure the system clock */
5    SystemClock_Config();
6    /* Configure the peripherals common clocks */
7    PeriphCommonClock_Config();
8    /* Initialize all configured peripherals */
9    MX_GPIO_Init();
10   MX_TIM1_Init();
11   MX_ADC2_Init();
12   if (SysTick_Config((uint32_t)(SystemCoreClock/1000.0))) {
13       autoReloadTimerLoopVal_S = 1;
14       do {
15         autoReloadTimerLoopVal_S++;
16       } while ((uint32_t)(SystemCoreClock/1000.0)/autoReloadTimerLoopVal_S
     >
17               SysTick_LOAD_RELOAD_Msk);
18       SysTick_Config((uint32_t)(SystemCoreClock/1000.0)/
     autoReloadTimerLoopVal_S);
19     }
20     remainAutoReloadTimerLoopVal_S = autoReloadTimerLoopVal_S;
21     {
22       int i;
23       for (i = 0; i < 1; i++) {
24         OverrunFlags[i] = false;
25       }
26     }
27     /* Initialize model */
28     DABfolder_initialize();
29   /* Infinite loop */
30   while (1){
31    if (remainAutoReloadTimerLoopVal_S == 0) {
32       remainAutoReloadTimerLoopVal_S = autoReloadTimerLoopVal_S;
33       if (OverrunFlags[0]){
34           rtmSetErrorStatus(DABfolder_M, "Overrun");
35       }
36        OverrunFlags[0] = true;
37        /* Step the model for base rate */
38        DABfolder_step();
39        OverrunFlags[0] = false;
40    }}}
```

3.3.4 Simulink and STM32 Implantation

The implementation of the STM32 into a Matlab/Simulink model was done for a few critical reasons. The main reason was to generate the code that could be integrated into the CubeIDE with the already existing main file from the CubeMX not to write the complicated code from nothing. The simulations and the microcontroller needed to work together to implement any control system.

Integration and configuration

The first step is to configure the MCU with the Simulink model. The MCU configuration block from the integrated target support package sets a path to the CubeMX file. After that, the code generation was set up in the model set in the Simulink toolbar. In the code generation, the stm32.TLC file in system target file was selected and C-code set as the programming language. Finally, in the configuration, the cubeMX.ioc file must be included, which will automatically read the file and allow us to use the active function set in the cubeMX software.

STM32 Simulink model

The model is built up of blocks from the integrated target support package where only the timers and ports are determined in the CubeMX configuration. An ADC is set up as a read port to control the phase shift instantaneously. However, a few lines of code were altered so that the phase shift could be set manually from the code. If requested, the four register access block could directly changes the four CCRx values. The model was designed to generate code that created the two square waves of the right frequency and 50% duty-cycle, as described in figure 3.12.
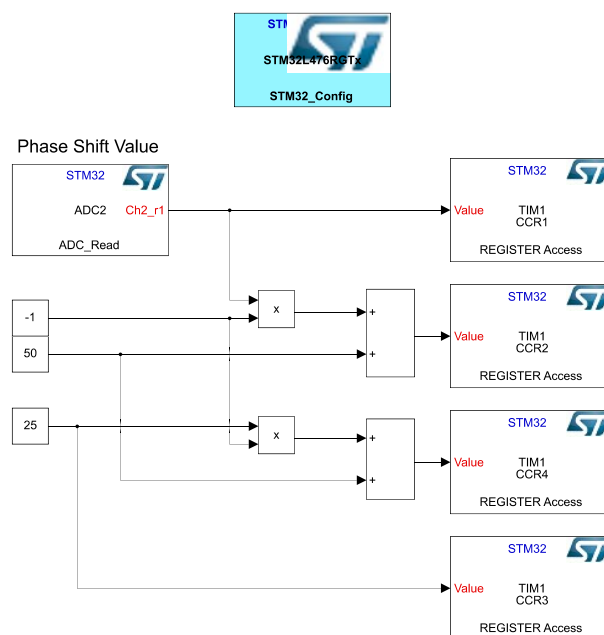
Figure 3.13: Simulink model with STM32 implementation

Code generation and file combination

The embedded coder will automatically generate code from the Simulink model. Then the code needs to be implemented with the existing main file generated from the CubeMX in the CubeIDE. The main file created from the setup in the CubeMX initialized the timers, PWM signals, and the input and output ports of the board. The file generated from the Simulink model is used as a step function within the while loop of the main file.

The listing 3.4 is the step function generated from the Simulink model and shows how the phase shift is decided as well as how the four CCRx values are calculated to achieve the wanted phase shift and duty cycle. There is one change that has been done between the code generated from model 3.13, which is that the ADC input value has been changed to a constant to make it more straightforward to implement a specific phase shift.

Listing 3.4: Step function

```
1 void DABfolder_step(void){
2   /* Get regular rank1 output value from ADC2 regular value buffer */
3   DABfolder_B.ADC_Read2 = ADC2_RegularConvertedValue[0];
4    /* Re-Start ADC2 conversion */
5     HAL_ADC_Start(&hadc2);
6
7     double D=0.5; //Between -0.5 and 0.5
8     double PhaseShiftValue=0;
9
10    PhaseShiftValue=25+50*(D);
11    int CCR = 25; //Used to control the secondary bridge, but no need to
      change.
12
13
14    DABfolder_B.Add2 = PhaseShiftValue * (-1.0) + 50.0;
15  {
16    /* CCR1 */
17    TIM1->CCR1 = PhaseShiftValue;
18  }
19  {
20    /* CCR2 */
21    TIM1->CCR2 = DABfolder_B.Add2;
22  }
23  {
24    /* CCR3 */
25    TIM1->CCR3 = CCR;
26  }
27  {
28    /* CCR4 */
29    TIM1->CCR4 = CCR * (-1.0) + 50.0;
30  }
31 }
```

3.4 Hardware Prototype Design

This section will present the design, construction, and assembling of the DAB converter hardware prototype. The first part describes the schematic of the DAB converter, then the PCB design using KiCad. The electrical components will be presented with a detailed description of why they were chosen. Finlay, the assembling of the whole converter is presented. The full schematic diagram, PCB layout as well as important component datasheets are found in the appendix B, and C, respectively.

3.4.1 Schematic

The starting point for the prototype was to draw the schematic layout in KiCad, based on the topology presented in section 2.2.1 figure 2.5. The schematic diagram represents the DAB converter, excluding the power modules but including current and voltage measurements circuits on both the input and output sides. The diagram is fabricated to make the circuit board interface with in and output connections and the four power modules.
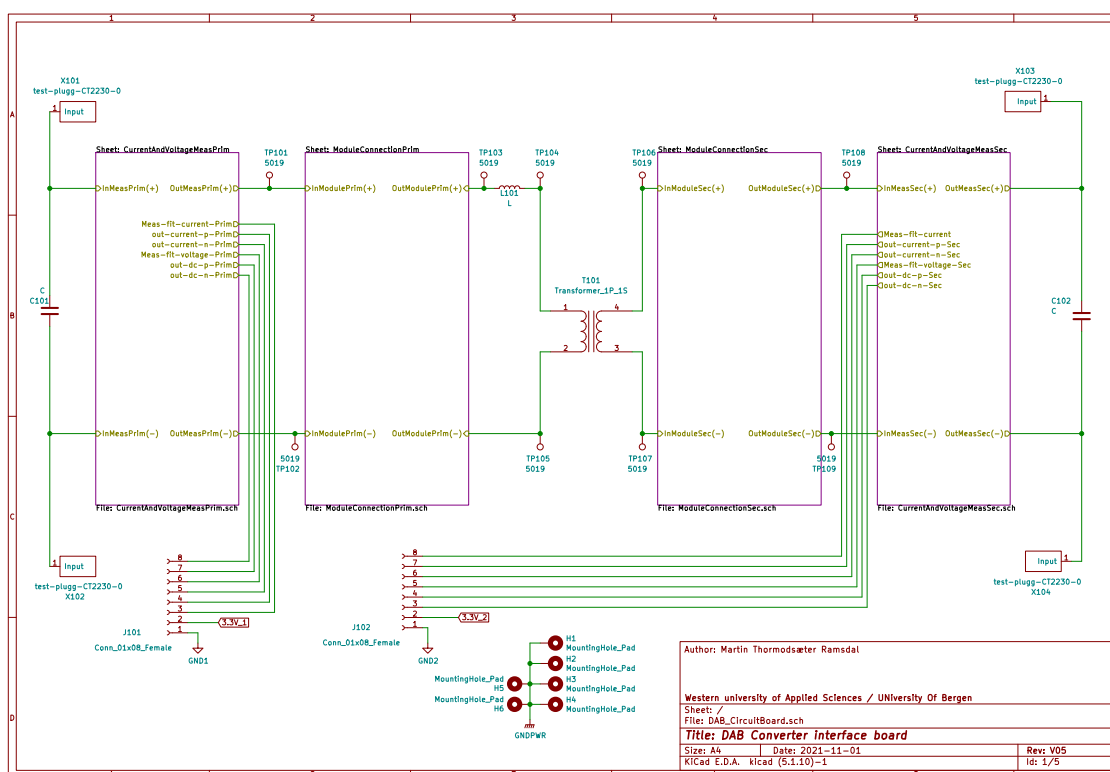
Figure 3.14: Schematic layout of the interface board

Power module connections

Each power model consists of two transistors, so a total of four connections, as shown in the schematic in figure 3.1. These four connections had to correctly connect the output ports of the modules such that they are connected in a full-bridge topology on each side of the HF transformer. The schematic for this is found in Appendix B

Current and voltage measurements

The current and voltage measurements are essential when it comes to implementing the converter's control and regulation systems. These schematics were already designed at HVL and could be transferred to this project. The schematic only needed to be scaled accordingly and implemented in the correct areas. The schematic for primary and secondary measurement circuits is located in Appendix B.

3.4.2   Printed Circuit Board Design

When the schematics were completed, they needed to be realized through KiCads PCB designer. Each element was placed and connected according to the schematic with associated footprints. An essential aspect of the design was to ensure large enough copper areas to handle the current capabilities, which was verified using KiCads' built-in calculator. Other aspects of the design included the implementation of the measurement circuits, vias to interconnect the copper layers on each side, and good ground connectivity. The finalized and printed interface card is located in Appendix B.6.

Footprints

Footprints for the interface card were either found in the KiCads' library or made to fit elements such as the transformer and power module connections. Figure 3.15 shows the PCB overview of the interface card, and a more detailed in located in appendix B.
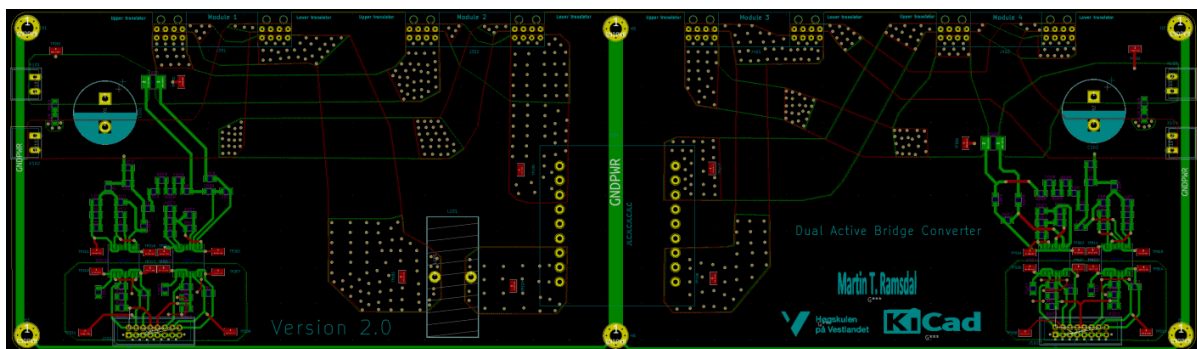
Figure 3.15: PCB overview of the interface board

3.4.3   Components and Assembling

Essential components such as the series inductor, filter capacitors, and current sense resistor will be presented here. The data sheets for these components are found in Appendix C. Other components such as the connectors and test pints will not be presented.

Because of a microchip shortage and production delays, receiving the specific current and voltage measurement integrated circuit components was unattainable. Some different circuits and components were tried without success, so the voltage and current measurement circuits were never realized.

Filter capacitors

The filter-capacitors are placed in parallel with the in and output ports of the converter, as shown as C1 and C2 in figure 3.16 presented in the following section 3.5. Based on the values calculated in section 3.1.1 the **450VXH150MEFCSN22X35** aluminum electrolytic capacitors ware used.

Current sense resistors

The current sensor resistor was a **WSHP2818R1000FEB** from Vishay Intertechnology. It is a Surface Mounted power Metal Strip resistor for high power, producing low resistance values. Even though the measurement circuits were not realized, the resistors were implemented to see how they would react to the power handling of the converter.

Series inductor

Two series inductors were used throughout the converter testing and have therefore been labeled as inductor 1 and inductor 2. Both induction values of the inductors vary from what was calculated in section 3.1.1, which could change the expected results with some margin. No suitable inductors with the exact desired value were obtainable.

- Inductor 1 is a 600 μH API Delevan PT500-1750HM inductor with a Iron Powder core.

- Inductor 2 is a 680 μH Bourns 2300LL-561-H-RC inductor with a ferrite core.

3.5   Laboratory Setup

This section will present the laboratory setup for the hardware prototype. It includes the signal transfer from the microcontroller to the power modules and how the modules are connected to the interface board and the testing equipment. The experimental setup was used to test the power flow, phase shift implementation, and bidirectional operation.

3.5.1   Hardware DAB Converter Prototype

Figure 3.16 shows the final hardware prototype of the DAB converter, with highlighted components and connections. The modules are powered and connected as described in section 3.1.2.
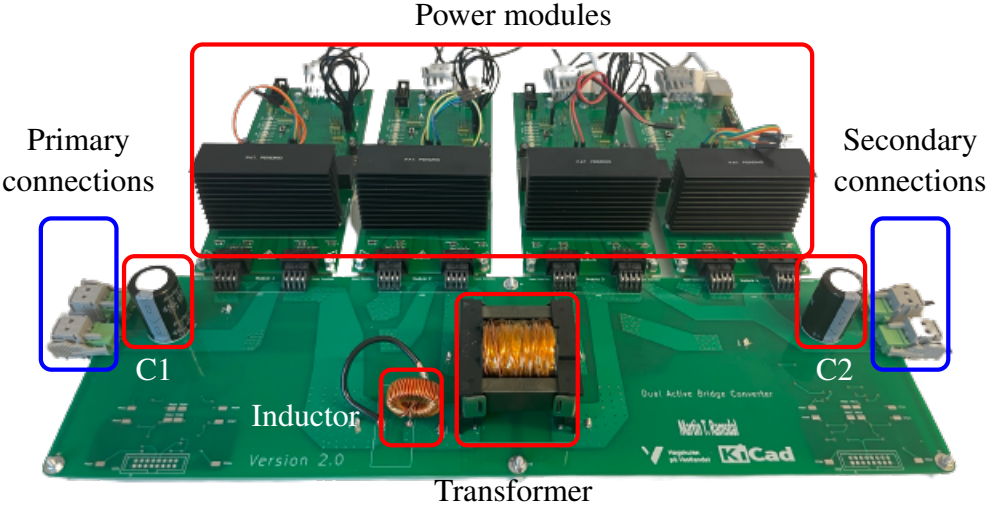
Figure 3.16: Hardware DAB Converter Prototype

3.5.2   Modules and Microcontroller Implementation

As mentioned in section 3.1.2, the power modules were implemented with an integrated differential receiver circuit. Therefore, a complimentary driver circuit had to be designed such that the signal from the microcontroller would be split into two signals and combined again in the power module. This would balance the transmission lines and reduce external interference to the signal. The component used in the power module and the external circuit was an SN65C1167, a Dual differential driver and receiver from Texas Instrumental. Figure 3.17 shows the microcontroller and two driver circuits for the SN75C1167N chip, as well as the output Ethernet cables which are connected to the power modules. The schematic of the circuit is found in appendix B and the datasheet for the SN75C1167N chip is found in appendix C.
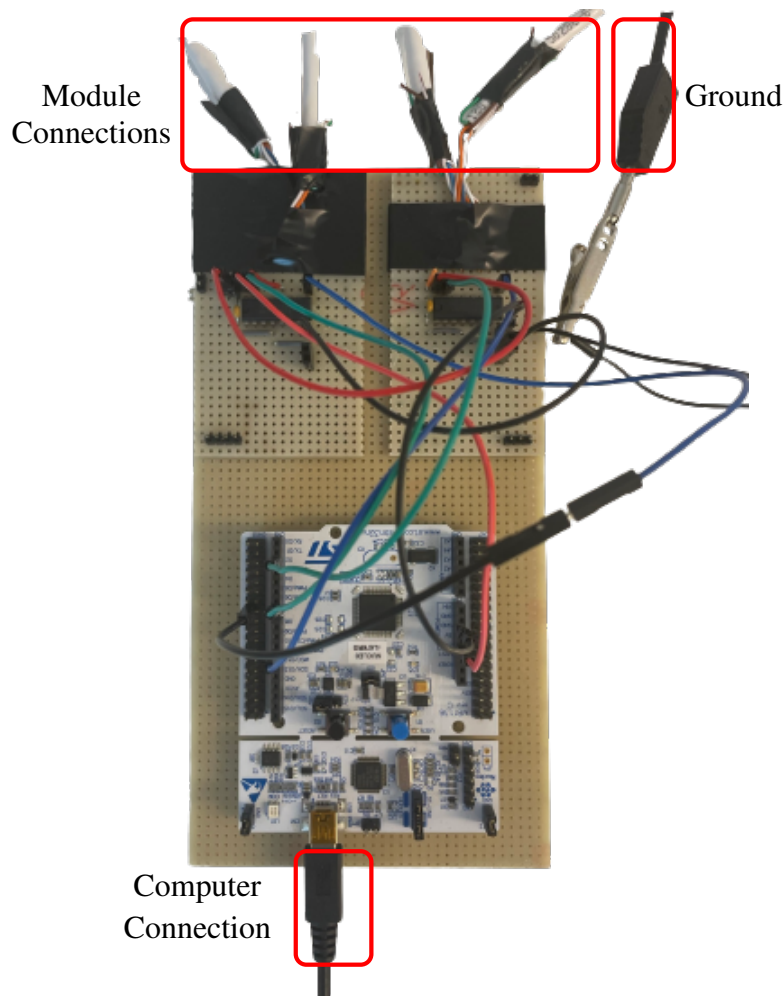
Figure 3.17: Microcontroller and Dual differential driver circuit

3.5.3 Equipment

The equipment used during the testing of the DAB converter is depicted in figure 3.18 and listed in table 3.4. The oscilloscope was used for detailed current and voltage plots gathered from the current and differential voltage probes. The Mascot supplied the power for all the transistor modules with a 15V DC source. The supply voltage on the primary side of the converter came from two different Electro-Automatik power supplies. The multimeter from Hioki was used to measure steady-state voltages and ohmic loads and as a backup for the display for the Electro-Automatik power supply. Image of the DC load, EA-PSI power supply and the thermal camera in located in Appendix E.

Figure 3.18: Equipment

System	Manufacturer	Type	Figure 3.18
Digital Oscilloscope	Rigol	Ultra Vision DS1054	1
Power Supply	Elektro-Automatik	EA-PS 2032-050	3
Power Supply	Mascot	719	4
Multimeter	Hioki	DT4282	2
Diff. Probe	Micsig	DP10013	6
Current	Probe Micsig	CP2100A	5
DC load	Terco	MV 1100	E
Power Supply	Elektro-Automatik	EA-PSI 9500-06 T	E
Thermal camera	fluke	Ti27	E

Table 3.4: Equipment

Chapter 4

Results

This chapter presents the results from both the simulation and physical prototype that have been presented in this thesis. First the gate signals with interlock delay time will be presented in section 4.1, followed by results without any series inductor in section 4.2. Then implementation of phase-shift, and bidirectional power flow is presented in section 4.3. Then power results are presented in section 4.4 and heat dissipation results in section 4.6.

The simulation results from the Matlab/Simulink model have been provided from the subsystem described in section 3.2.3. The figures have been displayed using the scope block from the Sinks library in Simulink. All the results from the model have been sectioned out after the simulation has reached its steady state.

The data points from the hardware prototype have been measured and saved on the oscilloscope as CSV files. These data points are used directly to produce the figures as they were shown on the oscilloscope. Therefore, the y-axis begins at zero even if the system is in steady state.

When testing using the hardware prototype, the first series of tests were done with an applied voltage of 60V and a current of approximately 1A. This was because several tests did not require the total power rating determined in section 3.1.1. Later, when the full power tests were set up, the power source could not reach the selected power levels. Therefore, the applied primary voltage was reduced from 200V to 120V.

As mention in chapter 3, there were utilized two different series inductors. These have been classified as inductor 1 and inductor 2.

4.1 Gate Signals

The gate signals determine the switching sequence of the IGBTs and, therefore, the power control of the DAB converter. The interlock delay time in the power module causes a dead-time which was measured on the oscilloscope to be $4.5\mu s$, which then was implemented in the Matlab/Simulink model.

Figure 4.1 shows the four gate signals (S14,S23,S58,S67) from the Matlab/simulink model. Figure 4.2 is the measured gate signals from the two complementary signals on the primary side, and figure 4.3 is the same on the secondary side. All gate signals shows an applied dead-time of $4.5\mu s$ and a switching period of $Ts = 100\mu s$. The primary and secondary bridges are phase-shifted to each other by a value of D=0.5, which is equal to $\delta = 25\mu s$.

Whereas the voltage levels in the simulation model alternate between 0V and 1V, the gate signals from the power modules alternate between -1V and 3V. The higher interval ensures that the gate signals do not change state when not desired.
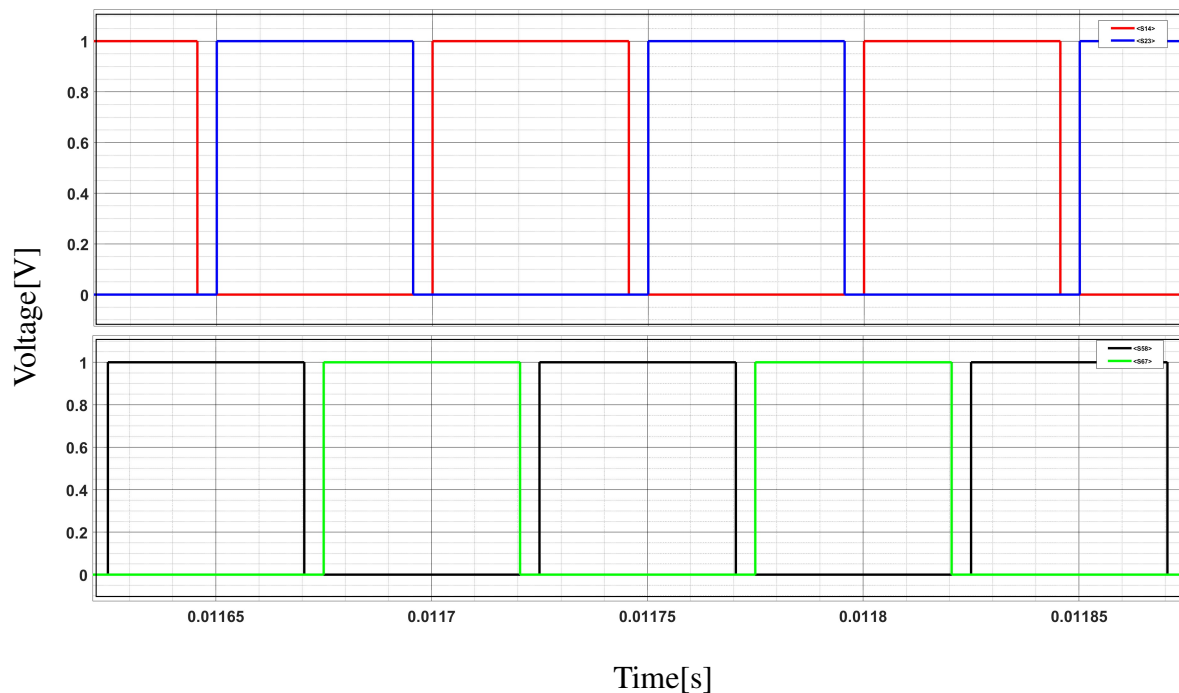
Figure 4.1: Gate signals from Matlab/Simulink model
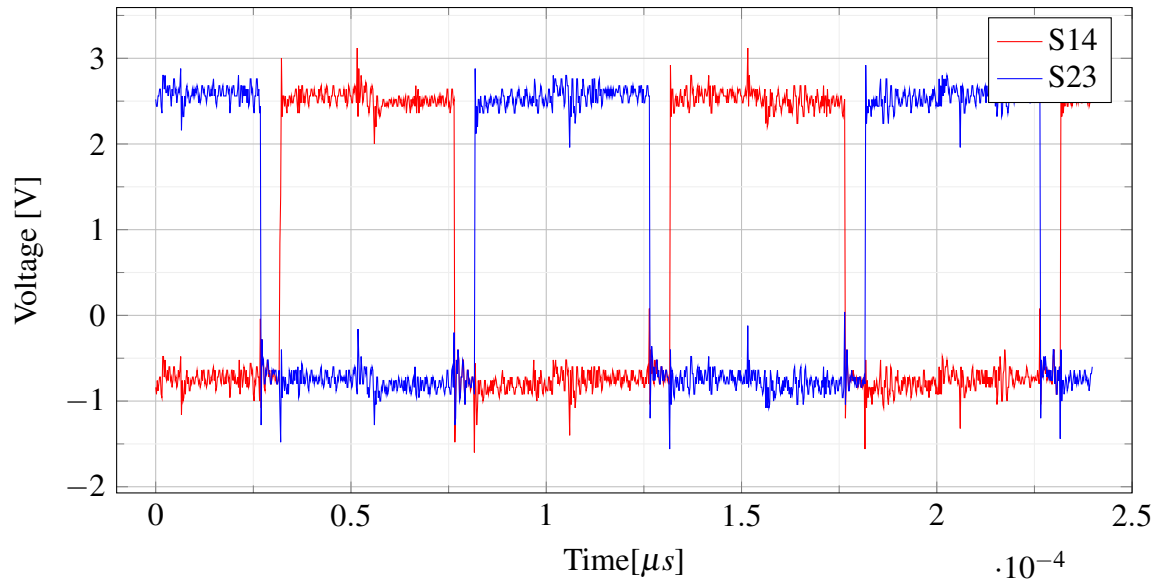
Figure 4.2: Gate signals from hardware prototype on primary bridge
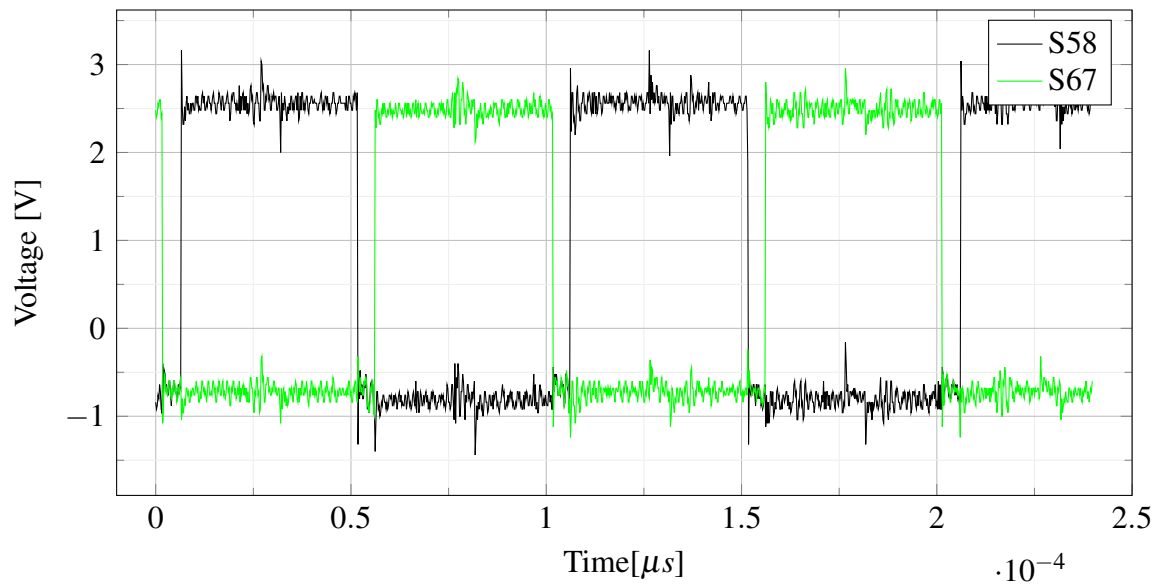
Figure 4.3: Gate signals form hardware prototype on secondary bridge

4.2 Hardware Testing Without Series Inductor

The results in this section describe the power flow through the converter without any series inductor. Without substantial inductance, the power flow can not be controlled using SPS modulation or flow between two power sources. This topology can still transfer power from an input source to an output load using the two active bridges as an inverter and rectifier. The results can indicate power losses in the transistor and transformer.
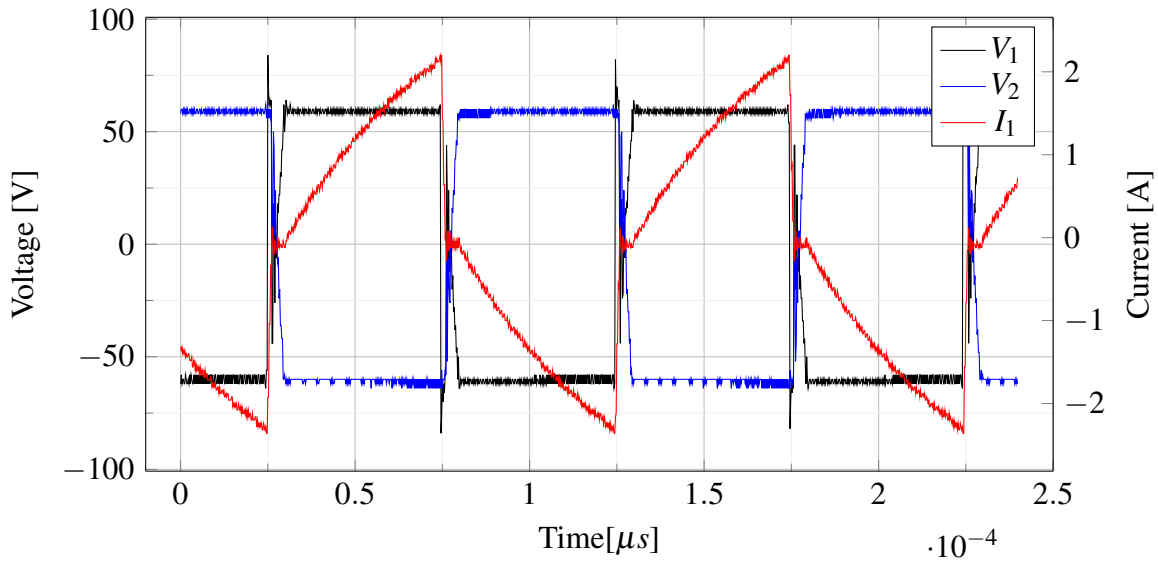
Figure 4.4: Voltage and current characteristics measured on the transformer windings and current trough primary winding with an applied voltage of 60V on the hardware prototype
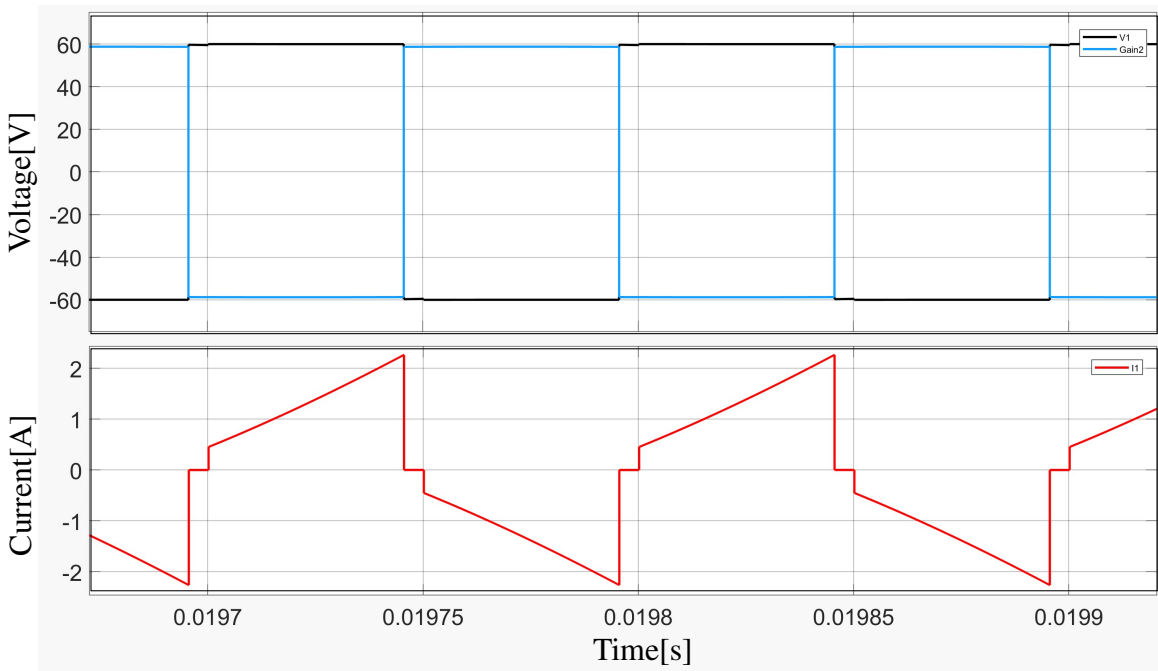
Figure 4.5: Voltage and current characteristics measured on the transformer windings and current trough primary winding with an applied voltage of 60V from the Matlab/Simulink model

Figure 4.4, and figure 4.5 present results from the hardware prototype and the simulation model

where the series inductor have been removed from the topology. Both figures show the two square voltage waves on either side of the transformer and how the current passes through it.

V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
10	0.116	7.4	0.130	1.16	0.962	0.830
20	0.309	16.7	0.310	6.18	5.177	0.840
30	0.503	26.1	0.502	15.09	13.10	0.868
40	0.640	35.6	0.630	25.6	22.43	0.876
50	0.899	45.1	0.880	44.95	39.688	0.883
60	1.09	54.5	1.08	65.4	58.86	0.900

Table 4.1: Power results from hardware prototype using to series inductor

V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
10	0.2	9,8	0.19	2.0	1.9	0.962
20	0.40	19.5	0.40	8.0	7.7	0.962
30	0.60	29.4	0.59	18.0	17.2	0.962
40	0.80	39.2	0.78	31.9	30.7	0.962
50	0.99	48.9	0.98	49.9	48.0	0.962
60	1.20	58.7	1.18	71.8	69.1	0.962

Table 4.2: Power results from Matlab/simulink using to series inductor

Table 4.1 and table 4.2 shows power results from this topology with varied applied voltage, ranging from from 0V to 60V, with 10V intervals. The most notable result from the hardware prototype is how the efficiency increases when the applied power increases as the converter elements operate close to their rated values. This is not observable in the simulation model as these elements always operate at the best functionality.

4.2.1   Transformer Ratio

Without the series inductor connected, the transformer turns could be measured to confirm the turn-ratio of 1. Each side of the transformer was measured with a voltmeter in an input voltage of 50V. The result was a turn-ratio of right above 1, as shown in eq. 4.1. The deviation is probably a result of one turn too much or too little on one of the sides when constructing the transformer.

$$\frac{V_{prim,transformer}}{V_{sec,transformer}} = \frac{n_1}{n_2} = 1.0175 \qquad (4.1)$$

4.3   Implementation of Phase-Shift

This section will present the voltage and current characteristics of the series inductor, with different phase-shift values. The applied primary voltage was 60V and inductor 1 as series inductor was used. The simulation and hardware results from phase shift of D=0.0 and D=0.5 are presented in this section, while D=0.2,0.3,0.4 are provided in Appendix F.
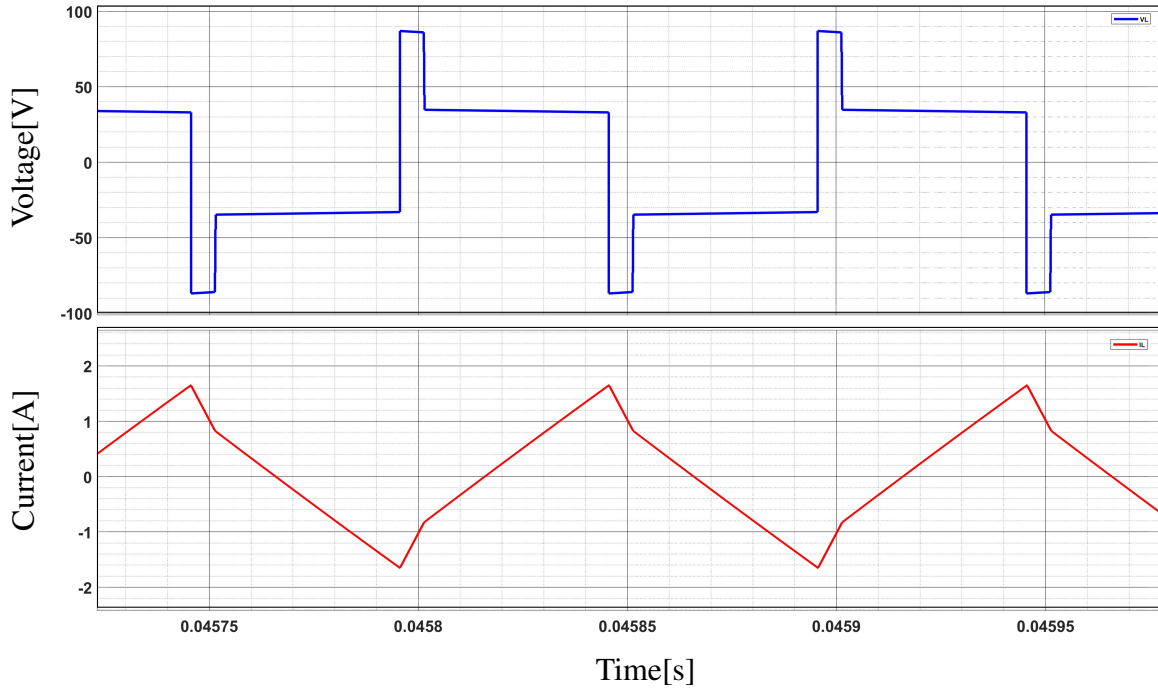
Figure 4.6: Matlab/simulink waveforms of inductor characteristics with a phase-shift value of 0.1
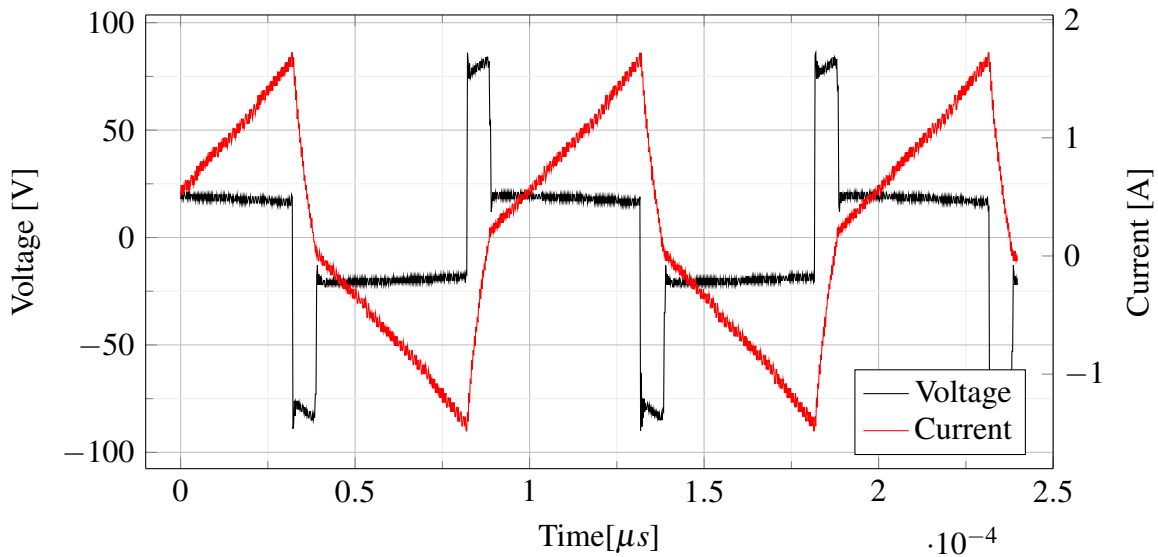
Figure 4.7: Hardware prototype waveforms of inductor characteristics with a phase-shift value of 0.1
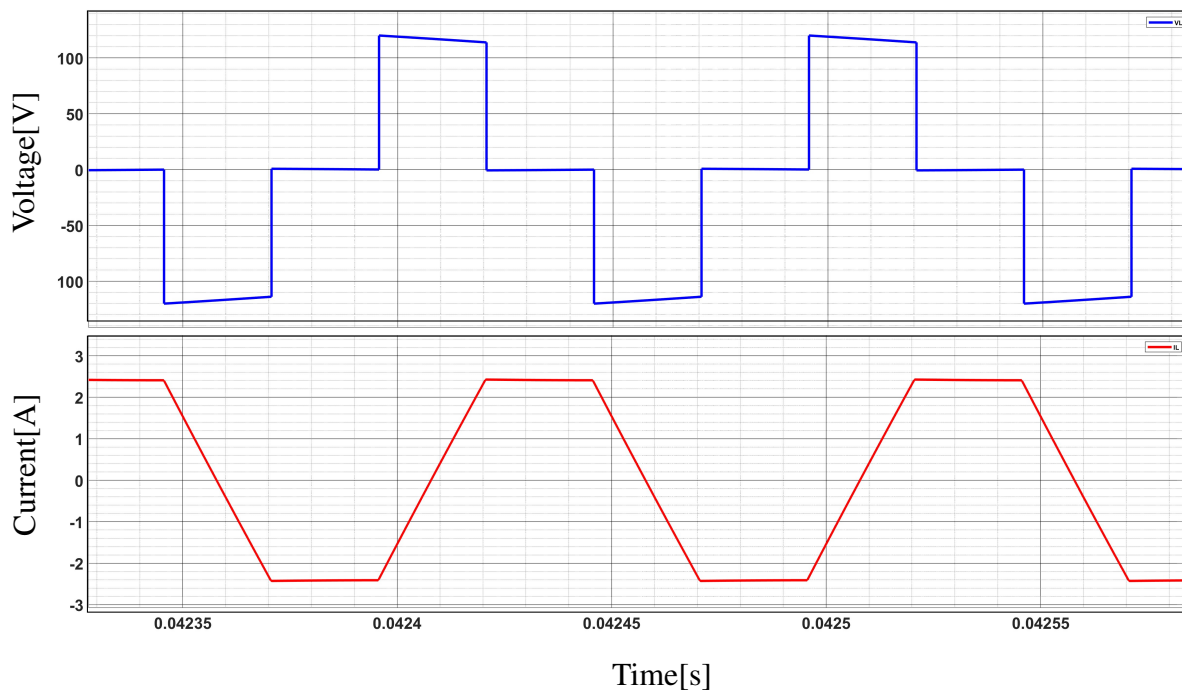
Figure 4.8: Matlab/simulink waveforms of inductor characteristics with a phase-shift value of 0.5
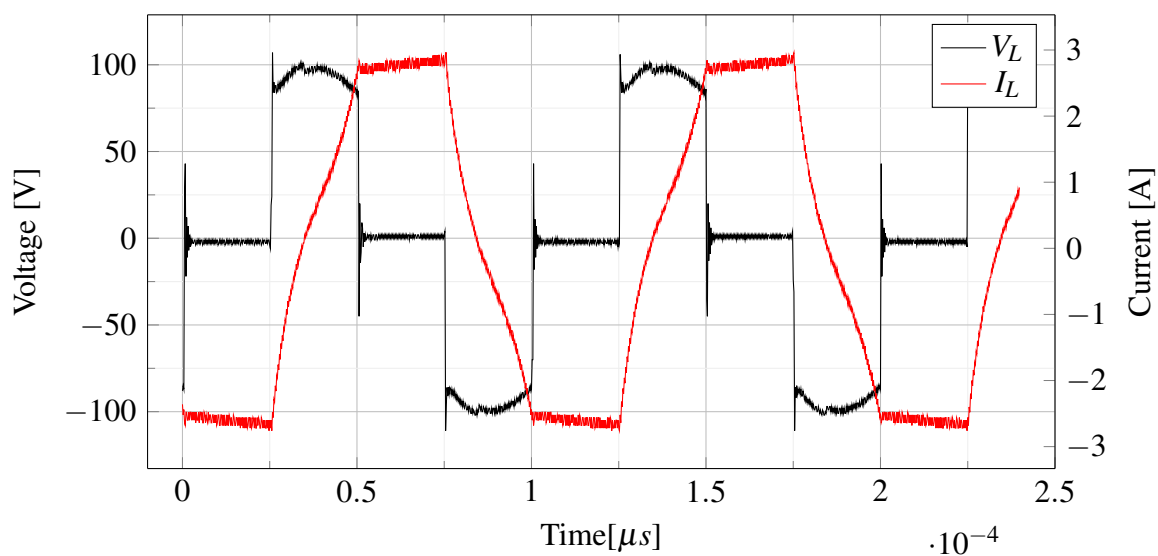
Figure 4.9: Hardware prototype waveforms of inductor characteristics with a phase-shift value of 0.5

When the phase-shift value D changes whit a step of 0.1, the phase shift should in theory, simulation, and in the prototype change with $5\mu s$. However, where this was accurate for any value above D = 0.2, there were anomalies for lower values. When no phase shift was produced (D = 0), both simulation and hardware prototype phase-shifted with $4.5\mu s$. At D=0.1, the Matlab/Simulink model resulted in a phase-shift of $6\mu s$, and the hardware prototype experienced a phase shift of $9\mu s$. This is a consequence of the applied interlock delay time which results in a dead-time of $4.5\mu s$.

4.4   Power Flow Determined by Phase-Shift Value

A series of power results have been gathered from the hardware prototype of the DAB converter. The phase-shift value was controlled by the PWM modes in the STM32 CubeIDE software. DC voltage measurements was collected using the Hioki multimeter, and current measurement through averaging values on the oscilloscope using the Micsig current probe. The power source and load was swapped when power values for negative phase shift values where gathered.

Table 4.3 and 4.4 are results using inductor 1 and inductor 2, respectively. The most noteworthy result to compare are the overall efficiencies. Inductor 1 was not designed to withstand the power of the converter and hence dissipated a considerable amount of reactive power which causes heat loss. Inductor 2 could withstand the high current considerably better than inductor 1.

D	V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
-0.5	60	1.44	47.7	0.952	86.4	45.4	0.525
-0.4	60	1.24	49.0	1.01	74.4	49.5	0.665
-0.3	60	1.02	47.2	0.962	61.2	45.4	0.741
-0.2	60	0.768	40.5	0.840	46.1	34.0	0.738
-0.1	60	0.539	34.2	0.698	32.3	23.9	0.740
0.0	60	0.526	31.6	0.640	31.6	20.2	0.639
0.1	60	0.641	36.0	0.781	38.5	28.1	0.731
0.2	60	0.810	41.7	0.891	48.5	37.2	0.767
0.3	60	1.08	48.2	1.03	64.8	49.7	0.767
0.4	60	1.40	53.1	1.13	84.0	60.0	0.714
0.5	60	1.54	55.3	1.12	92.4	59.7	0.646

Table 4.3: Power results with varying phase shifts when using inductor 1 and an applied primary voltage of 60V

D	V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
-0.5	60	1.15	53.6	1.07	69.0	57.4	0.832
-0.4	60	1.01	50.7	1.01	60.6	51.2	0.845
-0.3	60	0.749	44.1	0.876	44.9	38.6	0.860
-0.2	60	0.480	35.4	0.705	28.8	25.0	0.868
-0.1	60	0.431	33.3	0.668	25.9	22.3	0.861
0	60	0.261	23.9	0.480	15.7	7.5	0.478
0.1	60	0.440	34.6	0.660	26.4	22.8	0.864
0.2	60	0.521	36.5	0.734	31.3	27.0	0.863
0.3	60	0.754	45.2	0.887	45.2	40.1	0.888
0.4	60	1.02	51.8	1.01	61.2	52.3	0.855
0.5	60	1.18	55.4	1.11	70.8	61.5	0.869

Table 4.4: Power results with varying phase shifts when using inductor 2 and an applied primary voltage of 60V

Table 4.5 are results using an input voltage of 120V, which is close to the power values that the converter was designed for. However, the converter could not reach results for an applied phase-shift value of -0.5, or 0.5, since at this point some of the components started to overheat.

Increasing the applied power does increase the efficiency by a small factor. All of these results also validates that the power on the secondary side can be changed as a function of the applied phase-shift between the two full bridges.

D	V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
-0.5	n/a	n/a	n/a	n/a	n/a	n/a	n/a
-0.4	120	3.52	119.9	2.41	422	241	0.685
-0.3	120	2.10	100	2.02	252	197	0.802
-0.2	120	1.15	75.8	1.55	138	117.5	0.851
-0.1	120	0.92	70.1	1.43	110	100.2	0.911
0.0	120	0.60	52.6	1.11	72	58.4	0.811
0.1	120	1.09	75.7	1.52	130	115.1	0.885
0.2	120	1.20	80.0	1.60	144	128	0.889
0.3	120	2.10	105.9	2.09	251	213	0.882
0.4	120	3.89	141.8	2.90	466	411	0.883
0.5	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Table 4.5: Power results with varying phase shifts when using inductor 2 and an applied primary voltage of 120V

4.4.1 Voltage Ratio to Achieve ZVS

Table 4.6 are results where ZVS is achieved in both bridges, which, as described in section 2.4.1, is when the voltage-ratio in the converter is equal to 1. The converter is tuned until V_{prim} and V_{sec} are equal, and then the power values are measured. The converter could not reach this for lower phase-shift ratios because of the power source limits.

The results do not indicate that the efficiency increase by any considerable value, which could be because the switching losses are not substantial in this converter or that ZVS is not implemented correctly.

D	V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
0.3	160	3.57	160	3.20	571.2	512	0.896
0.4	100	2.23	100	1.96	223	196	0.880
0.5	77,4	1.81	77.4	1.48	140.1	114.5	0.818

Table 4.6: Power results with varying phase shifts and achieving ZVS using inductor 2

4.4.2 Power Flow Results From Matlab/Simulink Model

Power results from simulation was also acquired using both a primary voltage of 120V and 60V. The results are mirrored and therefore only the absolute values are presented.

|D|	P_{prim}[W]	P_{sec}[W]	η
0.0	31.9	29.1	0.92
0.1	48.6	45.7	0.94
0.2	100.0	95.5	0.96
0.3	167.5	158.5	0.94
0.4	216.9	202.0	0.93
0.5	234.8	214.7	0.91

(a) Applied voltage of 120V

|D|	P_{prim}[W]	P_{sec}[W]	η
0.0	9.4	8.6	0.92
0.1	13.4	12.7	0.94
0.2	29.4	28.1	0.96
0.3	49.3	46.5	0.94
0.4	63.8	59.2	0.93
0.5	69.1	62.8	0.91

(b) Applied voltage of 60V

Table 4.7: Power results with varying phase shifts from the Matlab/simulink model

4.4.3 Variations in Load

Table 4.8 and 4.9 shows power results with variation different restive loads values. The first one with 25Ω, and the second with 75Ω. Neither of the changes seems to increase the efficiency of the converter, but does changes the secondary voltage levels and hence the secondary power. Which is as expected according to eq. 3.3 in section 3.1.1.

D	V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
0.0	60	0.207	12.0	0.458	12	5.5	0.458
0.1	60	0.336	18.7	0.732	20	13.7	0.684
0.2	60	0.464	23.0	0.912	28	21.0	0.75
0.3	60	0.489	23.7	0.941	29	22.3	0.769
0.4	60	0.596	26.2	1.04	36	27.3	0.757
0.5	60	0.658	27.1	1.08	39	29.3	0.751

Table 4.8: Power results with varying phase shifts when using inductor 2 and an applied voltage of 60V, load of 25 Ohm

D	V_{prim}[V]	I_{prim}[A]	V_{sec}[V]	I_{sec}[A]	P_{prim}[W]	P_{sec}[W]	η
0.0	60	0.298	32.8	0.406	18	13.3	0.740
0.1	60	0.456	42.6	0.538	27	22.9	0.845
0.2	60	0.646	51.1	0.657	39	33.6	0.862
0.3	60	1.08	65.6	0.850	65	55.8	0.859
0.4	60	1.54	77.0	0.981	93	75.5	0.812
0.5	60	1.93	84.3	1.09	116	91.9	0.792

Table 4.9: Power results with varying phase shifts when using inductor 2 and an applied voltage of 60V, load of 75 Ohm

4.5 Bidirectional Inductor Characteristics

Bidirectional flow was implemented in the hardware converter model converter and power flow values was presented in the previous section. Figure 4.10 is the inductor characteristics with the phase shift resulting in maximum power transfer in forward mode and figure 4.11 presents the inductor characteristics in backward more. These results were gathered to compare the series inductor characteristics of the two modes in the bidirectional converter.

The applied primary voltage of 60V, and inductor 2 was utilized. The most notable characteristic is the lower voltage spike in which occur in backward power flow compared with forward.
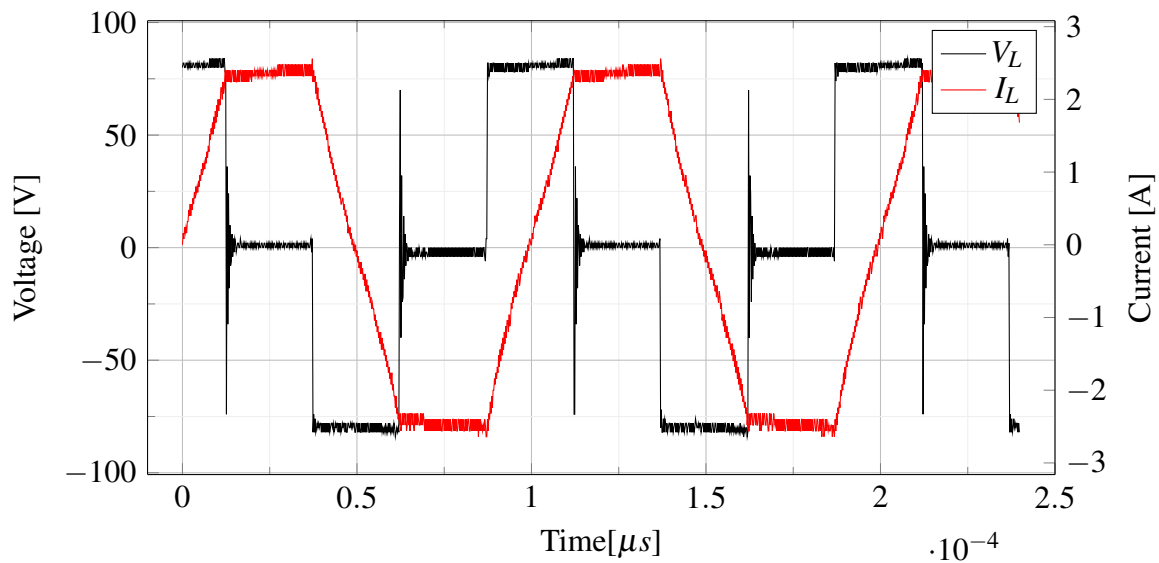

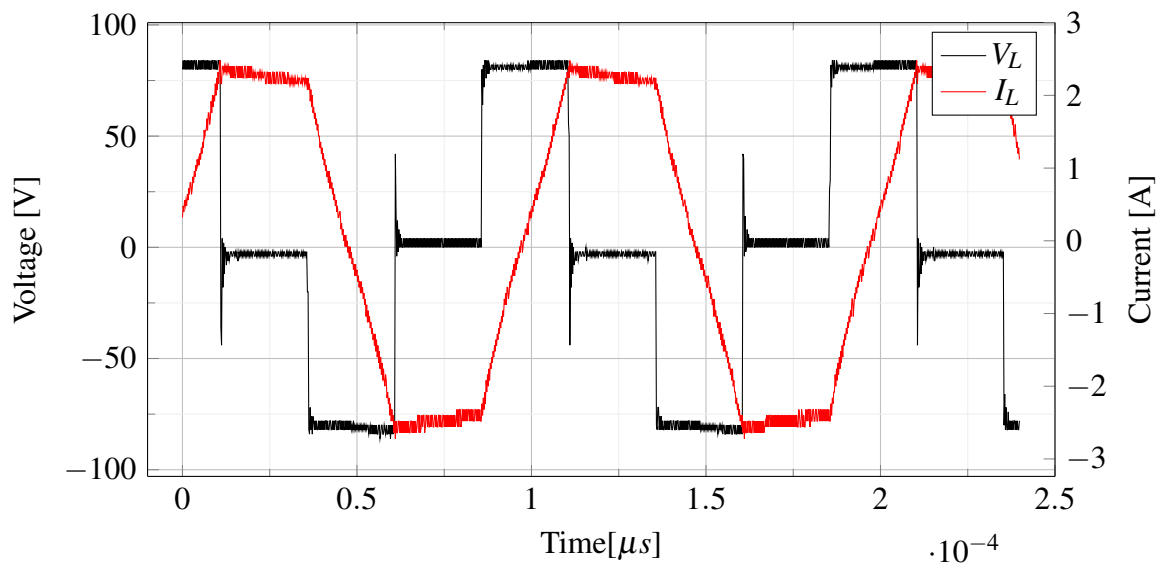Figure 4.10: Inductor voltage and current waveforms with implemented phase-shift of D=0.5

Figure 4.11: Inductor voltage and current waveforms with implemented phase-shift of D=-0.5

4.6   Heat Flow in the DAB Converter

Temperature was measured to see how the heat in the converter was distributed and of any elements experienced excessive heat which could indicate power losses.

The ambient temperatures of key components in the converter was attain using a Fluke Ti27 thermal camera. The four picture taken are shown below in figure 4.12, and a result of an 100 voltage, 2.3A applied primary voltage and current in the converter.

(a) Overview of the converter
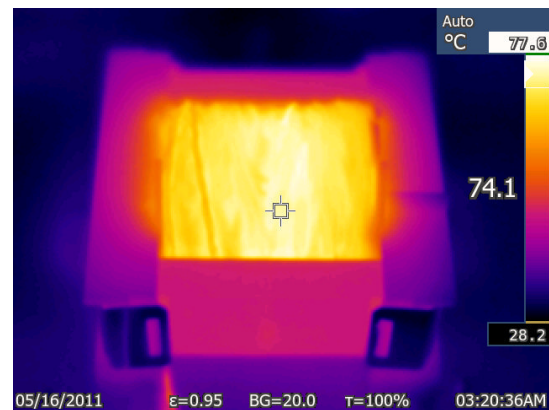
(b) HF Transformer

(c) Series inductor
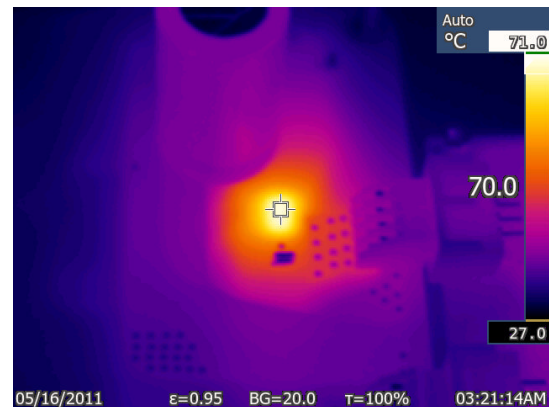
(d) Power Metal Strip Resistors

Figure 4.12: Thermal images of the DAB converter

The three elements that had an substantial increase in ambient temperature were the HF transformer, series inductor and the two metal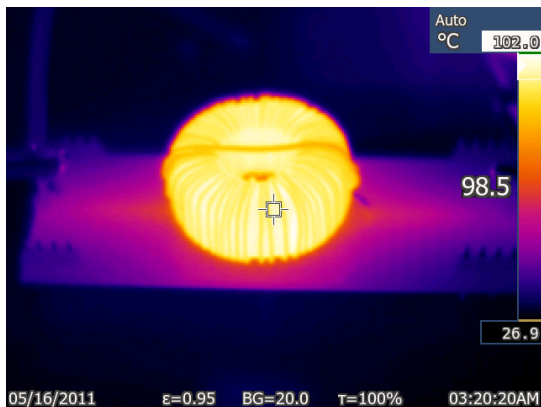 strip resistors. Referring to the datasheet in appendix C.3, the performance of the resistor starts to decrease after an ambient temperature of 70 °C. The exact same temperature as measured in figure 4.12d. During one of the tests with an applied primary voltage of 120V, one of the resistors reached a too high temperature and subsequently burnt.
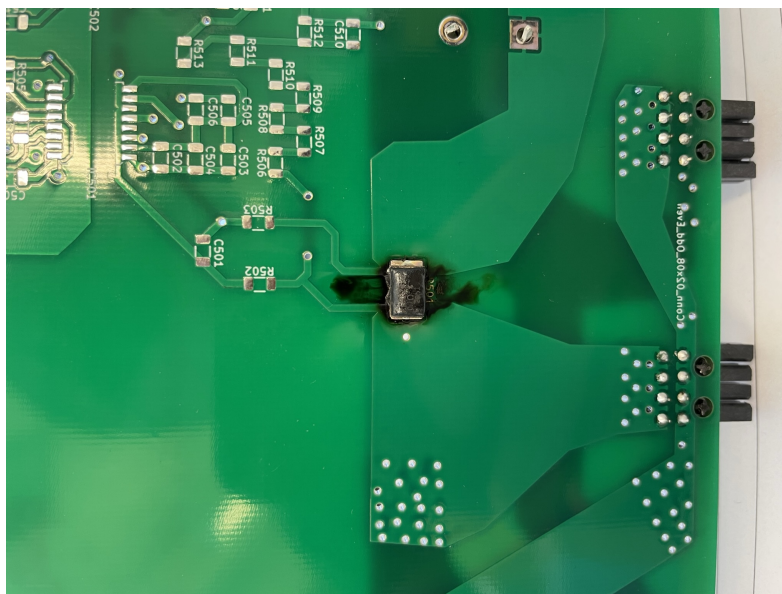
Figure 4.13: Destroyed WSHP2818 resistor

Chapter 5

Discussion

The discussion is divided into three primary parts. Section 5.1 discusses the functionality of the DAB DC/DC converter, the Matlab/simulink model in section 5.1.1, the hardware prototype in section 5.1.2, and compared them in section 5.1.3. In section 5.2 the efficiency of the converter is presented . Finally, section 5.3 discusses the power losses which occur in the hardware prototype of the converter and compares them to the power losses from the simulation model.

5.1 Functionality of the DAB Converter

The functionality of the DAB converter are determined by the following points.

- Have SPS modulation been implemented correctly by modifying the PWM signals which govern control of the converter.

- The topology and converter elements are designed properly and implemented so that the converter can vary output power and voltage.

- Does the converter function with bidirectional power flow and can it withstand the rated power values presented in section 3.1.

5.1.1 Simulation Model from Matlab/Simulink

The signals are generated and controlled correctly. The waveform are similar to what would be expected to form the theory with a correct implementation of dead-time though interlock delay time., switching frequency, and duty-cycle. Based on the dead-time observed in the physical prototype, and dead-time of $4.5\mu s$ was implemented in the simulation model as shown in figure 4.1.

Referring to tables 4.7b, 4.7a and the figures in section 4.3, the simulation shows correct implementation of controllable phase-shift to determine output values of the converter. One aspect that stands out is the phase shifts that occur when the applied phase shift is less than D=0.2 the measured phase shift does not correlate with implementation. This is pretty likely an effect of the dead-time which was implemented. The reason is that when no phase-shift is applied, the phase-shift appearing is the same as the applied dead-time. Moreover, when D=0.1 is applied, the phase-shift over the inductor is two times the dead-time.

5.1.2   Hardware Prototype

The functionality of the hardware prototype of the DAB converter with SPS modulation begins with modifying the PWM signals in the microcontroller with the correct frequency, duty-cycle, controllable phase shift. They are then transmitted to the gate inputs of the IGBTs through the power modules driver circuit, which also integrates the interlock delay time.

Figures 4.2 and 4.3 show that the signals have been correctly modified and transported to the gate inputs on the primary and secondary full bridges with implemented interlock delay time. The figures from the hardware prototype in 4.3 show that SPS modulation has been successfully achieved in the converter as well as bidirectional power flow. Like the simulation model, the dead-time affects the phase shift, which occurs for the smaller phase-shift ratios. When no phase-shift is applied, the phase-shift which appears is equal to the dead-time. And when D=0.1 is applied, the phase-shift which occurs over the series inductor is $6\mu s$.

The HF transformer was implemented and functioned as desired to achieve galvanic isolation. The transformer never reached saturation during the testing, but no tests were done to where the limit was. Table 4.1 from section 4.2 highlights the general functionality of the transformer and how the efficiency increases with applied power. In section 3.1.1 the transformer ratio was also measured to be approximately 1, but not exactly. Other tests to find the transformer's leakage inductance and the magnetizing current were not carried out, limiting the knowledge of this specific transformer.

5.1.3   Comparison

The comparison is based on the similarities and the dissimilarities on the waveforms provided in section 4.1, section 4.3 and appendix F. All results indicated that the signals in both simulation and hardware prototype are generated and modified correctly and provide the switching transient to ensure the operation of the DAB converter with SPS modulation. The phase-shift ratio correlated with the implemented phase-shift value in both the simulation and hardware prototype, and the converter functioned with bidirectional power flow.

One difference is how the phase-shift varies because of the influence of dead-time for the smaller values of D. This is most clear at D=0.1, where the phase-shift differs from the simulation and the hardware prototype of $3\mu s$.

Figure 5.1 displays the power flow as a function of the phase shift ratio, where positive power indicates forward flow and negative backward. The dotted line is the theoretical values calculated from equation 2.19 in section 2.2. The line from the hardware prototype is taken from table 4.4 and the red line, which is values from the Matlab/Simulink model, is table 4.7b. They all show how the power flow varies as a function of the phase shift with bidirectional power flow. The simulation and hardware prototype results show smaller output values because of power losses and the problems around D=0.
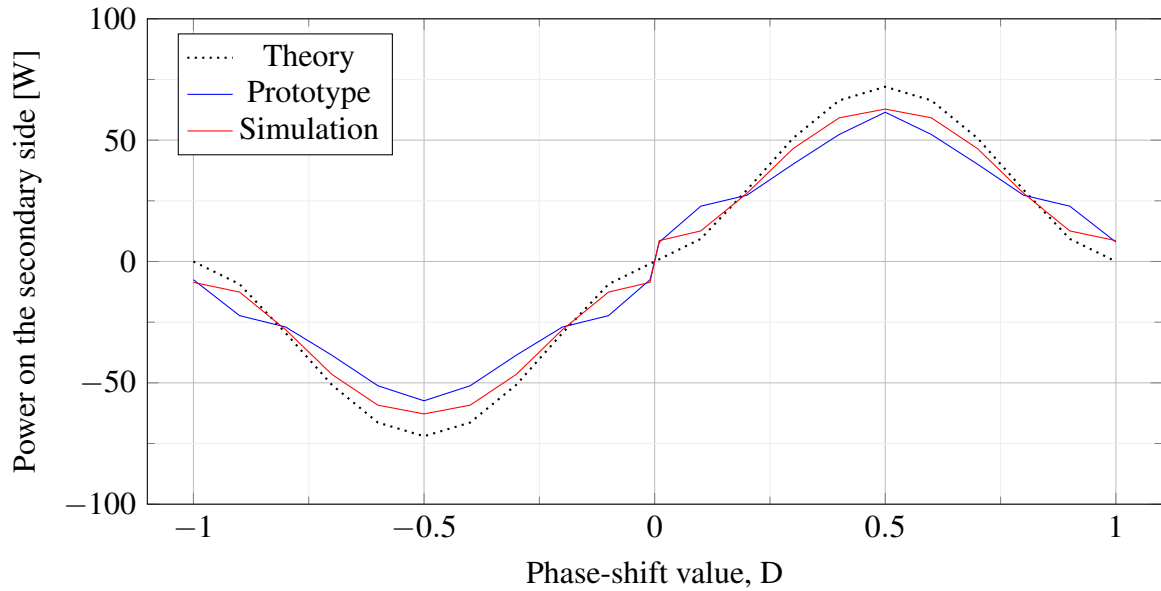

Figure 5.1: Power flow as a function of phase-shift

5.2 Efficiency

This section will analyze the efficiency through the hardware prototype and Matlab/simulink model of the DAB converter as a function of the phase-shift ratio. The power is governed by equation 3.2 which then results in the power on the secondary side as shown in 5.1. This is also true for negative phase-shift ratios and would result in the power flow in the opposite direction.

$$P_{sec} = I_{sec}^2 \cdot R_{load} \tag{5.1}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{sec}}{P_{prim}} \tag{5.2}$$

The results which are analysed in this section comes from the tables of results from table 4.3, 4.4, and 4.7b. When the preliminary testing was done on the operational principles of the converter, the inductor (Inductor 1) heated up substantially. There was no other inductor with similar properties available, so several tests were completed using this inductor. Figure 5.2 shows the efficiency as a function of the phase shift value. The blue is with inductor 1, the black with inductor 2, and the red line shows efficiencies from the Matlab/simulink model.
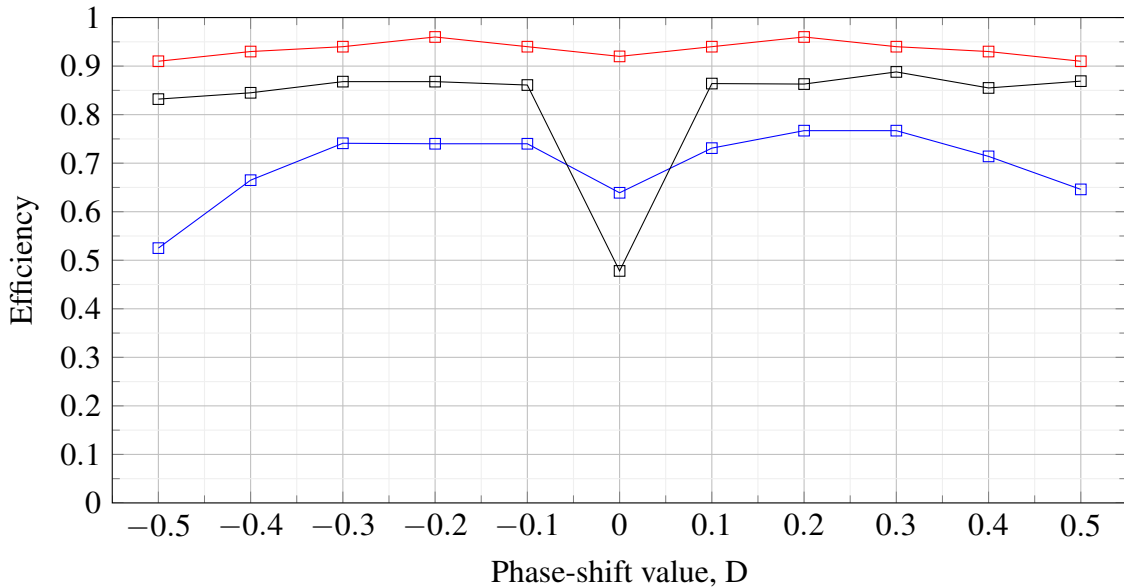

Figure 5.2: Efficiency as a function of phase-shift ratio through the hardware prototype of the DAB converter

As clearly shown in 5.2, inductor 2 substantially increased the efficiency by around 15 to 20% compared to inductor 1. The thicker wire and the metal is inductor two are much better for this hardware prototype.

The simulation shows a notable increase in efficiency, which is as expected since several power losses are not taken into consideration in the simulation.

Other tests with variation in load and input power also showed small variation in efficiency, presented in section 4.4. Both increasing and decreasing the load showed a decrease in overall efficiency, while an increase in applied power increased the efficiency in the converter.

However, over time, the higher power rating over time overheated some components, severely decreasing the efficiency and even destruction of the metal strip resistor as presented in section 4.6.

5.2.1 Zero-Voltage Switching

ZVS should, if implemented correctly decrease the switching losses in the transistors and hence increase the overall efficiency. The energy required is calculated as,

$$E_L = E_C \longrightarrow i_L = \sqrt{\frac{C_T V_T^2}{L}} \tag{5.3}$$

The other aspect of achieving soft-switching in the form of ZVS is a voltage ratio equal to 1, which was challenging to achieve for the full phase-shift range. The tests where both of these requirements were implemented and presented in section 4.4.1, table 4.6. The results do not show any notable increase in efficiency of the DAB converter. This could be because the switching losses, calculated in the next section, are not as prevalent compared to other losses such as convention in this hardware prototype. However, a designed converter with more focus and testing with soft-switching would probably achieve higher efficiency.

5.3 Power Losses

This section will analyze the most prevalent power losses (P_{loss}) which occur in the hardware prototype of the DAB converter. The values have been acquired directly from the appropriate datasheets found in appendix C.

Considering the power result test with 120V, inductor 2 and a phase shift of 0.4 from table 4.5:

$$P_{loss} = P_{prim} - P_{sec} = 55W$$

For this situation, there is 55 Watt dissipating in the DAB converter. The losses in the IGBTs, series inductor, and HF transformer are expected to be the most prevalent and are calculated for this specific result in the following sections.

5.3.1 IGBT Losses

Estimating the switching and conduction losses from the eighth power IGBTs, including the anti-parallel diode.

$$P_{con,IGBT} = V_f \cdot I_{avg} = 0.389W$$

$$P_{con,D} = V_D \cdot I_{avg} = 0.9W$$

$$P_{sw,IGBT} = (E_{on,IGBT} + E_{off,IGBT}) \cdot f_{sw} = 0.125W$$

$$P_{sw,D} = E_{on,D} \cdot f_{sw} = 0.015W$$

$$P_{IGBT,total} = 8 \cdot (P_{sw,T} + P_{sw,D} + P_{con,T} + P_{con,D}) \approx 11.5W \tag{5.4}$$

5.3.2   Power Losses from Transformer and Inductor

There is a clear power loss because of the inductor, can be clearly shown in figure 5.2 by comparing results from inductor 1 and inductor 2. Another aspect is when the inductor was taken out completely, results in an even more efficient converter. This converter could not regulate output and utilize phase-shift in the same way as the DAB, however, it indicates losses in the converter. The results are from section 4.2 and shown an higher efficiency then when the inductor was used.

$$P_{con,Transformer} = I_{L,rms}^2 \cdot (R_{prim} + R_{sec}) = 13.5W$$

$$P_{con,inductor} = I_{L,rms}^2 \cdot R_{ind} = 3.32W$$

$$P_{core,loss} = P_v \cdot A_E = 1.37W$$

Core losses in the inductor was not calculated since the required values was not provided in the datasheet. However, it is estimated to be quite low compared to the transformer core losses.

5.3.3   Total Power Losses

The total calculated losses is therefore approximately,

$$P_{loss} = 11.5W + 13.5W + 3.32W + 1.37W = 29.69W$$

for this instance, which only accounts for around half of the overall dissipated power. Other losses which has not been accounted for are conduction losses in the circuit board, including the two series resistor. The are also AC resistance losses in the inductor and transformer which have not been accounted for.

5.3.4   Power Losses in the Matlab/simulink Converter

The same parameters as for the calculations in the previous sections are used, which are the results from table 4.7a, section 4.4.2 where the primary voltage is 120V, inductor 2 is used, and the phase shift value (D) is 0.4. The power losses from the simulation is,

$$P_{loss} = P_{prim} - P_{sec} = 216.9W - 202.0W = 14.9W.$$

The only power losses embedded in the Matlab/Simulink model were the conduction losses in the inductor and HF transformer. Magnetic and losses form IGBTs were too challenging to implement precisely to represent the physical model. This will, of course, result in the simulation model being more efficient than the hardware prototype, as shown in figure 5.2. The only loss which can be compared is the conduction losses, which are only differentiated by 1.92 watts.

Chapter 6

Conclusions

6.1   Conclusion

This thesis presents a Matlab/Simulink simulation model and hardware prototype of a bidirectional Dual Active Bridge Converter for energy storage applications. A high-frequency transformer, interface circuit board, and microcontroller connections were designed and built for the hardware prototype, while Power modules had already been developed at HVL and could be implemented. Both systems utilize SPS modulation with a controllable phase shift ratio to determine the direction of power flow and output power values.

The results showed that power flow using SPS modulation was accurately implemented in both the simulation and hardware prototype. The only error was because of the implemented interlock-delay time, which affected the low phase-shift ratio in the converter.

The efficiency of the hardware prototype was shown to be around 0.82 to 0.9, while the simulation model reached a higher efficiency of 0.91 to 0.96. Several of the power losses in the hardware were challenging to account for, so the only losses realized in the simulation model were the conduction losses in the series inductor and HF transformer. The estimated losses in the hardware prototype accounted for approximately 50% the total dissipated power.

6.2   Further work

Since the hardware prototype works as a bidirectional dual active bridge converter, more work could be done to elevate the project's hardware and software side. The following points are suggestions further to develop the bidirectional DAB Converter.

- Implement other modulation techniques, such as those mentioned in section 2.2.3 and compare them to each other. Evaluate if they can reduce the transistors' current stress and ensure a wide ZVS range.

- Optimize the converter by minimizing power losses, for example, by designing and implementing snubber-circuits or evaluating different transformer concepts (planar cores, E-core).

- Apply the voltage and current measurement circuits and utilize them to implement a control system using a PI-regulator or another control system. A robust and fast dynamic

response is essential for DAB converters in industry applications.

- Implement control methods such as direct power control to achieve a dynamic response. The output voltage is controlled by the amount of power flow, while the power flow depends on the phase shift ratio between the primary and secondary bridge.

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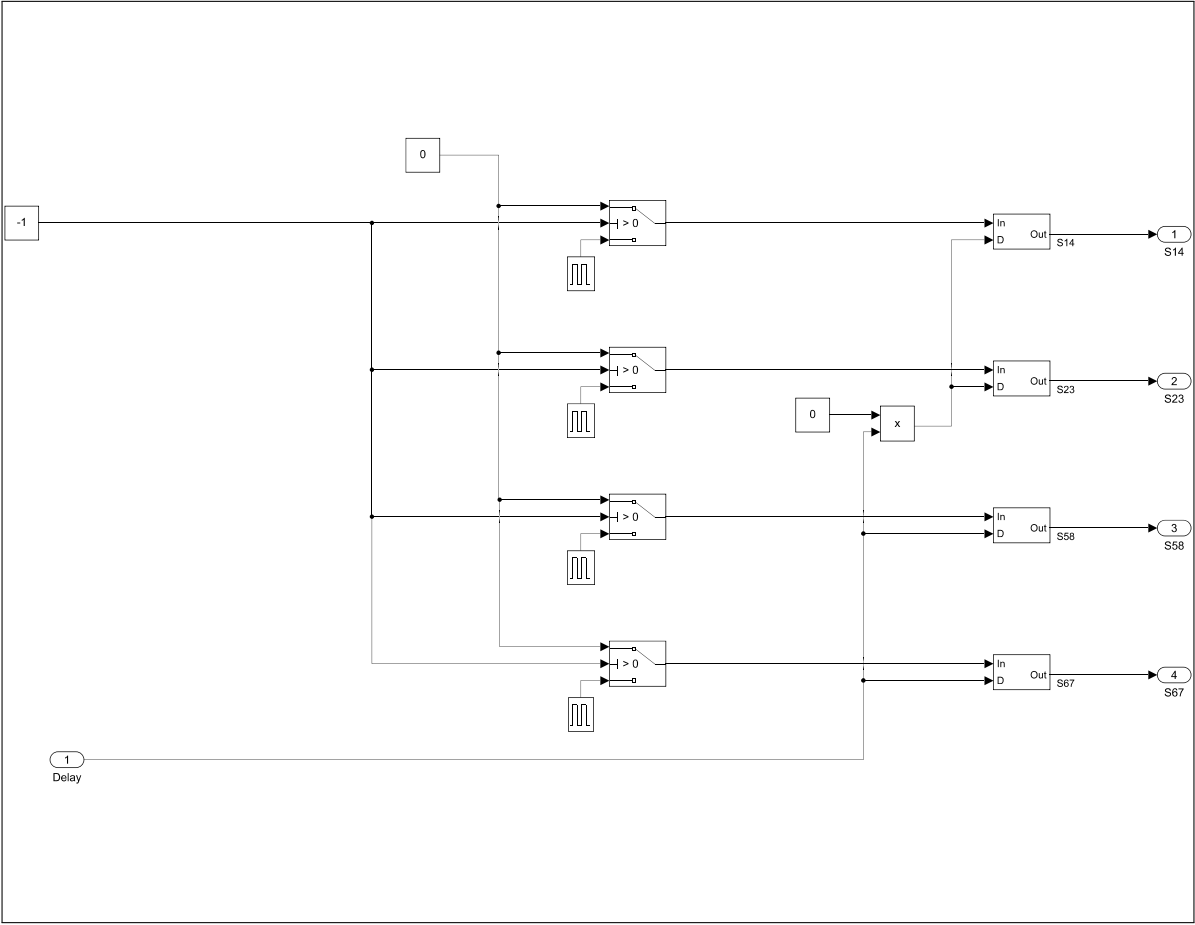
Appendix A

DAB converter simulation model

A.1 Signal generation submodel
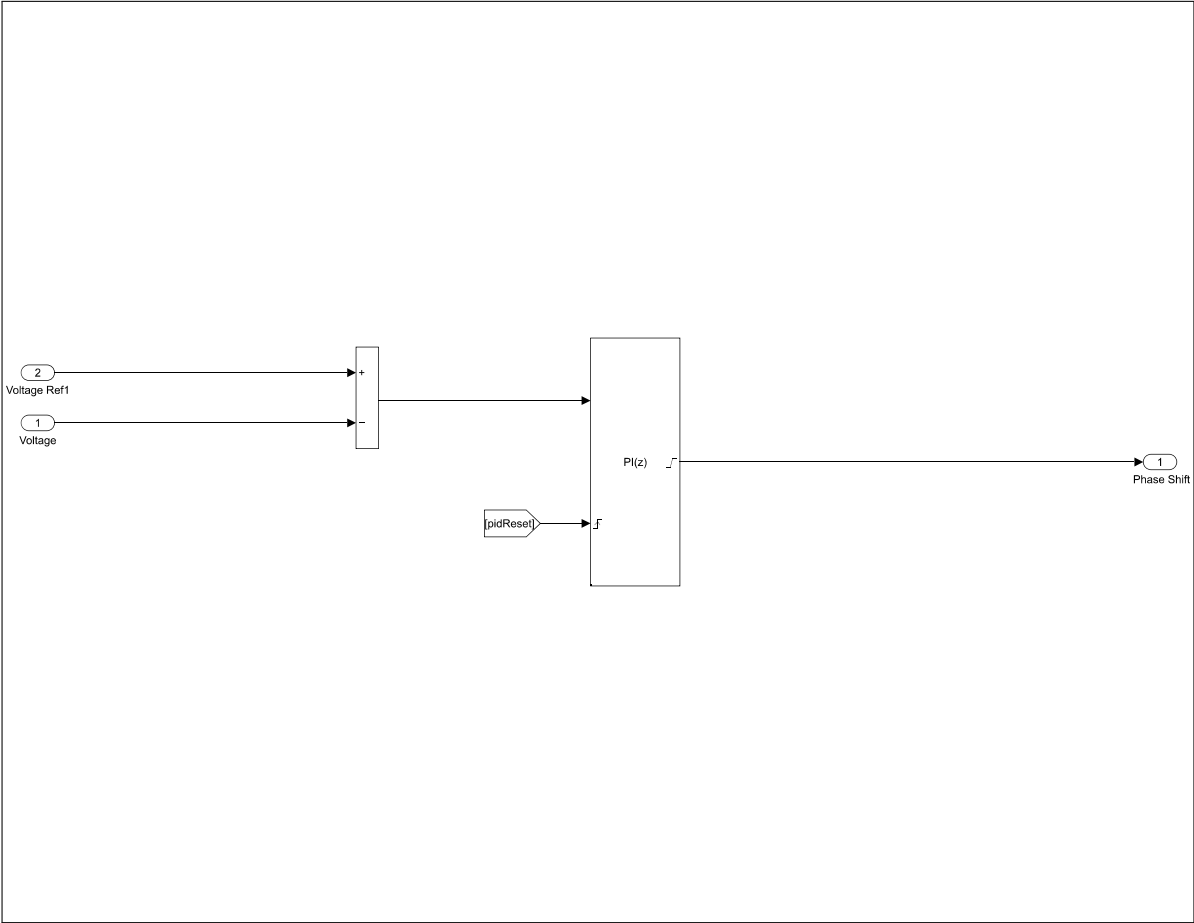
A.2   PI-regulator submodell

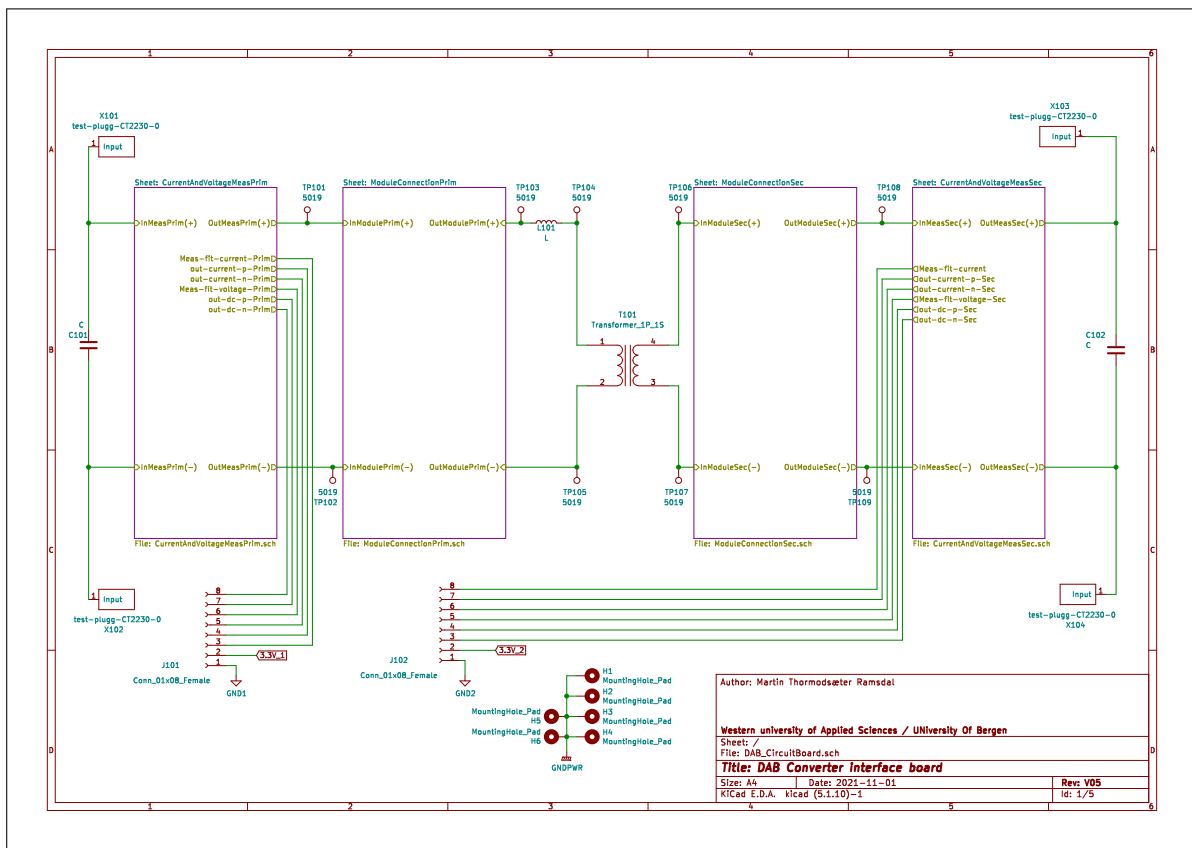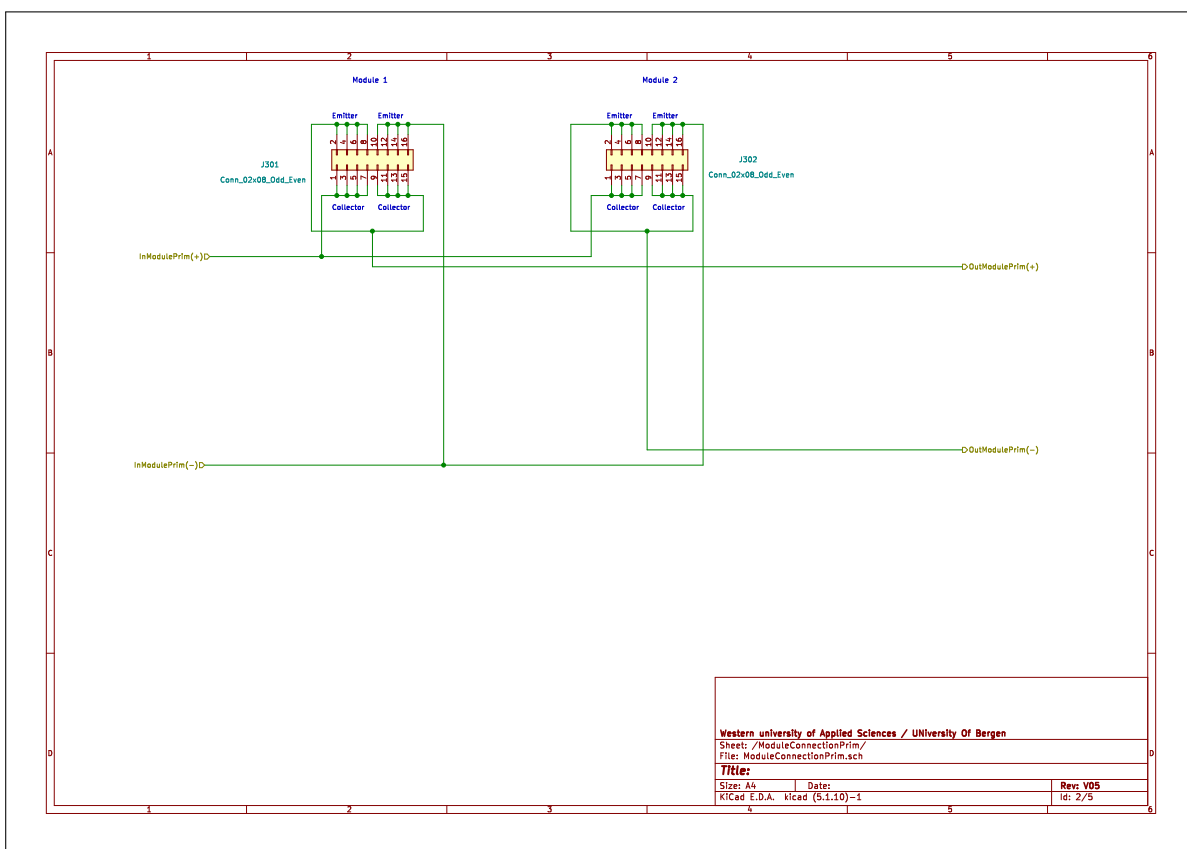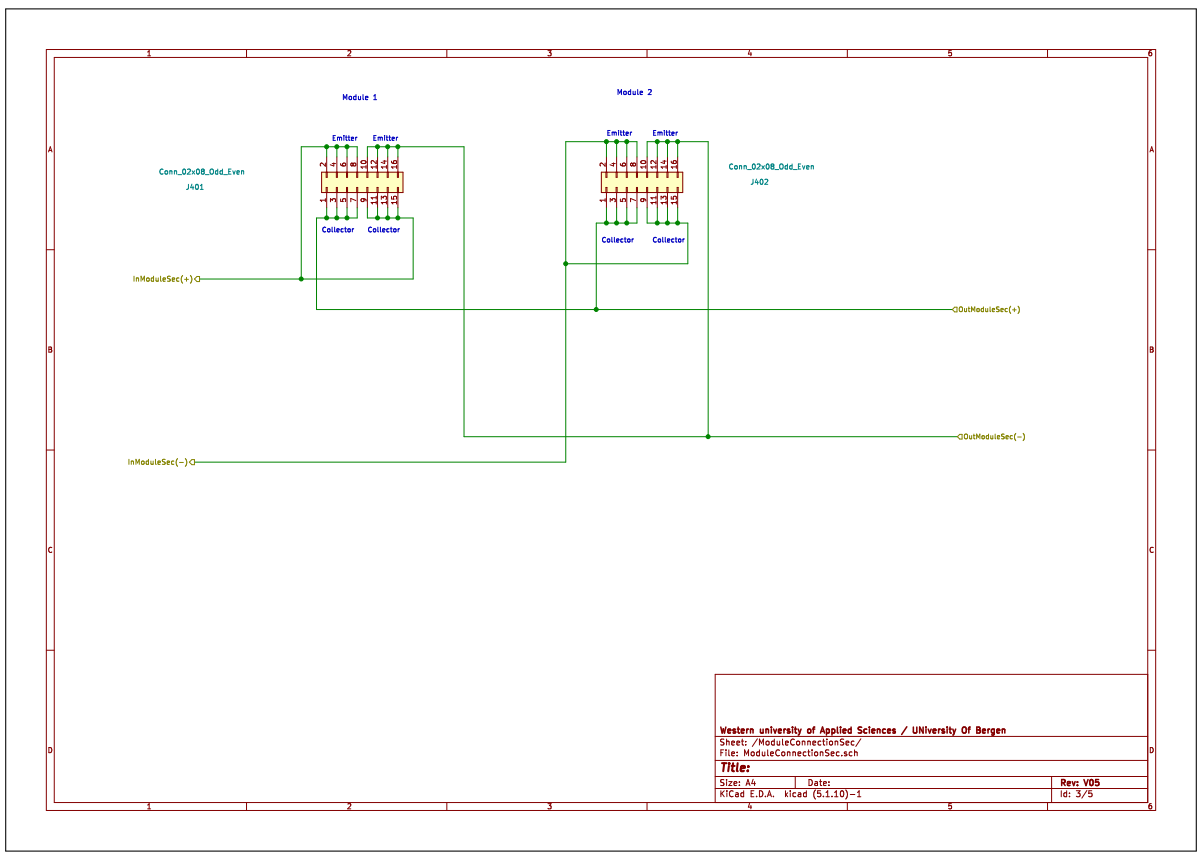# Appendix B

Schematics and PCB

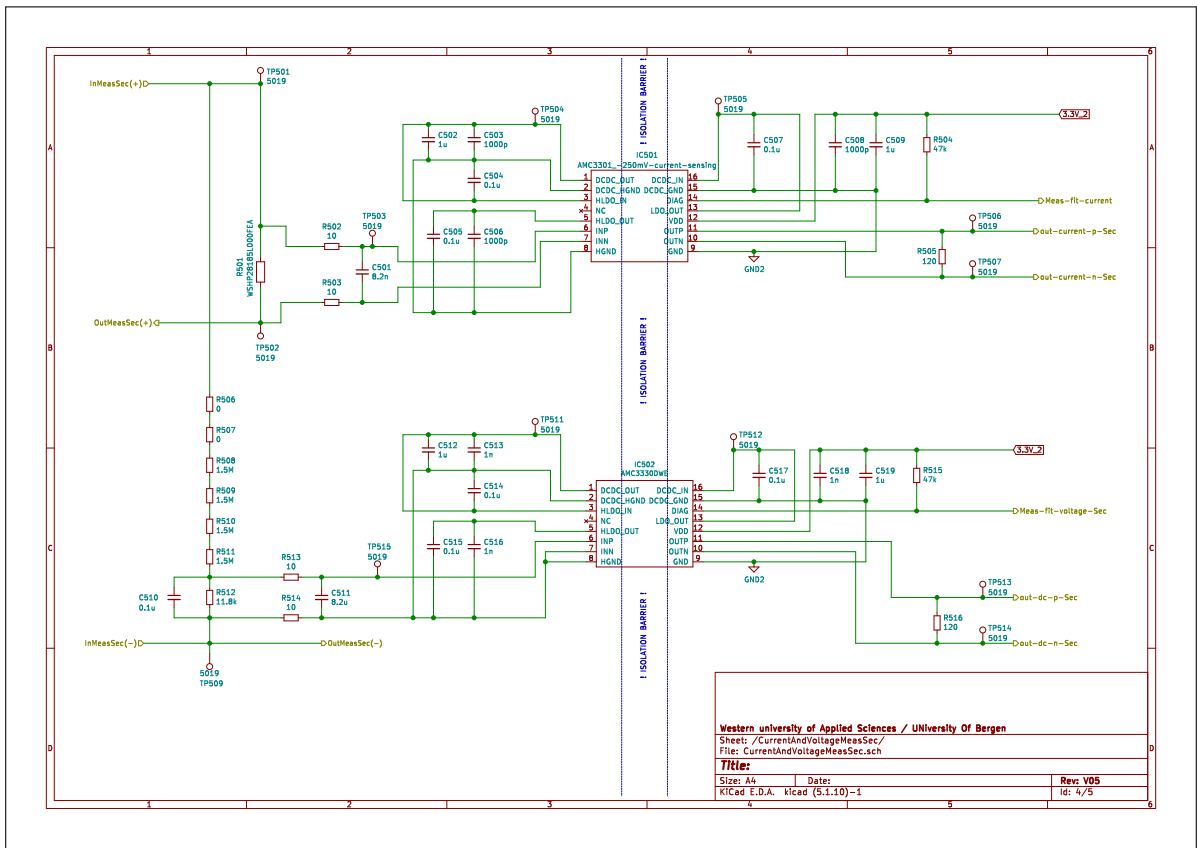# B.1   DAB converter interface board, Schematic
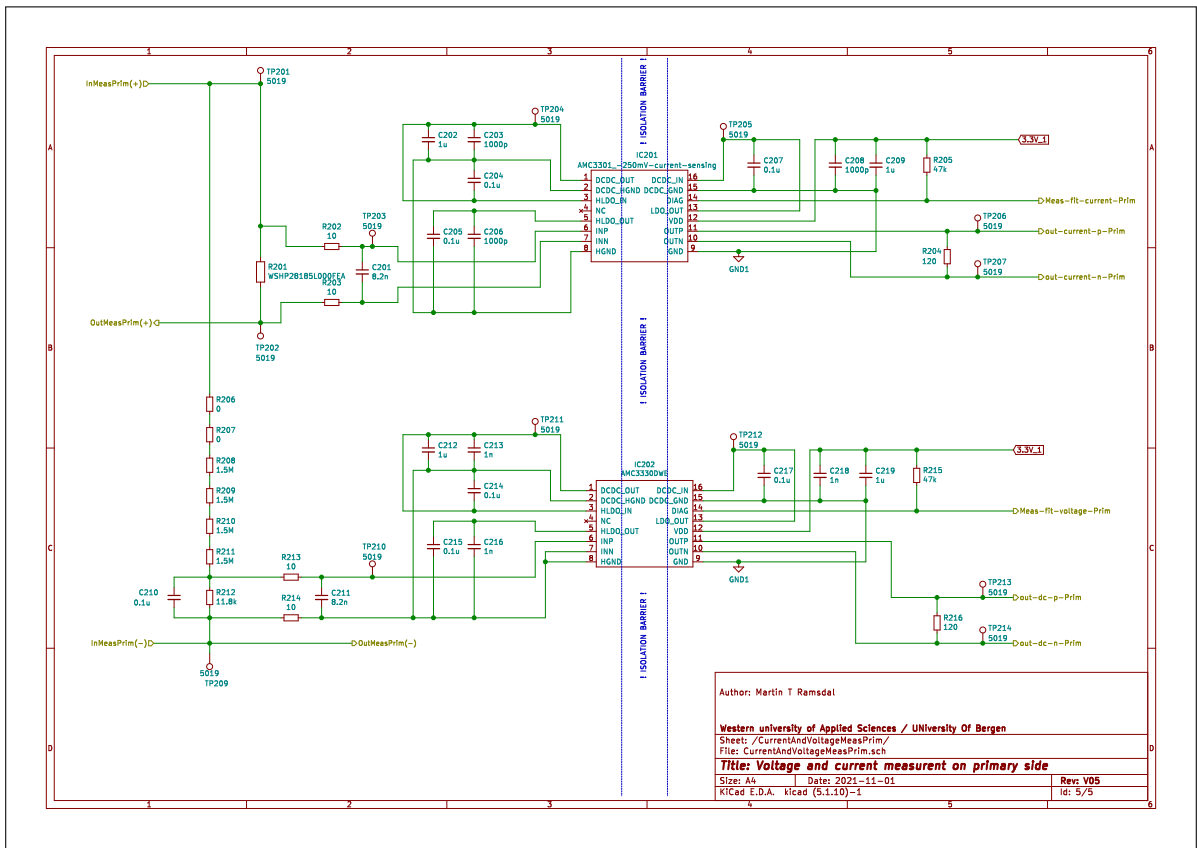
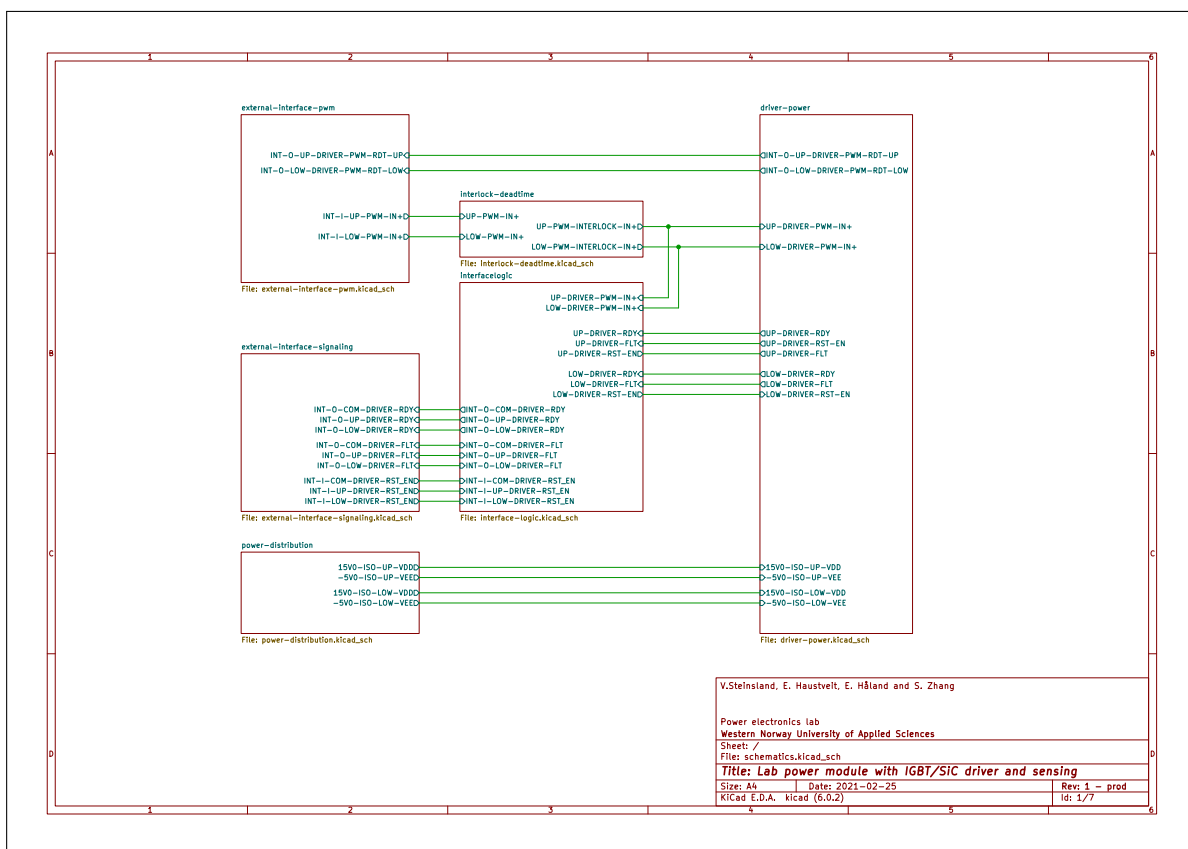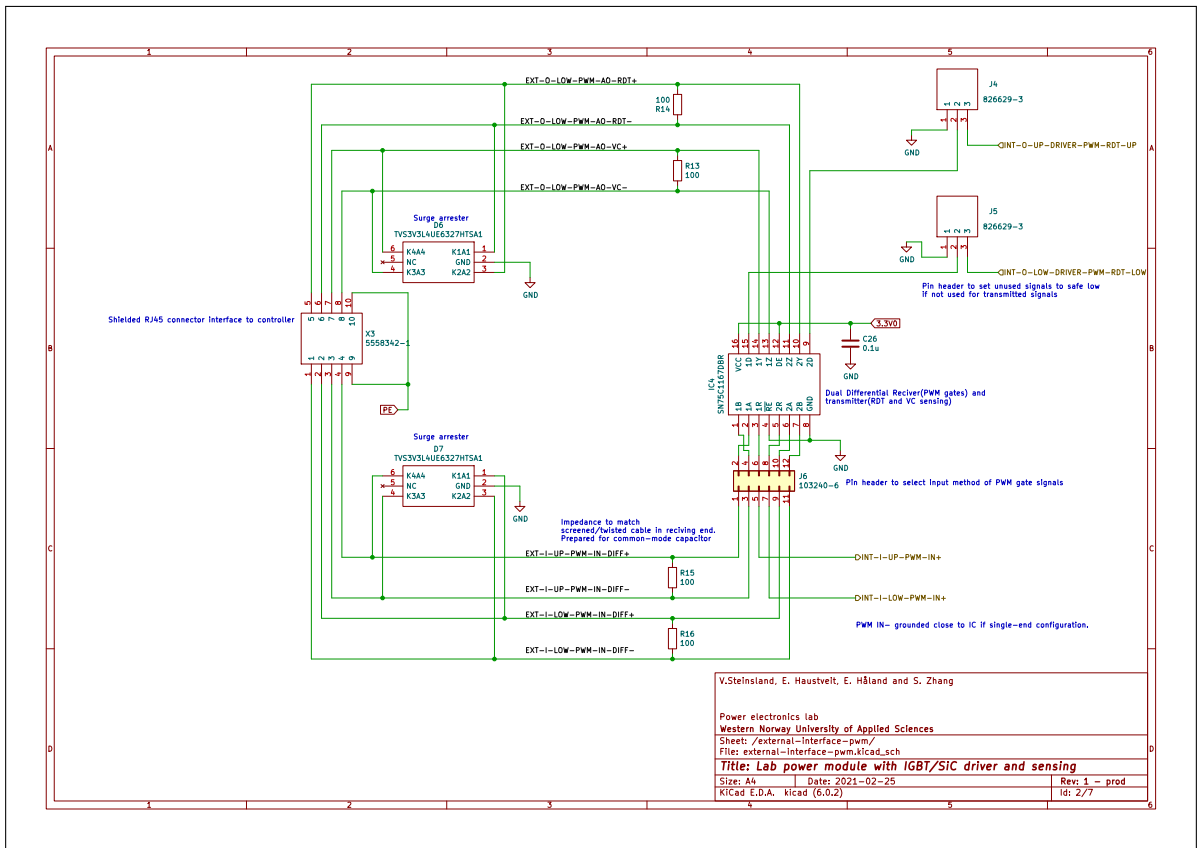## B.2   DAB converter interface board, PCB

B.3   Power module

Title: Lab power module with IGBT/SiC driver and sensing
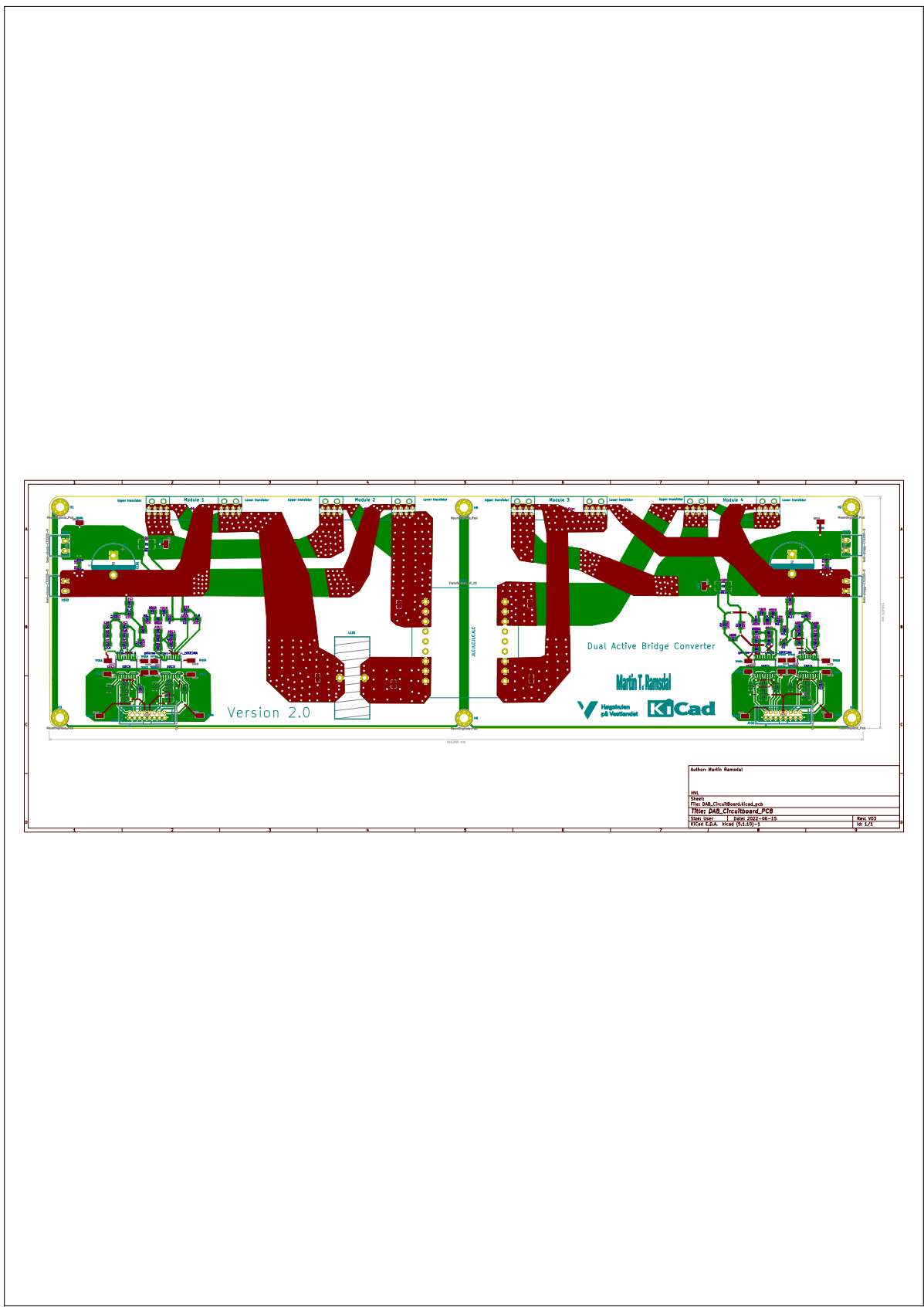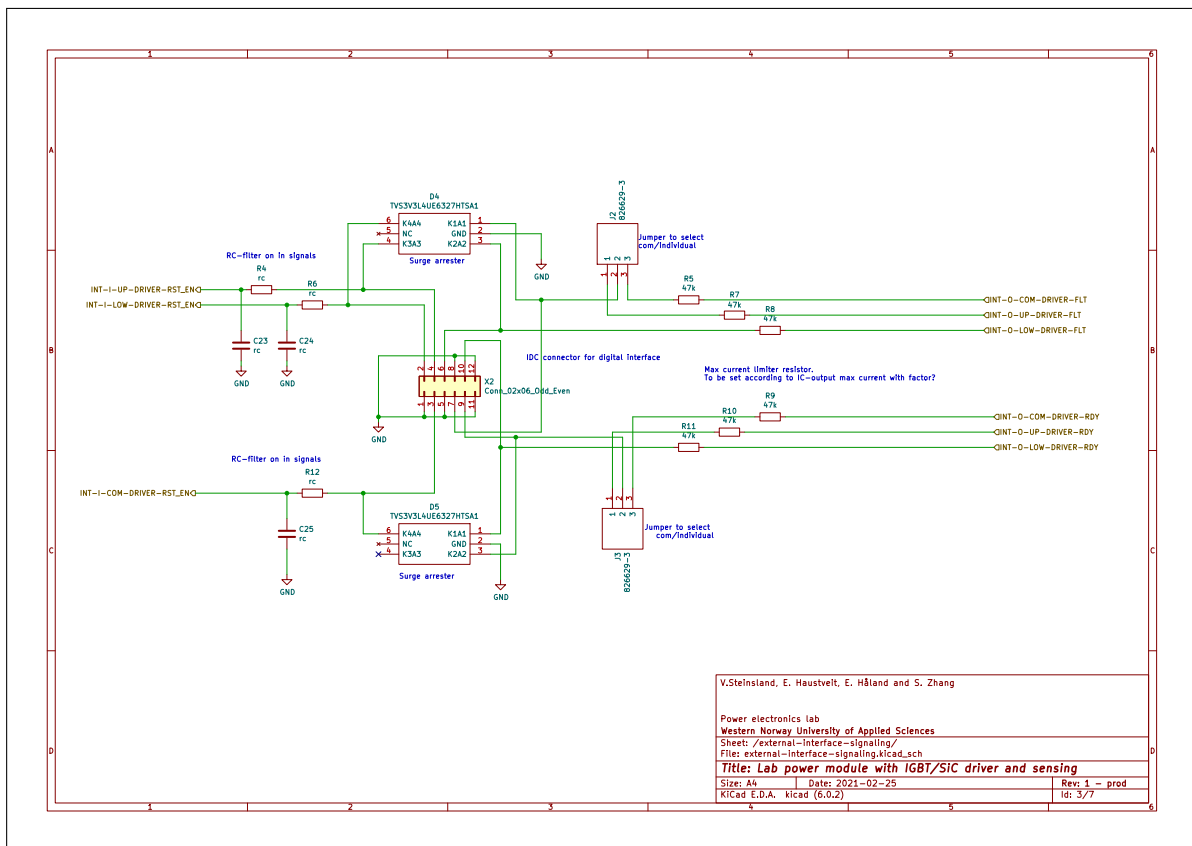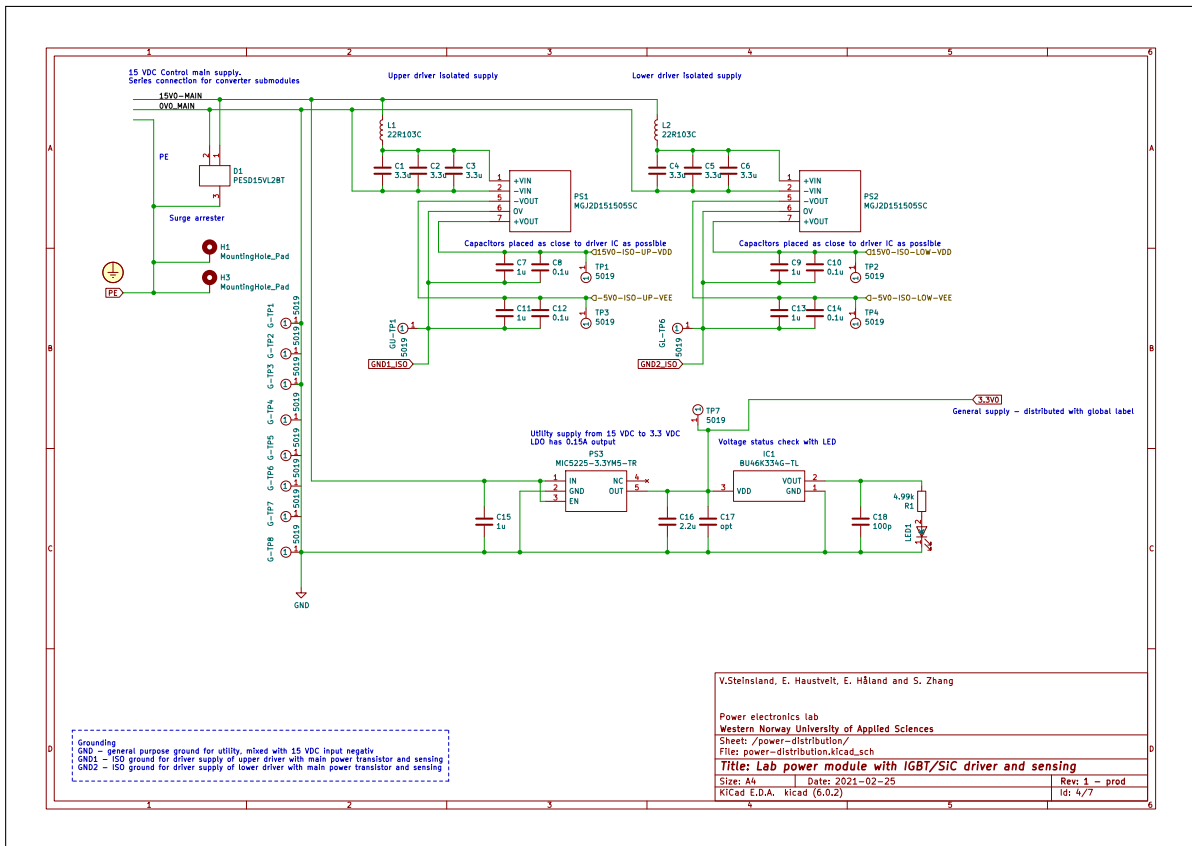
B.4 New voltage measurement circuits

B.5   Dual differential driver circuit schematic

B.6 Physical model of the interface card

Figure B.1: Top side of interface card
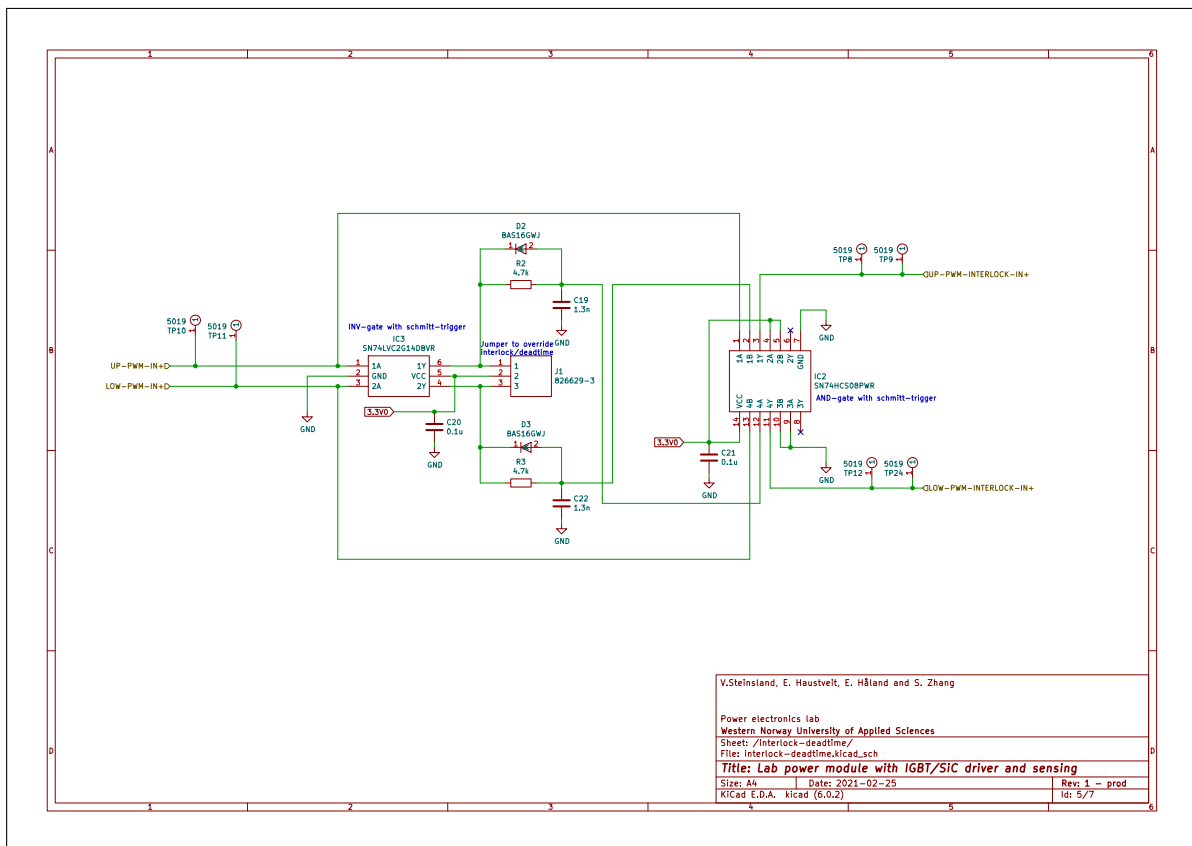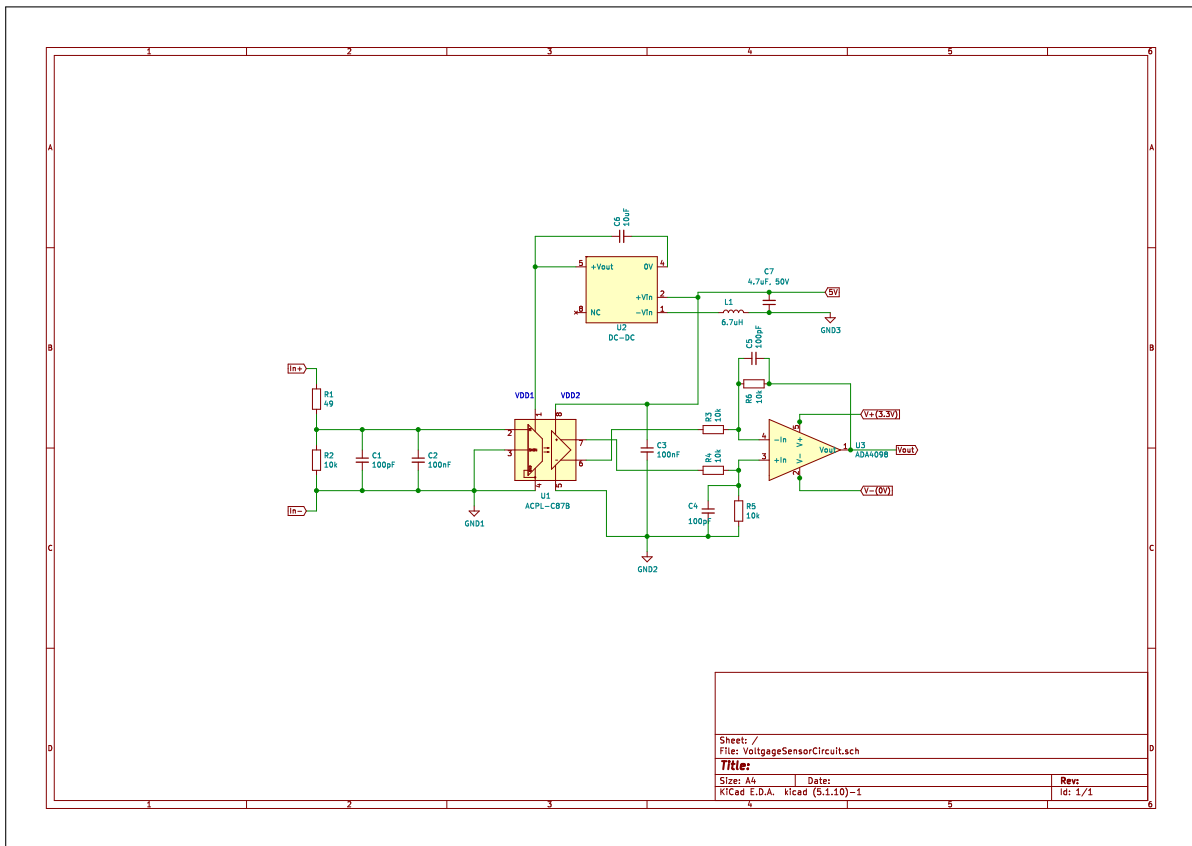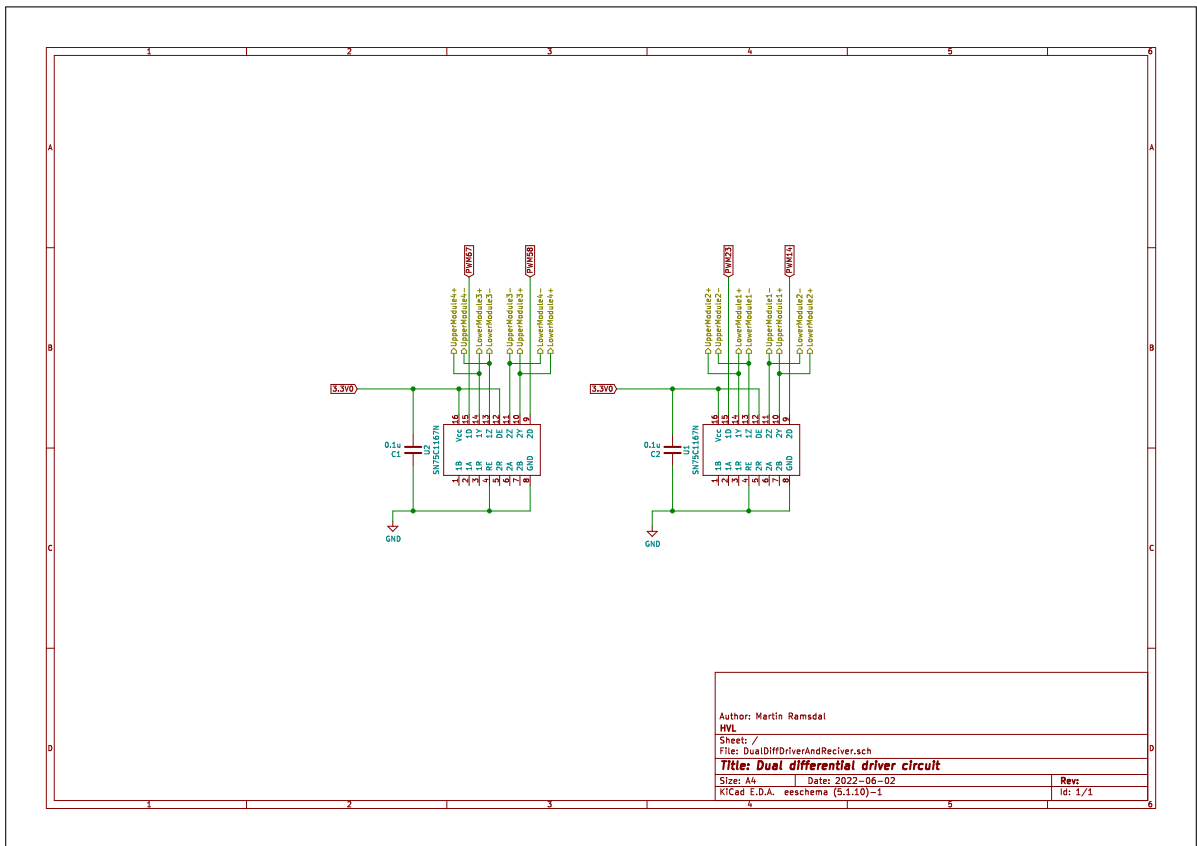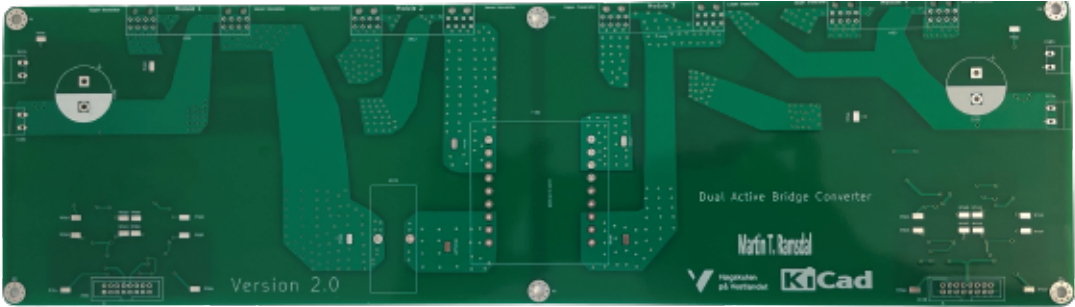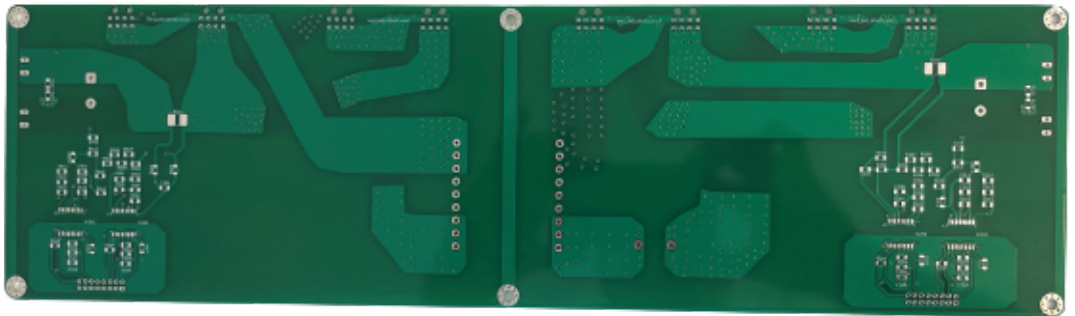

Figure B.2: Bottom side of interface card

Appendix C

Datasheets

Presents the most central datasheets used presented in the Thesis.

C.1   IGBTs

STGW60H65DFB, STGWA60H65DFB, STGWT60H65DFB

Datasheet

Trench gate field-stop 650 V, 60 A high speed HB series IGBT

TO-247

TO-247 long leads

TAB

TO-3P

C (2, TAB)

G (1)

E (3)
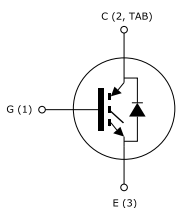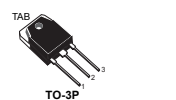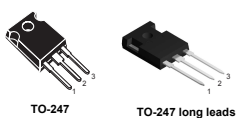
Features

- Maximum junction temperature: T_J = 175 °C
- High speed switching series
- Minimized tail current
- Low saturation voltage: $V_{CE(sat)}$ = 1.6 V (typ.) @ I_C = 60 A
- Tight parameter distribution
- Safe paralleling
- Positive $V_{CE(sat)}$ temperature coefficient
- Low thermal resistance
- Very fast soft recovery antiparallel diode

Applications

- Photovoltaic inverters
- High-frequency converters

Description

These devices are IGBTs developed using an advanced proprietary trench gate field-stop structure. These devices are part of the new HB series of IGBTs, which represent an optimum compromise between conduction and switching loss to maximize the efficiency of any frequency converter. Furthermore, the slightly positive $V_{CE(sat)}$ temperature coefficient and very tight parameter distribution result in safer paralleling operation.

STPOWER

Product status link
STGW60H65DFB
STGWT60H65DFB
STGWA60H65DFB

ST

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	650	V
I_C	Continuous collector current at T_C = 25 °C	80 [1]	A
	Continuous collector current at T_C = 100 °C	60	A
I_{CP} [2][3]	Pulsed collector current	240	A
V_{GE}	Gate-emitter voltage	±20	V
	Transient gate-emitter voltage (t_P ≤ 10 µs)	±30	V
I_F	Continuous forward current at T_C = 25 °C	80 [1]	A
	Continuous forward current at T_C = 100 °C	60	A
I_{FP} [2][3]	Pulsed forward current	240	A
P_{TOT}	Total power dissipation at T_C = 25 °C	375	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	°C

1. *Current level is limited by bond wires.*
2. *Pulse width is limited by maximum junction temperature.*
3. *Defined by design, not subject to production test.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case IGBT	0.4	°C/W
R_{thJC}	Thermal resistance junction-case diode	1.14	°C/W
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

2   Electrical characteristics

T_J = 25 °C unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V, I_C = 2 mA	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 60 A		1.60	2	V
		V_{GE} = 15 V, I_C = 60 A, T_J = 125 °C		1.75		
		V_{GE} = 15 V, I_C = 60 A, T_J = 175 °C		1.85		
V_F	Forward on-voltage	I_F = 60 A		2	2.6	V
		I_F = 60 A, T_J = 125 °C		1.7		
		I_F = 60 A, T_J = 175 °C		1.6		
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V			25	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±250	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	7792	-	pF
C_{oes}	Output capacitance		-	262	-	pF
C_{res}	Reverse transfer capacitance		-	158	-	pF
Q_g	Total gate charge	V_{CC} = 520 V, I_C = 60 A, V_{GE} = 0 to 15 V (see Figure 28. Gate charge test circuit)	-	306	-	nC
Q_{ge}	Gate-emitter charge		-	126	-	nC
Q_{gc}	Gate-collector charge		-	58	-	nC

STGW60H65DFB, STGWA60H65DFB, STGWT60H65DFB

Electrical characteristics

Table 5. IGBT switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time		-	66	-	ns
t_r	Current rise time		-	38	-	ns
$(di/dt)_{on}$	Turn-on current slope	V_{CE} = 400 V, I_C = 60 A,	-	1216	-	A/µs
$t_{d(off)}$	Turn-off delay time	R_G = 10 Ω,	-	210	-	ns
t_f	Current fall time	V_{GE} = 15 V (see Figure 27.	-	20	-	ns
E_{on} [1]	Turn-on switching energy	Test circuit for inductive load switching)	-	1590	-	µJ
E_{off} [2]	Turn-off switching energy		-	900	-	µJ
E_{ts}	Total switching energy		-	2490	-	µJ
$t_{d(on)}$	Turn-on delay time		-	59	-	ns
t_r	Current rise time		-	40	-	ns
$(di/dt)_{on}$	Turn-on current slope	V_{CE} = 400 V,	-	1230	-	A/µs
$t_{d(off)}$	Turn-off-delay time	I_C = 60 A, R_G = 10 Ω,	-	242	-	ns
t_f	Current fall time	V_{GE} = 15 V, T_J = 175 °C	-	147	-	ns
E_{on} [1]	Turn-on switching energy	(see Figure 27. Test circuit for inductive load switching)	-	2860	-	µJ
E_{off} [2]	Turn-off switching energy		-	1255	-	µJ
E_{ts}	Total switching energy		-	4115	-	µJ

1. *Including the reverse recovery of the diode.*
2. *Including the tail of the collector current.*

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time		-	60	-	ns
Q_{rr}	Reverse recovery charge	I_F = 60 A, V_R = 400 V,	-	99	-	nC
I_{rrm}	Reverse recovery current	V_{GE} = 15 V, di/dt = 100 A/µs	-	3.3	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b	(see Figure 27. Test circuit for inductive load switching)	-	187	-	A/µs
E_{rr}	Reverse recovery energy		-	68	-	µJ
t_{rr}	Reverse recovery time		-	310	-	ns
Q_{rr}	Reverse recovery charge	I_F = 60 A, V_R = 400 V, V_{GE} = 15 V,	-	1550	-	nC
I_{rrm}	Reverse recovery current	di/dt = 100 A/µs, T_J = 175 °C	-	10	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b	(see Figure 27. Test circuit for inductive load switching)	-	59	-	A/µs
E_{rr}	Reverse recovery energy		-	674	-	µJ

C.2 Dual driver and receiver

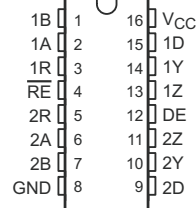![Texas Instruments logo] TEXAS INSTRUMENTS

SN65C1167
SN75C1167, SN65C1168, SN75C1168

DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

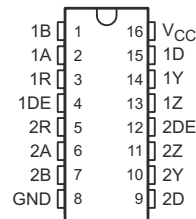Check for Samples: SN65C1167 SN75C1167 SN65C1168 SN75C1168

FEATURES

- **Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11**
- **BiCMOS Process Technology**
- **Low Supply-Current Requirements: 9 mA Max**
- **Low Pulse Skew**
- **Receiver Input Impedance . . . 17 kΩ Typ**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Common-Mode Input Voltage Range of −7 V to 7 V**
- **Operate From Single 5-V Power Supply**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Receiver 3-State Outputs Active-Low Enable for SN65C1167 and SN75C1167 Only**
- **Improved Replacements for the MC34050 and MC34051**

SN65C1167 . . . DB OR NS PACKAGE
SN75C1167 . . . DB, N, OR NS PACKAGE
(TOP VIEW)

1B	1	16	V_{CC}
1A	2	15	1D
1R	3	14	1Y
$\overline{RE}$	4	13	1Z
2R	5	12	DE
2A	6	11	2Z
2B	7	10	2Y
GND	8	9	2D

SN65C1168 . . . N, NS, OR PW PACKAGE
SN75C1168 . . . DB, N, NS, OR PW PACKAGE
(TOP VIEW)

1B	1	16	V_{CC}
1A	2	15	1D
1R	3	14	1Y
1DE	4	13	1Z
2R	5	12	2DE
2A	6	11	2Z
2B	7	10	2Y
GND	8	9	2D

DESCRIPTION

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

C.3   Power Metal Strip Resistors

VISHAY.
www.vishay.com

WSHP2818
Vishay Dale

Power Metal Strip® Resistors, High Power (10 W), Low Value (down to 0.001 Ω), Surface Mount

FEATURES

- Improved thermal management incorporated into design
- All welded construction of the Power Metal Strip resistors are ideal for all types of current sensing, voltage division, and pulse applications
- Proprietary processing technique produces extremely low resistance values
- Sulfur resistance by construction that is unaffected by high sulfur environments
- Very low inductance (< 5 nH)
- Low thermal EMF (< 3 µV/°C)
- Solid metal nickel-chrome or manganese-copper alloy resistive element with low TCR (< 20 ppm/°C)
- AEC-Q200 qualified [1]
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

e3

RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(5-2008)

DESIGN SUPPORT TOOLS

click logo to get started

3D Models Available

Design Tools Available

Notes
- Follow link to Overview of Automotive Grade Products for more details: www.vishay.com/doc?49924
[1] Flame retardance test may not be applicable to some resistor technologies

STANDARD ELECTRICAL SPECIFICATIONS

GLOBAL MODEL	SIZE	POWER RATING $P_{70\,°C}$ W	RESISTANCE VALUE RANGE Ω		WEIGHT (typical) g/1000 pieces
			Tol. ± 0.5 %	Tol. ± 1.0 %	
WSHP2818	2818	10 [1]	0.010 to 0.1	0.001 to 0.1	167.8

Note
[1] The WSHP2818 is rated at 10 W with maximum surface temperature of 200 °C based on 70 °C ambient temperature

GLOBAL PART NUMBER INFORMATION

Global Part Numbering: WSHP2818R1000FEA (visit www.vishay.net Vishay Dale parts numbering manual for all options)

| W | S | H | P | 2 | 8 | 1 | 8 | R | 1 | 0 | 0 | 0 | F | E | A | | |

GLOBAL MODEL (8 digits)	RESISTANCE VALUE (5 digits)	TOLERANCE CODE (1 digit)	PACKAGING CODE [1] (2 digits)	SPECIAL (up to 2 digits)
WSHP2818	**L** = mΩ* **R** = decimal **4L000** = 0.004 Ω **R0100** = 0.01 Ω * Use "**L**" for resistance values < 0.01 Ω	**D** = ± 0.5 % **F** = ± 1.0 %	**EA** = lead (Pb)-free, tape/reel **EK** = lead (Pb)-free, bulk	(dash number) from **1** to **99** as applicable

Note
[1] EB (lead (Pb) free) is a non-standard packaging code designated for 1000 piece reels. The non-standard packaging code is identical to our standard EA (lead (Pb) free), except that it has a package quantity of 1000 pieces

For technical questions, contact: ww2bresistors@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

VISHAY®

www.vishay.com

WSHP2818

Vishay Dale

TECHNICAL SPECIFICATIONS

PARAMETER	UNIT	RESISTOR CHARACTERISTICS
Component temperature coefficient (including terminal) [1]	ppm/°C	± 200 [4] for 1 mΩ to 5.99 mΩ
		± 75 [4] for 6 mΩ to 100 mΩ
Element TCR [2]	ppm/°C	< 20
Inductance	nH	< 5
Operating temperature range	°C	-65 to +170
Maximum working voltage [3]	V	$(P \times R)^{1/2}$

Notes

[1] Component TCR - total TCR that includes the TCR effects of the resistor element and the copper terminal
[2] Element TCR - only applies to the alloy used for the resistor element; refer to item 1 in the construction illustration on the following page
[3] Maximum working voltage - the WSHP is not voltage sensitive, but is limited by power / energy dissipation and is also not ESD sensitive
[4] Typical TCR is positive, for more details contact factory
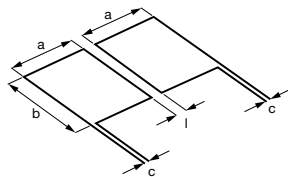
DIMENSIONS in inches (millimeters)
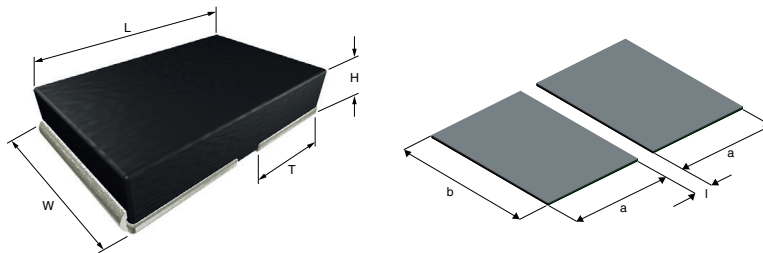
Notes

- 3D models available: www.vishay.com/doc?30349
- Surface mount solder profile recommendations: www.vishay.com/doc?31052

MODEL	RESISTANCE RANGE Ω	DIMENSIONS				SOLDER PAD DIMENSIONS		
		L	W	H	T	a	b	l
WSHP2818	0.001 to 0.1	0.280 ± 0.010 (7.1 ± 0.25)	0.180 ± 0.010 (4.6 ± 0.25)	0.059 ± 0.010 (1.50 ± 0.25)	0.125 ± 0.010 (3.18 ± 0.25)	0.138 (3.5)	0.200 (5.1)	0.024 (0.61)

TYPICAL SENSING LAYOUT

a	b	c	l
0.138 (3.51)	0.210 (5.33)	0.020 (0.51)	0.024 (0.61)

SENSING WITH VIA LAYOUT (best performance)
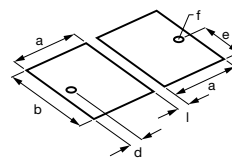
a	b	d	e	f	l
0.143 (3.63)	0.210 (5.33)	0.026 (0.66)	0.105 (2.67)	Ø 0.020 (0.50)	0.024 (0.61)

Note

- Sensing locations are based on the construction of the part; terminals are wrapped from the outside to underneath. These options place the sensing location nearest the temperature stable resistance element, which minimizes contact resistance and optimizes TCR
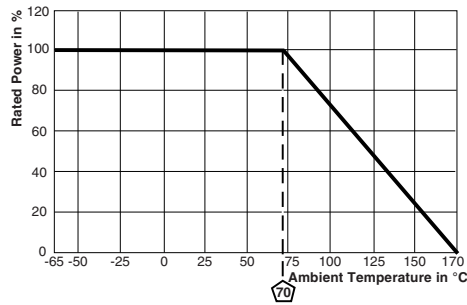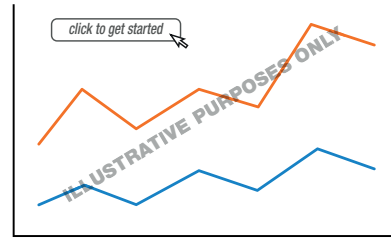
VISHAY.

www.vishay.com

WSHP2818

Vishay Dale

DERATING

PULSE CAPABILITY

www.vishay.com/resistors/power-metal-strip-calculator

PERFORMANCE

TEST	CONDITIONS OF TEST	TEST LIMITS
Thermal shock	-55 °C to +150 °C, 1000 cycles, 15 min at each extreme	± 0.5 %
Short time overload	4x rated power for 5 s	± 1.0 %
Low temperature operation	-65 °C for 24 h	± 0.5 %
High temperature exposure	1000 h at +170 °C	± 1.0 %
Bias humidity	+85 °C, 85 % RH, 10 % bias, 1000 h	± 0.5 %
Mechanical shock	100 g's for 6 ms, 5 pulses	± 0.5 %
Vibration	Frequency varied 10 Hz to 2000 Hz in 1 min, 3 directions, 12 h	± 0.5 %
Load life	1000 h at 70 °C, 1.5 h "ON", 0.5 h "OFF"	± 1.0 %
Resistance to solder heat	+260 °C solder, 10 s to 12 s dwell, 25 mm/s emergence	± 0.5 %
Moisture resistance	MIL-STD-202, method 106, 0 % power, 7b not required	± 0.5 %

PACKAGING

MODEL	REEL			
	TAPE WIDTH	DIAMETER	PIECES/REEL	CODE
WSHP2818	16 mm/embossed plastic	330 mm / 13"	3500	EA

Notes
- Embossed carrier tape per EIA-481
- Additional packaging details at www.vishay.com/doc?20051

ADDITIONAL RESOURCES

Video: Power Metal Strip Short Time Overload	www.vishay.com/videos/resistors/power-metal-strip174-resistor-short-time-overload-product-demo

C.4 Ferrites and accessories

⬦TDK

Ferrites and accessories

ETD 49/25/16
Core and accessories

Series/Type:	**B66367, B66368**
Date:	May 2017

⊛TDK

ETD 49/25/16

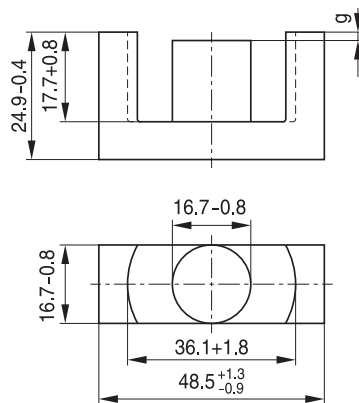**Core**   **B66367**

■ To IEC 62317-6
■ For SMPS transformers with optimum
   weight/performance ratio at small volume
■ Delivery mode: single units

Magnetic characteristics (per set)

$\Sigma l/A$ = 0.54 mm^{-1}
l_e = 114 mm
A_e = 211 mm^2
A_{min} = 209 mm^2
V_e = 24100 mm^3

Approx. weight 124 g/set

FEK0061-Y

Ungapped

Material	A_L value nH	μ_e	B_S* mT	P_V W/set	Ordering code
N27	3700 +30/−20%	1590	320	< 4.59 (200 mT, 25 kHz, 100 °C)	B66367G0000X127
N87	3800 +30/−20%	1630	320	< 12.40 (200 mT, 100 kHz, 100 °C)	B66367G0000X187
N97	3900 +30/−20%	1680	320	< 10.60 (200 mT, 100 kHz, 100 °C)	B66367G0000X197

* H = 250 A/m; f = 10 kHz; T = 100 °C

Gapped (A_L values/air gaps examples)

Material	g mm	A_L value approx. nH	μ_e	Ordering code ** = 27 (N27) = 87 (N87)
N27, N87	0.20 ±0.02	1035	444	B66367G0200X1**
	0.50 ±0.05	525	225	B66367G0500X1**
	1.00 ±0.05	314	135	B66367G1000X1**
	1.50 ±0.05	230	100	B66367G1500X1**
	2.00 ±0.05	188	81	B66367G2000X1**

The A_L value in the table applies to a core set comprising one ungapped core (dimension g = 0 mm) and one gapped core (dimension g > 0 mm).

Other A_L values/air gaps and materials available on request — see Processing remarks on page 5.

Please read *Cautions and warnings* and
Important notes at the end of this document.   **2**   5/17

⏇TDK

ETD 49/25/16	
Core	**B66367**

Calculation factors (for formulas, see *"E cores: general information"*)

Material	Relationship between air gap – A_L value		Calculation of saturation current			
	K1 (25 °C)	K2 (25 °C)	K3 (25 °C)	K4 (25 °C)	K3 (100 °C)	K4 (100 °C)
N27	314	−0.741	504	−0.847	470	−0.865
N87	314	−0.741	485	−0.796	460	−0.873

Validity range: K1, K2: 0.10 mm < s < 3.50 mm
K3, K4: 120 nH < A_L < 1160 nH

C.5   Inductor 1

Recommended Hole Pattern: [mm]

30,0 max.   14,0 max.

1,0 min.

12,0 ±1,0

Φ 0,5 ±0,05   12,5 typ.

Recommended Hole Pattern: [mm]

2x Φ 0,7

12,5

Scale - 1:1

Schematic:

Scale - 1:1

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	10 kHz/ 5 mA	600	µH	±20%
Rated Current	I_R	ΔT = 40 K	2.2	A	max.
Saturation Current	I_{SAT}	IΔL/LI < 10 %	1.1	A	typ.
DC Resistance	R_{DC}	@ 20 °C	0.33	Ω	max.

Certification:

RoHS Approval	Compliant [2011/65/EU&2015/863]
REACh Approval	Conform or declared [(EC)1907/2006]
Halogen Free	Conform [JEDEC JS709B]
Halogen Free	Conform [IEC 61249-2-21]

General Properties:

Ambient Temperature (referring to I_R)	-40 up to +65 °C
Operating Temperature	-40 up to +105 °C
Storage Conditions (in original packaging)	< 40 °C ; < 75 % RH
Moisture Sensitivity Level (MSL)	1
Test conditions of Electrical Properties: +20 °C, 33 % RH if not specified differently	

CHECKED	REVISION	DATE (YYYY-MM-DD)	GENERAL TOLERANCE	PROJECTION METHOD
JKe	006.000	2020-12-14	DIN ISO 2768-1m	

DESCRIPTION
WE-SI Leaded Toroidal Storage Choke

ORDER CODE
744118

	BUSINESS UNIT	STATUS	PAGE
	eiSos	Valid	1/5

C.6   Inductor 2

Low Core Loss, High Current Toroid Inductors

Special Features
• Low core loss
• Low magnetic radiation
• High current capacity
• Horizontal or vertical mount available
• Operating temperature: -55 to +125 °C

Typical Applications
• Switch mode power supplies
• DC/DC converters
• Output chokes
• EMI filters

Notes
* Rated Idc causes a 30 °C temperature rise
** Insert -H or -V for mounting style before -RC
Example: 2300LL-390-V-RC

*† RoHS Directive 2002/95/EC Jan 27 2003
including Annex.*

2300LL Series						
Part Number**	L (µH) ± 20 % @ 1 KHz	Idc* (A)	L (µH) ±20 % @ I rated	DCR (Ω) Max.	Dim. A Nom.	Dim. B Nom.	Dim. C Nom.
2300LL-1R5-RC	1.5	34.0	1.1	0.001	0.59	1.21	0.066
2300LL-2R7-RC	2.7	29.4	1.9	0.002	0.59	1.21	0.066
2300LL-3R9-RC	3.9	26.3	2.6	0.002	0.59	1.21	0.066
2300LL-5R6-RC	5.6	24.0	3.5	0.003	0.59	1.21	0.066
2300LL-8R2-RC	8.2	22.3	4.9	0.003	0.59	1.21	0.066
± 15 %		± 15 %					
2300LL-100-RC	10	20.8	5.8	0.004	0.59	1.21	0.066
2300LL-120-RC	12	19.6	6.7	0.004	0.59	1.21	0.066
2300LL-150-RC	15	18.6	8.0	0.005	0.59	1.21	0.066
2300LL-180-RC	18	18.5	9.0	0.005	0.59	1.21	0.066
2300LL-220-RC	22	17.7	10.6	0.005	0.59	1.21	0.066
2300LL-270-RC	27	17.0	12.6	0.006	0.59	1.21	0.066
2300LL-330-RC	33	13.0	17.9	0.010	0.56	1.18	0.053
2300LL-390-RC	39	12.2	20.1	0.011	0.56	1.18	0.053
2300LL-470-RC	47	11.8	23.7	0.012	0.56	1.18	0.053
2300LL-560-RC	56	8.9	31.9	0.020	0.54	1.16	0.042
2300LL-680-RC	68	8.5	37.4	0.023	0.54	1.16	0.042
2300LL-820-RC	82	8.1	43.7	0.025	0.54	1.16	0.042
2300LL-101-RC	100	7.8	51.7	0.027	0.54	1.16	0.042
2300LL-121-RC	120	7.4	59.3	0.030	0.54	1.16	0.042
2300LL-151-RC	150	7.0	71.1	0.033	0.54	1.16	0.042
2300LL-181-RC	180	6.7	82.1	0.037	0.54	1.16	0.042
2300LL-221-RC	220	5.1	116.6	0.063	0.52	1.14	0.034
2300LL-271-RC	270	4.8	137.7	0.070	0.52	1.14	0.034
2300LL-331-RC	330	4.6	160.8	0.079	0.52	1.14	0.034
2300LL-391-RC	390	4.4	183.6	0.085	0.52	1.14	0.034
2300LL-471-RC	470	4.2	212.5	0.094	0.52	1.14	0.034
2300LL-561-RC	560	4.0	243.6	0.103	0.52	1.14	0.034
2300LL-681-RC	680	3.8	283.0	0.113	0.52	1.14	0.034
2300LL-821-RC	820	3.6	327.4	0.123	0.52	1.14	0.034
2300LL-102-RC	1000	3.5	378.9	0.137	0.52	1.14	0.034

"-RC" suffix indicates RoHS compliance.

Vertical

Horizontal

Dimensions: Inches

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

BOURNS®

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www.bourns.com

Appendix D

Source code

Source code is uploaded to a GitHub repository which can be accessed by clicking the GutHub logo:

Appendix E

Laboratory test Equipment

(a) fluke Ti27 - Thermal camera

(b) Terco MV 1100 - DC load

(c) EA-PSI 9500-06 T - Power supply

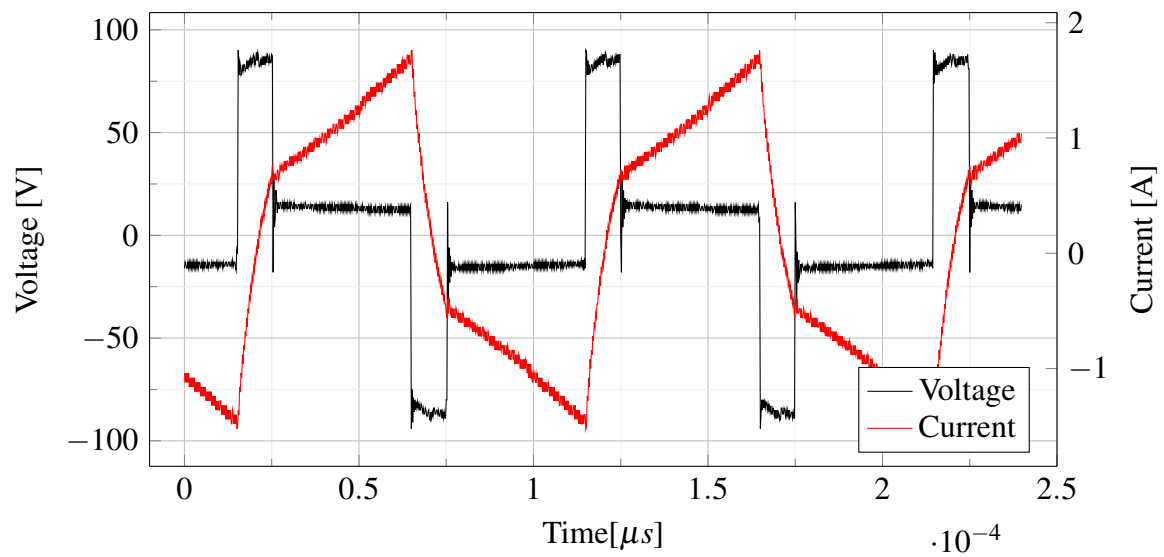Figure E.1: Lab equipment

Appendix F

Supplementary results

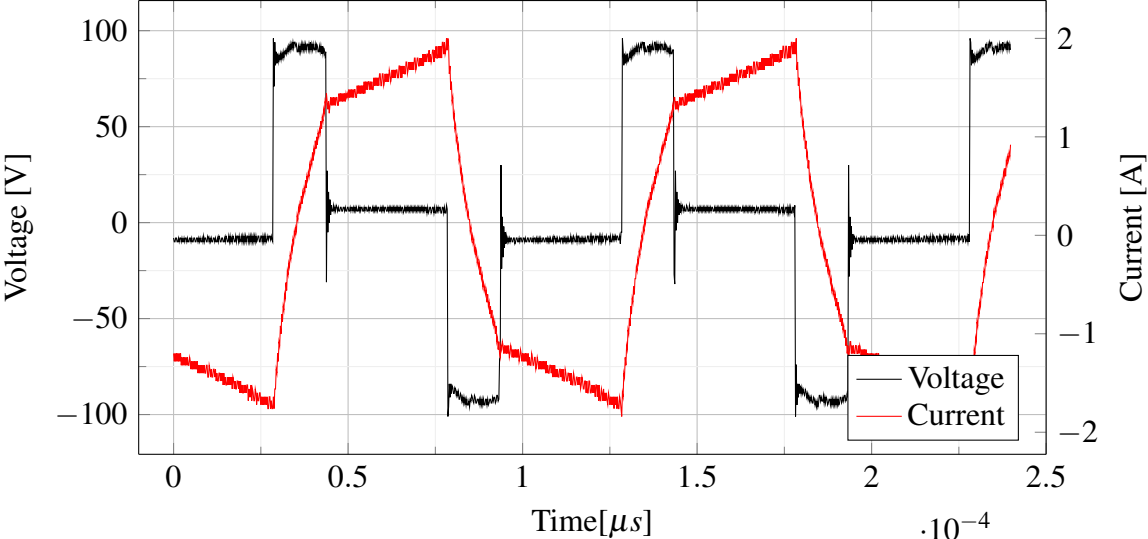*Figure F.1: Matlab/simulink waveforms of inductor characteristics with a phase-shift value of 0.5*

Figure F.2: Matlab/simulink waveforms of inductor characteristics with a phase-shift value of 0.5
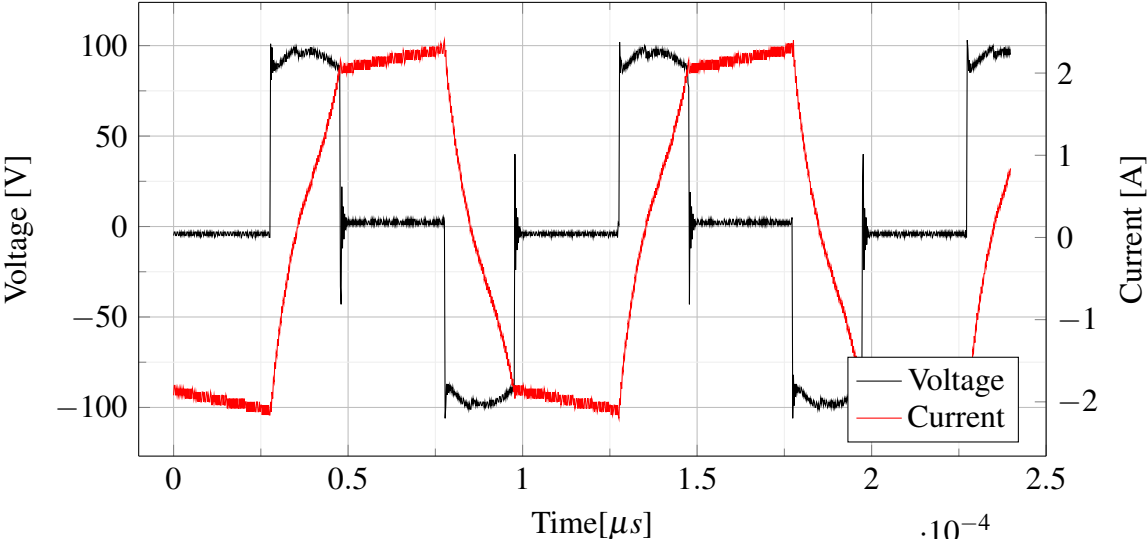

Figure F.3: Matlab/simulink waveforms of inductor characteristics with a phase-shift value of 0.5