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Long, stitch-free slot waveguide with s-bend tapered couplers for IR-sensing applications using electron beam lithography

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We use the fixed beam moving stage (FBMS) electron beam lithography technique to pattern a 10 mm long slot waveguide with s-bend tapered double tip couplers. The fabrication method solves two major limitations of the FBMS mode, namely the requirement for fixed-width structures and the incidence of stage placement drift for patterns involving elements of different widths. This has been achieved by fracturing the outline of the structure into fixed-width elements of gradually increasing width and creating intermediate overlap areas between the elements to mitigate the stage placement drifts.

I. INTRODUCTION

Long, low-loss waveguides are critical for a wide spectrum of photonic applications including telecom and sensing[1–3]. Losses in waveguides can occur due to material absorption, mode leakage/radiation, and scattering. Material absorption is typically well-managed in the state-of-the-art photonic integrated circuits operating in the NIR and VIS, although it is still one of the principal loss mechanisms in the MIR spectral region. Mode leakage and radiation are geometry dependent and can be in most cases well mitigated by proper waveguide design. Scattering, on the other hand, is present across all spectral ranges, and, while dedicated waveguide design can help to mitigate it, the presence of scattering is mainly down to the technological limits of current nanofabrication technology. Scattering occurs at waveguide sidewall roughness or at waveguide defects and imperfections. The former is mainly caused by roughness in a lithographically written pattern that is exacerbated by pattern transfer through etching. Waveguide defects and imperfections arise due to inhomogeneities and impurities present in the photoresist, the device material, or on the wafer surface prior to patterning. Defects are also caused by re-deposition of etched matter, or simply by dust particles on the waveguide that deposit over time.

Stitching errors are another common source of imperfections typical in large-area high-resolution nanostructures patterned using mask-less methods such as electron beam lithography (EBL)[4,5]. The addressable area for the e-beam is limited by the maximum beam deflection defining the writing field (WF) size. Patterns extending beyond the dimensions of the write field must be "stitched" together by mechanical repositioning of the sample. Seamless stitching requires extreme positioning accuracy of the stage and beam placement and positioning errors as small as 5 nm or less lead to undesired pattern offsets resulting in light scattering. The current state-of-the-art EBL using stitching of WF achieves $\pm$15 nm stitching error[6] which could significantly degrade the performance of nanophotonic waveguides. As an example, a 2 dB/cm loss contribution from stitching was reported for suspended MIR slot waveguides[7], and this figure is expected to further increase at NIR and visible wavelengths.

Both sidewall roughness and stitching errors lead not only to excessive power loss due to light scattered out of the waveguide but also to spurious reflections, which have random powers and arise at random positions along the waveguide length. Interference of the direct signal with the reflected components leads to sharp and often dramatic variations in spectral transmission that are known as spectral fringes or interferometric noise. Due to the quasi-random nature of the reflections, the fringes are difficult to describe analytically, reduce, or compensate, and are subject to changes in temperature or composition of the surrounding environment. The fringes negatively affect the performance of all nanophotonic devices, however, they become most critical in the sensing devices, where they interfere with analyte absorption or cavity resonance spectra[8]. Stitching is also particularly detrimental in photonic crystal waveguides, where the line of stitching constitutes a perturbation of periodicity that is fundamental for the device operation[9].

The stitching error generally refers to the limitation in placement accuracy of two neighbouring WF's by the instrument itself. As the pattern extends several WF's any system drift and instabilities can result in a gradual but further increase of the stitching error. There are several strategies to keep this error as low as possible and even to push the stitching beyond the instrument specifications. The standard approach to maintain stitching error is to include and use reference alignments marks in the pattern for in-situ write field and beam tracking alignment. However, methods for reducing the stitching error further has also been demonstrated using pattern overlap or field shift, strategies which also are effective in reducing the line edge roughness[10]. Furthermore, using a fidusial grid for spatial-phase-locked EBL long ranged stitching down to a few nanometers has also been demonstrated[11]. As an alternative to conventional stitch-field (SF) writing, a fixed-beam moving stage (FBMS) method has been implemented in selected EBL systems to address the challenges of WF stitching accuracy. FBMS is a method that allows for stitch-free and in theory infinitely long paths or area elements to be patterned. The basic principle is to use a stationary or spiraling e-beam while moving the stage in a continuous manner under it, producing a path or an area element, respectively. Stage movement is carried out using a closed loop piezo stage

with position accuracy ensured by a laser interferometer. For a given beam current and width of the element to be patterned, the stage speed is set to obtain the correct exposure dose. As the stage speed has an upper-speed limit, for a given resist sensitivity and beam current, there is a limit to the minimum possible feature width which can be calculated as:

$$\text{Structure width} = \frac{\text{Beam current}}{\text{Area Dose} \cdot \text{Stage speed}} \quad (1)$$

For CSAR62 with a clearance dose 72 μC/cm^2 at 30 kV[12], with a beam current of 29 pA (typical for a 10 μm aperture), and using the fastest stage speed of 1 mm/sec, a FBMS structure with a width as small as 40 nm can be patterned.

Although FBMS appears as an ideal solution for waveguide applications offering long and stitch-free area elements, it has been used to a somewhat limited extent. The main reason is that FBMS has been historically limited to fixed width area elements patterned along a single path and is consequently not very suitable for varying width structures (tapers etc.), non-continuous structures (dots, etc.) and in general complex shapes made from several elements. Applying FBMS to fabricate taper structures has been of interest by several research groups and solved with various methods. Khodadad et. al.[13], investigated three methods for writing long tapered waveguide structures, using a sleeving method, longitudinal FBMS-path fractioning method and finally a custom beam deflection combined with FBMS. Mere et. al. realized tapering waveguides using FBMS by joining two FBMS paths towards a common point (taper end), obtaining a smooth and stitching-free taper[14]. Recently the patterning of tapers using FBMS has also been solved by the manufacturer as well, where a so called dynamic beam expansion has been made available[15].

Another challenge in using FBMS is the placement of neighboring structures. Inaccurate relative placement can become problematic in e.g. directional couplers or the slot waveguides presented in this paper. While the FBMS mode in principle ensures two stitch-free waveguides, their relative waveguide placement, which is imperative for the performance of the devices, could be offset if there is any system drift present. As the patterning time is inversely proportional to the area to be exposed, the impact of drift and instability due to e.g. temperature variations or mechanical drift will become more apparent. A solution to this is to use alignment marks with the FBMS as proposed by Sanabia et. al.[16]. However; alignment marks are good for the starting point of the pattern only and, if the pattern is long enough, drift problems may manifest towards the far end of the structure.

In this paper, we propose a new way of realizing long (10 mm) and complex waveguide structures using FBMS. We demonstrate the patterning of a slot waveguide with a narrow, and continuous gap of 170 nm, including a structure layout with tapered s-bend input/output couplers. We combine FBMS and SF mode and use an inverse patterning strategy for the realization of our waveguides, which allow for a direct pattern transfer to the substrate using the CSAR62 EBL resist as our dry-etch, etch mask. For the patterning, we solve inherent stitching problems, stochastic drift-related stitching and system drift-related stitching in a simple way by fracturing and overlapping the design in a judicious way. Our strategies can be applied to many other devices requiring stitch-free patterning using conventional FBMS.

II. WAVEGUIDE DESIGN AND FABRICATION

A slot waveguide proposed by Almeida et al.[17] is a popular waveguide design for e.g. sensing and nonlinear applications as it provides large optical field confinement in the surrounding environment and thus high sensitivity to any environmental changes. It consists of two high refractive sections separated by a narrow gap (slot). If properly designed, a large part of the TE-polarized fundamental guided mode is concentrated in the slot, reaching air confinement factors of 70% or beyond[18]. While the strong air confinement provides for strong light-analyte interaction in sensing or nonlinear experiments, it also increases the sensitivity to any slot side-wall imperfections including stitching errors, making the waveguide prone to excessive scattering and interferometric noise. Therefore, slot waveguide performance is highly reliant on stitch-free writing, which makes it a perfect case for our study.

The slot waveguide reported here is designed for applications in the MIR spectral region and uses a silicon on insulator (SOI) platform with a 500 nm device layer and 3 μm buried oxide (BOX) layer. The waveguide dimensions including 550 nm wide waveguide sections and 150-180 nm slot region (see Fig. 1) were chosen to achieve an evanescent field confinement factor of 70 % at 3.2 μm. In order to facilitate light in/out-coupling and minimize facet reflections, a double tip coupler[19] has been included in the design as also shown in Fig. 1. Both the slot waveguide and the coupler interfaces have been designed and optimized using Ansys Lumerical Mode and FDTD.

The waveguide fabrication follows a standard process with EBL patterning and inductively coupled plasma reactive ion etching (ICP RIE) outlined in Fig. 2. For the patterning, Elionix ELS-G100 and Raith e_line electron beam lithography systems have been used, combined with a 330 nm thick positive e-beam resist (CSAR62). The Elionix EBL was operated in the stitch-field mode at 100 kV acceleration voltage and 1 nA beam current with 500 μm write field size. The Raith system was used in FBMS mode with its maximum acceleration voltage of 30 kV and 7.5 - 10 μ apertures yielding beam currents of 15 pA to 29 pA, respectively. The patterning is carried out by exposing the area surrounding the waveguide, and, after resist development, the pattern is transferred into the device layer using inductively coupled plasma reactive ion etching (ICP RIE) with SF_6 and CHF_3 chemistry. A gas mixture of 50 sccm of CHF_3 and 7.5 sccm of SF_6 at 10 mTorr gas pressure was used, with an RF power of 40 W and ICP power of 600 W. This process resulted in a well-defined slot waveguide with fully etched slot, vertical side-walls, and minimal surface roughness as demonstrated in Fig. 3a and Fig. 5. However, as also shown in Fig. 3a, patterning with the conventional stitch-field method using Elionix EBL system results in stitching errors as large as ∼30 nm. Imaging of the chip

surface using MIR camera (Telops, FAST M350) showed that such stitching produces clearly visible out-of-plane scattering and, hence, presumably also back reflections contributing to the interferometric noise.

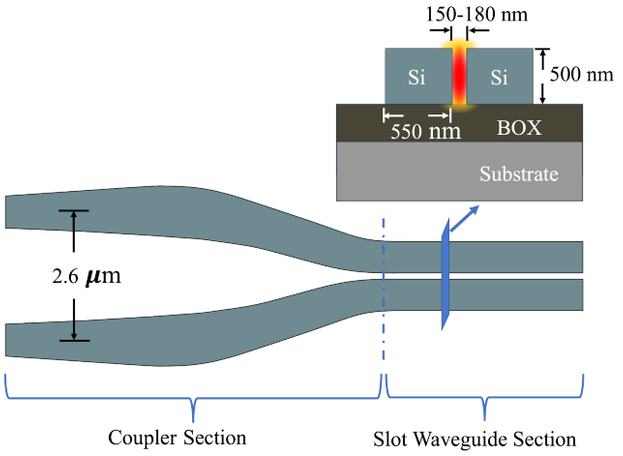

FIG. 1: Schematic illustration of the slot waveguide terminated with a double tip coupler. The inset shows a cross-sectional view of the slot waveguide with dimensions optimized for gas sensing application in the mid-infrared.

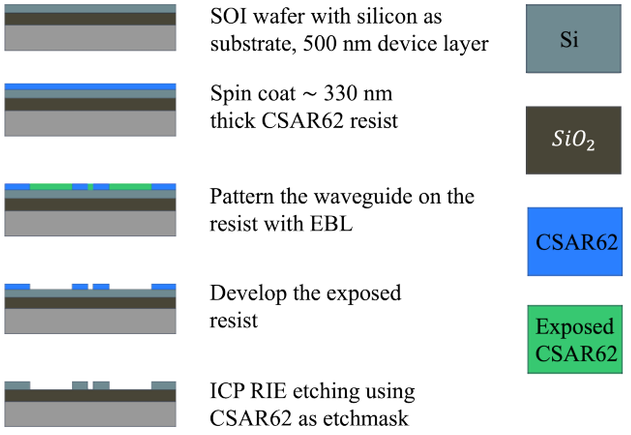

FIG. 2: Process steps for waveguide fabrication

III. FIXED BEAM MOVING STAGE (FBMS) PATTERNING

Figure 1 shows the schematic of the input (output) section of the structure consisting of a coupler that adiabatically tapers into the slot waveguide. Each coupler section is 50 μm long while the slot waveguide has the overall length of 1 cm. As can be seen from the design, direct patterning of the wires with FBMS using a negative EBL resist is not feasible because of the tapered couplers. A possible approach is to use a positive EBL resist, and pattern the outline of the waveguide wires, as

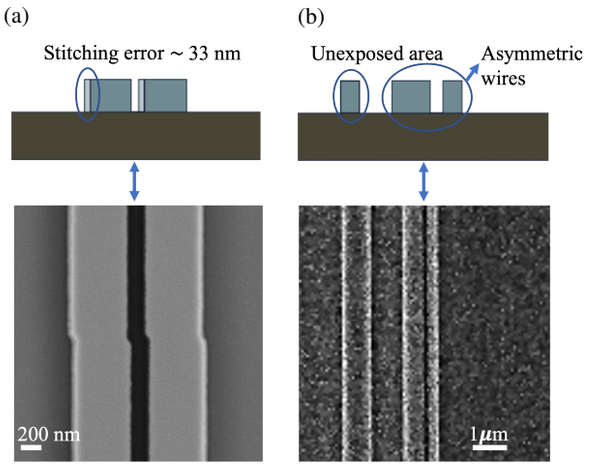

FIG. 3: (a) Top-view SEM image of a stitching error observed on a waveguide patterned in stitched write field mode with an EBL system with laser interferometric stage. (b) Top-view SEM image of a developed resist following initial FBMS patterning, showing on the left an unexposed area between two elements and undesired waveguide width variations due to element placement drift. In both a) and b), a schematic illustration of the respective slot waveguide cross section is included.

is illustrated in Fig. 4a. We started with 150 nm wide FBMS elements (Path-A and Path-B) that pass through the slot and along the inner edges of the coupler arms (see Fig. 4b). The outer areas of the couplers and waveguides are patterned using separate FBMS elements with a width of 10 μm(Path-C). The different elements are placed in separate layers to control the patterning sequence, and the different width elements are patterned sequentially starting from the 150 nm to 10 μm wide elements, followed by the stitching mode exposure for the remaining area between the coupler arms.

After the exposure, the resist was developed and examined with SEM. It was discovered that there was an asymmetry in the dimensions of the two slot waveguide wires for all fabricated samples. The asymmetry was found to vary in severity from sample to sample and it was attributed to the incorrect placement of the 10 μm wide element (seen in Fig. 3b, as right 10 μm element moved towards the left). It was confirmed that the process through which the stage switches from one element to another is not accurate; Upon completion of the writing process for one element, a certain time has passed. As the stage moves to the next area element to be patterned some drift has occurred and the starting point for this element, relative to the previous, has shifted by the amount of the drift. This was supported by the fact that the severity of the pattern placement error increased with patterning time (element size). The stitching problem was isolated to two main contributions; the obvious system drift due to temperature and mechanical vibration/movement, and an inherent beam placement inaccuracy for the FBMS mode.

In order to avoid the drift, the entire waveguide must be patterned using only a single fixed width element with "one stroke". This is clearly challenging to achieve in the slot waveguide design. The best solution is to design as much as possible of the waveguide outline as a single and connected 150 nm wide element. In Fig 4c, this is illustrated with Path-A, starting at one end and moving around most of the waveguide edge, including the outer edge. To complete the structure, two extra FBMS elements (Path-B) for the inner side of each of the coupler arms must be added. Path-B terminates in a common point with Path-A to overlap perfectly. The small area addressed in this pattern is quickly patterned, and the outline of the waveguide is made with the highest possible speed and accuracy. Then, to reduce the time spent patterning a single element, and consequently, the time for drift to take place, an intermediate element (Path-D), with a width of 1 μm was patterned next. This path in itself is a drift gradient for the patterning. It was designed with an overlap region of 50 nm with Path-A (seen as dark red lines in Fig, 4c) to compensate for any drift that might occur during the time it takes to pattern Path-D. The width of the overlap region was determined by trial and error and is obviously dependent on the specific EBL instrument and location. Finally, Path-C, the last FBMS area, was patterned. This has the overlap of 500 nm with Path-D and ensures that all remaining resist is exposed - independently of any drift occurring.

After the FBMS writing has been completed for the FBMS elements, the system switches to stitching mode exposure for the remaining area between the coupler arms. An overlap region of 50 nm is left, for the area that has been exposed with the stitching mode, with the neighboring FBMS elements to avoid any possible drift.

It was observed that using the FBMS for larger area elements, the CSAR62 tends to leave slightly more residue after development and typically requires a higher dose to clear the resist properly compared to the smaller area elements. Therefore, the wider 10 μm areas (path-C and D in 4c) are exposed with a dose of 78 μC/cm^2 while the smaller areas (path-A and B in 4c), and the stitched area are exposed with 71.5 μC/cm^2.

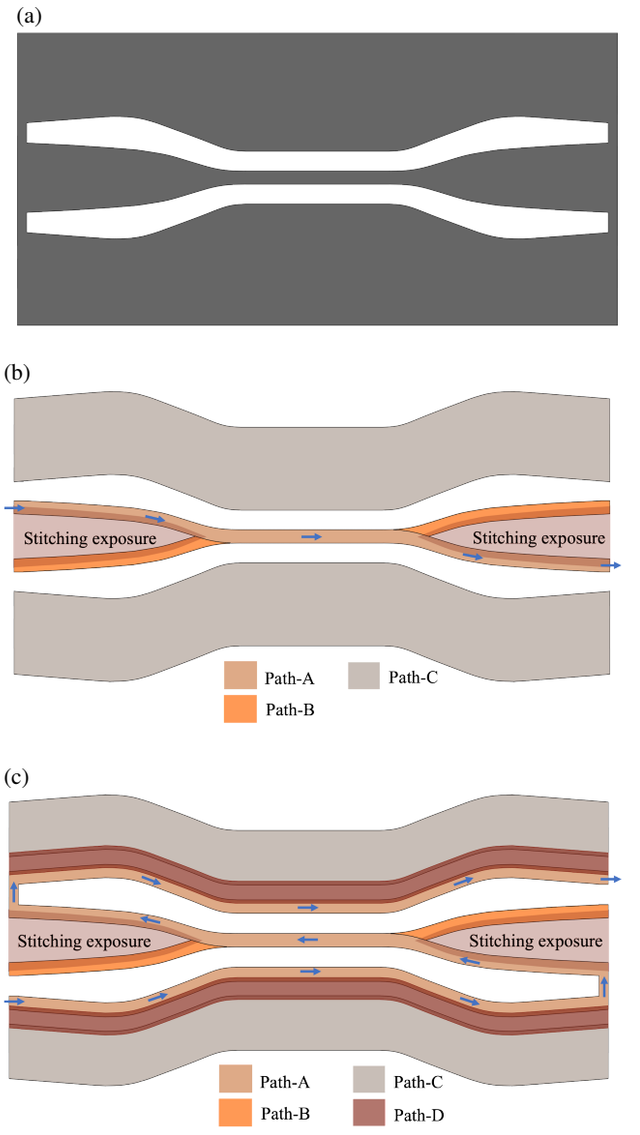

FIG. 4: FBMS patterning of complex structures with outline elements and overlap regions.(a) Schematic of the pattern. With a positive resist, the shaded area is exposed while the unexposed white regions form the waveguide structure. (b) The area in (a) is fractured into an area element represented as path-A and path-B with a width of 150 nm and path-C with a width of 10 μm. The small region between the coupler arms is patterned in stitch-field mode. The arrows indicate the direction of the stage movement along path-A. (C) Path-A in (b) is extended along the outer waveguide edge to define the structure outline with one stroke. Short path-B elements are added in a new layer due to software restrictions on element overlap. Intermediate path-D with a width of 1 μm, is included between path-A and path-C with an overlap region at the boundaries. The arrows indicate the direction of the stage movement along path-A.

IV. RESULTS AND DISCUSSION

Fig. 5 shows SEM images of the fabricated slot waveguide and the coupler, respectively. Fig. 5a is a representative image of a series of images taken along 9 waveguides (input, middle section, output) that were processed on three different chips. The images illustrate a defect-free pattern realized over the full waveguide length. By measuring the slot waveguide dimensions for each of the images, we obtained a statistically reliable value of residual asymmetry of 2.71.3%, which corresponds to approx. 15 nm for our slot waveguide wires of 550 nm width. Such asymmetry does not have a significant effect on the slot waveguide performance, primarily leading to a small decrease of the air confinement factor by as little as 0.5%.

In Fig. 5b we show a typical coupler. First of all, it is worth noting that paths A and B are meeting perfectly at the

center of the slot and no effects such as slot broadening can be seen where they overlap. Further, the image shows that the area where the stitched field meets the FBMS pattern neither exhibits any stitching between the two writing mode because of the sequence of patterning priority used.

Finally, the inset in Fig. 5b demonstrates the cross-section of a fully etched slot waveguide, and the measured dimensions are given. It is noteworthy how sharp the profiles of the waveguides are defined and how vertical the sidewalls are, keeping in mind that a resist thickness of 330 nm was exposed using a 30 kV acceleration voltage EBL. Optimizing the thickness of the resist layer is essential in order to obtain the correct dimension for the slot width and achieve vertical side walls. In most cases, the resist needs to have a thickness at least equal to the device layer thickness, i.e. 500 nm, to minimize the possibility of the resist being removed before the device layer is fully etched. A 500 nm thick resist layer with a 30 kV acceleration voltage, however, would not result in a very good vertical sidewall profile due to the forward scattering of the electrons. As CSAR62 exhibits good plasma etch resistance, the resist thickness was lowered to 330 nm, where an optimal slot width and vertical sidewall was still achievable. It can be seen from Fig. 5b inset that the measured slot width is 171 nm, which is well within the range for optimal device operation.

V. CONCLUSION

We have demonstrated a new method for patterning of long and stitch-free slot waveguide with s-bend tapered couplers using FBMS. In this method, the outline of the structure is initially patterned as one FBMS element at maximal speed, in order to eliminate the element placement inaccuracy and minimize time dependent system drifts. Using the outline of the structure also gives the ability to define tapers and other complex shapes with a high degree of flexibility. In addition, applying overlap regions eliminates drift-related issues when more area elements are involved.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose

DATA AVAILABILITY

The data that supports the findings of this study are available within the article.

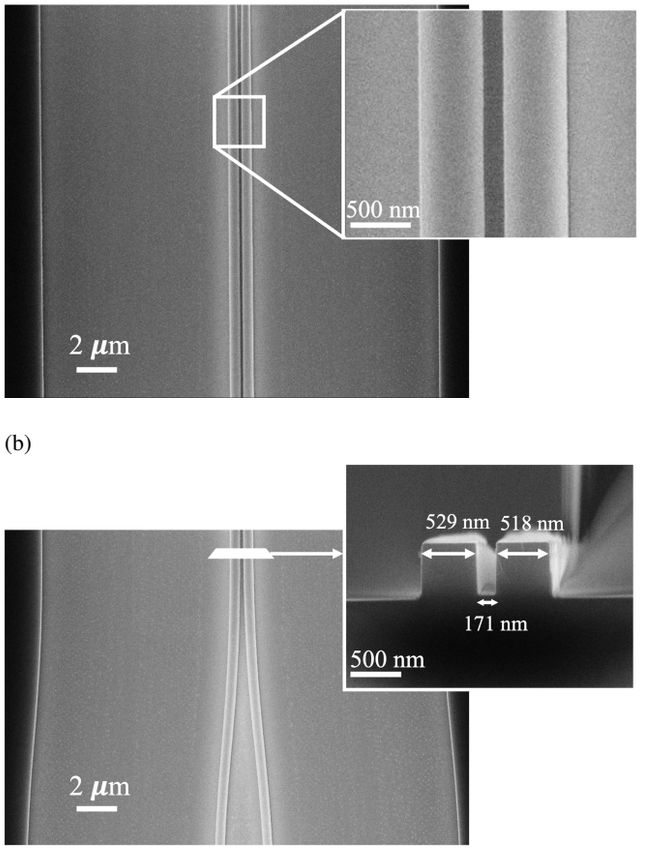

FIG. 5: Top view SEM images of (a) the fabricated slot waveguide and (b) the double-tip input coupler. Inset in (b) shows the cross-sectional view of the slot waveguide

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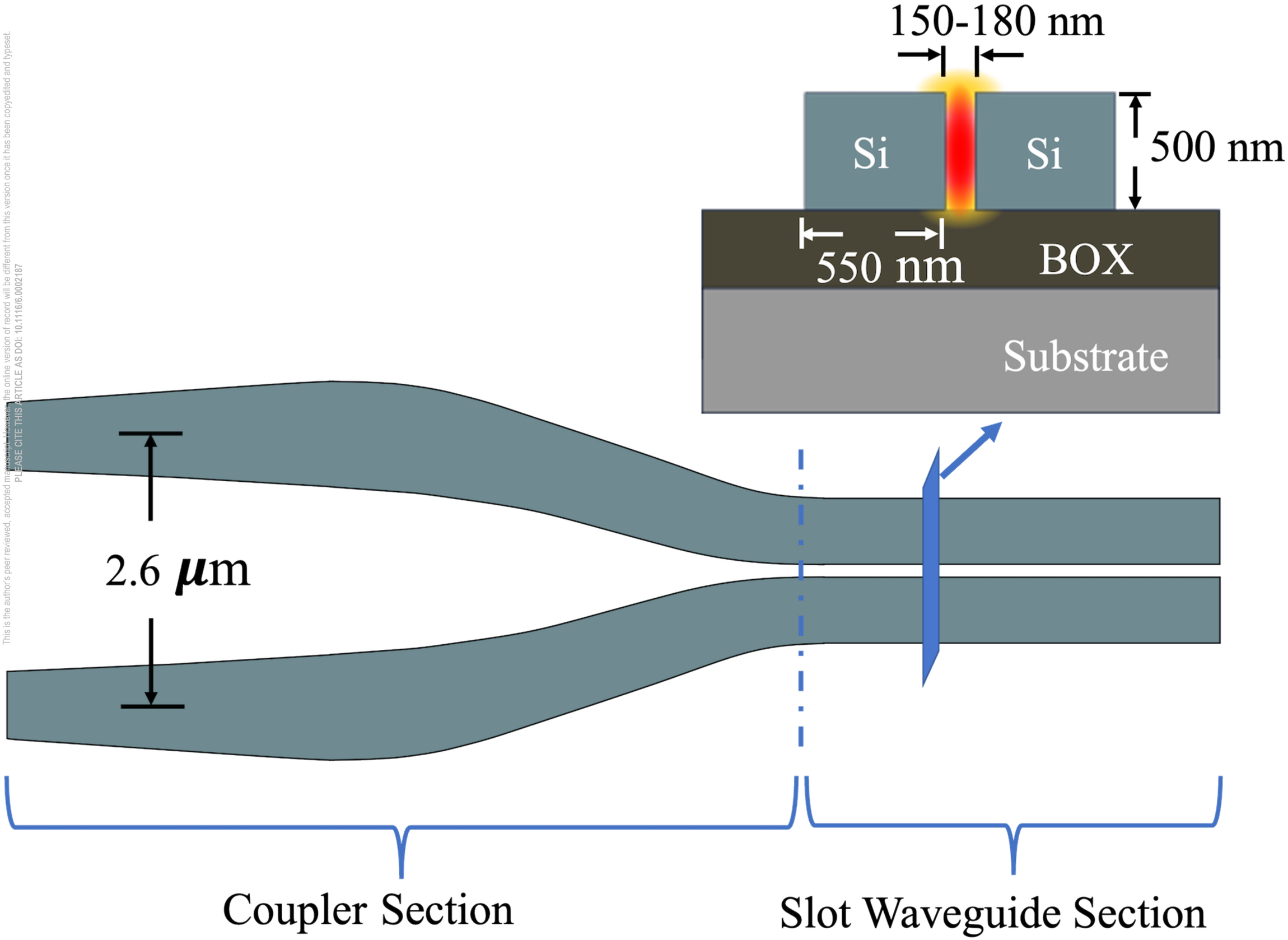
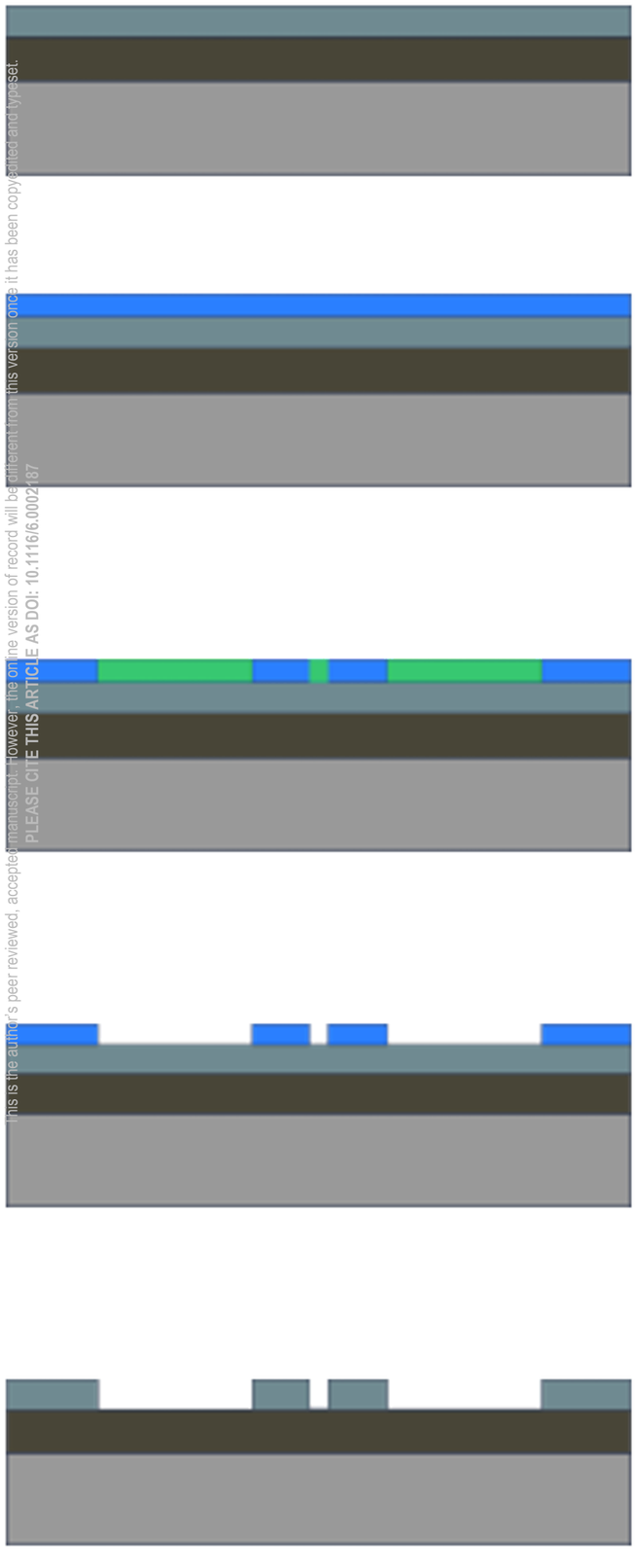




SOI wafer with silicon as substrate, 500 nm device layer

Spin coat ~ 330 nm thick CSAR62 resist

Pattern the waveguide on the resist with EBL

Develop the exposed resist

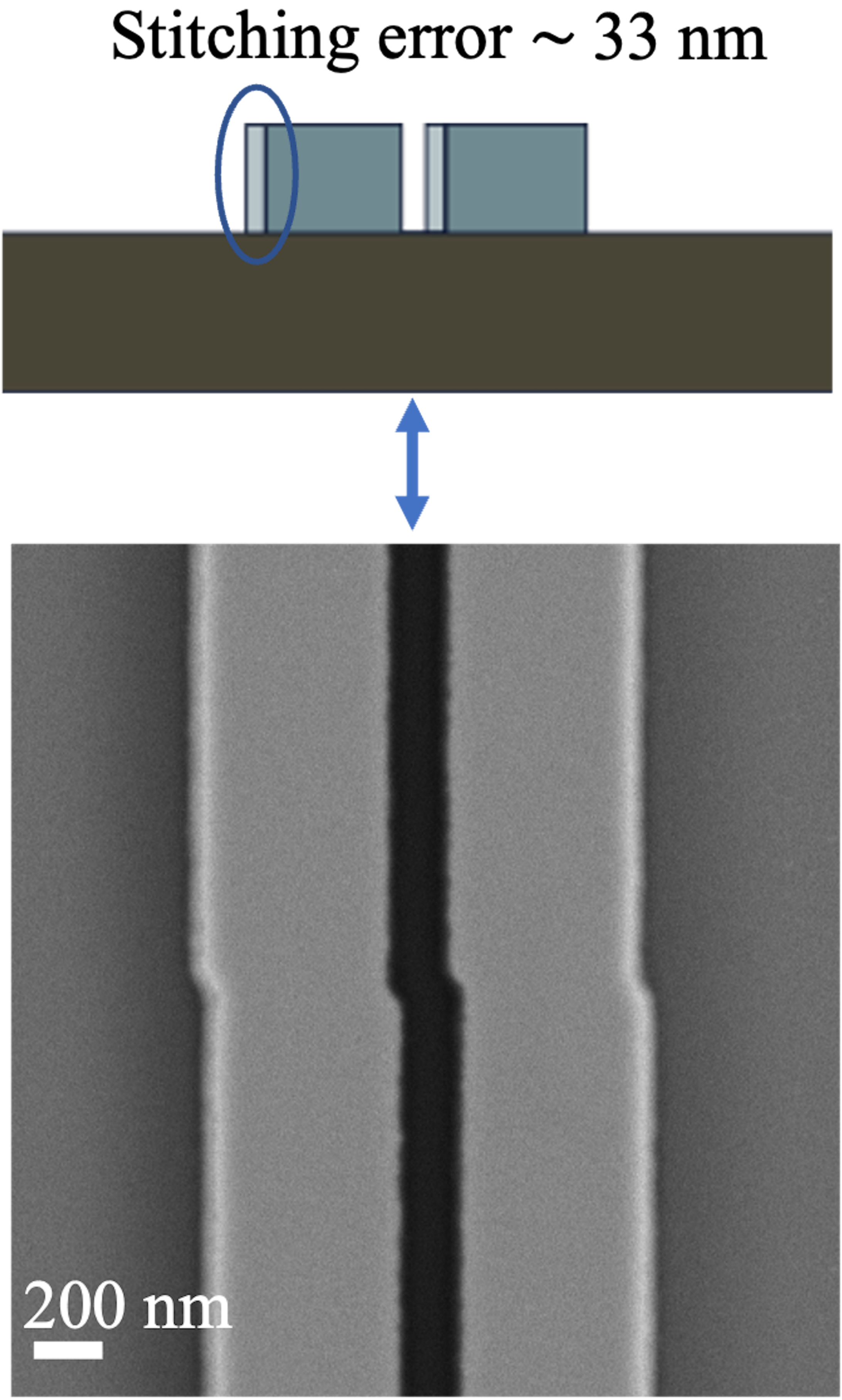
ICP RIE etching using CSAR62 as etchmask

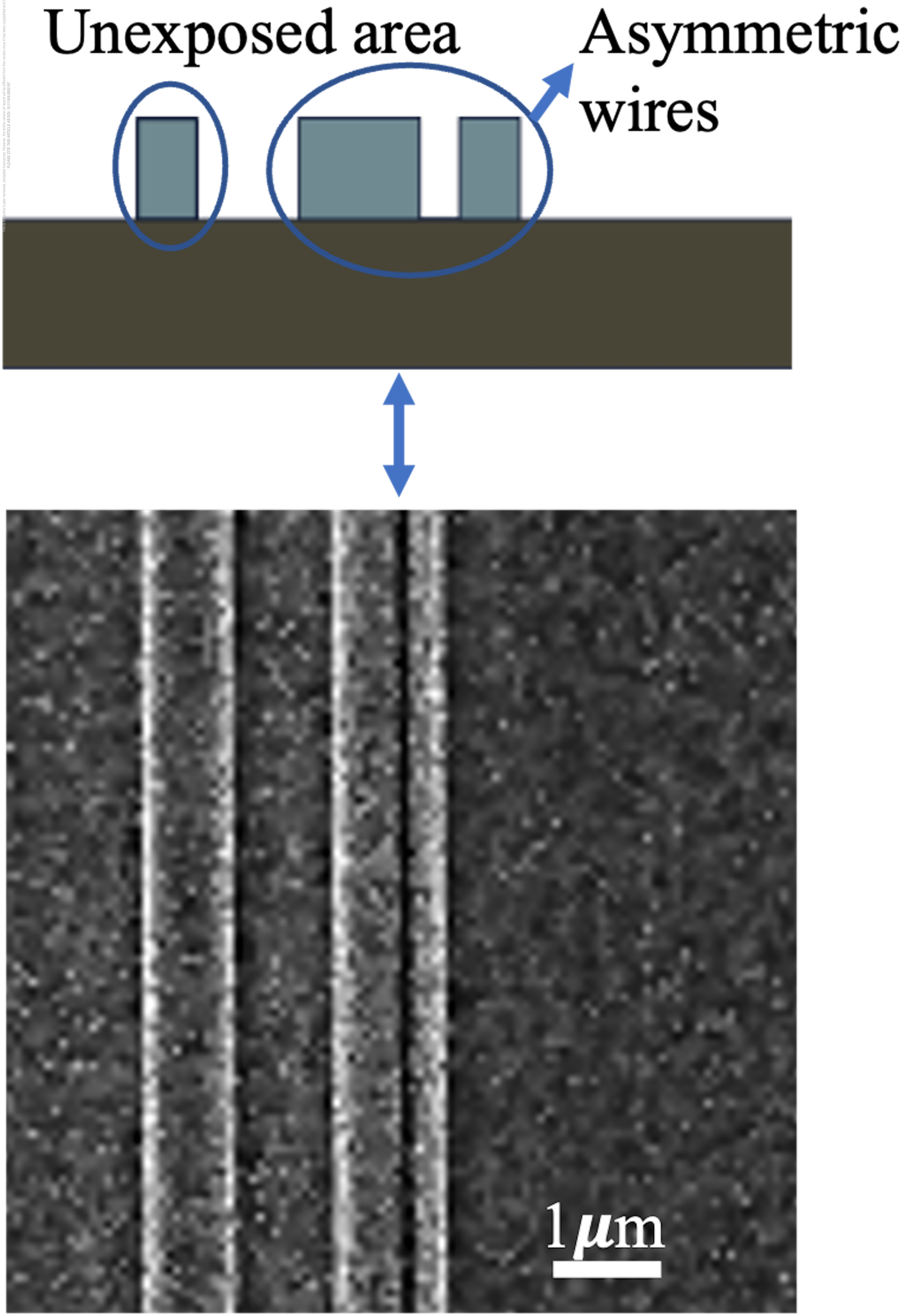
Si

SiO_2

CSAR62

Exposed CSAR62





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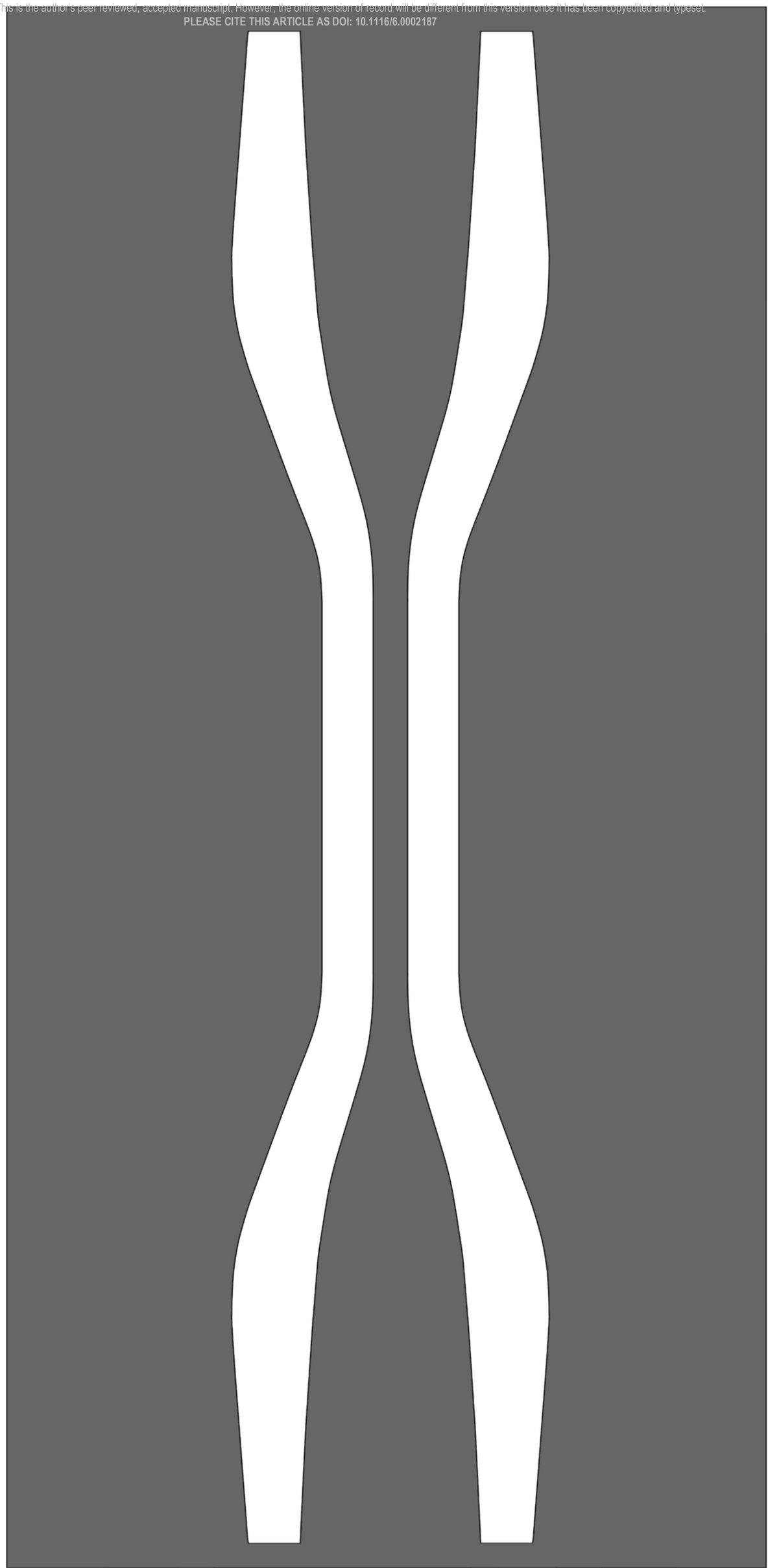

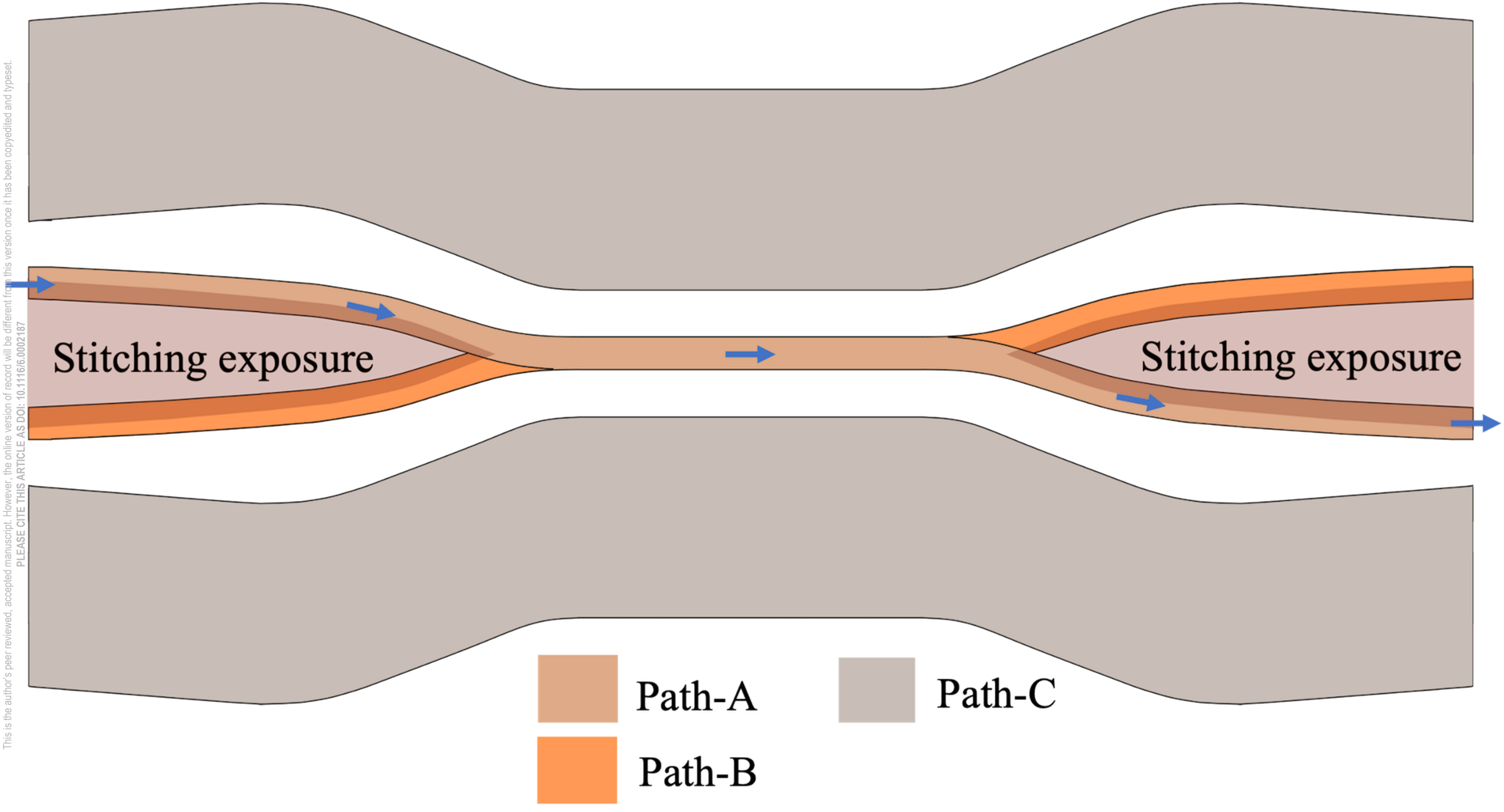

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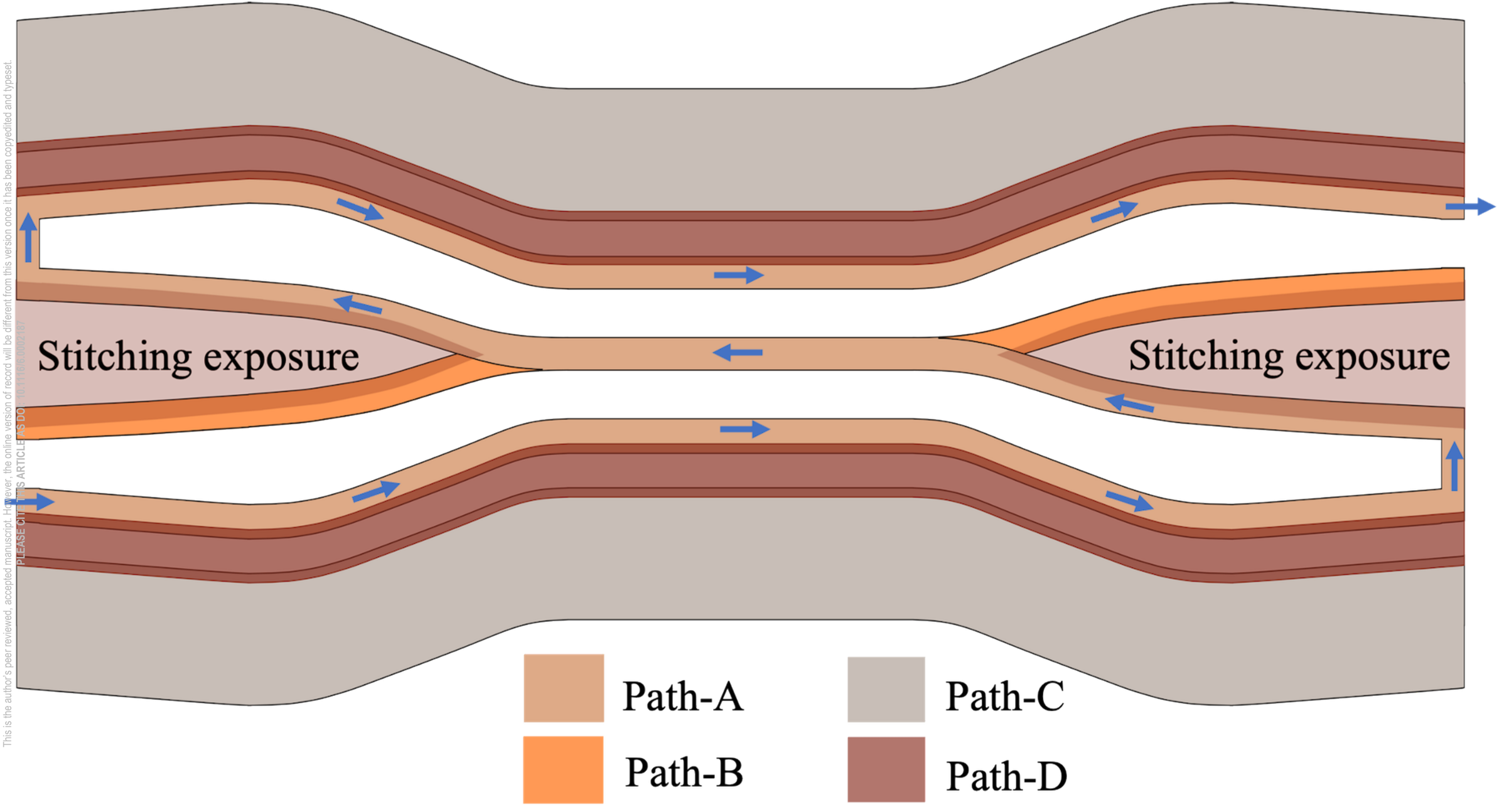

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