Marine Thruster I/O Board Redesign, Prototyping, and Certification

A thesis by

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Abstract

For about 20 years, the company Marine Technologies have used a circuit board called the IOB, which controls input and output signals. The Input Output Board (IOB) uses a logic device to manage the different signals. For the last 20 years this has been an FPGA (Field Programmable Gate Arrays). The manufacture, design, and supply of IOB belonged to another company, but the time came for Marine Technologies to claim the ownership of the IOB and make a design of their own. This was a good opportunity to make design changes and the possibility of using microcontrollers instead of FPGAs became an interesting pursuit. Microcontrollers naturally are cheaper and easier to acquire and have become considerably advanced, making them a possible replacement candidate. This thesis explores the process of implementing a microcontroller with the new IOB design and having the product certified.

The new IOB must fulfill Marine Technologies' set of demands which require it to be functionally identical to the original; it also needs to fulfill the international sets of standards that amongst other things set the demands for environmental robustness and Electromagnetic Compatibility (EMC) performance. To meet this set of demands, I completed an analysis of the current I/O usage of Marine Technologies' systems and reduced the amount of I/O available to match this actual usage. This proved that a microcontroller have enough resources to handle the actual required I/O load of Marine Technologies' systems. In terms of EMC, the best one can do is to design a circuit board that follows design guidelines for EMC as closely as possible and test it when the prototype arrives. The number one rule for EMC minded design, is to allow return currents to flow directly under the outgoing signal trace, which is best achieved by having dedicated, proper, and unbroken power and ground planes, placed in the layers between the top and bottom layer of the PCB.

The design of the new IOB, called MT-IOB-Mk3-Transit, was done by closely examining the design of the previous two FPGA based iterations of the IOB, called the MT-IOB-Mk1 and MT-IOB-Mk2. The IOB-Mk3-Transit uses elements from both boards, by looking at 20 years of field testing and usage, what works best and what does not, while at the same time considering how the new microcontroller fits within these elements. In most aspects the IOB-Mk3-Transit is a mosaic containing elements from both the IOB-Mk1 and the Mk2, which are known to function reliably for 20 years.

During functional testing of the IOB-Mk3-Transit, the crucial functions were working well. The board was tested in a certification lab in Italy, and due to the board being designed with sub optimal EMC practice, we used two attempts in Italy before finally passing the EMC tests, requiring some research at home before travelling for the second attempt. The product was then certified, installed on a vessel and is now in use.

Taking the lessons learned from the IOB-Mk3-Transit, the new iteration purely called the MT-IOB-Mk3 has been designed, following the stated EMC guidelines closely to improve performance, and correcting a few minor issues of the IOB-Mk3-Transit. This board has yet to be tested. In the end, the question of using a microcontroller instead of an FPGA to perform the duties of the IOB, is only partially answered. Yes, the microcontroller can perform all the required functions that the FPGA did, and it will be implemented as a part of the Marine Technologies environment for now, but long-term reliability is a question that can only be answered by long-term use and testing.

Acknowledgements

Words simply cannot express how thankful I am for my advisor Johan Alme from the University of Bergen. I could not have completed my thesis without your willingness for patience, guidance and understanding. I also must state my vast gratitude to the company Marine Technologies LLC for the opportunity to take on this task and providing me with the necessary resources to do so.

I would like to extend my thanks to my colleagues at Marine technologies of receiving my many questions and responding with many answers. In addition to many questions, the number of dry jokes you had to brave from my part is not lost on me, I commend your resilience.

As for my friends, my family, and my wife. Friends, you sent me words of encouragement and provided me with laughter when I needed it. Dearest family, you showed unwavering support and provided a place of peace and restitution. And lastly my wife, you stood by me when I needed help and never gave up faith in me.

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Terminology and Abbreviations

ADC	(Analog to Digital Converter)
AI	(Analog Input)
AO	(Analog Output)
CAN	(Controller Area Network)
DAC	(Digital to Analog Converter)
DI	(Digital Input)
DNV	(Det Norske Veritas)
DO	(Digital Output)
DP	(Dynamic Positioning)
ECDIS	(Electronic Chart Display and Information System)
EMC	(Electromagnetic Compatibility)
EMI	(Electromagnetic Interference)
EUT	(Equipment Under Test)
FAT	(Factory Acceptance Test)
FPGA	(Field Programmable Gate Arrays)
GPS	(Global Positioning System)
IEC	(International Electromechanical Commission)
IMO	(International Maritime Organization)
IOB	(I/O Board)
MCU	(Micro Controller Unit)
MRU	(Motion Reference Unit)
MT	(Marine Technologies)
PCB	(Printed Circuit Board)
PISO	(Parallel In Serial Out)
RAM	(Random Access Memory)
RBW	(Resolution bandwidth)
RMII	(Reduced Media-Independent Interface)
ROM	(Read-Only Memory)
SMD	(Surface Mounted Device)
SPI	(Serial Peripheral Interface)
UART	(Universal Asynchronous Receiver/Transmitter)

1 Introduction

The offshore industry is a vast and advanced field, requiring a multitude of different technologies and areas of expertise to cover everything from transport to fishing, wind farming and oil and gas production. A crucial commonality between offshore industries are the ships in use. Advancements in ship construction, sailing and navigation have heavily influenced human progress throughout history. The motorization of shipping meant steady and consistent sailing that the unpredictable use of wind could not match. Timekeeping pieces like the H1 marine chronometer clock was a large step towards solving the longitude problem, meaning one step closer to an efficient method of mapping and positioning. And now highly advanced communications systems have given us GPS and ECDIS (Electronic Chart Display and Information system), allowing a vessel always to be aware of its position and the terrain below where it is sailing.

Figure 1-1: ASD Tug 5016 Vessel

The thesis is written in collaboration with Marine Technologies LLC (MT)[1]. Marine Technologies specializes in Dynamic Positioning (DP) systems for industrial class marine vessels. DP allows a vessel to use its multiple thrusters along with GPS data to anchor the ship and its orientation to a geographical point, counteracting the currents and winds at sea to keep the vessel still.

The basic working principle of a DP system could be split into two main parts, what the ship can see, and what the ship can do. First let us cover what can the ship see, which is what data is has. The vessel

[1] https://www.marine-technologies.com/

has access to accurate GPS positioning, wind speed and direction data, sea current data and vessel orientation by using MRU's that have gyroscopes and accelerometers. The vessel now knows where is, it knows how it is oriented and the vessel knows what direction it is being pushed and how hard it is being pushed.

How does a vessel use this data? Vessels that use DP usually have multiple thrusters that can generate thrust in any direction. Using these thrusters, the vessel can directly oppose the forces of wind and current while maintaining its orientation and geographical position. However, to do this, computers must be used to calculate the vessels response based on the data it can see. With this data, the computers and the thrusters can maintain ship position with an accuracy within one meter.

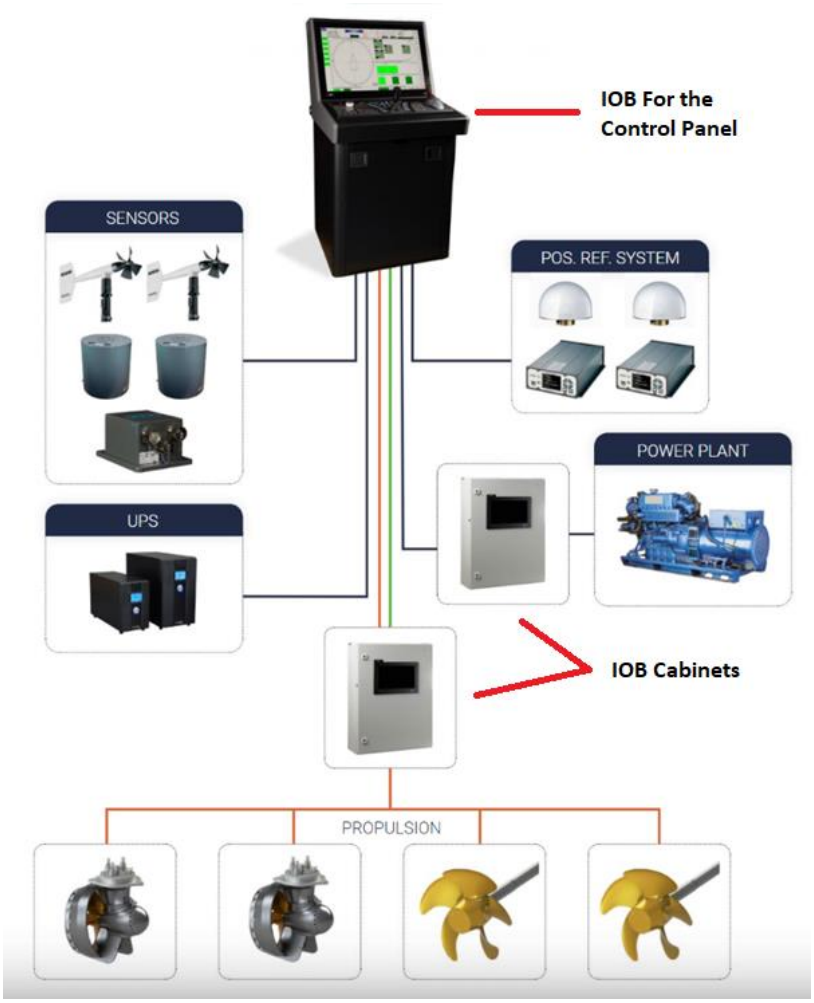

Figure 1-2: MT DP1 System Overview

This process requires use of feedback systems and controllers, which means communication between the antennas, the DP computer, control computers, and the thruster control boards which are shown as IOB cabinets in Figure 1-2. Our focus in this thesis is one of MT's crucial components in this network,

the General purpose I/O Board (henceforth called IOB). The original IOB-Mk1 was designed and made operational in 2003, and IOB-Mk2 in 2014, and is one of the most important PCBs in the system. The IOB is mounted directly on the thruster board and is responsible for receiving and executing the thruster control commands. The Mk1 and Mk2 boards are designed with an FPGA solution creating Fly by Wire control over ethernet from lever to thruster.

At the time of writing, the world market has had to fight a shortage problem that started to take a foothold during and after the COVID-19 outbreak. This shortage has also affected IC's and other circuit board components and silicon-based chips. Together with the rising capability of standard microcontrollers means that it is of interest to implement them in an IOB redesign, moving away from the FPGA based solution that has been used for 20 years.

1.1 I/O Board

The IOB is a general purpose I/O control and monitoring board. It is made to be general purpose so that it can be used for a wide array of devices internally for MT. The IOB is mainly used in thruster control cabinets to connect thruster command and monitoring to the ships network, but the IOB is also used for operating panels that comprise of buttons, joysticks, heading wheels and the like. The system overview in Figure 1-2 includes two examples of where the IOB is put to use.

Although the IOB is equipped with multiple communication functions, its main features are its inputs and outputs, its "I/Os". The IOB has two varieties of I/O, the first is analog I/O and secondly, digital I/O.

Imagine the analog inputs as your ear, as it can not only hear sounds, but also can hear how loud they are; this loudness is represented in the IOB as electrical voltage, which can go as loud as 10 volts. Now think of how your ear can deduce if a sound is in front of you or behind you; this is represented as positive voltage in front of you and as a negative voltage behind you. For us, the sound is often a signal from a ship's rudder, reporting its position, where zero volts is quietly in the middle position. Next, imagine your voice as an analog output that produces sound. This analog output can produce the same negative and positive 10 volts to for example control a rudders position.

For digital I/O, your eye and a light are a good example of a digital input, since you can perceive with your eye when the light is on or off. Just as your eye can tell if a light is on or off, a digital input can tell whether a signal is high or low. This signal is often used to tell us if a button is being pushed. As for digital outputs, this is simply like you turning a switch on or off, and that switch can be used to turn external systems such as pumps on or off.

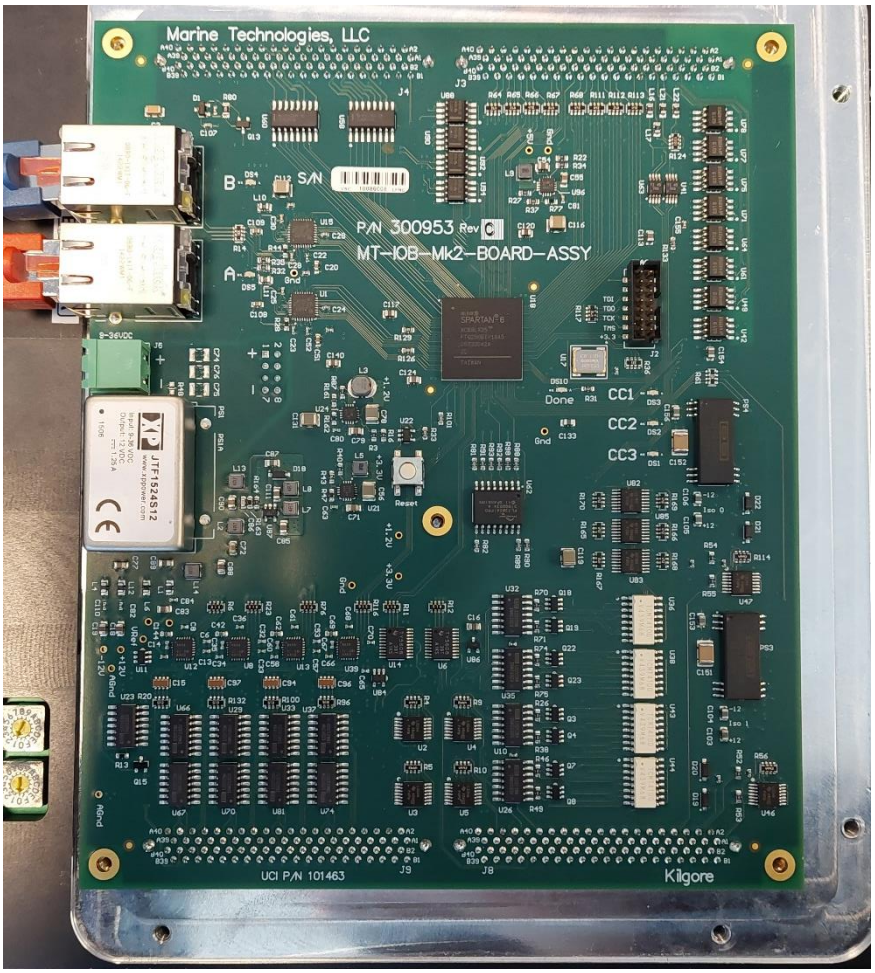

Figure 1-3: Example of a IOB-Mk2 Board

Another circuit board that is essential to fully understand the IOB is the Central-TB (Thruster board). The IOB and Central-TB were designed in tandem with each other, and therefore they are best explained in company with each other.

For another board to make use of the IOB, it must have four sets of 80-pin board to board sockets. The IOB's matching pin headers can be seen on the boards four corners in Figure 1-3. The Central-TB board takes these pins from the board-to-board contacts and passes them on to wire termination blocks on the Central-TB so that technicians can wire I/O to the vessel.

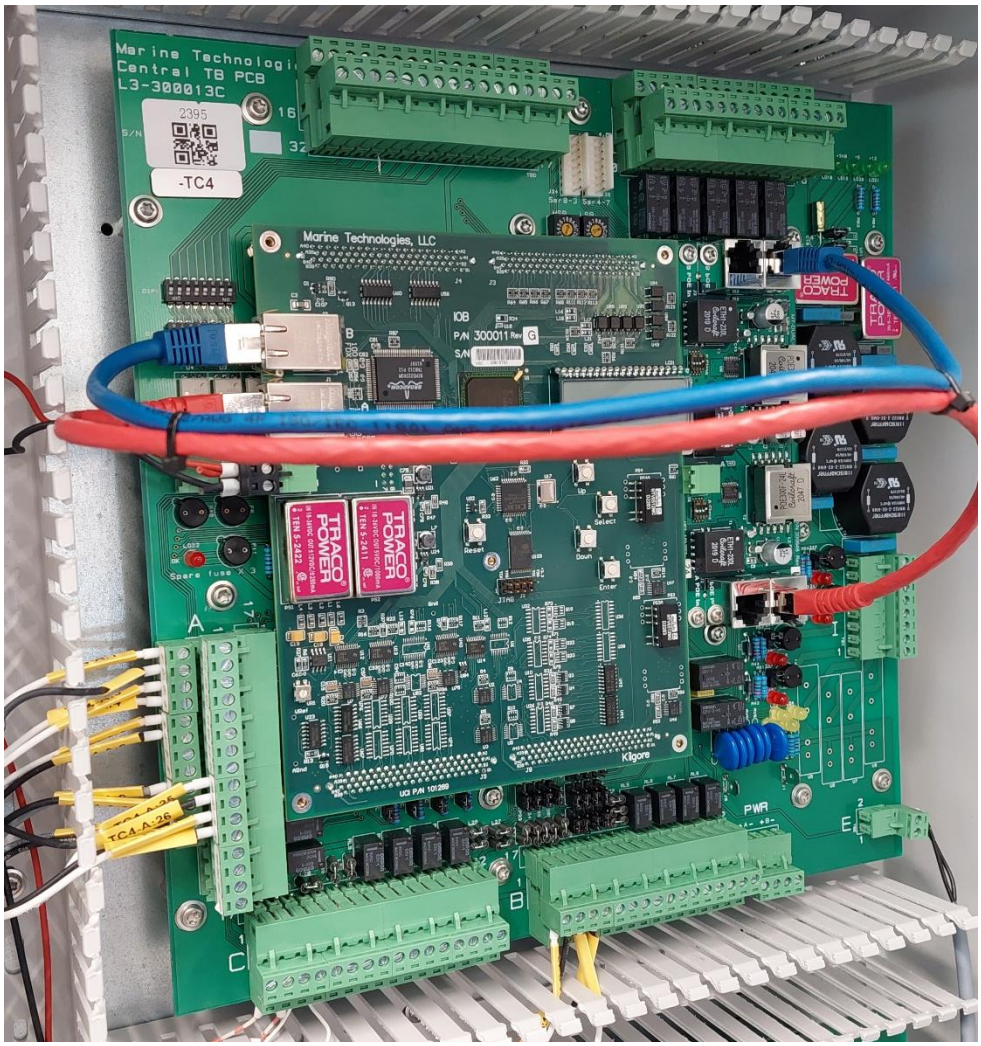

Figure 1-4: Central-TB with an IOB-Mk1 card mounted

1.2 Objective

Though Central-TB's design and manufacture is handled by Marine Technologies, the design of the IOB belongs to a separate company that Marine technologies purchases the IOB from. Marine Technologies needs the IOB to become fully proprietary and have therefore decided to design the next IOB iteration themselves. This thesis outlines the process of the IOB-Mk3 from concept to product, based on the requirements set by Marine Technologies LLC. This is a multi-step process that requires concept evaluation, in-house design review and approval, prototyping and external verification and certification.

The process starts with evaluation of the redesign concept and if it is at all manageable and worth taking the risk of putting in time and resources in development of the IOB-Mk3. The main aspect of this redesign was converting the previous FPGA-based design to a microcontroller-based design. Is essence this is a change from a hardware base processing unit to a device that runs on software code

to process I/O data. This is to our knowledge the first time a software-based unit will directly take on this task in this industry.

The starting objective is to evaluate if the switch from FPGA to a microcontroller could realistically be done. This means compiling all the previous IOB functionality and mapping them to the microcontrollers pin functions and checking for pin availability on the microcontroller, as well as evaluating speed, memory, and reliability.

Next objective is to review peripheral circuitry and its compatibility to the MCU, reworking them to be compatible and updating components that could approach the end of their lifecycle.

After the analyzation portion of the assignment, actual design of a prototype will take place by use of CAD software to create circuit diagrams, a board layout in GERBER format and a specified Bill of Materials (BOM). Circuit diagrams must be made orderly so it can be easily reviewed and understood by others in the future.

Crucially, at the time of writing, the world is still in a state of material and goods shortage. This is especially felt in the electrical component and IC market. Therefore, component sourcing, and choosing easily replaceable components is important in the design phase. Of course, all this is influenced by availability.

With the design finalized, prototype boards will be manufactured so we can perform in-house testing. It is necessary to test and verify all areas of the board to find any faults that exist in the IOB design due to either the circuit diagram or board layout. Discovered faults must be corrected and accounted for in the next iteration of boards until we can satisfy the function requirements.

Finally, after function has been verified, a series of tests performed by a 3rd party authorized laboratory will have to be conducted to receive a lab report, detailing that the board meets all requirements for a device to be used in offshore vessels. The main obstacle and our focus will be on the Electromagnetic Compatibility (EMC) portion of the tests. These tests are often the first to be issued because they are the tests that often fail due to the strict but necessary demands; thus, it is crucial that EMC is heavily considered in the design phase.

1.3 Outline of Thesis

This thesis describes a design that is highly internal to the company and a large portion of the work material are internal documents, schematics and lists that are not publicly available. This implies that there is a distinct lack of external citations and references when addressing Marine Technologies systems related material. Since this is mostly the basis of my work, this results in fewer external references than one might expect in a thesis in total. Internal documents will however be cited and referenced despite not being publicly available.

Chapter 2 Requirements of the New IOB Design

This chapter gives the specific requirements for the redesigning of the IOB. The requirements are divided into two parts. First are the requirements as stated by Marine Technologies, which specifies

the required functionality of the IOB product. Thereafter, focusing on internationally set requirements for devices used in maritime applications. This set of requirements pertains to the sturdiness and compatibility of the device, of which I focus on the EMC tests.

Chapter 3 Predesign Considerations

In this chapter I discuss why the FPGA was the correct solution in the first version of the IOB board from 2002/2003 and why Marine Technologies decided to move forward with the redesign project replacing the FPGA with a microcontroller. Then looking at some of the predesign planning that took place to best prepare myself for the design. I also discuss guidelines for Electromagnetic Compatibility (EMC) minded design, as well as PCB layout and PCB stack principles.

Chapter 4 Design

The different aspects of the design are discussed here. The aspects being component selection, circuit design and schematics. The main principle of the design is a proof-of-concept approach to the IOB-Mk3 where a development kit board is used, combined with a peripheral board to complete the IOB-Mk3-Transit. I mainly compare the previous circuit solutions and consider how to implement them for the new board.

Chapter 5 Test and Verification

This chapter covers the process and findings of the in-house testing process of the IOB-Mk3-Transit board. Here, the tests performed are described, together with the results of these tests. The faults uncovered and their solutions are also presented.

After that, I cover the process of board Certification, mostly looking at EMC testing. I show the results of the successful certification by presenting some EMI graphs of the IOB.

Chapter 6 Integrated Design Phase

This chapter describes the phase where the microcontroller is integrated with the PCB to make a single unit, as well as making general improvements to the design. I look at the process of testing the first version of the IOB and use what was learned to make the integrated board version design.

Chapter 7 Discussion and Conclusion

This chapter concludes the thesis. It discusses the state of the current product at the time of writing, and then considers future work and potential improvements and looks at the lessons learned.

2 The Requirements of the New IOB Design

The redesigned IOB has two primary areas of requirements. The first set is required by IEC (International Electrotechnical Commission) and IMO (International Maritime Organization) and are verified and controlled by DNV (Det Norske Veritas)[2]. The other set of requirements is provided by MT itself.

For anything to be mounted and used onboard a marine vessel, said equipment must comply with a set of rules and requirements that are in place to insure uptime, performance, compatibility and most importantly, crew safety.

For the updated version of the IOB to be successful, these requirements must be met, along with the additional requirements from Marine Technologies itself. This IOB must be function identical to the previous versions of the IOB. To the point where retrofitting previous vessel installations with this new board must be seamless. Marine Technologies must be able to use the redesign as a drop-in replacement for the previous IOB in any given installation.

2.1 Marine Technologies Requirements

As the MT set of requirements are centered on previous IOBs, this chapter will cover what those functions are. Since there are two iterations of the IOB, it is useful to look at the commonalities between them, as that will be an accurate method to examine the required specifications. This set of requirements is mainly based on the IOB-Mk2, but is partially dependent on the Mk1 as well, for example when Mk1's solutions performed more favorably in long term tests and use in the field.

In addition, multiple updates to this set of requirements are done during the project because of information acquired and lessons learned. This section presents the requirements in their final iteration.

2.1.1 IOB-Mk1 and Mk2 Description

The IOB series of circuit boards are Input/Output boards that are made for general purpose use within the Marine Technologies system framework. The IOB must be mounted onto a circuit board made to interface with a specific piece of equipment. The receiving circuit board must be designed to be compatible with the four Board-to-board connectors of 80 pins each and their pinout. When the IOB is mounted, that piece of equipment becomes connected to a network that can command and monitor its I/Os.

2.1.2 Functional Overview

Figure 2-1 displays a block diagram with the required functions to be present on the IOB-Mk3. All the functions are peripherals that are required to be connected to the MCU apart from the +-10V reference that is mainly used to bias joystick potentiometers. All these peripherals need to connect

[2] DNV – Det Norske Veritas are the world's leading classification society and a recognized advisor for the maritime industry. https://www.dnv.com/

to the MCU because the MCU's main task is to pack all the data into an ethernet package structure and forward it to the network and the control computers.

There is also a physical form factor requirement regarding mechanical mounting and electrical connection. The dimensions of the board and the placement of the M3 screw holes must be identical to Mk1 and Mk2. The electric connectivity points that have been present in earlier versions must also be present in the updated version. Of these, there are five pin headers that require identical placement to the previous versions. Four of them are the 80-pin board-to-board connectors that are responsible for breaking out the IOB's functionality, and the last is J6, the 24VDC input power connector. The rest of the electrical connection points should be placed as identical to the previous versions as possible.

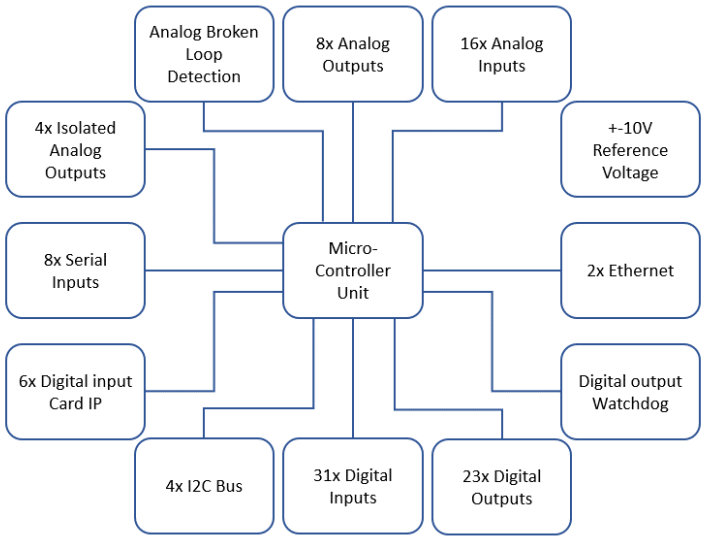

Figure 2-1: Sketch given the functional requirements of the IOB in terms of functional entities.

Table 2-1 shows the peripheral functionality available on the Mk2 IOB and some notes on each function. Comparing the block diagram in Figure 2-1 with this table, notice the I/O reduction in some of the functions, like analog inputs for example. The requirement reduction stems from an overestimation in previous specification that has not been necessary to correct until recently. However, the reduction in the amount of I/O in each function greatly eases the requirement and makes it easier to accomplish.

The IOB's actual I/O requirement has been thoroughly observed by the example of use over 20 years, those observations can be used to cut down the requirement of the IOB-Mk3 to its actual requirement.

Table 2-1: IOB-Mk2 Functionality Summary Table

Interface	Amount	Notes
I2C Buses	4	Standard I2C
Digital Inputs	32	Triggered by grounding the input
Digital Outputs	34	Darlington Collector type pulldown output
Analog Inputs	32	Can read either +-10V mode or 4mA to 20mA mode. (External shunt resistor required for current mode)
Analog Outputs	16	+-10V out and 4mA to 20mA
Isolated Analog Outputs	4	+-10V out and 4mA to 20mA
+10V Reference	1	100mA polyfuse (Resettable fuse)
-10V Reference	1	100mA polyfuse (Resettable fuse)
RS-422 RX Inputs	8	Convert differential RX input to single wire UART RX signal
IP Address Inputs	8	Digital inputs reserved to determine the IOB's IP address
Ethernet Interface	2	Network A and B both present for redundancy

I/O reduction was done by looking at every single circuit board that the IOB is paired with, and taking note over what pins from the IOB that the product board has available for use. To clarify "available for use", I mean no actual wires are connected to that specific I/O, hence that I/O is not electrically supported by that product board.

A table that lists the IOB connector pinout and what functions are electrically supported by the product boards, and hence what functions can be omitted, can be found in the appendix.

It is important to keep any function that is used, even if a function is only used with one product board, since the Mk3 is required to be a drop-in replacement for the Mk1 and Mk2, both in older and newer installations.

2.2 International Requirements

The international requirements can be divided into two parts in this project, the most difficult requirement to fulfill tends to be the EMC portion, as it is easy to underestimate its strictness. The second part is environmental testing, which demands that the device function and integrity is maintained across many circumstances and stresses that the device can experience in the field. This section gives a summary of these requirements[3].

The usual major obstacle of the certification process, hence a major focus in this thesis, is to make the product conform with the EMC requirements stated in IEC-60945. See Table 2-2, Table 2-3 and Table 2-4 for the requirements. The EMC requirements are made up of two parts, conducted emissions and

[3] The documents that the requirements are based on are not available free of charge.

radiated emissions. These two parts focus on different frequency areas and have different emission limit requirements. Keep in mind that to meet the requirements, the equipment under test must beat the requirement listed, along with a margin equal to the third-party laboratory's measurement error margins worst case scenario. Also observe that in the radiated emissions requirement, there is an exception range at 156MHz to 165MHz. This is the emergency frequency band, in which the requirements are ever stricter to ensure proper communication in times of distress.

Table 2-2: Conducted Emissions IEC 60945

Frequency Range	**Emission Limit**
10kHz – 150kHz	96 dBµV – 50 dBµV
150kHz – 350kHz	60 dBµV – 50 dBµV
350kHz – 30MHz	50 dBµV

Table 2-3: Radiated Emissions IEC 60945

Frequency Range	**Emission limit**
30MHz – 2GHz	54 dBµV/m
156MHz – 165MHz (Exception range)	24 dBµV/m peak (Or 30 dBµV/m Quasi peak)

Table 2-4: Radiated Emissions DNV 0339

Frequency Range	**Emission Limit**
150kHz – 300kHz	80 dBµV/m – 52 dBµV/m
300kHz – 30MHz	52 dBµV/m – 34 dBµV/m
30MHz – 1GHz	54 dBµV/m
1GHz – 6GHz	54 dBµV/m
156MHz – 165MHz (Exception range)	24 dBµV/m peak (or 30 dBµV/m Quasi Peak)

The challenge with EMC requirements is that it is difficult to know how your prototype performs prior to executing the tests in a designated lab facility; EMC lab facilities of good quality are hard to come by as well. There is a high probability that EMC issues will be uncovered while attempting to get the device certified. However, the designers should try to follow typical EMC friendly design guidelines to minimize EMI as much as possible. Those guidelines will be explored in section 3.3.

As for the environmental requirements, these include being able to withstand situations such as high voltage ESD to buttons that one can expect personnel to touch, temperature variation, mechanical vibration, power supply spike and power supply voltage drops.

Arguably the issue of functional redundancy is also a requirement, but this is already considered by matching the functions given by the previous iterations of the IOB. The only real instance of function redundancy present on the board are the two ethernet interfaces (NET A and NET B), making the board network redundant. These interfaces have the same functionality, but in case the active network interface loses connection for some reason, the other interface will be used instead.

3 Predesign Considerations

With the stated requirements in mind, there are further considerations to make. Typically, the design process starts with understanding the requirements, considering them and their implications, planning possible solutions and then starting the design. However, anyone in this position quickly learns that with a complex system, this approach is an oversimplification.

One cannot completely understand the requirements and foresee potential adaptations of the requirements beforehand. Additionally, one cannot plan for every case and complication before shaping the design. This chapter will however present the initial planning that is crucial for being able to proceed to the design phase.

3.1 FPGA and Microcontroller in the IOB

The first and major consideration, the one that the whole project leans on, is the microcontroller. The main feature and major difference from previous iterations is the fact that Marine Technologies has been using IOBs with FPGAs as their processor for 20 years. That is 20 years of field testing on actual in use vessels, and 20 years of finetuning the firmware and circuitry. It is truly a big risk to change something that has worked reliably for that large amount of time.

The main reason for the redesign of the IOB is that the IOB is not proprietary to Marine Technologies. Instead, they are bought from another company that designs and manufactures them. Since the IOB is a very important product, it is of great long-term value for Marine Technologies to own the design themselves. Thus, redesigning and making the IOB proprietary has been a goal for some time. However, the worldwide component shortage following the 2020 global pandemic pushed the issue forward. As the FPGAs as well as other components used for the previous iterations of the IOB were no longer available anywhere, the question arose if the functionality of the IOB could be implemented by a microcontroller instead.

Using FPGAs for the IOB in 2002/2003 made sense since the flexibility, stability and I/O capacity of an FPGA far outmatched that of any microcontrollers at the time. In the early 2000s, reprogrammable flash MCUs that matched the price of One Time Programmable MCUs had barely hit the market [1], and they had very limited memory capacity and pin availability. In short, microcontroller technology and capability were just not mature enough to handle the I/O load needed for the IOB, therefore the processor chosen for the first IOB was the “Xilinx Spartan XC2S600E” FPGA [2].

Now, choosing a microcontroller in the redesign is not unthinkable, since the MCU capability has in many ways been improved to the point that they can cover the processing requirement of the IOB at a significantly lower cost. The availability is better, and writing code for the MCU is something Marine Technologies already has in-house competence to perform. FPGA technology is still more capable and powerful, but the microcontroller suits IOB’s needs sufficiently at a considerably lower price point.

The proposed Microcontroller is the “STM32H743ZIT6” [3]. This microcontroller comes in a 144-pin package with sufficient general-purpose I/O, memory, and on-chip functionality such as I2C buses, SPI lines, UART channels and RMII support. All these capabilities are necessary for the chip to be useful to the IOB-MK3.

3.2 Microcontroller Considerations

The microcontroller is a flexible piece of hardware that is essentially a microprocessor equipped with peripherals, such as RAM and ROM memory, timers, input/output ports (I/O) and often communication hardware such as I2C, SPI, CAN, UART. This combination of hardware makes a computer that is programmable to interface with many types of sensors and devices. The microcontroller can gather data from sensors, store the data, report information through a network connection, and use its own I/O to act upon gathered information as decided by the custom program running on it. It is a small chip with the capability to control local peripheral electronics according to custom specifications.

One important decision made was to utilize the ST Microelectronics Development board for the prototyping. Shown in Figure 3-1 is the demo board called “Nucleo-H743ZI2” and its circuit board reference is “MB1364” [4]. On this demo board, the microcontroller chip “STM32H743ZIT6” is mounted and it’s I/O is made available on two connectors (CN11 and CN12). Rather than mounting the microcontroller directly onto the prototype board and testing the whole system, the development board itself would be mounted on a prototype PCB containing all the peripheral electronics needed to complete the IOB. In this way, the design is split into two stages, where the design and functionality of the peripherals could be tested with the certainty that any potential fault is not due to the MCU and its supporting electronics. The other significant advantage, especially considering the component shortage, is that one MCU can be used on multiple prototype boards to test different fixes and tweaks that are done in the testing phase.

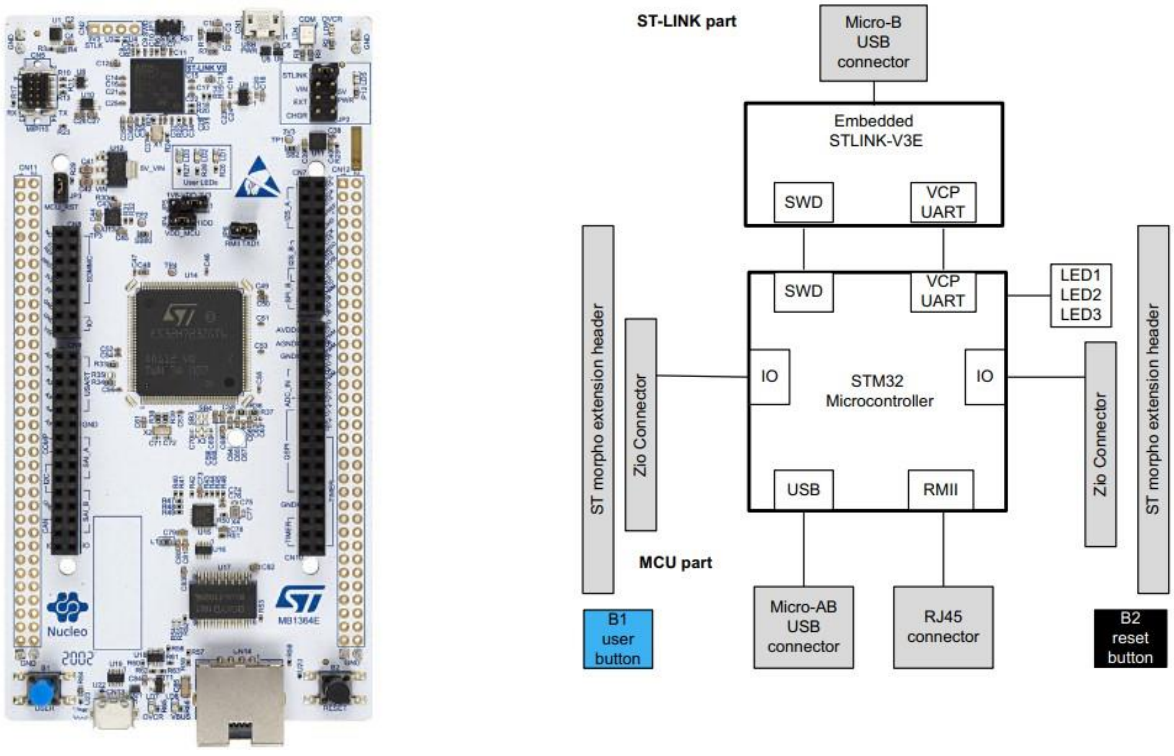

Figure 3-1: Nucleo MB1364

3.2.1 Pin Function Planning

The development team at Marine Technologies determined that the chosen STM32 has enough processing power, speed, memory, and available functions. However, there is a crucial difference between microcontrollers and FPGAs that complicates the task. In an FPGA there is freedom to configure what type of functionality a pin should have; mostly any pin can be used to implement functionality such as SPI, UART or I2C. In an FPGA based design one can simply configure the functions that you require a pin to have and assign that function to a pin that you deem appropriate, providing a large degree of flexibility.

A microcontroller on the other hand, hardwires certain functions to designated pins by design and this cannot be changed later by a user. To offer some flexibility to the designers, the MCU has several instances of the same peripheral connected to different pins, as well as multiple peripherals multiplexed onto the same pins. The latter implies that all peripherals offered by the MCU architecture cannot be used simultaneously. In other words, by selecting a set of pins for a specific interface, you are actively removing the use of the available peripherals from the MCU, and selecting pins becomes somewhat of a game of “microcontroller solitaire”.

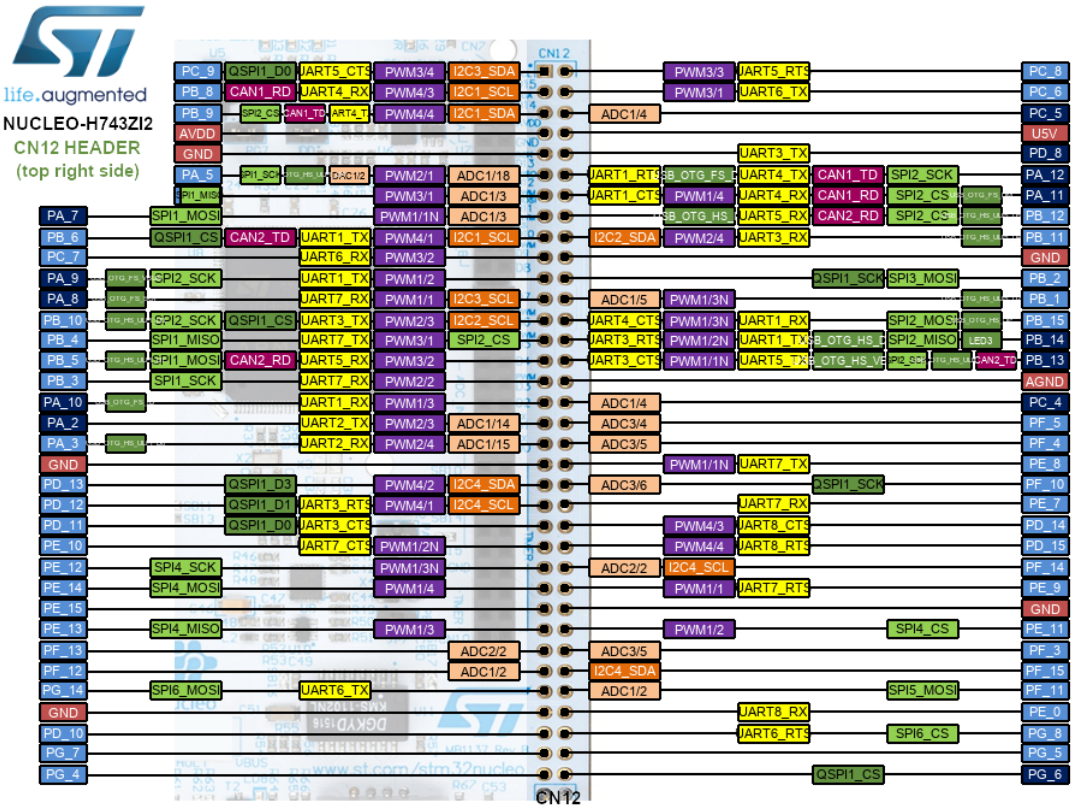

Figure 3-2: Nucleo Demo Board CN12 [5]

See Figure 3-2 for a visualization of the Nucleo connectors CN11 and CN12 and how the pin functions are overlayed. The first step in planning how to assign pins is to find out what pin functions must be present; defining the bare minimum function requirement and how many pins we can reduce our use to. Once the necessary pin types have been defined, the game of solitaire begins, using the map of pins from the figure and the microcontrollers datasheet.

Analyzing Marine Technologies hardware environment, I realized that there is an excess amount of I/O present in the IOB. MT hardware does not have physical wire connections to half of its analog input and output, as well as a few digital I/Os. This resulted in being able to reduce the requirement substantially by removing three SPI buses entirely. Additionally, some of the analog inputs (AI 27, 28, 29) were only used in one instance on a specific piece of hardware where they were the only AI present, thus they could also be redirected to be the same as AIs 13, 14 and 15.

The completed pin assignment of CN11 and CN12 can be found in the appendix along with the chart that shows I/O usage and simplification.

3.3 EMC Minded Design

Taking EMC into account when making PCBs can be confusing. More often circuits will involve some sort of high frequency that will be able to radiate and cause disturbance. Every long cable attached can act as an antenna, every switching power supply in the circuit can result in radiated and conducted emissions and every high-speed data line requires careful EMC design considerations. Conducted emissions is noise that travels from the device and into the power grid that the device is connected to; this of course can affect other devices on the power network and is therefore important to regulate [6]. Radiated emissions are propagated as EMI through the air and can affect the function of instruments, communication, and devices in proximity to the radiating device and is therefore important that it is regulated.

3.3.1 The Path of Least Inductance

The main effect that will shape the design is the awareness of the behavior of electrical current when it is of a higher frequency. Frequencies emitted from devices start to be measured at 10kHz conducted and 150kHz radiated. It is often taught that electrical current will always seek to travel the path of the least resistance, which is somewhat true, but that's not the whole picture. Current will seek and travel the path of least impedance. Impedance equals resistance for low frequencies, but for higher frequencies, inductance comes into play as well. As a rule of thumb, the path of least inductance lies directly under the signal trace [7].

In Figure 3-3 you can see the difference between a low and high frequency return path. The image depicts a signal going between two components on the top routing path, with a solid and continuous ground plane beneath them.

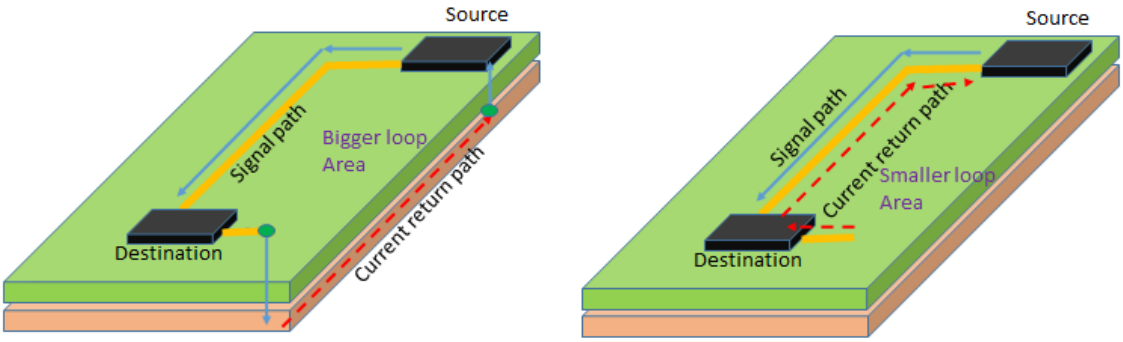

Figure 3-3: Current return path visualization of a high frequency signal [8]

In the image to the left, the current return path follows the shortest, most direct path because of its low resistivity, which is indicative of its low frequency behavior. The key is to notice the loop that it creates and that all current exist as loops as per Kirchhoff's Current law. The area inside of any given current loop is important because it forms an antenna.

In a DC (Direct Current) environment this is not an issue since there are no frequencies to radiate, until noise is introduced to the loop or if the signal is a varying signal. The frequencies of the noise or signal that is tuned to the current-loop will use that loop as an antenna, because it is one, and it will radiate. Frequencies with a quarter of their wavelength matching the loop antennas length, will be able to make use of the antenna.

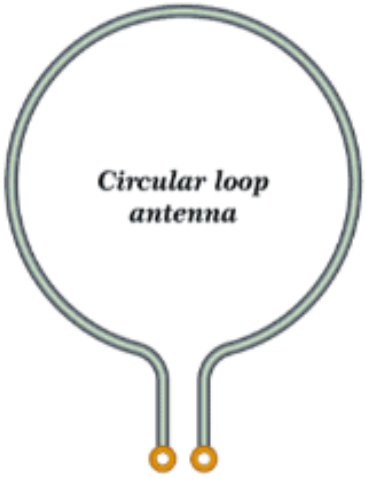

Figure 3-4: Circular Loop Antenna

However, following good design practices as the frequency increases, the path of least impedance will be determined by inductance rather than resistance, and the current's return path will seek itself directly under the signals outgoing trace wire.

This naturally closes the loop and restrains the loop antenna's ability to radiate. This is shown in the right side of Figure 3-3. In poorer designs, if the return path is restrained from directing itself under the trace wire, in which case the loop area and shape is maintained, and the antenna has access to higher frequencies to radiate.

3.3.2 Layer Structure and Polygons

Having established that the best practice to reduce radiated EMI is to allow the current return path to have a way to follow directly under the outgoing trace. The best way to do this is by having dedicated power and ground planes and polygons for the current flow to use freely. In PCB design, copper pours are used to fill copper into polygon shapes defined in the design, which is very practical for designating zones of operation, such as separating the digital zone from the analog zone.

In a PCB stack up there are multiple possibilities to how you organize your layers. It is common to break the layers into three main categories; these are the grounding layer, the power layer and finally the signal layer. The fourth category, when relevant, is the high-speed signal layer. In this instance, I chose to work in 8 layers to afford myself some flexibility in routing and I chose to mount SMD (Surface Mounded Device) components on both sides of the PCB. With this configuration, the usual way to proceed with 8 layers is to delegate four of them to signal traces, two of them to power distribution and the remaining to for ground reference.

The next step is to order these layers in the stack up; and which configuration to choose is based on application and preference, but let's look at two examples [9].

Table 3-1: PCB Layer Configuration Examples

Configuration	Shielding	Power Coupling
Layer 1	SMD pads and Ground	Signal 1
Layer 2	Signal 1	Ground
Layer 3	Power	Signal 2
Layer 4	Signal 2	Power
Layer 5	Signal 3	Ground
Layer 6	Power	Signal 3
Layer 7	Signal 4	Ground
Layer 8	SMD pads and Ground	Signal 4

The shielding configuration example in Table 3-1 presents a stack up order that prioritizes shielding the signals. However, one must be careful while routing, however tempting, to not utilize the top and bottom layer for routing, since this breaks the continuity of the ground plane and can then force returning current to take a non-optimal path.

In the power coupling configuration, the power and ground planes of layers 4 and 5 are close together, allowing for good signal integrity. Also, the ground planes are more intact due to not hosting all the SMD pads on the top and bottom layer.

4 Design

The PCB design presented in this chapter is called the IOB-Mk3-Transit Board (Figure 4-1). It is named so due to it being the peripheral board that sits between the Nucleo development board that holds the MCU and the target board that needs the I/O control. The name also marks the transition from FPGA based I/O control to MCU based I/O control. This board is distinctly different from the board that is covered in chapter 6, where the fully integrated MCU board will be referred to simply as IOB-Mk3. The IOB-Mk3-Transit and IOB-Mk3 are two different boards.

The design of the IOB-Mk3-Transit peripherals was a systematic approach based on looking at the different sections of the previous IOB iterations (IOB-Mk1 and IOB-Mk2) and analyzing their circuits by function and component choice. The goal is to reuse as much as possible due to the proven robustness of previous iterations. Each segment of the following chapter will contain an explanation of the function solutions of the IOB-Mk1 or IOB-Mk2 and whether I am directly adopting the solution and components; solutions that have been changed, along with the how and why they have been changed, follows where applicable.

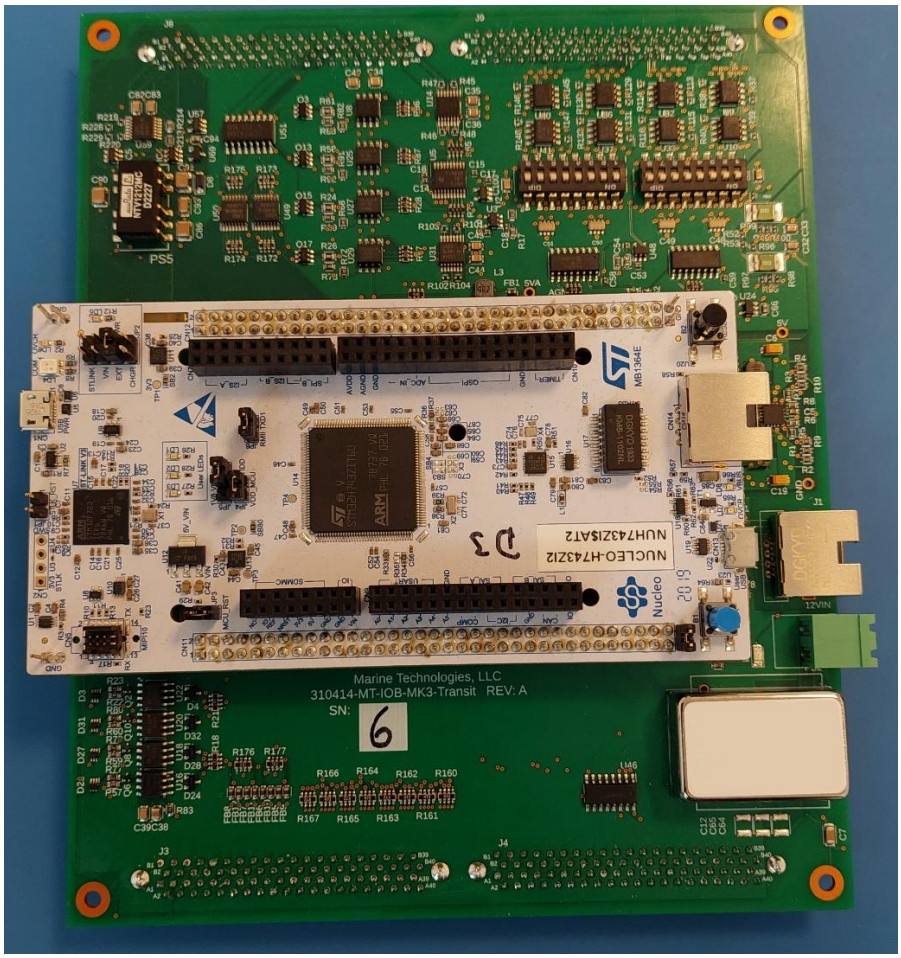

Figure 4-1: IOB-Mk3-Transit Board

4.1 The Digital Inputs and Outputs

The digital I/O section contains digital inputs (DI) and digital outputs (DO) and bases itself on the principle of a DO pulling down the DI to ground, therefore triggering it. Meaning that the DI is pulled up in a high state by default and the DI supplies the DO port with itself and a grounding wire. The DO then only has to connect these two wires, pulling the DI down to a low state, which is then registered as a DI trigger. The DO can do this with a dry-contact, which is just a potential-less switch, connecting two wires.

4.1.1 Digital Inputs (DI)

There are two implementations of the pullup network on the previous iterations of the IOB. One for the Mk1 and another for the Mk2 shown in Figure 4-2.

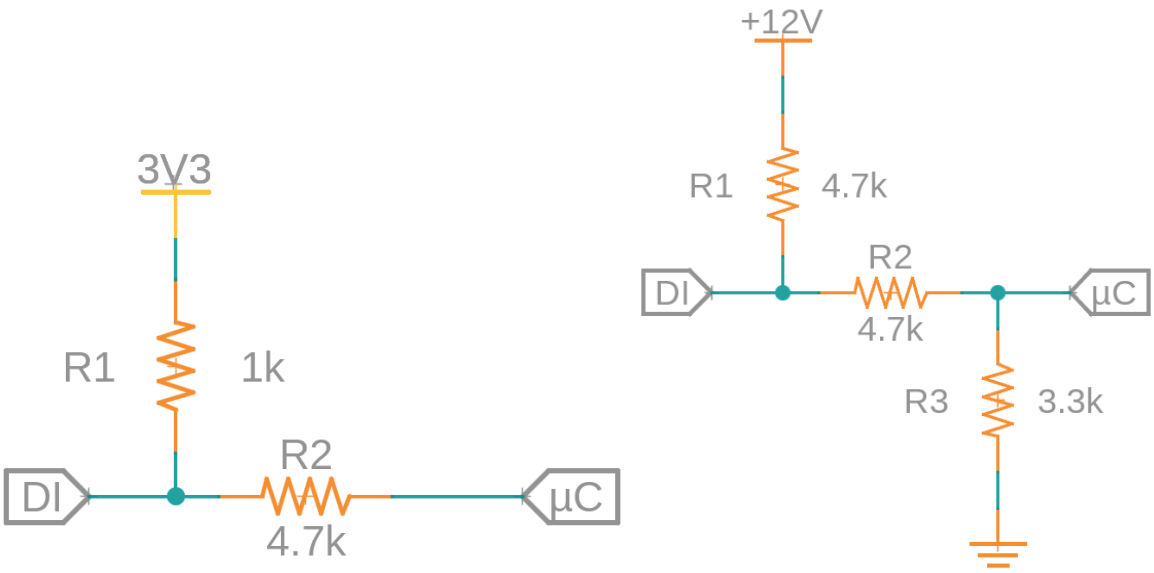

Figure 4-2: Mk1 DI (Left) and Mk2 DI (Right)

The reason for the difference in these two iterations is due to an issue on the Mk1 that can sometime occur where the input if falsely triggered, likely due to a sudden low resistance to ground on the data line. It has been noted over time that the suggested solution on the Mk2 did not improve performance in this matter and indeed made it somewhat worse.

Doing some testing with a simple potentiometer connected between the input and ground, I found that the Mk1's input configuration registered a trigger when the potentiometer reached a value of about 600Ω and below. Meanwhile the Mk2 input registered a trigger already at 1kΩ, making it easier to falsely trigger, which would explain the reports of Mk2's digital input performance.

To improve on Mk1's design while adapting the pullup structure to the STM32 microcontroller, the design for the Mk3 Transit card combined aspects of both previous iterations. The idea is to use a 12V

pullup to increase the amount of voltage that must be redirected for the digital input to register. Also, the higher resistance is to ensure that the microcontrollers pin is protected from stresses and injection currents; later and finer adjustments to the resistors can be made in following revisions of Mk3.

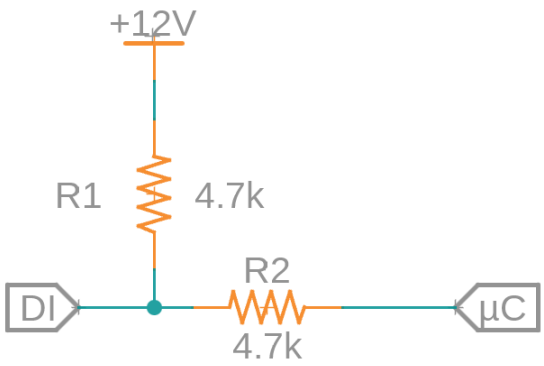

Figure 4-3: Mk3 Transit DI pullups

4.1.2 Digital Output (DO)

The digital output located on the IOB is a Darlington transistor pulldown type. This means that the microcontroller raises the voltage on the base of the Darlington component shown in Figure 4-4 as device U31. This pulls down the collector pin on the other end, acting like an inverter with a decent current sinking capability. However, this sinks current to its own local ground reference connection and is not the dry-contact referred to in section 4.1.1 Digital inputs.

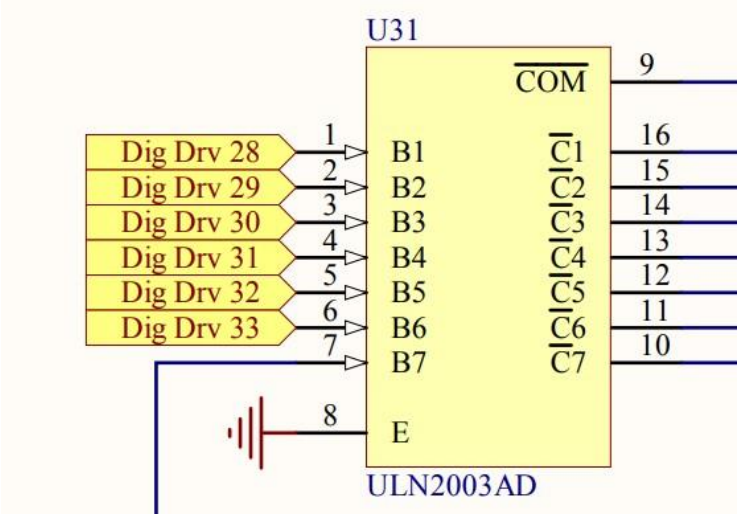

Figure 4-4: IOB-Mk2 Digital Output Driver [10]

The Central-TB extends the IOB's digital output by using the current sinking capability of the Darlington component to power a mechanical relay component (Figure 4-5). Now the IOB is equipped with a potential free dry contact to toggle other external devices.

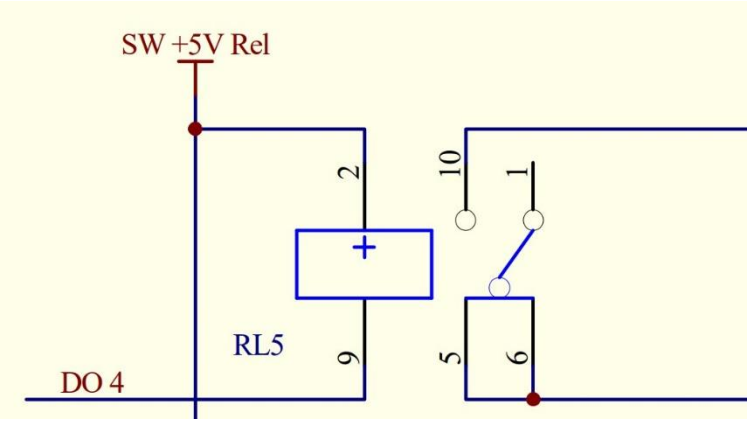

Figure 4-5: Central-TB Digital Output Relay

The relay is connected to the voltage "SW +5V Rel" which is only available if the IOB's watchdog signal is active, thus all digital outputs are disabled if the watchdog signal is in an alarm state. To clarify, a watchdog signal is fed into the B7 pin in Figure 4-4, which then controls the mechanical relay that allows the "SW +5V Rel" voltage to feed into all digital output relays, making them available to toggle.

4.1.3 Watchdog

In the case of network connection loss, the IOB no longer receives updates to the digital output states. Digital outputs control external devices, or mechanical processes that in an event of connection loss should not be latched in active state. Therefore, the IOB is equipped with a watchdog that oversees the function of the digital output relays. In the case of the Central-TB, this watchdog circuit activates the mechanical relay that feeds the driving current to every digital output mechanical relay; whilst the watchdog is inactive, every digital output on the Central-TB becomes inactive.

The watchdog circuit is driven by monitoring a heartbeat signal from the IOB, which in turn is only output when the IOB detects that it is connected to the network via NET A or NET B. In short, if the IOB is connected to the network, the heartbeat is enabled, and the digital output relays can be operated. In the IOB-Mk1 and Mk2, this is solved by using a charge pump that charges itself by using the heartbeat output generated by the processing unit. On the IOB-Mk2 that heartbeat is a 50kHz square wave signal.

Figure 4-6 shows the charge pump watchdog circuit on the IOB-Mk2. Capacitor C107 functions as an AC bypass capacitor for the heartbeat signal. The two diodes in Figure 4-6 act as one way charge valves; the diode on the bottom of the figure acting as the valve that lets capacitor C7 to receive a

charge current when the heartbeat is at 0V; the diode at top of the figure allows capacitor C107 to equalize itself when the heartbeat is at 3.3V.

Notice that the voltage over capacitor C7 is shared with the MOSFET's Gate-Source voltage, which decides if the MOSFET will be turned on or off. As the heartbeat continues to charge C7, the Gate-Source voltage increases, and at some point, the MOSFET's voltage threshold is met, turning the MOSFET on; with the MOSFET turned on, the IOB's digital output driver can power the relay that feeds current to all the digital output relays.

If the IOB loses connection, the heartbeat signal freezes to a static value of either 0V or 3.3V, at which point the C107 capacitor will act as a break in the circuit, allowing capacitor C7 to equalize its charge though resistor R80, switching off the MOSFET, which then cuts off the power supply to all digital output relays.

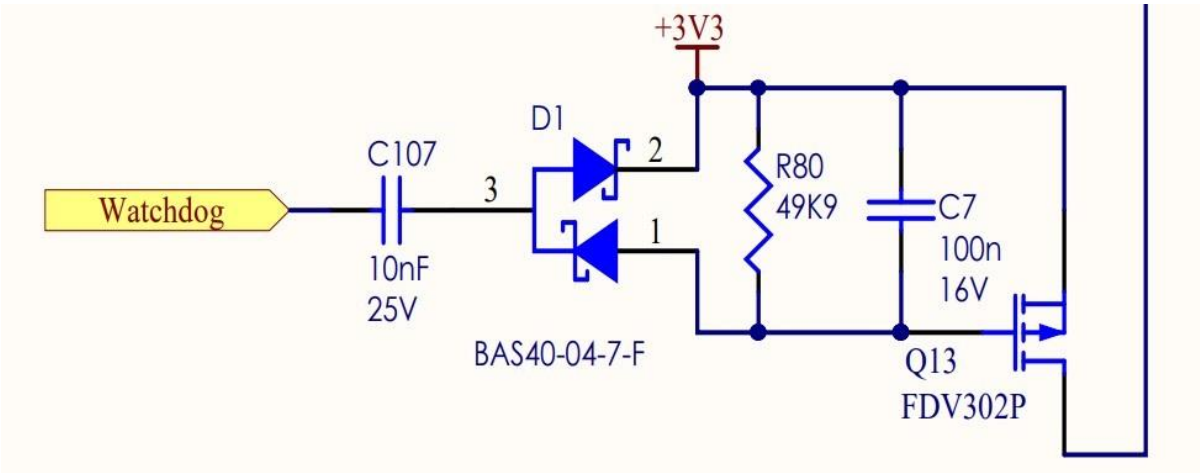

Figure 4-6: IOB-Mk2 Watchdog

This is a solid and reliable method that relies on easy-to-acquire passive components, and it is easy to tweak its alarm time by adjusting the values of the of its resistor and two capacitors. However, the 50kHz heartbeat signal from FPGA is harder to reliably replicate and maintain by the microcontroller; there is no guarantee that the microcontroller could reliably keep the heartbeat stable at 50kHz without delays that would trigger an alarm.

Often, a watchdog function overseen by a microcontroller is handled by an additional external component, like for example from the STWD100 component series [11]. The STWD100 is an IC (Integrated Circuit) component that only requires a toggle of the input signal state within an alarm period that is predefined by the component. A valid toggle of the input signal is both a falling and rising edge of the input signal, and the alarm time on the circuit chosen and shown in Figure 4-7 is 6.3ms. This is easy for the microcontroller to handle consistently without experiencing a delay of that would surpass the alarm time, making this a safe choice.

However, in future revisions and tweaks of the Mk3 board, after evaluating the performance and assessing if more processing capacity is available, the previous charge-pump solution could be calibrated for a slower and more manageable heartbeat signal and reintroduced as a solution.

As a sidenote, there is an annoyance to the function of the STWD100's alarm function. In the event of a dead input heartbeat signal, the STWD100's output alarm, which is an active low signal, repeatedly toggles high while in the alarm state. Usually, this component is used to reset a frozen processor, in which case having the alarm rise temporarily allows some time for the processor to reboot. However, in the IOB's case, this repeatedly activates the mechanical relays. Therefore, a pullup resistor and capacitor on the STWD100's output is used to effectively negate these output pulses.

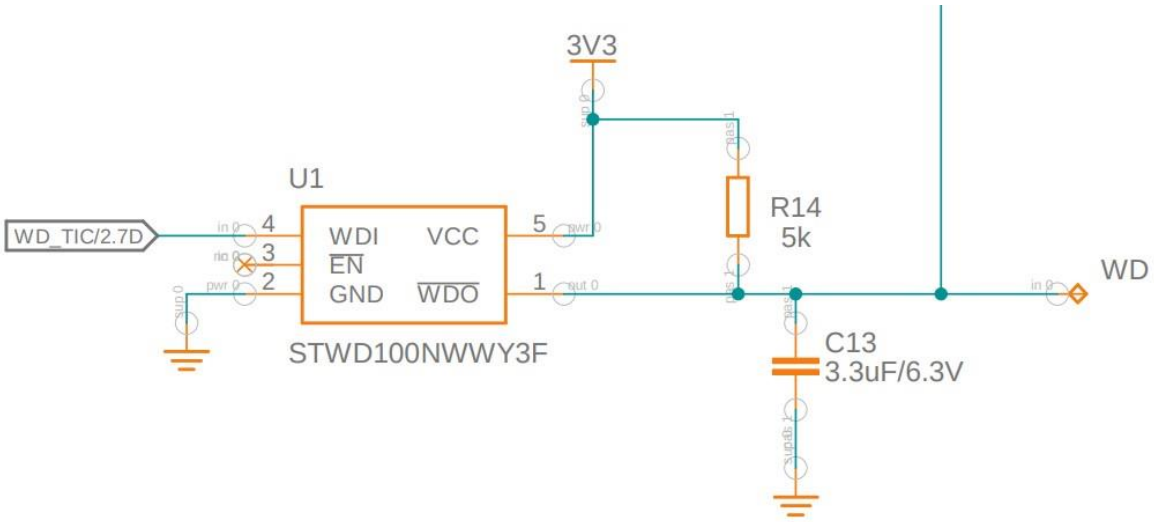

Figure 4-7: IOB-Mk3 Transit Watchdog circuit

4.2 Analog Inputs (AI)

The analog input (AI) section of the IOB-Mk3-Transit deviates from Mk1 and Mk2 design quite a lot due to component shortages. Both ADCs (Analog to Digital Converter) used for the Mk1 (TLC2578IPW) and the Mk2 (ADS8638SRGER) were not available, as well as the operational amplifier (INA2132UA) used by both iterations.

4.2.1 Mk1 and Mk2 Analog Input Design

The analog input portion of the IOB is designed to read a current (4mA to 20mA) or a voltage (±10V). Figure 4-8 shows the circuit that is a standard differential amplifier follower by an RC circuit for low pass signal filtering. The analog input can read both differential and single ended outputs without needing to ground the negative differential wire, this is due to the virtual ground present in the case that the LO connection is left floating [12]. The circuit reads a current by sampling the voltage off a shunt resistor located on the Central-TB circuit board.

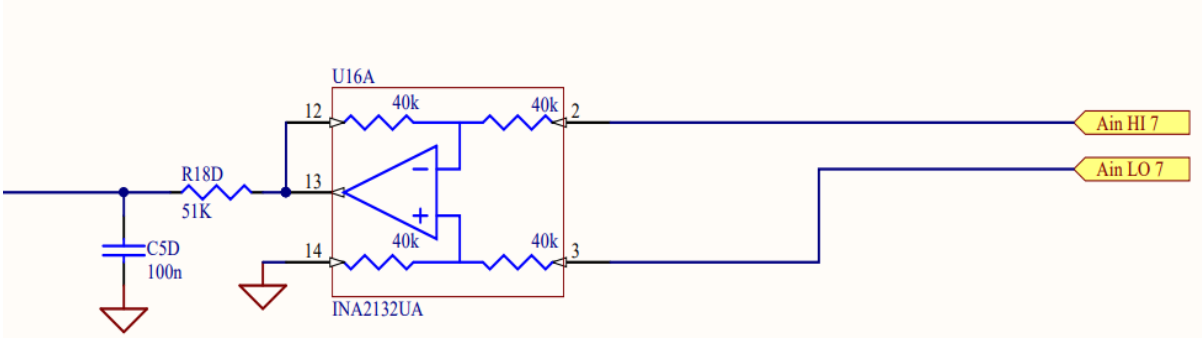

Figure 4-8: Stage 1 Analog Input IOB-Mk1 and Mk2

The input voltage is received by a differential operation amplifier configuration, which works by subtracting the voltage at the negative terminal from the voltage at the positive terminal. This configuration solves this elegantly by choosing all resistors in the circuit to be of an equal value, in this case the INA2132UA internal resistors are precision cut to 40kΩ. This simplifies the gain of the circuit by setting the gain ratio to $\frac{R_2}{R_1} = 1$.

The positive component works as a standard non-inverting amplifier configuration except for that the input is halved before interacting with the gain of the amplifier. All resistors being equal allows the positive input to be connected to a voltage divider (R3 and R4) that exactly halves the input at the positive terminal, making the positive terminal contribution equal $V_{O+} = V_{I+}$.

The negative component is summarized as a standard inverting amplifier, with equal resistors, its contribution can be simplified to $V_{O-} = -V_{I-}$. Adding these two components gives us equation 1, that states that the circuit simply subtracts the negative input from the positive input and outputs the result.

$$V_O = V_{I+} - V_{I-} \tag{1}$$

The primary function of this circuit on the IOB is to be able to input either a single ended or a differential voltage input and leave us with a single ended output for further processing. It is always recommended to use differential mode for transferring the analog signal over long distances due to common-mode noise cancellation.

The IOB-Mk1 uses the TLC2578IPW ADC using an operational amplifier in the non-inverting voltage follower configuration (AKA buffer) as stage 2 of the analog input, feeding into the ADC [13]. This buffer allows the LP filter in stage one to benefit from the low leakage current into the buffer and eliminates operational amplifier loading effects due to the ADCs analog input currents; the buffer allows amplifier stage one to be unaffected by the current demands of the ADC.

The IOB-Mk2 uses the ADS8638SRGER ADC instead, which has a low current demand on its analog input ports, rated as a leakage current at 200nA [14]. This allows the IOB-Mk2 to forgo the buffer

circuit and have the subtracting amplifier in stage 1 to directly feed into the ADC since 200nA does not stand to have any substantial loading effect on the amplifier.

4.2.2 Mk3-Transit Analog Input Design

The analog input of the Mk3-Transit required a different structure due to the lack of ADC availability. The ADC components used in the previous IOB iterations used ADCs capable of directly reading voltages spanning -10V to +10V, a span of 20V. The replacement that was the safest to rely on, component stock-wise, was the MCP3208 [15]. This ADC, however, can only read voltages in from 0V to 5V.

This poses a challenge when the desired function of the analog input is to read both a ±10V signal and a 0.88V – 4.4V signal (4mA to 20mA on a 220Ω shunt resistor) on the same circuit. The solution decided for this issue is to have a second stage between the receiving op-amp and the ADC; the second stage's task is to dampen the signal and squeeze it into the 0V – 4V range, keeping a margin from the maximum voltage rating of the ADC's input pins. Figure 4-9 shows the second stage op-amp.

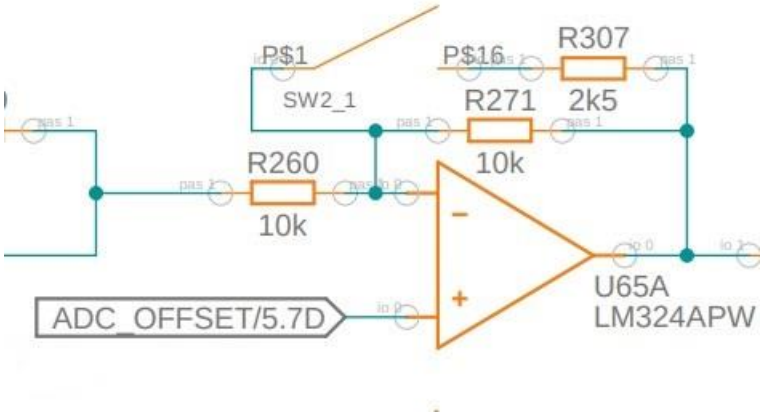

Figure 4-9: Mk3-Transit AI stage 2

Now there is a large reduction in readable voltage range, since the ±10V signal had to be dampened five times to attain the desired 4V range. This also damps the current-based signal by five times, and the already lower range is reduced to a mere 0.7V range total (0.176V at 4mA and 0.88V at 20mA). So, by adding a DIP switch on the PCB to add in an optional parallel resistor, I can change the damping and the offset to maximize the range and improve the reading for both modalities.

The "ADC_OFFSET" seen in Figure 4-9 is set to 2.3V by a voltage reference, followed by a voltage follower. Now, with the switch turned on, the second stage dampens, and translates ±10V into a signal that is 2.76±2V; this is the voltage reading mode. With the switch turned off, the output offset changes from 2.76V to 4.6V, and the voltage that is input decreases the output voltage by the same value; the current reading mode now has a range that is 4.6V at 0mA, 3.72V at 4mA and 0.2V at 20mA. The

reason I specify and separate the 0mA value, is that it is specifically used as a broken loop detection function; the true range of the signal, is 4mA to 20mA.

4.3 Analog Outputs (AO)

The analog output (AO) has two output modalities, a voltage (+-10V) mode and current (4mA – 20mA) mode, and they are both commanded simultaneously by the same DAC (Digital to Analog Converter) circuit which in this case is the TLV5608IPW. This device is an 8 channel DAC that is connected to the MCU via SPI communication and it outputs 0V to 5V on each of its 8 channels.

Each DAC output channel is connected both to a voltage output amplifier circuit and a current output amplifier circuit simultaneously, without multiplexing on the IOB. Multiplexing is not necessary since the Central-TB ensures that only one output modality can be used on a given analog output. The Central-TB board chooses an output's modality by physically disconnecting the other output mode option with a jumper strap, basically the output mode selection/multiplexing is done the user. See Figure 4-10, this is the analog output mode selection on the Central-TB, where jumper straps are used to select only one output mode to the respective analog output channel's designated wire terminal [16].

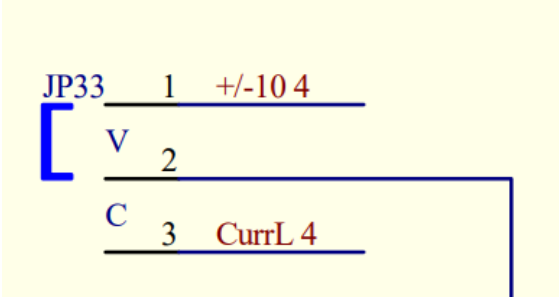

Figure 4-10: Central TB Analog Output mode selection [16]

4.3.1 Voltage Output

Figure 4-11 shows the inverting amplifier used in voltage mode analog output. The amplifier has a gain of -5, as well as an offset. The offset is present because the purpose of the circuit is to provide an output of -10V up to +10V. Since the DAC feeding the input of this circuit is only of a positive voltage (0V to 5V), and since this is an inverting amplifier, it needs an offset voltage to be able to provide positive side of the output range.

The offset voltage works by providing a reference voltage of 1.7V, which is precisely maintained by a separate voltage reference IC followed by a voltage follower circuit. This 1.7V is input to the positive terminal of the circuit, where the gain is that of a non-inverting amplifier, which in this case becomes a gain of 6. In essence, the output of the amplifier is set to $1.7V * 6 = 10.2V$ by default and is then pushed downward by the DAC as shown in equation 2. Now, if the DAC outputs 4.04V, this would bring the output all the way down to -10V, giving the circuit the full range of ±10 V.

$$V_O = 10.2V - V_I * 5 \quad (2)$$

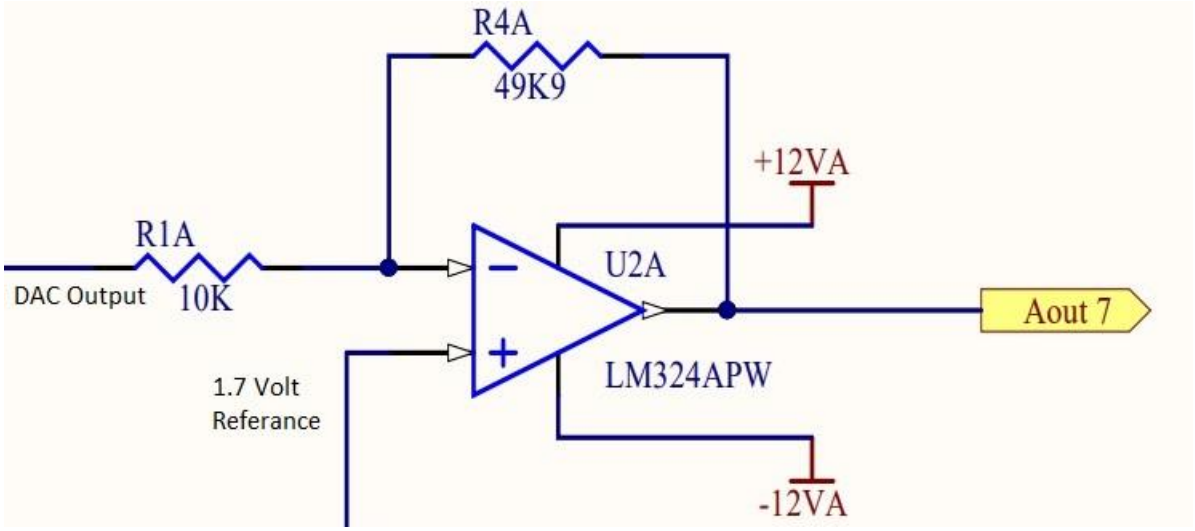

Figure 4-11: IOB-Mk2 Analog Voltage Output Amp [10]

All necessary components required for this circuit were available and possible to acquire, so this design was directly reused and adapted to the IOB-Mk3 Transit design.

4.3.2 Current Output

The current output is designed to be able to output 4mA to 20mA commanded from the same DAC output of 0V to 5V. The circuit design that is used in both IOB-Mk1 and IOB-Mk2 is shown in Figure 4-12. Firstly, notice the optocoupler which is labeled as U34D in this example. It has one function that does not affect the overall function of regulating the current output. The optocoupler acts as a status indicator for broken loop detection and will be discussed in 4.3.3.

The circuit that controls the current output requires a voltage source from the host product that will generate the current; the source is labeled in Figure 4-12 as “Out HI 7” and has been set to 12V for all its time in use, however raising the voltage does not affect the output. This will be demonstrated in the analysis.

The basic function of the circuit is that the operational amplifier operates the BJT transistor like a current valve, regulating the current through the output resistor R24. What happens is that the voltage from the DAC is directly applied as a voltage drop over the output resistor, which the current produced is divided between the circuits output and feedback. Interestingly, the negative feedback in this amplifier circuit utilizes the positive op-amp terminal. This works because the feedback current decreases as the voltage input increases, making the positive terminal function as a negative terminal.

All in all, the basic formula of the circuit for all practical uses is $I_O = \frac{V_I}{R_O} - I_{FB}$, where the feedback current can be ignored.

Looking at Figure 4-12 I name the following aspects of the circuit: Resistor R24 as output resistor R_O, Voltage source V_S, transistor collector voltage V_C, operational amplifier internal resistors R_i.

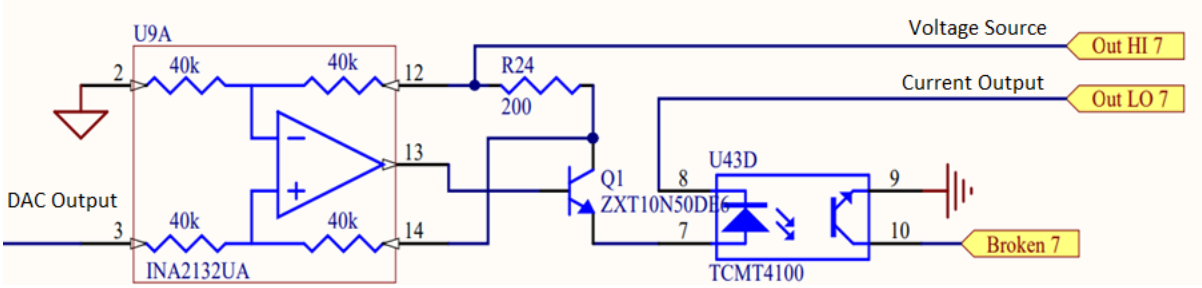

Figure 4-12: IOB-Mk2 Analog Current Output [10]

Before analyzing the circuit completely, it is useful to make some baseline observations. Firstly, V_S sees a voltage divider that is connected to the negative terminal of the operational amplifier; the voltage divider results in $\frac{V_S}{2}$ being present on both the negative and positive terminal. Secondly, the voltage drop over R_O is equal to $V_{Ro} = V_S - V_C$. Thirdly, the feedback current I_{FB} is defined as the current from the V_C node to the V_I node.

From that the analysis begins by approximating the feedback current as having no loss to the positive terminal and thus being equal though both internal resistors as shown in equation 3. Looking at the relationship of the voltage drop over both internal resistors, I simplify equation 3 to $V_S - V_C = V_I$. With this, observe that V_I has the same relationship as V_{Ro} and that they must be equal.

Lastly, see equation 4 as it lays out how the output relates to the input and how the I_{FB} component lessens as V_I is increased. Also, observe that the value of V_S is not relevant to the set voltage drop V_{Ro}, since is equates to and is only dependent by V_I.

$$I_{FB} = \frac{\frac{V_S}{2} - V_I}{R_i} = \frac{V_C - \frac{V_S}{2}}{R_i} \tag{3}$$

$$V_I = V_{Ro}$$

$$I_O = I_{Ro} - I_{FB}$$

$$I_O = \frac{V_I}{R_O} - \left(\frac{\frac{V_S}{2}}{R_i} - \frac{V_I}{R_i}\right) \tag{4}$$

This is a very clever circuit that has a very simple concept once broken down properly, and it was adopted directly to the IOB-Mk3 Transit, replacing only the operational amplifier as done with the rest of the INA2132UA's.

However, the current output circuit has a known problem when used to drive a shunt resistor with too high value. The circuit, while being used towards other company systems with a higher shunt resistor, locks itself in a hysteresis-like state while trying to reach the 20mA output level. The output is first unable to reach 20mA and then, after failing it freezes at the failure current until a much lower current value is commanded, releasing it from its hysteresis state.

This is thought to be mended if the voltage source used to drive the current loop is increased. In an idealized scenario with a 12V source and commanding an output of 20mA, the voltage over our shunt resistor is 4V, the broken loop detection diode has a forward voltage of 1.6V, leaving 6.4V to the external shunt resistor used to read the current. Thus, any external shunt resistor over 320Ω will cause an output freeze unless a higher voltage source is used.

4.3.3 Broken Loop Detection

The broken loop detection aspect relates to the analog current output section. As stated, the output ranges from 4mA to 20mA as valid values; in the case of a broken signal line, the current will be 0mA which is an invalid value. The IOB's solution within this format is using an optocoupler circuit shown as component U43D in Figure 4-12, to lower a flag when there is an active and intact loop, as any value of 4mA or above is enough current drive the internal LED (Light Emitting Diode) of the optocoupler. However, if the loop is broken then the LED will be inactive, raising the flag, signifying that there is a broken loop present.

Each analog output loop has their own flag, which is fed into the same parallel in serial out shift register (PISO) shown in Figure 4-13. The Shift register is then controlled and monitored by the MCU by having a clock line, a shift/load line and a serial data read line fed into it. The shift/load line is output from the MCU and determines if the shift register clock line input updates the broken loop status or if it shifts the currently held data out the data read line in a serial fashion for the MCU to receive. Each shift register is equipped with a serial input pin that can be connected to another register's data output to effectively add 8 bits of data to the total PISO structure. This linking of registers also requires that all registers share clock line and shift/load line.

This solution is also adopted to the IOB-Mk3 Transit board, with the small adjustment of reducing the number of linked shift registers down to two, due to there being fewer current outputs in the Mk3 iteration.

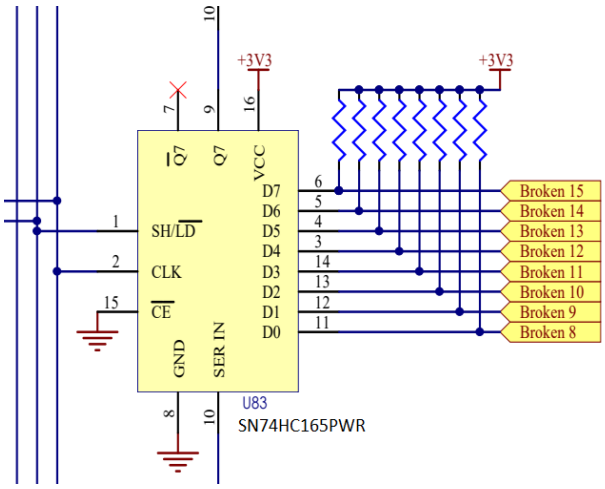

Figure 4-13: IOB-Mk2 Broken Loop Shift Register [10]

4.3.4 Isolated Analog Output

There are some applications for analog outputs that require that the analog output is galvanically isolated from the rest of the IOB. The IOB has four such outputs spread over two separate isolated regions. The 4 outputs are functionally the same as the standard analog outputs, meaning that the four outputs each have a current and a voltage modality.

The regions are isolated with use of the use of a power isolation component like DCP021212DU [17]. These take a 12V input and create galvanically isolated +12V, 0V and -12V on the output, with a 2W capability.

To communicate with the DAC, two optocouplers are used to inject the I2C bus to the DAC's and command them (Figure 4-14), with the drawback that the communication to the DAC is one directional. This solution was directly adopted to the Mk3-Transit board. However, there is a problem with this solution pertaining to the microcontroller as I2C the master instead of an FPGA, and this is discussed in chapter 5.

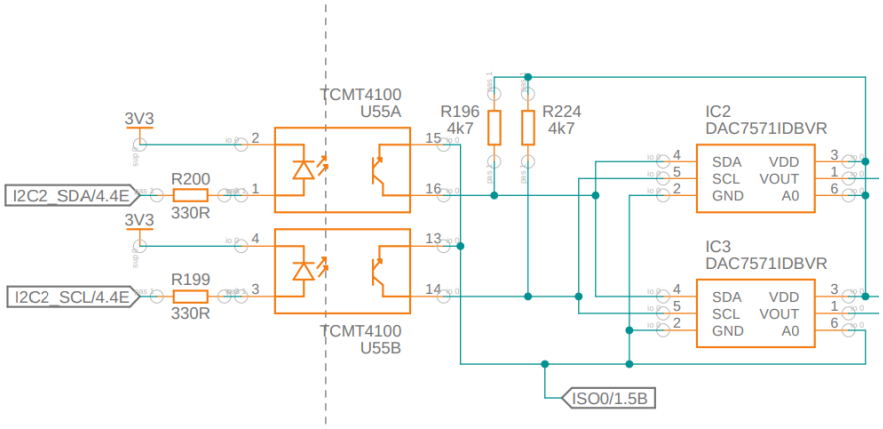

Figure 4-14: Isolated Analog I2C DAC input

4.4 Data Transmission

The IOB hosts three data bus types that are intended for external connectivity. These are two ethernet ports, eight receive-only RS-485/422 serial data inputs and four I2C buses. The ethernet is used to communicate with the rest of the Marine Technologies system environment, while the I2C is mostly used for controlling and retrieving commands from button panels that the IOB is equipped to. The receive-only serial communication is mainly for receiving and reporting external instrument data.

4.4.1 Ethernet

In this section I only explain the applied solution for the Mk3-Transit, as the Mk1 and Mk2 solutions were not relevant in this case. The first ethernet port is mounted directly on the Nucleo development board and the micro controller only has support for one RMII interface. The other ethernet port, mounted on the transit board directly is paired with a PHY chip uses SPI buss communication to interface with the microcontroller. The development boards PHY is dubbed “NET A” and the SPI based PHY located directly on the IOB-Mk3-Transit is dubbed “NET B”.

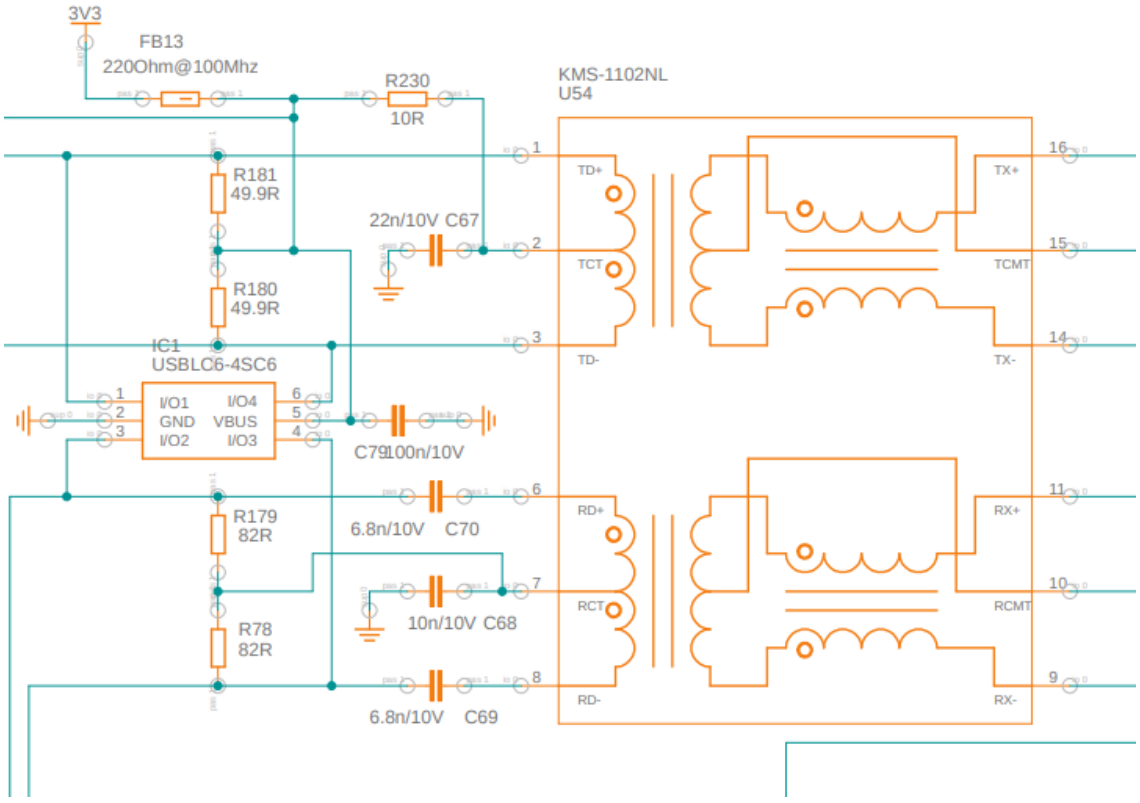

Figure 4-15: SPI Ethernet Magnetics

Ethernet ports must however have isolation and ESD (Electrostatic Discharge) protection, thus an ethernet magnetics component (U54) is connected along with a ESD protection component (IC1) as per Figure 4-15. This offers protection for the IOB in case of a critical failure on the ethernet cable that can damage the IOB.

4.4.2 Serial Inputs

The serial inputs are as stated purely inputs, and they follow the differential modality seen in RS-485 and RS-422. These, like all other signals going to external systems must be isolated, so they are optocoupled. The Mk1 and Mk2 board do this slightly differently.

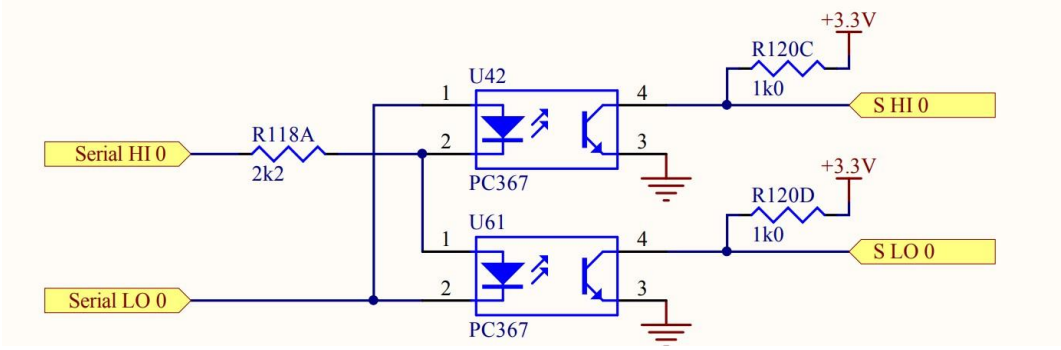

Figure 4-16: IOB-Mk1 Serial Input [12]

In the Mk1 board shown in Figure 4-16, two optocouplers are used to isolate the incoming RX signal. The signal is not inverted or anything of the sort, it is just passed on to the FPGA for processing.

The Mk2 board used a different approach, shown in Figure 4-17 to implement a differential to single ended conversion. This circuit converts the incoming RS-485/422 to pure UART format, considering that the incoming signals is inverted; an input of “Serial HI = 0” and “Serial LO = 1” translates to a UART signal “Serial In = 1”, and vice versa.

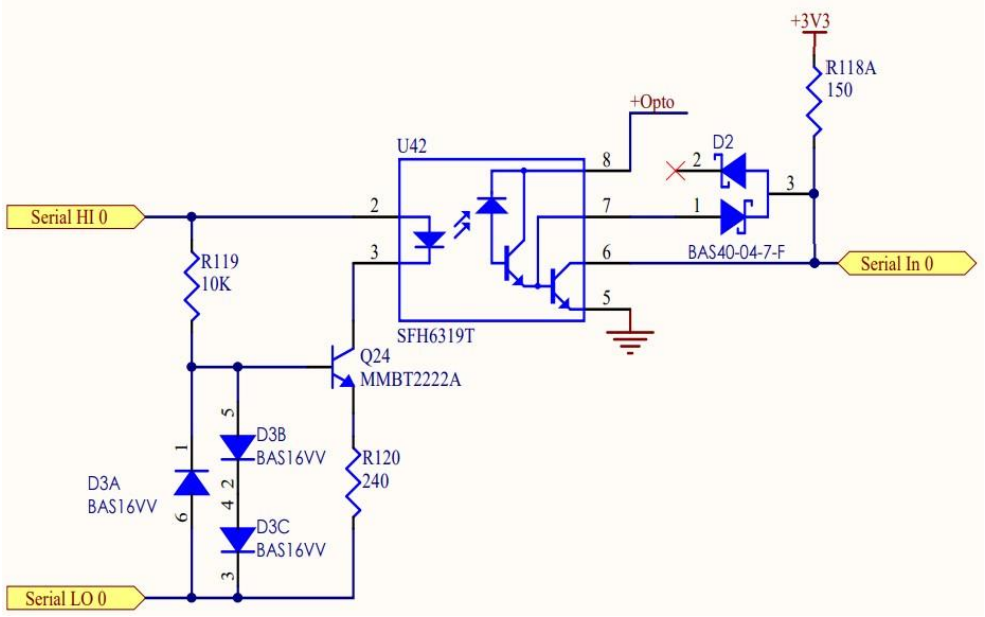

Figure 4-17: IOB-Mk2 Serial Input [10]

The tight pin restrictions on the microcontroller made the single wire data line solution much more desirable, and therefore the Mk2 solution was adopted. Regardless, also due to the microcontrollers pin availability, I had to make use of the extra LPUART (Low Power UART) on board the microcontroller chip to fulfil the requirement of 8 input channels. I also used the alternative single wire data UART function on the microcontroller that allows me to utilize the TX pins as RX for any given UART channel [3].

4.4.3 I2C

The I2C buses are very simple as I2C should be. There are four distinct buses, two of which are used partially by the isolated analog output region previously mentioned in this chapter. All four buses are made available on the IOBs board to board connectors; however, the I2C buses are still only intended for the boards that are directly connected to the IOB, not external systems, and therefore they do not require galvanic isolation.

The Mk2 board featured I2C repeater components that appeared to have little effect on the signal and performance quality of the I2C buses, so I chose to revert to the Mk1 implementation (Figure 4-18). This is a simple combination of a 3.3V pullup with a ferrite component for noise reduction.

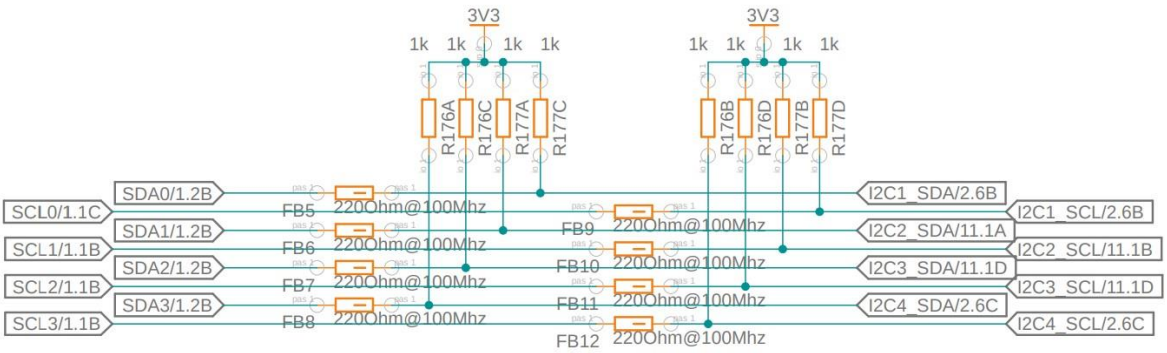

Figure 4-18: Mk3 I2C Implementation

4.5 Nucleo Modification

The Nucleo development board for the STM32H743ZIT6 microcontroller that is mounted on and completing the IOB-Mk3-Transit board, cannot be mounted on as is. Certain modifications must be made to it for it to function properly. These modifications are standard modifications that the Nucleo intends a user to be able to perform by adding or cutting specific solder-bridges [4]. There are also jumper straps on the board that must be set in specific positions. A full overview of the necessary configuration is listed in Table 4-1.

Table 4-1: Nucleo Modification Table

Solder-bridge or Jumper	**Action**	**Reason**
SB14	Add	Gain access to pin PD0
SB15	Add	Gain access to pin PD1
SB23	Cut	Disconnect pin PA9 from USB power monitoring.
SB44	Add	Gain access to pin PH1
SB76	Cut	Disconnect pin PG7 from USB overcurrent monitor
SB77	Cut	Disconnect pin PD10 from USB power enable
JP1	Not connected	This allowed the ST-Link chip to be active
JP2	EXT setting	Nucleo board power source selection. Select external 5V source
JP3	Connected	This in the NRST pin
JP4	Connected	Microcontroller current intake
JP5	VDD -> 3V3	Supply microcontroller with 3.3V
JP6	Connected	Ethernet data to microcontroller

4.6 Power Distribution

The IOB needs a host of different voltages to function, as well as a separate analog region to separate the analog signals from the noisy digital activity. Some organization is necessary to make sure these voltages are treated properly, apart from choosing components that make these voltages available. Power distribution relating to component choice and circuit diagrams will be discussed in this section, while distribution pertaining to PCB layout will be covered in the next section. This section will also only cover the solutions that were applied to the Mk3 Transit board, despite being like previous IOB iterations.

The IOB receives power from a 24V net that is supplied by the ship. The IOB has a DC/DC converter that galvanically isolates the IOB from the vessel. The DC/DC converter is a wide input device that receives 9V to 36V and converts it to 12V; the 12V output is what is used to power and attain all other voltages used onboard the IOB.

The voltages needed are: 12V, 5V, 3.3V, +12V analog, -12V analog and 5V analog.

4.6.1 Digital Power Distribution

The 12V received from the DC/DC converter is broken down on the digital side into a 3.3V net and a 5V net by using the TPS54394RSAR from Texas instruments. This is a dual output switch mode voltage regulator that can provide as much as 3A at both channels.

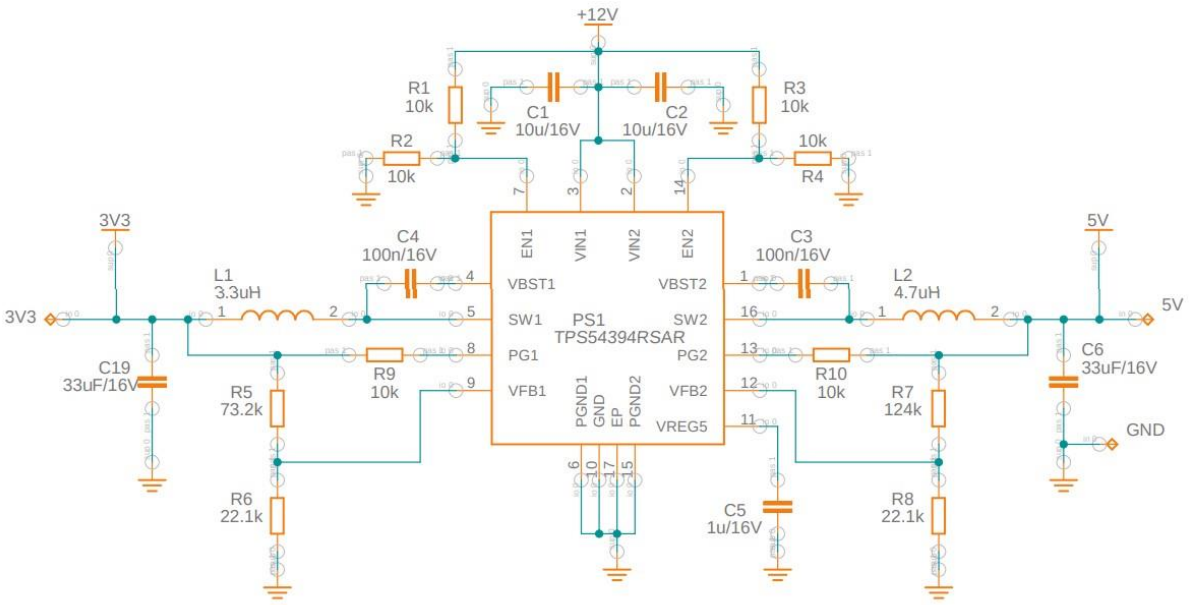

Figure 4-19: Mk3-Transit 3.3V and 5V regulator

4.6.2 Analog Power Distribution

The analog voltages are filtered versions of the digital voltages by use of ferrite beads, capacitors, and inductors. Both +12VA and 5VA are supplied this way, while the analog ground connection is just made by a ferrite bead (Figure 4-20).

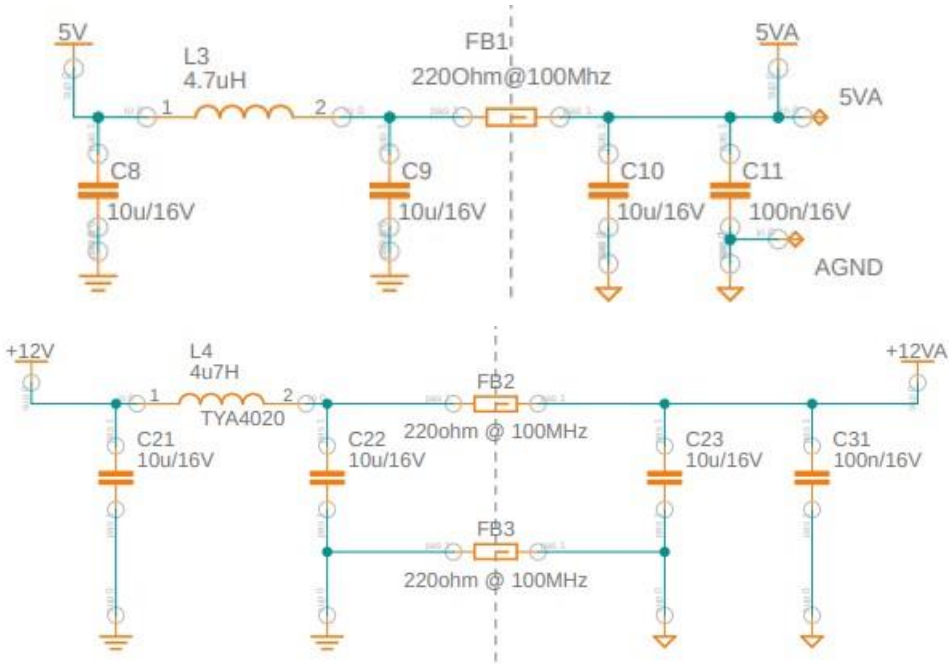

Figure 4-20: Analog Power Filtering

The -12VA is however and is made by the LT1931AES5#TRMPBF by Linear Technology. This circuit is a switching and inverting DCDC converter that is 12V in and -12V out. The circuit layout is very unforgiving and EMC performance is reduced drastically if designed incorrectly, so be sure to follow the layout guidelines carefully (Figure 4-21). After the -12V is generated, is filtered into the analog area the same way the other analog voltages are in Figure 4-20.

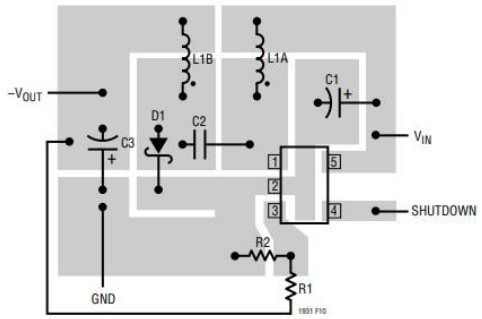

Figure 4-21: Negative 12V Converter Layout [18]

4.6.3 ±10V Reference

External levers and potentiometers require stable +10V and -10V references. These two 10V values are derived from a 2.5V voltage reference component that is fed into an operational amplifier that produces the +10V reference. That +10V is then fed into another operational amplifier to invert it into the -10V reference.

4.7 PCB Layout

The PCB has an 8-layer structure where the ground plane is present in the top layer and bottom layer, acting as a shielding for the PCB. Power distribution polygons are placed starting from layer 2 and continuing down the different layers as needed. Signal traces were used in every layer as needed around these power planes.

Table 4-2: IOB-Mk3 Transit PCB Layer Stack Assignment

Top Layer	Power plane (Ground)
Layer 2	Power plane (3.3V)
Layer 3	Signal plane (with 12V polygon)
Layer 4	Signal plane (with +12VA polygon)
Layer 5	Signal plane (with -12VA polygon)
Layer 6	Signal plane
Layer 7	Signal plane
Bottom Layer	Power plane (Ground)

This structure referred to in Table 4-2 is not recommended as it poses significant EMC difficulties. The lack of solid and unsplit polygons and dedicated power planes that cover the whole plane and dedicated signal planes makes this board difficult to certify, as will be apparent in chapter 5. All these issues are addressed and fixed in chapter 6, where proper EMC etiquette was considered in the layout of the IOB-Mk3.

The top and bottom layer is split into two regions, these are the digital ground polygon and the analog ground polygon regions. The main surface level routing between most adjacent components mounted on the PCB is done on this layer and this is the reason for much of the difficulty caused in the EMC performance. Since not only vias, but also component SMD pads and actual routing traces deform the polygon and break its continuity, causing return currents to travel other convoluted routes in the copper.

5 Test and Verification

Testing the IOB-Mk3-Transit board was done in three main steps: (1) Testing physical dimensions and Power distribution voltages, (2) testing all the functionality of the IOB-Mk3-transit, and finally (3) performing the EMC and environmental tests. Most of the EMC and environmental tests were performed in a licensed laboratory in Italy where the IOB-Mk3-Transit was eventually certified for maritime use.

Figure 5-1 shows the tool used for monitoring the states of the analog and digital inputs, commanding the analog and digital outputs, and reviewing serial input data is called “MT IO Test tool”. It was made by Marine Technologies for the purpose of testing the IOB series cards and is therefore the tool I used while testing.

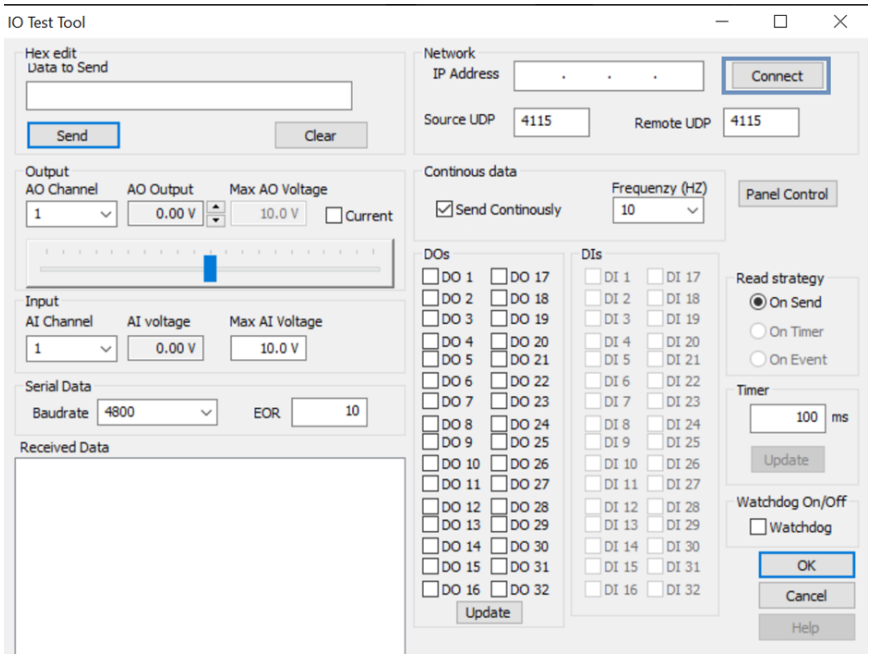

Figure 5-1: MT IO Test tool

It should be noted that the microcontrollers’ software is designed to match the Marine Technologies requirements for the IOB-Mk3-Transit board, and it is not my work. However, the designer of the software and I cooperated in the effort of making the code operational. We sifted through the different IC’s datasheets, making sure that the microcontroller issued the correct commands to the respective components, as well as troubleshot when a system was not responding correctly.

Table 5-1 contains the varying tests that have been performed in the process of getting the IOB-Mk3-Transit operational and certified. Some of these tests are simple measurements that verify expected voltage measurements or functions. These tests are marked with a ‘*’ and if passed successfully they are not discussed further in the thesis.

Table 5-1: Testing and Verification Overview

What is tested	What is tested for	How it is tested
PCB build and voltage bias		
Visual inspection*	Misplaces components and manufacture faults	Visual inspection under magnifying lens and checking mounting dimensions
Power distribution*	Are all supply voltages correct	Probe various test points with multimeter: 3.3V, 5V, +12V, +12VA, -12VA, 5VA
Voltage references	Are all voltage references holding desired value	Probe various test points with multimeter: 1.7V, 2.3V, ±10V
PCB functionality		
Ethernet connectivity	Check network A and Network B port connectivity	Connect to computer by ethernet cable and establish contact with the IOB with MT IO testing tool
Serial input connectivity*	Check every serial input for functionality	Transmit data into the serial port and read data in the MT IO testing tool serial data terminal
Analog input	Any deviation from expected values along the first and second analog stage	Probe the various stage inputs and stage outputs with a multimeter
	Are the values correctly interpreted by ADC	Check Analog input values transmitted to MT IO testing tool
Isolated analog output	Isolated voltages	Probe various test points with multimeter: -12Viso, 0Viso, +12Viso
	Check I2C DAC function	Loop analog output to an analog input to check for correct value in MT IO testing tool
	Does the voltage output produce the desired values	
	Does the current output produce the desired values	
Analog output*	Does the analog voltage output produce desired values	Loop analog output to an analog input to check for correct value in MT IO testing tool
	Does the analog current output produce the desired values	
Broken Loop Detection	Observing if the shift registers are outputting the correct data.	Use oscilloscope to observe and check the shift register output
Digital Inputs	Can the digital input be interacted with, and what is the trigger resistance	Ground the input and see if it registers as a trigger in MT IO testing tool

What is tested	What is tested for	How it is tested
Digital outputs*	Can the digital output be toggled	Toggle the digital output in MT IO testing tool while mounted to Central-TB. Listen for an activated relay
Watchdog Circuit	Watchdog output state and ability to toggle digital output	Establish connection with MT IO testing tool to activate the watchdog circuit, listen for Central TB relay
Environmental testing and EMC		
EMC Pre-testing	Radiated emissions	EMC tests performed in advance of verification process. Performed in an EMC chamber in Norway
EMC Certification	Radiated	EMC chamber with the EUT on a rotating platform, with antenna aimed at it
	Conducted	EMC chamber with frequency analysis monitoring noise activity on 24V supply wires
Temperature test	Investigate Analog Input and output performance issue	Establish an analog Input output loop. Heat up PCB with a heat gun to provoke the fault and probe voltages

5.1 PCB Build and Voltage Bias

Visual and mechanical checks were made to the board to check for manufacturing faults. The Nucleo development board was mounted on the IOB-Mk3-Transit and the completed IOB was mounted on a Central-TB to check for mechanical design faults. After this was verified to be in order, the board was powered up while looking out for severe electrical failure (Smoke test).

Thereafter I performed a voltage probing sweep with a multimeter, looking for all the expected voltage values. All power distribution voltages both analog and digital, and all voltage reference outputs. Only the reference voltages displayed faults. After all the discovered faults were diagnosed and amended, uploading software to the development board could proceed so that the board's peripheral functionality could be tested.

5.1.1 Voltage References

Measuring of the voltages on the reference outputs showed unexpected values at both U48 and U3, which are the op-amp based voltage followers used to secure a stable voltage. Discovering this, I checked the voltage on the input voltage divider and read an unexpected value there as well. After confirming that the 4.1V voltage reference itself was outputting the correct value, I discovered that

the voltage divider had a resistor with a value 1000 times smaller than it was intended to be (49.9Ω instead of 49.9kΩ). This was a misunderstanding of the Bill of Materials issued to the manufacturers.

Unfortunately, after discovering this issue, and soldering an approximately correct resistor (47kΩ), the issue persisted. The voltage follower output was still incorrect. The ultimate fault was in my design, being that the footprint of the op-amp component was of a version of the op-amp that was not available. The op-amp in question had two pinouts for the same SOT-23 package, and I had chosen the one not made available.

The solution for this was to painstakingly lift the incorrect pins from the SMD pads with a soldering iron and a sewing needle and use small copper wire to correctly route the signal to its proper SMD pad. After completing this modification, the area is covered with non-conductive RTV (Room Temperature Vulcanizing) silicone to seal, isolate and secure the modification. The same faults and fixes are applied to both components U3 and U48.

The second Voltage reference fault was discovered to be in the +10V and -10V reference outputs, as the OP-amps were not outputting the expected output of +10V and -10V. Starting by measuring the voltage output of the 2.5V reference that maintains the op-amps output, I found that the output was way too low. Reading the datasheet of the voltage reference in question, I discovered that I had forgotten to place the 10µF output capacitor required for the 2.5V voltage reference to function properly. Adding this capacitor and sealing the modification with RTV fixed the issue entirely.

5.2 Functional Verification

The whole process of function verification was done along with my colleague in software development. When a functional fault was found, I was contacted, and hardware and software diagnosis was performed in tandem with each other.

5.2.1 Ethernet Connectivity

Testing of the ethernet function relies on whether contact can be established with the microcontroller through the ethernet port. Both the Net A and Net B port must be able to be used to contact and send valid values to the MT IO testing tool.

Also, it is a requirement to maintain contact with the IOB with both ports in use simultaneously. Additionally, removing one of the ethernet cables must not affect the traffic flow on the other network port, obtaining network redundancy.

There was one issue that was discovered, diagnosed, and amended at a later point. Communications from the SPI PHY of NET B would cease, and the port would become undiscoverable by computers. This was due to an EMC issue caused by a false copy of the 24V to 12V DCDC converter onboard the IOB-Mk3-Transit board. Fixing the EMC issue also fixed the network issue. The amendment of the EMC issue will be discussed in section 5.3.2.

5.2.2 Analog Inputs

Analog loop tests were conducted, which consisted of taking an analog output (AO) and looping it to an analog input (AI) and then commanding the AO with the MT IO testing tool reading the value reported by the IOB to the MT IO testing tool. Voltage and current measurements were made simultaneously with a multimeter in to confirm the voltages commanded and reported.

At the start of these tests, it became clear that the AO was functioning perfectly, but the AI was not. The problem was the MT IO testing tool reported all AI voltages across every AI input to be 0V, no matter the voltage applied to the input. Probing the card revealed that the input of each ADC channel pin was indeed pulled low, to 0V.

The frustrating cause of this problem was a capacitor component that I used that seemed to be consistently faulty. The capacitor component in question is an 8-pin component called a “Capacitor-array” component, that combines four equally matched capacitors next to each other, saving space and acquiring consistency.

Unfortunately, the capacitor-array that I received shorted everything to ground. Every single ADC input was connected to every other ADC input, as well as ground. Removing the capacitor-arrays fixed the issue entirely.

After amending the analog inputs reading capability, it was decided that the measurement resolution, both current modality and voltage modality, were both satisfactory on the same DIP switch setting. These switches are deemed unnecessary, and the circuit will be redesigned with the ON configuration hard wired in the circuit.

5.2.3 Isolated Analog Outputs

The isolated analog outputs did not respond during testing. Seeing as they share identical outputting amplifier structure, the DAC was immediately put into question. The DAC in the isolated AO region is an I2C based DAC that is connected to its I2C bus via optocouplers to maintain isolation with the rest of the board. This revealed itself to be a mistake and rendered the isolated analog region useless.

In the IOB-Mk1 and IOB-Mk2, the same solution shown in Figure 4-14 is used to communicate with the DACs, having them behind a one-way transmission of the I2C bus. This is only doable, because the FPGA used in the Mk1 and Mk2 was likely configured to ignore the need of an “acknowledgement” signal from the DAC. However, since the microcontroller cannot simply be programmed to ignore the absence of the DAC’s “acknowledgement” signal, the microcontroller ceases the command action, and the DAC is never properly given a value to output.

This was confirmed in testing by removing the isolating DCDC converter, connecting the power distribution of the isolated region with the rest of the board and bypassing the optocouplers with copper wire, making the communication with the DAC bi-directional. After applying these changes, communication was established, and we could command the Isolated AOs with an added bonus of having tested I2C functionality.

However, since this solution removes the “Isolated” quality of these outputs, the regions effectively become useless since isolation was the whole point of these outputs. As this functionality is not

necessary for all applications of the IOB, the IOB-Mk3-Transit can still be used in other applications. Additionally, the issues encountered in this test were addressed at a later point and a new solution is implemented in chapter 6.

5.2.4 Broken Loop Detection

Testing of the broken loop detection shift registers was done by connecting certain current loops and then commanding the current output up above 4mA, which is the lowest valid current of a current based signal. The parallel inputs of the shift registers are then checked to see if all the expected input values are present. Moving on, the shift register is commanded to shift all values out its serial output, where we were monitoring with an oscilloscope to view the output data.

Monitoring the output serial line shows a fault that was due to choosing a wrong version of the shift register. There are two shift registers in the IOB-Mk3-Transit, one linking its output to the next register and then the total output is given to the microcontroller. There is a passive version of the shift register, where the output has a pull-down state, and a high impedance state, a more passive output. The intentions were to use the other version that can command the output both to a high voltage state and a low voltage state, a more active output.

Note that the passive output component is present on the board, the modification solution was just to solder a pullup on to the outputs of the shift registers, and we could successfully read the broken loop states.

5.2.5 Watchdog

At first when powering the board, one of the first issues noticed was that the watchdog-controlled relays were nonfunctioning, the watchdog relay onboard was not activating. Testing proceeded by testing the timer circuit responsible for the original watchdog signal, then logically following that signal measuring for expected values along its path.

During these measurements, a missing wire trace was discovered, and reviewing the design schematics and layout files revealed a spelling error in naming the wire, resulting in it not being connected. Luckily, the missing trace is only 3cm long and soldering a small wire resolves this issue.

5.3 EMC and Certification

EMC testing is the most crucial and difficult step in the certification process. It is either a hit or miss, and it can quickly become a hassle if it turns out that there are EMC problems. Even more reason to properly check the EMC related design guidelines before producing boards that you know are going to go through a crucial EMC test. After I knew what we had in term of board functionality, we started testing radiated emissions in a local EMC chamber to get an idea of what was waiting for us in the actual certification Lab in Italy.

In the end the tests were passed, and the board was ultimately certified with a detailed report documenting the tests performed. This process took two attempts in Italy and a great deal of work at

home in preparation for the different attempts. One thing that made this process more difficult than usual was the fact that the certification lab had just gotten word of a tightening of the demands. Previously, the requirement for a compliant device was that it had its max noise EMI peak below a certain value specified in the requirements manuals. However, now the specific lab's uncertainty must now be considered, giving the compliance cases shown in Figure 5-2. This effectively increases the difficulty by adding another 6dBµV that we need to stay below to our requirements.

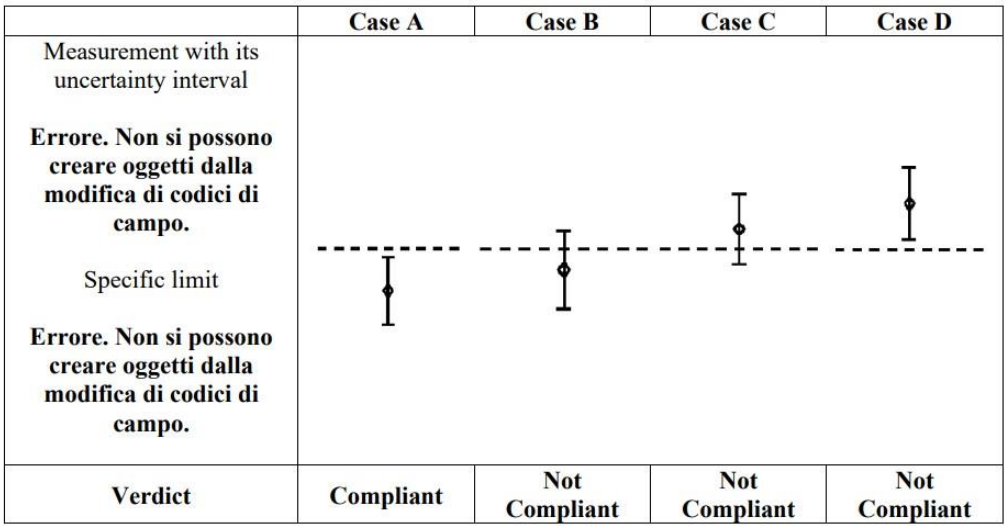

Figure 5-2: Certification EMC Margin Requirement [19]

The following figures Figure 5-3 and Figure 5-4 show the different Test setups in the EMC chamber at the certification lab in Italy. All the tests were performed in a building which has large inductors and capacitors filtering noise from the outside power grid. Additionally, the chamber used to measure the device is a faraday cage, further isolating the device from the outside EM signals. And finally, the inside of the chamber is made anechoic with absorbers designed to absorb the EM signals that hit the walls, so that reflections and echoes are not included in the measurements. All this ensures that the test readings are only of the device under test itself and nothing else.

Note that the different frequency range tests feature different antennas to capture that frequency range; two of the other radiated emissions test setups can be seen in the appendix. Also be aware that the table that the device under test is placed on, is rotated 360 degrees to measure all angles of radiation, as well as the antennas shift between horizontal position to vertical, to take radiation polarization into account. All tests throughout the whole rapport are performed while monitoring performance, checking if the performance is degraded in any way.

Figure 5-3: Test Setup Conducted Emissions [19]

Figure 5-4: Test setup Radiated (30MHz-1000MHz) [19]

5.3.1 Radiated Emissions Testing: Westcontrol

These tests covered only radiated emissions, and only on one specific angle, in contrast to in the certification lab, where the device is rotated 360 degrees. A rough estimate of what awaits is the only thing needed in this phase. Figure 5-5 shows the first test of the IOB-Mk3-Transit as it is with no EMC based modifications. It shows the emergency communications band of 156-165MHz which has a stricter criterion, seen by the red line that drops in that frequency range. The test did indicate that there was going to be a challenge already and that additional filtering and damping of the IOB was going to be necessary.

This is also seen by in Figure 5-6, as it shows the activity when the SPI based network PHY was being used to communicate with the MT IO testing tool.

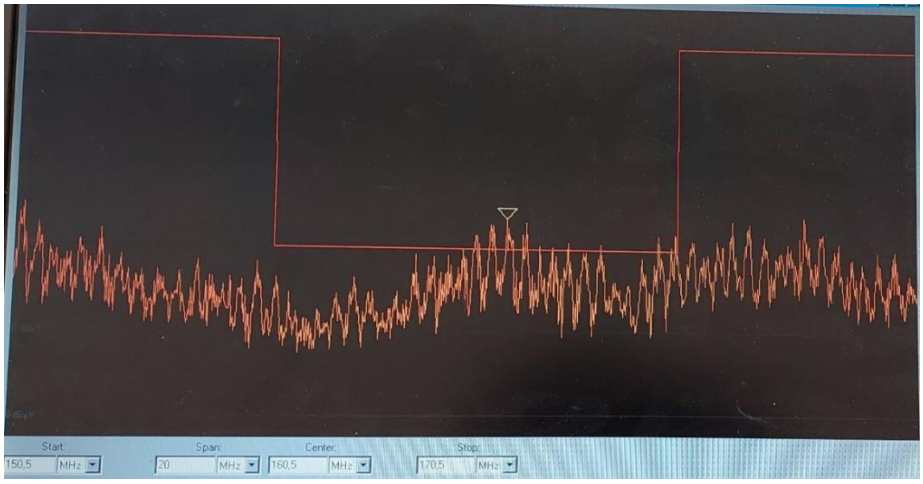

Figure 5-5: Initial Radiated EMI test at West Control (156-165MHz)

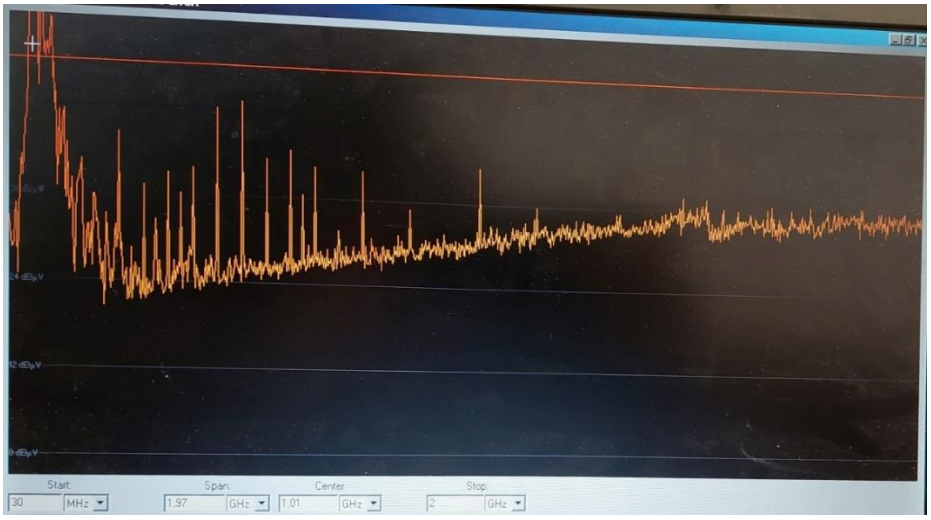

Figure 5-6: Initial Radiated EMI test at West Control (30MHz-2GHz)

By process of trial and error, many input filters of different variety and values were tested. Surprisingly, the one single component that seemed to work the best was a ferrite bead component with a center tap pin. The ferrite bead was connected in parallel to the 24V input positive lead and center tapped to the IOBs chassis connection. The result of this unusual method is shown in Figure 5-7, with a clear improvement over the results in Figure 5-5. Although it was not enough to pass, it was a good starting point.

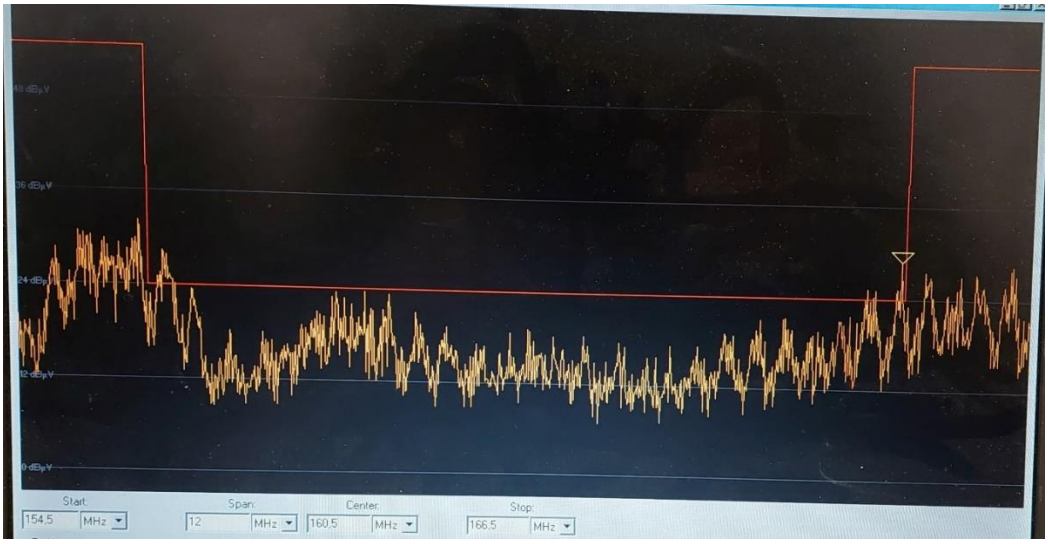

Figure 5-7: Initial Radiated EMI test at West Control (156-165MHz) with input ferrite

5.3.2 First Attempt EMC Certification

Performing these tests in the first attempt of certifying the board, we were able to pass the conducted emissions segment, until the lab was notified that the stricter criteria of taking lab margins into account. The radiated emissions tests were never passed at any point, although we did get somewhat close with many different input filters, experimenting with different values and mainly looking at PI-filter designs, common mode chokes with input and output bypass capacitors.

In the first attempt, three days were spent in Livorno trying to solve the EMC issue. Figure 5-8 and Figure 5-9 show results of the radiated emission tests early in the process of the first day, where we had problems in the lower frequency band and the emergency frequency band that we could not tame. The red line represents the required noise level that the IOB must stay under.

If you pay attention to the red line in Figure 5-8, starting from the left it slopes downward and then shoots up a little, and the yellow measurement follows this. The instrument used in the certification lab to measure the EMI is called a “Measuring Receiver”, and the measuring receiver uses different receiver bandwidths for the different frequency areas. With a wider receiver bandwidth, more energy is received by the analyzer in that range, and this can be seen visibly in the measurement.

The requirements document specifies what receiver bandwidth to use for each frequency range. For example, in Figure 5-8, the receiver bandwidth in the initial slope is 200Hz and is turned up to 9kHz after the spike on the red line. You can clearly see the effect of the increase of receiver bandwidth on the input signal, that it rises accordingly.

Figure 5-8: Conducted Emissions Failure (10KHz-30MHz)

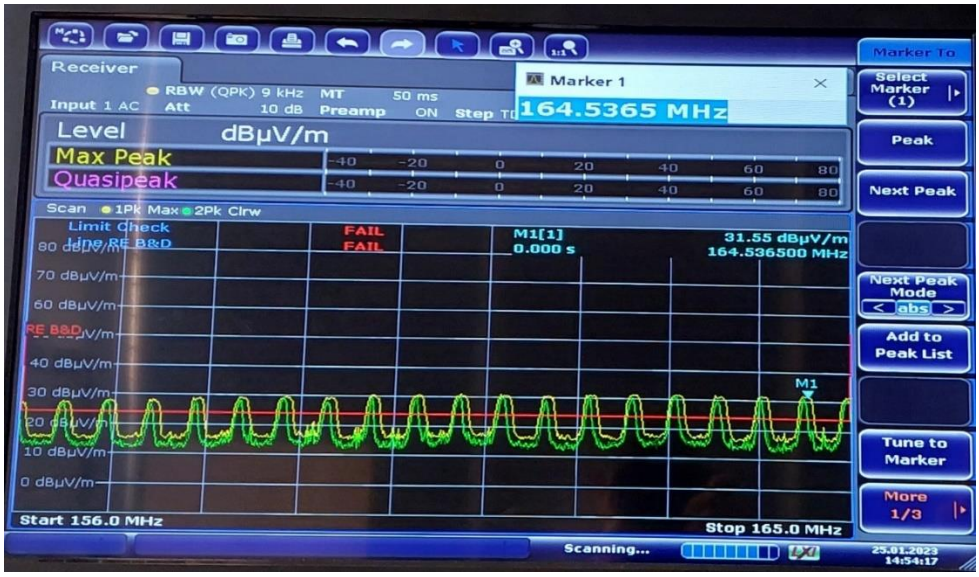

Figure 5-9: Radiated Emissions Failure (156MHz-165MHz)

5.3.3 Test Using Spectrum Analyzer at Marine Technologies

During the tests in Italy, there was suspicion that the DCDC converter was overly noisy and perhaps a false copy of the original product. To test this suspicion, the DCDC converter was powered up and the EMI was viewed with a spectrum analyzer. We also have access to the guaranteed original component, so we ran a direct comparison of their "EMI profile".

What was found when zooming in and measuring the wave tops of the EMI, was the switching frequency of the DCDC converters. And they were noticeably different, with the original component operating at a 330KHz switching frequency as stated in the component's datasheet, while the suspected false copy operated at 420KHz. Some quick emails with the manufacturer of the original part confirmed our suspicion and the DCDC converter was replaced with an original part.

Continuing the use of the spectrum analyzer, we performed a series of tests where a quarter wavelength antenna was fashioned from a single wire of around 45cm length and connected to the coaxial input of the instrument. The antenna was fastened alongside the ethernet cable used to connect to the IOB-Mk3-Transit. Noise present on a board can easily find ways to use connected cables to radiate out from, and therefore measuring the ethernet cable closely can give a better overall picture than a small local EM field probe can.

Figure 5-10 shows a background reference measurement, so that the ambient room interference can be taken into account. In Figure 5-11 the IOB is powered and communicated with, while using the new DCDC power unit. In Figure 5-12, a 6.8mH common choke with 100nF bypass capacitors is used as an input filter. Although the difference is slight between the filtered and non-filtered, the filtered measurement does display some amount of attenuation. Of all filters tested, this gave the best result, considering the noisy conditions we tested in.

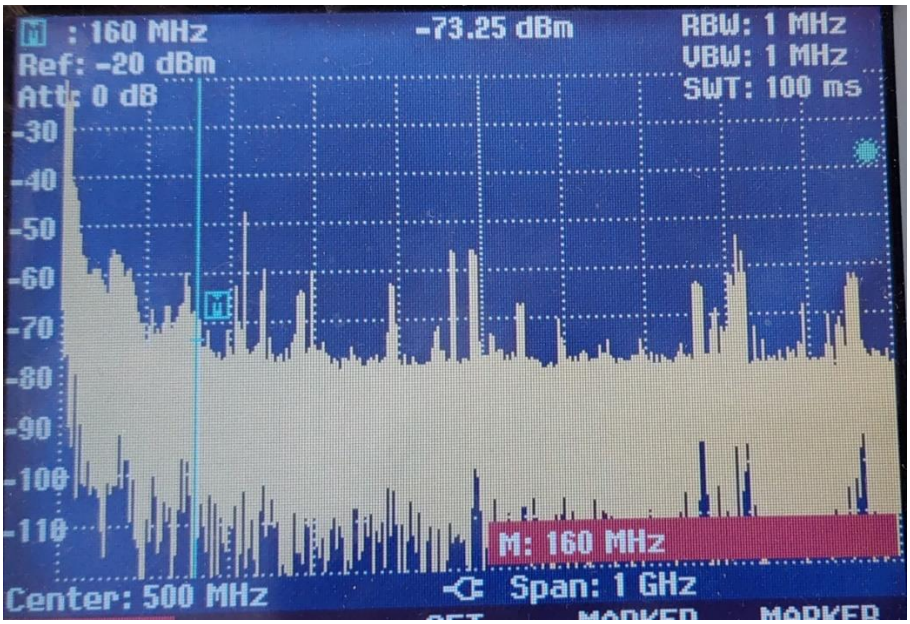

Figure 5-10: Background Measurement

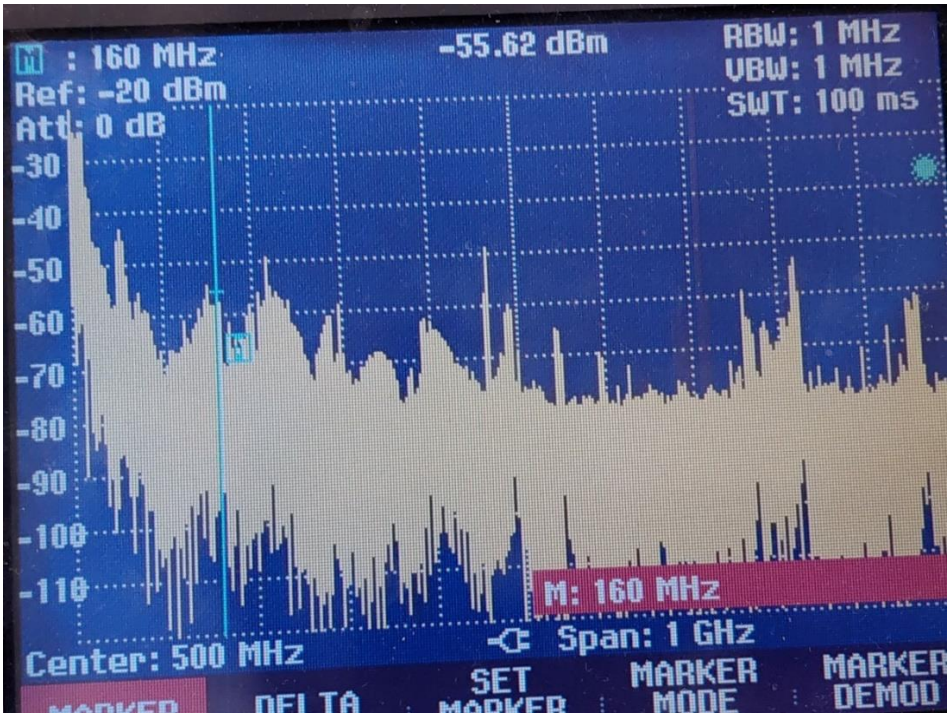

Figure 5-11: No Change Measurement

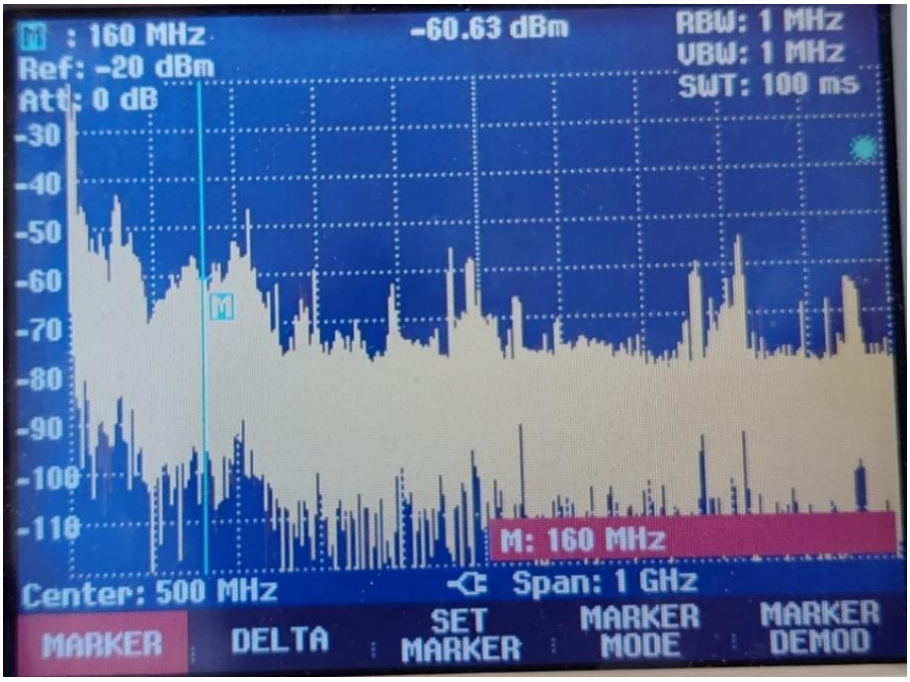

Figure 5-12: 6.8mH Choke PI Filter with New DCDC Power

5.3.4 Second Attempt EMC Verification

During the second attempt after some trial and error, an input filter was made containing three stages of common mode choke filters around the DCDC 12V converter to cover a wide area of frequencies. Two filters on the input side and one on the output side.

The input side of the DCDC converter has a first stage with a 2.2mH common-mode choke and 10pF bypass capacitors and a second stage with a 6.8mH common-mode choke with 100nF bypass capacitors. The output of the DCDC converter has a 6.8mH common-mode choke with 100nF bypass capacitors. With this filter, both conducted emissions and all radiated emissions tests were passed with acceptable margins. The graphs of Figure 5-13 to Figure 5-17 show the results of the report measured from the worst-case angle of each measurement category. All these graphs show successful results that passed the requirements.

Note that in Figure 5-16, the red line and input signal suddenly drops due to the receiving bandwidth being tuned down to 9kHz over the 156-165MHz range, while the rest of that measurement uses 120kHz as the receiving bandwidth.

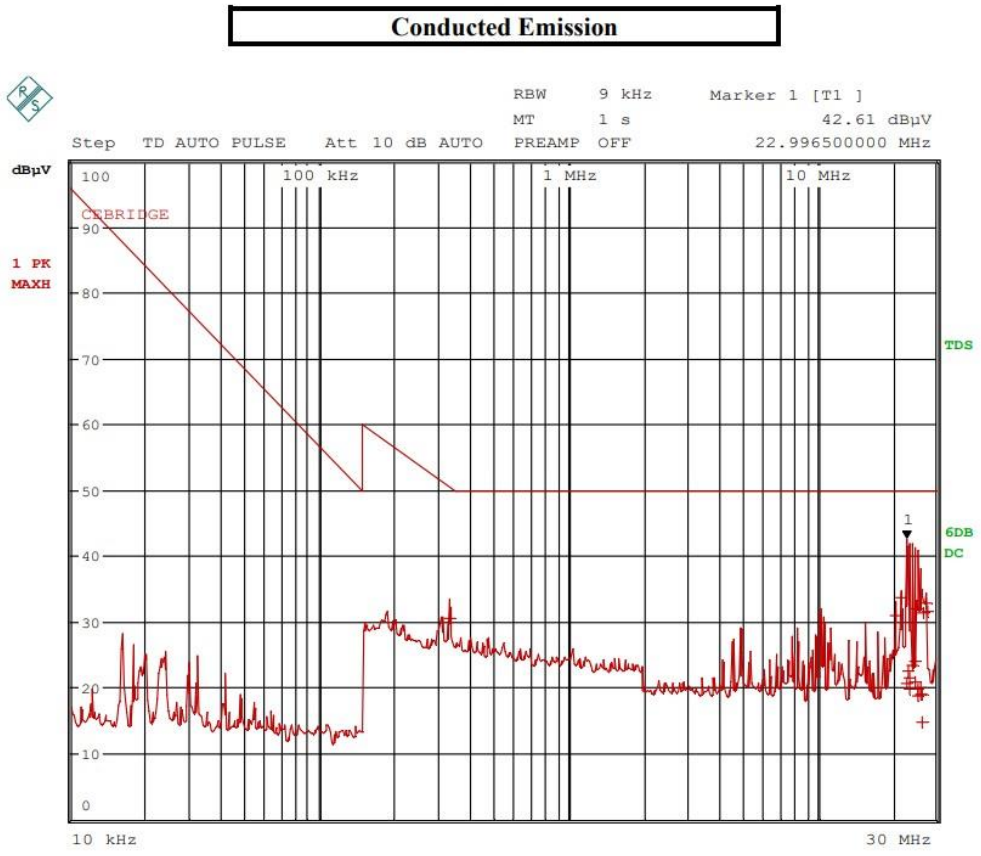

Figure 5-13: Passed Conducted (10KHz-30MHz) [19]

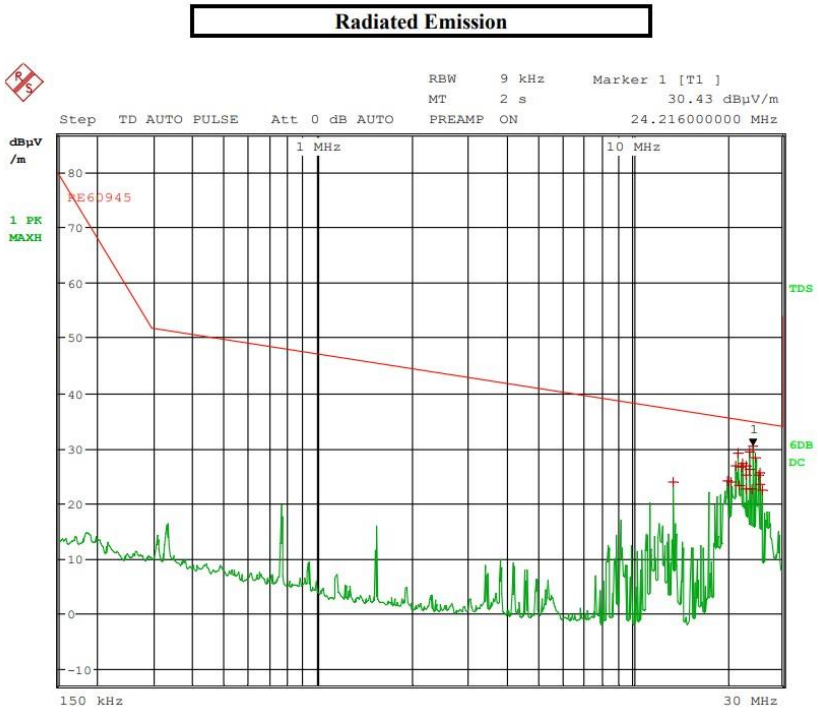

Figure 5-14:Passed Radiated (150KHz-30MHz) [19]

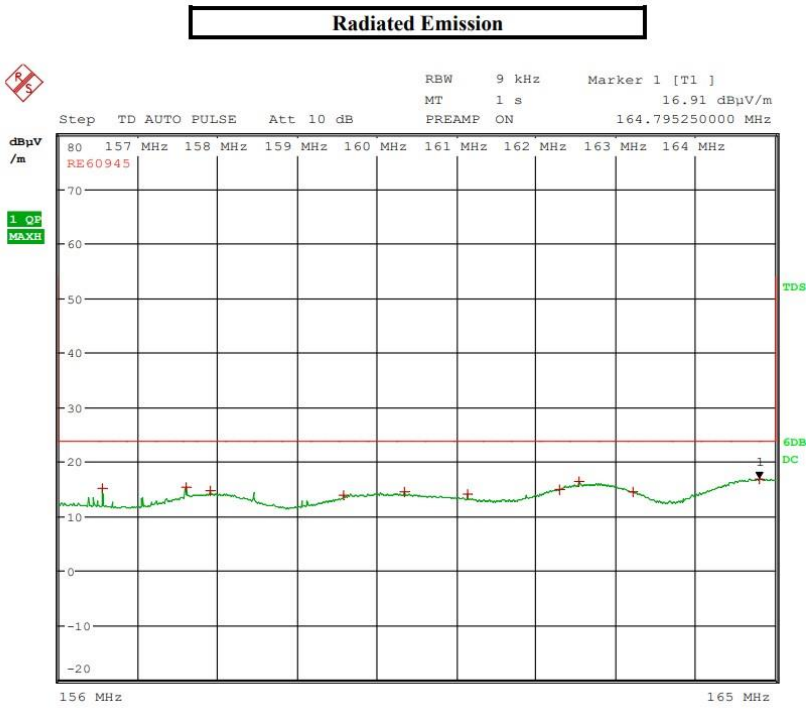

Figure 5-15: Passed Radiated (156-165MHz) [19]

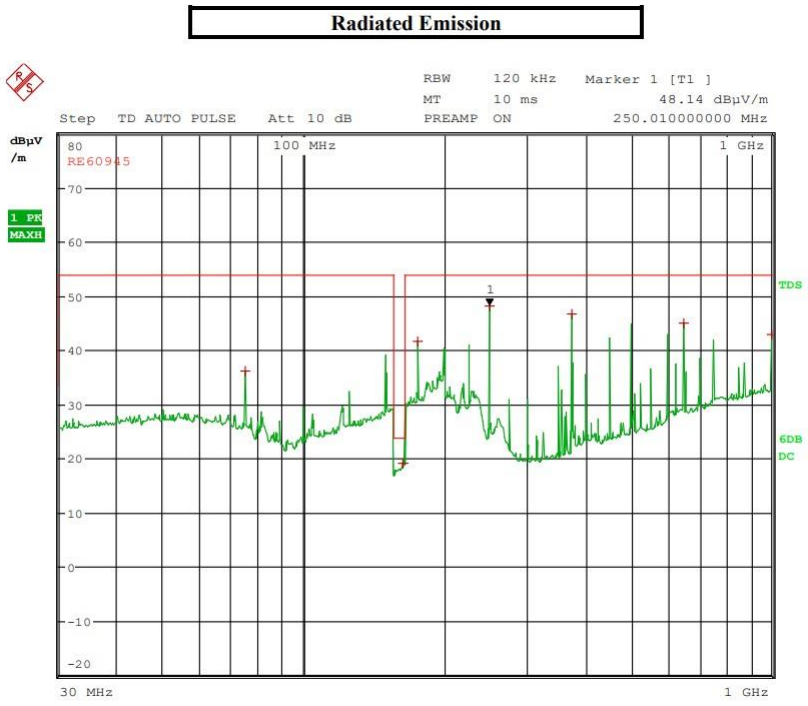

Figure 5-16: Passed Radiated (30MHz-1GHz) [19]

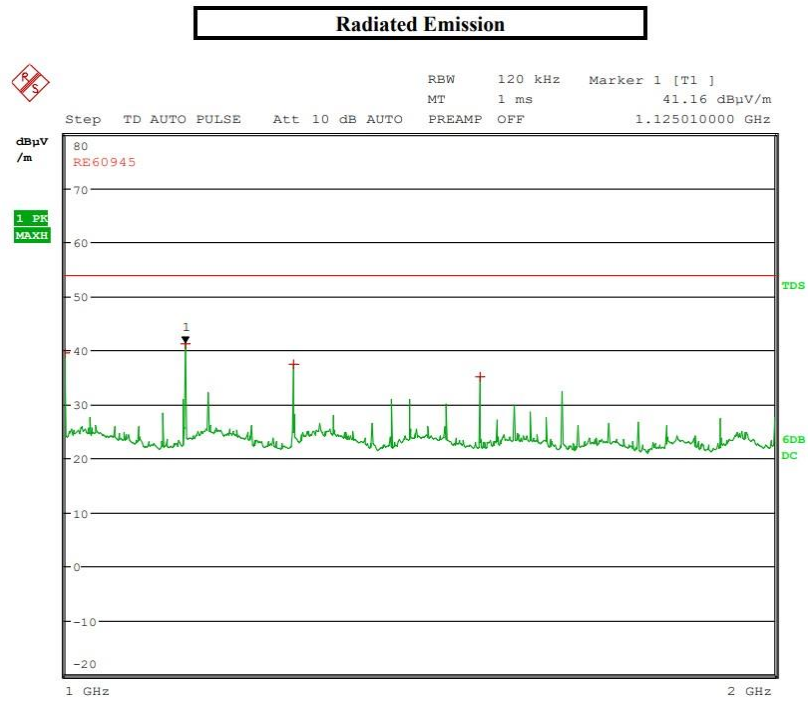

Figure 5-17: Passed Radiated (1GHz-2GHz) [19]

5.3.5 Temperature Test

Reviewing the rapport received from the lab, it had a comment mentioning the analog input performance during the dry heat temperature tests, pointing out that the registered voltage on the analog input was deviating from the target value. Using our own heat chamber confirmed this deviation.

Our own heat test was performed by inputting a known voltage to the analog input and recording the registered voltage, while recording the values of the microcontroller's internal temperature sensor (Figure 5-18 and Figure 5-19).

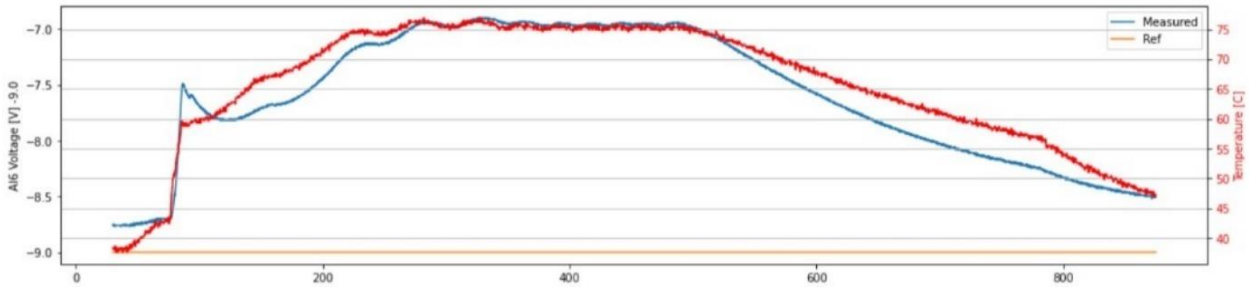

Figure 5-18: Analog Input Temperature Test

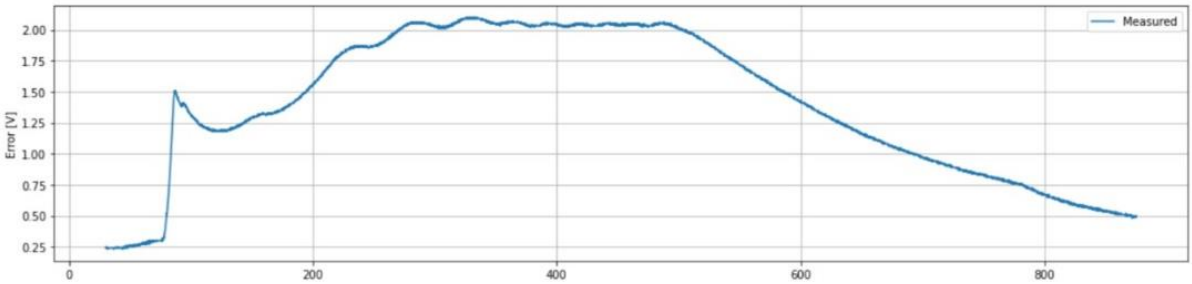

Figure 5-19: Analog Input Test Voltage Error

The results seemed to indicate that that the input tended towards 0V while under high temperatures. Probing the analog input's second stage with a voltmeter showed that the second stage amplifier was not the issue. Which left only the low pass filter and ADC input voltage protection diodes (Figure 5-20).

The diodes seemed to act like resistors when exposed to higher temperatures and removing them instantly solved the problem. We could also short the 51kΩ resistor, however removing the diodes is easier, and the diodes are rendered useless anyway. Due to the decision discussed in section 5.2.2 to keep the analog input mode-switches in the ON position, the voltages necessary to damage the ADC inputs cannot be produced.

So, removing the diodes makes the board register a stable voltage reading through the whole heat cycle. Note that the capacitor in the Figure 5-20 is the array capacitor that is removed due to the issue discussed in section 5.2.2.

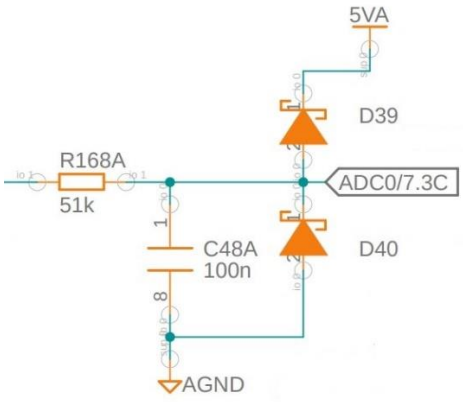

Figure 5-20: ADC Input, Voltage Protection [20]

5.4 Overall Testing Results

In the end of the testing process, we officially have a certified product that can be used for marine applications. The board as it stands lacks the isolated analog output functionality that was intended for it; we did test the function of the isolated analog outputs, purely for testing purposes, but since this breaks the isolated property, it is not viable for use. To properly use this board, it must be powered through the large input power filter that we used to pass the EMC tests.

Apart from fixing the obvious small faults in the voltage references and analog input section, further design of the IOB will have to redo the layer structure completely to improve EMC performance so that the input power filter can be discarded. Also, isolated I2C transceivers must be added so that the isolated analog output region can be used.

6 Integrated Design Phase

The next version of the IOB is purely called the IOB-Mk3 (Figure 6-1) where the microcontroller is placed directly on the board. At this stage. all the peripheral functions are verified using the previous board, the IOB-Mk3-Transit. The central 10 pin connector seen the Figure 6-1 is the programming plug, where a Single Wire Debug method will be used to program and debug the board in the next testing phase.

This design also benefited greatly from having many of the faults from the IOB-Mk3-Transit addressed and fixed. However, this board has yet to be tested beyond basic visual inspection, fundamental power voltages and reference voltages, all of which this board passed. This chapter will look at the updates, changes and improvements made to the IOB. For a more detailed overview of the difference in power planes and PCB layers, have a look at the appendix.

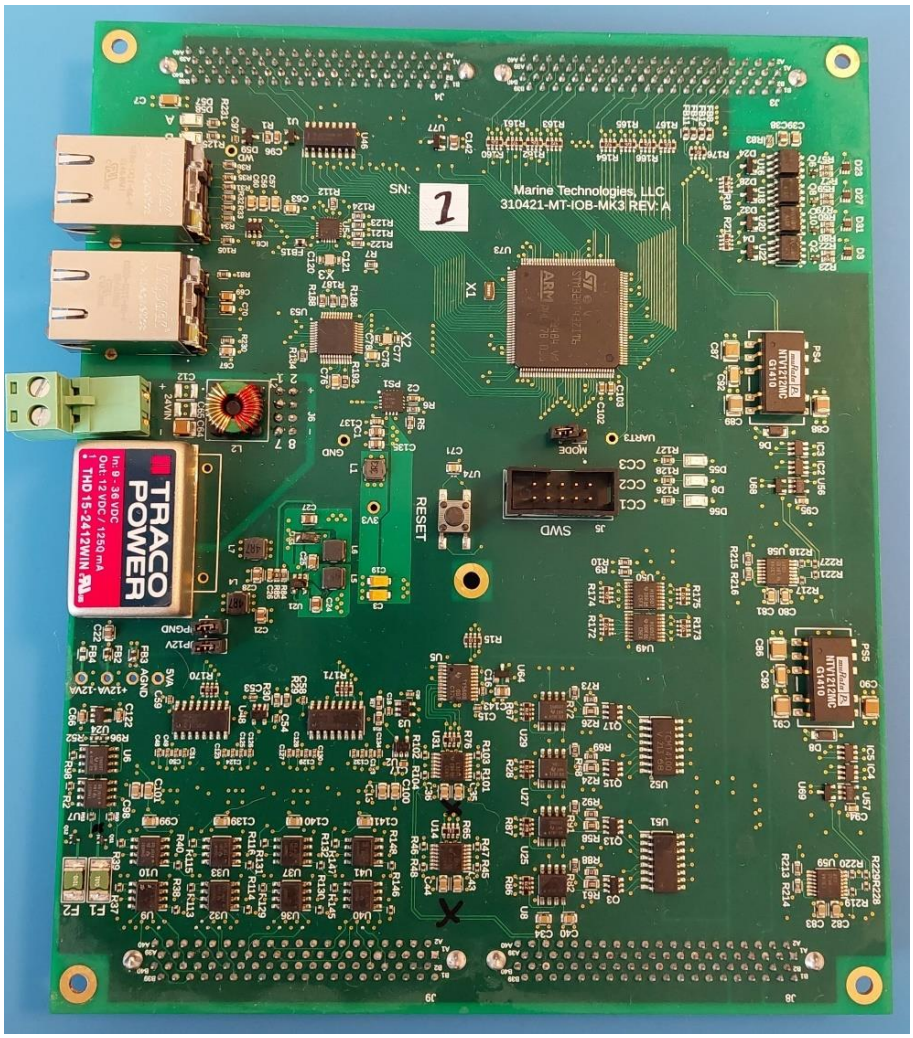

Figure 6-1: IOB-Mk3

6.1 Corrected Issues

The circuity changes that were implemented are the lessons learned from the IOB-Mk3-Transit; mostly simple layout and circuit mistakes that were made. These are the voltage reference mistakes of section 5.1.1 where the pinout of certain components was wrongly defined and the one instance where a necessary capacitor was not added. Also, the broken loop issue of section 5.2.4 has also been addressed by keeping the passive output version of the shift register and just adding the pullup resistors.

The analog input went through many fixes, as described in section 5.2.2. In the IOB-Mk3, the capacitors were re-added as single capacitor components and not the capacitor array as before. The mode-switches are removed and over voltage diodes are removed as well.

An important issue was the isolated analog output region, which in section 5.2.3 was discovered to have an I2C issue where isolated data bidirectionality was required. The suggested fix implemented in IOB-Mk3 is to use the ADUM1250ARZ component [21]. This component uses magnetic isolation, seemingly like ethernet magnetics to achieve isolated bidirectional data transmission.

Lastly, in section 4.1.3 the watchdog circuit solution used the STWD100 circuit instead of the previously used charge pump in Figure 4-6 [11]. The STWD100 solution did work, however the charge pump circuit is preferable due to its flexibility and availability, being an adjustable passive component solution.

The circuit in Figure 6-2 shows the edited charge pump with an increased time constant of the internal RC segment, giving this circuit a longer alarm time than the IOB-Mk2s circuit, allowing the microcontroller to use a slower input frequency to drive this circuit. The input capacitor is also increased to be able to increase the amount of charge that can be pumped in by each input pulse.

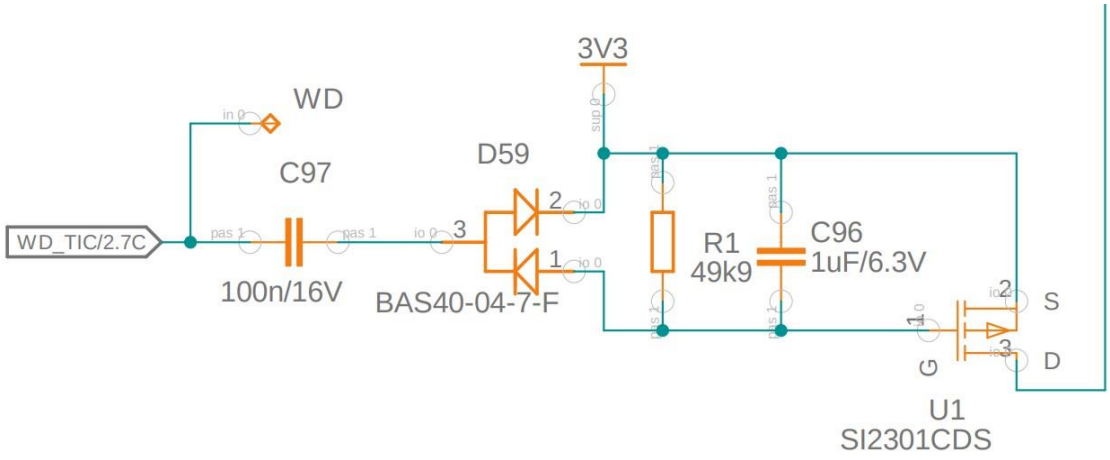

Figure 6-2: IOB-Mk3 Watchdog Charge Pump [22]

6.2 EMC Improvements

The second goal of the IOB-Mk3, aside from mounting the microcontroller directly, is to improve the EMC performance and hopefully to not require the large amount of input filtering that the IOB-Mk3-Transit requires. This was done by being strict with the layer definition and use, where signals are contained to the signal layers and power polygons can enjoy their respective layers without continuity breaks from traces. The polygons also cover the board more completely, coupling the ground and power planes more closely. The new layer designations are listed in Table 6-1.

Table 6-1: IOB-Mk3 Layer Structure

Layer 1	Single Plane
Layer 2	Ground plane
Layer 3	Signal Plane
Layer 4	Power Plane
Layer 5	Power Plane
Layer 6	Signal Plane
Layer 7	Ground Plane
Layer 8	Signal Plane

In some ways, planning the traces that went to the microcontrollers was made easier in this iteration, due to not having the development board scatter the microcontroller pins over such a large area. This made terminating especially the digital inputs and outputs much more organized. Additionally, having the development board removed gave freedom of component placement, not only in board area, but also in height.

All the power distribution relevant components could now be kept close together, allowing me to make an input-power-island of sorts. In Figure 6-3 you can see a single layer this power island, marked as the two 24V polygons. This island includes the two connectors that feed in the 24V or pass it on for external use. Inside the 24V island, the recommended input filtering is applied before the DCDC converter as per the datasheet, using a 2.2µF bypass capacitor followed by a 325µH common mode choke.

The surrounding polygons in Figure 6-3 give brief insight how the analog region receives its 12V based voltages; showing both “Pre +12VA” and “Pre -12VA” in the process of being completely filtered and ready for analog use. Lastly, for testing purposes, two jump straps were added that can completely disconnect the DCDC converter from the rest of the board. These can be used to measure current consumption, add output filters to the DCDC converter, or even injecting a known clean 12V source directly to the board.

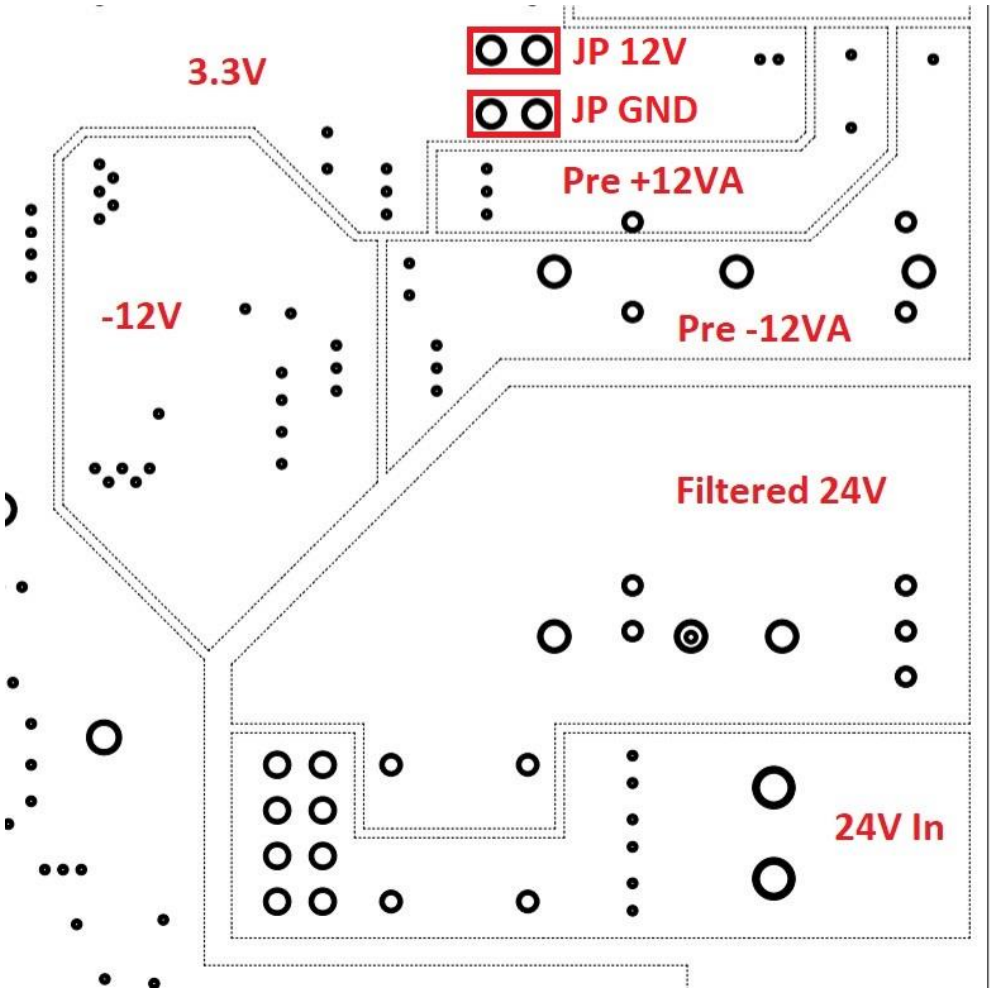

Figure 6-3: IOB-Mk3 Layer 4 Power Polygons

7 Discussion and Conclusion

The core of this thesis from the start was the design and testing of a circuit board with microcontroller doing the task previously reserved for an FPGA, while attempting to create and release a viable, approved and certified product. As far as we are aware, this is the first time that microcontrollers have been applied to thruster control in the maritime sector, perhaps because of the lack of reason to stray from tried tested and true methods.

The main reason for the redesign from the start was to make the IOB line of cards proprietary to control and predict the supply of boards, and to not rely on another party to always supply them. Considering recent microcontroller advancements, it became hard to not consider their use when a rare opportunity arises to do something different after nearly ten years.

Some of the reasons why we wanted to try breaking out of the FPGA mold were reasons like practicality, flexibility, and component availability, all of which contribute to expanding the use of the product by lowering the threshold of its use. Also, the issue of availability became apparent when FPGAs suddenly became scarce and the ability to deliver new systems was threatened.

I had access to the complete set of schematics and time to review and understand before designing. A good portion of the design of peripheral electronics, like the analog and digital I/Os, is similar to what has been done for 20 years. However, certain components had to be updated or switched in order adapt to the microcontroller or to guarantee design longevity.

To summarize this process and my contribution, I have researched Marine Technologies' I/O system and reduced it to its essentials, made those essentials fit into the microcontrollers resource capacity. I adapted the schematics, taking aspects from two previous versions of the IOB and added some new contributions, defined the BOM, measured the physical dimensions of the previous boards to match the connector layout to ensure mechanical backwards compatibility, and designed the board layout. When the boards arrived, I stood for testing of the prototypes on a hardware basis, while my colleague aided me by leading the charge in software. After the board function had been clarified and we knew what we had, I traveled to a certification lab to make the board comply with EMC requirements.

At the current state, we have a board that is certified for maritime use. The IOB has also been installed into a system that cleared a "Factory Acceptance Test" (FAT) and has thus been delivered out to a vessel for assembly; the product is in use, although not with the full set of functions. The gained knowledge has been applied to design the latest version featured in chapter 6, which will now enter its own testing phase.

The original research question was to validate whether a Microcontroller could replace an FPGA on the MT I/O board. Initially, this assignment was about the microcontroller and how it fared in comparison to the FPGA. However, most of the work and research went into the design and testing on the EMC front. In the end, microcontroller function was tested and verified, and the microcontroller seems to be able to hold performance as intended even through rigorous environmental testing, even being able to pass an FAT in actual system installment. While this is true, the question of long-term reliability is a question where the answer is only revealed over the same long-term. Moving forward, continuous in-house testing is necessary; testing the limits and ensuring that these two new boards continue to be reliable is crucial for the microcontroller to earn our trust completely.

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Appendix

A. EMC Certification Test Setup

Figure 0-1: Radiated Emissions Test Setup (150KHz-30MHz) [19]

Figure 0-2: Test Setup Radiated 1GHz and Above [19]

B. Nucleo Pin Selection

Nucleo Dev Board Pin Selection C11 Left Row

C10	ADC1			SPI3_SCK
C12	Serial_in_4		UART5_TX	
VDD				
BOOT				
F6	DIN_29			
F7	DIN_28			
A13*				
A14*				
A15	NIC			SPI1_CS
GND				
B7*(SB68)	DIN_22			
C13	DIN_20			
C14				
C15				
H0				
H1*	CARD_ID_44			
VBAT				
C2	ADC0			SPI2_MISO
C3	ADC0			SPI2_MOSI
D4	DIN_15			
D5	Serial_in_1		UART2_TX	
D6	ADC1			SPI3_MOSI
D7	DIN_10			
E3	DIN_7			
GND				
F1	I2C2_SCL	I2C2_SCL		
F0	I2C2_SDA	I2C2_SDA		
D1	Serial_in_3		UART4_TX	
D0	DOUT_5			
G0	DOUT_9			
E1*	DOUT_12			
G9	DOUT_22			
G12	DOUT_24			
NC				
D9*				

Nucleo Dev Board Pin Selection C11 Right Row

C11	ADC1		[redacted]	SPI3_MISO
D2	DIN_30			
E5V				
GND				
NC				
3V3				
NRST				
3V3				
5V				
GND				
GND				
VIN				
NC				
A0	DIN_16		[redacted]	
A1*	[redacted]			
A4	ADC1			SPI3_CS
B0*(SB39)	NIC INT			SPI INTERREUPT
C1*	[redacted]			[redacted]
C0	CARD_ID_42			
D3	ADC0			SPI2_SCK
G2	DIN_14			
G3	DIN_12			
E2	DAC			SPI4_SCK
E4	DAC			SPI4_CS
E5	x	LED		[redacted]
F2	DIN_2			
F8	DOUT_0			[redacted]
F9	DOUT_2			
G1	DOUT_6			
GND				
E6	DAC			SPI4_MOSI
G15	DOUT_23			
G10	DOUT_25			[redacted]
G13*	[redacted]			
G11*				[redacted]

Nucleo Dev Board Pin Selection C12 Left Row

C9	I2C3_SDA	I2C3_SDA		
B8	I2C1_SCL	I2C1_SCL		
B9	I2C1_SDA	I2C1_SDA		
AVDD				
GND				
A5	DIN_27			
A6	DIN_26			
A7*				
B6	Serial_in_0		UART1_TX	
C7	DIN_24			
A9*(SB23)	BL_Data			
A8*	I2C3_SCL	I2C3_SCL		
B10	DIN_18			
B4	NIC			SPI1_MISO
B5	NIC			SPI1_MOSI
B3	NIC			SPI1_SCK
A10*(SB24)	Serial_in_2		LPUART1_RX	
A2*				
A3	CARD_ID_41			
GND				
D13	I2C4_SDA	I2C4_SDA		
D12	I2C4_SCL	I2C4_SCL		
D11	DIN_9			
E10	DIN_6			
E12	DIN_4			
E14	DIN_1			
E15	DOUT_1			
E13	DOUT_3			
F13	DOUT_7			
F12	DOUT_10			
G14	DOUT_20			
GND				
D10*	DOUT_26			
G7*(SB76)	SH/!LD			
G4	DOUT_29			

Nucleo Dev Board Pin Selection C12 Right Row

C8	DIN_31	
C6	serial_in_5	UART6_TX
C5*		
U5V		
D8*		
A12*		
A11*		
B12	ADC0	SPI2_CS
B11	DIN_25	
GND		
B2	DIN_21	
B1	DIN_19	
B15	DIN_17	
B14*	CARD_ID_45	
B13*(JP6)		
AGND		
C4*		
F5	CARD_ID_43	
F4	CARD_ID_40	
E8	Serial_in_6	UART7_TX
F10	DIN_13	
E7	DIN_11	
D14	DIN_8	
D15	DIN_5	
F14	DIN_3	
E9	DIN_0	
GND		
E11	DOUT_4	
F3	DOUT_8	
F15	DOUT_11	
F11	DOUT_21	
E0	Serial_in_7	UART8_RX
G8	DOUT_27	
G5	DOUT_28	
G6* (SB59)	WD_TIC	

C. IOB 4X 80p Hirose usage

J3

Iobmk2	J3	Central TB	Panel TB	Comment	Transit
Serial Lo 7	A1				
Serial Hi 7	B1				
Serial Lo 6	A2				
Serial Hi 6	B2				
Serial Lo 5	A3				
Serial Hi 5	B3				
Serial Lo 4	A4				
Serial Hi 4	B4				
Serial Lo 3	A5				
Serial Hi 3	B5				
Serial Lo 2	A6				
Serial Hi 2	B6				
Serial Lo 1	A7				
Serial Hi 1	B7				
Serial Lo 0	A8				
Serial Hi 0	B8				
GND	A9				
SDA0	B9				
SCL0	A10				
SDA1	B10				
SCL1	A11				
SDA2	B11				
SCL2	A12				
SDA3	B12				
SCL3	A13				
GND	B13				
GND	A14				
+3V3	B14				
+3V3	A15				
NC	B15				
Di 31	A16	DPM			
DI 30	B16	DPM			
DI 29	A17	DPM			
DI 28	B17	DPM			
DI 27	A18	DPM			
DI 26	B18	DPM			
DI 25	A19				
DI 24	B19				
DI 23	A20				
DI 22	B20				
DI 21	A21				
DI 20	B21				

DI 19	A22				
DI 18	B22				
DI 17	A23				
DI 16	B23				
GND	A24				
GND	B24				
DI 46	A25				
DI 45	B25			CARD ID	
DI 44	A26			CARD ID	
DI 43	B26			CARD ID	
DI 42	A27			CARD ID	
DI 41	B27			CARD ID	
DI 40	A28			CARD ID	
+3V3	B28				
+3V3	A29				
DI 47	B29				
DI 15	A30				
DI 14	B30				
DI 13	A31				
DI 12	B31				
DI 11	A32				
DI 10	B32				
DI 9	A33				
DI 8	B33				
DI 7	A34				
DI 6	B34				
DI 5	A35				
DI 4	B35				
DI 3	A36				
DI 2	B36				
DI 1	A37				
DI 0	B37				
GND	A38				
GND	B38				
NC	A39				
NC	B39				
NC	A40				
NC	B40				

J4

Iobmk2	J4	Central TB	Panel TB	Commment	Transit
NC	A1				
1V2	B1				
NC	A2				
NC	B2				
NC	A3				
+5V	B3				
+5V	A4				
DO 0	B4				
DO 1	A5				
DO 2	B5				
DO 3	A6				
DO 4	B6				
DO 5	A7				
DO 6	B7				
+5VREL	A8				
GND	B8				
GND	A9				
NC	B9				
NC	A10				
DO 7	B10				
DO 8	A11				
DO 9	B11				
DO 10	A12				
DO 11	B12				
DO 12	A13				
DO 13	B13				
+5VREL	A14				
GND	B14				
GND	A15				
RS_0P	B15				
RS_0N	A16				
DO 14	B16				
DO 15	A17				
DO 16	B17				
DO 17	A18				
DO 18	B18				
DO 19	A19				
DO 20	B19	DPM			
+5VREL	A20				
RS_1P	B20				
RS_1N	A21				
+5V	B21				
+5V	A22				
DO 21	B22				

DO 22	A23				
DO 23	B23				
DO 24	A24				
DO 25	B24				
DO 26	A25				
DO 27	B25				
+5VREL	A26				
GND	B26				
GND	A27				
RS_2P	B27				
RS_2N	A28				
DO 28	B28				
DO 29	A29				
DO 30	B29				
DO 31	A30				
DO 32	B30				
DO 33	A31				
!WD	B31	Charge pump			stwd100
+5VREL	A32				
GND	B32				
GND	A33				
NC	B33				
NC	A34				
+5V	B34				
+5V	A35				
NC	B35				
RS_3P	A36				
RS_3N	B36				
RS_4P	A37				
RS_4N	B37				
RS_5P	A38				
RS_5N	B38				
RS_6P	A39				
RS_6N	B39				
RS_7P	A40				
RS_7N	B40				

J8

Iobmk2	J8	Central TB	Panel TB	Comment	Transit
Aout 19	A1			Isolated	
Aout18	B1			Isolated	
Iso 1	A2			Iso GND	
+12V Iso 1	B2			Isolated	
Out HI 19	A3			Isolated	
Out LO 19	B3			Isolated	
Out HI 18	A4			Isolated	
Out LO 18	B4			Isolated	
NC	A5				
NC	B5				
Aout 17	A6			Isolated	
Aout16	B6			Isolated	
Iso 0	A7			Iso GND	
+12V Iso 0	B7			Isolated	
Out HI 17	A8			Isolated	
Out LO 17	B8			Isolated	
Out HI 16	A9			Isolated	
Out LO 16	B9			Isolated	
NC	A10				
NC	B10				
NC	A11				
NC	B11				
AGND	A12				
AGND	B12				
NC	A13				
NC	B13				
+12VA	A14				
-12VA	B14				
Out HI 15	A15				
Out LO 15	B15				
Out HI 14	A16				
Out LO 14	B16				
Out HI 13	A17				
Out LO 13	B17				
Out HI 12	A18				
Out LO 12	B18				
Out HI 11	A19				
Out LO 11	B19				
Out HI 10	A20				
Out LO 10	B20				
Out HI 9	A21				
Out LO 9	B21				
Out HI 8	A22				
Out LO 8	B22				

Out HI 7	A23				DAC0
Out LO 7	B23				DAC0
Out HI 6	A24				DAC0
Out LO 6	B24				DAC0
Out HI 5	A25				DAC0
Out LO 5	B25				DAC0
Out HI 4	A26				DAC0
Out LO 4	B26				DAC0
Out HI 3	A27				DAC0
Out LO 3	B27				DAC0
Out HI 2	A28				DAC0
Out LO 2	B28				DAC0
Out HI 1	A29				DAC0
Out LO 1	B29				DAC0
Out HI 0	A30				DAC0
Out LO 0	B30				DAC0
AGND	A31				
AGND	B31				
Aout 15	A32				
Aout 14	B32				
Aout 13	A33				
Aout 12	B33				
Aout 11	A34				
Aout 10	B34				
Aout 9	A35				
Aout 8	B35				
Aout 7	A36				DAC0
Aout 6	B36				DAC0
Aout 5	A37				DAC0
Aout 4	B37				DAC0
Aout 3	A38				DAC0
Aout 2	B38				DAC0
Aout 1	A39				DAC0
Aout 0	B39				DAC0
AGND	A40				
AGND	B40				

J9

Iobmk2	J9	Central TB	Panel TB	Comment	Transit
NC	A1				
NC	B1				
NC	A2				
NC	B2				
NC	A3				
NC	B3				
AGND	A4				
AGND	B4				
NC	A5				
Ain HI 31	B5				
Ain LO 31	A6	AGND		AGND	AGND
Ain HI 30	B6				
Ain LO 30	A7	AGND		AGND	AGND
Ain HI 29	B7				
Ain LO 29	A8	AGND		AGND	AGND
Ain HI 15	B8			Joystick	
Ain LO 15	A9	AGND	AGND	AGND	AGND
Ain HI 14	B9			Joystick	
Ain LO 14	A10	AGND	AGND	AGND	AGND
Ain HI 13	B10			Joystick	
Ain LO 13	A11	AGND	AGND	AGND	AGND
Ain HI 25	B11				
Ain LO 25	A12				
Ain HI 24	B12				
Ain LO 24	A13				
Ain HI 23	B13				
Ain LO 23	A14				
Ain HI 22	B14				
Ain LO 22	A15				
Ain HI 21	B15				
Ain LO 21	A16				
Ain HI 20	B16				
Ain LO 20	A17				
Ain HI 19	B17				
Ain LO 19	A18				
Ain HI 18	B18				
Ain LO 18	A19				
Ain HI 17	B19				
Ain LO 17	A20				
Ain HI 16	B20				
Ain LO 16	A21				
Ain HI 15	n				ADC1
Ain LO 15	A22				ADC1
Ain HI 14	B22				ADC1

Ain LO 14	A23				ADC1
Ain HI 13	B23				ADC1
Ain LO 13	A24				ADC1
Ain HI 12	B24				ADC1
Ain LO 12	A25				ADC1
Ain HI 11	B25				ADC1
Ain LO 11	A26				ADC1
Ain HI 10	B26				ADC1
Ain LO 10	A27				ADC1
Ain HI 9	B27				ADC1
Ain LO 9	A28				ADC1
Ain HI 8	B28				ADC1
Ain LO 8	A29				ADC1
Ain HI 7	B29				ADC0
Ain LO 7	A30				ADC0
Ain HI 6	B30				ADC0
Ain LO 6	A31				ADC0
Ain HI 5	B31				ADC0
Ain LO 5	A32				ADC0
Ain HI 4	B32				ADC0
Ain LO 4	A33				ADC0
Ain HI 3	B33				ADC0
Ain LO 3	A34				ADC0
Ain HI 2	B34				ADC0
Ain LO 2	A35				ADC0
Ain HI 1	B35				ADC0
Ain LO 1	A36				ADC0
Ain HI 0	B36				ADC0
Ain LO 0	A37				ADC0
+10V Ref	B37				
+2.5 Ref	A38				
-10V Ref	B38				
+12VA	A39				
-12VA	B39				
AGND	A40				
AGND	B40				

D. PCB Layers for Mk3-Transit

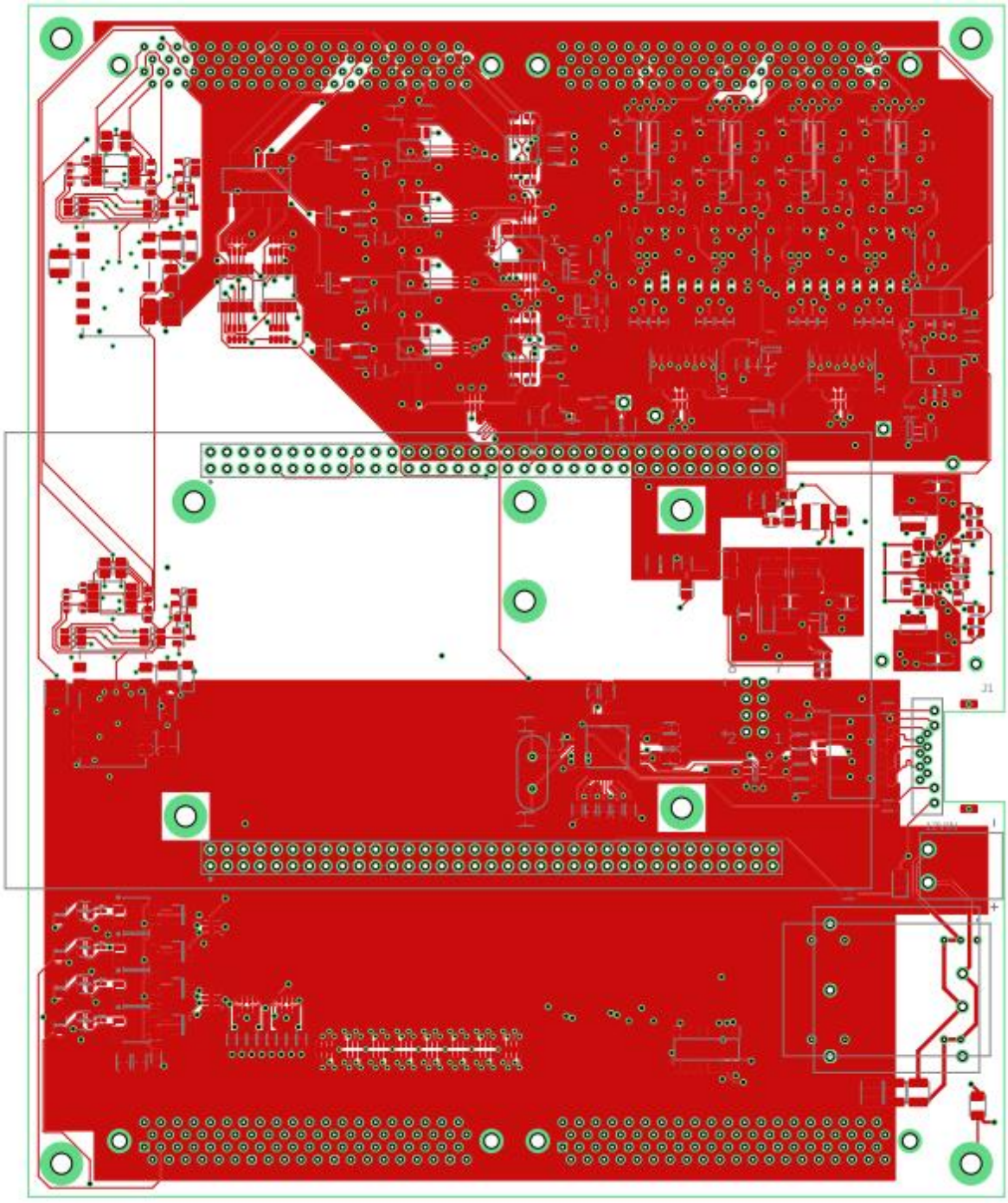

Figure 0-3: IOB-Tranist L1

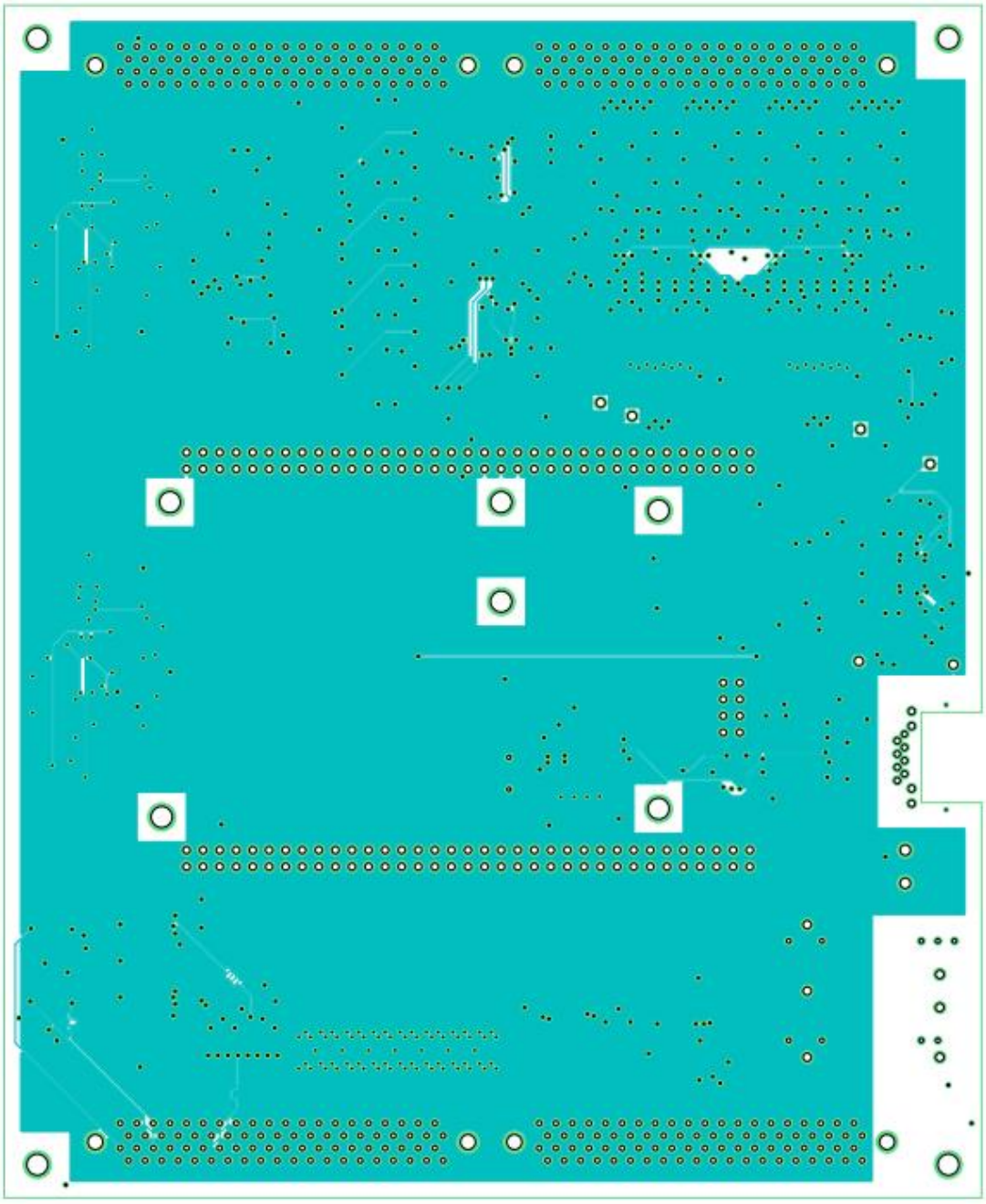

Figure 0-4: IOB-Transit L2

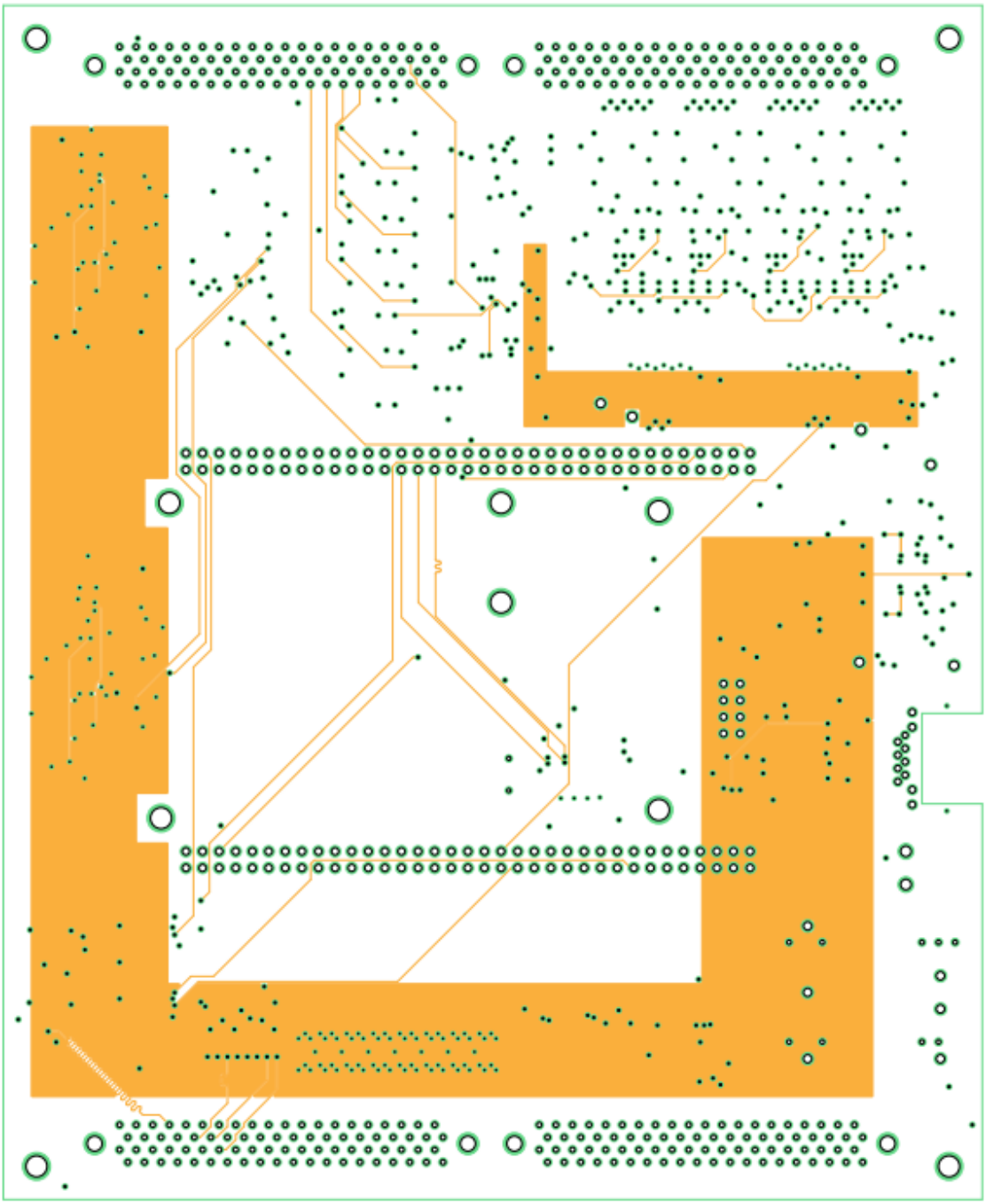

Figure 0-5: IOB-Transit L3

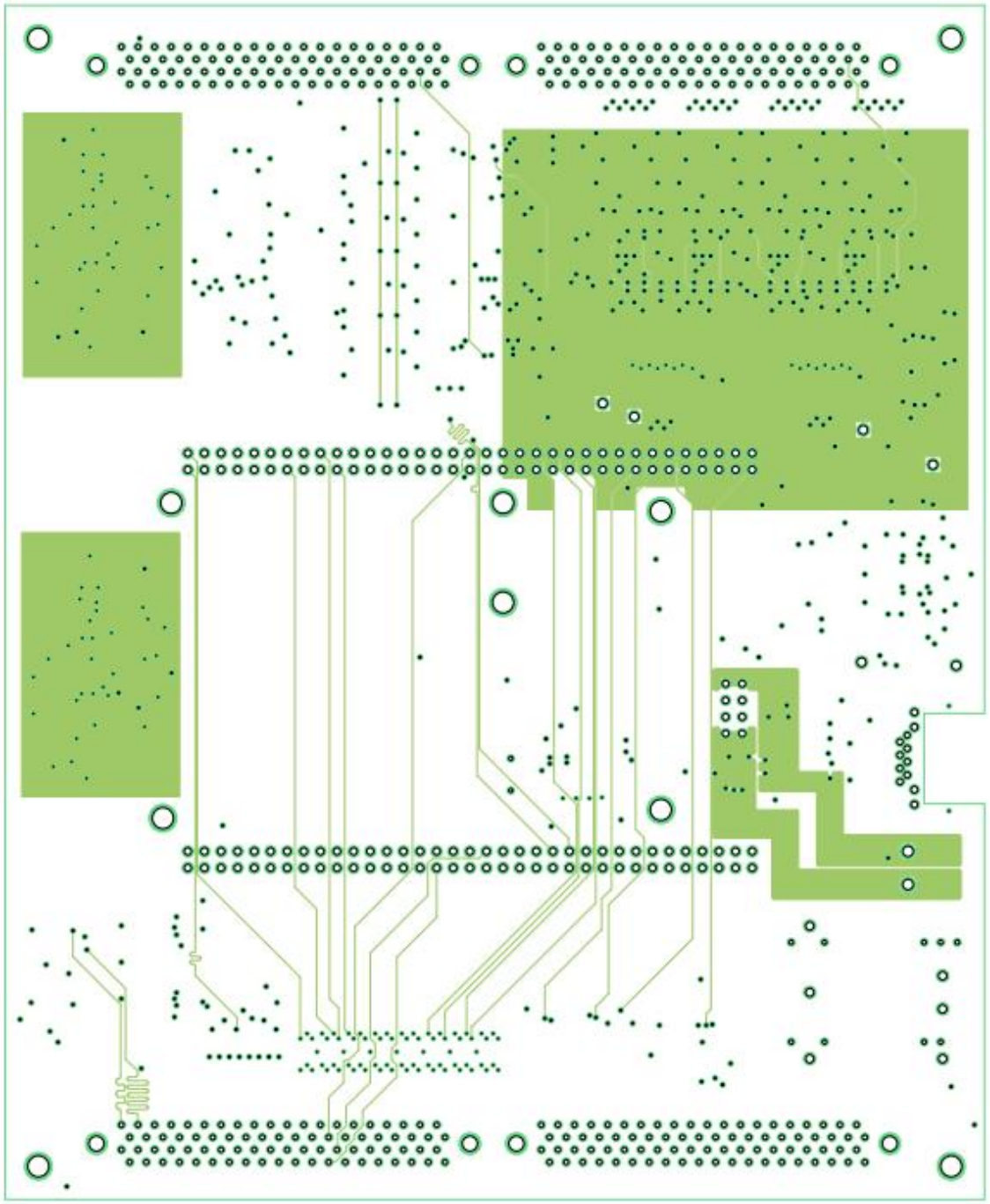

Figure 0-6: IOB-Transit L4

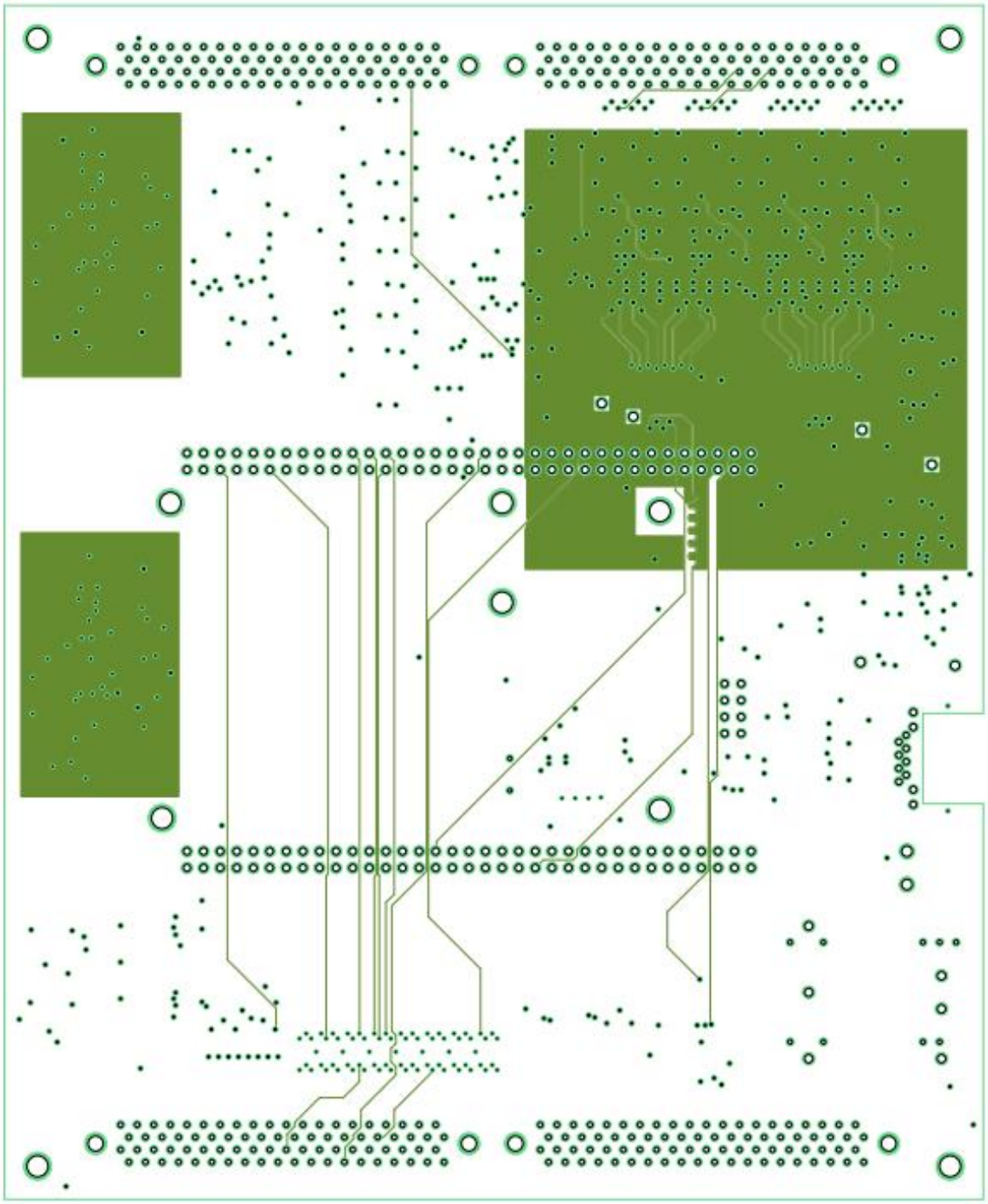

Figure 0-7: IOB-Transit L5

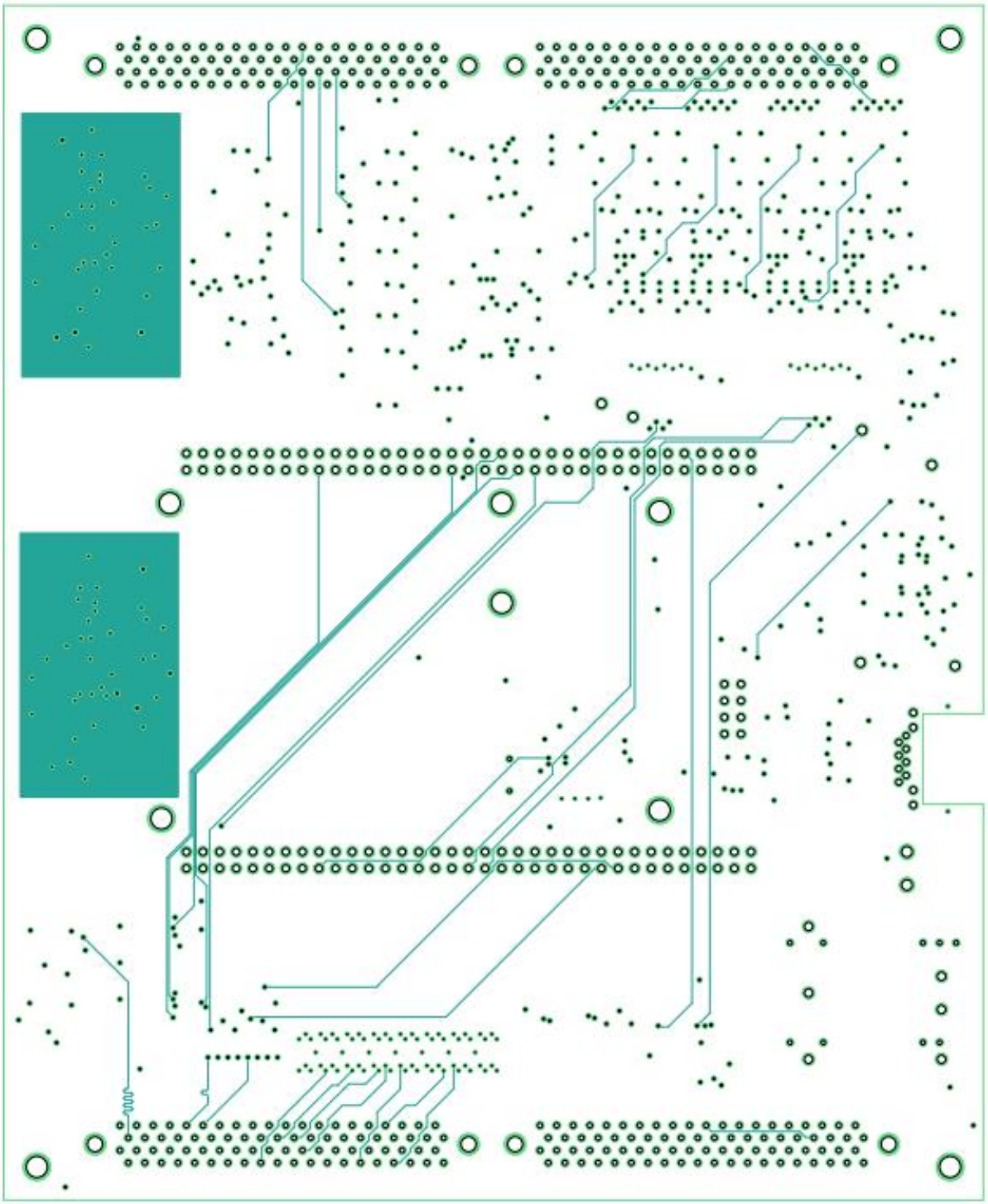

Figure 0-8: IOB-Transit L6

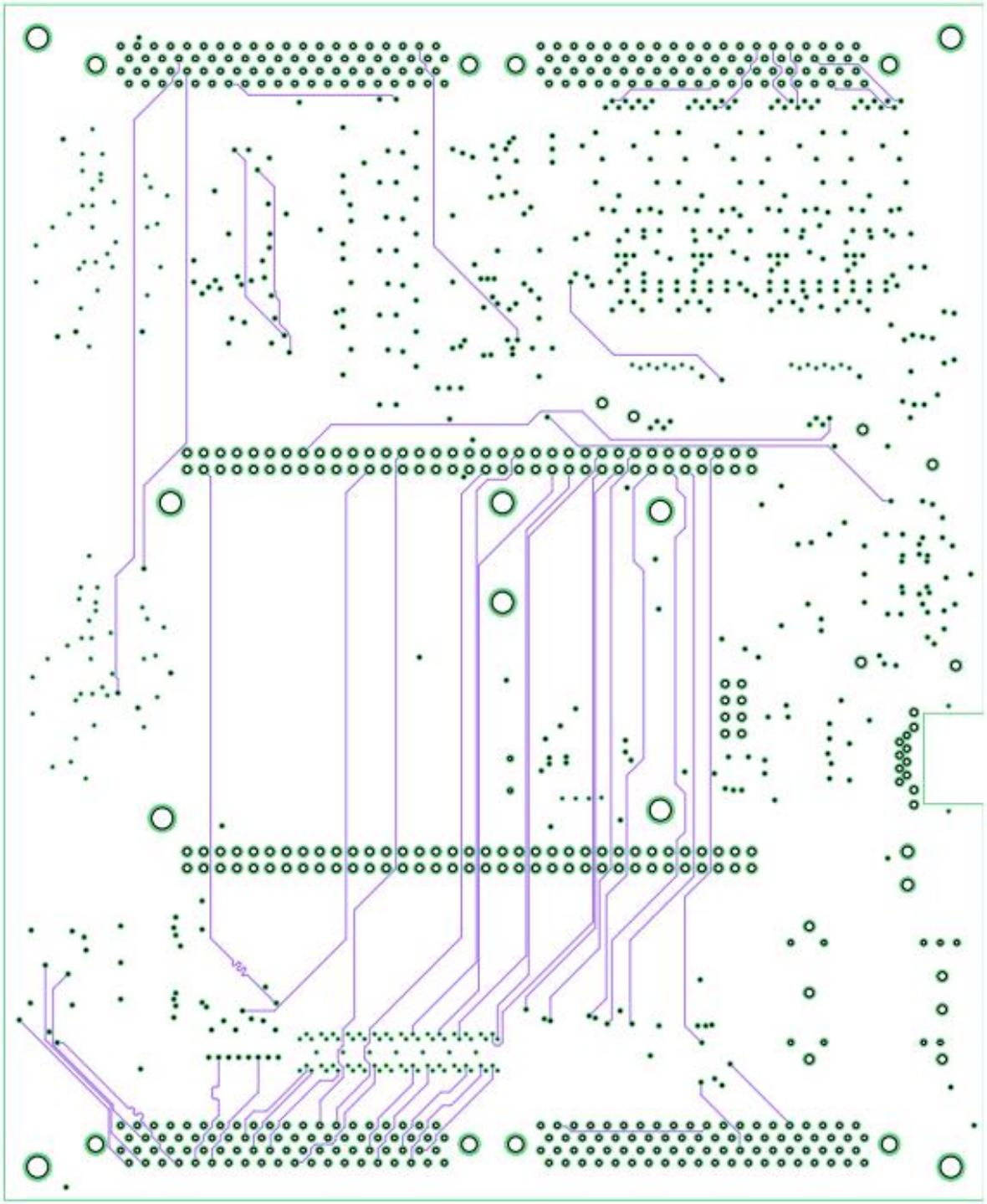

Figure 0-9: IOB-Transit L7

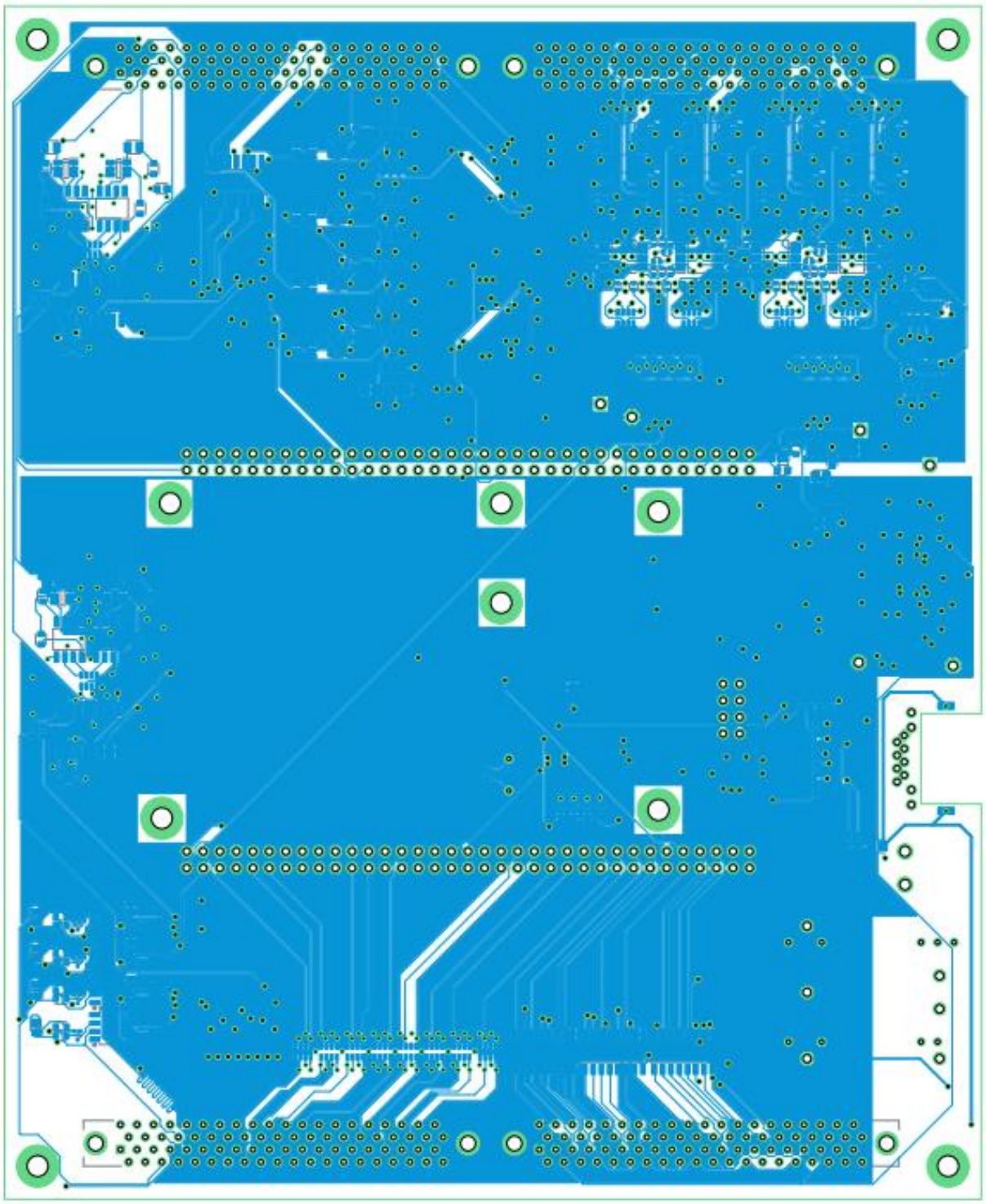

Figure 0-10: IOB-Transit L8

E. PCB Layers for IOB-Mk3

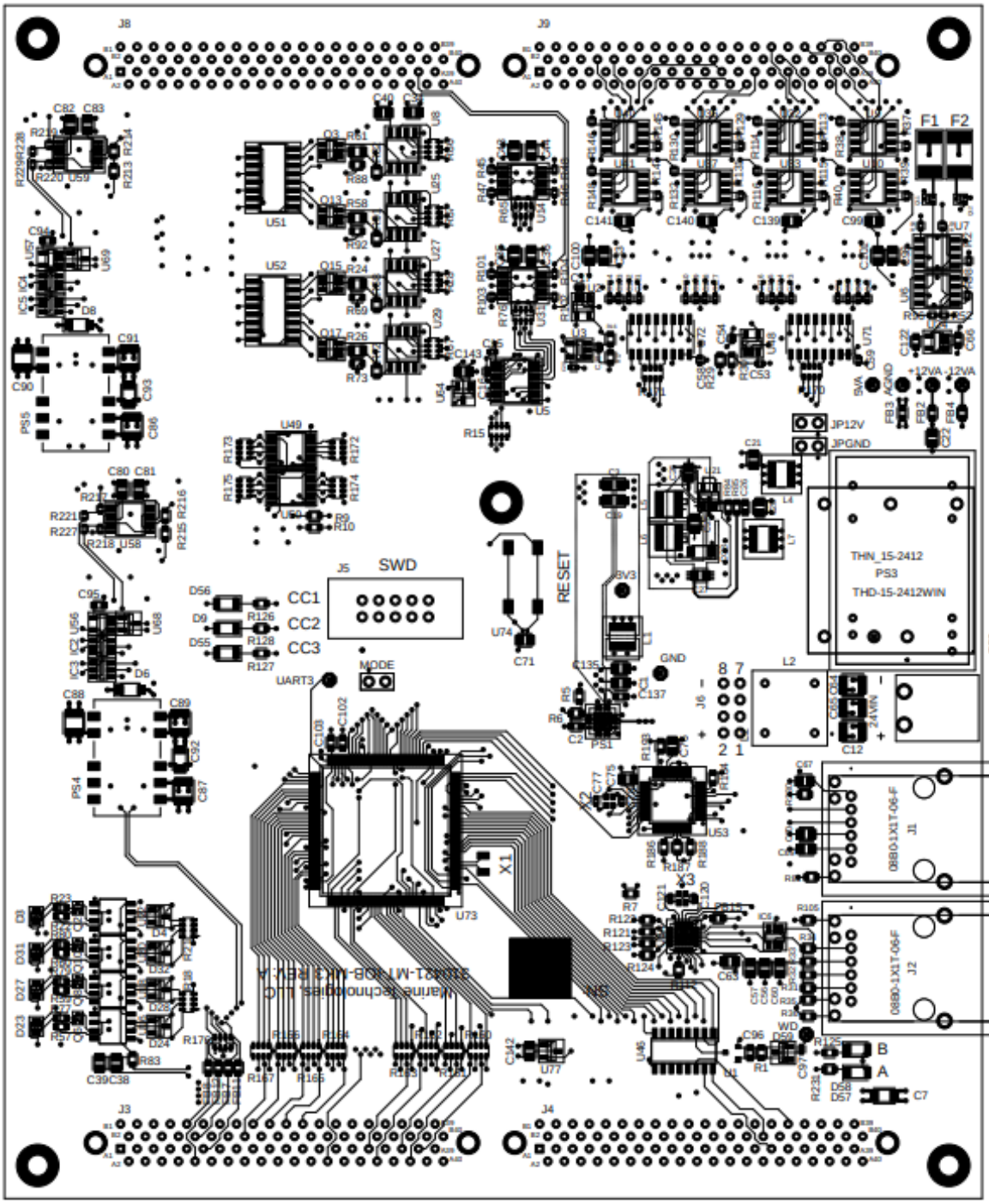

Figure 0-11: IOB-Mk3 L1

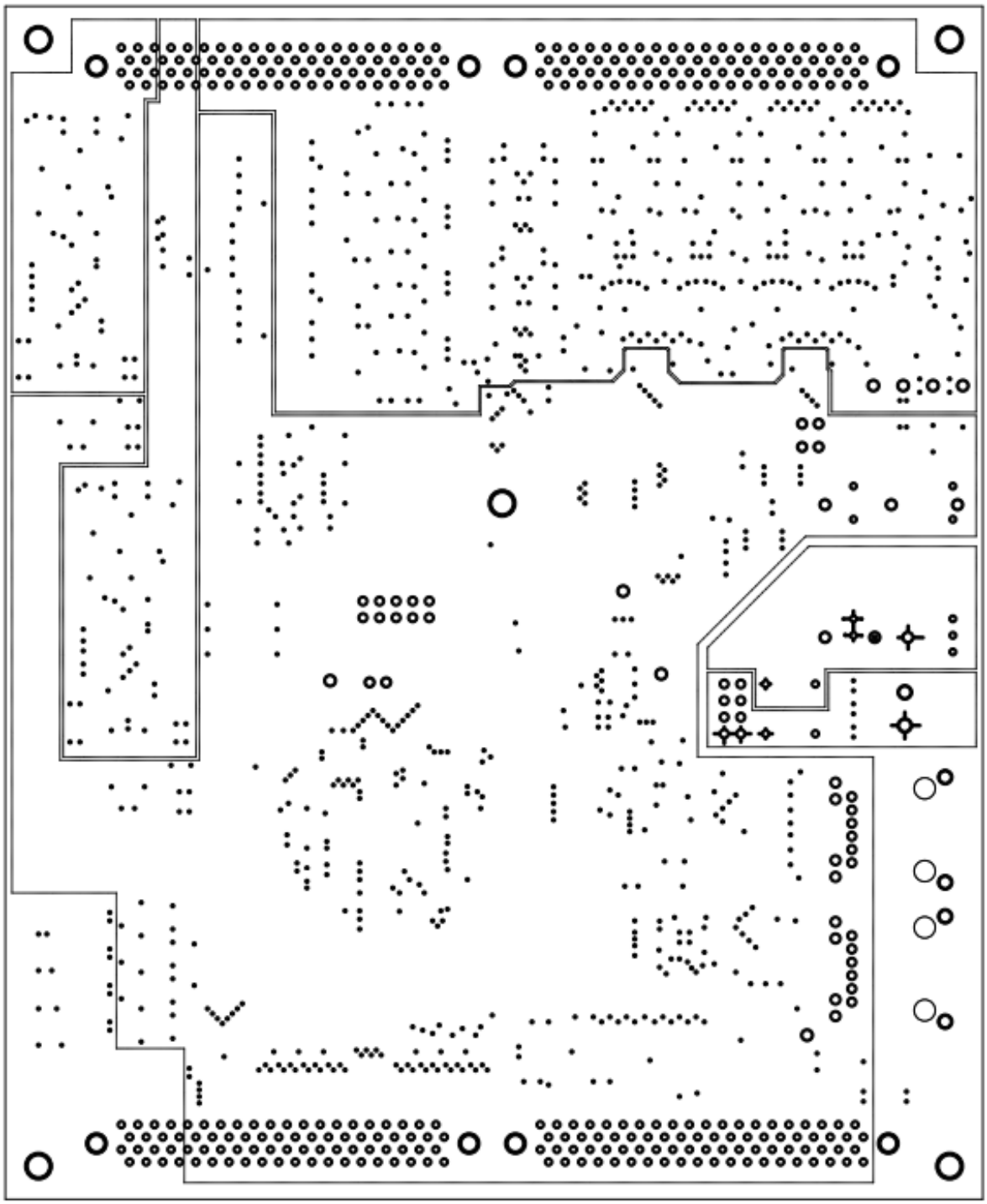

Figure 0-12: IOB-Mk3 L2

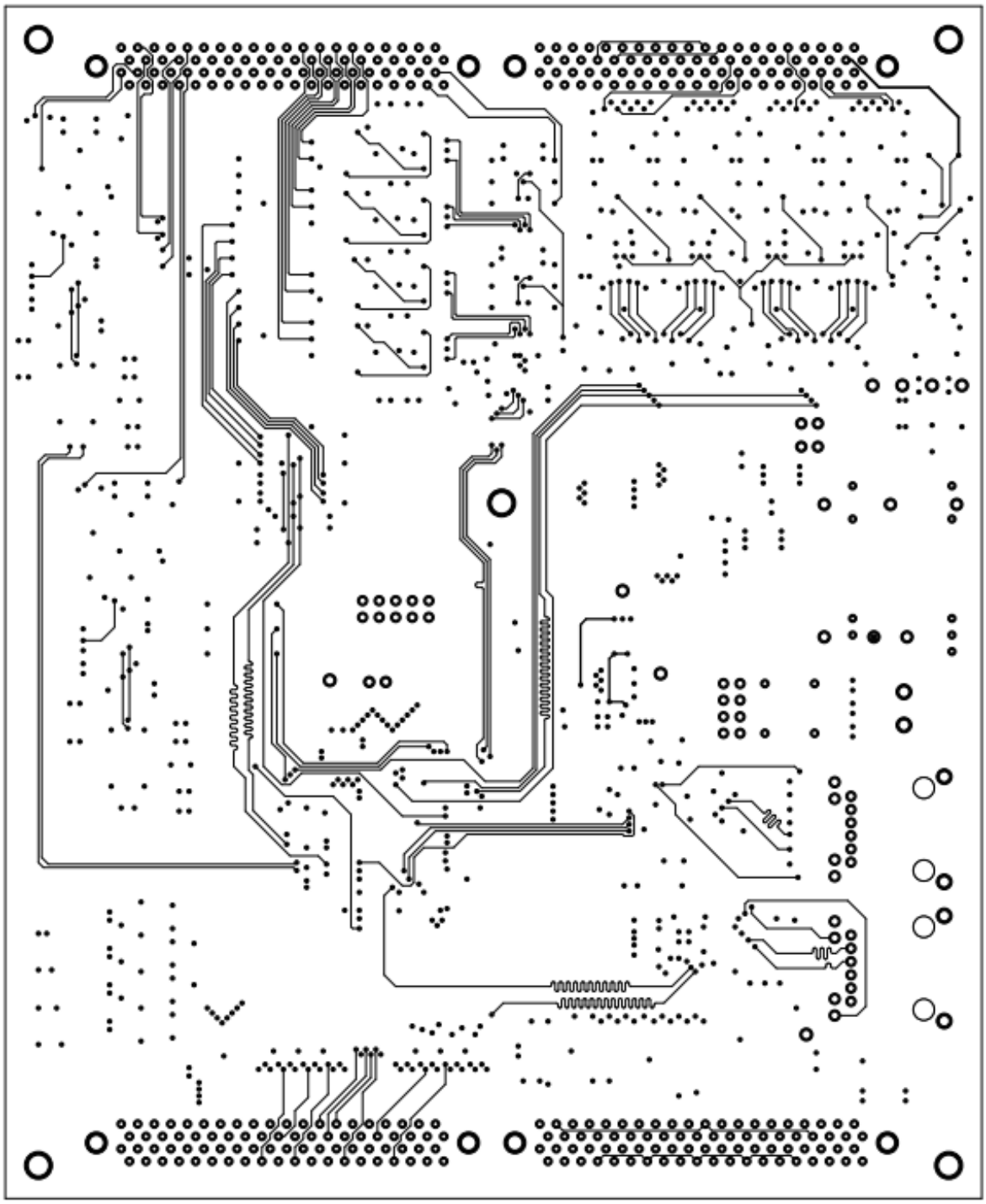

Figure 0-13: IOB-Mk3 L3

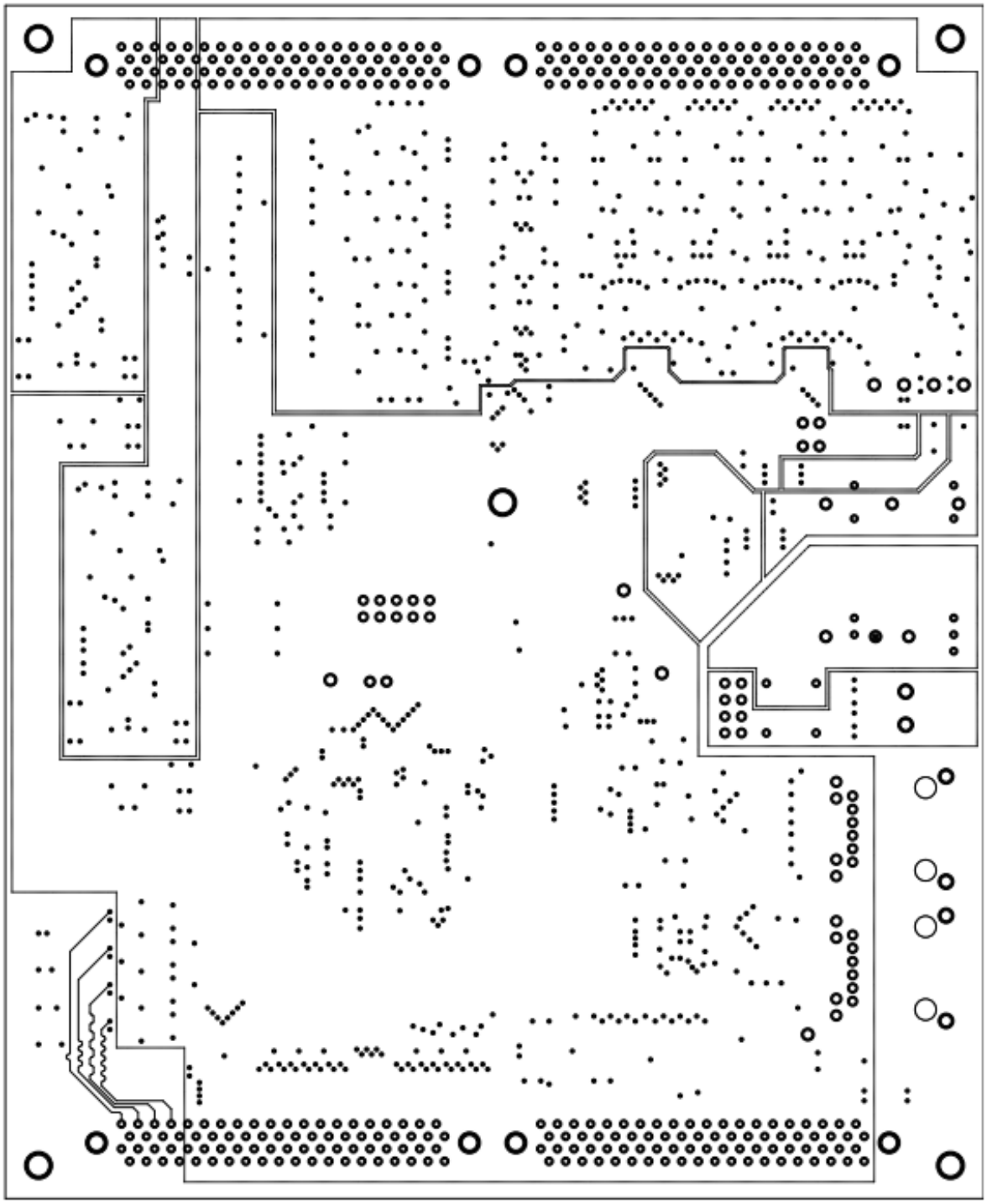

Figure 0-14: IOB-Mk3 L4

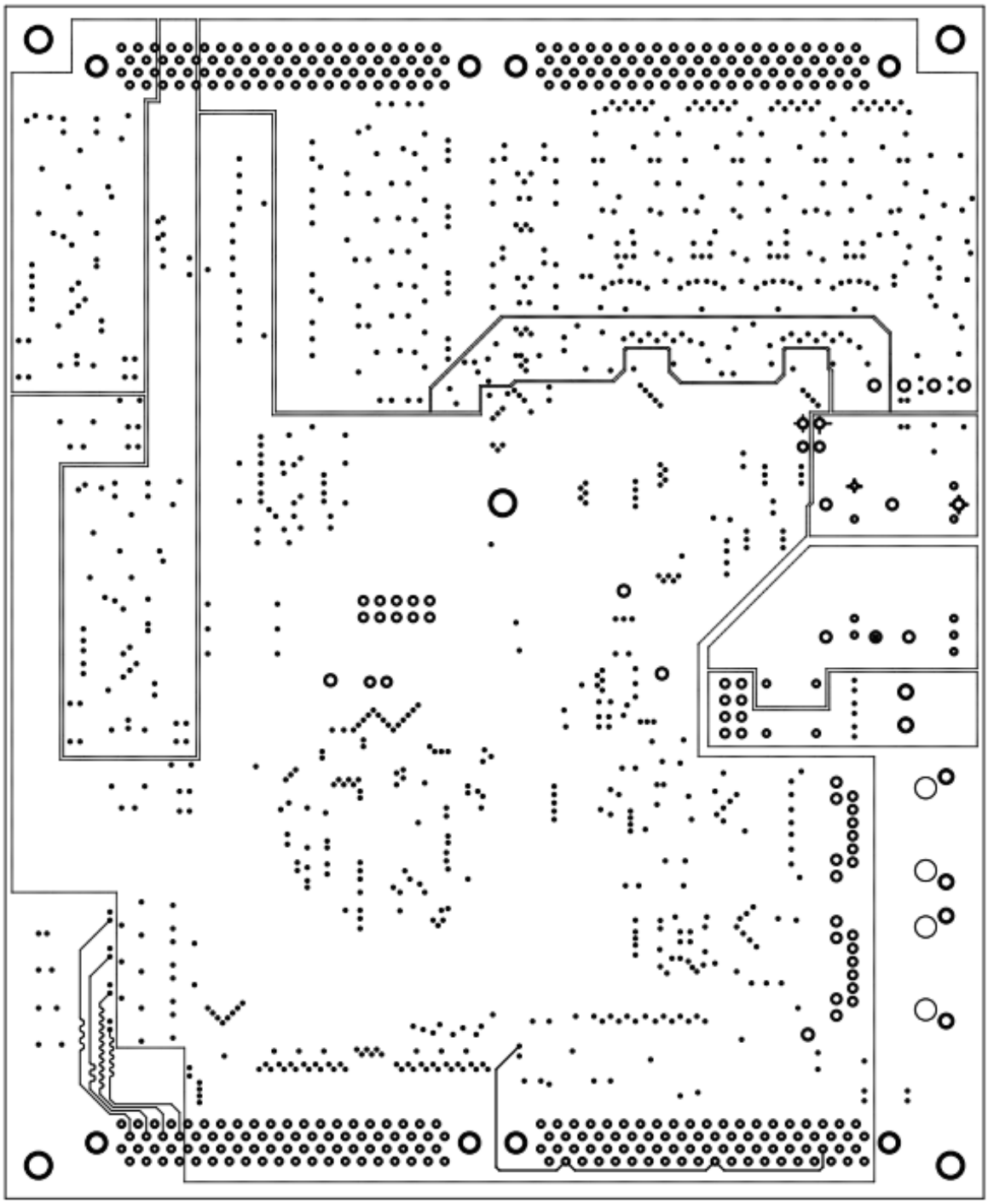

Figure 0-15: IOB-Mk3 L5

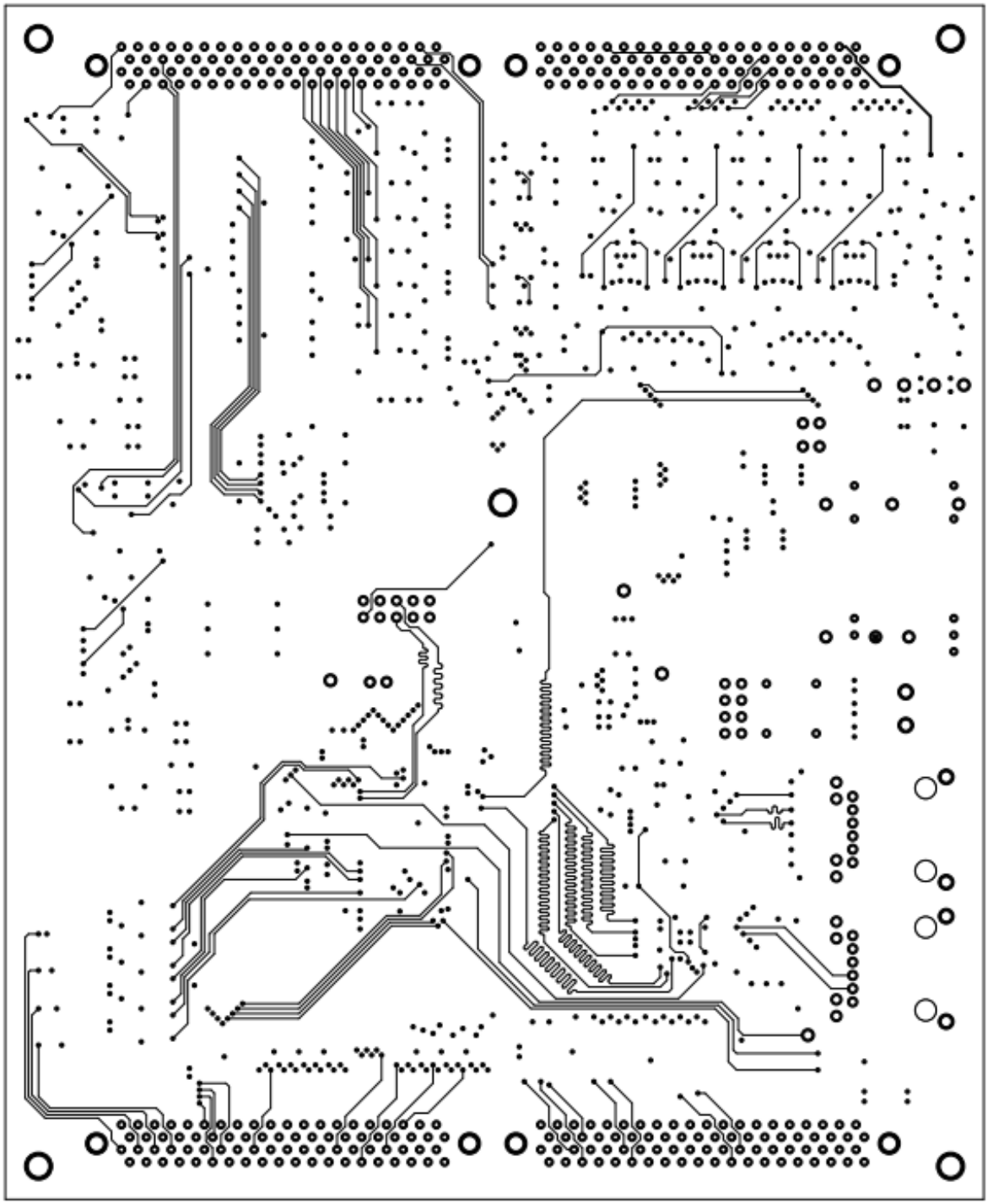

Figure 0-16: IOB-Mk3 L6

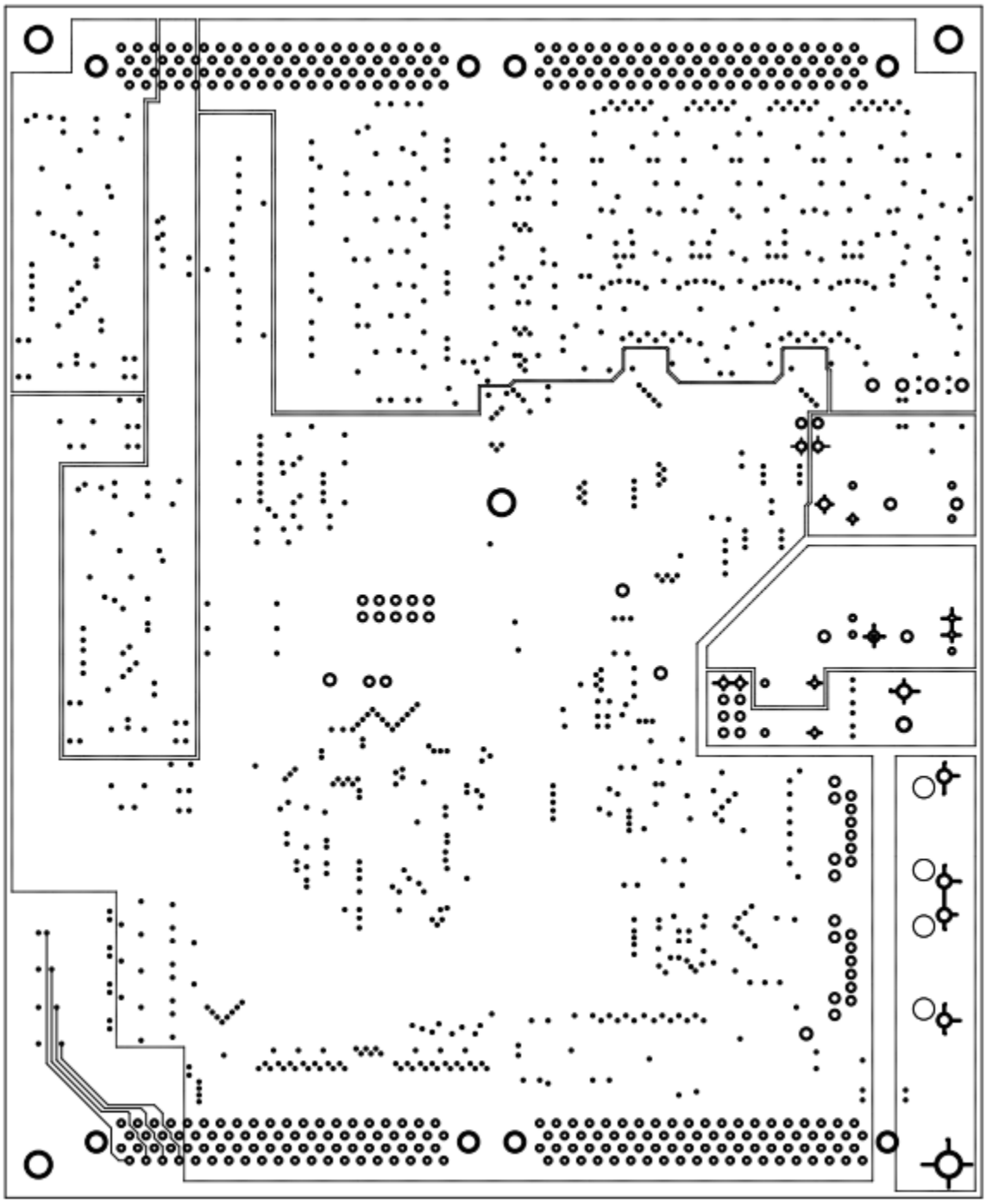

Figure 0-17: IOB-Mk3 L7

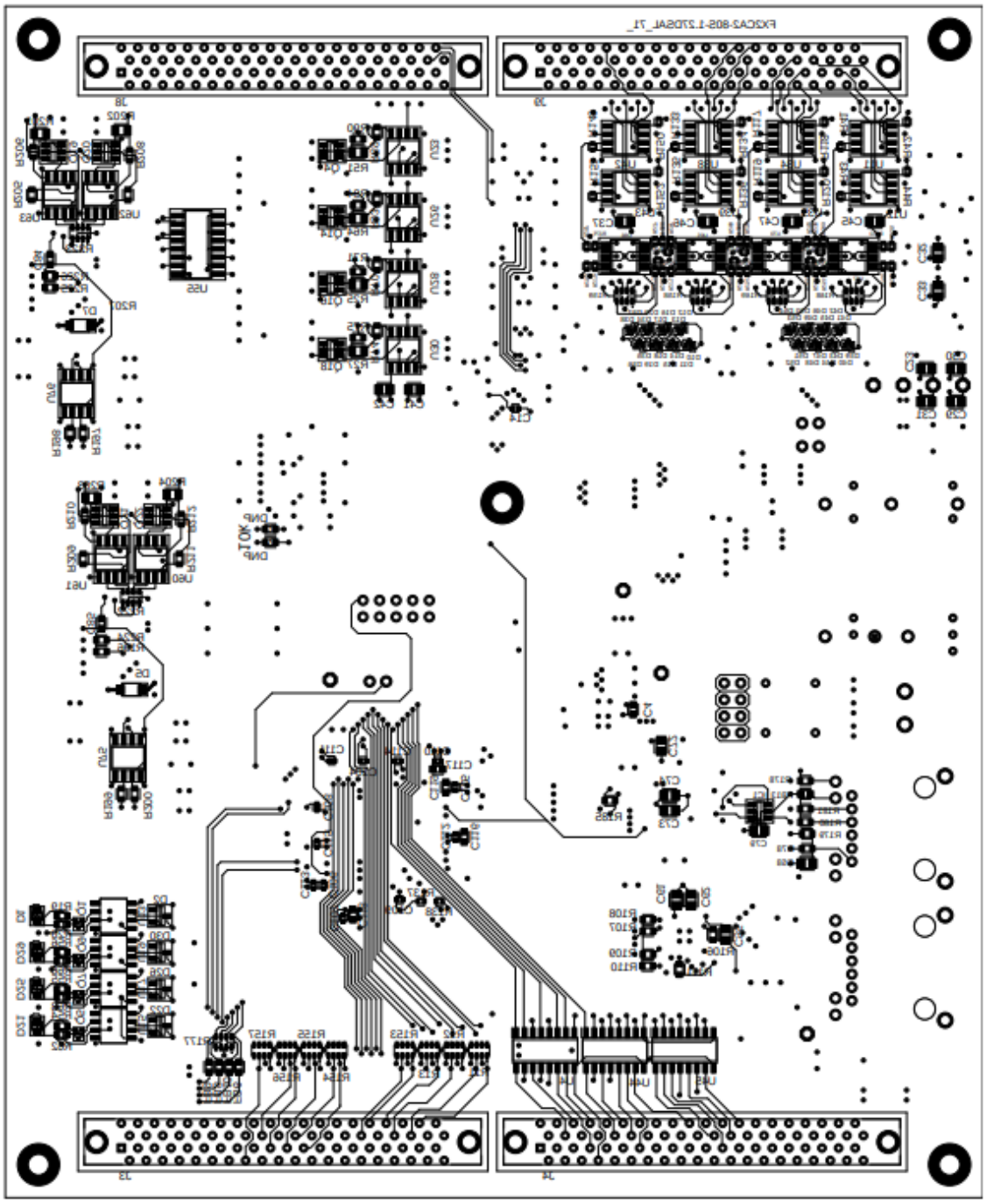

Figure 0-18: IOB-Mk3 L8

F. Certification tests and Documents

Known tests:

- Conducted Voltage Emission (IEC 60945 edition 4)
- Conducted Voltage Emission (DNVGL-CG-0339)
- Radiated Emission
- Immunity to Electrostatic Discharge
- Immunity to Radiated Radio-Frequency Electromagnetic Field
- Immunity to Fast Transients/Burst
- Immunity to Surge test
- Immunity to Conducted Radio-Frequency Electromagnetic Field
- Immunity to Conducted low frequency
- Insulation resistance
- High Voltage Test
- Dry heat cycle
- Damp heat cycle
- Cold Test
- Degrees of protection indicated by second characteristic numeral (IPX1)
- Degrees of protection indicated by first characteristic numeral (IP2X)
- Vibration Test: Sinusoidal
- Compass safe distance
- Extreme power supply
- Excessive condition
- Immunity to power supply failure

Other known standards documents:

- EN 61000-4-2 (2009)
- EN 61000-4-3 (2006)+A1(2008) +A2(2010)
- EN 61000-4-4 (2012)
- EN 61000-4-5 (2006)
- EN 61000-4-6 (2009)
- EN 61000-4-11 (2004)
- EN 55016-2-1 (2009)+A1(2011)
- EN 55016-2-3 (2010)
- EN 60529 (1991)+A1 (2000)
- EN 60068-2-1 (2007)
- EN 60068-2-2 (2007)
- EN 60068-2-6 (2008)
- EN 60068-2-30 (2005)
- ISO 694 (2000)