Design of a 60 GHz Low Noise Amplifier in a 0.13 μm SiGe BiCMOS Process

A thesis by

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Abstract

The Large Hadron Collider (LHC) in CERN outside Geneva in Switzerland is scheduled for an upgrade to improve the luminosity. This upgrade will require higher granularity for the triggering system, increasing the need for very high bandwidth data transfer. This thesis is a part of a feasibility study at the University of Heidelberg regarding the possibilities of using wireless data transfer in the 60 GHz band for data readout on the trigger system. In order to realize 60 GHz data transfer, a fully functional transceiver operating at 60 GHz must be developed. This work covers the design and realization of a low noise amplifier for use in this system.

In order to obtain the required design knowledge, a comprehensive study of microwave theory is performed. This theory forms the basis for designing a low noise amplifier operating at very high frequencies. A summary of the most important theory is also included in this thesis.

A low noise amplifier for use in a 60 GHz transceiver is designed and simulated using National Instruments Microwave Office. Simultaneous impedance- and noise matching is used in order to realize both low noise and low return loss at the same time. The amplifier is designed in a 0.13 µm SiGe BiCMOS process and a layout measuring 0.13 mm^2 is proposed. The resulting low noise amplifier has 9.5 GHz bandwidth, 4.3 dB noise figure, 20.4 dB gain and 9.8 mW power consumption and is within all given specifications. Although the results only show simulated response, we have good reason to believe that these results can be realized by performing a thorough EM simulation and process variation simulation. If this is the case, the resulting amplifier will be very competitive to previously published low noise amplifiers.

Preface

This work was carried out between August 2015 and June 2016 at the University of Bergen, in collaboration with Hans Kristian Soltveit at the Physikalisches Institut, Heidelberg University.

My experience within electronics at the start of the thesis mainly covered low frequency analog electronics and thus microwave engineering was a completely new topic for me. Microwave engineering is a comprehensive subject and a large part of this work was therefore attributed to the learning of RF design.

A fellow student, Hans Schou, which is designing the power amplifier in the same system, is also in the same situation. This has led to a very productive collaboration in learning microwave engineering theory and RF design methods. We have also continuously discussed various RF topics throughout the thesis and assessed specific problems together in order to ensure the quality of the work. Even though we have collaborated with theory, we have carried out an independent work.

Acknowledgments

First and foremost, I would like to thank my supervisor **Kjetil Ullaland** at the University of Bergen for his support and guidance throughout this work.

A special thanks goes to **Hans Kristian Soltveit** for providing the opportunity to work with 60GHz IC design, for sharing his vast knowledge within IC design and for arranging an enjoyable trip to Heidelberg University with both great academic progression and local sightseeing.

I would also like to thank **Yngve Thodesen** at the Royal Norwegian Naval Academy for providing essential guidance within RF-design.

Last but not least, I would like to thank my fellow students for great moments at our office. A special thanks goes to **Hans Schou** for the collaboration throughout the whole year and for the good collegial solidarity.

Contents

CHAPTER 1

Introduction

The Large Hadron Collider (LHC) in CERN outside Geneva in Switzerland is scheduled for an upgrade to improve the luminosity/collision rate. After the upgrade, there will be in average 50 times more proton-proton collisions. The two multi-purpose experiments ATLAS and CMS are therefore facing a big challenge to identify rare physics processes in an immense background of events. A trigger system is used to separate interesting physics processes from the background and in the present detectors the trigger decision is based on information from all sub-detector systems except the tracker. These detectors have limited granularity and after the upgrade it will no longer be able to differentiate physics processes and background. It is therefore interesting to use the tracker data for triggering decision since this detector has the required granularity. There is, however, a challenge in reading the amount of data produced by the tracker in time for the fast trigger decision. The bandwidth required to perform a complete readout of the silicon micro-strip tracker is between 50 and 100 Tb/s. In order to use the tracker in the fast triggering system it is therefore necessary to increase the transfer bandwidth from the tracker or reduce the amount of data or use a combination of both. [2]

This high bandwidth readout has usually been performed using wire based systems or optical links, perpendicularly to the particle path. The weakness of this approach is the size of the connectors and that the cabling is mechanically fragile. In addition to this, the readout is bound to the modularity of the tracker which is not ideal for a fast trigger decision. Wireless data transfer does however not suffer from these problems.

The technical paper *Towards Multi-Gigabit readout at 60 GHz for the ATLAS silicon microstrip detector*[26] describes a system for reading out the data radially using wireless transceivers operating in the 60 GHz band. Figure 1.1 illustrates the idea of wireless radial readout. The bandwidth in the proposed system is much higher

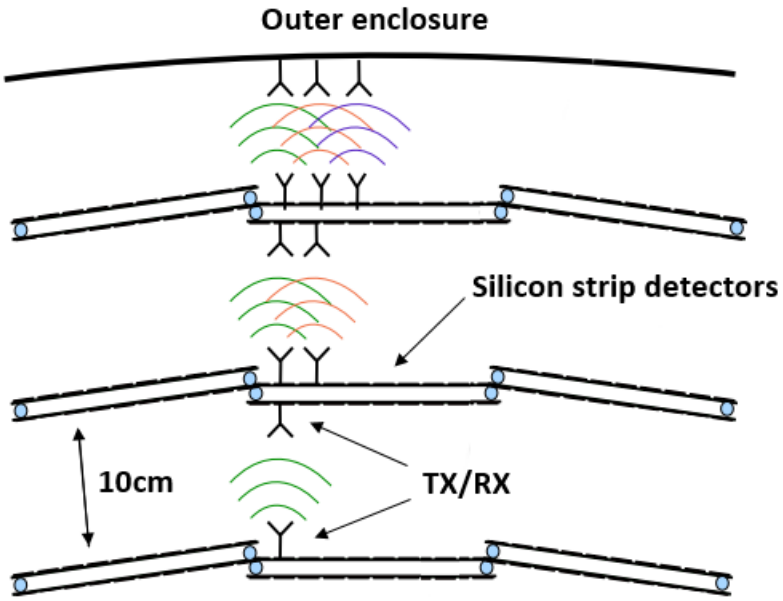


Figure 1.1: Radial readout for the tracker detector of the ATLAS experiment [26].

than the present optical links, the connectors are not needed and the readout can be performed radially instead of perpendicular. [2]

The 60 GHz band provides a spectral bandwidth of $4 - 9$ GHz, which combined with a good modulation scheme would allow for a data rate in the 10's of Gbs [26]. In order to realize this data transfer, a fully functional 60 GHz transceiver must be developed for this purpose. This thesis focuses on the design of a 60 GHz Low Noise Amplifier (LNA) for use in this transceiver.

1.1 System Architecture

Figure 1.2 shows a block diagram of the proposed 60 GHz system. The system consists of two parts, the transmitter and the receiver. The transmitter part comprises of an oscillator which provides the carrier frequency, an on-off-keying (OOK) modulator, a power amplifier and a band pass filter. The band pass filter is necessary in order to suppress broad band noise generated from the PA. The receiver chain consists of a band pass filter, a low noise amplifier, a mixer, an intermediate frequency (IF) amplifier and an OOK demodulator. The low noise amplifier is located behind a band pass filter, which is present to filter out of band interference. The input sensitivity of the LNA must be very high, and it must produce very little noise in order to maintain the integrity of the signal.

Both the transmitter and receiver is to be implemented on a single transceiver chip.

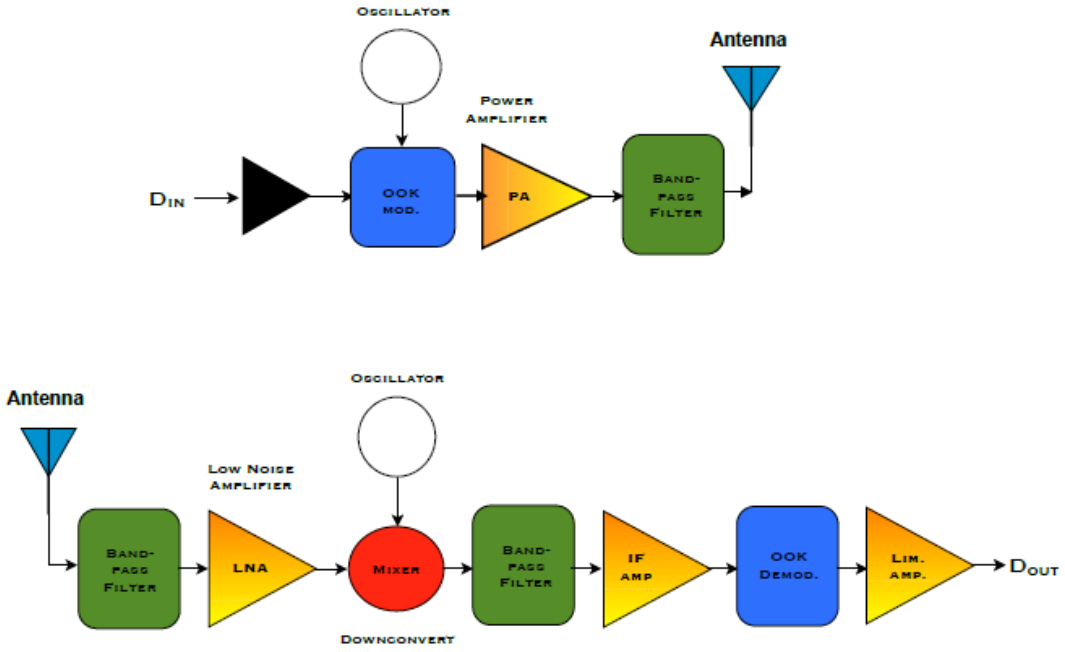


Figure 1.2: Block diagram of proposed 60 GHz system[26]

1.2 60 GHz Band Characteristics

Frequencies from $30-300$ GHz has very short wavelengths ranging from $1-10$ mm and is therefore called millimetre waves. Use of these frequencies has increased in popularity due to technology advances and is today used in several applications. Millimetre wave radars using 77 GHz provides good resolution and small integration size in the automotive industry and is also a key component in future autonomous cars. The millimetre wave based imaging is a different type of radar application where millimetre waves is used in security and surveillance applications to disclose concealed items [30]. In addition, the 60 GHz band provides up to 7 GHz of unlicensed bandwidth. This allows for multigigabit short range wireless transfer in many applications. Figure 1.3 shows the unlicensed band for different regions.

The 60 GHz frequencies have several properties beneficial for short range communication. One of the properties is the atmospheric attenuation caused by the absorption of microwave energy in molecular oxygen. Maximum absorption occurs when the frequency is equal to one of the resonance frequencies of the water vapor or molecular oxygen[22]. This absorption is peaking at 60 GHz, making long range communication with 60 GHz unsuitable. Since the range of transmission in our system is well below 1 m, this attenuation will not influence the signal noteworthy. It does however ensure that radio waves from other interfering 60 GHz sources is well attenuated.

Another benefit of the 60 GHz band for this specific purpose is the high attenuation

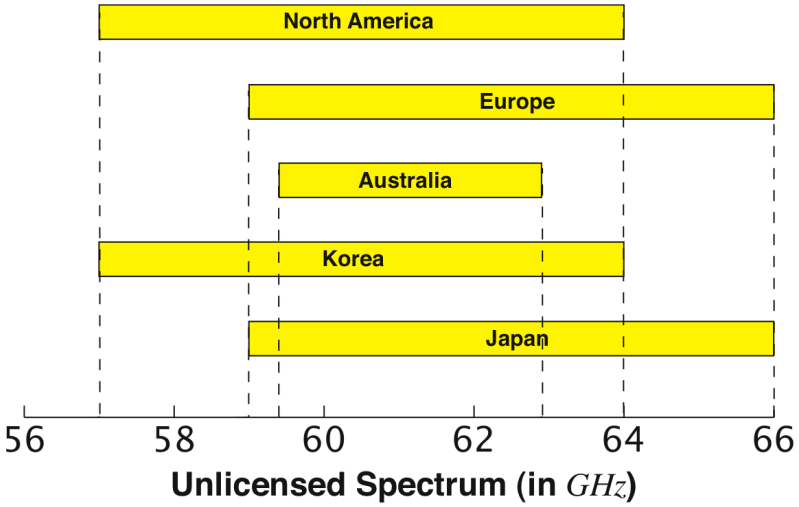


Figure 1.3: Unlicensed spectrum for 60 GHz band. [6]

through silicon detectors. The wide bandwidth also allows for a simple and low spectrum efficiency modulation scheme.

1.2.1 60 GHz transmission

Figure 1.4 shows a basic radio system where P_t is the transmit power, G_t is the transmitter antenna gain, G_r is the receiver antenna gain, P_r is the power delivered to the matched load and R is the distance between the antennas.

The delivered power is described by the *Friis formula* given in equation 1.1 [22].

$$P_r = \frac{G_t G_r \lambda^2}{(4\pi R)^2} P_t \tag{1.1}$$

The received power is highly dependent on the distance between the antennas as well as the frequency. The transmitted power is distributed isotropically, causing the power to drop over distance since the transmitted power musts cover a larger area corresponding to a growing sphere. The $\frac{1}{4\pi R^2}$ term is due to this power loss. The frequency dependency is not because of the signal getting attenuated in free space, but rather due to a definition that the antenna is unity gain. Antenna size is dependent on the frequency. The lower the frequency is, the larger the antenna is. A larger antenna would be able to cover a larger area and hence the energy collection is better. This leads to the frequency dependency, λ^2.

A useful measure of the attenuation in free space is the free space path loss (FSPL). This is basically the ratio of the transmitted power and received power with unity gain antennas. For a signal in the 60 GHz band this would lead to the following loss

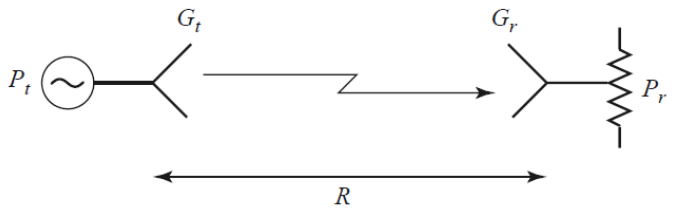


Figure 1.4: Basic radio system[22]

for one meter:

$$FSPL = \left(\frac{4\pi d}{\lambda}\right)^2 = \left(\frac{4\pi \times 1\text{m}}{5\text{mm}}\right)^2 = 68\text{dB} \tag{1.2}$$

1.3 Goal of This Thesis

The goal of this thesis is to design and simulate a low noise amplifier for use in the 60 GHz transceiver ASIC. In addition, a layout should be made and eloectromagnetic (EM) simulations performed to ensure that parasitics are accounted for. The performance of the LNA must satisfy the specifications given by Table 1.1.

The bandwidth is defined by the region where S_{11} and S_{22} is below -10 dB, although this measure is somewhat conservative. The gain should be as flat as possible within the bandwidth without sacrificing power consumption and fall below 0 dB as quickly as possible. Both gain and noise is specified for the center frequency, 61.5 GHz. The input and output is to be matched towards 50 Ω, since the bonding method and antenna configuration is not yet decided.

Specification	**Value**	**Unit**
Bandwidth	57-66	GHz
Input sensitivity	-100 to -30	dBm
S_{21}	≥ 20	dB
Noise Figure	≤ 5	dB
Power Consumption	≤ 12	mW
S_{11}	≤ -10	dB
S_{22}	≤ -10	dB

Table 1.1: LNA specifications.

1.4 Thesis Outline

This section provides an overview over the different chapters in the thesis.

Chapter 2 - Microwave theory Provides basic theory related to transmission lines and RF circuit design for better understanding of this thesis.

Chapter 3 - Process technology Brief introduction to different RF processes and the SG13S process.

Chapter 4 - Low noise amplifier design methodology Theory related to low noise amplifier design.

Chapter 5 - Design and simulation A detailed description of the whole design procedure as well as pre-layout simulations.

Chapter 6 - Design Realization and Layout Realization of design with real components and design of layout. Post-layout simulations.

Chapter 7 - Discussion The results of the design is discussed.

Chapter 8 - Conclusion A conclusion is made based on the results of this work.

CHAPTER 2

Process Technology

This chapter includes a description of the chosen process technology as well as some theory related to the transistors and process. In addition to this, a brief explanation of some common RF processes are made.

2.1 III-V Devices

Silicon (Si) devices are well suited to high-transistor-count, high-volume production of microprocessors, memory applications and general purpose ICs. Although Si is the most used semiconductor it has small electron and hole mobility as well as relatively low saturation velocity, compared to other processes. RF and microwave circuit applications places high performance demands and thus Si may provide insufficient performance for these applications. Many of the compound semiconductors[1] from group III and V provides far better mobility and saturation velocities. GaAs and InP are two semiconductor compounds that are widely used whereas GaAs is often used in RF circuits. In addition to the improved speed, the bandgaps of III-V devices are easily altered for specific needs. This atomic-level customization of the semiconductor is called *bandgap-engineering*. [5]

One of the drawbacks of III-V devices is that the yield is lower than for standard Si technologies[5]. In addition to this, the thermal conduction is poorer. The result is that the production is more difficult causing more expenses. In order to overcome these drawbacks, SiGe was utilized to allow for bandgap-engineering in the Si material system.[5]

[1] A compound semiconductor is made of elements from two or more different groups of the periodic table.

2.2 SiGe Heterojunction Bipolar Transistors

A *heterojunction* is a *pn* junction made of two different materials [11]. In contrast, a regular bipolar *homojunction* transistor uses the same material in both the *p*-type and *n*-type regions. In the 0.13 µm SiGe process the transistors are heterojunction with silicon *n*-type region and germanium *p*-type region (the base of the transistor). Usually 10-20% of the atoms in the silicon crystalline in the base are replaced with Ge atoms.

By adding Ge to the base one can change the bandgaps of the two junctions. Ge has lower bandgap than Si and by forming a SiGe compound in the base, the bandgap for this region can be decreased [11]. The relatively large bandgap in the emitter is used to prevent holes from being injected from the base to the emitter and therefore the current gain, β, gets higher since the base current is lower in theory. In addition to this it is now possible to dope the base region more heavily and reduce the base width compared to a normal BJT. This decreases the transit time and base capacitance, without making the base resistance larger. The net result is that f_T increases, making the HBT more beneficial for high frequency applications compared to a normal BJT. [10]

SiGe HBTs can also be easily adapted with Si CMOS to form a monolithic SiGe HBT BiCMOS technology [5]. Compared to a normal CMOS process, the typical SiGe process has a mask addition of approx. 20%. This means that there will be an increase of approx. 20% in process manufacturing steps. This is often considered as an acceptable compromise between performance benefit and cost[5].

2.3 SG13S Process Specification

The process technology chosen for realization of the transceiver is the SG13S process from IHP (Innovations for High Performance Microelectronics). SG13S is a high performance 0.13 µm BiCMOS process. The process includes SiGe npn-HBTs with f_T and f_{max} up to 250GHz and 340GHz respectively. This makes the process ideal for applications in the higher GHz bands.

This section includes basic information about the SG13S process. The process specification is IHP confidential proprietary and thus the details provided in this work is published online at the IHP website[13].

The SG13S process provides 7 layers of aluminum metal whereas two of the layers are thick top-metal layers. These top-metal layers are intended for design of passives e.g. inductors and transmission lines in order to reduce the resistance and parasitic capacitance. In addition to this, a special MIM layer is available for MIM capacitors. Each metal layer is separated by a layer of Silicon-dioxide.

Figure 2.1 shows a cross-section of the SG13S process.

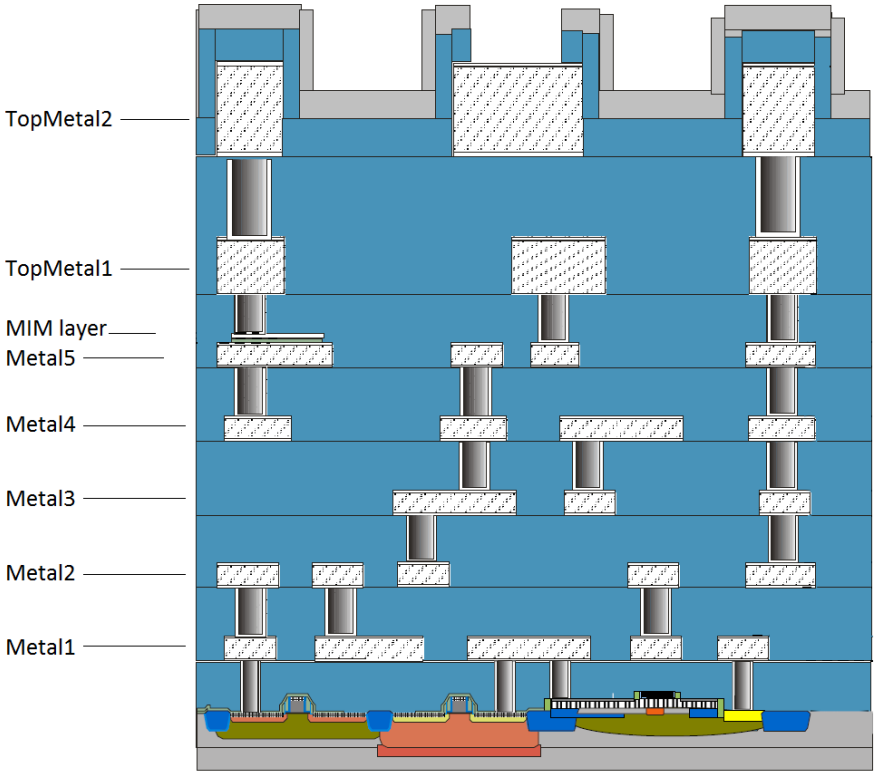


Figure 2.1: Cross-section of SG13S process (not to scale) [12]

2.3.1 SG13S NPN Transistors

SG13S provides three different HBT transistors, npn13p, npn13pl2 and npnv2. npnv2 is a high voltage transistor with a relatively low f_T. npn13p and npn13pl2 have comparable f_T but differs in the way the layout is made. npn13p utilizes a BEC layout while npn13pl2 utilizes a CBEBC layout. These two configurations are shown in Figure 2.2. Table 2.1 shows the performance of the npnpl2 transistor.

BEC layout was historically preferred by IHP, but the CBEBC layout was included in the 0.13µm process due to the fact that users of other technologies are used to CBEBC layout. In addition to this, CBEBC layout is mandatory for the high voltage npn and thus implementing the CBEBC layout for the high performance transistor is easy. (G. Fischer, IHP, private communication, 01.12.2015)

The BEC layout has the disadvantage that the base resistance gets high when the emitter length increases. This will lower the f_{max}. For high power design one should therefore use many emitters in parallel. npn13p is available in two lengths, 0.48µm

Parameter	npn13p
A_E	0.12×0.48 µm^2
Peak f_{max}	340
Peak f_T	250
BV_{CE0}	1.7
BV_{CB0}	5
β	900

Table 2.1: SG13S npn13pl2 bipolar performance

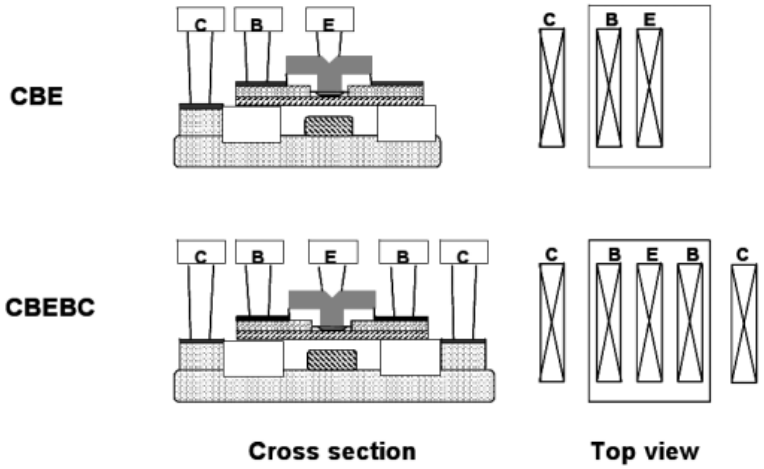


Figure 2.2: BEC vs CBEBC layout [15]

and 0.84µm.

2.3.2 SG13S Passive Components

SG13S provides models for MIM capacitors, planar spiral inductors and poly silicon resistors.

Metal-insulator-metal (MIM) capacitors are formed between Metal 5 and a special MIM layer located above Metal 5. The distance between the two metal layers is very short and thus it is possible to gain high values of capacitance.

Inductors are not well documented in the process specification, but IHP provides a model for an octagonal planar spiral inductor. The inductor is formed on top-metal 2 with contacts on top-metal 1. The minimum inductance provided by these inductors is approx. 120 pH, making it unsuitable for use in very high frequency designs e.g. 60 GHz.

SG13S provides three different types of resistors with sheet resistances ranging from low to high. These are listed in Table 2.2.

Resistor	**Sheet Resistance**	**Resistor material**
Rsil	-	N+ poly resistor
Rppd	250 Ω	P+ poly resistor
Rhigh	1300 Ω	High Poly Resistor

Table 2.2: SG13S resistors

CHAPTER 3

Microwave Theory

This chapter will provide basic theory related to transmission lines and RF circuit design for better understanding of this thesis. The theory is mainly based on subjects found in [21], [22] and [18].

3.1 Transmission Lines

Standard circuit analysis requires the assumption that the physical dimension of the network is much smaller than the wavelength of the electrical signal. This means that the amplitude and phase is unchanged through the whole network. For a transmission line where the electrical wavelength is comparable[1] to or shorter than the length of the line, this assumption is no longer true. The amplitude and phase can now vary along the transmission line, as a consequence of finite speed of wave propagation.

Transmission line elements with a finite physical length are thus called *distributed elements* while elements with negligible physical dimensions are called *lumped elements*.

The transmission line can be represented by a lumped element model shown in figure 3.1. The model represents a small fraction of the whole transmission line, and a complete transmission line consists of several cascaded lumped element models.

L is the series inductance represented by self inductance of the conductors. C is the shunt capacitance, caused by the close proximity of the conductors. R and G represent losses due to the series resistance of the conductor, R, and the dielectric

[1] Generally considered to be $\frac{\lambda}{10}$ [28]

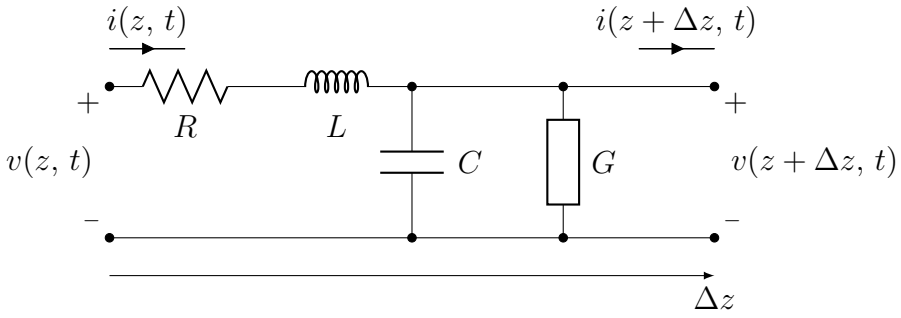


Figure 3.1: Lumped element model of a small fraction of a transmission line.

losses in the material between the conductors, G.

By using kirchoff's voltage law and solving the differential equations, it can be shown that the traveling wave solutions for a transmission line is[21]:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}, \tag{3.1}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}. \tag{3.2}$$

where the $^+$ and $^-$ label denotes respectively the incident wave and the reflected wave. γ is the propagation constant given by equation 3.3:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{3.3}$$

The real part, α, is called the *attenuation constant*, while the imaginary part, β, is called the *phase constant*.

In the traveling wave solution, the $e^{-\gamma z}$ term represents the wave propagation in the $+z$ direction while the $e^{\gamma z}$ term represents the wave traveling in the $-z$ direction. In other words, both the incident wave and the *reflected* wave is represented in the traveling wave solution. Reflection of a traveling wave is a transmission line phenomenon that will be further discussed in section 3.1.2.

3.1.1 Characteristic Impedance

The characteristic impedance Z_0 of a lossy transmission line is given by equation 3.4 [21]. The definition of this impedance is based on the ratio of the positive and negative traveling voltage and current wave. Therefore, Z_0 is not an impedance in the conventional circuit sense.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \frac{V_0^+}{I_0^+} = \frac{V_0^-}{I_0^-} \tag{3.4}$$

For a lossless transmission line, this simplifies to equation 3.5.

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3.5}$$

Note that the characteristic impedance is no longer frequency dependent when the transmission line is lossless.

3.1.2 Transmission Line Reflections

When a incident wave initially travels down a transmission line, the voltage to current ratio must satisfy the characteristic impedance. However, when the transmission line is terminated with an impedance not equal to the characteristic impedance, the voltage to current ratio will no longer satisfy the load impedance. Therefore a reflected wave must be generated at the load to satisfy this condition.

The voltage ratio of the reflected wave to the incident wave is called the reflection coefficient, and is denoted by Γ, given by equation 3.6 [21].

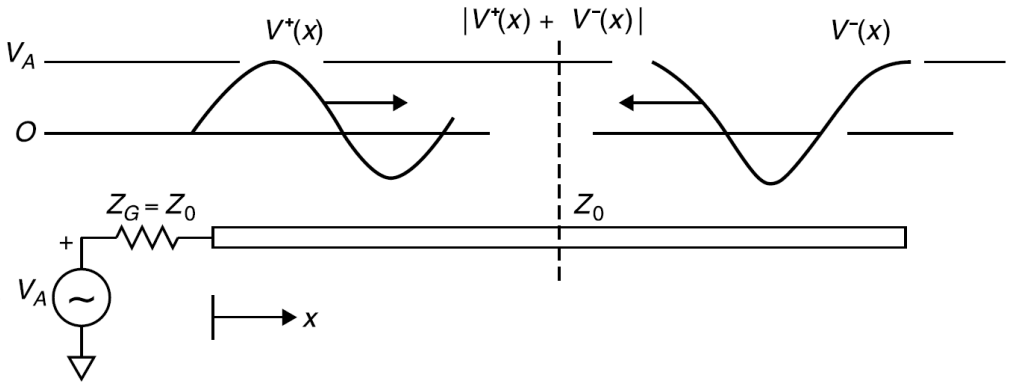
$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.6}$$

Figure 3.2a shows how a sinusoidal wave travels on a open-circuit terminated transmission line. The incident wave, V^+, is reflected at the end of the line, due to the impedance mismatch, causing a reflected wave, V^-. This reflected wave will sum with the incident wave and distort the transmitted signal. Since the source resistance is equal to the characteristic impedance, all the energy from the reflected wave will then dissipate in the source.

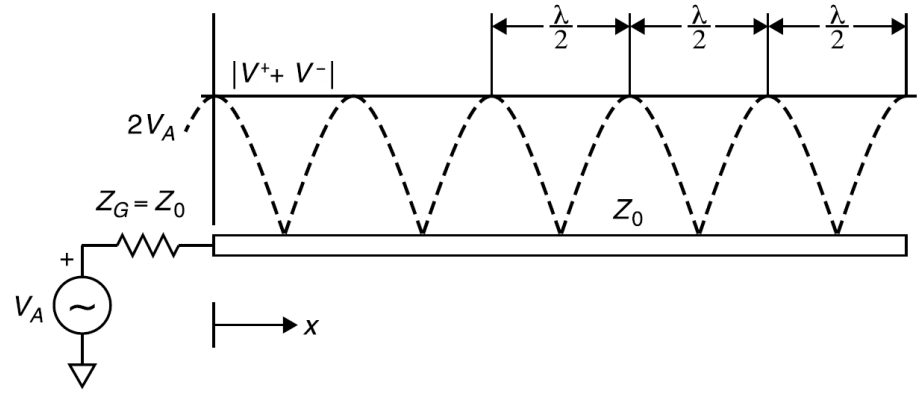
When the length of the transmission line is a multiple of $\frac{\lambda}{2}$, standing wave patterns will form as shown in 3.2b. Since the incident wave is in phase with the reflected wave, the amplitude is doubled at their maxima. The maxima and minima are separated by a half wavelength due to the doubling of their relative velocities resulting from their opposite directions of travel [28].

By sizing the load resistance equal to the characteristic impedance, one can eliminate the reflections by making $\Gamma = 0$. We then obtain what is called a *matched* load.

Although the reflections is unwanted in most situations, one can purposely introduce reflections in order to provide impedance matching. This is is called *impedance matching with distributed elements* and is discussed further in Section 3.6.2



(a) Incident and reflected wave on open-circuit terminated line.



(b) Standing waves on a transmission line.

Figure 3.2: Behaviour of traveling waves on an open-circuit terminated transmission line. [28]

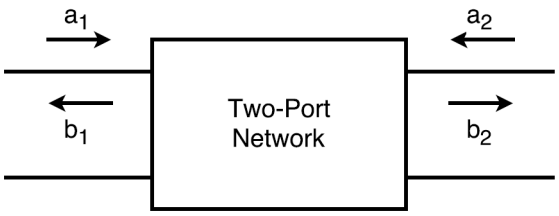


Figure 3.3: Convention for defining S-parameters.

3.1.3 Wavelength in a dielectric

The velocity of a wave propagating with air as dielectric is very close to the speed of light in vacuum. This is due to the relative permittivity of air which is ≈ 1. The velocity and thus the wavelength of the wave propagating is reduced when traveling in a dielectric material with higher than 1 relative permittivity. This relationship is given by Equation 3.7 [28]:

$$\lambda = \frac{v}{f\sqrt{\epsilon_R}}, \tag{3.7}$$

where ϵ_R is the relative permittivity of the material.

3.2 Scattering Parameters

Scattering parameters or *S-parameters* are commonly used to characterize a two-port network in RF circuit design. The reason for not using the traditional two-port parameters is the fact that in order to determine the parameters one would need to short or/and open the input and output of the two-port network. This is not preferable due to several reasons. For instance, a wire from a short may introduce a significant amount of inductance, and an open circuit can load the output with a significant amount of capacitance. Both instances may cause failure of the correct conditions for determining the traditional two-port parameters. Another aspect is that a short or/and open circuit will cause reflections of the traveling waves. By using S-parameters it is possible to characterize the two-port network without requiring unachievable terminal conditions. [18]

Figure 3.3 shows the convention for s-parameters. Each port has two parameters, a_n and b_n. a_n represents the wave traveling towards the network. b_n represents the wave traveling away from the network. All parameters are normalized by the characteristic impedance, Z_0.

The S-parameter matrix for a two port network are as follows [18]:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.8}$$

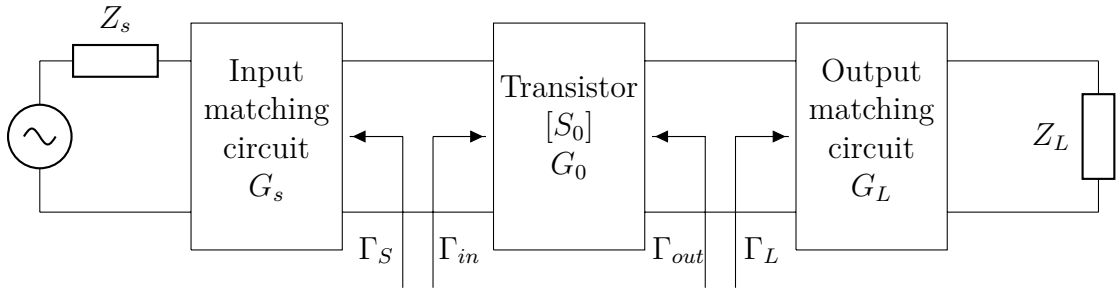


Figure 3.4: General two-port amplifier

where the terms are

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \equiv \frac{\text{reflected power wave at port 1}}{\text{incident power wave at port 1}} \tag{3.9}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \equiv \frac{\text{Transmitted power wave at port 2}}{\text{incident power wave at port 1}} \tag{3.10}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \equiv \frac{\text{reflected power wave at port 2}}{\text{incident power wave at port 2}} \tag{3.11}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \equiv \frac{\text{Transmitted power wave at port 1}}{\text{incident power wave at port 2}} \tag{3.12}$$

$a_2 = 0$ and $a_1 = 0$ conditions assumes that no power waves are returned to the network. These conditions requires that the transmission lines are terminated with the characteristic impedance.

By looking at equation 3.9 we immediately see that this must be the reflection coefficient for the input side, Γ_{in}. Equation 3.11 is the reflection coefficient for the output side, Γ_{out}. Equation 3.10 and 3.12 represents respectively the forward power gain and the reverse power gain.

3.3 Two-port Power Gain

Figure 3.4 shows a general two-port amplifier with input and output matching network.

G_S and G_L represents the *gain* due to impedance mismatches between the transistor and the source and load impedance whereas G_0 is the transistor gain.

There are several definitions of power gain in a two-port system. The distinction between the different definitions are primarily in the way the input and output are

matched.

The different types of gain are defined as follows:

$$\text{Power Gain} = G = \frac{P_L}{P_{in}} \tag{3.13}$$

Power gain is the ratio of the power dissipated in the load Z_L to power delivered to the input of the two-port network. This gain is independent of Z_S. [21]

$$\text{Available Gain} = G_A = \frac{P_{avn}}{P_{avs}} \tag{3.14}$$

Available gain is the ratio between the available power from the two-port network to the power available from the source. This assumes conjugate matching of both the source and the load, and depends on Z_S but not Z_L. [21]

$$\text{Transducer power gain} = G_T = \frac{P_L}{P_{avs}} \tag{3.15}$$

Transducer Power Gain is the ratio of the power delivered to the load to the power available from the source. This depends on both Z_S and Z_L. [21] This dependency makes G_T a very useful gain, since it accounts for mismatches in both the source and load.

If both the input and output are conjugately matched to the two-port, the gain is maximized and $G = G_A = G_T$.

3.4 Two-port Noise Parameters

The noise performance of a two-port is usually specified by the *noise factor*, F, or the noise figure, NF, where the noise figure is simply $10\log(F)$ [17]. The noise factor is defined as

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}}. \tag{3.16}$$

The noise factor is a measure of the degradation in signal-to-noise ratio for the system and thus for a noiseless system the noise factor will be unity.

Figure 3.5 shows a noiseless two-port with a source admittance, Y_S and the corresponding noise source, I_S. The net effect of all internal noise sources can be modeled as two external noise sources, e_n and i_n. This is a huge advantage and simplifies the noise calculations significantly as long as we are only interested in the overall noise performance. This will also allow for rapid evaluation of how the source admittance affects the overall noise performance.

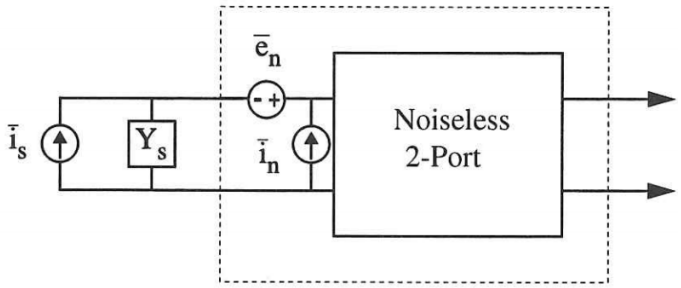


Figure 3.5: Two-port system with external noise sources [17].

Lee [17] describes how the noise parameters for a two-port system is derived. The noise factor for the two-port system in figure 3.5 is given by equation 3.17:

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_S e_n|^2}}{i_s^2} \tag{3.17}$$

Notice that the noise from the source admittance is not correlated with the noise from the two-port. Both sources from the two-port are however assumed correlated. This may not be the case, and to accommodate the possibility for uncorrelated noise, i_n is expressed as the sum of both correlated and uncorrelated noise:

$$i_n = i_c + i_u \tag{3.18}$$

i_c is correlated with e_n, and hence i_c can be treated as proportional to e_n:

$$i_c = Y_c e_n \tag{3.19}$$

Y_c is defined as the *correlation admittance* since $\frac{i_n}{e_n}$ is an admittance.

By combining Equation 3.17, Equation 3.18 and Equation 3.19 the noise factor is expressed by the following equation:

$$F = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{e_n^2}}{i_s^2}. \tag{3.20}$$

Equation 3.20 contains three independent noise sources. These noise sources can be treated as thermal noise produced by an equivalent resistance or conductance:

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f}, \tag{3.21}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f}, \tag{3.22}$$

$$G_s \equiv \frac{\overline{i_s^2}}{4kT\Delta f}. \tag{3.23}$$

By decomposing each admittance into both conductance, G, and suscpetance, B, and by using Equation 3.21, 3.22 and 3.23, we can rewrite the noise figure equation:

$$F = 1 + \frac{G_u + \Big((G_c + G_s)^2 + (B_c + B_s)^2\Big)R_n}{G_s}. \tag{3.24}$$

3.4.1 Optimum source admittance

Once the expression for the noise factor has been established, a determination of the general conditions for minimum noise factor is necessary. By taking the first derivative of Equation 3.24 with respect to the source admittance and setting this to zero we obtain the following expressions:

$$B_s = -B_c = B_{opt}, \tag{3.25}$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt}. \tag{3.26}$$

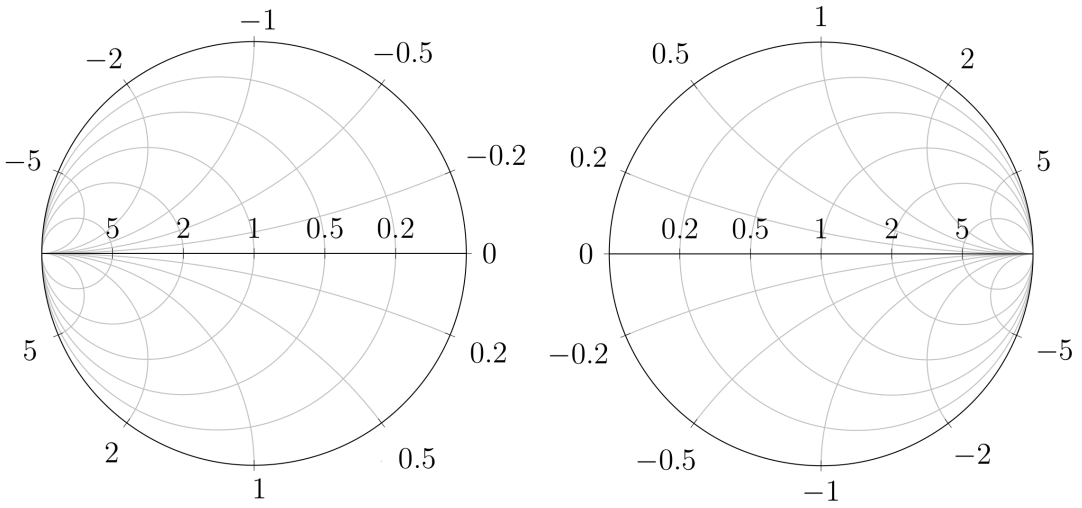
For minimum noise factor, the source susceptance should be made equal to the negated correlation susceptance. The source conductance should also fulfill the conditions of Equation 3.26. Thus, for a low noise design great care should be taken in designing the circuit to provide $G_{opt} = G_s$.

Notice that minimizing noise does not necessarily give maximum power transfer and hence there will usually be a gain vs. noise trade-off. There are for example no reason to expect that the correlation susceptance is equal to the negated input source susceptance.

Choosing $Y_s = Y_{opt}$ would result in a minimum noise factor, defined as F_{min}. The noise factor can thus be expressed in terms of F_{min}[21]:

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2. \tag{3.27}$$

R_n applies as a multiplier in front of the second term in Equation 3.27. For a fixed source admittance, R_n tells something about the relative sensitivity of the noise figure when deviating from the optimum noise conditions. When R_n is of large magnitude, the sensitivity gets higher and thus the noise conditions is more difficult to optimize [17].



(a) Admittance smith chart **(b)** Impedance smith chart

Figure 3.6: Plotting constant values

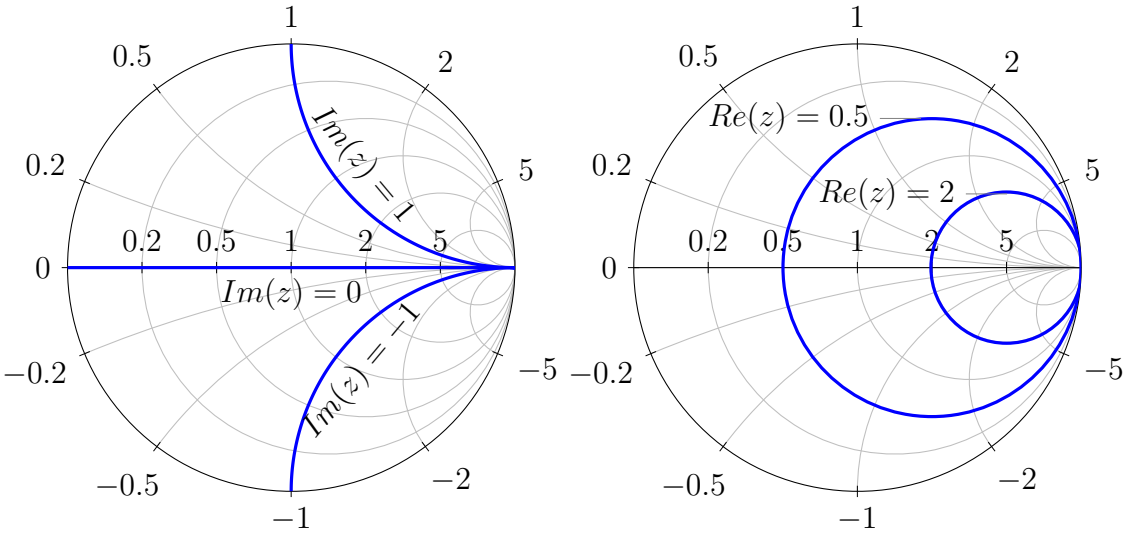
3.5 Smith Chart

Phillip H. Smith developed the Smith chart in the 1930s as an easy and intuitive display of the reflection coefficients as well as the line impedance in one single graph[18]. The Smith chart is essentially just a polar plot of the voltage reflection coefficient, Γ. The polar plot is overlayed with an impedance and/or admittance grid. The impedance/admittance is normally referenced to a normalized 1Ω characteristic impedance.

Figure 3.6 shows both the admittance and the impedance smith chart.

The Smith chart has a circumferential scale expressed in both degrees and wavelengths. The wavelength scale represents a distance along the transmission line and is used with distributed components. The degree scale represents the angle of the reflection coefficient at a specific point. The resistance and reactance is represented by values along circles (reactance) and arcs (resistance). As an example a constant resistance will transform to a circle. Similarly, a constant reactance will transform into an arc. Figure 3.7 shows an example of some constant reactances and resistances plotted.

There are some properties that are worth discussing. The left and right corners of the horizontal line corresponds to respectively $\Gamma = -1$ and $\Gamma = 1$. In therms of impedance, this corresponds to a short ($Z_{in} = 0$) or open circuit ($Z_{in} = \infty$). The center point corresponds to a perfect match leading to $|\Gamma| = 0$. Figure 3.8 shows these locations. Further on, the top half of the diagram corresponds to the inductive region. Thus the lower half is the capacitive region.



(a) Plotting a constant reactance **(b)** Plotting a constant resistance

Figure 3.7: Plotting constant values

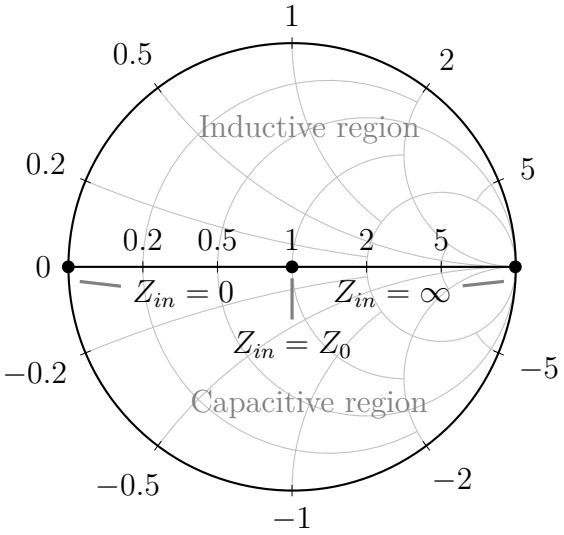


Figure 3.8: Regions of the Smith diagram

The relationship between the reflection coefficient, Γ, and the input impedance (plotted impedance) is given by Equation 3.28 [16]:

$$Z_{in} = Z_0 \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} \tag{3.28}$$

3.5.1 Constant-Gain Circles

Gain circles utilizes the Smith chart to provide a graphical aid in designing an amplifier for a specific gain. This is practical in cases where one would need a specific gain or when gain is traded for improved noise figure, bandwidth etc. The design procedure is facilitated by plotting circles of constant gain in the smith chart. When a specific gain is needed for either the input section or output section (G_S or G_L), impedance mismatches are purposely introduced by placing Γ_S or Γ_L along the circle of interest.

It can be shown that the center and radius for the input section gain circle is expressed by the following equations[21]:

$$C_S = \frac{g_S S_{11}^*}{1 - (1 - g_S)|S_{11}|^2}, \tag{3.29}$$

$$R_S = \frac{\sqrt{1 - g_S}(1 - |S_{11}|^2)}{1 - (1 - g_S)|S_1 1|^2}. \tag{3.30}$$

Likewise, the center and radius for the output section is expressed by the following equations:

$$C_L = \frac{g_S S_{22}^*}{1 - (1 - g_L)|S_{22}|^2}, \tag{3.31}$$

$$R_L = \frac{\sqrt{1 - g_L}(1 - |S_{22}|^2)}{1 - (1 - g_L)|S_2 2|^2}. \tag{3.32}$$

where g_S and g_L are the normalized gain factors expressed by:

$$g_S = \frac{G_S}{G_{S_{max}}} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2}(1 - |S_{11}|^2), \tag{3.33}$$

$$g_L = \frac{G_L}{G_{L_{max}}} = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}(1 - |S_{22}|^2), \tag{3.34}$$

Figure 3.9 shows a noise circle plotted in the smith chart. Usually one would plot several circles to get a graphical overview of the gain trade-off. Placing Γ_S along the circle of interest would produce a specific amount of gain whereas placing it within the circle would produce more than the specified gain.

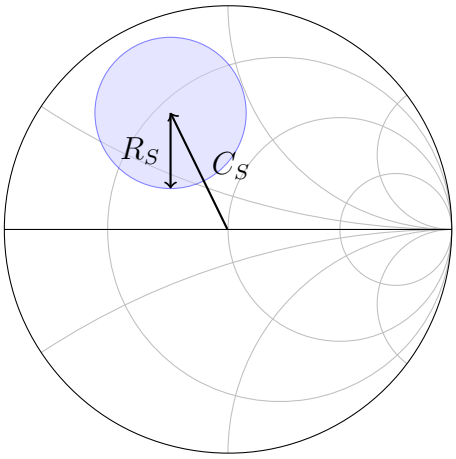


Figure 3.9: A Smith chart with a gain circle for the input section plotted

Notice that these expressions is in the case of a unilateral device. This is normally not the case and thus the error caused by approximating $|S_{12}| = 0$ must be assessed before evaluating the gain circles. Unilateral figure of merit is explained in Section 3.5.2.

These gain expressions are given explicitly for the input and output section and are thus not usable for assessing the available gain. Available gain circles are however often available in CAD tools.

3.5.2 Unilateral Figure of Merit

The design approach for constant gain discussed in section 3.5.1 assumes that the reverse gain, S_{12}, is zero. This is usually not the case and thus the error introduced by the actual value of S_{12} must be assessed. The unilateral figure of merit provides a method for quantifying this error, and is given by Equation 3.35.

$$U = \frac{|S_{12}||S_{21}||S_{22}||S_{11}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}. \tag{3.35}$$

This figure of merit should be as small as possible in order to use the unilateral design procedure. Usually an error of a few tenths of a dB or less will justify the unilateral assumption[21].

3.5.3 Constant-Noise Circles

As previously discussed in section 3.4.1 there is an optimum source admittance that produces a minimum amount of noise, F_{min}. This optimum source admittance can also be expressed as an optimum reflection coefficient, Γ_{opt} [21].

$$Y_{opt} = \frac{1}{Z_0}\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}}. \tag{3.36}$$

By using this relationship together with Equation 3.27 it can be shown that it is possible to define circles of constant noise in the smith chart[21]. The center of this circle is defined as:

$$C_F = \frac{\Gamma_{opt}}{N+1}, \tag{3.37}$$

where the radii is given by

$$R_F = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1}. \tag{3.38}$$

The noise figure parameter, N, is defined by Equation 3.39:

$$N = \frac{F-F_{min}}{4\frac{R_N}{Z_0}}|1+\Gamma_{opt}|^2. \tag{3.39}$$

These circles can be used as a graphical aid when designing amplifiers. By using the design specifications one can plot constant noise circles for specified noise levels. To design for a specific noise level one would then place Γ_S along the noise circle of interest. Placing Γ_S within the circle of interest would produce less than the specified noise. Figure 3.10 shows a noise circle placed in the smith diagram.

The biggest advantage of using noise circles are when they are used in conjunction with gain circles. The gain vs. noise trade-off is then easily assessed by placing Γ_S within the circles of interest. By moving the reflection coefficient towards the center of the noise circles one can achieve lower noise. The same applies for gain, where one can move the reflection coefficient towards the center of the gain circle to achieve higher gain.

Figure 3.11 shows a smith chart with both noise and gain circles plotted. In order to achieve a gain of 7dB as well as a noise figure of 2dB, Γ_s must be placed within both these circles. This area is shaded with grey. By moving Γ_s to the left or right, one can achieve respectively more gain or less noise. Figure 3.11 also shows that Γ_{opt} would obtain minimum noise figure. The center of all noise circles are located on a straight line from the center of the smith chart towards Γ_{opt}. This also applies for the gain circles where the centers of all circles are placed a long a straight line towards S_{11}^*

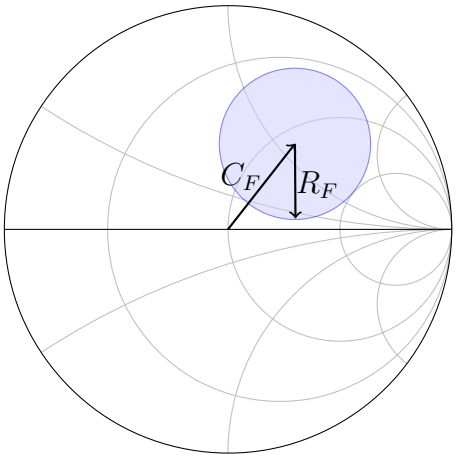


Figure 3.10: A Smith chart with a noise circle plotted

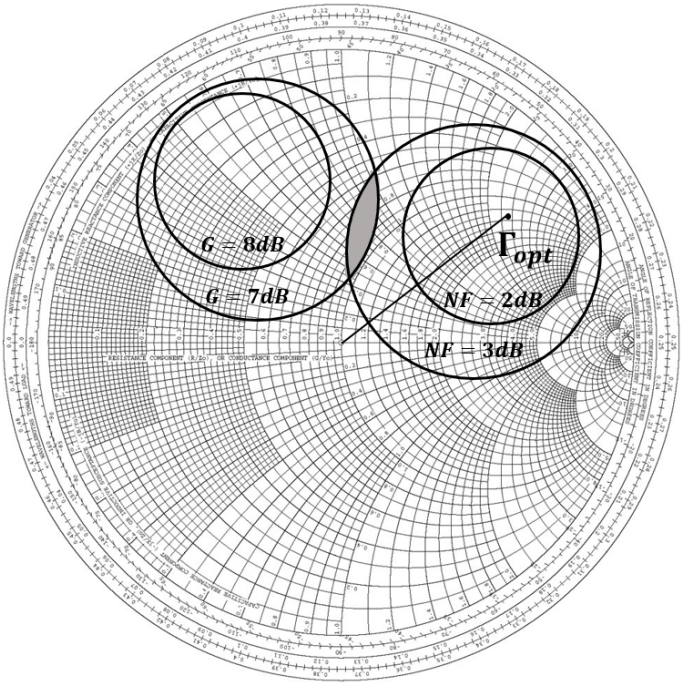


Figure 3.11: Smith chart with both noise and gain circles plotted

3.6 Impedance Matching

The maximum power transfer theorem states that, to obtain maximum external power from a source with a finite internal resistance, the resistance of the load must equal the resistance of the source as viewed from its output terminals. This means that the load resistance should *match* the source resistance. The theorem can also be extended to include circuits with reactive source impedance. It then states that the maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance[1].

$$Z_{in} = Z_S^*. \tag{3.40}$$

In terms of reflection coefficient this transforms to[21]:

$$\Gamma_{in} = \Gamma_S^*. \tag{3.41}$$

In practice when matching for 50Ω, this will make the source reactance resonate with the input reactance and thus make the terminations purely resistive and equal.

The impedance matching network is usually designed so that the impedance seen looking in to the matching network is Z_0, the characteristic impedance of the transmission line. This will eliminate the reflections between the matching network and the source, as previously discussed in section 3.1.2. In multistage designs where interfacing with 50Ω elements is not necessary, the matching impedance may differ from 50Ω as this makes the matching more easily achieved.

The matching networks can be implemented as both lumped or distributed elements. A common design strategy is to design the circuit using lumped elements and then if needed switch to a distributed element later in the design process. Whether or not this is needed depends on the frequencies of interest and the process specifications. Both methods are commonly used in Monolithic Microwave Integrated Circuit (MMIC) design.

Vendelin [27] does however point out that this equivalence between lumped and distributed elements are not recommended since the movements on the Smith Chart is somewhat different. Redesigning for distributed elements could then prove to be a time consuming process.

3.6.1 Matching with lumped elements using the Smith Chart

The matching network can easily ble implemented using both the impedance and admittance Smith Chart. By plotting the normalized impedance, one can simply navigate from this impedance to origo (perfect match) using a combination of the circles of constant resistance and conductance.

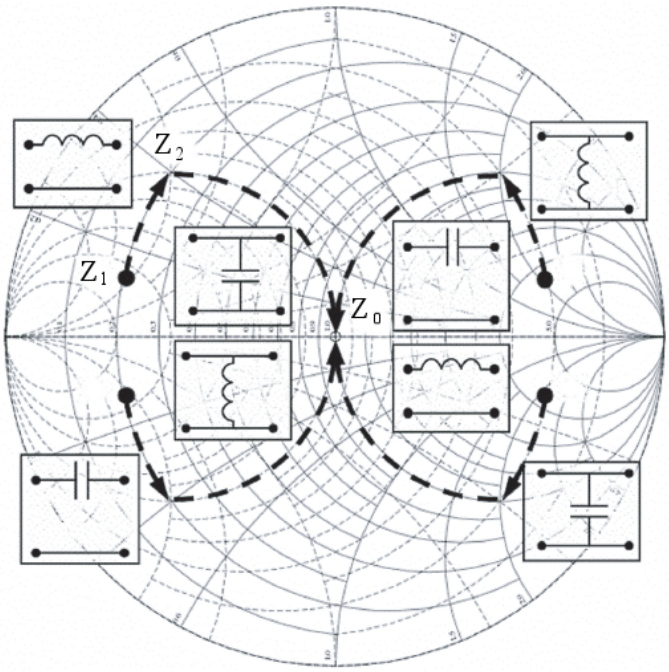


Figure 3.12: Using the Smith Chart for impedance matching. [16]

In general, placing a series element in the matching circuit will transform the impedance along the circles of constant resistance in the impedance chart. Placing a shunt element will transform the impedance along the circles of constant conductance in the admittance chart. A capacitor will shift the impedance towards the capacitive region whereas a inductor will shift the impedance towards the inductive region.

Figure 3.12 shows the different movements possible together with the corresponding lumped element required, and demonstrates four different matching situations. Starting with a load impedance, Z_1, it is possible to transform the impedance to a new impedance, Z_2, by using a series inductor. The impedance has now followed the circle of constant resistance in clockwise direction (towards inductive region). Stopping at Z_2 ensures that one can use a shunt capacitor in order to move along the circle of constant conductance towards Z_0. The load is now matched to Z_0. Figure 3.13 shows the matching network implemented between the source- and load impedance for this example.

The distance of the impedance shift equals the reactance of the required component and thus two simple design equations is used to calculate the value of the component:

$$C = \frac{1}{\omega Z_0 X_C}, \tag{3.42}$$

$$L = \frac{Z_0 X_L}{\omega}, \tag{3.43}$$

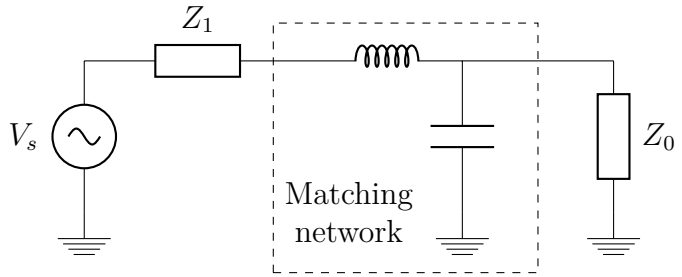


Figure 3.13: Matching network implemented between source and load.

where Z_0 is the characteristic impedance.

Note that these equations are for use with the impedance grid. For use with the admittance grid $X_{L/C}$ must be replaced with the susceptance $B_{L/C} = \frac{1}{X_{L/C}}$.

Another important consideration in impedance matching using the Smith chart is that high frequencies travels *faster* in the Smith chart, making the impedance match more narrow if the distance is large. It is therefore always good practice to choose the shortest distance when selecting devices for matching.

3.6.2 Transmission Line Impedance Transformation

One important property of a transmission line is that it has the ability to transform an impedance, Z_L, into a new input impedance, Z_{in}, by using a length of transmission line in series with the load. Figure 3.14 shows the equivalent circuit for this setup.

The length of the transmission line is given by the *electrical length* θ:

$$\theta = \frac{l}{\lambda} 360°, \tag{3.44}$$

where l is the length of the transmission line.

Equation 3.45 describes the input impedance of the equivalent circuit in Figure 3.14 [28]:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\theta)}{Z_0 + jZ_L \tan(\theta)} \tag{3.45}$$

Note that this equation assumes lossless transmission line. Equation 3.46 shows the relationship when losses are present [28]:

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)} \tag{3.46}$$

There are some special cases that are worth discussing:

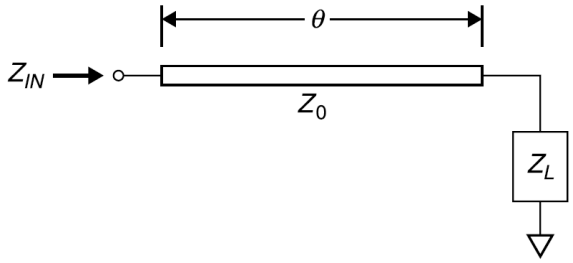


Figure 3.14: Equivalent circuit model for a transmission line, Z_0, in series with a load, Z_L [28].

- When a transmission line of zero length or a multiple of $\frac{\lambda}{2}$ is connected to the load, the load is not transformed and thus $Z_{in} = Z_L$.
- An open-circuit terminated transmission line is purely capacitive when $\theta < 90°$, becomes a short-circuit when $\theta = 90°$, and is inductive when $90° < \theta < 180°$. This behavior repeats every half wavelength. In this special case, Equation 3.45 is simplified to the following expression:

$$Z_{in} = -jZ_0 \cot(\theta) \tag{3.47}$$

The behavior will be similar for a short-circuit terminated transmission line, but the phase is then shifted 90°, making it inductive up to 90°, and capacitive from 90° to 180°. Equation 3.48 shows the impedance relationship for the short-circuit terminated transmission line:

$$Z_{in} = jZ_0 \tan(\theta) \tag{3.48}$$

3.6.3 Single Element Matching

Transmission line matching/impedance transformation is easily adapted with use of the Smith Chart. Given that the transmission line impedance is 50Ω, the movements are always along the constant voltage standing wave ratio (VSWR) circle as showed in Figure 3.15. The length of the transmission line is determined by using the wavelength scale on the Smith chart. A full rotation in the Smith Diagram corresponds to a electrical length of 180°.

If the characteristic impedance is different than 50 Ω, the center of the circular motion will be shifted. $Z_0 < 50\ \Omega$ will shift the circle towards 0 Ω while $Z_0 > 50\ \Omega$ will shift the circle towards ∞ Ω. This property is exploited when the load impedance is located within the $1 + jX/B$ circles and makes it possible to match the load impedance using only a single transmission line. Vendelin [27] explains a manual procedure using the Smith Chart. Utilizing this matching by hand is a tedious operation and it is therefore more convenient to use CAD tools for this

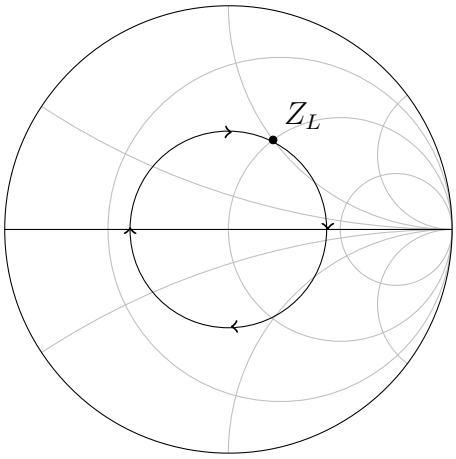


Figure 3.15: A transmission line with 50Ω impedance will exhibit a circular motion movement around the origo of the Smith Chart.

operation. The transmission line can then easily be tuned in order to achieve perfect match.

3.6.4 Single-stub Matching

As previously discussed in 3.6.2, a shorted or open transmission line will exhibit a purely inductive or capacitive response. If a transmission line is connected in parallel and left open or shorted it is called a *stub*. This stub can be utilized to cancel out any reactive impedance.

Since the stub is connected in parallel and acts purely reactive, the movement in the Smith chart follows the constant circles of conductance. A short-terminated stub will always start at $0+j0$ while a open-terminated stub will always start where the load is located. This is also analog to the previously mentioned 90° phase shift between the shorted and open stub. Increasing the length of the stub will move the impedance in a circular motion in clockwise direction. The initial matching conditions will therefore determine whether to use a shorted or open stub. As previously discussed in section 3.6.1 choosing a short matching path will provide higher bandwidth.

3.6.5 Two-element Matching

Even though matching is possible using only one element, most of the cases requires the use of two elements. This is achieved by combining a transmission line with a parallel stub. The matching procedure is as follows:

1. Plot the load in the Smith chart. Place a transmission line of 50 Ω between

the load and the input. 50Ω is used in order to rotate the impedance in a circular motion with origo of the Smith chart as center.

2. In the Smith chart, rotate the load in clockwise direction as previously showed in Figure 3.15. The rotation should stop as the impedance intersects the $1+jB$ circle of constant conductance.

3. The length of the transmission line is then determined by reading the *wavelengths toward generator* scale on the Smith chart. The length of the transmission line is then given by: $l = (\lambda_{end} - \lambda_{start}) \times \lambda$

4. Use a stub with 50 Ω impedance to cancel out the reactive part of the load impedance. The impedance will then move along the constant circle of admittance in clockwise direction. The length of the stub is determined by reading the susceptance where the load is located and then read the *wavelength toward generator* scale. Use the equation given in step 3 to calculate the length of the stub. Choose the appropriate termination of the stub based on the initial location in the Smith chart.

Using this procedure with a $Z_0 \neq 50$ Ω transmission line is also possible, but keep in mind that the center of the circular motion is then shifted away from the center of the Smith Chart.

3.6.6 Considerations With Lossy Transmission Lines

The previous matching methods with transmission lines and stubs assumes lossless elements. When designing a real transmission line there are losses present and thus ideal behavior is not the case. In addition to this there will be parasitic capacitance and inductance as well as coupling to surrounding structures. This will cause the movements in the Smith chart to be somewhat different. These movements are difficult to anticipate and thus CAD tools are used in order to match using transmission lines.

3.6.7 Smith Chart Q-Contours

An important consideration in filter design and impedance matching is the quality factor. The quality factor is a quantitative measure of the bandwidth relative to the center frequency. A high Q-value corresponds to a narrow bandwidth and vice versa. The smith chart with constant Q-contours is a useful aid in designing a matching network with a specific Q-value. Figure 3.16 shows a smith chart with these Q-contours. By keeping the impedance transformations within the desired Q-contour one can achieve a specific Q-value. In general it is apparent that one could achieve

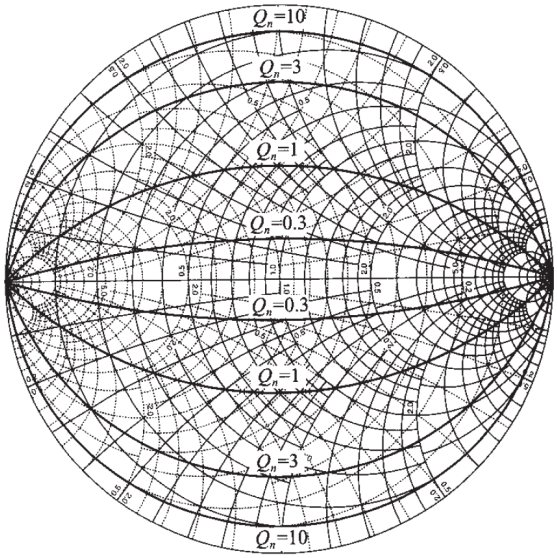


Figure 3.16: Contours of constant Q in smith chart [18]

lower Q-values and thus higher bandwidth by constraining the movements in the smith chart within a small area close to the $I_m = 0$ line. The disadvantage of this is that one must often use additional components to achieve this, increasing the area and complexity. Figure 3.17 shows how one could achieve a q-factor of 1 when the impedance is originally located far from the center of the smith chart.

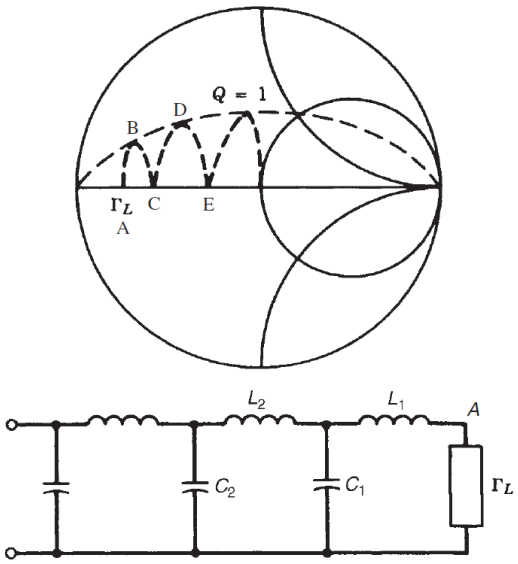


Figure 3.17: Matching for a q-factor of 1 [27]

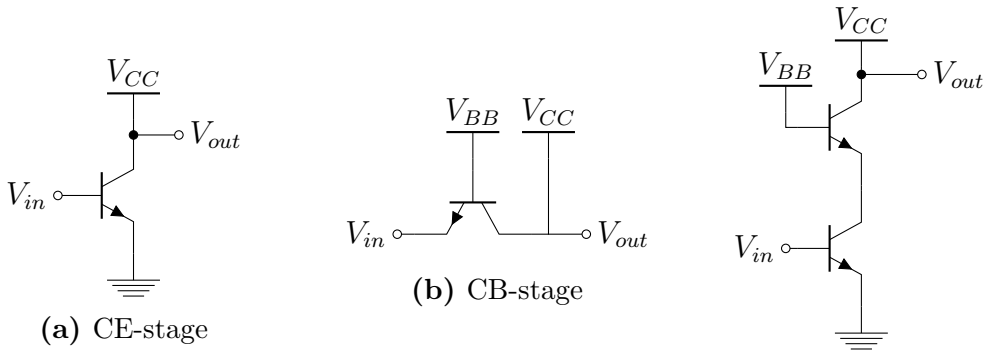
CHAPTER 4

Low Noise Amplifier Design Methodology

The LNA is the first stage after the antenna and it must handle very small signal amplitudes. In addition to this, the amplifier must have little contribution to the overall noise figure. This chapter will go through some of the theory needed for the design of a LNA.

4.1 Topologies

There are three prevailing topologies that are used in LNA designs. These are the common-emitter (CE), common-base (CB) and cascode topology shown in Figure 4.1. A comparison of some of the most important parameters in these topologies are shown in Table 4.1 [7].



(a) CE-stage

(b) CB-stage

(c) Cascode stage

Figure 4.1: The three prevailing LNA topologies

Characteristic	Common Emitter	Common Base	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher than CE
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
f_{-3dB}	Low	Fairly high	High
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High
PVT Sensitivity	Greater	Lesser	Lesser

Table 4.1: Comparison of commonly used topologies[7]

The cascode amplifier is doing quite well on all parameters except for the noise figure which is slightly higher than for the CE-stage. The cascode stage does, however, add some complexity to the circuit since it needs higher supply voltage in addition to an extra bias voltage for the cascode transistor. The high supply voltage also results in a higher power consumption for the same bias conditions.

The common-gate amplifier has good reverse isolation and good linearity but has lower gain and more noise compared to the CE-stage. One additional advantage is that one could easily achieve 50 Ω match by manipulating the transconductance of the transistor, based on the fact that the input impedance of a common-base amplifier is $\approx \frac{1}{gm}$. The low gain and high noise does, however, make the common-base amplifier less suitable for a LNA design.

The common-emitter stage has the lowest noise of all three topologies and moderate gain and linearity.

As several stages are most likely needed, it will probably be beneficial to combine several topologies. The CE-stage does a very good job as an input stage based on the low noise and moderate gain. The cascode stage would make a good output stage based on the high reverse isolation and high gain.

4.2 Noise

Noise is one of the most important parameters in a system, and thus great care should be taken in analyzing the noise performance of the amplifier. As previously discussed in Section 3.4, NF is a important measure of the overall noise contribution of the amplifier. Keeping this figure low is of great importance.

4.2.1 Noise Sources in Bipolar Transistor

An HBT contains several intrinsic noise sources. Figure 4.2 shows a simplified bipolar transistor small signal model with the dominating noise sources.

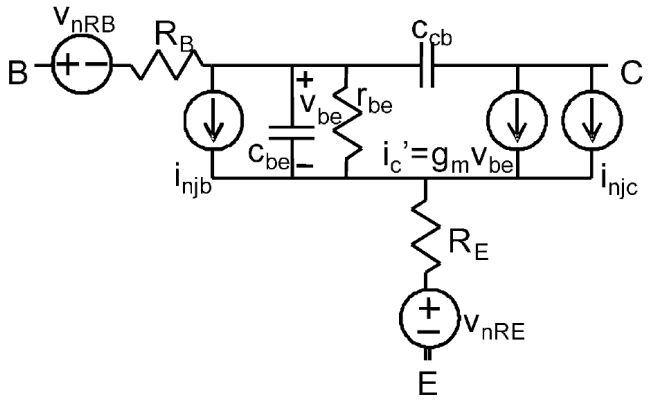


Figure 4.2: Small signal schematic of bipolar transistor with dominating noise sources [24]

The noise sources are as follows:

Collector current shot noise i_{njc} is the collector current shot noise given by the following expression: $i_{njc} = 2qI_c\Delta f$. This noise is caused by electron movements from the emitter to the base and the statistical distribution of different energy and direction of the crossing of the PN-junction.

Base current shot noise i_{njb} is the base current shot noise given by the following expression: $i_{njb} = 2qI_B\Delta f$. This noise source origins from holes moving towards the emitter. The base current shot noise and collector current shot noise is typically uncorrelated for a modern HBT.

Thermal noise Uncorrelated thermal noise is also present due to the parasitic resistance in the base and emitter. The expressions for the base and emitter thermal noise is $v_{nRB} = 4KTR_B\Delta f$ and $v_{nRE} = 4KTR_E\Delta f$.

4.2.2 Minimum Noise Figure

In order to evaluate the noise figure of the amplifier the term F_{min} is used. This is the minimum achievable noise figure for a given topology and configuration.

The minimum noise figure for a SiGe HBT is given by equation 4.1 [24]:

$$F_{min} \cong 1 + \frac{n}{\beta} + \sqrt{\frac{2I_C}{V_T}(R_B + R_E)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta}\right) + \frac{n^2}{\beta}} \tag{4.1}$$

where $V_T = kT/q$, R_B is the base resistance, R_E is the emitter resistance and n is the I_C ideality factor.

This expression can be simplified since β typically is larger than 100, n is very close to 1 and R_B is much larger than R_E. This gives the following expression:

$$F_{min} \cong 1 + \sqrt{\frac{2I_C}{V_T}(R_B)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta}\right)} \tag{4.2}$$

4.2.3 Noise Matching

Scaling of the transistor is primarily done to achieve noise matching through choosing the optimum source admittance. This was previously discussed in Section 3.4.1.

For a given bias, Equation 4.2 suggests that reducing R_B would yield better noise performance. This can be achieved by increasing the base area.

The optimum source resistance for low noise operation is given by equation 4.3 [25]:

$$R_{s,opt} = \frac{f_T}{f}\frac{1}{\sqrt{L_E}}\sqrt{\frac{2R_B}{J_C W_E}\frac{kT}{qI_C}} \tag{4.3}$$

If the current density is given by choosing a specific bias point, equation 4.3 suggests that the $R_{s,opt}$ could be matched by changing the emitter width or emitter length. For optimal noise performance, the $R_{s,opt}$ should be sized to 50 Ω which is the source impedance of the antenna.

Note that as previously discussed in section 3.4.1, the correlation susceptance will also have an impact on the noise matching of the device. Thus using the Smith chart with noise circles or the optimum reflection coefficient will give more insight in the noise matching of the device.

4.2.4 Noise in Casaded Stages

The total noise figure for n cascaded stages is given by equation 4.4 [1]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{n-1}} + ... \tag{4.4}$$

As seen by the expression, the noise from the subsequent stages have less impact on the total noise figure due to the gain from the previous stages. The gain of the first stage will therefore "suppress" the noise from the subsequent stages relative to the signal. Given that the gain in the first stage is adequate, the first stage will dominate the noise figure of the system.

4.3 Stability

An important consideration in amplifier design is whether the amplifier is stable at all frequencies of interest. Figure 3.4 shows the general two-port amplifier. Oscillation in this amplifier is possible if the input or output port impedance has a negative real part, causing the reflection coefficients to be larger than unity. Reflections can then sum with the input signal and cause uncontrollable oscillations. Since $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are directly related to $|\Gamma_S|$ and $|\Gamma_L|$ this means that the stability of the amplifier is dependent on the input and output matching. Two types of stability can be defined [21]:

- *Unconditional stability*: The network is unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances.
- *Conditional stability*: The network is conditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ only for a certain range of passive source and load impedances. This case is also referred to as *potentially unstable*.

4.3.1 Single Stage Stability

In order to determine if the amplifier is unconditionally stable there are two criteria that one must satisfy. This is known as *Rollet's condition* and is defined by the following two conditions[21]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{22}|} > 1, \tag{4.5}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \tag{4.6}$$

If both these expressions are satisfied, the device will be unconditionally stable. This test is also known as the *K-Δ-test*.

Not all CAD tools provide Δ as a simulation parameter. Thus, a second auxiliary parameter $B1$ is defined:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{4.7}$$

The necessary condition for unconditionally stability is then: $K > 1$ and $B > 0$.

If the s-parameters do not satisfy these conditions, *stability circles* in the Smith chart or other methods must be used to determine if the amplifier is stable.

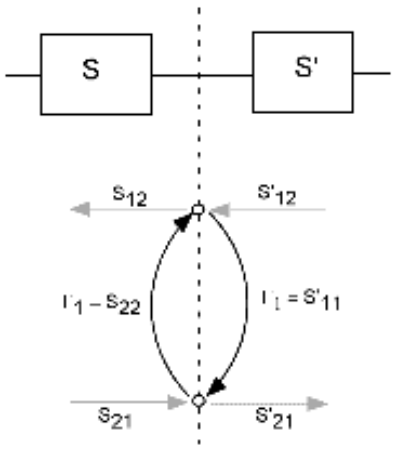


Figure 4.3: Two networks connected and described using signal flow chart modeling. [14]

4.3.2 Multistage Stability

The k-factor stability criteria is only valid for a single stage amplifier. Designing a multistage amplifier requires more advanced methods for determining stability since there could be internal oscillations that are not accounted for when looking at S_{11} and S_{22}.

One approach in making the multistage amplifier stable is to design each stage for unconditionally stability. This may prove to work, but feedback between the amplifier stages may cause oscillations. Although there will normally not be any feedback between the stages, unintentional feedback may occur through the bias networks. Another drawback with this method is that performance must be traded when making the amplifier unconditional stable.

Stability evaluation using *Gamma probes* provides a very good solution for evaluating the internal stability. Using this method may provide better performance as well as satisfactory margin for stability. [14] This method is based on the fact that one can represent the connection between two networks as a signal flow chart model shown in Figure 4.3.

Figure 4.3 shows two networks connected and represented by signal flow chart modeling. This modeling allows use of the Nyquist stability criterion which is often used to determine stability in control systems. The stability is now evaluated by looking at the loop in the signal flow chart as feedback loop. The open loop frequency domain response is then given by Equation 4.8:

$$G = -\Gamma_1\Gamma_2 \tag{4.8}$$

Γ_1 and Γ_2 represent the reflection coefficients of the gamma probe.

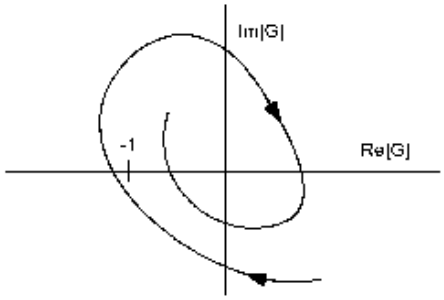


Figure 4.4: G plotted in polar plot showing instability. [14]

In order to evaluate stability, G is plotted in a polar plot. The Nyquist stability criteria states that if the open loop function G, when plotted in a polar plot as a function of frequency, encircles the -1 point in the clockwise direction, then the closed loop system will be unstable [14]. Figure 4.4 shows G plotted for an unstable system where the -1 point on the real axis is encircled in clockwise direction.

By inserting gamma probes within the circuit and plotting G, it is now possible to evaluate the internal nodes for stability. The gamma probes are placed in series with the input or output of active devices where the stability is to be evaluated. The element is completely transparent to the circuit and thus normal simulations can be applied with these probes inserted.

4.4 Non-linearity

One of the important properties of an amplifier is the linearity. Even though a transistor can be made fairly linear for small input signals, it will exhibit non-linear response for large input signals.

It can be shown that for a general non-linear system, the output can be modeled as a taylor series given by Equation 4.9

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + ... \tag{4.9}$$

If the second- or higher order coefficients are of large magnitude, the resulting output will be nonlinear. Thus, for a linear system, these coefficients should be zero.

4.4.1 1dB Compression Point

For most amplifiers, the a_3 coefficient is negative, causing the amplifier to experience a gain drop for larger input signals. This effect is called *gain compression* or

saturation. More specifically, this problem is due to the saturation of the transistor. The 1dB compression point is a good way of quantifying this effect. As the name suggests, the 1dB compression point is where the output signal is 1dB lower than the ideal linear response. Figure 4.5 shows a typical amplifier response and defines the 1dB compression point.

4.4.2 Intermodulation Distortion

Intermodulation distortion (IMD) is a distortion that occurs when two signals, f_1 and f_2 with slightly different frequencies are applied to a non-linear amplifier. The resulting output is that harmonic products are created and added to the original signal. Even though harmonics of several orders are created, it is the third order harmonics, $2f_1 - f_2$ and $2f_2 - f_1$ that are most problematic since they are near the original frequency and thus cannot be filtered out. IMD is typically defined as the difference between the desired and the undesired power level in dBm as given in Equation 4.10[18]:

$$IMD(\text{dB}) = Pout(f_2)(\text{dBm}) - P_{out}(2f_2 - f_1)(\text{dBm}). \tag{4.10}$$

Equation 4.9 shows that the output signal consists of the fundamental signal as well as harmonic components. It is also apparent that the linear part rises linearly while the harmonic components grow with n-th order. For low input powers, the linear part will be much higher than the harmonic part. However, for larger input powers, the harmonic components will be comparable to the linear part. More specifically, the third order harmonics will grow cubically thus there must be a theoretically interception point where the linear part intersects with the third order harmonic component. This interception point is called *Third order interception point* and is often used as a measure of linearity on an amplifier. Figure 4.5 shows how this interception point is defined. OIP3 refers to the output referred third order interception point while IIP3 refers to the input referred third order interception point. Since the amplifier will saturate with higher powers, the lines are extended as dotted lines to show the *ideal* response and thereby the interception point.

Many systems follow the approximate rule that the IP3 is 12-15 dB larger than the P1DB [21]. It should in any case be well above the P1DB so that the magnitude of the non-linear component is well below the linear part.

4.4.3 Emitter Degeneration

Even though the transistor is fairly linear for small input signals, the transconductance, gm, of the transistor will vary as the collector current varies. This will in

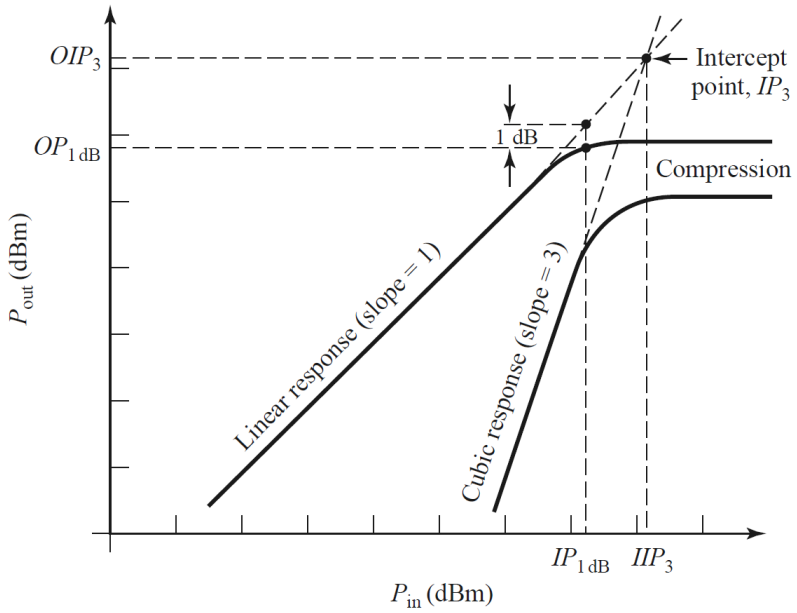


Figure 4.5: Definition of third order interception point and compression point [22]

turn change the gain of the amplifier and cause a non-linear response. In order to suppress this effect and thus make the transistor linear for a larger range of input voltages one can use an emitter degeneration inductor, L_E.

L_E will introduce negative feedback and suppress the variations in gm and thus make the transistor linear for a larger range of input voltages. The cost of this improvement in linearity is loss of gain.

In addition to the improved linearity, stability is improved due to the negative feedback. Hence the amplifier can be made unconditionally stable by adding a sufficient amount of emitter degeneration.

CHAPTER 5

Design and Simulation

This chapter will describe the design procedure of the LNA. Since the first stage of the LNA is the most important stage, the design procedure for this stage is reviewed in depth. The design of the two subsequent stages are described with less details since the procedure and approach is similar to the design of the first stage. After designing the three stages separately, all stages are combined to a multistage amplifier.

Multistage design is a iterative process. This means that design changes are continuously made and that the initial design should be optimized in several ways in order to maximize performance. This chapter will go through the whole design process, from start to finish. A short summary of the performance of the resulting multistage amplifier is shown in Section 5.8.5.

5.1 Design Specifications and Topology Decision

Table 1.1 given in Chapter 1 shows the design specifications for the LNA design. The resulting amplifier must fulfill these design specifications.

Section 4.1 describes the most used topologies for LNA stages and the pros and cons for these topologies. For this particular LNA design it would be beneficial to use a combination of common emitter and cascode topology. This would ensure low noise, high reverse isolation and high gain. However, the cascode topology was proven to provide insufficient bandwidth. This problem is elaborated in Appendix D. Common emitter is therefore to be used on all stages. This will make impedance matching more difficult since the reverse isolation is much lower for this topology.

In order to meet the gain requirements, several stages is needed. For ease of the design one should keep the number of stages at a minimum, since the complexity increases as the number of stages increases. By experimenting with the circuit in Figure E in Appendix E, it is found that three stages is a good compromise between complexity and performance. This also allows for some gain trade-off in order to achieve good noise conditions.

5.2 Choosing Transistor

There are three available npn transistors in the IHP 0.13 µm process, npn13p, npn13pl2 and npn13v2. The npn13v2 transistor has $f_T = 50$ GHz, and is thus not applicable for this design. As previously discussed in Section 2.3, npn13p and npn13pl2 differs in the way the layout is made but has very similar f_T. IHP recommends using the BEC layout unless very high currents are needed. (G. Fischer, IHP, private communication, 01.12.2015)

The most important parameter in LNA design is the noise figure and thus we have to make sure that we scale for minimum noise figure.

5.3 Gain vs. Noise Trade-off

As discussed in section 4.2.4, noise from the subsequent stages are suppressed relative to the amplified signal by the gain of the first stages. This does, however, require that the gain of the first stage is sufficiently large. By experimenting with different noise and gain trade-offs, it is apparent that a single stage does not provide sufficiently low noise and adequate gain for noise suppression. The second stage will therefore have some impact on the overall noise figure.

By investigating how the total noise figure is affected by the gain and noise of the first and second stage, the gain structure of the multistage amplifier can be determined. By using 6 data points from experiments with a CE-stage the gain vs. noise is plotted for a single stage, as shown in Figure 5.1. The graph shows a linear trend and thus linear regression can be used to predict the gain for different noise values and vice versa. The linear relationship is found by using the method of least squares and is given by equation 5.1. Note that this is a rough estimate, but it will still provide useful information regarding the gain structure.

$$\text{Gain} = 3.7354 \times \text{NF} - 3.2563 \tag{5.1}$$

By using equation 4.4 as well as varying the gain of the first stage and second stage, it

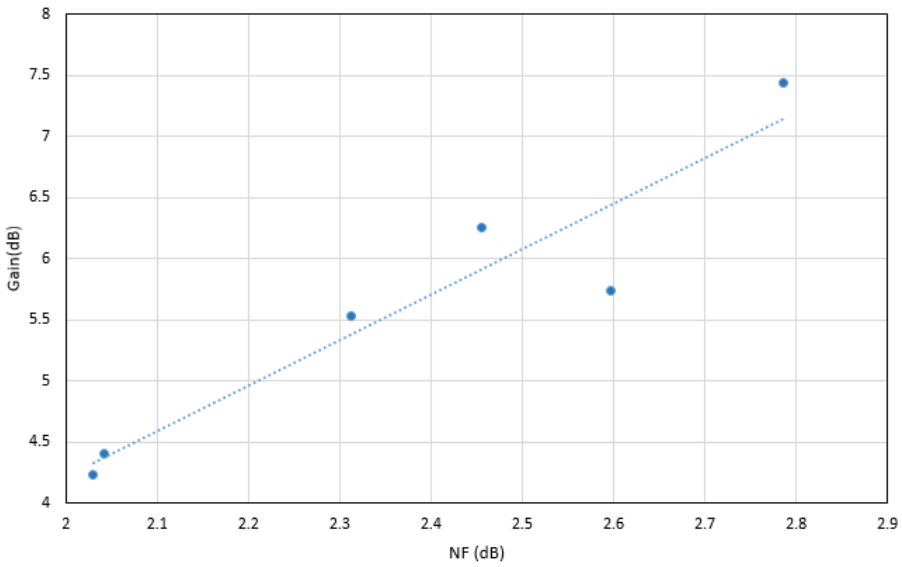


Figure 5.1: Linear regression of gain vs. noise trade-off

is now possible to calculate and plot total noise and gain for different configurations of input- and second stage. The gain of the output stage will have very little impact on the total NF, so this stage can be optimized for maximum gain. The gain of the output stage is fixed at $S_{21} = 9$ dB with NF = 3.8 dB (which is the approximate gain and noise for a stage optimized for gain).

Figure 5.2 shows the total NF plotted against total gain for different configurations of input stage and second stage gain. The gain of the first stage is swept from 3 dB to 9 dB corresponding to a NF of 1.7 dB to 3.3 dB. Each plot corresponds to a specific gain/NF in the second stage, indicated by the legend. This way of plotting the total gain vs. NF introduces a graphical aid in choosing the first and second stage gain for best gain vs. NF trade-off.

Notice that each curve has a noise equilibrium. This equilibrium corresponds to a gain of 4.2 dB and a NF of 2 dB for the first stage. Also note that that as the gain for the first stage decreases, the overall gain decreases and the total NF increases. The first stage should therefore have a gain of minimum 4.2 dB.

For the second stage, there seems to be an equilibrium at approx. 5 dB gain, which corresponds to a NF of 2.2 dB. It is also clear that choosing a lower gain than 5 dB will produce less total gain and more total noise, making 5dB a minimum amount of gain for the second stage. Choosing 5 dB gain at the second stage as well as 4.2 dB gain for the first stage will then produce a minimum in total NF.

However, by looking at the plot it is clear that one could trade a small amount of NF for several dB in gain. Since the noise figure is well below the specifications, trading some noise for gain is of interest. Therefore the second stage should be designed for

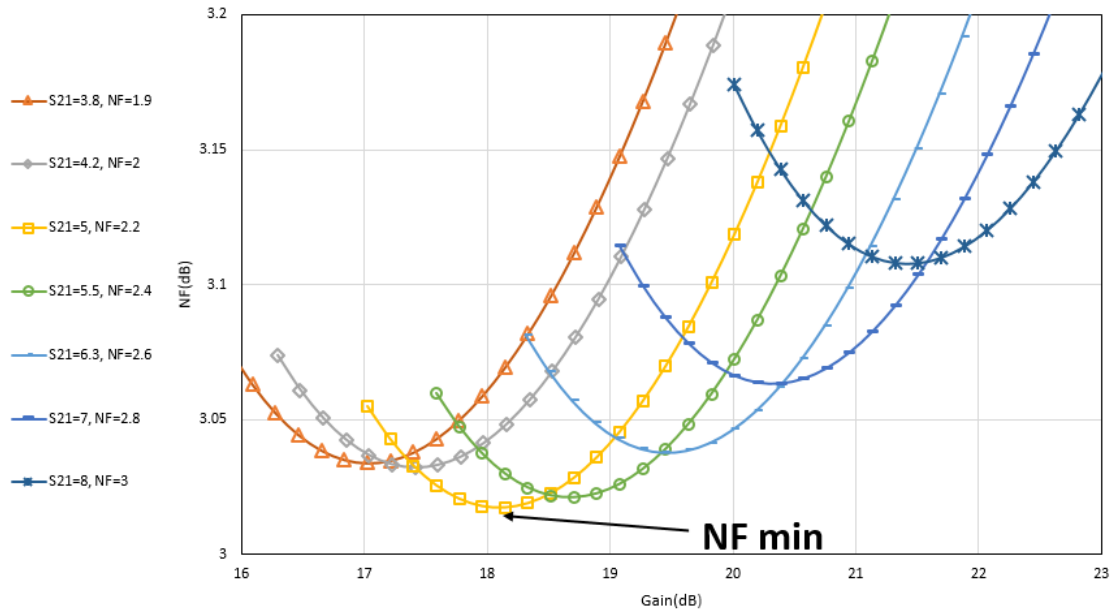


Figure 5.2: Gain vs. NF for 6 CE stages with different bias and noise matching. Plots and calculations are performed in Excel.

a gain of approx. $6 - 7$ dB.

Notice that this method is an approximation, so the results should be interpreted with this in mind.

5.4 Input Stage Design

The input stage is the most important stage in a LNA since it normally defines the noise level for the system. The main goal is to keep the noise as low as possible as well as keeping the gain adequate for noise suppression. In order to achieve low noise one has to match the input for lowest noise as discussed in section 3.4 and 4.2.3. In addition, it is desirable to achieve conjugate matching for maximum power transfer as previously discussed in section 3.6. By using the following general method, it is possible to meet both these requirements [5]:

1. Choose bias at F_{min} for minimum noise figure.
2. Scale the number of emitters and number of transistors to achieve $R_{opt} = 50\ \Omega$.
3. Match impedance at output
4. Use emitter inductor, L_E for increasing the real input impedance to 50 Ω.
5. Add base inductor for canceling the inductive part of the input impedance.

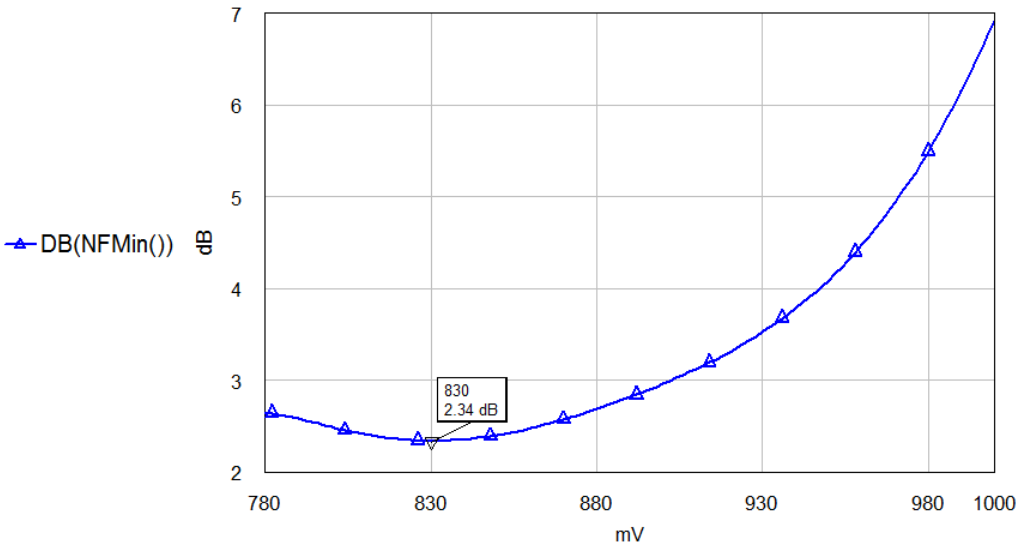


Figure 5.3: NFmin plotted against bias voltage at 61.5 GHz.

Biasing at F_{min}

Using the test setup shown in Appendix E, Figure E.1, the bias voltage is swept from 0.78V to 1V. F_{min} is then plotted against the bias voltage in order to set the optimum bias point. Figure 5.10 shows this graph.

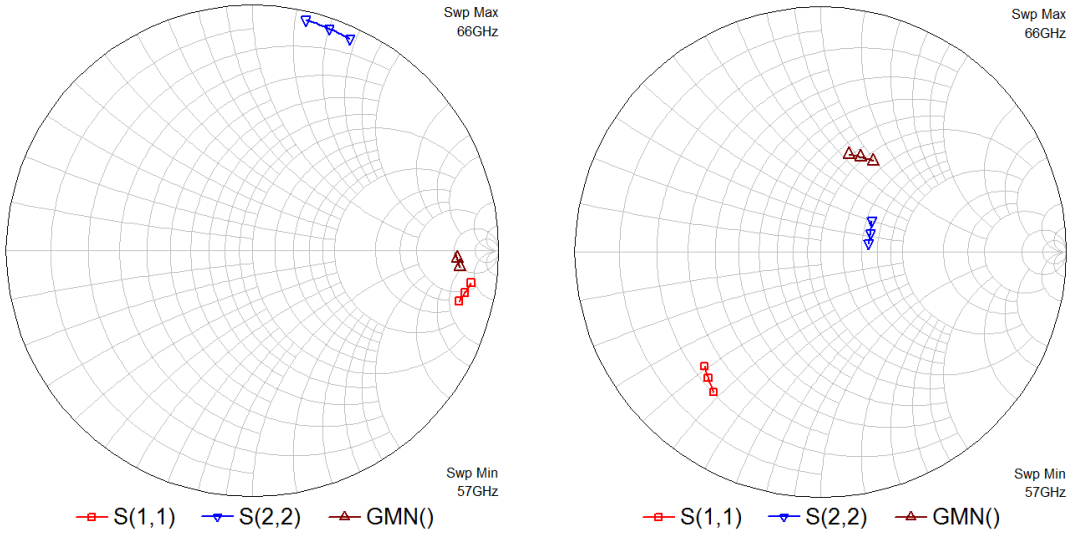
As seen by Figure 5.3, 830 mV will provide F_{min} and thus 830 mV is set as bias point for the first stage. Choosing 830 mV as bias also ensures that the power consumption is low, which is important in order to achieve the power consumption specification.

Scaling the Transistor

Scaling the transistor for optimum noise conditions is previously discussed in Section 4.2.3. The emitter length, L_E, is constrained by only two lengths in the IHP 0.13 µm SiGe process, and thus the emitter width, W_E, must be modified to match $R_{s,opt}$. This can be achieved by changing the number of emitters per collector, N_X. This changes the effective width of the emitter as well as lowering the base resistance.

$R_{s,opt}$ is possible to simulate in Microwave Office (MWO), but this parameter is simply the real part of the optimum reflection coefficient for minimum noise figure, GMN[1]. By tuning GMN, the correlation susceptance and optimum source resistance can be assessed simultaneously. Noise matching is performed by placing GMN close to the center of the smith chart.

[1]GMN is the abbreviation for the optimum reflection coefficient for minimum noise figure used by Microwave Office



(a) Input stage before tuning.

(b) Input stage after tuning the transistor size

Figure 5.4: S-parameteres and GMN.

S-parameters for the circuit in figure E.1 with m=3[2] and N_x=1[3] is shown in Figure 5.4a. m=3 is chosen for convenience, since the number of emitters, N_x only can span between 1 and 8. m=3 then gives a maximum number of $3 \times 8 = 24$ emitters for the tuning.

By tuning the total number of emitters between 3 and 24, the optimum size can now be determined. A total number of 12 emitters seems to be the optimum point, corresponding to $m = 3$ and $N_x = 4$. Figure 5.4b shows GMN and scattering parameters after tuning the size. Power consumption is approx. 1.91 mA $\times$ 1.2V = 2.29 mW after scaling to 12 emitters. 12 emitters can also be realized by $m = 2$ and $N_x = 6$ and this is preferable due to less parasitics in the layout. The length of the emitter is kept at 0.48 µm because the base resistance increases with L_E. This will in turn lead to increased noise and therefore for minimizing noise, L_E is kept at a minimum. The current capability of the 0.84 µm transistor is however better, but for low power designs this is not of any concern.

Output Matching and Optimization

Since the reverse isolation is low, tuning the output will also affect the input reflection coefficient. Therefore, the output is tuned before the input so that the output tuning will have less impact on the noise matching. By looking at Figure 5.4b, one

[2] m is defined as the number of transistors in parallel.
[3] N_x is defined as the number of emitters in parallel.

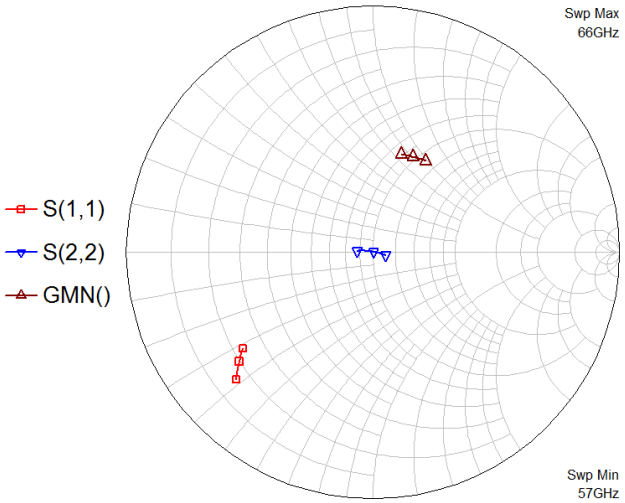


Figure 5.5: S-parameters and GMN for input stage after matching the output

sees that the output could be matched using a shunt inductor and a series capacitor. This is realized by using the collector inductor as the shunt inductor and adding a series capacitor of 70 fF. Figure 5.5 shows how the s-parameters and GMN are located after matching the output. Notice that the output does not alter anything regarding the noise matching, since GMN is not moved.

Emitter Inductor

As previously discussed in Section 4.4.3, emitter degeneration is desirable in order to make the amplifier more linear and provide better stability. In addition to this, the emitter inductor is used to modify the input impedance of the amplifier. Figure 5.6 shows a simplified small signal model for a transistor with emitter inductor.

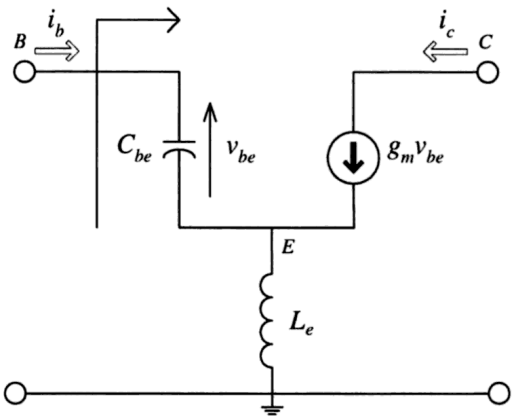


Figure 5.6: Simplified small signal model for a transistor with emitter inductor [5]

It can be shown that the input impedance for this common emitter amplifier with emitter inductor is given by Equation 5.2:

$$Z_{in} = \frac{1}{j\omega C_{be}} + j\omega L_e + \omega_T L_e \tag{5.2}$$

The resistive part of this impedance is given as $\omega_T L_e$. By setting it equal to 50 Ω one could achieve power matching at 50 Ω:

$$L_e = \frac{50\Omega}{2\pi f_T} \tag{5.3}$$

This matching is realized by tuning L_E in MWO. Since adding an emitter inductor also reduces the gain, one must have simultaneous control on both S_{11} and G_A. This is achieved by adding a gain circle to the Smith chart. A gain circle with a constant gain of 4.2 dB is added, since this value of gain are the minimum amount of gain for noise suppression according to Section 5.3.

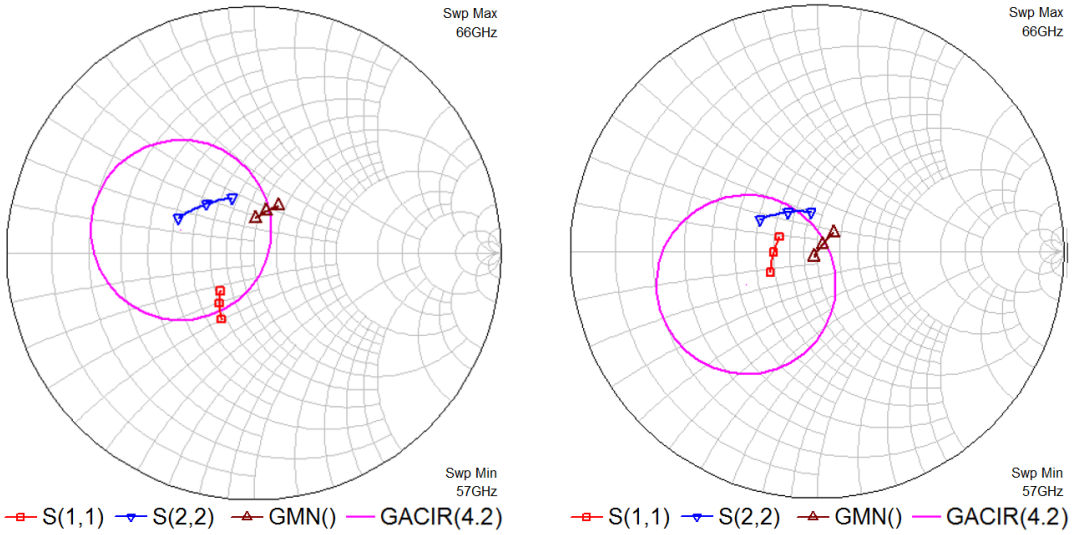
Tuning L_E also has the benefit of moving GMN closer to the center of the Smith chart, improving the noise match. In addition, icreasing L_E improves the k-factor, making the stage unconditionally stable for the whole bandwidth. The k-factor does however drop at low frequencies, but that does not necessarily mean that the amplifier is unstable. Stability is reviewed in more detail for the multistage amplifier in Section 5.8.2. Figure 5.7a shows how the s-parameters, GMN and gain circle is located after adding an inductor of 87 pH.

By inspecting Figure 5.7a it is apparent that the real part of the input impedance is still somewhat low. Increasing the value of L_E would increase this impedance, but the gain trade-off was simply too large. The gain circle of 4.2dB is now enclosing the center of the Smith chart.

Impedance Match With Series Inductor

The real part of the input impedance is now matched to approx. 50 Ω, so the only thing remaining is to cancel out the capacitive input impedance with an inductor. This will result in both power matching and noise matching. Figure 5.7b shows the s-parameters and GMN after adding the series inductor.

As seen by the Smith chart, both the input and output are now adequately matched. In addition to this, the optimum reflection coefficient for low noise has moved closed to the center, improving the noise matching. Figure 5.9 shows the frequency response. Both S_{11} and S_{22} are now below -10dB and the available gain is approx. 4.2 dB. The achieved gain is however slightly less than 4dB which is lower than the minimum gain for good noise suppression. This can be improved at a later point



(a) Input stage after adding an emitter inductor

(b) Input stage after adding series inductor

Figure 5.7: S-parameteres and GMN.

since the matching is not optimized at this point. Note also that S_{12} is very high, causing low reverse isolation and challenging matching conditions. NF for the input stage is now 2.0 dB.

Figure 5.8 shows the schematic of the input stage. Note that this is simply a base for further tuning and optimization. Bias network are now implemented as an ideal voltage source with a large AC-block inductor in series. Changing this to a realistic source and inductor will change both the input and output match.

5.5 Second Stage Design

The design of the second stage is similar to the design of the first stage. As previously discussed in Section 5.3, the noise is not fully suppressed by the first stage and thus the second stage will also have great impact on the overall noise figure. Since we are willing to trade some noise for gain, the second stage is biased with more current than the first stage.

A common-emitter stage is chosen for its low noise and moderate gain.

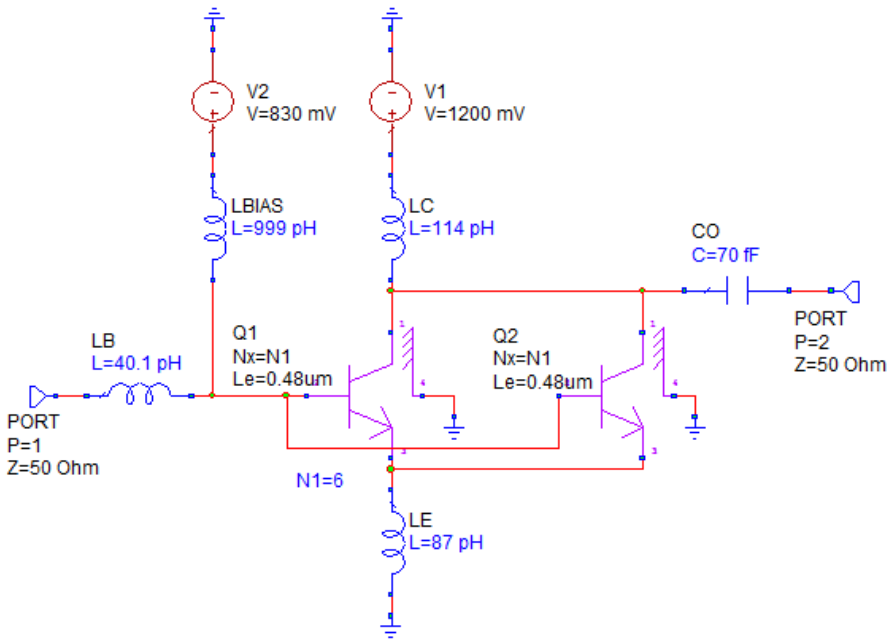
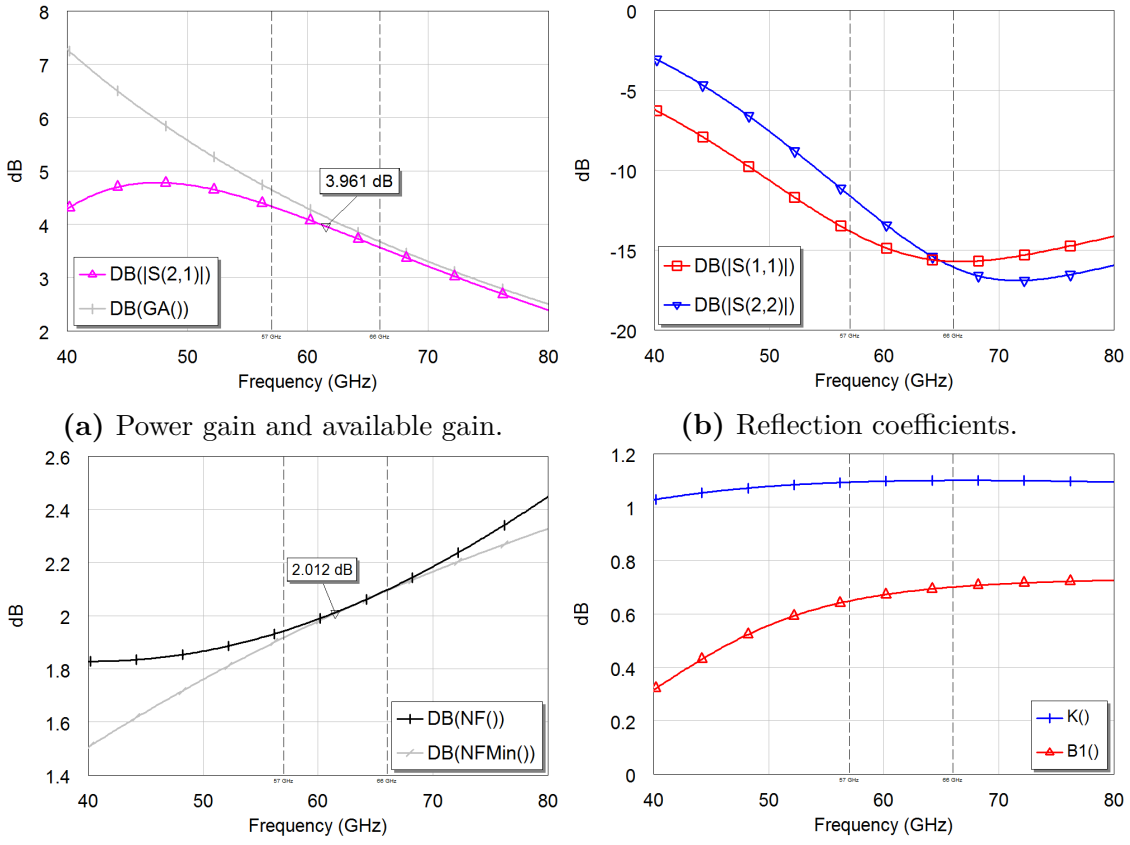


Figure 5.8: Input stage with matching



(a) Power gain and available gain.

(b) Reflection coefficients.

(c) NF and NFmin.

(d) $K - \Delta$-test

Figure 5.9: Simulations for input stage.

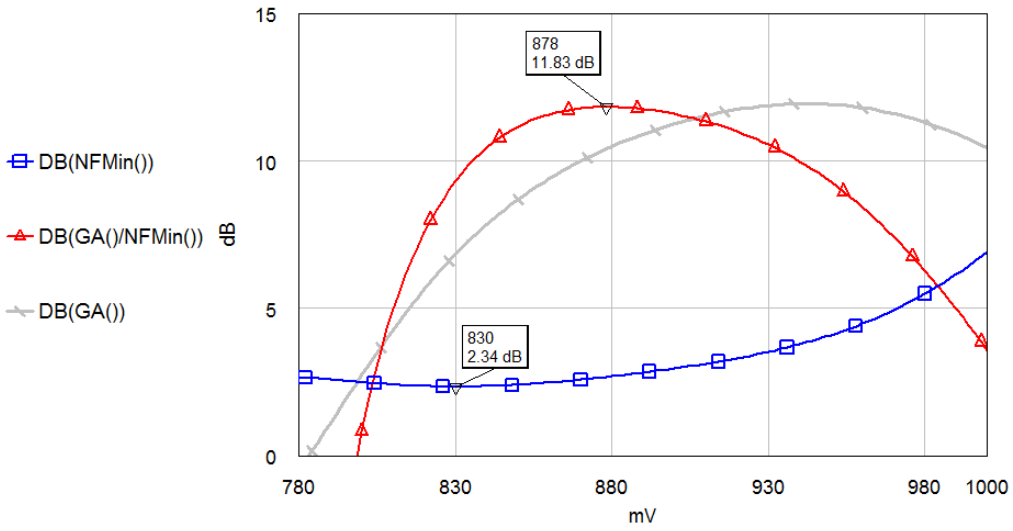


Figure 5.10: NFmin, GA and GA/NFmin plotted against bias voltage. Note that there is a maxima in GA/NFmin, leading to a good compromise between gain and noise.

Bias Conditions

By sweeping $\frac{G_A}{F_{min}}$ one can find the equilibrium for gain vs. noise where the graph peaks. This bias point will produce the most gain compared to noise, and is thus a good bias point for the second stage where both gain and noise must be optimized. Figure 5.10 shows this simulation.

By inspecting the simulation results it is found that 880 mV gives this equilibrium and thus this voltage is chosen as bias for the second stage. Note that this peak will shift somewhat by changing the input matching. 880 mV is in any case a good compromise between noise and gain for the second stage.

Scaling the Transistor

Scaling of the transistor in the second stage is primarily done to achieve noise matching. In addition to this, the power consumption must be kept low. The total number of emitters are tuned to be 8 in MWO and can thus be realized by a single transistor with $N_x = 8$. This places GMN fairly close to the center without sacrificing to much power consumption. The emitter length is kept at 0.48 µm due to the noise performance.

Power consumption is approx. $4.92\,\text{mA} \times 1.2\text{V} = 5.9\,\text{mW}$ after scaling to 8 emitters.

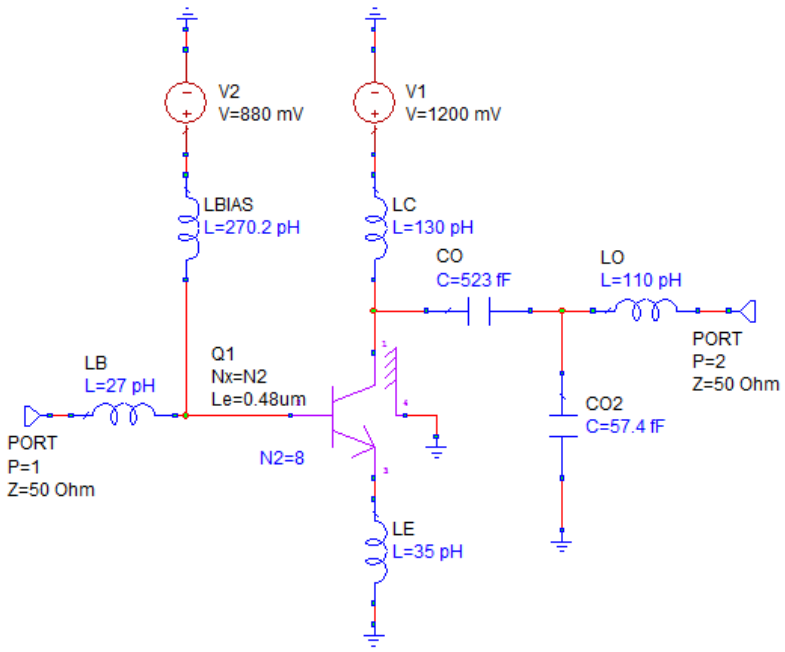


Figure 5.11: Schematic of second stage with matching network

Emitter Degeneration and Matching

Emitter degeneration and matching networks are implemented in the same manner as for the input stage. The *K*-Δ-*test* shows unconditional stability for the whole bandwidth due to the use of emitter degeneration. Matching is not fine tuned at this point since the cascading of several stages will have great influence on the matching conditions.

Figure 5.12, 5.13 and 5.11 shows the resulting s-parameters, frequency response and schematics. Both S_{11} and S_{22} are below -10 dB from 57 GHz to 66 GHz. In addition, noise is well matched and gain is relatively high.

5.6 Output Stage Design

The most important parameter for the output stage is gain, and thus the output stage parameters should be optimized for maximum gain. Noise is now suppressed by the gain of the first stages, so the NF of the output stage is not of great importance. However, the total gain of the two first stages is not enough to fully suppress the noise of the last stage. Therefore, noise must also be considered.

The cascode topology has high gain and good reverse isolation and would therefore be ideal as an output stage. This topology was originally chosen but was later proven to provide insufficient bandwidth. This is elaborated in Section D. A common

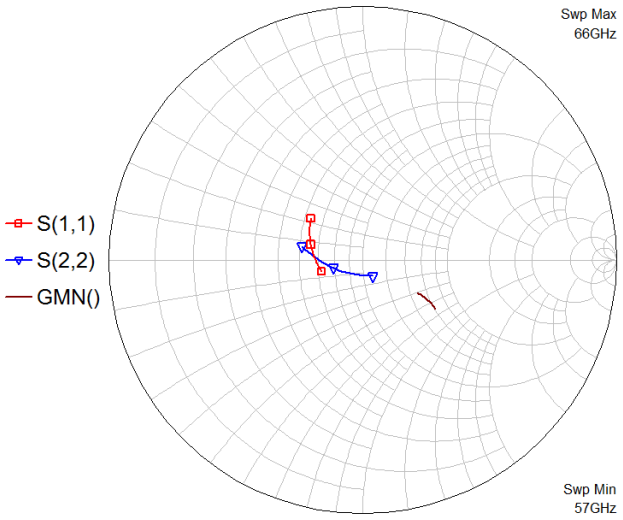
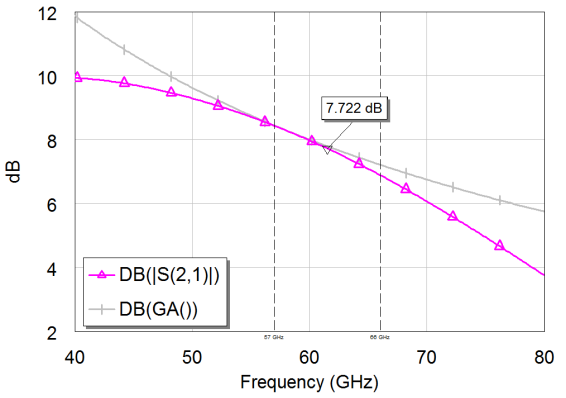
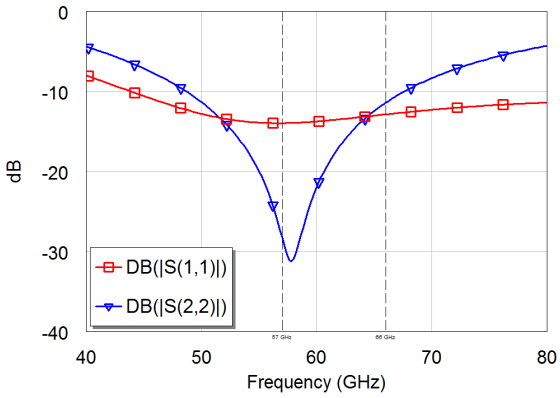


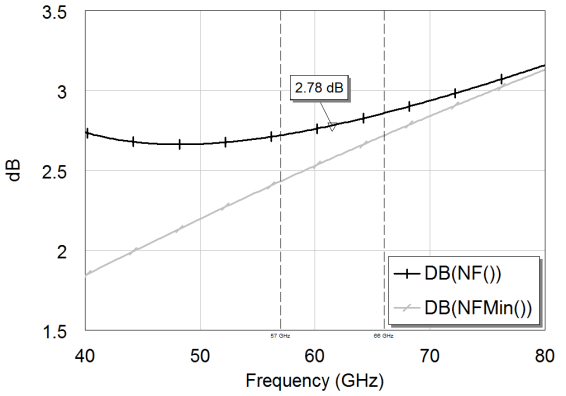
Figure 5.12: S-parameters for second stage



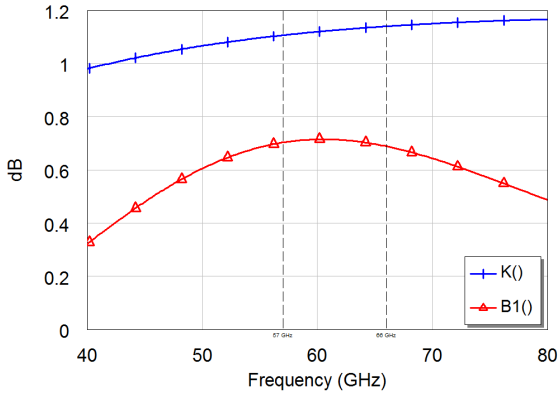
(a) Power gain and available gain.



(b) Reflection coefficients.



(c) NF and NFmin.



(d) $K - \Delta$-test

Figure 5.13: Simulations for second stage. The vertical dotted lines indicates where the $57 - 66$GHz bandwidth is.

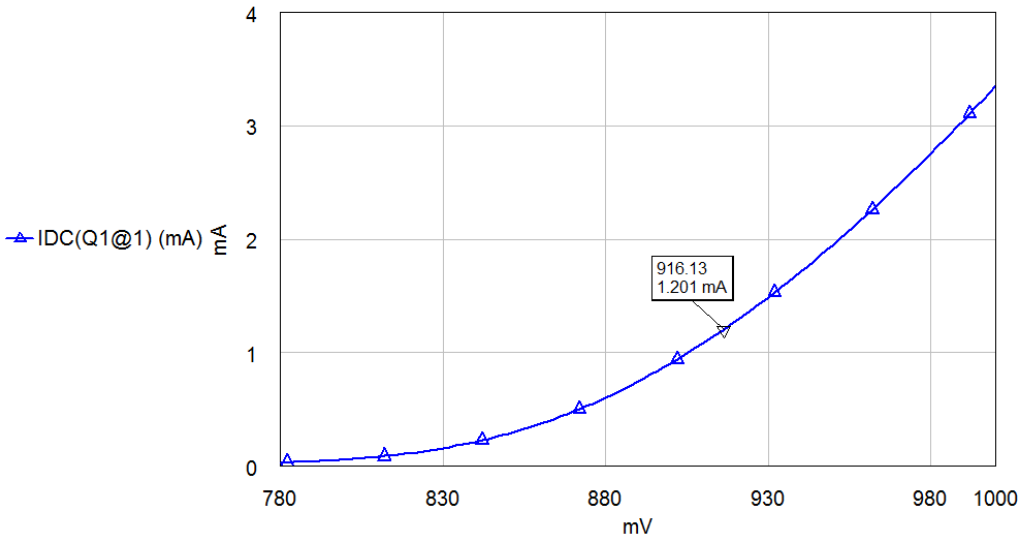


Figure 5.14: Collector current vs. bias voltage. A collector voltage of 916 mV will provide peak f_T.

emitter stage is therefore chosen for the output stage.

Bias Conditions

The process specification specifies the device current for maximum transit frequency. This current density will result in a maximum of gain and is thus of great interest for the output stage where gain is the most important parameter. I_C at peak f_T is specified to be 1.2 mA $\times$ N_x. Figure 5.14 shows a sweep of output current vs. bias voltage for the circuit in figure E.1. From Figure 5.14 it is clear that a bias voltage of 916 mV will provide peak f_T. Power consumption is however of great importance and thus some gain is traded for lower power consumption. 900 mV is a good compromise and is therefore chosen as bias.

Scaling the Transistor

Scaling of the output stage is primarily done in order to achieve low power consumption and adequate noise matching. In addition to this, the number of transistors will determine where S_{22} is located initially. S_{22} is intrinsically relatively high and thus increasing the number of transistors will improve the initial matching conditions. A total number of emitters of 4 seems like a good compromise, causing the power consumption of the output stage to be approx. 2.77 mA $\times$ 1.2V = 3.32 mW. The emitter length is kept at 0.48 µm.

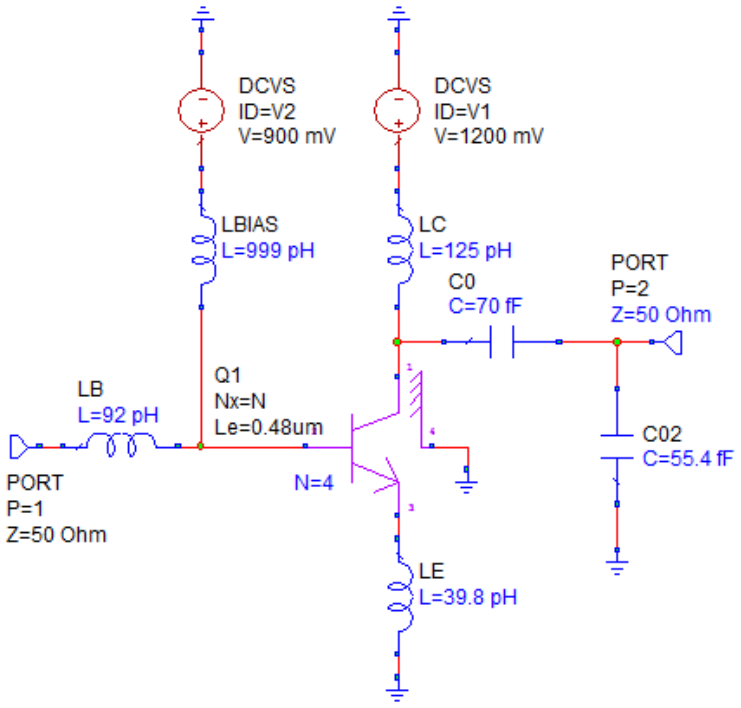


Figure 5.15: Schematic of output stage with matching network

Emitter Degeneration and Matching Network

Emitter degeneration is used to improve the stability of the amplifier. An emitter degeneration inductor of 39.8 pH is used in order to make the amplifier unconditionally stable for the whole bandwidth.

Matching network is implemented in the same manner as for the input- and second stage.

Figure 5.16, 5.17 and 5.15 shows the resulting s-parameters, frequency response and schematics. Both S_{11} and S_{22} are below -10 dB from 57 GHz to 66 GHz. In addition, the gain is high, noise adequately matched and power consumption is low.

5.7 Bias Circuit

The bias circuit is implemented using the circuit in Figure 5.18 (shown for 830 mV).

The base of the transistor in the amplifier is connected together with the base in the bias circuit. Since both the emitters are grounded, this configuration will *mirror* the

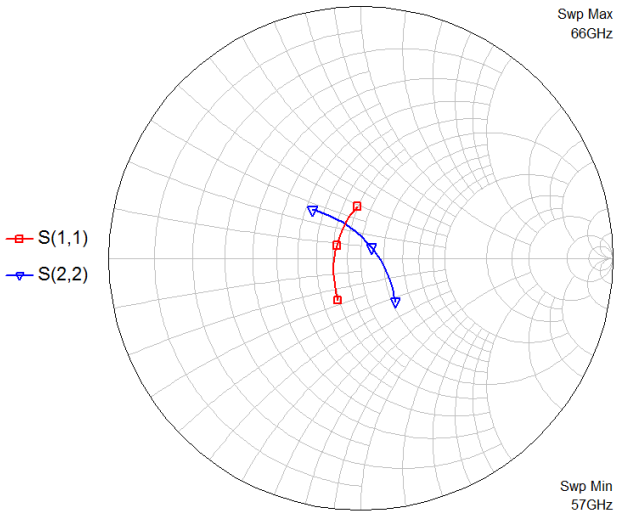
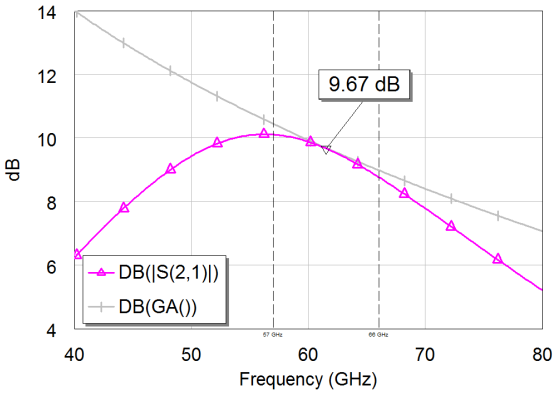
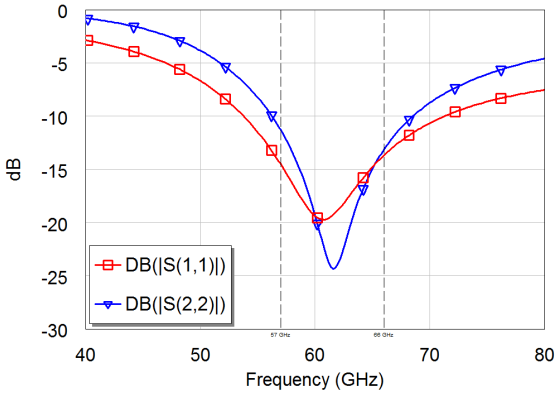


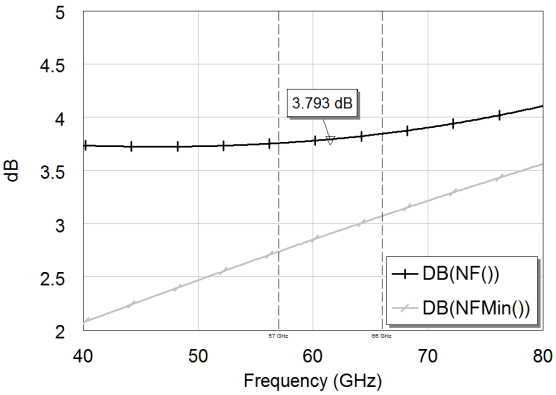
Figure 5.16: S-parameters for output stage



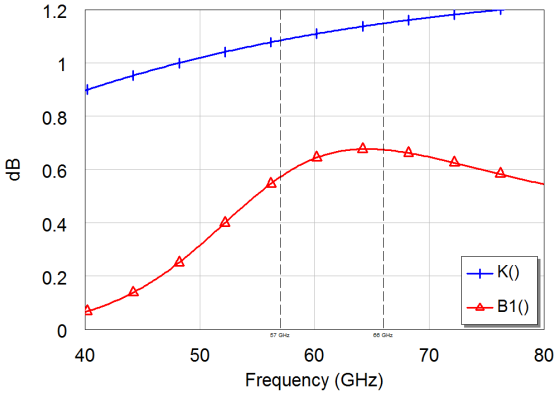
(a) Power gain and available gain.



(b) Reflection coefficients.



(c) NF and NFmin.



(d) $K - \Delta$-test

Figure 5.17: Simulations for output stage. The vertical dotted lines indicates where the $57 - 66$GHz bandwidth is.

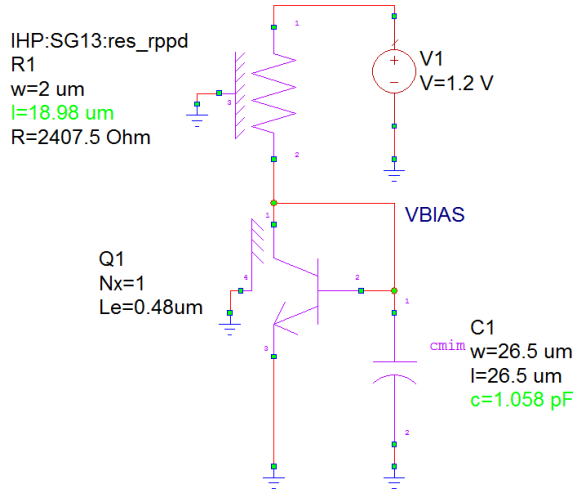


Figure 5.18: Bias circuit for 830 mV bias voltage.

current in the two transistors, forming a stable bias for the amplifier. This circuit is also known as the *widlar current source*. The current is set by the resistor R_1 and is adjusted to the required value for the desired bias current.

C_1 is used for noise suppression and provides a low impedance path to ground for higher frequencies at the output node.

5.7.1 Bias Circuit Temperature Dependency

The output voltage of the bias circuit is highly sensitive to temperature due to the temperature dependency of the bipolar transistor. Since both the bias transistor and amplifier transistor is operated in the same temperature environment, the bias voltage relative to the temperature will still be stable. There will, however, be an increase in bias current with increasing temperature and this will lead to different bias currents for different temperatures. This problem may be partially compensated by choosing a resistor with a positive temperature coefficient in the bias circuit. Figure 5.19 shows the bias current in the amplifier transistor ($m = 1$, $N_x = 1$) for a temperature range of $0°C - 100°C$. Each trace correspond to a specific type of resistor. The three available types of resistors exhibit different temperature coefficients. By choosing the Rsil resistor it is possible to minimize the current drift in temperature. This does, however, come at the expense of less precision, as the sheet resistance variations are higher than for the Rppd resistor. The low sheet resistance of Rsil will also result in a much larger resistor.

Rppd is therefore chosen for the bias circuits, as this will provide better precision as well as reduced size.

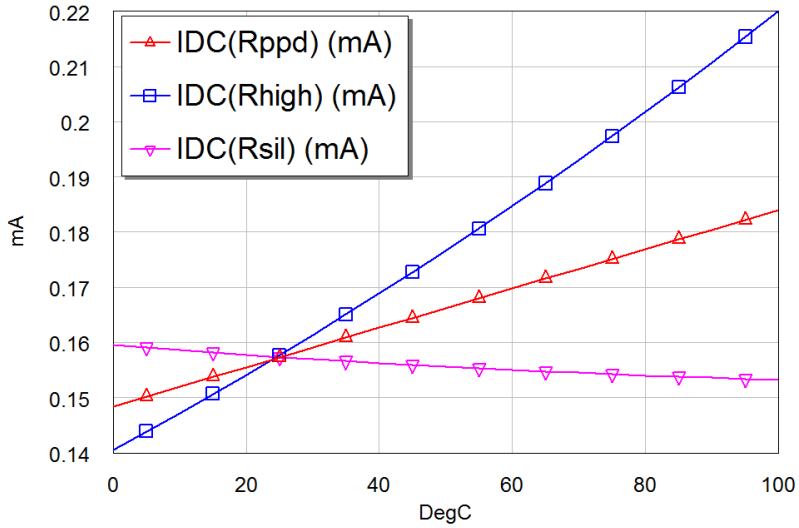


Figure 5.19: Temperature sweep of bias current for different resistors.

5.8 Multistage Design

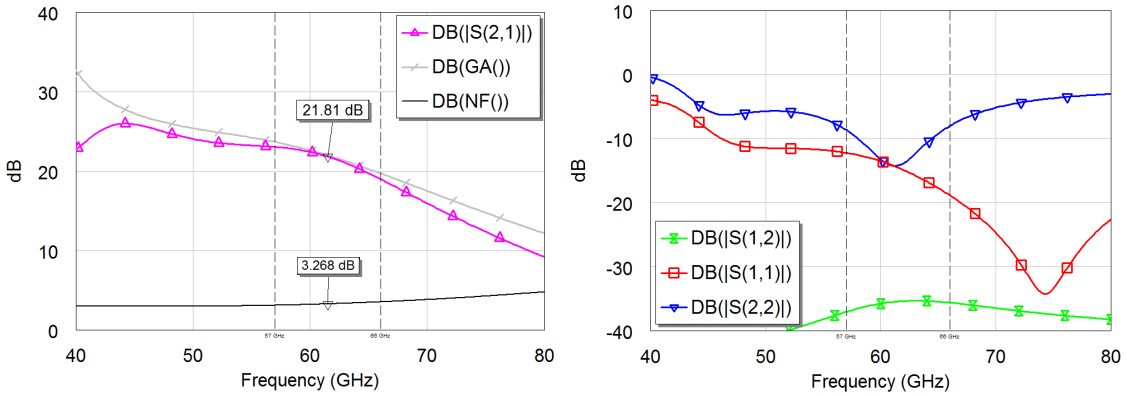
After designing the stages separately, all stages are combined to a multistage design, simply by cascading all stages. Figure 5.20 shows the frequency response for the resulting multistage amplifier.

It is clear that the output stage matching is insufficient since S_{22} is above the -10 dB line. Allthough S_{11} are well below -10dB, the minima is located at approx. 72 GHz. This could be improved to make the matching better at 61.5 GHz. Gain and noise is good and thus improvements should be done to other parameters.

All single stages are matched to approx. 50 Ω and thus the interstage matching should be fairly good. By adding gamma probes, the internal reflection coefficients can be assessed. The probes are added in series with the input and output of the active devices (in the base and at the collector at each transistor interstage). Figure 5.21 shows the port parameters and internal reflection coefficients in the smith chart. If the reflection coefficients of the gamma probe is conjugately matched, this would mean that power match is achieved. One of the reflection coefficients on each gamma probe is therefore showed conjugately so that it is easy to see if they are conjugately matched.

As seen in the smith chart, both S_{11} and S_{22} has potential for improvement. The internal reflection coefficients also shows that the internal matching could be improved. GMN is very close to center, indicating good noise matching.

The power consumption of the multistage amplifier with bias circuitry is now 14.4 mW, slightly higher than the desired power consumption of 12 mW.



(a) Port parameters and NF.

(b) S_{11}, S_{22} and S_{12}.

Figure 5.20: Simulations for initial multistage amplifier. The vertical dotted lines indicates where the $57 - 66$GHz bandwidth is.

Since the single stages are simply cascaded together, some of the components are now excessive, and thus the matching networks may be improved.

5.8.1 Improving the Initial Design

As discussed in the previous section, there are several parameters that need to improve. This list summarizes several improvements done to the design.

Remove excessive components Excessive components in the matching networks are removed in order to reduce the complexity of the circuit.

Improve S_{11} and S_{22} The input and output reflection coefficients are improved to accommodate -10 dB between 57 GHz and 66 GHz. Attempts on getting this bandwidth for S_{22} proved to be difficult but by changing the internal matching networks to t-networks, a bandwidth of 10.3GHz was achieved between 57.2 GHz and 67.5 GHz. S_{22} at 57 GHz is still -9.8 dB which is sufficiently close to -10 dB, since the -10 dB limit is a conservative number. This is most likely to be changed when real components are included at a later point. T-networks are chosen because they provide the required DC-block as well as providing an extra degree of freedom regarding matching.

Note that altering the output- and input reflection coefficients also changes the internal reflection coefficients since S_{12} is high for the CE-stage. The amplifier is therefore extremely sensitive to all changes in the matching network. Matching of all reflection coefficients is performed simultaneously using manual tuning and thus every change requires minor changes to almost every other component.

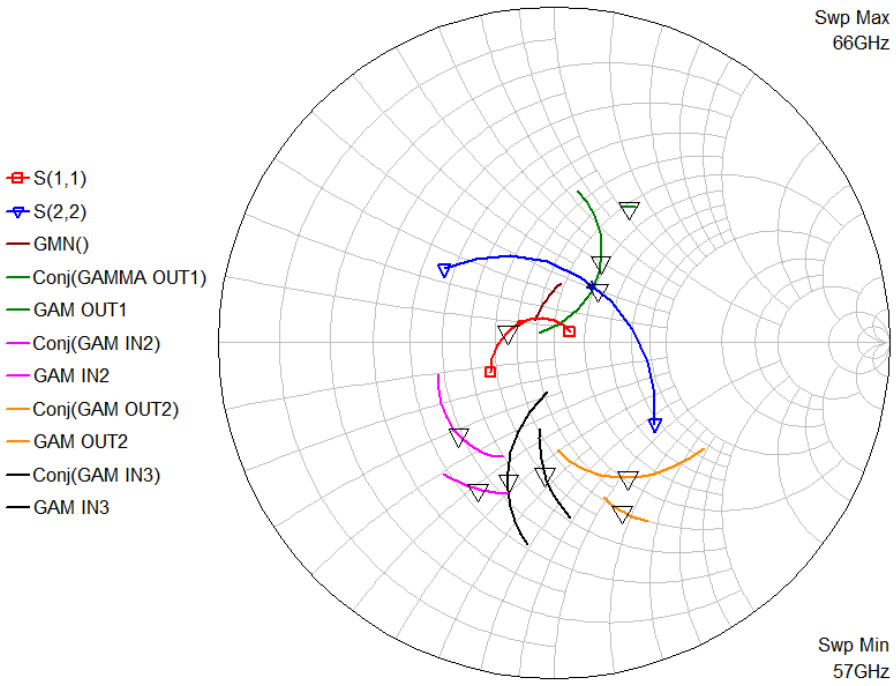
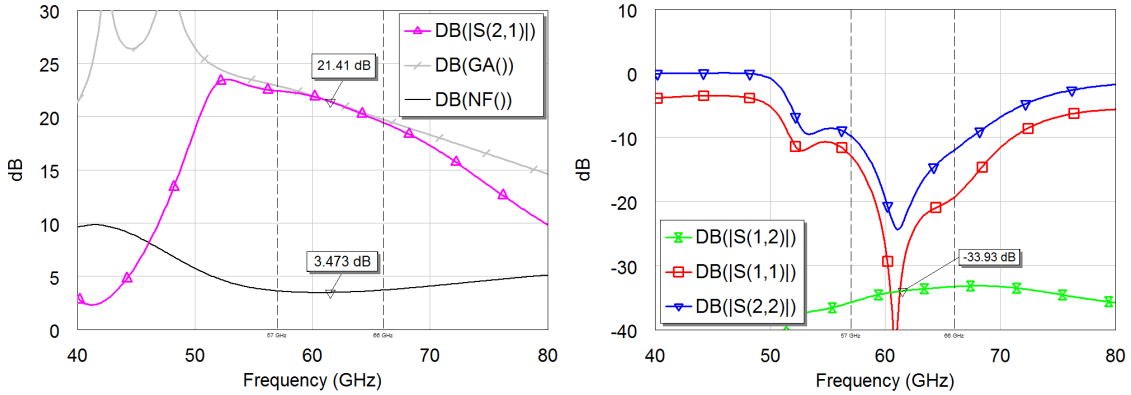


Figure 5.21: Port parameters and internal reflection coefficients for multistage amplifier. OUT1 indicates on output of stage 1, IN2 is input of stage 2 etc.

Improve interstage matching The interstage matching was initially performed at 50 Ω, but this is not necessary and may add some unwanted complexity. Therefore, matching interstage could be performed towards an arbitrary impedance level that is easy to achieve (since there are not any interfaces towards 50 Ω interstage anyway). The interstage matching was improved by adding T-networks between the stages. These t-networks form back-to-back pi-networks between the transistors, creating an extra degree of freedom for matching purposes. Some complexity is also added, making the matching more time consuming. Improving this matching added some gain to the amplifier making it possible to reduce the power consumption slightly.

Reduce power consumption By reducing the bias voltage for the output stage from 900 mV to 880 mV, the power consumption was reduced to 12.6 mW. This is somewhat above the 12 mW goal, but this is done in order to have some headroom on gain and noise before adding lossy passive components.

Several iterations have been done with improvements on different parameters. In the end, it is really down to what sacrifices that are acceptable on the different parameters. Some of the designs have better noise performance, but suffers from less bandwidth or less gain and vice versa. The final design is a compromise between all parameters.



(a) Port parameters and NF. **(b)** S_{11}, S_{22} and S_{12}.

Figure 5.22: Simulations for initial multistage amplifier. The vertical dotted lines indicates where the $57 - 66$GHz bandwidth is.

Figure 5.22 shows the frequency response for the improved amplifier. Noise and gain are pretty similar to the initial design, but S_{11} and S_{22} are now below -10 dB in the frequency band of interest. The minima are however located somewhat below 61.5 GHz. This is done because it proved to be difficult to achieve -10 dB in the frequency band of interest unless the minima was located below 61.5 GHz. Reflections are still very low at 61.5 GHz so this should not represent a problem.

Figure 5.23 shows the smith diagram for the improved amplifier. The internal matching is now improved as seen by the gamma probes. Noise matching is still good and the input- and output reflection coefficients are much better.

A schematic of the amplifier is shown in Appendix A. The schematic also includes the gamma probes used for stability analysis and interstage matching.

5.8.2 Stability of Multistage Amplifier

In order to evaluate the stability of the multistage amplifier, the gamma probes are utilized as described in Section 4.3.2. Gamma probes are inserted in the base, emitter and collector of all transistors. The circuit is then simulated from 100 MHz to 100 GHz in order to ensure stability for all frequencies. Figure 5.24 shows G plotted in a polar plot.

As long as the curves does not encircle the -1 point in clockwise direction, stability is maintained. The emitter node of Q2 indicated by the light grey curve is enclosing the -1 point in *counter clockwise* direction and this is thus stable. All other curves are within the -1 point and therefore show stable responses.

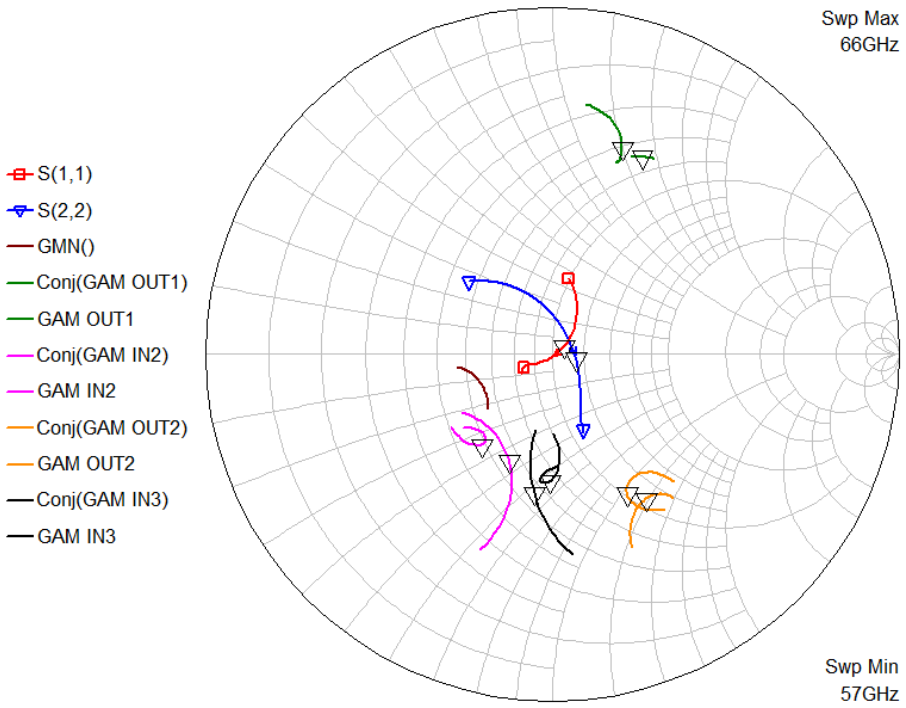


Figure 5.23: Port parameters and internal reflection coefficients for multistage amplifier after improvements. OUT1 indicates on output of stage 1, IN2 is input of stage 2 etc.

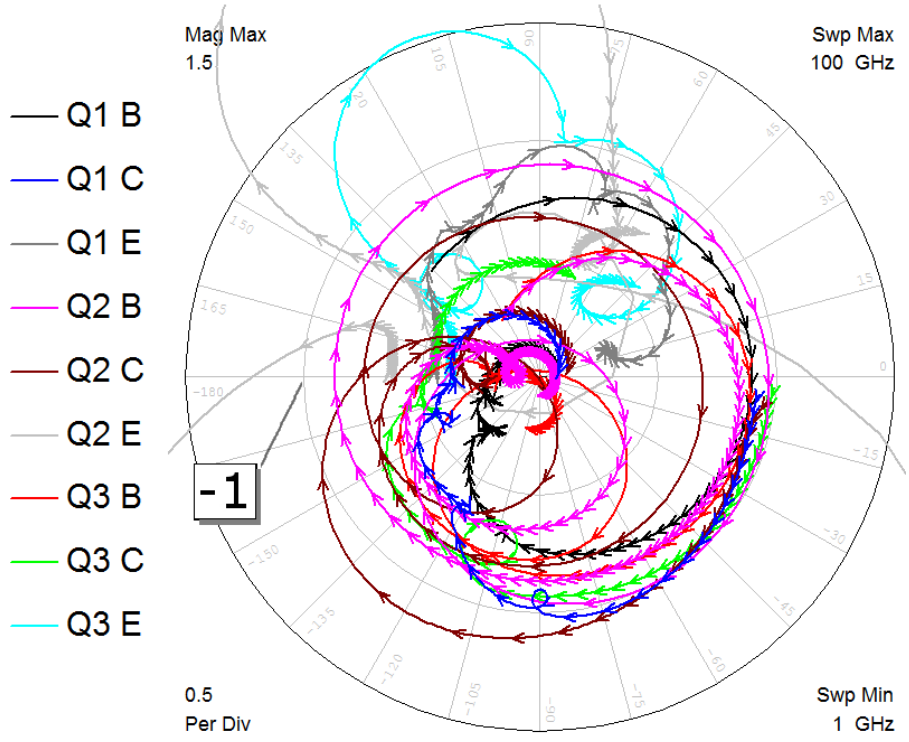


Figure 5.24: G for all gamma probes plotted in polar plot

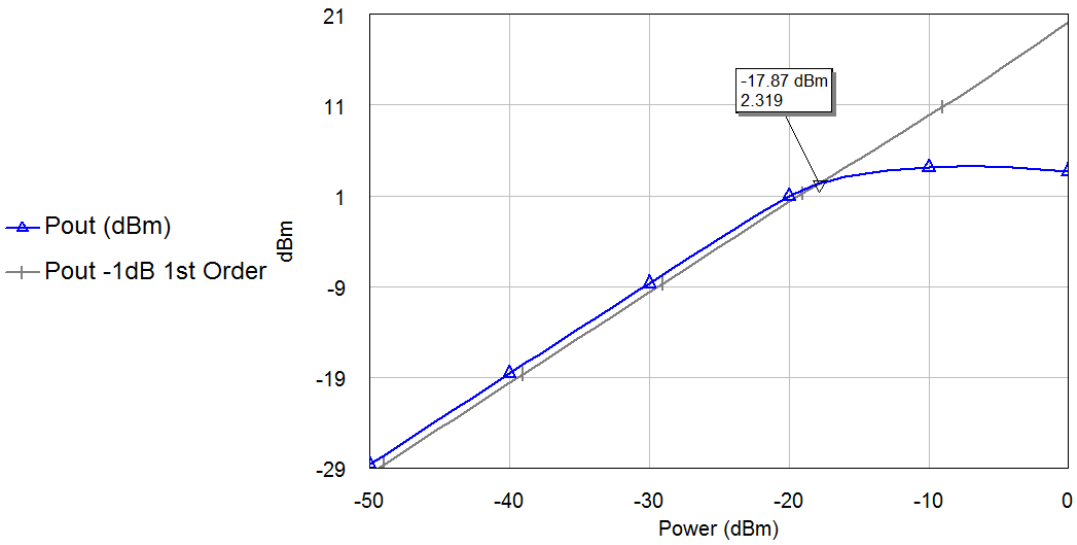


Figure 5.25: The compression point of the multistage amplifier is indicated by the marker. Sweep frequency is 61.5 GHz

5.8.3 Compression Point

In order to determine the large signal behavior of the amplifier, the compression point is simulated. This is done by sweeping the input power from −100 dBm to 0 dBm. The output power is then plotted against the input power in order to determine the 1 dB compression point. An additional linear 1st order response is plotted 1dB below the output power. The compression point is then easily recognized in the intersection of the plots. Figure 5.25 shows this simulation.

The marker indicates the compression point and the respective values for both the output- and input referred compression point. The input referred compression point is −17.8 dB and it is thus much higher than the maximum input power of −30 dB. Compression of the amplifier is therefore well controlled.

5.8.4 Intermodulation

As previosly discussed in Section 4.4.2, the third order interception point is measured in order to quantify the linearity of the amplifier. Figure 5.26 shows this simulation.

By comparing the output referred compression point of 2.3 dB with the OIP3 plot, it is apparent that the third order interception point is 15.3 dB and it is therefore within the requirements mentioned in Section 4.4.2.

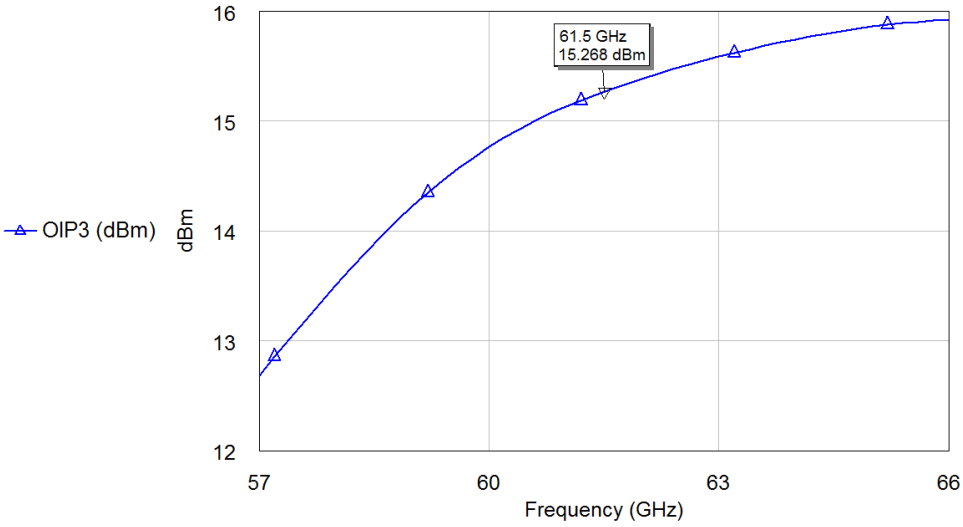


Figure 5.26: Third order interception point for the multistage amplifier.

5.8.5 Results

Table 5.1 summarizes the most important parameters for the multistage amplifier. All parameters are extracted at 61.5GHz. All goals except for the power consump-

Parameter	Value	Unit
Bandwidth	10.3 (57.2-67.5)	GHz
S_{21}	21.4	dB
S_{12}	-34	dB
NF	3.47	dB
OP1dB	2.32	dB
OIP3	15.3	dB
Power consumption	12.6	mW

Table 5.1: Simulated performance for multistage amplifier

tion is fulfilled for the multistage amplifier. In order to get below 12 mW, some performance may be traded. Both gain and noise is still well below the initial performance specifications, but some headroom is probably needed before adding lossy components. A minor adjustment in size or bias may be performed during layout in order to get below the 12 mW specification.

CHAPTER 6

Design Realization and Layout

This chapter describes the realization of the design with inclusion of real components and layout design.

6.1 Replacing Inductors With Transmission Lines

As previously discussed in Section 2.3.2, the inductors of the SG13S process provides to high inductance to be used with 60 GHz. As discussed in Section 3.6.2, transmission lines could be used as an inductive element and all inductors are therefore replaced with transmission lines.

The transmission line is by default routed in TopMetal1 with return path on Metal1.

The switch from inductor to transmission line is performed by replacing one inductor at a time and tuning the length of the transmission line in order to achieve the initial response. Since there is loss and parasitic capacitance present in the transmission line, the movement in the smith chart is not purely inductive. This means that one has to simultaneously tune both the transmission line and surrounding components to attain the initial response. The width of the transmission lines is chosen to be 5µm, as this provides low resistance and good current capability.

6.2 MIM Capacitors

All ideal capacitors are replaced with MIM capacitors. This imposes minimal changes in tuning, so no extra effort is needed in order to tune the amplifier.

The MIM capacitor is possible to draw in several different shapes, but a rectangular shape is chosen for its ease of design and good tolerance.

6.3 Thermal Noise From Transmission Lines

By introducing transmission lines with finite resistance, thermal noise is also added. This noise contributes to the overall NF of the system and thus the NF of the system is significantly higher after the introduction of transmission lines. We know from before that the gain in the first stage is slightly low. With the added thermal noise in the input stage, it is clear that the gain in the first stage must increase in order to reduce the noise relative to the signal. Three measures are taken to ensure low noise and low power consumption:

Increase bias for input stage The bias voltage for the input stage is increased from 830 mV to 850 mV in order to increase the gain. This improved the overall NF and gain. Power consumption has now increased to 14.4 mW, but the power gain is much higher than the specification.

Decrease bias for second stage In order to decrease the overall power consumption, some gain is traded for power consumption. The bias voltage for the second stage is therefore decreased from 880 mV to 850 mV. This reduces the power consumption to 10.4 mW.

Decrease the number of transistors in input stage It is found that decreasing the number of emitters in the input stage from 10 to 8, decreases the power consumption to 9.8 mW without sacrificing more than 0.1 dB in total NF.

6.4 Meandered Transmission Lines

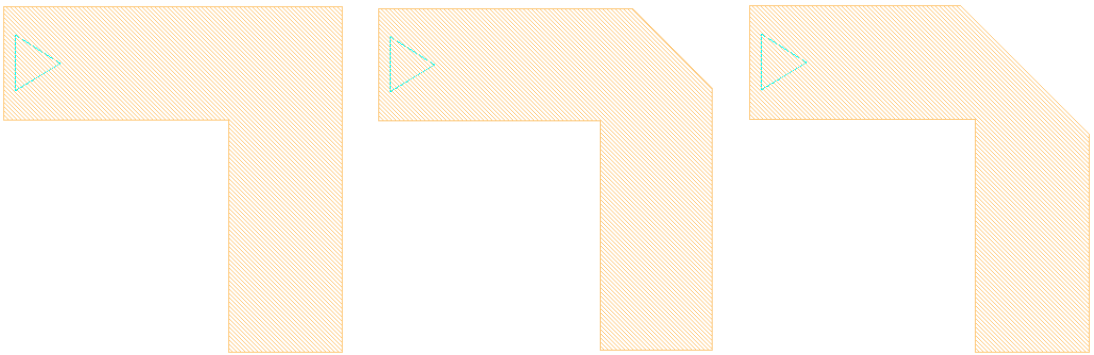
In order to reduce substrate area and hence the size of the amplifier, the transmission lines are meandered as shown in Figure 6.1.

This routing will cause capacitive coupling between different parts of the line leading to a change in the impedance of the line. This coupling is unaccounted for in the simulation model, and thus EM simulation must be used in order to tune the impedance of the line.

Another problem with meanders is that the extra metal in the bends cause excessive capacitance. This change in impedance will lead to reflections. The problem is minimized by using a mitered bend, as this will reduce the capacitance and keep the characteristic impedance more uniform.

Figure 6.1: Meander transmission line

MWO offers three different types of bends whereas one of the miter is a standard 90° bend and the two latter is respectively a regular mitered bend and an optimized mitered bend with less capacitance. These are showed in Figure 6.2. The regular mitered bend and the optimized bend shows very similar response and thus the regular mitered bend is used. In order to compensate the previously mentioned problem regarding excessive capacitance, the length of the lines are tuned while routing.



(a) Regular 90° bend **(b)** Regular mitered bend. **(c)** Optimized mitered bend.

Figure 6.2: Different types of bends provided by Microwave Office.

6.5 Layout of Bias Circuit

The layout of the 850 mV bias is shown in Figure 6.3.

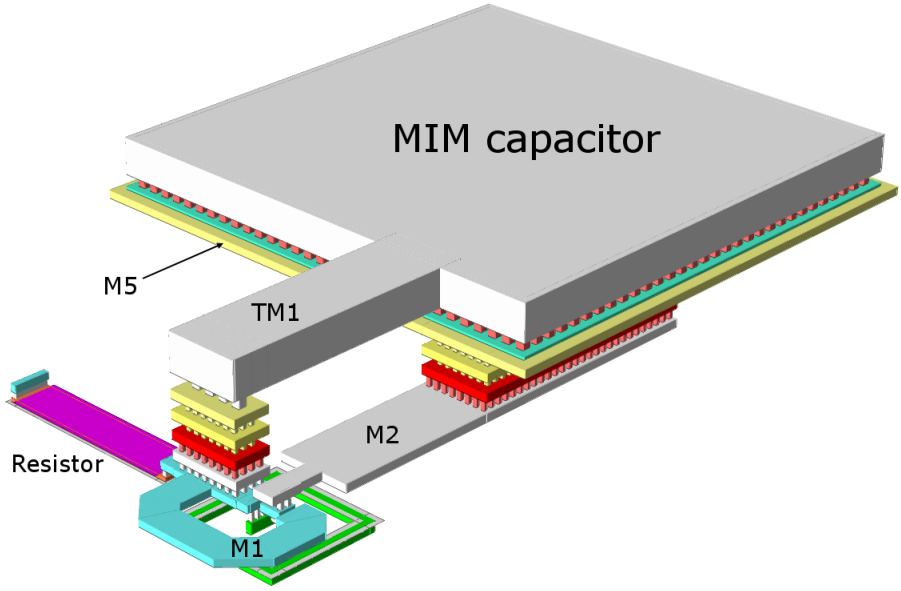


Figure 6.3: Layout shown for 850 mV bias.

The MIM capacitor connections is routed at TopMetal1 and Metal2 whereas the transistor connections is routed on Metal1. Since the current is low for the bias circuit, the width of the traces are not critical and can be kept small. The via area is, however, kept wider in order to increase the number of vias and hence the reliability of the connection.

Layout for the 880 mV cell is similar to the 850 mV cell. See Appendix B for more detailed images of the bias layouts.

6.6 Layout of Multistage Amplifier

Figure 6.4 shows the proposed layout.

V_{cc} and GND is not routed at this point, but a power bus will be added on TopMetal2 and a ground plane is to be added on Metal1. Since Metal1 is also used for connections on the transistor one has to pay attention to ground routing in close proximity to these terminals.

In general, signal routing is kept on Metal2 and higher layers while transmission lines is routed on TopMetal1. This ensures that the ground return path on Metal1 is continues. The width of the traces are kept at 5 µm as this ensures sufficiently low resistance and high current capability. The maximum AC current in the output stage is 6.3 mA and the traces are sized to withstand 10 mA. Via areas are made large in order to increase reliability and to keep the resistance at a minimum.

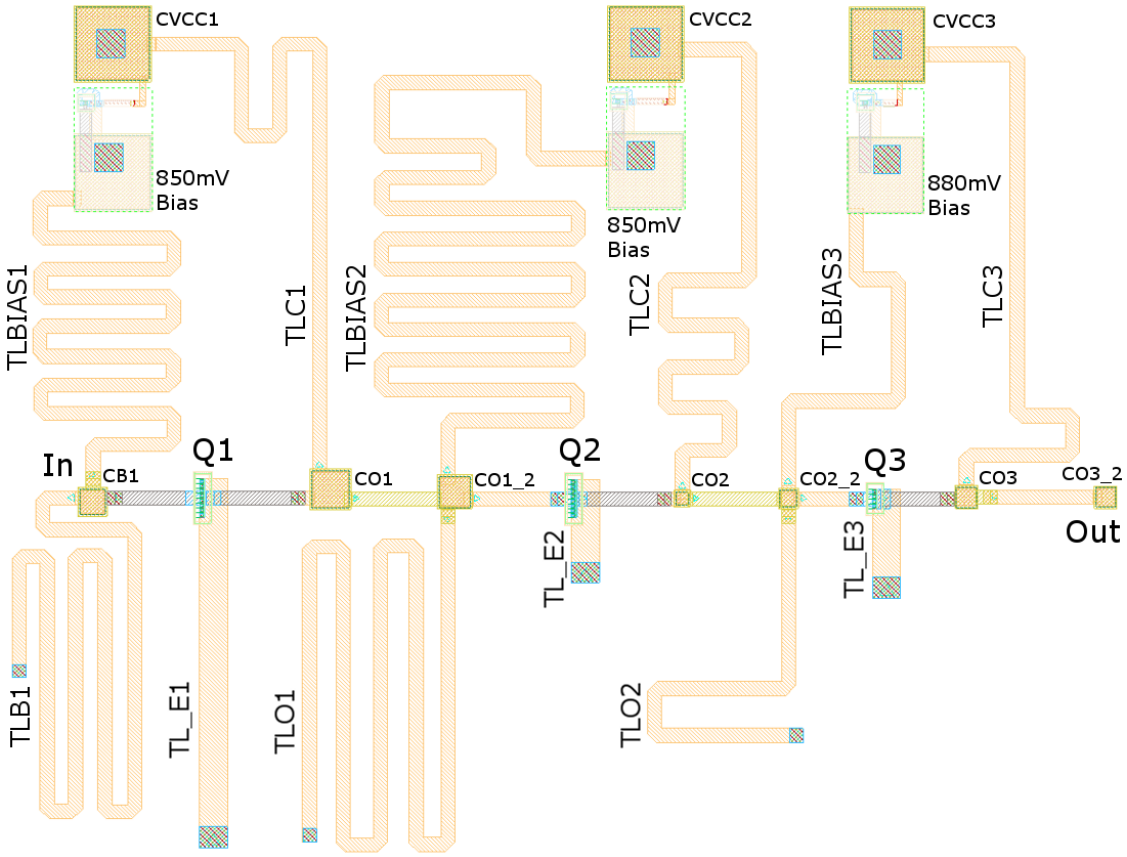
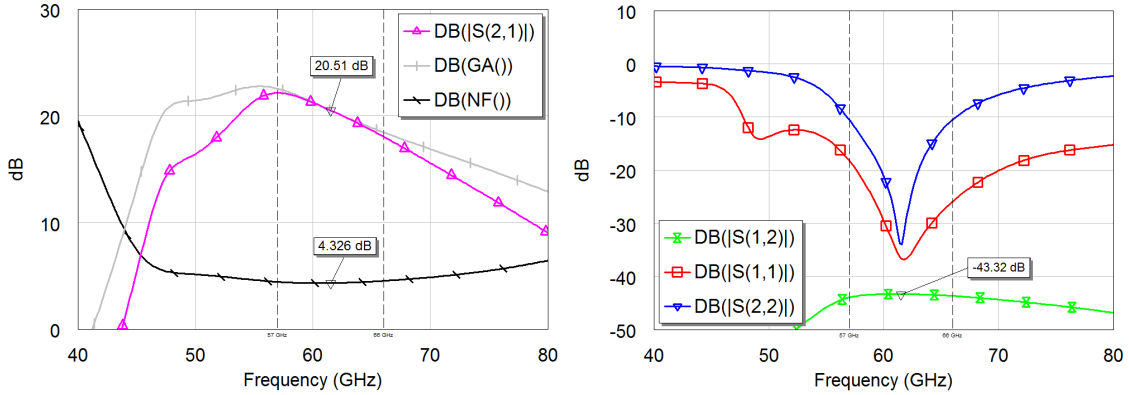


Figure 6.4: Layout for the multistage amplifier. Vcc and ground plane is not showed. See Appendix A, Figure A.2 for schematics.

In order to get sufficient spacing between the transistors and matching networks, short transmission lines of 30 µm is added between the components. These are also added in the schematic, so that the design will simulate more realistic. Spacing between lines on the input and output of the transistors are also kept as far away as possible to reduce the coupling between the nets. This makes the spacing between adjacent components in the interstage matching tighter, but this is simply a tuning issue.

At this point it would be beneficial to perform electromagnetic simulation for the different structures in the design. This is needed in order to account for the coupling in meandered lines and adjacent structures so that the matching networks can be tuned. Further optimization of the layout is then possible. Due to time constraints, EM simulation is not performed.

The size of the layout is currently 411 µm × 320 µm = 132µm^2. This area may be reduced if the EM simulation indicates that the spacing between structures is excessive.



(a) Port parameters and NF. **(b)** S_{11}, S_{22} and S_{12}.

Figure 6.5: Post layout simulation of port paramters for multistage amplifier. The vertical dotted lines indicates where the $57 - 66$GHz bandwidth is.

Detailed pictures of the layout is found in Appendix B.

6.7 Post Layout Simulation Results

The simulations performed in Chapter 5 is redone in order to verify correct behavior after layout. Post layout port paramters are shown in Figure 6.5, while the rest of the simulation plots are shown in Appendix C. Table 6.1 summarizes the post layout performance of the amplifier.

Parameter	**Value**	**Unit**
BW	9.5 (56.8-66.3)	GHz
S_{21}	20.5	dB
S_{12}	-43.3	dB
NF	4.3	dB
OP1dB	-1.7	dB
OIP3	9.4	dB
Power consumption	9.8	mW

Table 6.1: Simulated performance for post layout multistage amplifier

The most noticeable changes from the pre layout simulations is that the NF has increased due to the thermal noise in the transmission lines. This led to a change in gain structure that also altered the OP1dB and OIP3 as well as power gain.

Note that the compression point must be considered for the frequency with highest gain. This frequency will set the lowest input referred compression point and thus set the limit for the dynamic range of the input signal. The input referred compression

point at 57 GHz is approximate −23 dB and is therefore well above the required −30 dB limit. NF is well matched with its minima at 61 GHz and is within +0.2 dB in the whole bandwidth.

The gain peak of the amplifier is located at 57 GHz, with a variation in gain of 4 dB in the frequency band of interest. This variation in gain may cause problems for higher order modulation schemes, but for OOK this is considered to be sufficient. This is elaborated in Section 7.2.

By comparing the results with the specifications in Table 1.1, it is clear that all specifications is fulfilled.

CHAPTER 7

Discussion

Even though the design presented in Chapter 6 fulfills all specifications, a discussion of the results and work presented is needed. The aim of this is to address topics that needs to be considered before proceeding with production and to determine uncertainties in the design.

7.1 Performance Comparison With Published LNAs

Table 7.1 shows a performance comparison of this work with current published SiGe LNAs. The performance listed for this work is showing comparable performance when listed with work done in similar SiGe processes. This confirms that the design is performed using a valid design methodology and also indicates that performance is optimized. Note, however, that some of these amplifiers also include EM simulation and measured results. The gain and NF may change after EM simulation and thus it may compare differently. In addition, every system has different requirements in

	This Work	[9]*	[19]	[23]	[26]	[8]
SiGe Technology	0.13 µm	0.12 µm	0.13 µm	0.13 µm	0.13 µm	0.25 µm
Frequency [GHz]	**61.5**	61.5	77	60	60	61
S_{21} [dB]	**20.5**	17	21	20	21	18
NF [dB]	**4.3**	4.5	5.3	5	5	6.7
P_{DC} [mW]	**9.8**	10.8	60	27	11	20.25

*Measured values

Table 7.1: Performance comparison with current published SiGe LNAs.

terms of gain flatness, area, bandwidth etc. A direct comparison of gain, noise and power consumption may not be completely fair to all designs. By comparing the simulated- and measured response in the listed papers, it looks like it is possible to obtain performance with little deviation from simulations.

The main difference between this work and the amplifiers compared is mainly the location of the gain peak and gain flatness. Experiments with moving the gain peak towards 61.5 GHz has shown that the NF increases, and thus a higher, more comparable NF may have been achieved by a centered gain peak.

7.2 Design Trade-offs

Several design trade-offs are continuously discussed in the design chapters. This chapter will provide more insight in some of the design trade-offs that are made, and discuss the pros and cons of these trade-offs.

As seen by Figure 6.5, the frequency response has a relatively large variation of gain between 57 GHz and 66 GHz. One of the disadvantages with large gain variations is that it will cause an irregular baseband signal after the down-conversion [3]. Figure 7.1 shows how the input signal is affected with both a flat gain curve as well as a gain curve with large variations.

As seen by Figure 7.1, the variations in gain is causing an irregular signal after down conversion. This irregularity in the baseband signal will cause problems for higher order modulation schemes as some modulation schemes require high linearity. On-off-keying is one of the most simple forms of modulation and thus it does not require high linearity. The gain flatness is therefore not of great concern in terms of modulation.

Large variations in gain does, however, introduce problems related to the dynamic range. Since there is large variations in the output signal of the LNA, the subsequent circuits must handle a higher dynamic range. In addition to this, the input referred compression point of the LNA is determined by the frequency with highest gain. This must be taken into consideration when determining the compression point of the LNA. The design of the mixer must also account for this increase in dynamic range.

In order to design the amplifier for more flatness in the gain curve one must place the gain peaks for the different stages at different frequencies. This will result in a flatter gain curve at the cost of less gain. In order to increase the gain one could increase the quiescent current. This will in turn increase the power consumption. One other solution would be to add a fourth stage. This will add some complexity as well as increasing the power consumption. Since a flat gain curve is not required for the on-off-keying modulation scheme, it is considered to be more advantageous

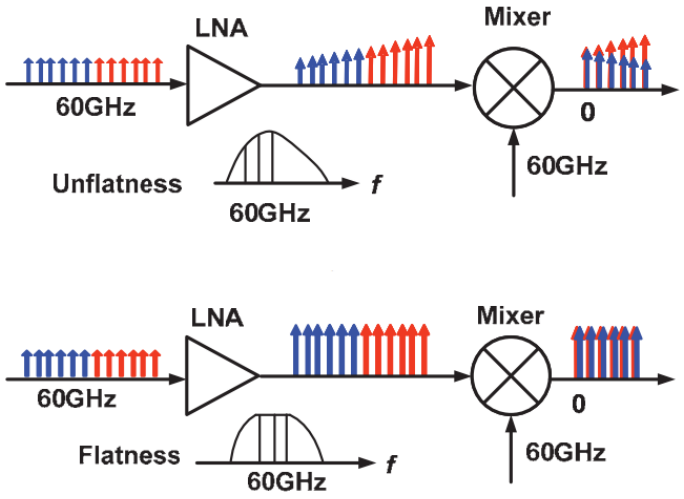


Figure 7.1: Consequence of gain variations [3]

to design for low power consumption and low complexity.

The NF of the amplifier is well below the specifications. This means that it is possible to trade some noise for less power consumption or more gain. Decreasing the size of the input- and second stage transistors will result in lower power consumption and higher NF while decreasing the emitter degeneration in the input stage will result in higher gain at the cost of more noise. Since the gain is already sufficiently high, a reduction in power consumption would be preferred.

The current area of the LNA can be reduced somewhat at the cost of more narrow response for S_{22}. This is done by removing the back-to-back pi-networks in the inter-stage matching, saving two lines and two capacitors. The area reduction is, however, not very large so this should not be considered unless area is very important.

7.3 Simulation Model Accuracy

The foundry provides lower and upper limits for model validity for the transistors. These values are confidential and will not be disclosed. In general, all simulations are within these values. There is, however, one exception for the current in the output stage. Simulations, especially high input power simulations, must therefore be verified by measurements.

Simulations within the limits are assumed to be accurate. This may not be the case for all simulations and thus measurements must be performed after manufacturing in order to characterize the accuracy of the simulations.

7.4 CAD Tools

The foundry provides process design kit (PDK) for several different CAD tools. The University of Bergen has been using Cadence Virtuoso for ASIC design and this was therefore chosen as design tool. Although Cadence offers a very comprehensive package with the Spectre RF option, we learned that the work flow provided with Virtuoso was very time consuming with respect to impedance matching. National Instruments offers Microwave Office (MWO) as a CAD tool specialized for RF and MMIC design. Microwave Office has very good integration with EM simulation and provides very fast simulations. In addition to this, MWO offers manual tuners in order to manual tune matching networks in realtime. This feature makes impedance matching of large circuits much easier. A switch was therefore made from Virtuoso to MWO after obtaining university licenses.

7.5 Future Work

A proposal for the layout is presented, but additional work is necessary before the block is ready for tape-out.

In order to gain more accurate simulation results before performing an EM simulation it is important to include physical structures from the layout in the schematic. Some of these elements are already implemented, but additional elements like junctions, width steps, vias etc. should be added in the schematic. This should be followed by am EM simulation in order to tune the matching circuits and determine coupling between different structures. This will probably make changes in the matching, and several iterations in layout may be needed.

A corner analysis must be performed in order to characterize the process-, voltage- and temperature variation impact on the design. In addition, a Monte Carlo simulation must be performed in order to characterize the sensitivity of the design with respect to tolerances on components. If problems regarding component sensitivity is detected, it is possible to perform a yield optimization by changing the nominal values of the components of interest.

All simulations are performed using ideal voltage sources with zero output impedance. This is not the case and thus a non-ideal voltage source must be used in order to account for voltage variations due to dynamic power consumption. The output impedance for the voltage supply must therefore be characterized and implemented in the simulations. This will also give more insight into possible stability issues caused by coupling through power- and bias networks.

CHAPTER 8

Conclusion

A thorough study of microwave theory has been carried out in order to obtain knowledge essential to RF- and low noise amplifier design. This theory forms the basis for designing a low noise amplifier operating at very high frequencies. The theory is also included in this thesis in order to provide readers with no previous experience within RF design an introduction to the field of microwave engineering.

Based on the previously attained knowledge, a 60 GHz low noise amplifier with 20.5 dB gain, 4.3 dB NF and 9.8 mW has been designed in a 0.13 µm SiGe BiCMOS process. The amplifier fulfills all specifications given. The results are based on post-layout simulations performed in Microwave Office. Although the results only shows simulated response, we have good reason to believe that these results can be realized by performing a thorough EM simulation and process variation simulation. If this is the case, the resulting amplifier will be very competitive to previously published low noise amplifiers.

APPENDIX A

Circuit Schematics

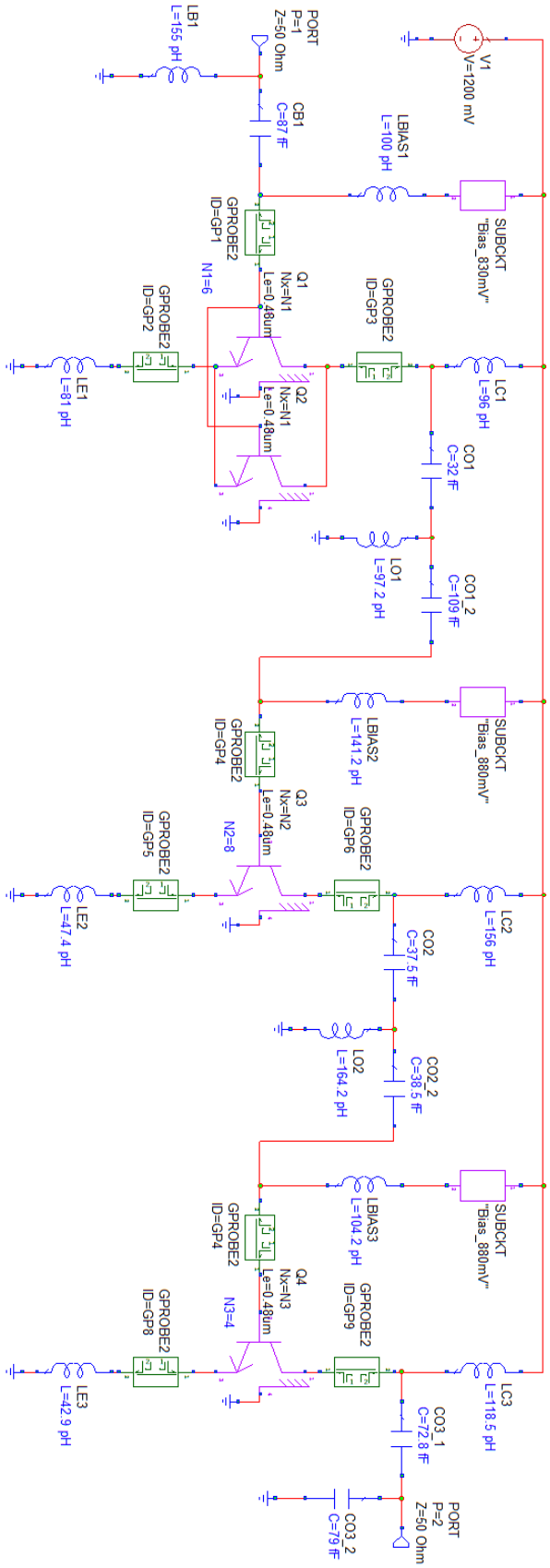


Figure A.1: Schematic of the multistage amplifier after improvements.

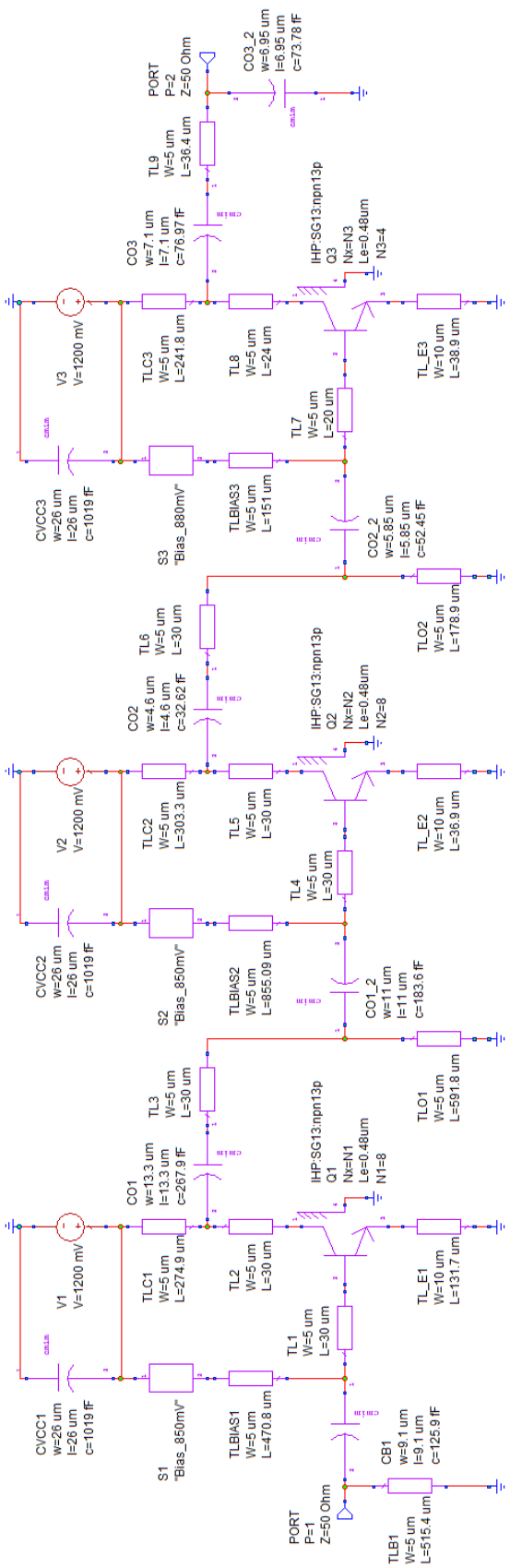


Figure A.2: Schematic of the multistage amplifier after layout. Note that CVCC1, CVCC2 and CVCC3 is added for decoupling.

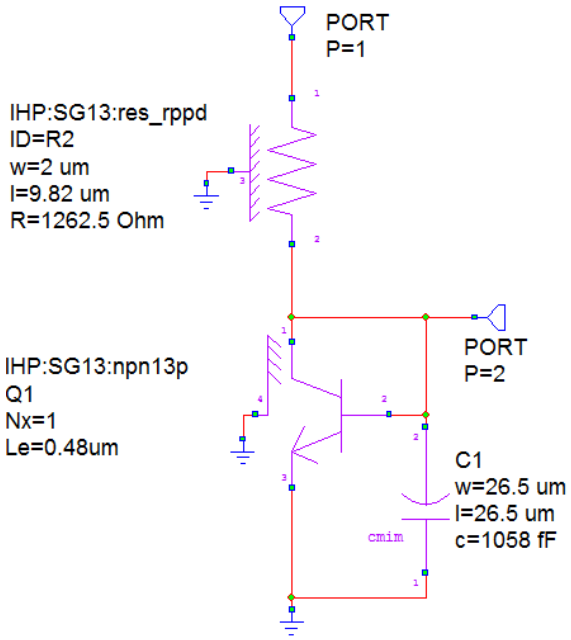


Figure A.3: Schematic of S1 and S2.

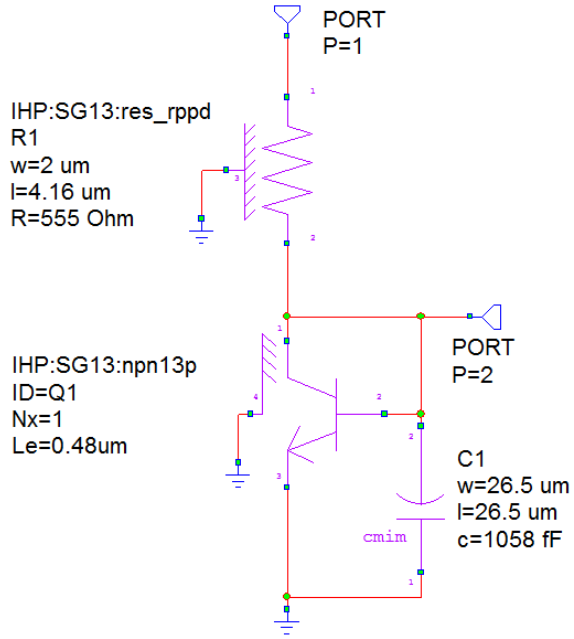


Figure A.4: Schematic of S3.

APPENDIX B

Layout

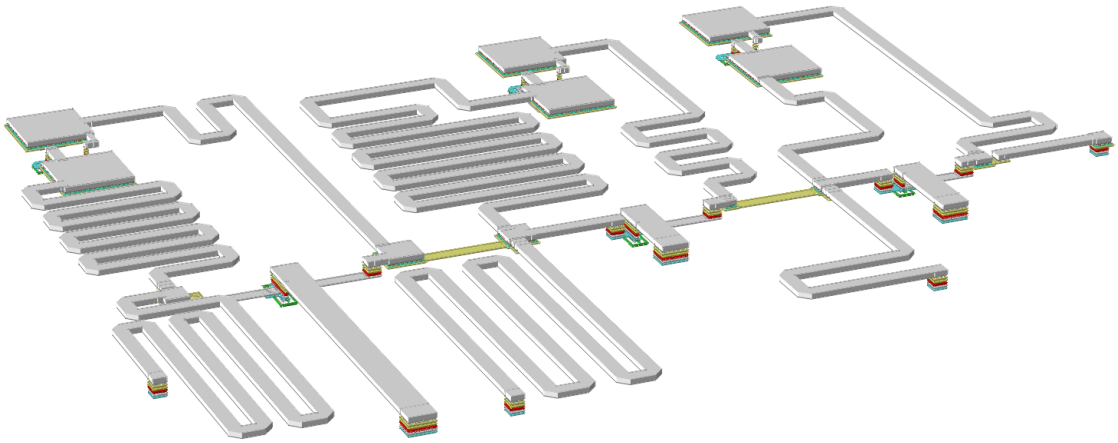


Figure B.1: 3D view of the multistage layout

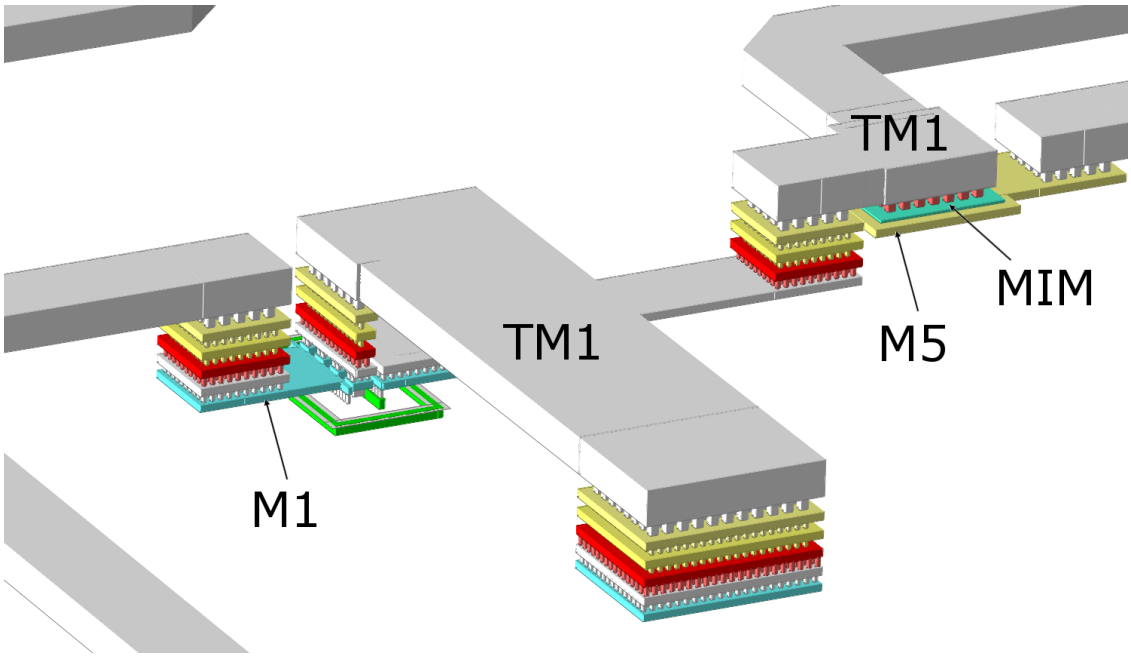


Figure B.2: 3D view of Q3 and the emitter line.

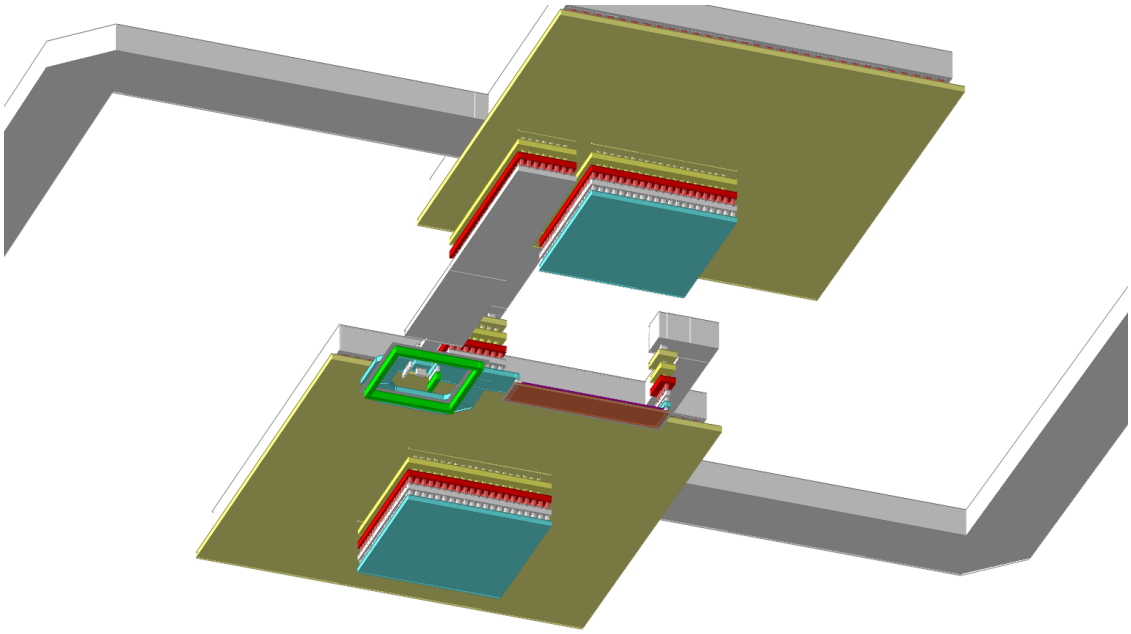


Figure B.3: 3D view of the underside of the decoupling capacitors on V_{cc} and bias voltage. Notice the ground connection vias from Metal5 to Metal1.

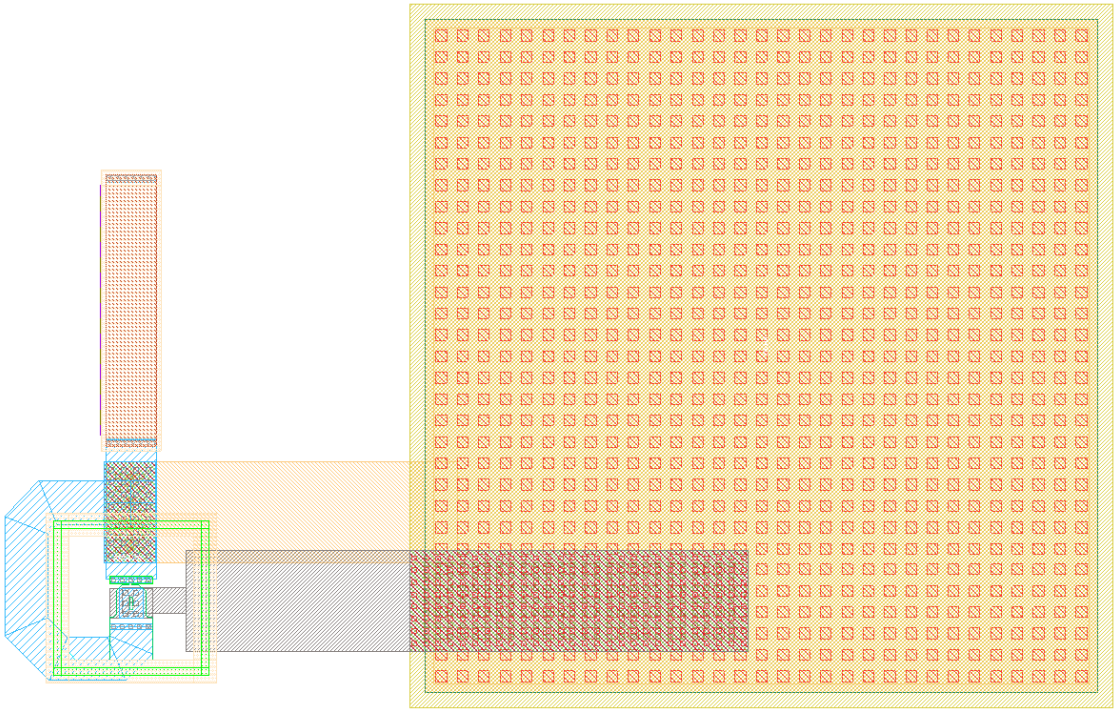


Figure B.4: Layout of 850 mV cell. The large block is the decoupling capacitor. The transistor is located in the lower left corner, with connections to both the resistor and decoupling capacitor.

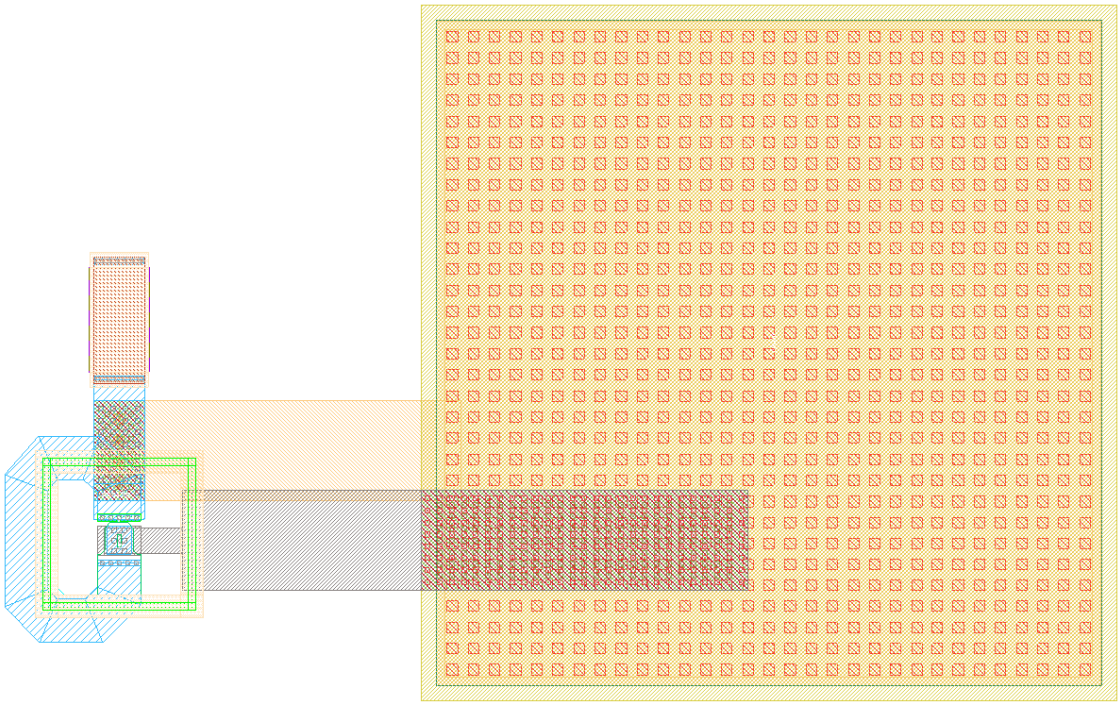


Figure B.5: Layout of 880 mV cell. The transistor is located in the lower left corner, with connections to both the resistor and decoupling capacitor.

APPENDIX C

Post Layout Simulations

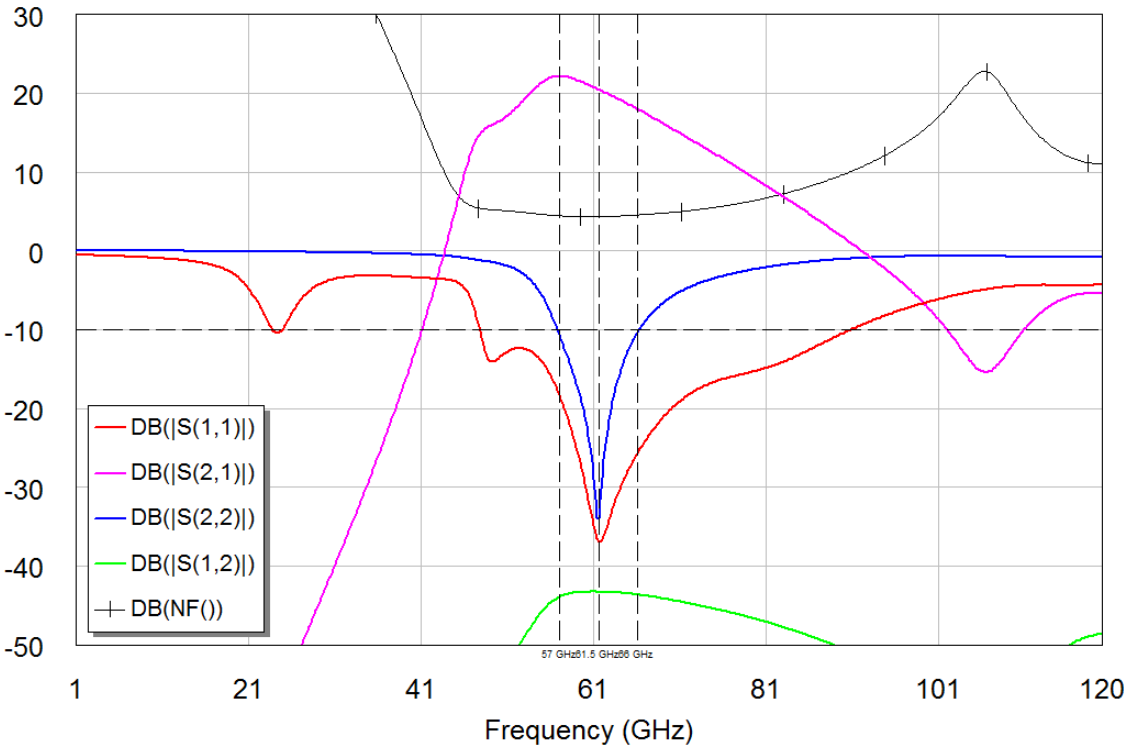


Figure C.1: Post layout simulation of port parameters from 1 GHz to 120 GHz. The horizontal dotted line indicates the -10 dB line and the vertical dotted lines indicates where the $57 - 66$GHz bandwidth is.

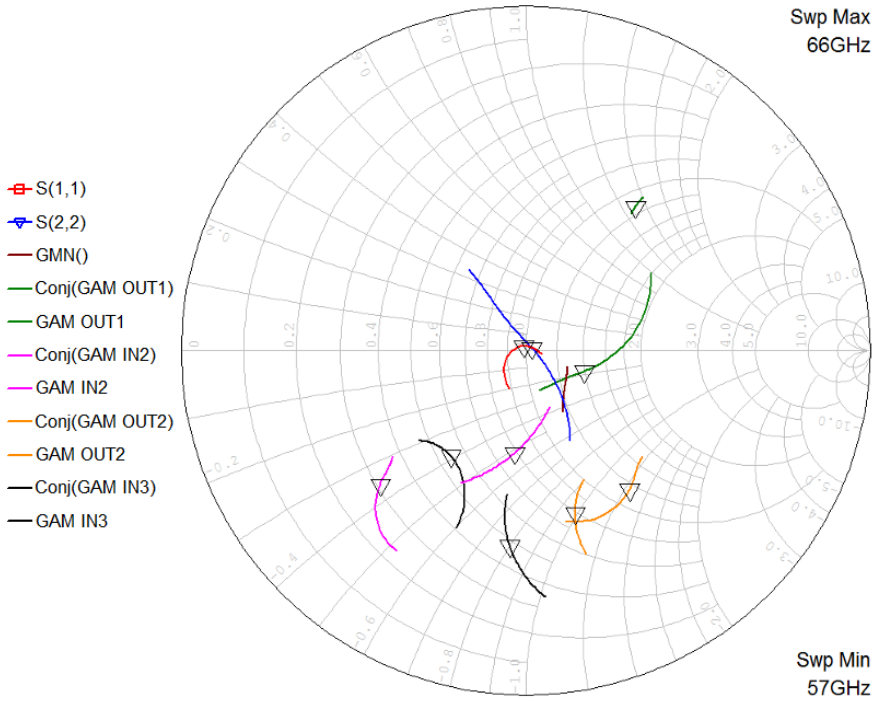


Figure C.2: Post layout simulation of gamma probes and reflection coefficients for multistage amplifier.

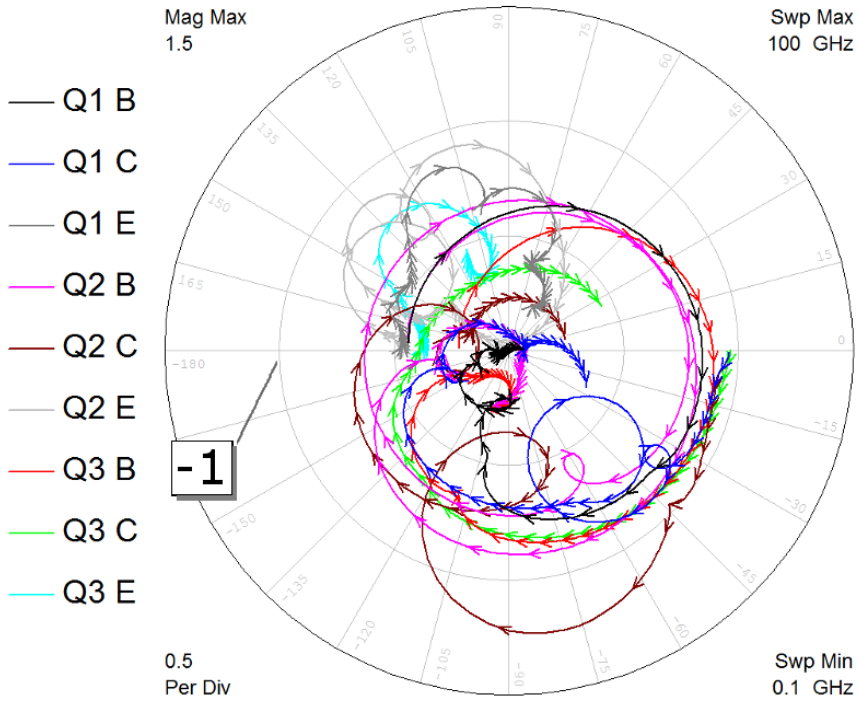


Figure C.3: Post layout simulation of stability of amplifier. Gamma probes are located on all terminals of transistors. All traces are located within a magnitude of 1, indicating stability.

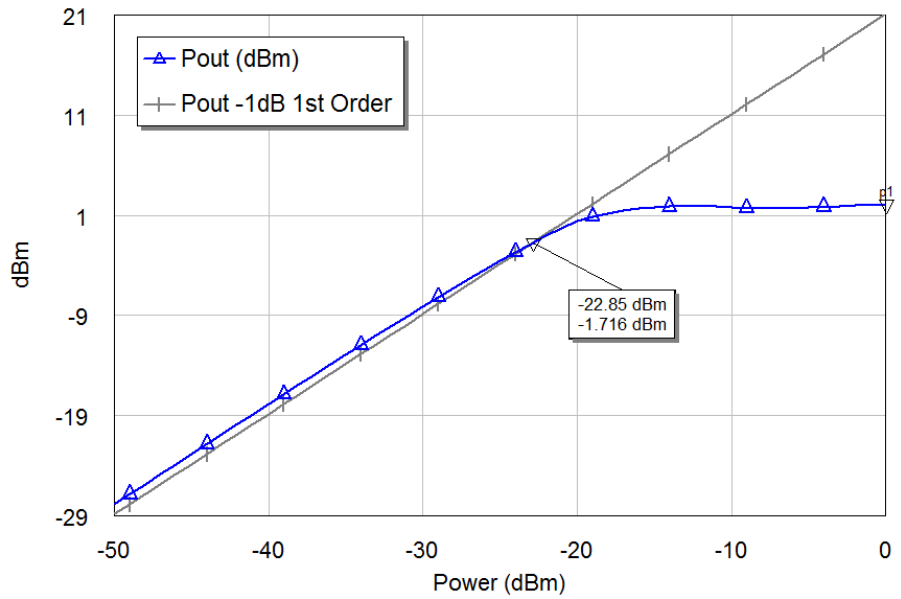


Figure C.4: Post layout simulation of compression point of amplifier. Simulation is performed at the frequency of maximum gain, 57 GHz.

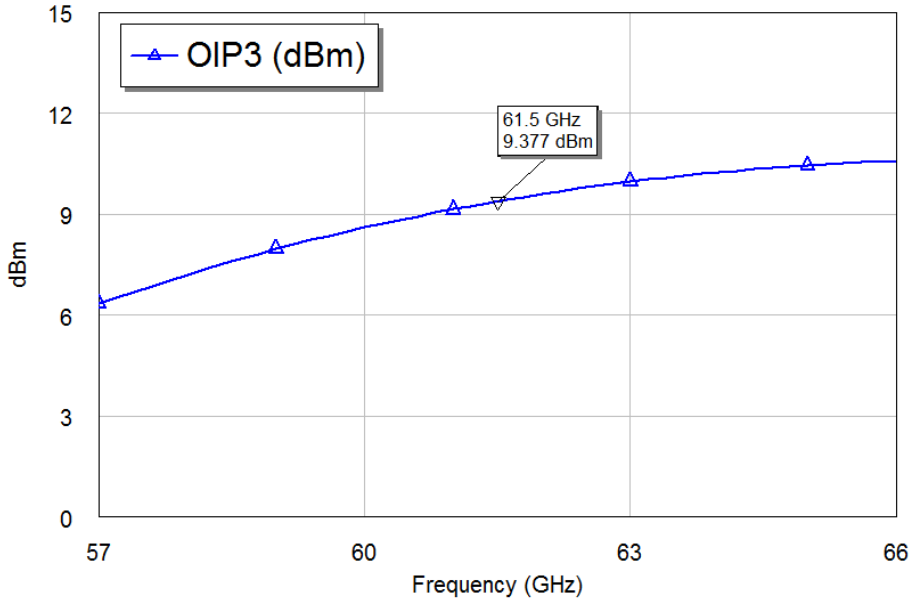


Figure C.5: Post layout simulation of third order interception point. Interception point is approximate 10 dB above the compression point.

APPENDIX D

Cascode Topology Bandwidth Issue

As mentioned in Section 5.1 the cascode topology was proven to provide insufficient bandwidth. This problem can be shown by simulating a cascode stage without matching network. Figure D.1 shows the test bench for this simulation.

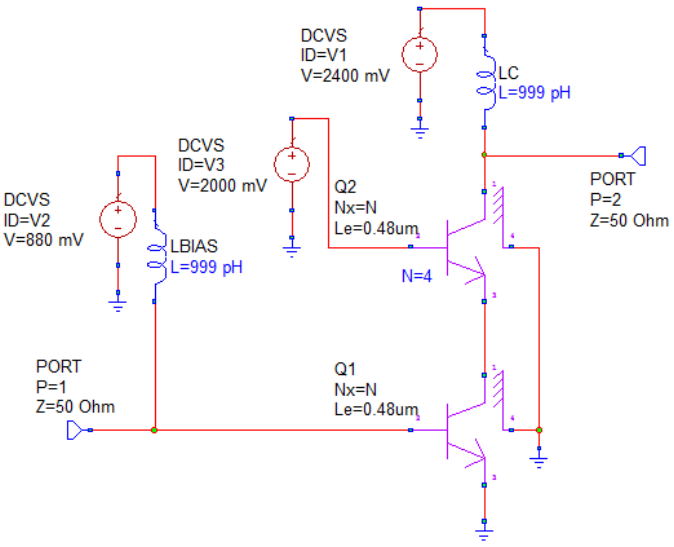


Figure D.1: Test bench for cascode topology

Figure D.2 shows the s-parameters for this circuit.

By inspecting the smith chart and comparing the placement of the s-paramters with the constant contours of Q-value, it is clear that the intrinsic Q-value must be high for this circuit. This is also confirmed by attempts to match this circuit. A bandwidth of approximately 2 GHz is achieved in attempts to use the cascode stage in a multistage amplifier.

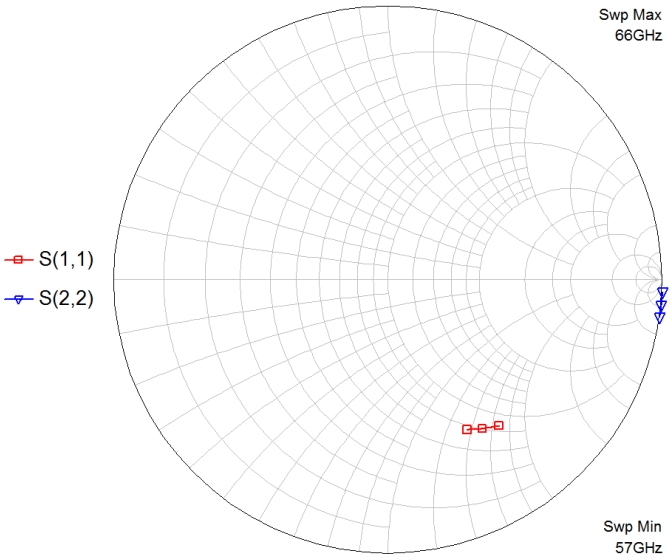


Figure D.2: S-parameters for cascode topology. Note that S_{22} is located far off to the right, causing a very high q-factor.

All attempts in extending the bandwidth have proven to be useless and this topology is therefore rejected due to the bandwidth issues. The root cause of this problem may be related to small transistor sizes and the high output impedance of the cascode topology [4]. Several papers ([20], [29]) have, however, reported cascode amplifiers with good bandwidth, but all these amplifiers use far bigger transistors and hence far more power in the output stage.

APPENDIX E

Test benches

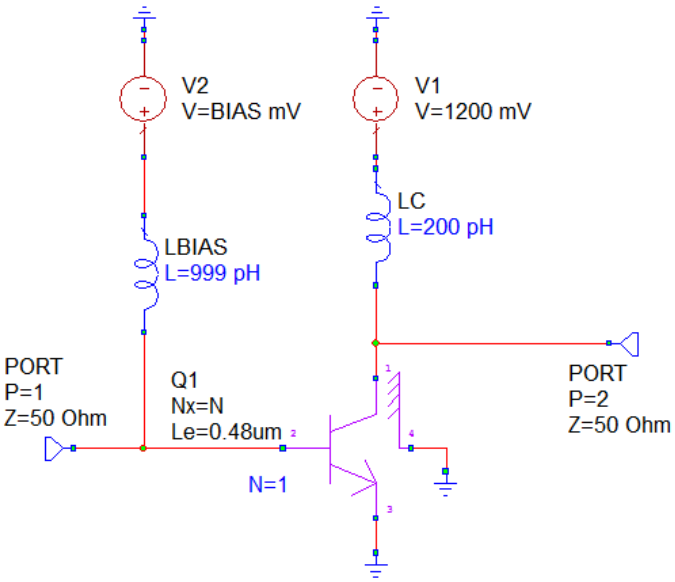


Figure E.1: Test bench for bias determination described in Section 5.4.

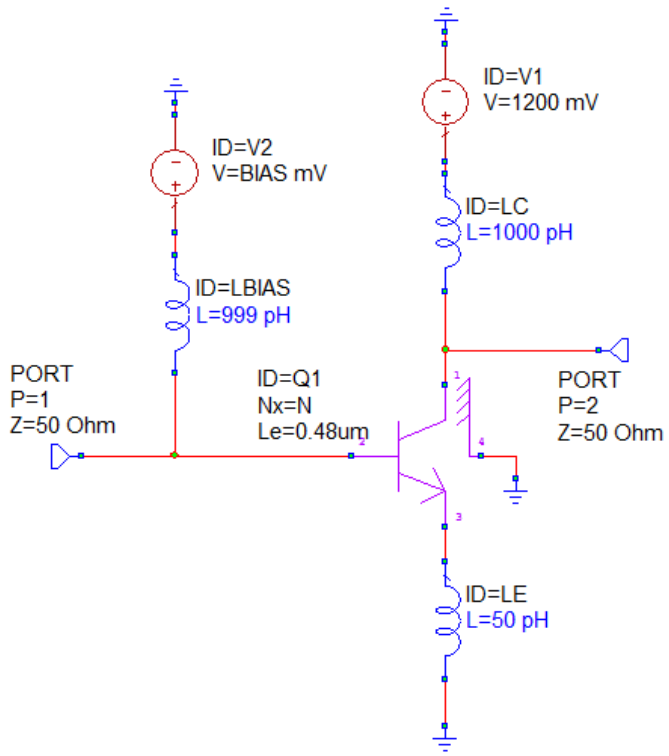


Figure E.2: Test bench for determining the number of stages in Section 5.1. Matching network is not shown.

Abbreviations

ASIC	Application-specific Integrated Circuit
BJT	Bipolar Junction Transistor
CAD	Computer-aided Design
CE	Common Emitter
CERN	European Organization for Nuclear Research
CB	Common Base
CMOS	Complementary metal–oxide–semiconductor
EM	Electromagnetic
FSPL	Free Space Path Loss
GaAs	Gallium Arsenide
GMN	Optimum Reflection Coefficient for Minimum Noise Figure
GND	Ground
HBT	Heterojunction Bipolar Transistor
IF	Intermediate Frequency
IHP	Innovations for High Performance Technology
IIP3	Input Referred Third Order Interception Point

InP	Indium Phosphide
LHC	Large Hadron Collider
LNA	Low Noise Amplifier
MIM	Metal–insulator–metal
MMIC	Monolithic Microwave Integrated Circuit
MWO	Microwave Office
OOK	On-off-keying
NF	Noise Figure
OIP3	Output Referred Third Order Interception Point
PDK	Process Design Kit
PVT	Process, Voltage & Temperature Variations
RF	Radio Frequency
RX	Receive
Si	Silicon
SiGe	Silicon Germanium
TX	Transmit

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