Design of a high power OOK modulator and verification of circuits in 60GHz SiGe BiCMOS

A thesis by

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Abstract

In this thesis, components for the UiB 60 GHz system are verified numerically and an on-off-keying (OOK) modulator is designed.
Presence of mass in particle detector systems decrease the accuracy measuring the particle paths. This is a problem e.g. in the ALICE and ATLAS experiments. The detector systems are also highly complex, and difficult to construct.
For reducing the mass and the construction complexity of particle detector systems, wireless data transfer for the sensors is proposed by WADAPT. The Microelectronics group at the University of Bergen (UiB/UoB) is working on the development of a low-power 60 GHz transceiver chip for this purpose. A previous system design exists, suggested by H.K. Soltveit, using a heterodyne receiver. This thesis suggests that a small improvement of power consumption can be achieved with a homodyne receiver scheme
A previously designed three-stage LNA for 60 GHz with $\geq$ 9 GHz bandwidth and $\leq$ 4.5 dB noise figure is verified and adjusted with electromagnetic simulation and yield analysis, to meet the performance requirements of 20 dB gain and $\leq$ 12 mW power consumption.
A previously designed three-stage PA with $\leq$ 30 mW power consumption, $+5$ dBm power output and $\geq$ 15 % power-added efficiency for the amplification of OOK modulated signals is verified and analyzed with electromagnetic simulations, corner analysis and bias tuning.
A possibly novel OOK modulator is presented with $\leq$ 40 mW power consumption, 11 Gbps maximum data rate and 56 dB simulated CNR. Using a single-ended three-stage switched-common-emitter topology where the speed of the switching is increased by switching the transconductance of the HBTs while in the forward-active mode of operation.

Acknowledgements

Thanks to **Kjetil Ullaland**, my supervising professor, and **Johan Alme** at UiB. **Yngve Thodesen** at Royal Norwegian Naval Academy, **Hans Kristian Soltveit** at Heidelberg University. Thanks to **Adriaan Rijllart** at CERN for strongly suggesting that I should apply for masters studies, and thanks to **Heidi,** for her continuous support and proofreading.

A special salute to **my fellow students**; without whom the two years of master studies, would have been gray and dull.

Contents

1 Introduction

1.1 Purpose

In modern particle physics detector systems there is a huge engineering problem; the cost of the measurement uncertainty introduced by mass, versus the requirements of detector and readout electronics. High-speed powerful detector electronics needs large support structures, cables and maybe heat-sinks. The detection of particles is by interaction with the detector. If the mass in the detector system is not well known, the uncertainty of the detection is increased. More mass in the vicinity of the particles means more uncertainty of measurement. In large particle detectors, there is specified a limit to how much mass the different detectors can have (the mass budget). Both electronics, mechanical support structure and interconnect requires space and mass. In detector systems, electronics are designed without allowing heavy shielding modules and with a goal of minimizing mass. Data interconnects have been changed from copper cable to fiber-optic in the ATLAS detector to save mass (probably many others as well).

The WADAPT[1] R&D project, as of May 2017, is seeking approval from LHCC as a CERN R&D project. The WADAPT group is suggesting to reduce the mass budget, and reduce construction complexity by introducing wireless data and power transmission into the detector environment, effectively replacing the fiber-optics with wireless links and copper power cabling with wireless power transfer. There is so much cabling in modern detectors that there is a significant amount of mass that can be eliminated, and because the wireless signals can possibly be fed out in a straight line, through the air, the delay of the data can become lower. Lower delay of the data will increase the allotted time of detector trigger processing that can be done. This is why there is done research on circuits and components, that can make such a system reality.

Advantages:

- ❑ Lower mass budget
- ❑ Better timing constraints on trigger processing systems
- ❑ Less work assembling the detector (less cabling)
- ❑ Possible application to industry/consumer electronics (5G/WiGig)

Disadvantages:

- ❑ Significant R&D cost
- ❑ Increased high-frequency electromagnetic energy flux in the detector could be a problem for other electronics susceptible to interference (not the case for 60 GHz).
- ❑ Loss of energy through wireless transfer, reducing efficiency of the circuits. As long as the power supply is practically unlimited (the power grid), this is not a problem.

- ❑ Additional heat developed by the new circuits

One challenge is that the specifications of the system are not set, so the design space is large. After a demonstration, or demonstrations of working prototypes, specifications for a system could be set by detector groups. And a large-scale implementation of a wireless data transfer system can be made. For the UiB 60 GHz project this means working towards a functional prototype of a transmitter and receiver. By doing this, and in conjunction, building the foundations of an academic community for high-frequency techniques, UiB is gaining the knowledge and experience for developing a future full scale high-frequency based data-transfer system for detectors.

1.2 Previous work

For the 60 GHz band there has already been demonstrated wireless transfer of video, radar, as well as links for possible 5G applications.

Previous work in the WADAPT project is referenced in [1]; Uppsala-, Heidelberg- and Bergen are some of the involved universities.

An OOK modulation based system design is suggested by Soltveit in [2] (see figure 1.5).

At the University of Bergen, two master theses are already made by Schou and Pallesen [3, 4], with the design of a power amplifier (PA) and low-noise amplifier (LNA) for the 60 GHz band, both in the context of a system like that in figure 1.5.

1.3 System introduction

To transmit digital data wirelessly, we need a receiver and a transmitter. For full-duplex transmission we need receiving and transmitting capabilities, on both sides of a wireless link. So we need a transceiver, for each wireless node in a system. To transfer information through the air, we need an oscillating electric or magnetic field exciting (See eq. A.1) an aperture or slab of metal called an *antenna.* To produce this oscillating signal we put our information (the baseband signal), on a carrier signal of higher frequency. This is called *modulation.* With the proper kind of modulation we can select our bit-rate and bandwidth, almost arbitrarily, limited only by engineering requirements and the Shannon-Hartley theorem (eq.B.9)[1].

For wireless transmission, there are strict government regulations to what frequencies that are legal to use in what cases, and how much bandwidth one can use (frequency bands). Recently, the 60 GHz band between 57 and 66 GHz was licensed to short-range low-power communication devices [5]. This 9 GHz of bandwidth allows for multi-Gigabit data transfer. The band lies within the V-band with wavelengths between 1 mm to 10 mm, also called "extremely high frequency" (EHF) or simply millimeterwave.

[1] e.g. $9 \cdot 10^9 \cdot \log_2(1 + 1000) = 89.7$ Gbps maximum theoretical bitrate with a SNR of 1000 (30 dB) and a bandwidth of 9 GHz. This would require QAM-1024 for a spectral efficiency of maximum 10 $\frac{\text{bps}}{\text{Hz}}$. To get higher bitrate additional communication channels are needed, making the system multiple input multiple output (MIMO)

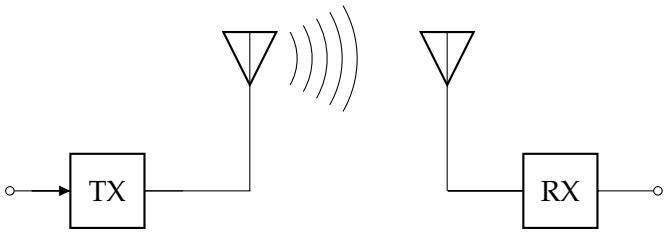


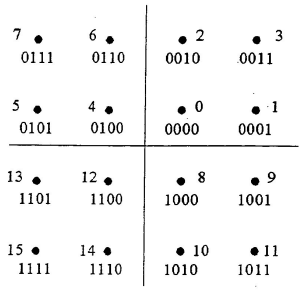
Figure 1.1: *Generic TX RX wireless system*

There are many different modulation schemes. Quadratrure Amplitude Modulation (QAM) is the currently most used scheme. It uses a in-phase and a signal 90 degrees offset (quadrature), amplitude modulated and summed. Effectively this modulates amplitude and phase simultaneously. QAM is used in conjunction with frequency division multiplexing (OFDM) by cell phones and WiFi signals, and allows the transmitted spectrum to be narrow. It is also notated as QAM-16,-256,-2048, by how many complex amplitude levels there are in the modulation scheme. High density constellations are usually found in optical transfer, because the noise, interference and loss in a wireless environment are difficult to mitigate. QAM modulation needs the receiver to know the phase and frequency of the transmitted spectrum. This is called synchronous detection. To know the carrier frequency and phase, a technique is used called *carrier recovery.*

QAM-256 (2^8) gives double the capacity (bitrate) of the QAM-16 (2^4) with the *same* bandwidth. This comes at the cost of a requirement for much better noise-performance. We can say that the QAM-256 has twice the $\frac{\text{bps}}{\text{Hz}}$ as QAM-16. The quantity $\frac{\text{bps}}{\text{Hz}}$ is called the *spectral efficiency.*

Figure 1.2: *QAM Constellations, each point a vector consisting of* $m \cdot \hat{I} + n \cdot \hat{Q}$,

(a) QAM-16



(b) QAM-256

I - Q (in phase - quadrature) constellation displaying the complex vectors in the QAM signal
Image sourced from : Google Patents (public domain) https://goo.gl/eDvz0Q.
To generate these signals requires two high-performance, very linear mixers, good phase matching and flat amplification over the band and digital signal processing.

Because of the complexity of a QAM system (see figure 1.2), it requires significant amounts of power, and may not be the ideal for very low power applications. Cell phones (using QAM) are relatively low-power, but they are power-cycled, and can use more than 1 Watt when communicating. Excluding the QAM modulation type, and others like it[2], limits the spectral efficiency of the system to 1 or 0.5 $\frac{\text{bps}}{\text{Hz}}$. To compensate for this, we have the 9 GHz of bandwidth available in the 60 GHz band.

With this wide bandwidth we can use spectrally - inefficient modulation types, and still be able to transmit data on the order of gigabits per second. The simplest, and earliest of modulation types is amplitude modulation (AM). The digital version of amplitude modulation, when the carrier is turned completely off is called On Off Keying (OOK).

Early simple radios and TV was using the amplitude modulation schemes. In modern technology it is used when the system requires a transceiver of low complexity. Mentions of on off keying itself, can be found with a patent search back to 1934. But of course, we all know of the telegraph. Therefore the concept can easily be traced back to Morse in 1837.

OOK modulation is the binary amplitude modulation of a carrier signal. It is a simple scheme where one simply turns off the carrier when sending a digital zero, while having it on when sending a digital one. It does not require very low noise, nor carrier recovery (it is asynchronous), and is perhaps the simplest type of modulation to make a modulator for. Additionally, the simplicity makes the modulator circuit able to use very little power.

An important consideration with OOK modulation is that even though, in time domain on an oscilloscope, the modulated signal *looks* like a sine wave turned on and off, the spectrum of the signal is much wider than the carrier wave. OOK modulation has the spectral efficiency of 0.5 $\frac{\text{bps}}{\text{Hz}}$. So a 1 Gbps signal needs 2 GHz of bandwidth. For the specified limit of 9 GHz between 57 and 66 GHz it is then possible to transfer 4.5 Gbps of data with OOK modulation. Low complexity allows for reductions in chip area cost, as smaller circuits can be made. This also helps to increase the circuit yield. Low power allows very many of the chips to be deployed in a large system, without introducing extreme power requirements. We can then see, that because of the properties of low power and low complexity, the OOK scheme is an excellent candidate for the system.

The system environment is assumed to be a low-interferer environment. As 60 GHz has high loss and equivalent short range in the air(see figure 1.3). This reduces the demands of the filtering needed on the input because of low or no interference, thus it reduces complexity. An elaboration about interference, scattering and 60 GHz absorbing materials is found in [2].

1.4 The 60 GHz Transceiver chip

As mentioned in the previous work section, Soltveit, Shcou and Pallesen have used the system concept published by Soltveit [2] (figure 1.5) as a guide for the OOK system. The goal is to have a 2 mm^2 chip doing the conversion from digital signal to 60 GHz modulated, and

[2]QPSK, N-PSK and, OFDM

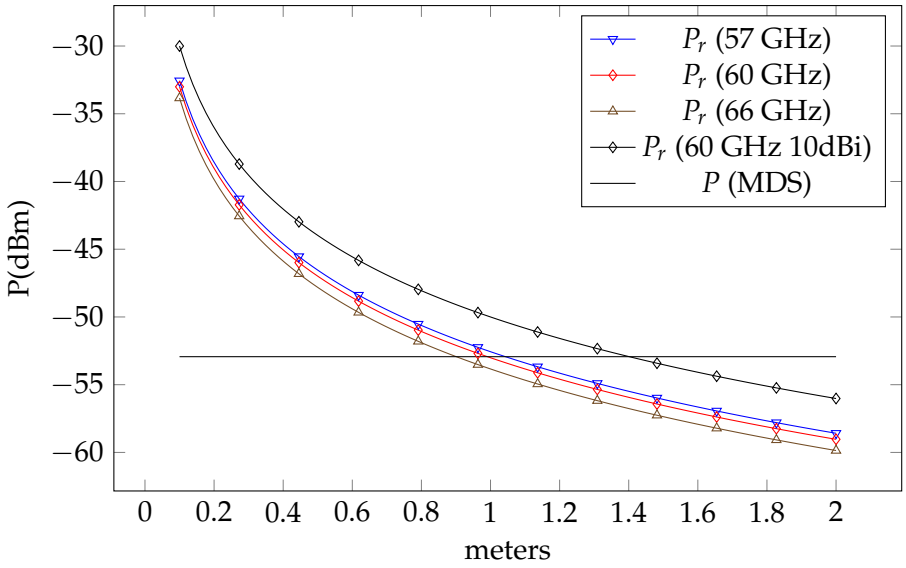


Figure 1.3: *Received power calculated using Friis free-space path loss (eq.1.3) and minimum detectable signal (MDS, eq.B.7)*
Assumed values : Pt=5 dBm , $G_{T,R}$= 5 dBi *(except for marked) , minimum* SNR=17 dB, *LNA noise figure* = 4.5 dB *All temperatures* = 290 K. *Equations B.6 and B.8.*

received, demodulated and converted back again to digital (figure 1.4). The small chip size reduces fabrication costs.

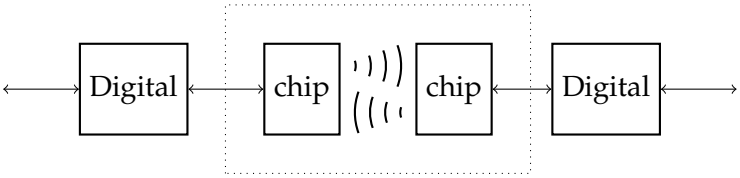


Figure 1.4: *System in context*

The chips integrated into a communication system, will appear no different than a transmission line to the rest of the system. It would be transparent, only providing a physical communication channel. In other words, it would provide the physical layer (PHY) in the OSI representation of the system.

Ideally, the complete transceiver system would be integrated on a single chip.This would save circuit board space and reduce the mass budget further. Antenna on chip is currently not possible, because of too high antenna losses in antenna on chip technology. The rest of the system can be integrated. Currently, antennas on chip for 60 GHz have too little gain to be used. The radiated field enters the (relatively) high-dielectric constant substrate, instead of the air. There exists small antennas that are usable, like [6] where a 15 dBi antenna with largest dimension of 55 mm, is presented. This is still 40 times the largest dimension of the chip.

The transmitter consists of a modulator, oscillator and power amplifier. The receiver in figure 1.5 is a heterodyne receiver. While the receiver in figure 1.6 is an even simpler solution

that can work (see [7] and [8]). The difference from this work and [7] is that [7] is a multi-IC solution, where one IC is made per function. In this work, it is assumed that a single chip solution can work. The target BER for the 60Ghz system is approx 10^{-12}, requiring a SNR better than 17dB[9] in a nonfading environment.

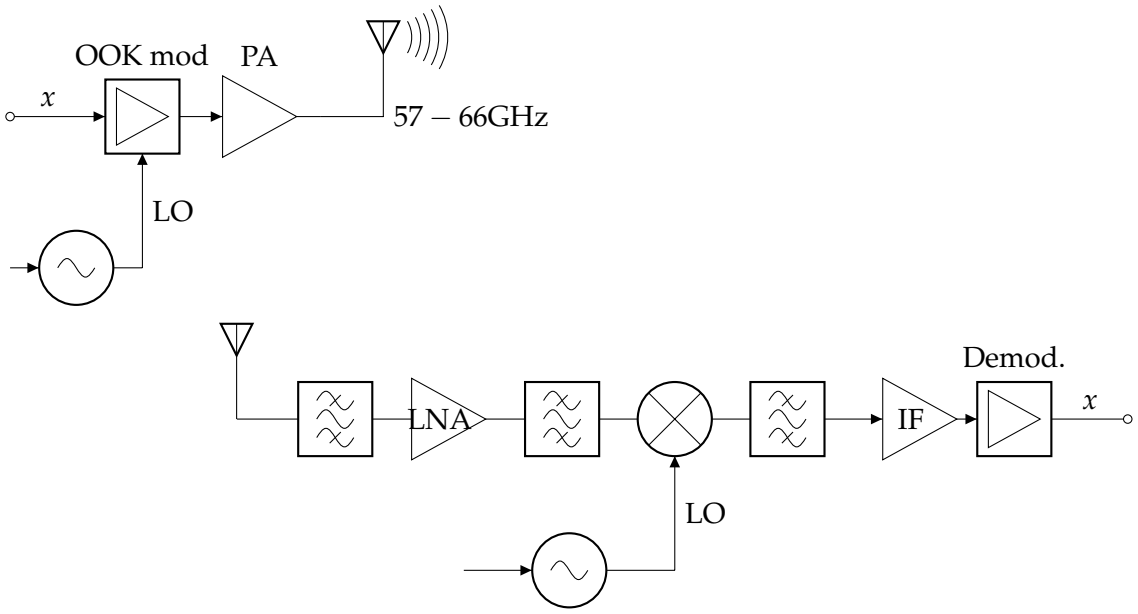


Figure 1.5: *Previously suggested OOK modulated system in [2, 4, 3]*

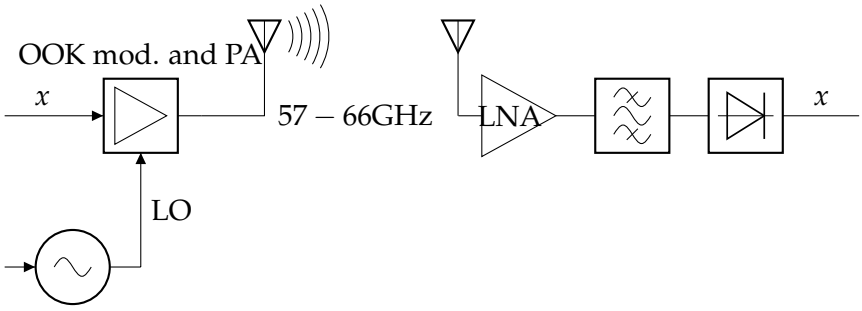


Figure 1.6: *A simpler OOK system*
Transmitter with integrated modulator and power amplifier for greater simplicity
Receiver with LNA followed by an OOK demodulator and conversion to digital. Conceptually similar to the system in [7].

1.5 About This work

For this thesis, the work was done autumn 2016 and spring 2017.

To validate and modify the previously made LNA circuit, during autumn 2016, I ran several tests, with different design of project layout and EM verification workflow. This resulted in higher proficiency with Microwave office (MWO). This also made the rest of the work easier to accomplish. The modifications of the LNA made the circuit more ready for production.

After this, to see if the entire UiB 60 GHz project was feasible, I did the feasibility study (sec.1.6). This was done by finding published articles where systems with similar parameters had been manufactured, and by selecting the same type of transistors (HBT) and operating frequency (60 GHz). This study confirms, or re-affirms the feasibility of the entire project.

The PA was verified and modified for the same reasons as the LNA circuit. To verify the PA firstly there was done EM simulations, then corner analyses. By small modifications and a wide range of corner simulations, the PA is more ready for production.

To know if oscillator phase noise negatively impacts the OOK modulation scheme, phase noise effects were investigated, by time-domain and frequency domain analysis, from the reference point of a transmitter. The effects were found to be negligible within certain limits.

To be able to modulate and amplify the OOK signal with low power consumption, a combined power amplifier and modulator was designed. A high-power OOK modulator. The specific circuit has not been found other places by the author, and is possibly novel. It was designed by combining nonlinear device behavior with amplifier design. This made a design that needs a few milliwatts more power than only a power amplifier, so that the transmitter design can be much more efficient using this circuit, instead of separate power amplifier and modulator.

1.6 Feasibility of the 60 GHz system.

To try to determine the feasibility of the system, this section will attempt to give perspective on what degree of challenge the design is, from the viewpoint of published research. Acknowledging the work in [2] and [10], that demonstrate the efficacy of 60 GHz data transmission, and its applicability to particle detector data channels. This work attempts to explore the design space for the 60 GHz SiGe systems that have been made. Possibly it may reveal a Pareto frontier, or Pareto-optimal point(s), where no further optimization can be done.

The system design is within a known technology, with several working examples. The SiGe 60 GHz implementations found in litterature is listed in figure 1.7.

To make a valid comparison, data was collected specifically on 60 GHz transceiver systems using a SiGe process. This eliminates the variables of operating frequency and semiconductor type. The plot of these systems (figure 1.7) incorporates bit-rate and power consumption. The remaining, uncharted variables between the systems are :

- ❑ Transistor feature size (0.25 µm / 0.18 µm / 0.13 µm)
- ❑ Modulation type
  (OOK / ASK / FSK / ODFM / BPSK / External / internal IQ generation)
- ❑ External reference oscillator or internally generated carrier frequency.
- ❑ Single chip transceiver, or one transmitter and receiver chip (chipset), multi-board system, or a wirebonded multi-chip solution
- ❑ Antenna gain
- ❑ Transmission range
- ❑ and others.

To make a quantitatively sane comparison, an assumption has to be made, that there is no unique component required for the successful operation of the system[3]. This is first *assumed*, and then also confirmed by studying the designs referenced in figure 1.7. There is no single design choice that is common to every author.

There are some recurring themes; differential amplifiers and mixers are common, and simplicity is emphasized, when designing for low-power.

Figure 1.7, made by combining data from the cited articles, illuminates the design space. We can see that this (the UiB 60 GHz) system lies in a challenging design corner, combining both very low power consumption and high data rates in the top left corner of the graph.

What makes this goal possible; the combination of the low supply voltage of 1.2 Volts, few system components, a focus on the efficiency of the individual system components and simplicity of the system.

Here is suggested a Pareto-optimal point in the vicinity of the coordinate, (100 mW, 5 Gbps) for a transceiver system. The real value might be slightly better (less power, more bit-rate), as

[3] No magic ingredient, so to speak.

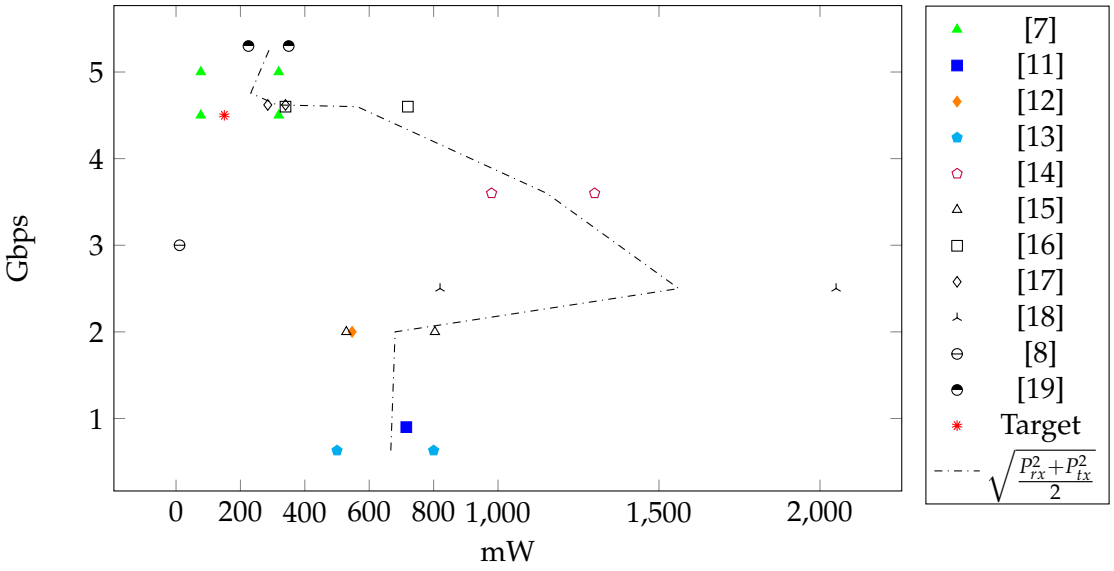


Figure 1.7: *60 Ghz SiGe transceiver systems comparisonin the litterature* [7, 11, 12, 13, 14, 15, 16, 17, 18, 8, 19]. *Separate points for Tx and Rx. Single point for the cases where this was the only data point, or the design was only a receiver. More power generally tends to offer more features. Lower bit-rate tends to increase transmission range.*

the precise value of the point is not feasible to find by a comparison of existing systems. Since the Pareto point is more optimal than the goals for the system, we can say that the system is realizable. A more concrete example; if we take the design in [7] and replace the power amplifier with one that uses less power, like the one presented in [3], the total dissipated power of that system is reduced to below 150 mW, and the power design goal is achieved.

1.7 OOK modulation and Phase noise

Phase noise is the random variation of phase in a carrier signal. It can appear as random FM, or AM modulation on the ideal signal. It is measured as a single-sideband power spectral density (SSB-PSD), with the carrier nulled out in the measurement. When the phase varies, a detector can detect a different signal. For example, say the modulator sends one bit with a reference phase φ_1, and after some time sends another bit with the same phase, the signals are the same, so the energy is equal. In the case where the second bit has a different phase φ_2, the signal is different and therefore the energy can be different.

Following, there is a discussion of time domain and frequency domain effects, for a OOK modulated signal influenced by phase noise.

A simple approach to phase noise, is to model it as a difference, in phase between two time intervals, t_1 and t_2. Say that t_1 is the five periods of stable carrier wave in figure 1.8, and say that t_2 is a period of five cycles after 22 radians on the lower signal. These signals will start and end with the same frequency, but the phase of them is different.

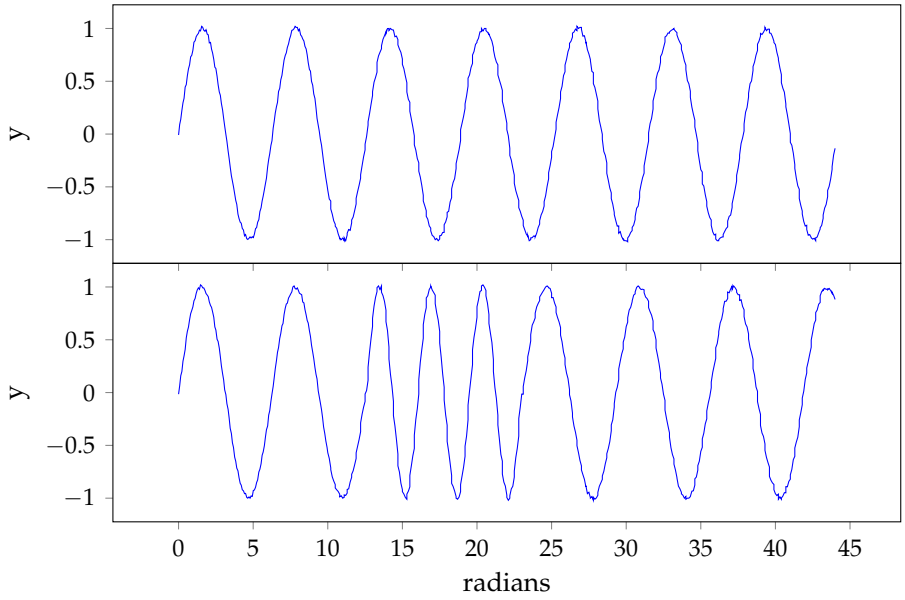


Figure 1.8: *Carrier phase noise of the FM type, exaggerated example*
From 11 to 18 radians, the frequency is different in the form of phase noise and then returns to the carrier frequency. Referenced to a stable source, the phase is different.

1.7.1 Time domain carrier phase and bit-energy considerations

> *Please note that in the following section, the term "energy" is used to describe the finite integral of the squared signal, and is not physically meaningful as real energy, because real energy is always conserved, unlike the signal.*

As the OOK is a binary modulation, the carrier is switched on and off, the phase of the carrier has very little importance for the data transfer. As the receiver is an envelope detector (for asynchronous detection), it detects the presence of energy from the carrier wave (CW). The phase of the CW does not affect the energy content. We can then assume that phase noise is

of minuscule importance to the system as a whole. This assumption is correct for a CW that is on all the time, as the energy is simply represented as the integral from $-\infty$ to ∞ (This is easily shown by Parseval's theorem).

For binary modulation, the assumption that the carrier always is there, falls away, and other ways of checking has to be applied. For simplicity there is used $\sin^2(x)$ instead of $|\sin(x)|$ because $\sin^2(x)$ is differentiable. Ratios will be equivalent, as we see in equation 1.1 and 1.2, with some margin of tolerance;

$$\lim_{x\to\infty} \frac{\sum(|\sin(x)|)}{\sum(\sin^2(x))} \approx 1.273 \pm 0.001 \approx \text{constant} \tag{1.1}$$

The ratios of the sums (digital equivalent to integrals) of the two functions will be constant, and the value of 1.237 converges very fast, therefore:

$$\frac{\sum \sin^2(x_1)}{\sum \sin^2(x_2)} \approx \frac{\sum |\sin(x_1)|}{\sum |\sin(x_2)|} \tag{1.2}$$

The ratios of the functions will be equal, with $\sigma = 0.01$.

Equations 1.3-1.11 is a simple algebraic example on the relative energy level of two time-limited sine waves.

$$A \cdot \cos(2\pi f t + \varphi) = f_\varphi(t) \text{ phase offset carrier} \tag{1.3}$$

$$A \cdot \cos(2\pi f t + 0) = f_0(t) \text{ zero phase reference carrier} \tag{1.4}$$

$$\Delta V = f_0 - f_\varphi \tag{1.5}$$

$$\Delta E = \int |\Delta V|^2 \tag{1.6}$$

$$\int_0^z (f_0)^2 dt = \frac{1}{8}A^2\left(4z + \frac{\sin(4\pi f z)}{\pi f}\right) \tag{1.7}$$

$$\int_0^z (f_\varphi)^2 dt = \frac{A^2(\sin(2(2\pi f z + \varphi)) + 4\pi f z - \sin(2\varphi))}{8\pi f} \tag{1.8}$$

$$f_{\Delta E}(z,\varphi) = \int_0^z (f_\varphi - f_0)^2 dt = \frac{A^2 \sin(\varphi)\sin(2\pi f z)\sin(2\pi f z + \varphi)}{2\pi f} \tag{1.9}$$

$$f_{\Delta E} = \int_0^z |f_0 - f_\varphi|^2 dt \tag{1.10}$$

From this, we can see that if there is inserted a 10 degree phase difference at 4.5 Gbps/61.5 Ghz, there is a $0.3\,\% = 0,03\,\text{dB}$ ratio from eq.1.11, describing energy ratio as a function of peak phase error on the carrier, with two bit pulses of duration z.

$$f_{E_R} = \frac{f_{\Delta E}}{\int_0^z (f_0)^2 dt} = \frac{4\sin(\varphi)\sin(2\pi f z)\sin(2\pi f z + \varphi)}{4\pi f z + \sin(4\pi f z)} \tag{1.11}$$

These equations (1.9-1.11) are valid, assuming that the phase does not change during the transmission of a bit, only between consecutive bits.

The value of this equation grows smaller with increasing number of periods, either in the form of increased frequency, or longer bit duration (z) .

$$\lim_{z\to\infty} f_{E_R} = 0$$
$$\lim_{f\to\infty} f_{E_R} = 0$$
$$f_{E_R} \propto \frac{1}{fz}$$

While 10 degrees is an improbable phase difference for any oscillator, it is useful to demonstrate the effects.

Concluding; for a OOK modulated system, with an envelope detector receiver, the phase noise of the oscillator will not affect the bit-error rate significantly. Thus, the power received by an envelope detector in the time domain, will not be significantly altered due to phase variations of the carrier between the bit periods.

1.7.2 Frequency band-spreading.

For the extreme case, where phase noise is high, say -20 dBc at 1Mhz above carrier, the frequency is random. For the more normal cases where the phase noise is from -45 to -90 dBc/Hz, the carrier is stable. The effect of a probability distribution for the signal is that some of the carrier power is spread out in the spectrum. For the legal limits, the 9 GHz span inside 57-66 GHz for Europe, the phase noise has very little effect on the signals bandwidth. We see in figure 1.10 that it is only in the very extreme case, where the carrier frequency is very random, that the spectrum is out of bounds. A system should also suppress the sidelobes (spectral leakage) . To conclude, the phase noise has low or insignificant effect on the OOK scheme as seen from the transmitter side. The exception to this is in the case of extremely high phase noise (see table 1.1). For phase noise that is increasing from some place between -60 dBc to -45 dBc at 1 MHz from the carrier, the modulation scheme will be impacted. In agreement with the litterature, the OOK modulation is not impacted severely, with the additional requirement presented here that the phase noise has to be within a normal range.

Table 1.1: *Peak CW value change with phase noise increase*

dBc	carrier level
$-\infty$	5
-90	4.81
-80	4.81
-70	4.8
-60	4.76
-45	0.9
-20	-16.08

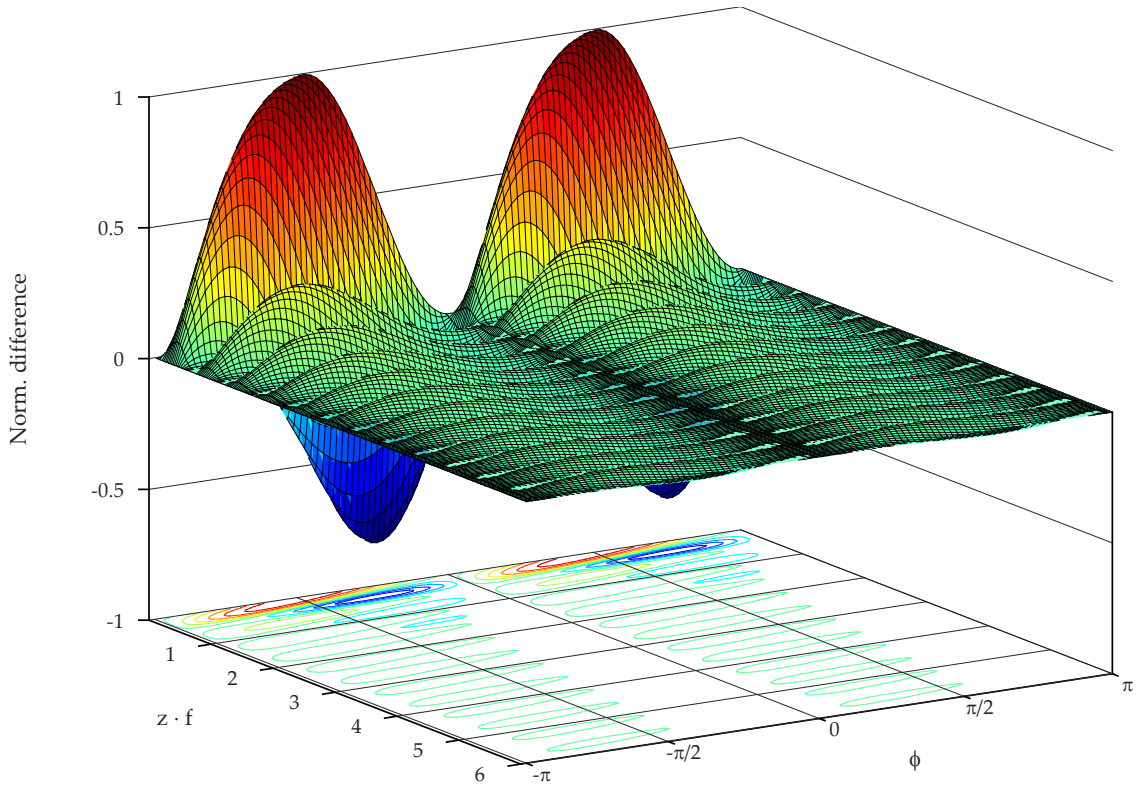


Figure 1.9: *3D plot of eq. 1.11*
The $z \cdot f$ axis can also be interpreted as the ratio $f_{Carrier}$ / Bandwidth. For ook dsb modulation. When the ratio is 1, the implementation becomes extremely difficult because it requires the full bandwidth from DC to twice the signal frequency. The normalized difference scale is unit-less and shows the normalized difference of the integrated waveforms.

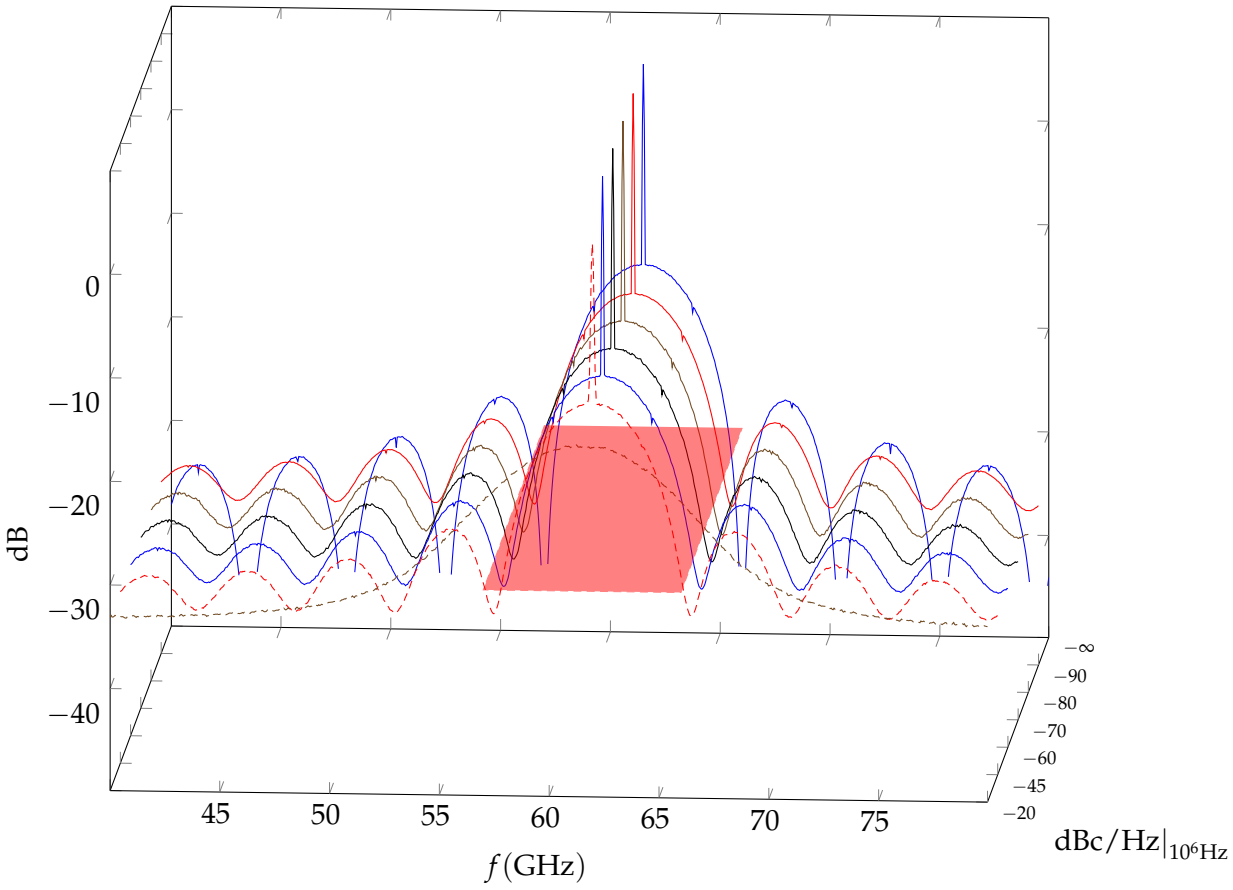


Figure 1.10: *Phase noise and OOK spectrum spread*
The small ripples in the graph is a result of the sampling span of the sim. Setup and not a physical effect.

2 Overall system design considerations

2.1 Process

The IHP sg13s 0.13 µm SiGe BiCMOS process is the process used in the previous work of Pallesen and Schou ([3, 4]). It is a CMOS process with SiGe (HBT) npn-transistors. The process offer availability for a multi-project wafer and is relatively inexpensive. In a BiCMOS process one can combine digital and high-performance analog circuits. This allows highly integrated systems on a small chip.

It is made available via the Europractice IC service, provided by IMEC and Fraunhofer.

2.1.1 Important high-frequency characteristics of the material

The metal is aluminium, with conductivity of $35.5 \cdot 10^6\,\mathrm{S\,m^{-1}}$ and notably higher sheet resistance than gold or copper. The aluminium requires less processing steps in the IC fabrication, and thus is cheaper to use. The insulator is Silicon Dioxide SiO_2 with $\epsilon_r = 4.1$. SiO_2 has low dielectric loss. Because of the different embedding depth, the effective dielectric constant and propagation factor, γ, is different in each layer.

Table 2.1: *Selected substrate properties, skin depth using* $\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}}$

Property	value	metal
ϵ_r	4.1(SiO_2)	–
Skin depth	334 nm	–
$\frac{\lambda}{4}$ at 60 GHz	590.66 µm $\pm$ 1°	TopMetal 1
$\frac{\lambda}{4}$ at 60 GHz	635.66 µm $\pm$ 1°	TopMetal 2

2.1.2 MIM Capacitors

Metal-Insulator-Metal (MIM) capacitors are high-capacitance per area capacitors on an IC, a vertical stack of two metal plates between a thin insulator. Thus giving much more capacitance per area than interdigital capacitors often used in MMIC designs. The supplied model only models series capacitance, not substrate capacitance, so there will be more loss from these components than simulated. CMP dishing effects are ignored and assumed to have low impact on final performance of the circuits.

Capacitance between objects in electrostatics is simple, $C = \frac{q}{\phi}$[1] or $C = \frac{\epsilon_r A}{d}$. For low frequencies, the electric field between the plates is $\mathbf{E} = \frac{\rho}{\epsilon}$, $\rho = \frac{q}{A}$. Assuming circular plates, we see from [20, ch. 23] that the field is modified with higher frequencies, because of the wavelength of the signal becoming comparable to the structure, resulting in current loops. We then get $\mathbf{E} = \mathbf{E}_0 e^{i\omega t} I_0\left(\frac{\omega r}{c}\right)$ (r is the radius of circular plates, I_0 the zeroth-order Bessel function)

[1] see eqs.A.8 + A.9

with perfect conductors and dielectric. This simple example, shows that any capacitor gets reduced capacitance at increasing frequencies.

As the capacitors in the process are measured at low frequencies, the value will be lower, resulting in higher loss through the signal paths. The larger the capacitor is, the more frequency dependent it is. A useful equation for measuring the capacitance in a network is

$$C = 10^{12} \cdot \frac{-1}{(2\pi f \cdot \Im\left(Z_{11} \cdot Z_{22} - Z_{12} \cdot Z_{21}\right) / Z_{21})} (\text{in pF}) \tag{2.1}$$

In the PDK, the model is an ideal capacitor with the same capacitance for all frequencies. To get an estimate of the order of magnitude of the stray capacitance values, some were calculated from fundamental principles (table 2.2b) and then measured from simulation (table 2.2a). Some uncertainty is expected, because of a simple and not well de-embedded set of tests. Also both the calculation and measurement of the peripheral capacitance can be assumed to be very inaccurate, as the last entry in table table 2.2b goes down (un-intuitive), and the corresponding value in table 2.2a, increases with an unnatural rate.

From EM simulations done during verification of components, a model was developed to fit the data from the EM results; shown in figure 2.1. It can be matched to EM simulated capacitors quickly, by optimization algorithms in the design environment. The capacitance (measured by eq. 2.1 or the included measurement in MWO), is frequency dependent, and the component itself has some loss. The assumed reason why the frequency dependent behavior is not included in the PDK, is that the measurements of the capacitors in the documentation, are done on low frequencies.

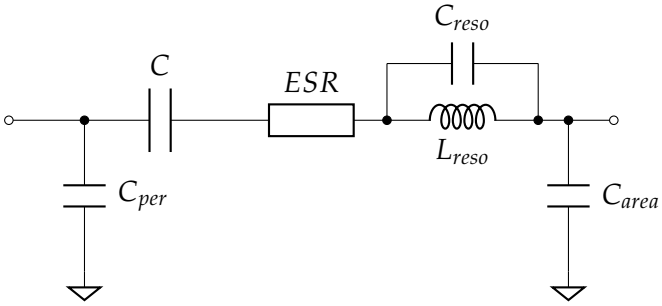


Figure 2.1: *Suggested capacitor model*
This model is a good representation of the capacitor, and has high enough accuracy to match the EM data closely. If very high accuracy is needed in the resonating area, additional parameters should be implemented.

2.1.3 HBTs

Heterojunction Bipolar transistors (HBTs), are made with different (hetero) materials of the base, and the emitter-collector. Usually SiGe or type III-V semiconductors[2] . Other materials used for HBTs are Gallium arsenide (GaAs), Indium phosphide (InP) and Gallium nitride (GaN).

[2]the roman numerals III and V stands for the 3 and 5 orbitals found in the outer shell of the Boron and Nitrogen group of the periodic table.

Table 2.2: *Capacitor simulated and calculated stray capacitances*

(a) Simulation

Dim.(µm)	Periph.	Area
8,1× 8,1	0,2 fF	0,6 fF
18,2× 18,2	2,5 fF	6,7 fF
25,8× 25,8	2,0 fF	14,6 fF

(b) Calculation

Dim.(µm)	Periph.	Area
8,1× 8,1	0,7 fF	1,1 fF
18,2× 18,2	2,8 fF	5,5 fF
25,8× 25,8	24,8 fF	12,6 fF

For simple series DC-blocking capacitors, the strays will cause slightly more loss. For phase or Q sensitive arrangements, the effects cannot be disregarded.

HBTs limit the injection of holes into the emitter region (reduced degeneration/higher β). The base is highly doped, reducing the resistance of the base material. This makes it possible to reduce the gate size, reducing the gate capacitance thereby increasing the f_t.

Historically, the ebers-moll model (figure 2.2a), was used in simulators. The model is based on the ebers-moll equation, modelling the forward characteristic behavior of a transistor. A new model was later made called the Spice Gummel-Poon (SGP) model (1970/1978)[21]. A later improvement (1996), was the VBIC (Vertical Bipolar Inter-Company) model (figure 2.2b) [22]. The HBT transistors in the sg13s design kit are specified with the VBIC model, as the VBIC has effectively superseded the SGP.

For the model supplied with the PDK, a range of operating points are in the measured data set. Outside these limits[3], the model takes over. To asses the performance of a circuit when simulating, having the HBTs within the measured data is advantageous, because it adds certainty to the realism and accuracy of the simulation. Outside the range of measured data, is model-extrapolated data. This can be accurate, but the accuracy and resemblance to the final product is unknown. Some care should be applied to keep the transistor model within realistic parameters.

The npn transistors has a transition frequency , f_t, larger than 200 GHz.

The definition used for transition frequency of bipolar transistors, is when the h_{21} parameter reaches unity, or when the short-circuited forward gain of the transistor reaches unity [23][4].

The bipolar transistor has four modes of operation[5]. To keep the transistor as an amplifier, we keep it in the active (active-forward) mode. When the transistor transitions between the modes of operation, like between active and cutoff, there are charge/discharge effects that slows the transition down. The transistor is then unable to instantly switch between one state and the other.

Breakdown power

In [24], the safety limits for RF power on SiGe HBTs are explained to be 10% to 20% above the static C-B breakdown voltage of the devices, before destruction by hot carriers. From this,

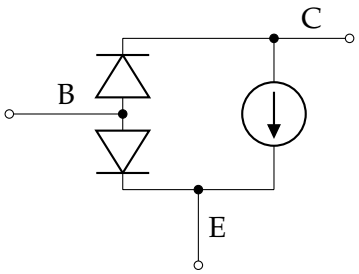
[3] The actual values and operating area are trade secrets/confidential

[4] $h_{21} = -\frac{2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$ [23]

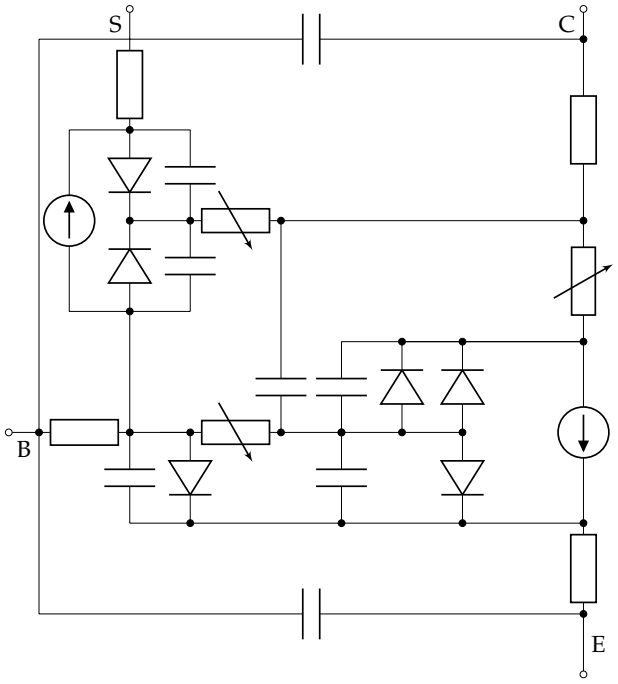
[5] Active-forward, Saturation, Cut-off and Reverse-Active

Figure 2.2: *NPN large signal model development*

(a) Ebers Moll 1 (EM1) (1954)



(b) VBIC (1996)



Reproduced from [21]

we can infer that a normal-case RF breakdown in the IHP process with a cascode stage, is $3.3 - 3.6\,V_{pp}$, using the process specification, and the method in [24]. The required collector voltage for max f_t, would be 1.2 Volts per transistor, so 2.4 Von Vcc. This gives a safety margin of 0.9 V, before hot-carrier injection, and subsequent device destruction or degradation. This is 18mA into 50Ω (16 mW = 12 dBm) . For the common-emitter (CE) stage, the safety margin is 0.45 V, reducing the safe power maximum (for 50 Ω) down to 6 dBm. For the design it is then recommended to keep the impedance seen by the output stage transistor, below 50 ohms .

2.2 Verification goals

1. Confirm that previous designs work, by simulating with an EM simulator, modify if necessary.

2. Provide confidence in the designs, by qualitatively comparing the designs against examples, theory and known design guidelines

3. Evaluate possible performance issues, by quantitatively measuring statistical variations of the performance metrics of the circuits

4. Estimate yield, by numerical techniques.

2.3 Choice of simulator

The University had access to the NI AWRDE CAD suite, for educational purposes. Because the simulators bundled with AWRDE was already available, they were chosen to use in this work. There was included a third party (process design kit) PDK, that also was used in the previous work at UiB.

AXIEM is a 3D planar full-wave method of moments simulator (MoM). The method of moments, is faster than the finite-element method for many problems. The mesh is made smaller, by only using the surface of the conductors (boundary conditions) as a solver basis. Finite element meshes the entire volume to use as as the basis. The method of moments, works by solving a matrix from the actual solution

$$L(f) = g \tag{2.2}$$

made into an approximation of the form

$$\sum_n \alpha_n \langle L f_n, w_m \rangle = \langle f_n, w_m \rangle \tag{2.3}$$

Made from basis functions f_n and weighting functions w_m, This is solved iteratively to the approximation of g. The solution has increased accuracy, with increased number of iterations (see appendix A.3 for more details).

This matrix can grow quickly or slowly in different simulators and settings.

Another simulator used is the FEM-based Analyst simulator. It also comes with the AWRDE software. It solves the entire volume of a problem. The advantage finite element solvers have is that the convergence of the result is better guaranteed, and it is general to any kind of structure. It is significantly slower than AXIEM for planar-type problems.

2.4 Simulation setup

In some simulations with large signal swings, the S-parameters are still used to represent the behavior of the component. This is a false interpretation, because S-parameters cannot be used to accurately represent non-linear responses [25], like intermodulation and dynamic operating point behavior of semiconductors. The response then needs to be interpreted for what it is, an estimation with some uncertainty. The limit of this, is when the signal levels in the circuit is small enough, that the linear representation is valid.

For the EM simulations, the simulator was set to extract the schematics for the AXIEM simulator, with Thick-metal models. A large, finite ground plane on M1 was used. The stackup and process definition was a pre-defined third party definition, using the IHP_SG13S.lpf file[6].

The stackup for AXIEM, should be changed when simulating capacitors. Vmim_drawing, and MIM_drawing, needs to be added to the EM layers. The thickness of the ThinAluminum2_5, should be rectified to match the process specification document. The thickness change is a small change that doesn't affect the rest of the simulations, with any significance.

2.4.1 Workflow design

The LNA and the PA projects for MWO, was provided by Pallesen[4] and Schou[3]. To try to compartmentalize the design during simulation and adjustments, the schematics was split up into three subsections (fig. 2.4); one for each transistor, and surrounding matching networks. . First, the validity of the existing model was evaluated qualitatively, then quantitatively. Most of the modification required, was to tweak the dimensions of meandering MS lines, requiring iterative and parallel simulations.

In the beginning of the project, the LNA schematic was subdivided into 9 pieces (fig.2.3). One for the input matching, transistor, and, output matching, for all 3 transistors. This was

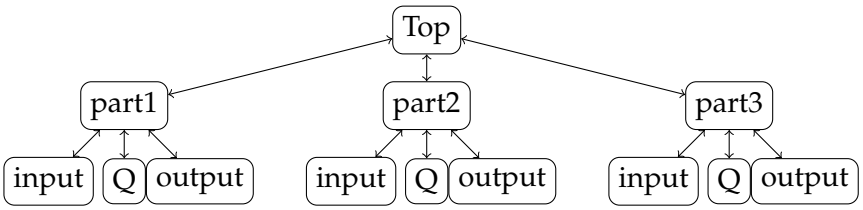


Figure 2.3: *First attempt at project structure*

connected in a hierarchy. The workflow with this became slow, because navigation between the circuit schematics became too frequent. After discovering the bottleneck nature of a heavily subdivided document, it was changed into that of fig. 2.5.

Simulating the meandered lines had several attempts at a method, before finding an efficient method.

1. Simulating all the meandered lines in the schematic with EM extractions.
2. Simulating single MS lines directly with individual EM extractions, editing and simulating repeatedly (fig. 2.4)

Both methods were inefficient because:

1. Simulating all lines, makes it difficult to see the impact of a single change.
2. Modifying and repeating this, is time consuming, requiring waits in between each modification. Comparing with previous results, required a re-simulation.

[6]The process definition is made available by K.U. at the univeristy and is the same one as used previously

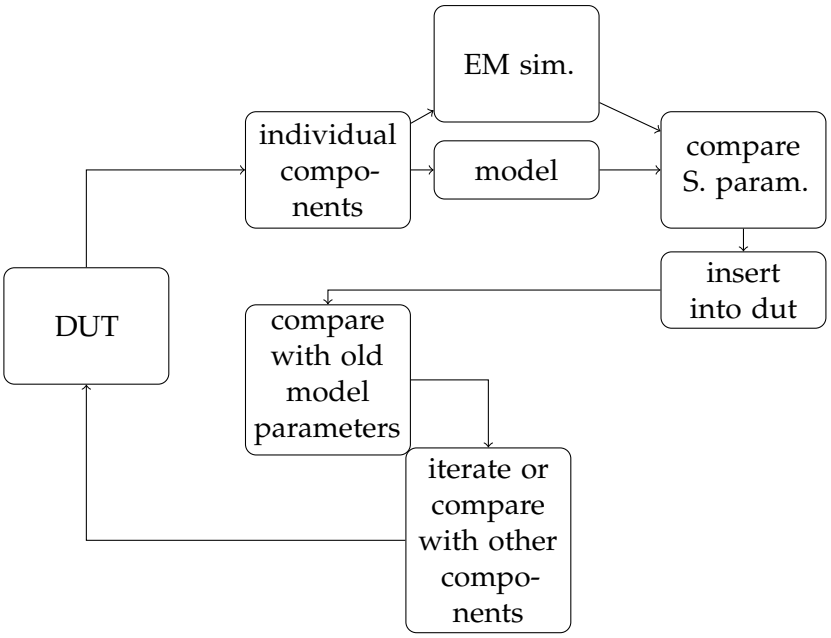


Figure 2.4: *First attempt at workflow*
Simulating individual components of the circuit and comparing against the model response iteratively.

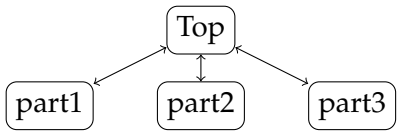


Figure 2.5: *New project structure*

Of the EM modeled components, there was one model simulation, using the linear simulator to give the port parameters of the parts connected to 50ohm ports. Additionally, a "modified" simulation. The modified schematic was used as a test-bench. Several schematics were made per MS line, and then simulated with AXIEM. This enabled bulk simulation of many microstrip lines, with different parameters. Then, all the resulting schematics were imported into their respective test-benches, and the different results were compared with the model S-parameter (fig. 2.4).

This procedure was redundant and time-consuming, therefore it was changed.

The components are EM simulated one at a time, with extraction from the schematic. Both the model, and the extracted S parameters are kept inside the schematic. This allows for the extract flow, but with no re-simulations of old parameters, because a new em structure is created for each change of parameters. This allows for fast comparison with the harmonic balance or transient simulator by just swapping pre-computed em simulations.

The new workflow also allows for fast in-schematic performance comparison of components (fig. 2.6).

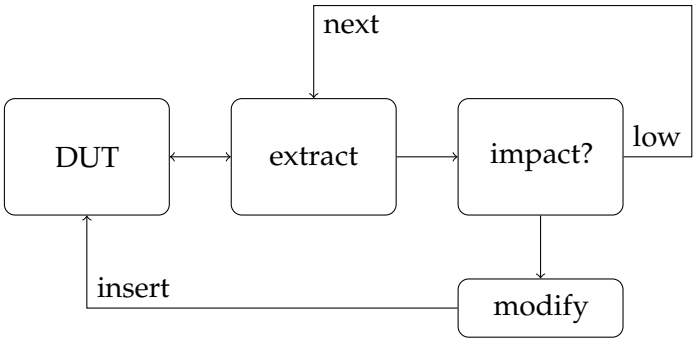


Figure 2.6: *More optimized workflow*
Using the extract flow more efficiently allows for a faster workflow and we can ignore components that don't make much of an impact.

2.5 Moment method accuracy

Generally in the design cycle, closed form models are used early in the design, and then verified by EM simulation. EM simulation is always slower, therefore it is more economic to use as fast models as possible. The simulation either confirms or modifies the expected response of the component that is verified. To ensure that the manufactured circuits match the simulated design, the models used for the design has to be accurate. Models used in the CAD design are based on fundamental principles, or closed form expressions made by experimentalists (e.g. eq. A.24). The difference between the model and the EM simulated result, can become large if the closed form model is pushed past its limits, see figure 2.11 for such a case. One can also use EM assisted modeling, matching a model to simulated responses. If there is made a model, it can aid in understanding the fundamental behavior of the component. For an example of a EM-derived model, see figure 2.1. The simulator uses the method of moments, therefore it is of critical importance to know what affects the accuracy of this method. This knowledge then enables the designer to know the expected accuracy of the circuit and components, before manufacture.

For the method of moments, some properties that affect the simulation accuracy are[26]:

- ❑ Scatterer smoothness, singularities in edges, corners and points.
- ❑ Scatterer geometry, resonances.
- ❑ Incident EM field/excitation, e.g. a plane wave incident on a dipole.
- ❑ Mesh density
- ❑ Mesh defects, irregular element size
- ❑ Geometrical discretization errors for curves or facets
- ❑ Integral equation formulation
- ❑ Expansion and testing functions, order and basis errors
- ❑ Integration rules used for evaluation of the matrix
- ❑ Solution algorithm

For a simulated solution, in a system where the eigenfunctions are not known, the computer self-checks a set of equations, and sees if the set converges. The solution is approximate, just like a Taylor series, and iterating increases the accuracy of the solution. This sort of numerical convergence, continues to be the best method for getting simulation results, and is accurate enough for researchers. It is important to recognize the limitations of the result, that it is a numerical estimation, with no proof of how near the actual solution it is[27].

There are many different approaches to using the moment method for EM simulation. Separate simulators use the method in different ways, for example by different mesh types (triangles vs rectangles), different basis functions (Galerkins, Rayleigh-Ritz, Rao-Wilton-Glisson, dipole moment) [28, 29], and different boundary conditions. Some of the basis functions have special cases, where they are badly behaved, for example at low frequencies, or in special geometries.

For boundary conditions, the AXIEM simulator uses top and bottom boundary conditions with infinite planes of dielectric, in between as default. Sonnet uses a perfect conductor box, surrounding the volume.

It is important to have confidence in the simulator tool. To get this, the AXIEM simulator was compared to the Sonnet simulator at Heidelberg University.

The results were qualitatively compared; a rectangular inductor, a coupler, vias and bends were simulated in the frequency range of 1 to 160 GHz. With the settings of both simulators being modified to account for thick metal, the other options were kept the same. Using the Sonnet API from MWO to simulate the structures, the resulting scattering parameters were all qualitatively similar. The documentation to both simulators is referencing [28](Harrington), when discussing the method of moments. When the two simulators agrees on the behaviors of the structures, we can have greater confidence in our tools.

The accuracy of CEM (computational electromagnetics) simulators, is generally high. The limits on the accuracy, is in reality decided by the one doing the simulations, how the problem is set-up, and how many iterations is done to refine the results. This means that it is the designer that ultimately decides the accuracy of the simulation.

In [30], there is shown that S-parameter accuracy from EM simulators can reach 0.1 %. Additionally, solutions to EM problems in [31] has generally error terms below 10^{-10}.

This high accuracy is difficult to measure in real systems, contrary to the simulator. A high-frequency measurement setup has error terms associated with it, and discontinuities leading up to the DUT, like the probes and pads on the circuit. This is usually calibrated out using de-embedding to move the reference plane to the DUT, and error term calibrations (figure 2.7). Generally, the higher frequency measured, the higher the uncertainty. In addition to being the result of device's properties, one can also see from equation 2.4 (uncertainty principle)

$$\Delta f \Delta t \geq \frac{1}{4\pi} \tag{2.4}$$

that the higher the frequency, the longer the measurement time needs to be, to have the same accuracy.

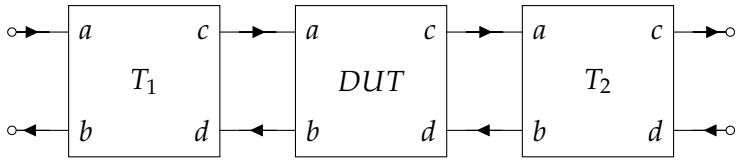


Figure 2.7: *8-term error correction diagram, forward and backward reflection and transmission is measured, T_1 and T_2 are de-embedded, placing the reference planes directly at the DUT. Calibration is done by measuring seven or more independent conditions. e.g. Thru + open/shorted/line on each port[32].*

In conclusion, any wanted accuracy can be obtained by the EM simulator. While this is true, it is up to the designer to decide what is sufficient, and what results are misleading. When comparing simulated and measured response, small deviations will appear, and in some cases the difference can be large. This difference can be analyzed, and lead to improvements on subsequent designs.

2.6 Boundary condition effects on EM problems

For the results in figures 2.8 and 2.9 , the 2d multi-physics application "Agros2d" has been used. The 2d finite-element differential equation solver displays the static solution in the x-y plane. The static solution is, in the perfect case equivalent to the TEM mode solution, because there are no fields in the direction of travel.

Three boundary conditions are set up, and the static electric field on an embedded microstrip conductor with a ground plane is simulated. This is a simple example, chosen because the similarity to the circuits in this thesis, and its simplicity. We can see from figures 2.8 and 2.9, that for simulating EM problems, boundary conditions can be made to have very little impact on the result. Thus the specific boundary conditions chosen for problems, is not very important in the numerical result, but more for the speed of the solver. This is of course assuming that there are no evanescent modes created by the boundary conditions.

2.7 Straight microstrip line simulation

For the straight, short MS lines the simulated difference was expected to be very small. This is because the theory of straight transmission lines is well-known, and its behavior closely matches that of a TEM line.

What may be predicted wrongly here is the ground - return path. As we know from stokes theorem (eq. A.7) the series reactance of a length of wire is dependent on its loop (or line integral). If it becomes different, by degenerated ground structures or routing mistakes, the simulated and real results will be skewed.

For a very short straight microstrip, the EM simulation was not different from the lumped model, and loss from the via path to ground can be eliminated by making the line shorter. The via from TM1 to ground (M1) is 5 µm long, the height and via resistance had some effect

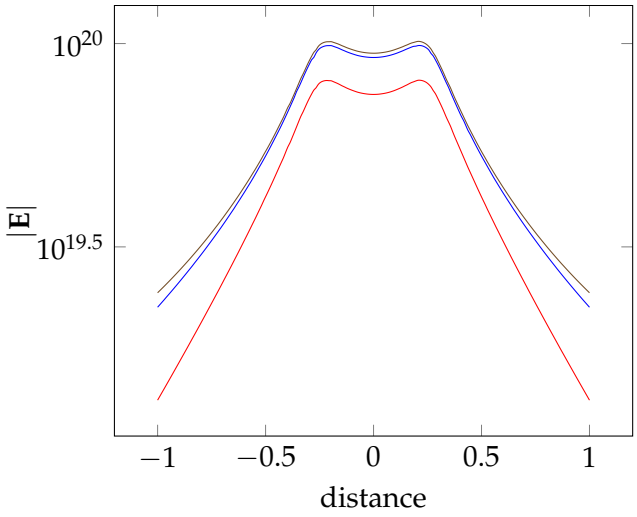


Figure 2.8: *E magnitude below the conductors in figure 2.9*

on the result, as the path effectively is longer. For a longer path, the difference is greater (fig.2.10.). Still, the short straight lines can be assumed to be within 5%.

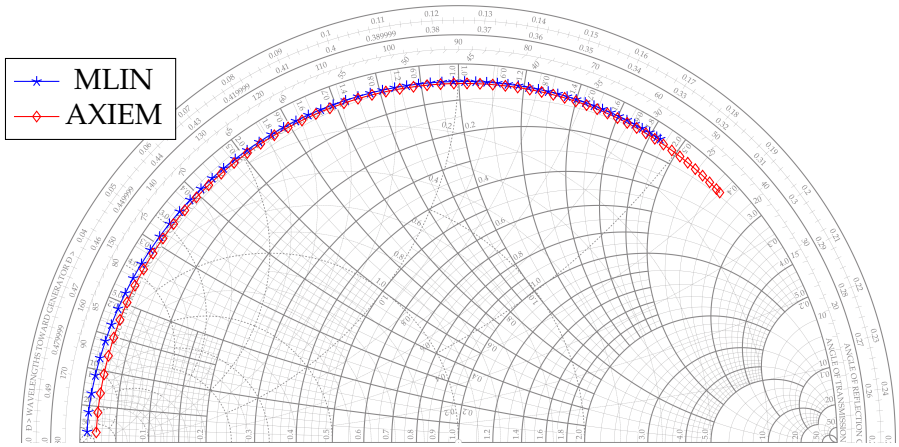
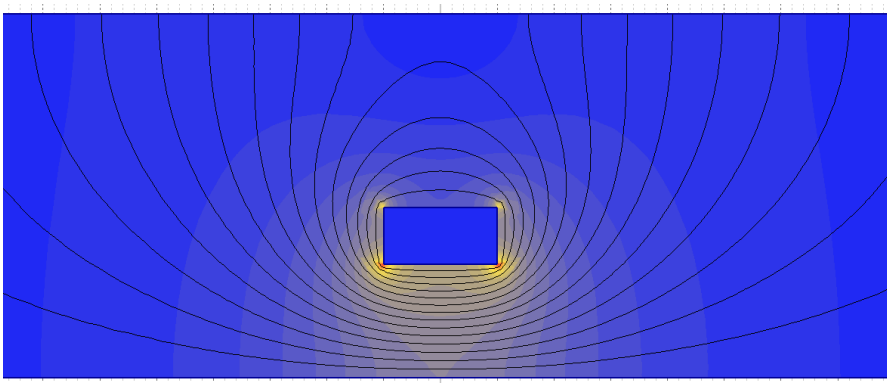


Figure 2.10: *EM and model of grounded straight microstrip lines, grounded,* 200 µm *long,* 5 µm *wide,* 10 µm *tall.* 1 − 120 GHz *with steps of* 2 GHz

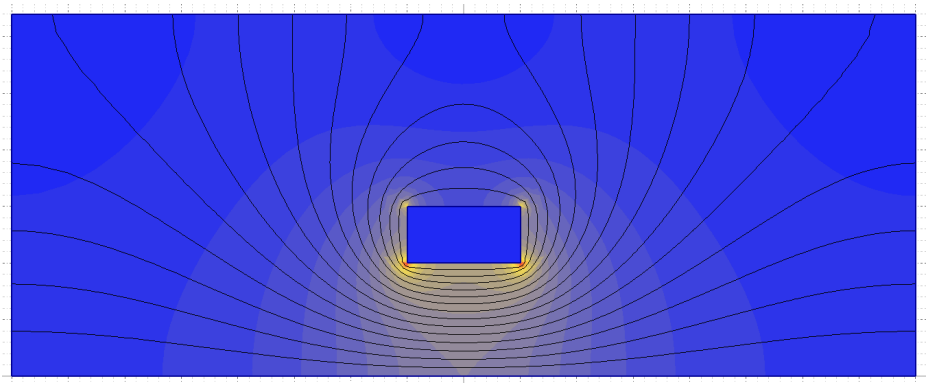
2.8 Meandered microstrip line simulation

For the meandered microstrip-lines the expectation was that they might appear electrically shorter, and also have a lower Q-factor than the closed-form models. Meaning they would represent some more loss to the circuit.

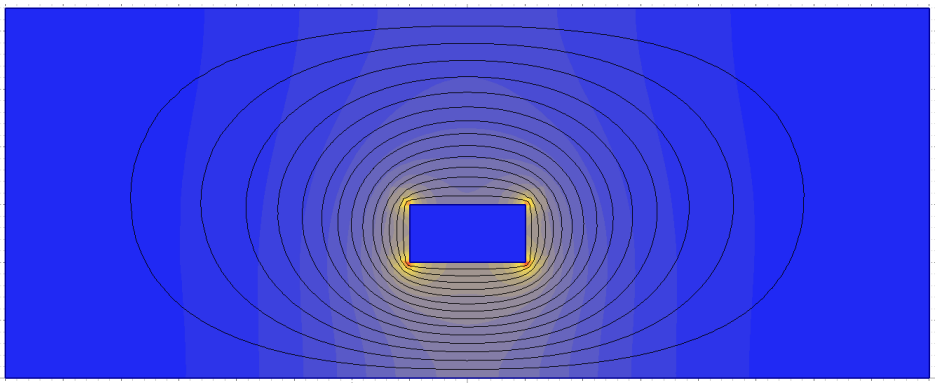
Broadside coupling, differential capacitance, etc.; losses in the EM simulations should be higher, and resonances should be of lower frequency. A bend in the line is a discontinuity, therefore giving a reflection. The fields around the discontinuity needs to change direction,



(a) Very large (effectively infinite) side boundary conditions (AXIEM default)



(b) non-conductive walls as boundary conditions



(c) grounded walls as boundary conditions

Figure 2.9: *Difference in solutions with different boundary conditions (static charge, representative of TEM solution of microstrip)*

Conditions: Central metal : positive voltage, perfect dielectric, bottom wall: zero voltage, non-conductive walls:$\sigma = 0\,\mathrm{C\,m^{-2}}$*. Scalar field (colormap) in* $|\boldsymbol{E}|$ $\left(\mathrm{V\,m^{-1}}\right)$*, Contour field of equipotential lines. Note that the field on the bottom of the conductor is very similar in all cases.*

therefore breaking the validity of a pure TEM approximation. Discontinuities can be modeled as lumped-element T- or π networks [33, 34, 35, 36].

We see a marked difference in the performance of the ideal meandered microstrip and the model. The MTRACE2 model does not account for broadside coupling[37]. So it is relatively easy to create a scenario where the model is insufficient to describe the response of the meandered microstrip. It was found that for a meandered microstrip with a separation distance of $3 \times$ (Substrate Height + Conductor Thickness), the closed-form MTRACE2 model is well-suited for design, and needs only be confirmed by EM.

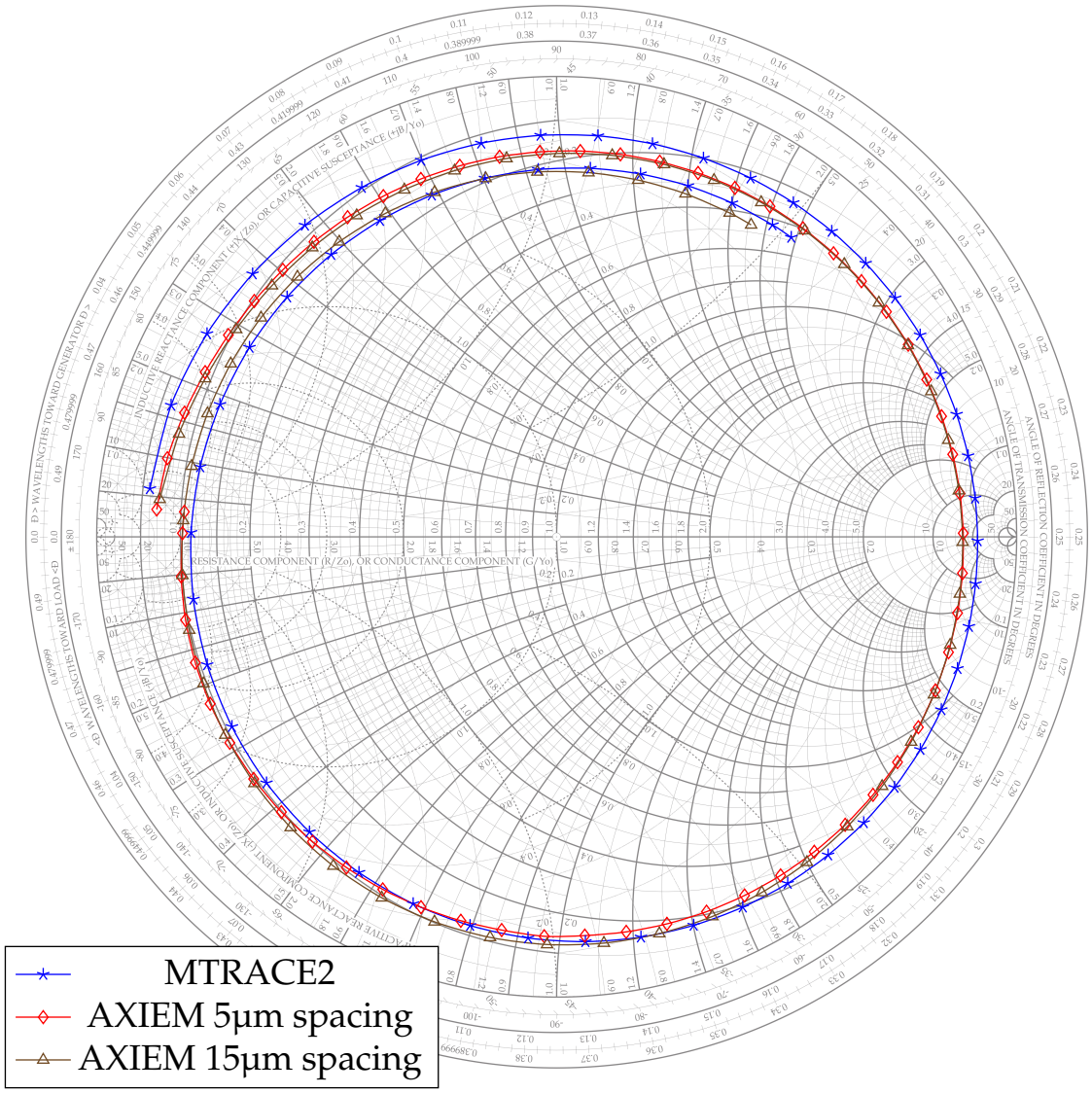


Figure 2.11: *EM and model of grounded meander lines,* 1000 µm *long with* 5 µm/ 15 µm *spacing on eight* 180° *turns (meanders) with a broadside length of* 45 µm. 5 µm *wide,* 5 µm *tall.* $1 - 120$ GHz *with steps of* 2 GHz. *Numerical method shows more capacitance, and shorter electrical length.*

2.9 Unwanted feedback from MS line structures in the system

Both previous projects on 60 GHz [4, 3] mention a need for discovering wether the transmission lines couple across the amplifying stages. To do this there is first introduced a simple model that is discussed, and then related to EM simulation results

To analyze the parasitics, the simplest approach is to get EM simulated S-parameters from each of the parts. Then a comparison of total circuit response vs. the model, will show if tuning is necessary. To do this, the design was first split into three stages, then duplicated. One original, representing the model, and one for EM simulations. S-parameters are assumed to be sufficient to verify if the circuit has good performance, as EM modeling is strictly linear.

After this a simulation combining several parts in the individual stages is done, to rule out any effects between the metal structures or the ground layer. To model the combined behavior, a simple model should be used to facilitate understanding of the problem, but the model should not lack the complexity to accurately represent the problem. A large simulation with many ports tends to give wrong results, because of the large number of ports, so this is not recommended. What really needs to be shown, is that especially the large metal features ($\geq 200\,\mu m$), have valid response, and that the coupling between them is negligible. To demonstrate effects of coupling, we have figure 2.12, showing uncoupled and coupled symmetric transmission lines across an amplifier. Calculated from linear theory, the response is approximately of the form:

$$S_{21} \propto\approx \sin^2(\omega\beta l)$$

when not coupled. When coupled it takes on the form (rearranged with the general feedback equation and a coupling factor, using the transfer function of a single transmission line from [39]):

$$S_{21} \propto\approx \frac{1+\coth(j\omega\beta l)}{1+K'\coth(j\omega\beta l)} \cdot \sin^2(\omega\beta l) \tag{2.5}$$

Where $K' = K \cdot C_1$ is seen as the coupling factor times a constant[7], making the first factor go to 1, if the coupling is zero. This equation shows the typical behavior for symmetric lines, different resonance frequencies will enter in an asymmetric system, also loss and line impedance difference is disregarded. The model is very simple, but it is used to demonstrate the huge effect coupled transmission lines can have over an inverting amplifier. To relate this to RF components, one can look at the two transmission lines as a generic coupler, and from introductory books in high-frequency electronics we see that the two ports that are connected are isolated from each other in the perfect case, this is also another perspective of the zero effect at resonance in figure 2.12.

The simulated result with the most complete model for the microstrip coupler, including loss and dispersion, has instability when tightly coupled. This is because the loss combined with the microstrip feedback, effectively makes the source see a negative impedance, and as

[7]The constant K is really made from a algebraic combination of different impedances in the circuit of fig.2.12. Later there was found more complete equations for reflecting medium in [31, eqs 5.5.5-8]

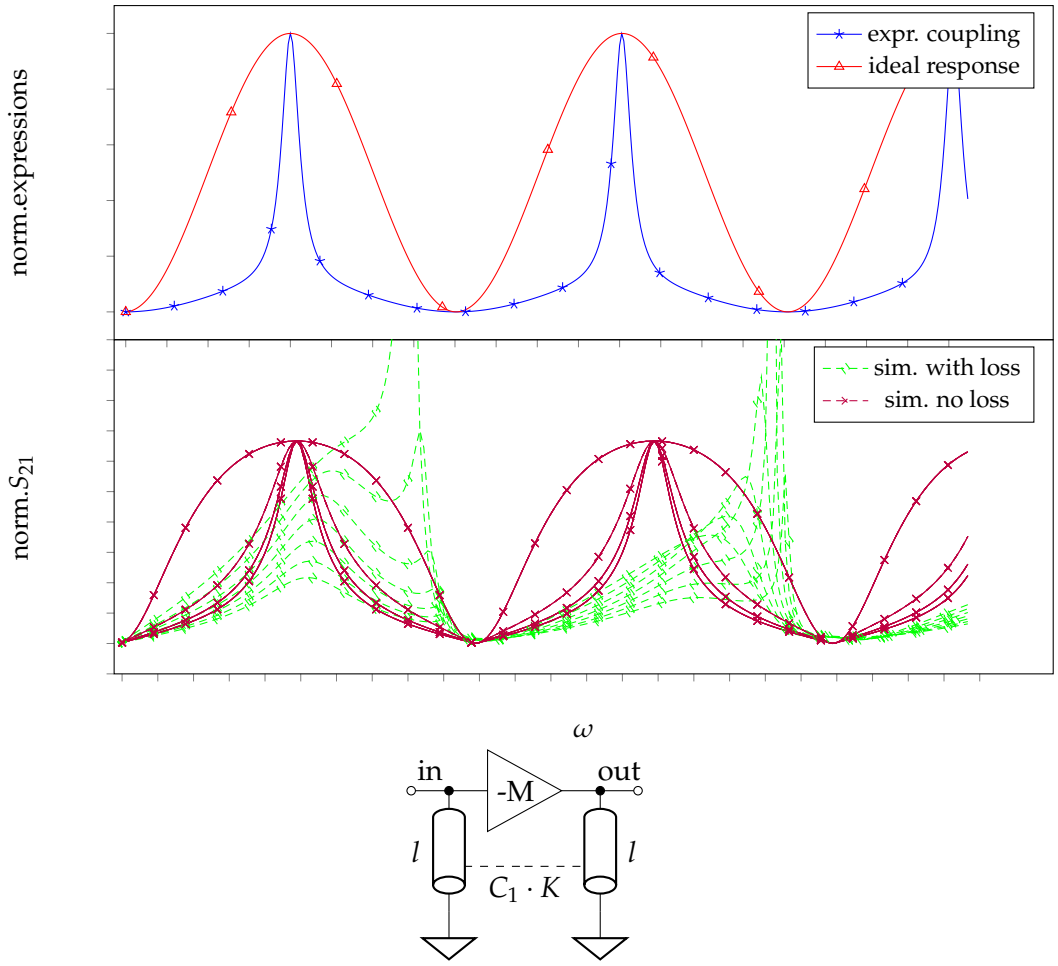


Figure 2.12: *Initial model for coupling, Geometric models (equation 2.5) and simulated models. The distance between the strips is varied to generate the multiple plots for the S_{21}. (y-axis not to scale) The expression and simulated results have a degree of similarity to the results in [38].*

follows, the positive feedback causes unstable regions for the amplifier. The equation and graph shows a severe bandwidth reduction, and a loss of gain outside of resonance when the coupling gets large (at resonance the transmission lines have no effect). This will be a symptom, only if the coupling is strong. There is also the issue of stability. For stability to be affected, there also has to be a large amount of coupling. If this appears in simulation, then the circuit will be modified. For asymmetric expressions for coupling, see [40]. The article also contains extensive expressions for coupling.

In general, all the unwanted effects appear with very large coupling factors. It has been experienced with help of the AXIEM simulator that with some distance comes good stray isolation. If there are unwanted effects of this kind in a prototype circuit, there is little chance that the unwanted broadside coupling across an amplifier stage is responsible, as long as the lines are not placed excessively close. It could be other effects like common conducting paths through the power network or mutual inductance of chip leads.

2.10 Grounding

Grounding is not a simple issue. The definition of a ground is varied among the literature, as "reference point", "common return", or "voltage source of zero volts". It is called a constant voltage. In circuit theory, the ground is an "infinite current sink". It can also be modeled as an infinite capacitor, so it can accumulate infinite charge without changing its voltage. In electrostatics, voltages are defined as the sum of the total charges on each conductor, a zero volt reference is then a conductor where all charge that enters it disappears. An integrated circuit has no such thing. As we are working with high frequency signals with wavelengths within the same order of magnitude as the chip, a well defined "return path" for the signal is required, for good signal integrity [41], - this will act as a non-ideal ground. If two points on a schematic are marked as "grounded", the charges on them will distribute across all its common paths on the chip, like the ground layer and the substrate. Looking at this from the perspective of Stoke's theorem, the return path of a current loop will be of unknown length. For signal traces with badly defined return loops, the inductance can vary extremely much.

For the designer, it is important to know where the return path of the signal goes. There are a lot of trade-offs in this area; isolation, DGS[8] design, and to know if there is a risk of slit- or surface- modes or other resonances. This can be explored in a design with full-wave EM simulations.

[8] Defected Ground Structure

3 EM simulation, verification and tuning of LNA and PA

Both the LNA and PA topology are three-stage common emitter amplifiers. This is because of the limit of the maximally available gain of the transistor (~9-6 dB), at the wanted frequencies. With this low amplification, we need 3 stages for 20 dB of gain.

In high-frequency designs, a larger part of the design effort is spent with making suitable passive interconnect. This is called matching networks. The matching networks enable power transfer (both current and voltage) in the system, and controls the effects of distributed electrical networks. In low-frequency analog design, the signal is viewed as simultaneous everywhere (non-causal or the propagation time is zero), effectively removing the possibility of waves. In the domain of higher frequencies, this non-causal assumption falls away and allows for the existence of waves, modes, reflections and dispersion.

Different authors specify different ways to estimate when a system needs to be concerned with waves. This determines when a designer needs to use high frequency techniques. Some say $\frac{\lambda}{20}$ of the highest frequency of interest (in air, for 50 Hz, $\frac{\lambda}{20}$ is 300 km, for 60 GHz; 250 µm).

The two designs that were made by Pallesen and Schou are here analyzed with the help of EM simulations and yield analysis, for the purpose of tuning and validation.

3.1 LNA verification

The LNA is the first active component, a received signal sees. As such it has key performance parameters that decide the total performance of the system.

The LNA mentioned in section 1.2, designed by Pallesen, is a circuit combining wide-bandwidth and low noise. This introduces some inherent trade-offs in the design space, as the lowest noise is *always* achieved with the lowest bandwidth (eq. 3.1).

$$P_{WN} = kTB \tag{3.1}$$

The LNA is the most critical component of the receiver chain. This is because the noise figure of the LNA decides the minimum detectable signal (eq. B.6). The LNA provides the first stage of gain, setting the limit for receiver noise (eq. B.3) performance, dynamic range and system capacity (eq. B.9) . The design is already within specifications, when using the models in MWO.

The future work section in the previous work on LNA design, [4], describes that there are mainly two things needed:

1. EM simulation confirming operation of the circuit
2. EM simulation inspecting possible coupling across the transistors, caused by MS lines. This can lead to decreased bandwidth and oscillations. This is shown not to be the case, and the problem is discussed in sec.2.9.

The LNA described in [4] is a three-stage common-emitter (CE) design. It uses a π-type input matching network, for an additional degree of freedom on the input matching, compared with a two-element network. It uses m-type inter-stage matching, and for the output there is a tapped-C transforming network. The emitter lines are used for noise matching and stability improvement, by degenerative local feedback.

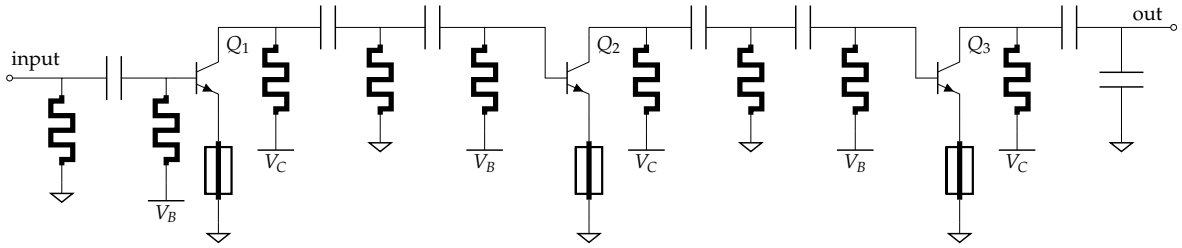
Table 3.1: *Specifications table*

LNA	S_{21}	NF (60GHz)	Pdc
pre	22.4 dB	4.33 dB	9.8 mW
post	21.2 dB	4.31 dB	9.8 mW

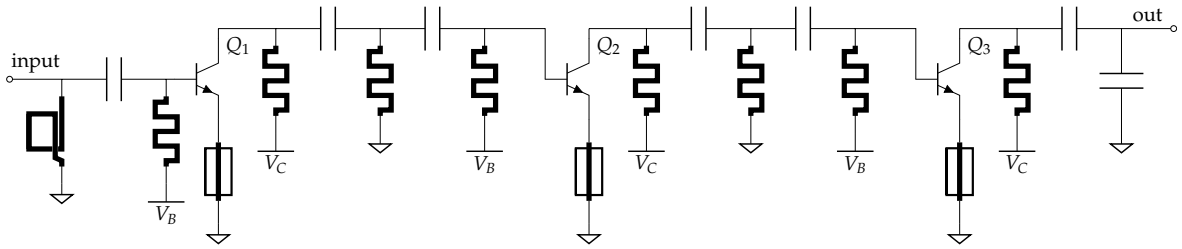
All the individual large MS lines, were individually checked by EM simulation and comparing each component to the closed-form model response.

This workflow was inefficient (figure 2.4), and was later upgraded to that seen in (figure 2.6). See section 2.4.1 for more on this.

Interpretations of the results of the second workflow progression, showed that most components were close to their ideal responses. They were changed a little, but not much, to be brought back to the designed response. The only exception was the first matching MS shunt line. This line was meandered and long, and on a sensitive node in front of the base of Q_1 (see figure 3.1a) . The loss in this when EM simulated (see figure 3.7) caused the circuit



(a) Old LNA schematic



(b) New LNA schematic

Figure 3.1: *Schematic pre and post modification*

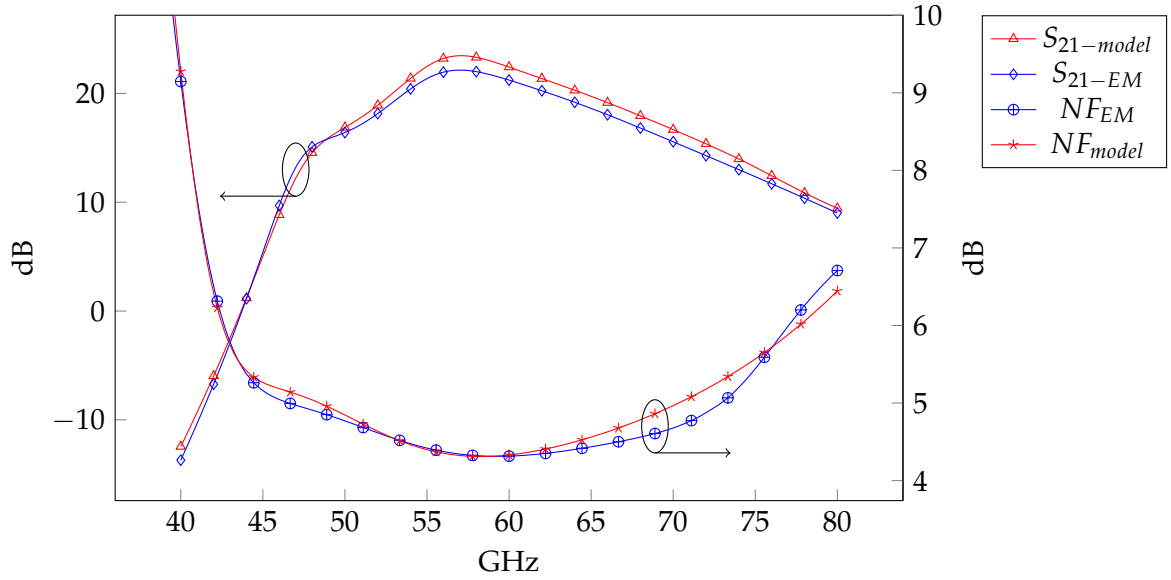


Figure 3.2: *S_{21} and NF before and after tuning*

to malfunction. The gain was severely degraded, as well as the noise figure. This had to be rectified.

3.1.1 Rectangular microstrip inductor design

To reduce the loss, and increase the Q of the component (figure 3.4), it was decided to move most of the metal up to TM2.

The line is long (515 µm), so a slow-wave (or artificial transmission line) structure, interleaving low and high Z_0 elements of MS line was attempted. A slow wave structure, is a structure where alternating elements of different characteristic impedances, acts electrically longer than it physically is; the length of the line can then be reduced. This did not reduce the

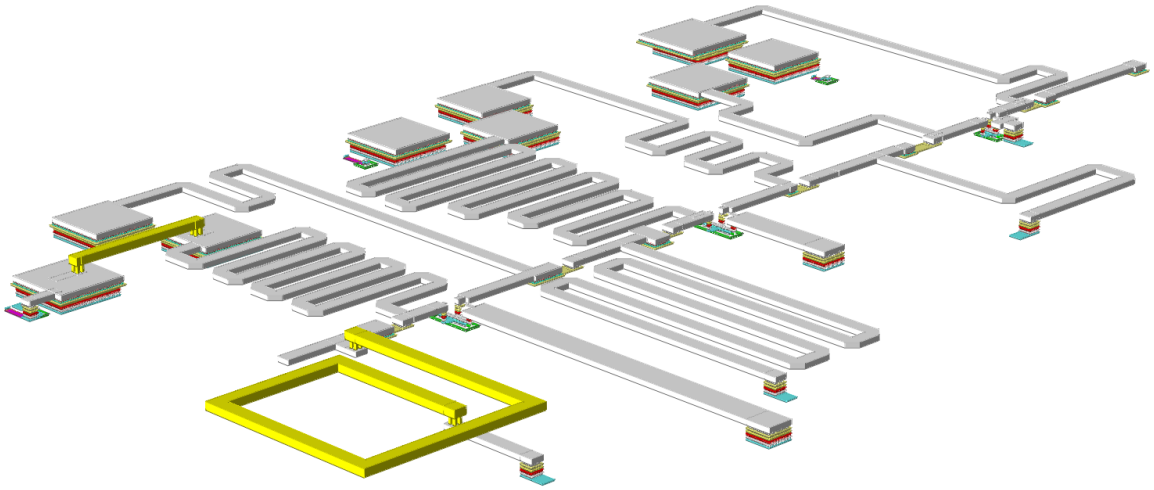


Figure 3.3: *LNA Layout, excluding ground layer on M1*

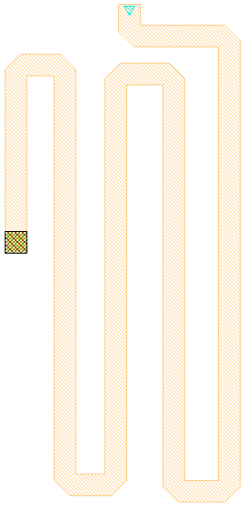


Figure 3.4: *Replaced MS line layout*
This particular MS line has long parallel meanders, this causes stray broadside capacitance (shorting out the length) together with its location on a sensitive node of the circuit it had to be changed length = 515 µm

length significantly, and had the disadvantages of long simulation times, and no significant loss differences. Then, a slow-wave structure with defected ground slits was attempted. This had lower length, but even longer simulation times. Therefore, the design cost would be high, if a optimized solution was to be found.

For reference; a slowing factor of 2, giving a new length of 257.5 µm, would need to consist of elements $\frac{\lambda_{80\,GHz} \cdot 5^\circ}{360^\circ} = 25.7\,\mu m$ long[1], so about 10 elements. With this length, the width is also very limited, inhibiting the slowing factor, a.

$$K = 2a^2 + 2\sqrt{a^2\left(a^2 - 1\right)} - 1 \tag{3.2}$$

[1] 5 electrical degrees is a rule of thumb such that the highest frequency of operation on the artificial transmission line is on half the Bragg frequency of the line.

Where K is the ratio of the microstrip impedance, $\frac{Z_A}{Z_B}$. We see that K must be 14, therefore, the high impedance ratio is difficult to make with the limits previously set, because for $Z_0 = 50\,\Omega$, Z_A and Z_B would have to be $\sim$ 13 and $\sim$ 182 ohms. So both are impractical impedance values for microstrip in this process (requiring a ratio of W_{max}/W_{min} of over 100, see figure A.2). The search for a good artificial transmission line type replacement, then ended.

After this, a rectangular inductor line was attempted as a replacement component. After few iterations of the main geometry, the ground layer directly below the inductor was removed, to improve performance, and the component was satisfactory (figure *3.5*). A performance comparison is shown in figure 3.7.

The inductor is $75 \times 75\,\mu$mwith a 10 µm long entry line and a 40 µm long underpass, to the shunt end (figure 3.5),. Total length is 370 µm and the area required is slightly less than that of the old component . The spacing between the turns is 15 µm, to balance broadside capacitance with mutual inductance $\left(\frac{L}{C}\right)$. If the broadside capacitance becomes large, it reduces the effective inductance. The metal ground layer is also removed from under it, increasing the height of the MS, decreasing shunt distributed capacitance. Simulated results shown in figure 3.6. The design of DGS structures and techniques involving ground plane removal or patterning, are covered in other material ([33, ch. 6]), and is not covered in length here.

The lines connecting the supply voltage for the bias network (V_{Bias}), and the collector voltage (V_{CC}), were disconnected, to decrease the chances of inter-stage coupling through the supply network, and to enable tuning of the bias voltage from an external pin. The vertical connections to the transistors were changed, to decrease the possible extra parasitic capacitance across the base-collector node.

3.1.2 Future work

The bias network needs to be redrawn because the vias in some of the connections do not adhere to the design rules. This was not done here because of time constraints. Power network needs to be drawn, and more bypass capacitors for the supply added. Then the circuit is ready to be inserted into a larger design.

3.1.3 Conclusion

To summarize, the performance of the LNA (fig.3.2) was changed slightly, The noise figure was improved, mostly as a result of the rectangular inductor having higher impedance than the old model. But also due to some subtle changes, in the inter-stage matching networks. The inter-stage matching networks loss, when simulated with the EM simulator, had a different spectral response. The combined effect of this, caused the noise figure for frequencies above the 60 GHz band to increase, while at the same time reducing the losses slightly inside the band. The deepest point of the noise figure (fig. 3.2), is dominated by the input noise matching. While at 61-70 GHz, the gain of the first transistor has greater influence (i.e. the input matching combined with the degeneration, and the equivalent impedance in the collector node). This complex combination has a large influence on the gain. The gain slightly changed with the modifications, and subsequently, we get a slight improvement in noise

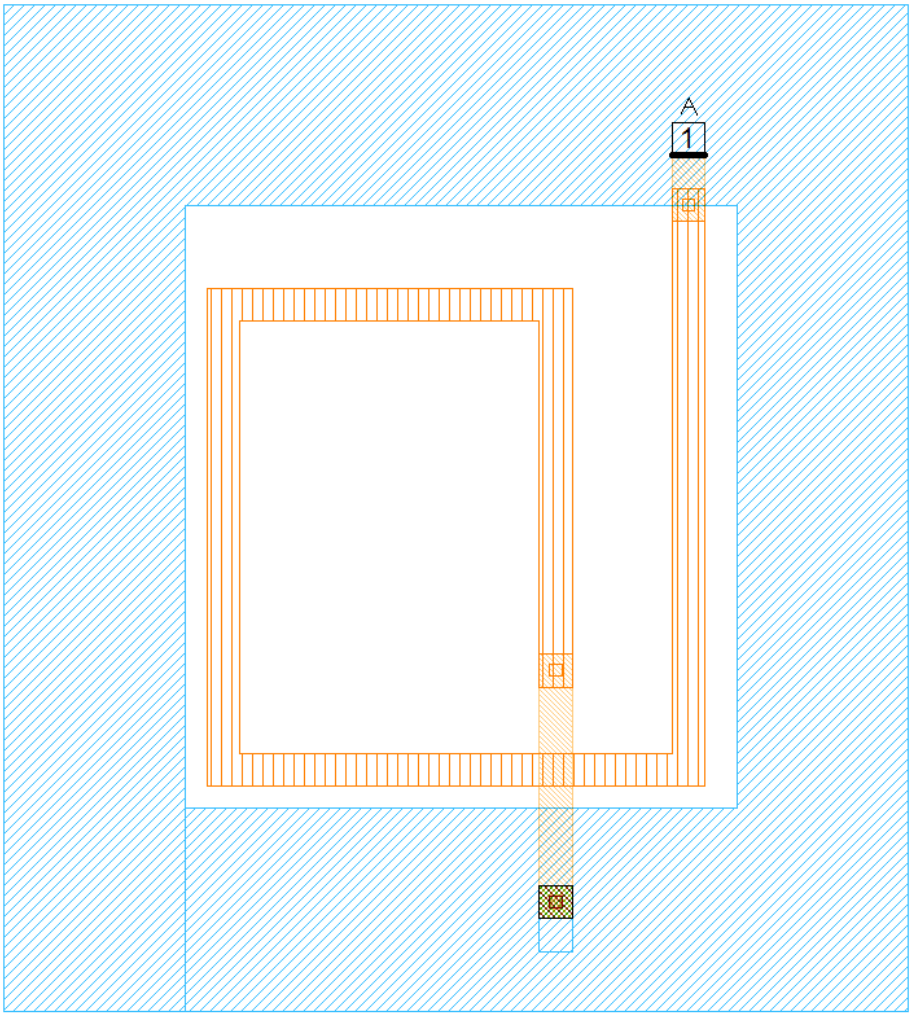


Figure 3.5: *Rectangular inductor layout with DGS*

figure. At higher frequencies the noise figure rises again, showing the trade-off, where in band noise was reduced for increased out of band noise.

From the experience gained, a faster workflow for these kinds of designs could be one, where the limits of the models were figured out beforehand by EM simulation, and then the models were used within their limits from the start. This would enable faster design cycles, and reduce the risk of having to re-design after EM simulation. This knowledge was used in the design in section 4, when designing the OOK modulator.

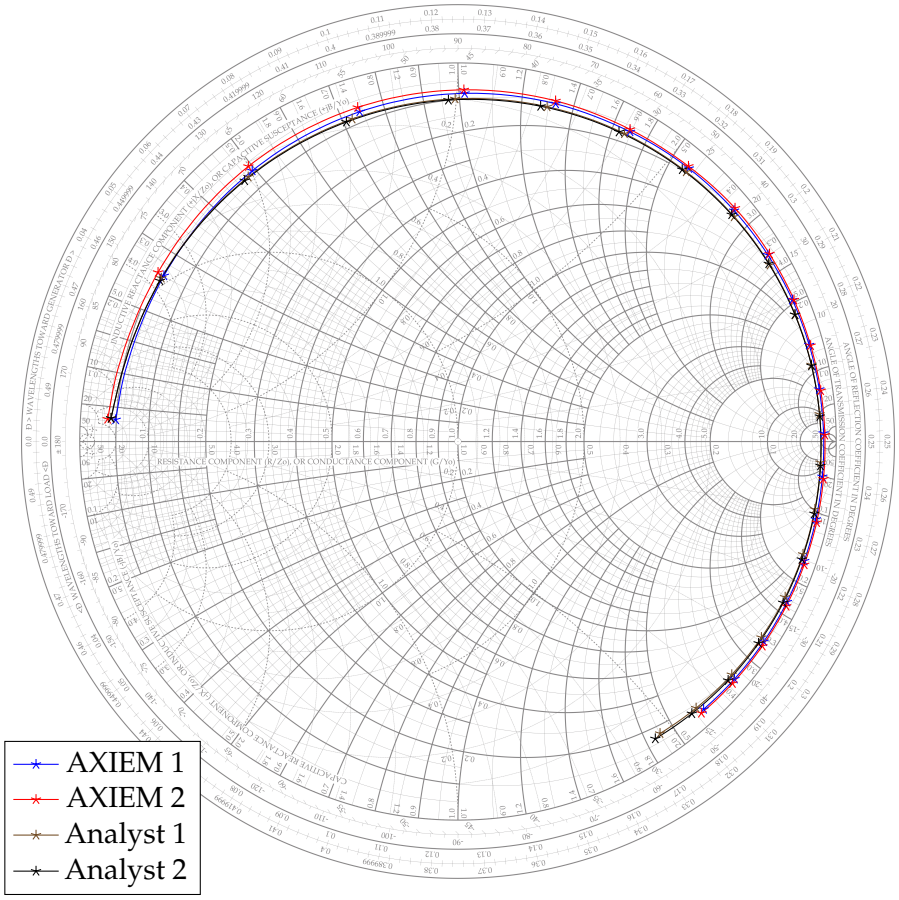


Figure 3.6: *AXIEM MoM and Analyst FEM simulation of S_{11} of the rectangular shorted inductor. 1 to 160 GHz. Simulation times for MoM: 2 minutes, for FEM :60 and 260 minutes*

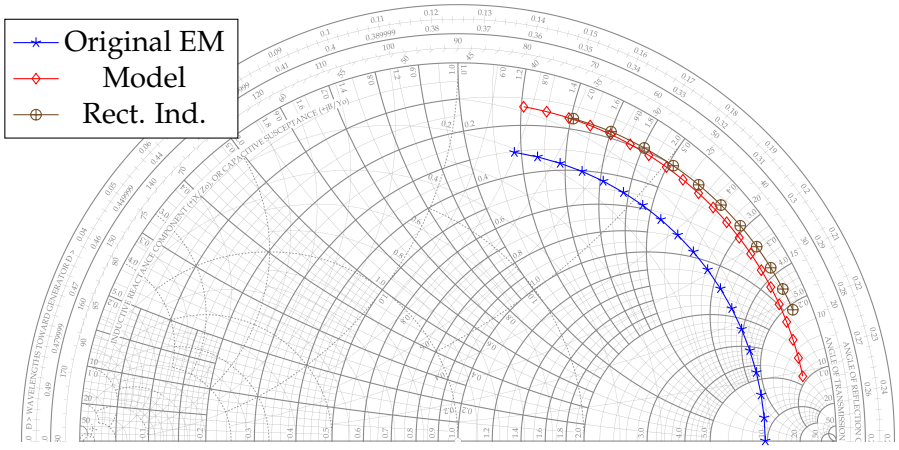


Figure 3.7: *Reflection of new rectangular inductor replacement*
The original MS line (figure 3.4) , when simulated had lots of loss ($|\Gamma| \approx 0.8$ instead of the ideal case of $|\Gamma| = 1$), whereas the replacement rectangular inductor (figure 3.5) lies on $|\Gamma| \approx 0.9$, the same as the model. We can see that the new component has higher characteristic impedance by its shorter locus for the same frequency span.

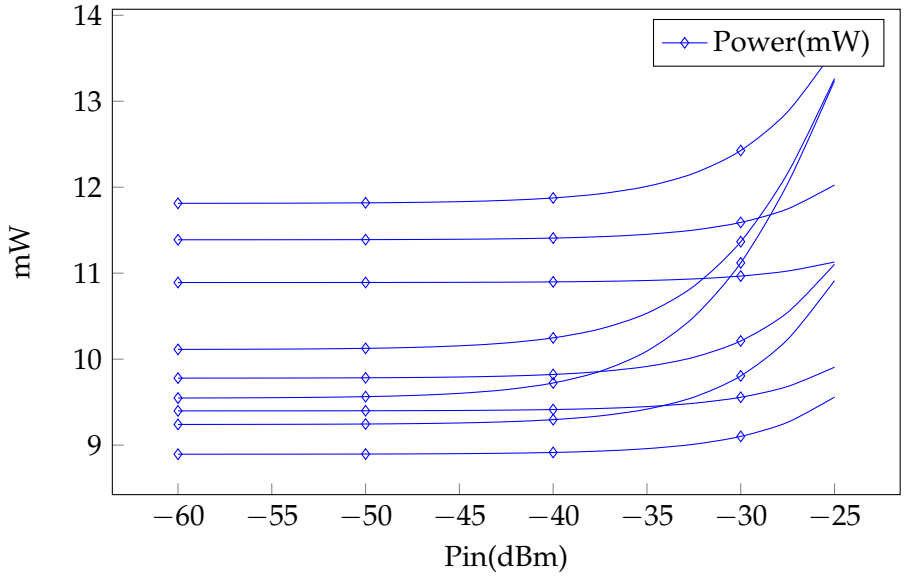


Figure 3.8: *Power consumption with HBT and temperature corners. This graph display the range from the slow, normal fast HBT corners and 0 to 100 degrees C.*

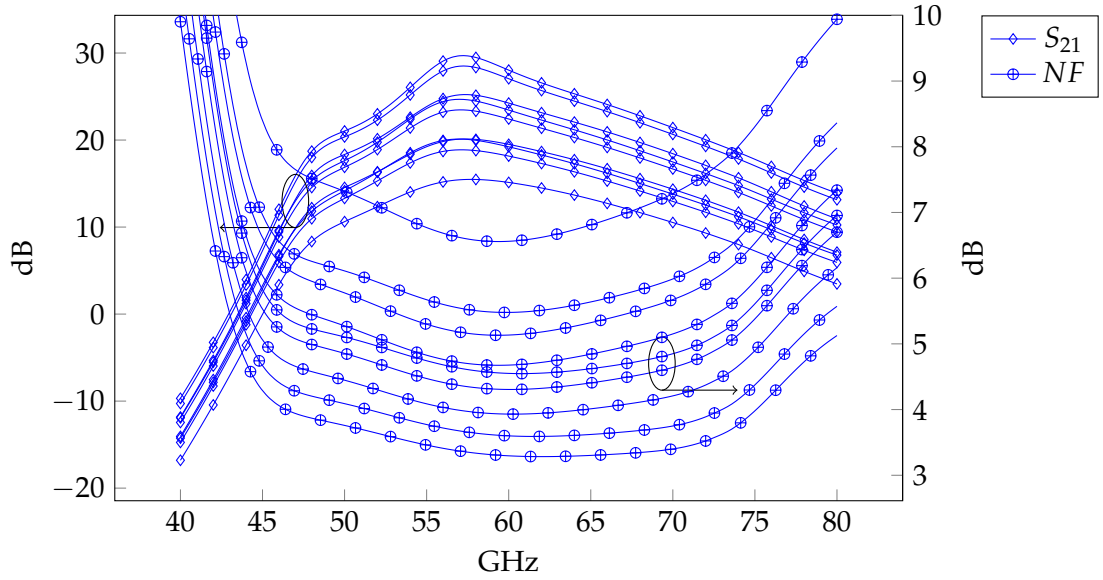


Figure 3.9: *LNA NF and S_{21} over corners*

3.2 PA verification

The power amplifier (PA) in a wireless data transfer system, is responsible for providing power to the antenna, and by extension; the receiver. This is the component of the system that has the highest power density internally, and is probably the part taking up most of the power budget. Efficiency is therefore very important in this component. It has to be efficient enough to keep the power dissipated low, and, at the same time enable a high output level.

In this circuit, the large metal features has more spacing than the ones in the LNA (see sec. 3.1). This made the EM verification process significantly faster, because of less broadside coupling between the meandering structures, the model of the lines often had the same response as the EM simulated response.

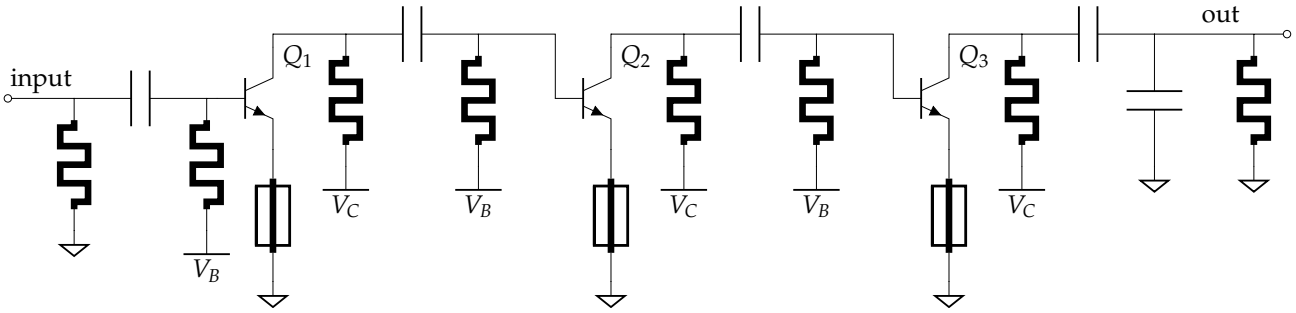


Figure 3.10: *PA schematic*

This specific Power amplifier design, is demonstrated in Schau's work. The design is already sufficient with respects to;

- ❑ Gain
- ❑ Power
- ❑ Noise
- ❑ Bandwidth

The PA is a 3-stage degenerated CE topology. This is, in essence the same kind of topology as the LNA. Input and inter-stage matching is done with high-pass π networks. The output matching network, is a tapped C transformer loaded with a transmission line.

The transistors have $f_T \geq 225$GHz, but they are not very unilateral, i.e. their S_{12} is high. For efficiency, the PA is biased in class-AB. In class AB, the transistors are operated with reduced conduction angle, so, this accounts for the relatively high efficiency(19%). The circuit is input and output matched to nominally 50Ω.

What Schau explains is needed[3, sec."Future Work"], is an analysis of:

- ❑ Parasitics
- ❑ Corners
- ❑ Yield

What is optional is:

- ❑ Reducing the footprint
- ❑ Stage gain scaling optimization
- ❑ optimized load impedance for improvement of PAE

Table 3.2: *Design goals*

Specification	Value	Unit
Power Gain	20	dB
1 dB Compression point	≥ 5	dBm
Power consumption	≤ 30	mW
Bandwidth	9 (57-66)	GHz
Center frequency	61.5	GHz
in-band reflection coeff.	≤ -10	dB

The fractional bandwidth, will be greater than 14,6%. This is a relatively wideband design, compared to other 60 GHz designs, where the power amplifier frequency response is designed to fit into channels, defined by the IEEE 802 set of standards, for wireless communication (bandwidth of > 2.5 GHz).

It has a -10dB reflection coefficient equivalent to VSWR $= 1,92$. It is also mentioned, that some circuit elements exist only on the layout, so the schematic and the layout is inconsistent. This should also be considered to be a possible change, with pros and cons; consistency between the schematic and the layout increases the accuracy of the schematic, but also increases its obscurity.

3.2.1 Reasoning

Vcc and VBias, needs to have separate pins so that voltage tuning can be done in testing (following the same line of reasoning as in [42], where the base-collector junction capacitance can be changed, independently of the bias voltage and vice-versa.). Both power lines are a nominal 1.2V. Putting the bias voltage on its own pin, should allow a tester to tune the bias voltage for all the transistors, giving a degree of freedom for testing. For adjustments, the voltage range of 1-1.6V is suggested. The variation of the Bias circuit supply voltage, will change the base voltage for the transistors, but V_{CE} will stay at the same value. This has the advantage that the voltage-dependent parasitic capacitors on the collector node, are unchanged, minimizing any change to the matching behavior of the stages. Without any control of the input, the output power will be unpredictable (fig 3.17). Tuning the gain of the PA, can be as simple as setting a resistive voltage divider on the supply. Other projects does automatic gain compensation (AGC), with internal sampling, and digitally controlled bias feeds ([43]). Circuits inspired by this, might be a sound design choice, if the design is to be mass produced and self-adjusted. The separation of the bias and collector power supply lines, might also reduce the coupling between them. Seeing as they need only be connected

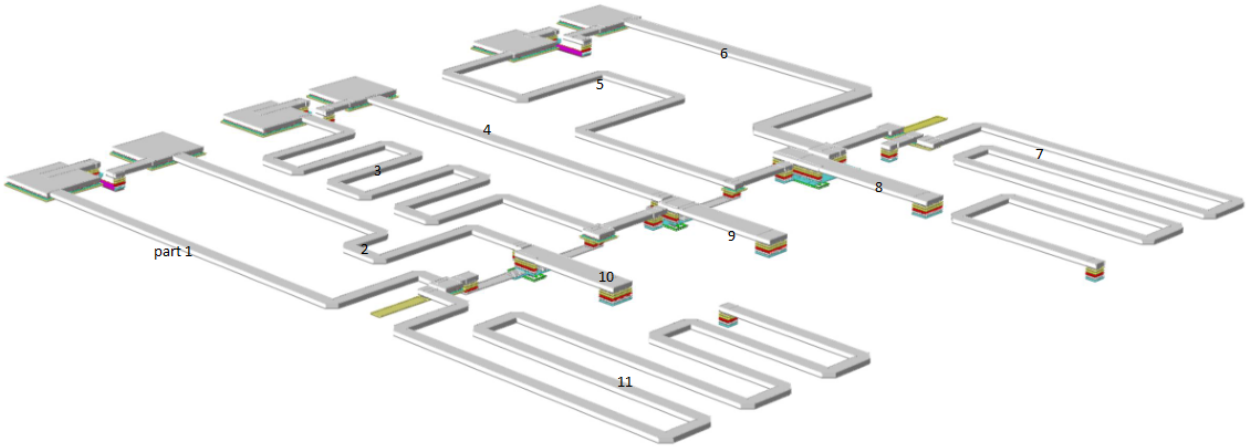


Figure 3.11: *The PA layout without the ground plane on M1, the parts labeled clockwise from the top left. Reproduced from [3]*

outside the chip. Discontinuities in the signal path, should also be reduced, for the obvious reason that the more (unwanted) discontinuities there are, the more losses there will be[35].

Error measurements are done with L2 (l^2) norm, called "S parameter model difference" in AWRDE, calculated in the form of [44]

$$\varepsilon = \frac{\sum_{i=1}^{N}\sum_{j=1}^{N}\left(\left|S_{ijA} - S_{ijB}\right|\right)^2}{N^2}$$

(Where ε is the error).

Corner analysis is done with a strong caution against quick assumptions, in interpreting the results. Measuring efficiency over HBT corners, seems like a simple task, but to get results that interpret properly, the power level in the circuit needs to be the same. This is because it makes no sense to compare the efficiency of a circuit, when its output power differs by over 10dB. Test-benches measuring power gain and efficiency, were set up to have a constant output power level (5dBm), or to always stay at the 1dB compression point (using MWO elements CONSTPOUT & XDB). Orthogonality of the different corner cases is initially assumed, i.e., the varying parameters are assumed independent. This is to simplify the analysis. The orthogonality assumption will lead to very extreme cases, (unrealistic) of performance variation. This large variation is assumed to extend further than all realistic scenarios, because of regression toward the mean.

3.2.2 Work done and results

First round of EM simulations, went into modeling the parts (1-11). In this design, the models and the simulated response, was very close resulting in an initial $\varepsilon \leq 3\%$ error between the model and the EM simulation. There was almost no difference with the straight conductors, and some more difference with the meandered structures. Then the coupling was qualitatively assessed, by simulating the parts with their original separation, and then with a larger separation. The simulation of the coupling showed no difference between original

spacing, and double this spacing ($\varepsilon < 1\%$). A rule of thumb, is that the coupling between lines is negligible when the separation is more than 2 times the substrate height (possibly from [38, fig. 12]). A quick preemptive check was done to this guideline. The statement is very dependent on line length, but any lines separated by more than 4 substrate heights, had minimal coupling, even when exited in the odd mode for maximum coupling (figure 3.12). Because the distances between the measured lines are more than 20 µm, the low coupling is sensible. This is reasonable, because designs with high coupling, like the design of Lange couplers, have very tight spacing, like [45] using 2 µm between the metal features. Thus, a large spacing of 20 µm should have low coupling. We see from figure 3.12, that the reverse gain S-parameter, S_{12}, for the HBT is an order of magnitude larger than the coupling between the base, and collector transmission lines. This figure also shows the error terms (ε) for the simulation of distance between the lines, for odd and even mode excitation, and the EM simulation versus the model.

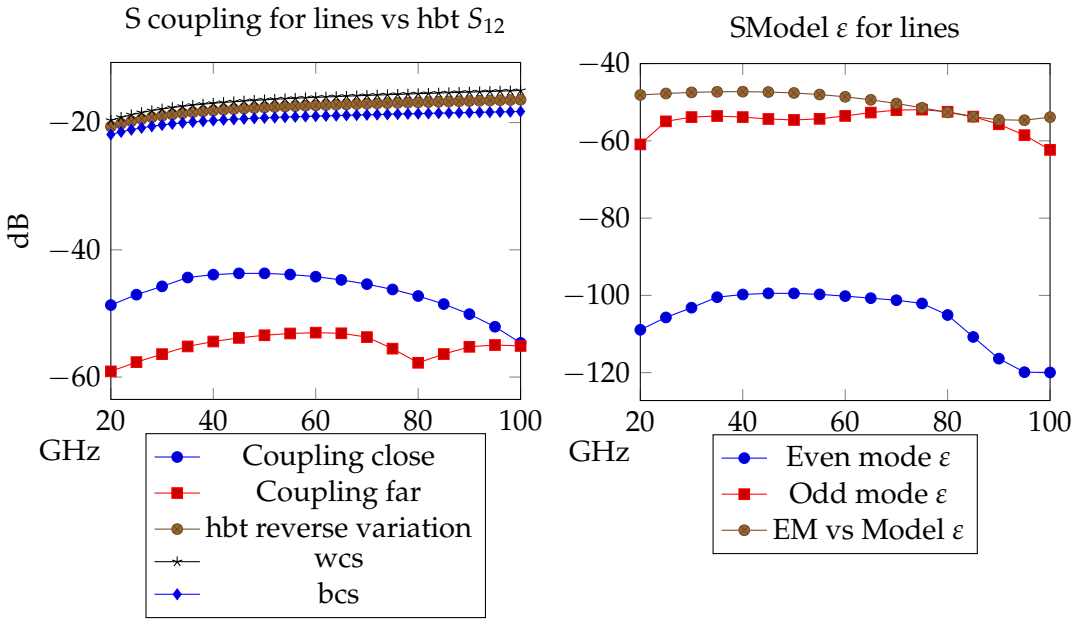


Figure 3.12: *S_{12} of HBT + S_{12} of coupled signal + SModel*

Sometimes the simulation would be obviously wrong. As an example; terminated metal lines having a reflection constant of 1, i.e. being an open circuit, at low frequency. These results were ignored as faulty simulations, or faulty extrapolations, by the software. Transistor contacts was modified to small contacts, fulfilling current density rules, but kept small in an attempt to minimize collector-base capacitance. The lines shorting V_{cc} and V_{Bias} was removed. The number of times the signal line goes up and down through the layers of the chip, was minimized by changing some routing, especially around the tapped C transformer.

Many test-benches were made to characterize the circuit over the corners. In the normal corner, the circuit fulfills all performance requirements. It is also good for the best-case corner, although the gain is much higher, requiring a lower power input.

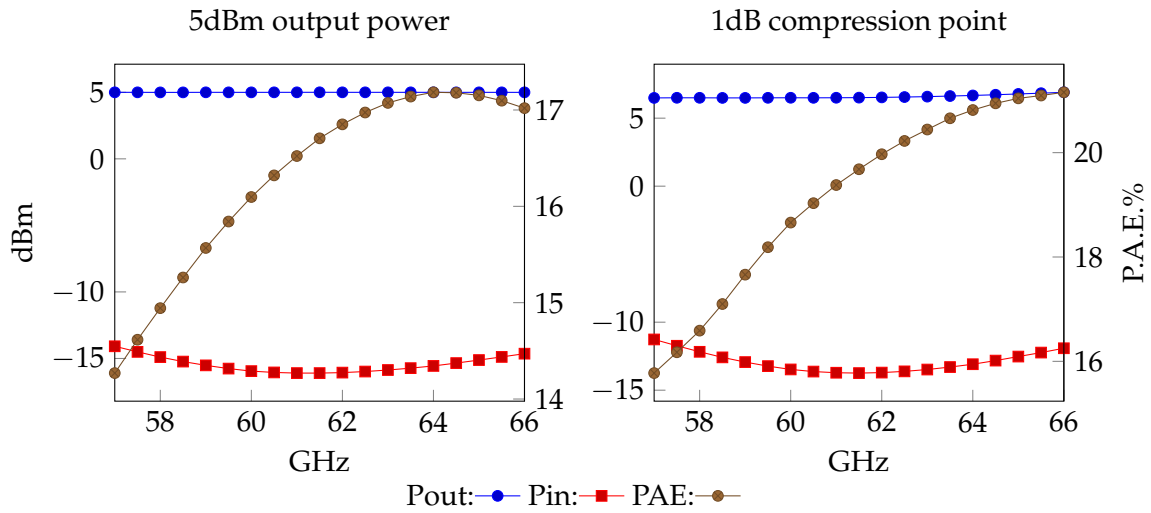


Figure 3.13: *In band performance shows the input power required and the efficiency of the PA.*

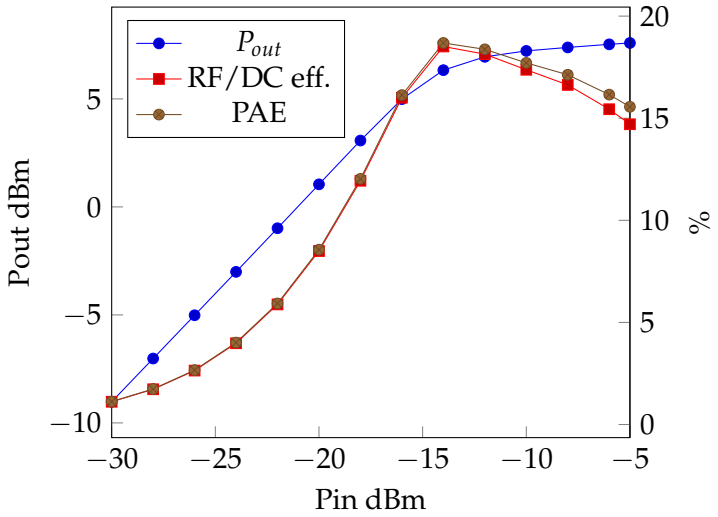


Figure 3.14: *Power and efficiency*

Power output was held to a constant level, or the 1 dB compression point, to make sure that the power level in the circuit was approximately the same for all the simulations. Avoiding a change in the nonlinear operating point of the circuit, was considered essential to get results that were useful for interpretation. The in-band performance (figure 3.13), shows that the efficiency is very dependent on the output power level. The efficiency has a local, broad maximum (figure 3.14), around -15 dBm input power, that is just below its 1 dB compression point. For the corner cases, only one parameter was varied at a time. Power gain in figure 3.17, reflections in figure 3.20 .

Figure 3.16 displays the tuning range of the circuit, by adjusting the VBias around the nominal 1.2 Volts. The gain can be increased or decreased. All the input powers under the -15 dBm line, are cases where the design has gain better than the specification $(-15-(+5)=20\,\mathrm{dB})$. For the slow HBT corner, the circuit can be tuned to get enough gain (figure 3.19). This demands a huge trade-off, in the form of reduced efficiency. A different approach would

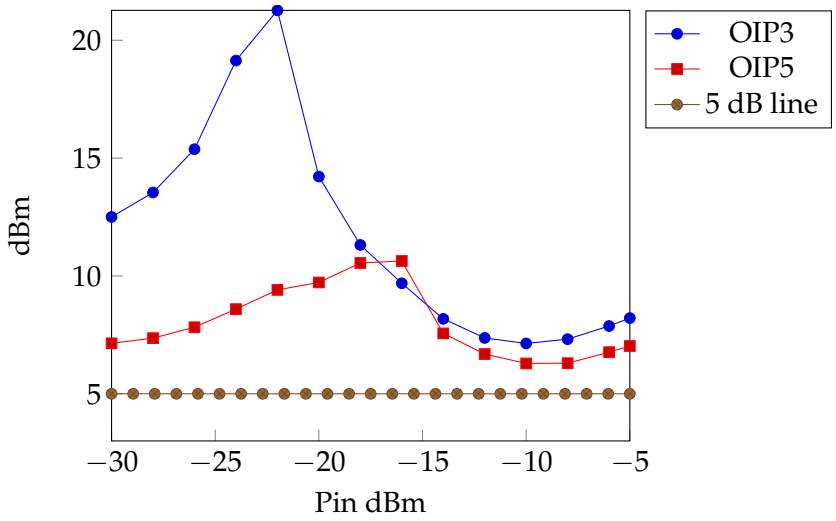


Figure 3.15: *Distortion Vs Pin. The peaking is attributed to the transistors internal emitter resistance by [46]. The OIP5 might be very inaccurate, as the model might not be accurate down to the 5th derivative (this is unknown).*

be to require a range of input powers from the feed circuit.

The steady-state transient response, is plotted in figure 3.22

3.2.3 Conclusion

The circuit has little coupling between the metal conductors. The extraction based EM simulation[2], gives the appearance that the circuit works as specified. If there was significant coupling, the simulations with larger distances (fig 3.12) would have larger error factors when compared.

The OIP3 is at 9 dBm for an input power of -15 dBm, therefore the distortion is manageable (fig 3.15). As the goal of this amplifier is efficiency, the distortion is designed to be quite high. It is an inherent trade-off between linearity and efficiency.

The gain is controllable within acceptable parameters, (fig 3.16) but needs to be taken into account when designing the preceding stage, in the transmitter chain. To have the total transmitter system always perform within specifications, more tuning range is required from elsewhere in the system. The graph successfully illustrates why it is absolutely required to be able to tune the bias supply, in an independent manner.

The DC power consumption is within limits (fig 3.18). In the fast corner, the power consumption is high, but still within specification.

The input reflections has quite high variations (fig. 3.20), but this is inevitable across the corners, given the goal of little complexity in the matching network. Variation is also high, as a consequence of no global feedback.

For a broader frequency range, the R, C, and HBT corners have been plotted (fig. 3.21).

[2]The extraction based EM simulation is documented in the AWRDE user manual

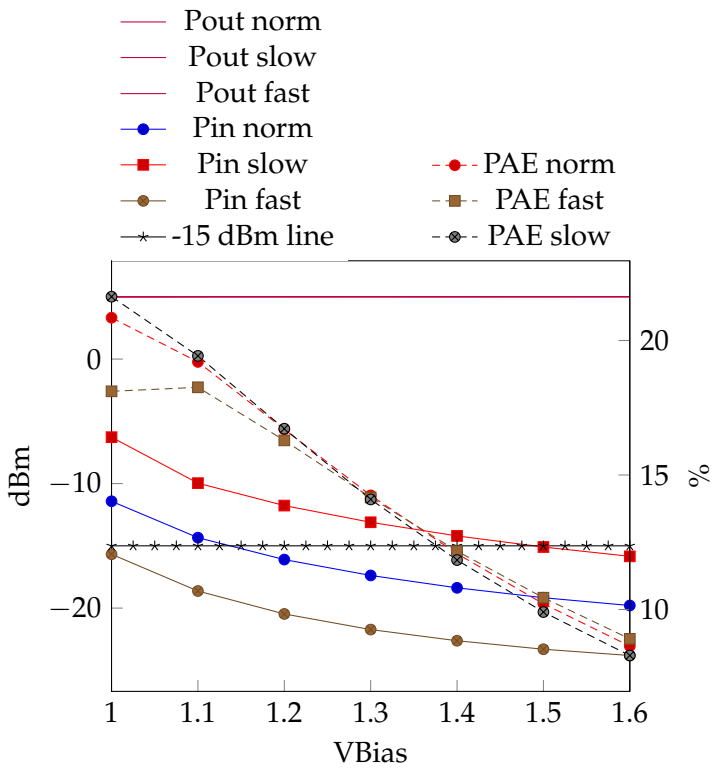


Figure 3.16: *Power and Efficiency, over VBias range with HBT corners, constant Pout=5dBm to demonstrate the tuning range of the PA circuit.*

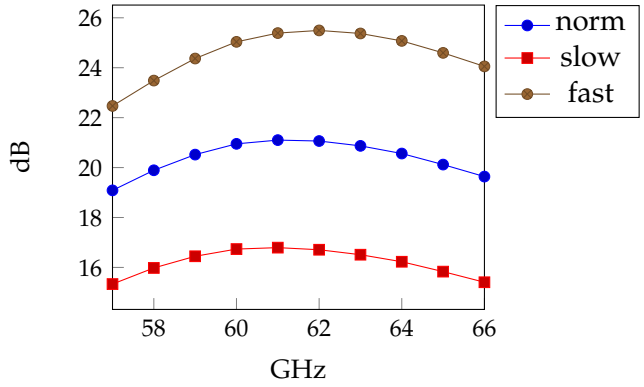


Figure 3.17: *Power Gain and HBT corners, showing a range of ±4 decibels*

The time-domain waveforms (fig 3.22) appears satisfactory. They look very much like sines, except for the highest power of -10dBm in, where the circuit clips quite much. This corresponds to the power transfer function in fig.3.14.

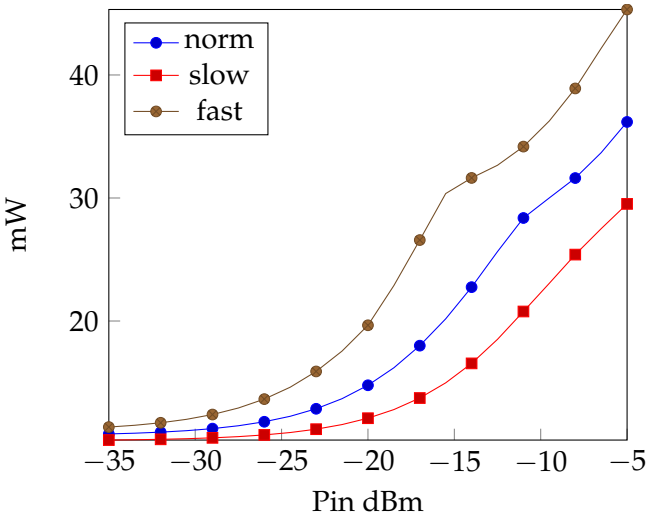


Figure 3.18: *DC power and corners vs input power*

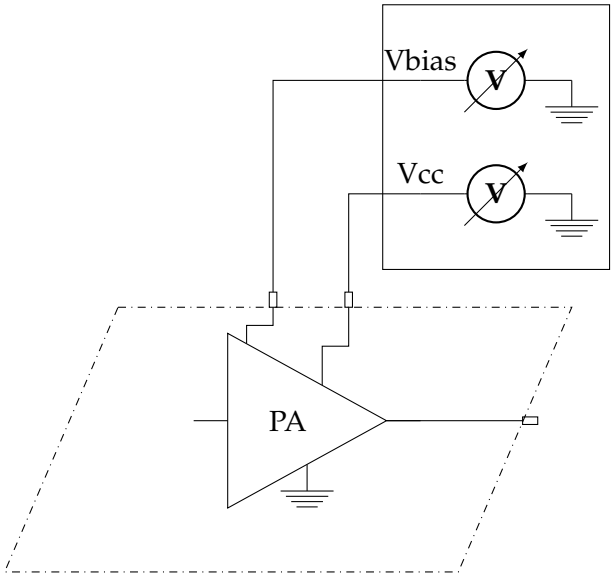


Figure 3.19: *Possible voltage supply tuning scheme for PA characterization and test*

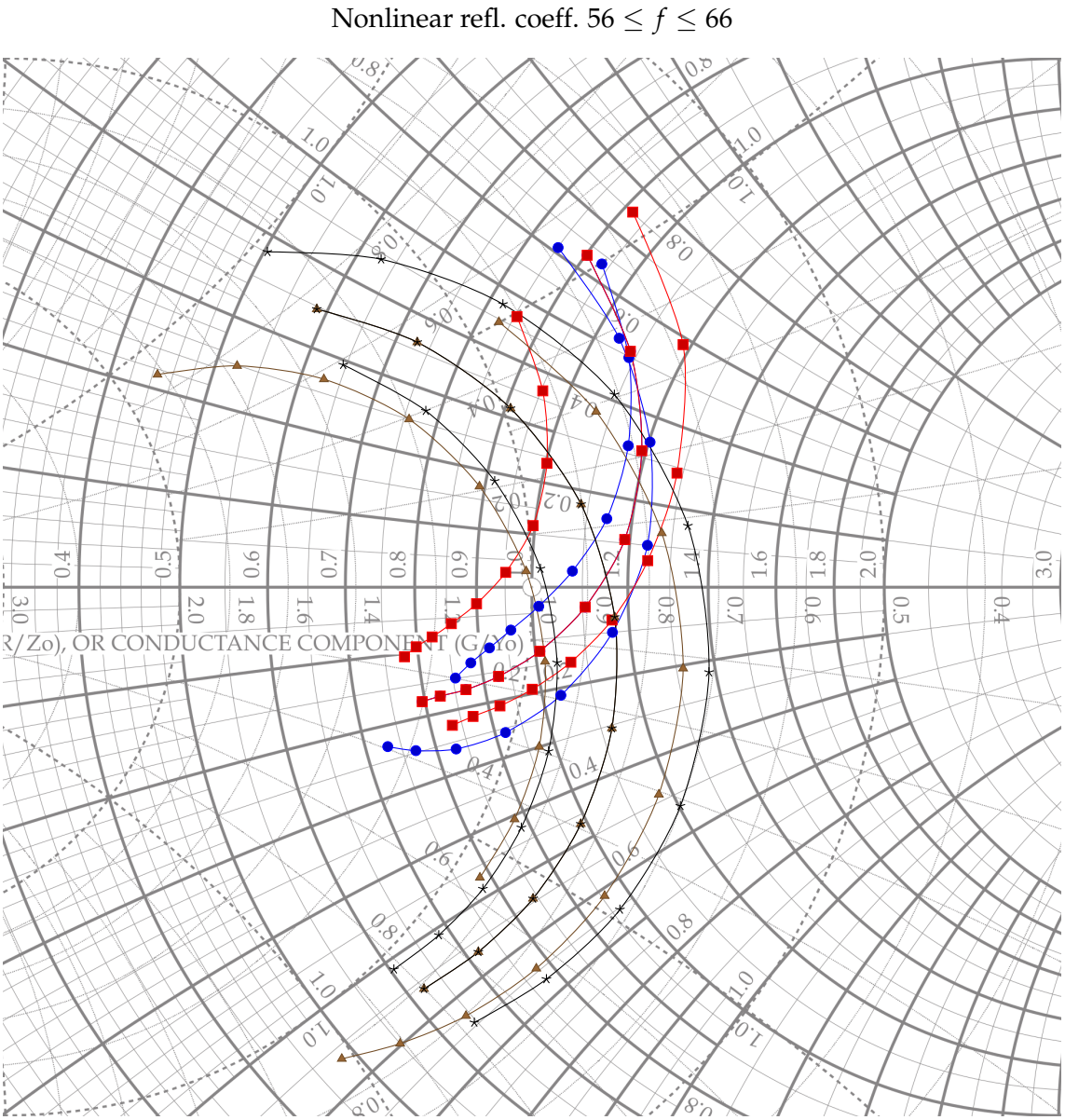


Figure 3.20: *Spread of reflection coefficients vs HBT and Capacitor corners (middle line is norm)*

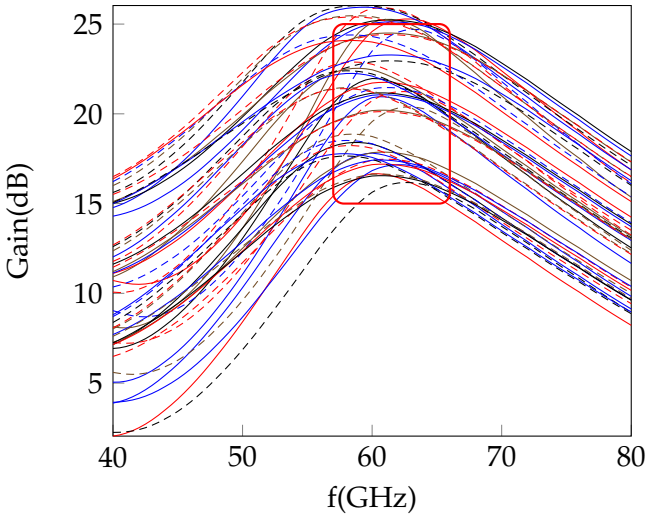


Figure 3.21: *Wide range gain, showing variations with R,C, T and HBT corners. Marked is 57-66*GHz*, 15-25*dB *gain*

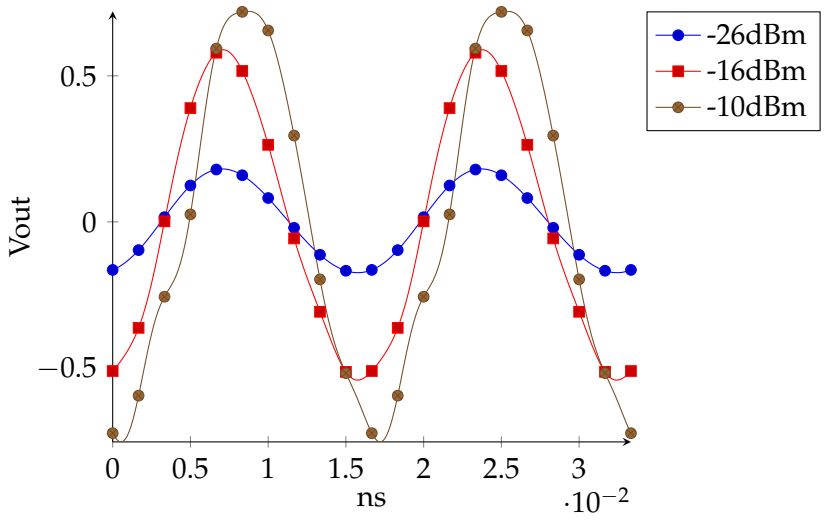


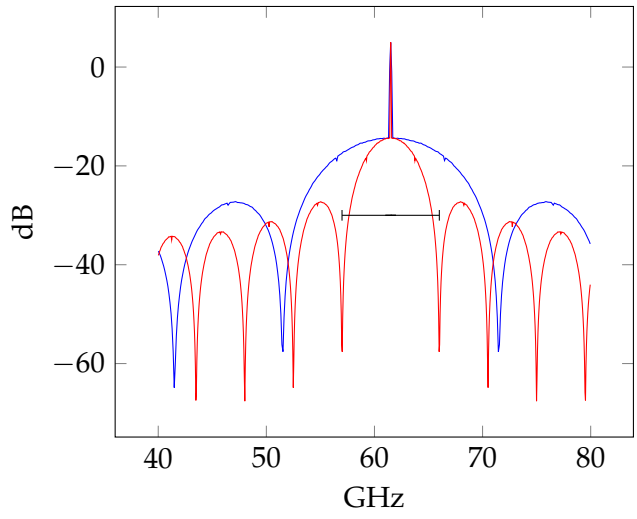
Figure 3.22: *Steady-state waveforms*

4 High Power OOK modulator design

OOK modulation is the binary amplitude modulation of a carrier signal. The information of the signal, is present in the upper and lower sideband. The efficiency of the modulation, in bits per Hz is 0.5 (1 if one includes only one sideband). An initial specification from earlier in the 60 GHz project, is 4.5 Gbps. For the wireless link, maximum bitrate and low power are important specifications, so a long term specification could become up to 10 Gbps in the future. The bandwidth limitation of 9 GHz in the European law, and the possible future design specification of 10 Gbps in a SISO system, with amplitude modulation are incompatible. But with high levels of vestigial sideband[1], approaching a spectral efficiency of 1 can be possible, but this needs more complex circuitry. A more spectral-efficient modulation type could also be chosen, at the cost of more power and complexity. Conversely, the OOK scheme is simple, and requires minimal power.

The modulator is designed to handle greater than 4.5 Gbps modulation, to have a solution that is robust enough to be compatible with mass-production. This above-spec performance, is so that the less-than-ideal process corners and operating points, will not render the circuit useless.

Figure 4.1: *FFT of OOK modulated signals,* $f_c = 61.5 \cdot 10^9$ Hz



10 Gbps *in blue, 4.5* Gbps *in red. Legal 57-66* GHz *limit marked. The 4.5* Gbps *signal is within the legal limit.*

[1] Vestigial sideband AM transmission was used for TV transmission, where the lower sideband was almost removed. This increased the data throughput of the wireless channel. Because the carrier was still present an envelope detector could still be used as an inexpensive demodulator.

Table 4.1: *Switched CE specifications table*

(a) Input to module

Input	Val.
Bitrate	0-10 Gbps
Digital signal	rail-to-rail
Carrier input power	-5 dBm
Carrier frequency	59-62 GHz

(b) Design variables

Output	Val.
Gain(on/off)	15 dB/-12 dB
Bandwidth	57-66 GHz
Power consumption	$\leq$50 mW
CW Power	5 dBm
V-supply	1.2 V

(c) Post simulation spec table

Output	Val.
Gain(on/off)	15 dB/-45 dB
Bandwidth	50-65 GHz
Power consumption	25-40 mW
For 4.5 Gbps	27.65 mW
CW Power	5 dBm
Input power std.dev	–
over corners	σ =4 dBm

Std deviation measured between HBT corners, for input power giving 5 dBm *output (assumed 3 sigma). Data in figure 4.14.*

4.1 Design

Requirements for the circuit are rapidly summarized: A 5 dBm power output of the carrier wave, with better than 17 dB SNR for the wanted BER $\left(10^{-12}\right)$of the system. Ideally the leakage is zero, or $-\infty$ dB, but this is never obtainable.

-12 dB was chosen as a maximum leakage signal, to have extra design headroom for the ratio of energy, from bit on vs off.

There is a trade-off in design, between high-speed and high isolation [47]. A high-isolation modulator topology is an amplifier (unilateral device), with its power modulated to achieve OOK. A high-speed modulator is of the distributed-switch architecture. A distributed switch built with bipolar transistors, has the disadvantage that one uses power when the transmitter is off. The design space, lies in between making a switch, to suppress and absorb all 60 GHz signal, or making the bias and power circuitry in an amplifier do the switching. It is then hypothesized, that for higher isolation, there is a direct trade-off in speed. Highest efficiency is achieved if all the currents in a PA, can be turned off when not transmitting, also reducing the maximum possible speed. A HBT, switches fastest when kept in the same mode of operation. So the Vbe and Vce should be set for forward active mode, all the time. The transistors should be biased for high transconductance, when the circuit is in the transmitting state, and for very low transconductance while not transmitting. If the transistor is allowed to go into cutoff mode, it is much too slow (10$\times$ the time of keeping it between two active states) to go back, into forward-active mode again.

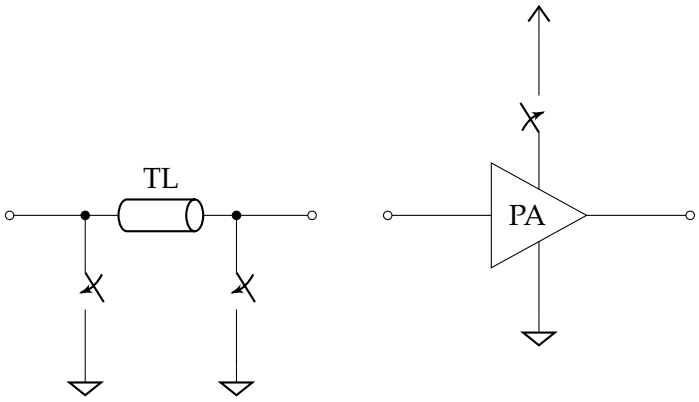


Figure 4.2: *Design space conceptual figures*

Isolation in measured results, is expected to be less than 46 dB. This is because the simulation shows 56 dB, and in [48], the simulation had 10 dB higher isolation than the measured result. The 46 dB figure, is then extrapolated from this. The reason for less isolation are coupling effects that are not simulated. The silicon substrate is tall, so signals can propagate through this. Isolation is not included in between components, or through the substrate (5 or 10 µm to metal and an additional µm to a thick conductive Epi layer).

Most types of modulators, are based around a mixer as a system element. From most sources ([11, 49, 50, 7]), whether CMOS or BiCMOS, mixers are balanced or quadrature. They are also large and relatively high-power ($\geq$ 100 mW). ASK modulators made in CMOS [47, 51, 52, 53], have the advantage of low (or zero) static power dissipation, at the cost of more expensive, modern CMOS processes like 40 nm. The 40 nm CMOS processes available at the time of writing, are simply too costly for the project.

Only two single-ended active OOK modulator topologies were found, [53] (CMOS) and [48] (BiCMOS). Apparently the design space of single ended modulators with bipolar transistors, is not widely explored. This might be because of the combined requirements of low Q inter-stage matching, low power consumption, high gain and switching speed. A design combining modulation and power amplification, was designed using HBTs for gain, and switching CMOS for data signal distribution. This will reduce the digital input power demands.

As the switched waveform (see figure 4.1) has a bandwidth so wide as it can be characterized as an ultra-wideband (UWB) signal, dispersion in the transmission line between the output and the chip periphery should be considered [33, ch. 12]. As we see in section A.4.1, making an artificial transmission line with balanced ratios of R/L and G/C, will reduce dispersion.

4.1.1 Evaluated architectures

Several configurations were evaluated in an attempt to find a good, simple, and power efficient modulator. If modulating with a mixer, a Gilbert cell would be required. The Gilbert cell requires lots of power, so is not an optimal solution. Another design choice could be differential switching circuits, then high-bandwidth, low-loss baluns would be needed.

The baluns are challenging to design, and several articles deal with the design of baluns themselves. With the lack of rapid prototyping of designs, using baluns should be avoided, because of the inherent difficulty in getting them right. It was then decided to try to make a single ended modulator. Some time later, the idea was suggested that modulating and power amplification functionality, could be integrated into a single circuit. This is seen in section 4.1.2.

An early attempt, was the common collector - common base configuration (CC-CB). This had the possibility of high isolation of a single stage, and relatively low interaction between the data, LO and output nodes.

The circuit was inspired from the amplifier in [54, ch. 7]. The CC-CB configuration was evaluated, requiring a very low impedance at the output, making for a more complex matching network. The impedance transformation made the inter-stage matching impractical, due to the many elements required for such a high impedance ratio. The area required (un-optimized), per amplifying transistor was $0.6\,\text{mm} \times 0.4\,\text{mm} = 0.24\,\text{mm}^2$ (versus the final of $0.4\,\text{mm} \times 0.1\,\text{mm} = 0.04\,\text{mm}^2$). Also, the topology is more suited to low-power signals (-10dBm and lower), as the transistors quickly saturates above -10 dBm in the CB configuration, of the output transistor. To get power up to $-5\,\text{dBm}$, the impedance at the RF node had to be $3 + j2.5\,\Omega$ (using power matching). The advantage to the CC-CB configuration, is that the circuit has a low-impedance node on the emitter of the transistors, same as differential circuits, making switching easily implementable, and very fast. This low impedance can be seen by the emitter connections, in parallel with the switched current mirror. This configuration is capable of modulating a low-power OOK signal, with 15 Gbps in a preliminary simulation, without much optimization (figure 4.3).

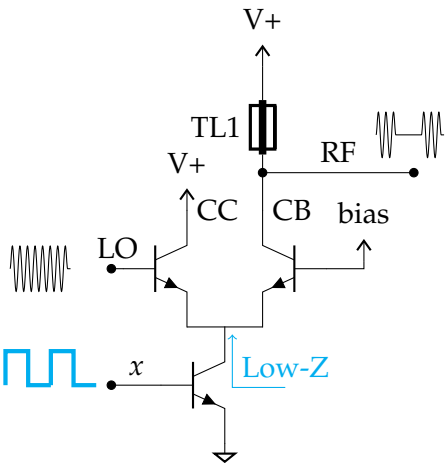


Figure 4.3: *CC-CB conceptual schematic*

A distributed switch architecture was simulated. This required lots of dynamic and static power, as well as having low isolation. It was thus found to be not suitable. In CMOS this design has been made for ASK applications, and it requires zero static power[47].

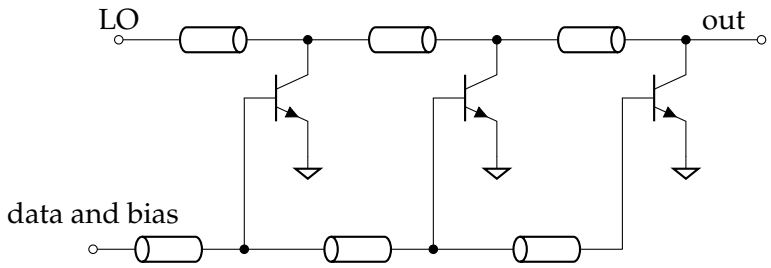


Figure 4.4: *Distributed npn switch*

A simplification of the CC-CB circuit, the common base (CB) amplifier topology was attempted to modify into a modulator (figure 4.5). Any literature on using the common base as a modulator in the 60 GHz band, was not found.

Using a CB configuration with the modulating 4.5 Gbps signal as a current-mode signal on the base of the transistor, had the same power-handling and matching impedance challenges, as the CC-CB, where very low impedance matching networks was needed. The base node of the CB is a very sensitive node, and matching networks were put on it. The base impedance in conjunction with the transistor gain, made the configuration a negative-impedance on-off modulated oscillator, instead of an on-off modulated amplifier. This topology was found to be not optimal.

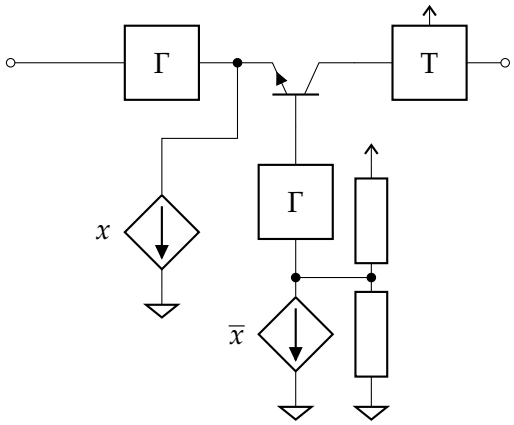


Figure 4.5: *Switched CB schematic*

The cascode (CE-CB) topology was modified for switching and evaluated (figure 4.6). The advantage to cascode circuits, is the high input-output isolation and high impedance output. While it has been shown, that cascode power amps with HBTs in the cascode configuration is a sensible architecture, the simulated switching characteristics with the wanted power levels, were unsatisfactory. Some avalanche effects, were seen in the simulation when biasing the cascode for switching (reverse gate bias current). See section 2.1.3 for safe operating area (SOA) considerations.

For this design, the cascode was unsatisfactory, but it has been proven many times to be a good power amplifier stage. For some perspective, in [55], a very modern balanced PA design with higher-voltage InP HBTs, is shown in a chip that uses more than 1W of power,

and clearly demonstrating the capabilities of cascode designs. ($\geq$ 20 dB S_{21} from 210-255GHz, 16 cells, 3 stages). The same source ([55]), also claims that the cascode stage offers the most output power per mm of chip area, for the InP process technology.

To summarize, cascode was satisfactory in gain and power consumption, but the attempted design where the base of both transistors was switched on and off, in conjunction with high carrier power levels, led to reverse conduction (avalanche) effects. This can either be attributed to the limited range of real measurements on the VBIC model supplied, or actual physical breakdown. Neither effect is good, or satisfactory for the performance of the design, so the cascode design was shelved.

It was later found a source that had successfully implemented this kind of topology (cascode) for *low power* OOK modulation ([48], see table 4.2)

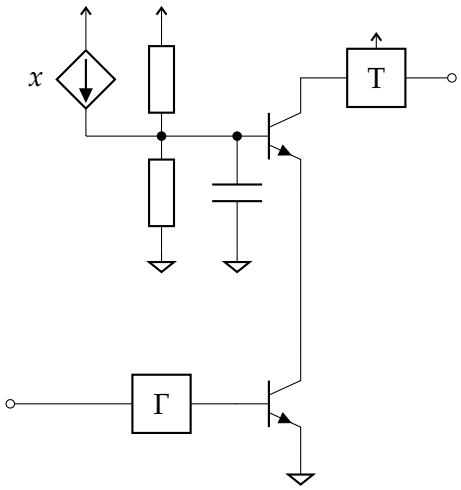


Figure 4.6: *Switched cascode schematic*

4.1.2 Multistage high-power modulator design

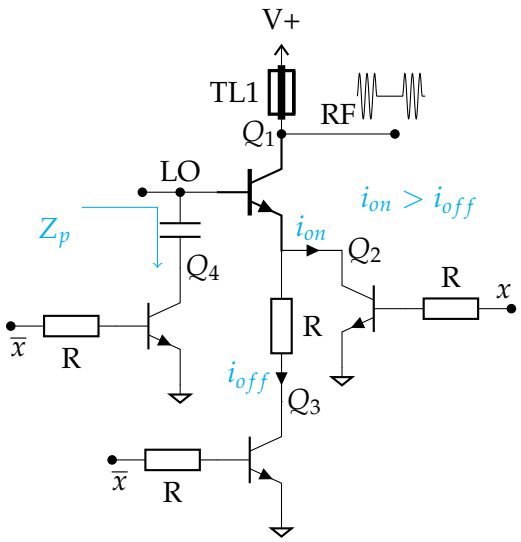


Figure 4.7: *switched CE gain stage*

The idea for this circuit came from the experimentation of the aforementioned CC-CB stage, and the resulting insight into the switching current properties of the HBT transistors. This combined with ideas from [53, (Lee)] for the single ended configuration, and the previous PA work from [3, (Schou)], coagulated into the design seen in this section.

The circuit has two states, one "off-state" where Q_1 is biased in the forward-active mode, but with very low transconductance (gm). In the circuits "on-state" the transistor is configured, with high collector current and low emitter resistance, for high gm.

A compromise was reached, where the emitter current of Q_1 is reduced to 0.4 mA in the off-state with 500 ohms series resistance (in addition to the resistance represented by the saturated switching transistor). In the on-state, minimum emitter resistance is required for high gm, thus the emitter is routed directly through the saturated Q_2. For high power capability the current is 8 mA. The on vs off currents were first selected, as the ratio of these directly controls the isolation and gain of the circuit.

The switching is done with transistors, controlled as switches by the data signal. Q_2 is fed by the baseband signal x, Q_3 and Q_4 fed by the signals complement $\overline{x}$. The resistor above Q_3 together with the bias voltage on Q_{1B} sets the off-state current and gm.

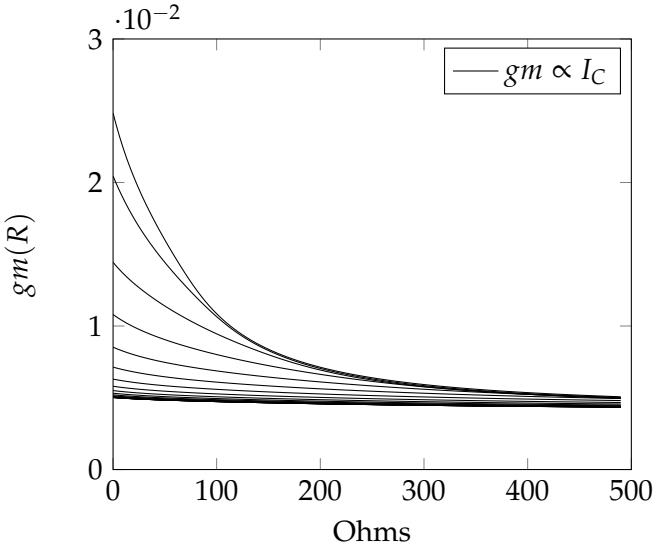


Figure 4.8: *Nonlinear simulated transconductance vs emitter resistance. Collector current (I_C) is swept. Greater current increases the gain at high transconductance because of less compression.*

Collector transmission lines are added to shunt higher harmonics, and to feed DC. For inter-stage matching networks, a shunt transmission line is inserted to match the impedance, from collector to base. There are also short degeneration transmission lines, on the emitters, for stability. All the transmission lines were attempted to be made as small as possible, as they have the highest area-cost in the circuit. Capacitors are used for DC blocking, and are scaled large enough, so that they have little effect in the network. Simulated with a

pseudo-random bit-sequence, the simulation gives an estimate of steady state (transmitting) power consumption, of the whole circuit in figure 4.9.

$$P\,(\mathrm{mW}) = \frac{\int_0^t I_{supply} \cdot V_{supply} dt}{t} \tag{4.1}$$

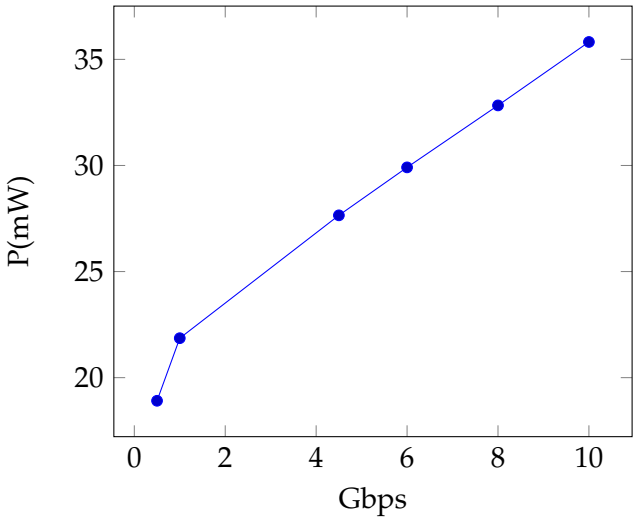


Figure 4.9: *Power vs Bitrate CE switched PA*
Total power vs bitrate. (see eq.4.1). Slope $\approx 2.9\,\mathrm{mW/Gbps}$

The power budget in the circuit, increases with bitrate and is mainly caused by the linear increase in dynamic switching currents.

4.2 Detailed walk-through of the circuit operation

4.2.1 PA gain stages

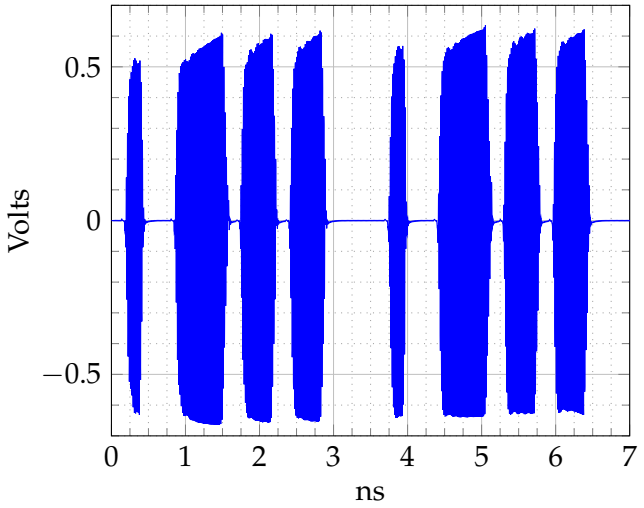
All the transistor stages amplifying the carrier, is 6x2 transistors. This is slightly different from the PA design in [3], where only the last transistor stage is that size. The Q_1 transistor is responsible for the gain of the circuit. Q_2 switches on with the data and $Q_3 - Q_4$ switches complementary to Q_2. The total collector current per stage, is kept between 8-9 mA in the on state, and 0.4 mA in the off-state. This keeps the transistor in the forward active mode (forward gummel - poon in the model), at all times. The final gain stage gets a high collector-emitter voltage, close to the supply voltage. This is the dynamic range limit of the circuit, so to increase power, a different stage is needed. The stages are matched with the power match method, instead of the complex conjugate, because it is inherently a large-signal circuit. This makes for some reflections (fig. 4.12).

4.2.2 Base impedance

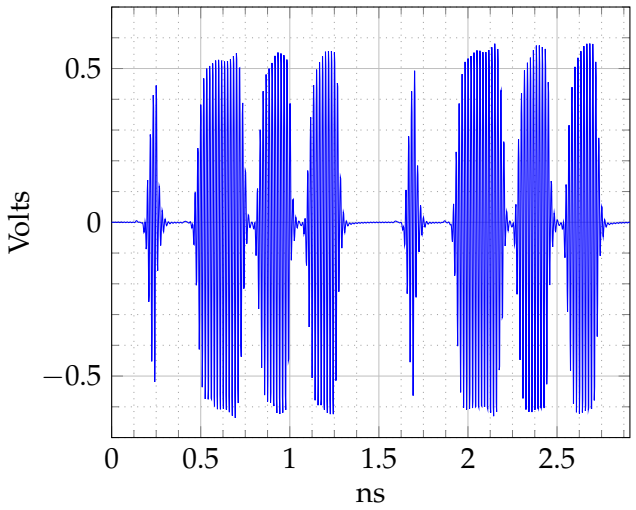
The base impedance is switched between low and high, ideally an RF short, when muting the output. Z_p is high when the data is high, and low otherwise. The input impedance of the gain stage is $Z_p || Z_{B_{Q_1}}$, so it varies with the data signal, and also gives a higher Γ, when the circuit is in the off-state (see fig. 4.12). This increases isolation.

Figure 4.10: *Time domain waveforms. Startup effects reduce the peak of the first bit. Output transistor is strongly saturated, so the negative swing is larger.*

(a) 4.5 Gbps



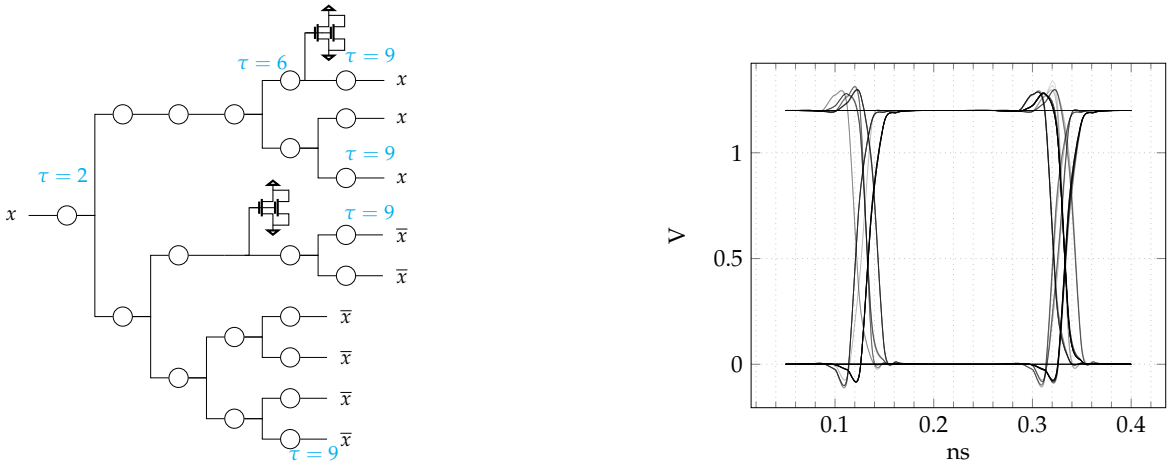
(b) 11 Gbps



4.2.3 Emitter switching

The emitter current needs to be kept on, for the transistor to stay in the same region. As mentioned in section 2.1.3, the transistor slows down when turned completely off. For this reason, the emitter current is routed through a hard-on transistor (Q_2), acting somewhat as a short when the circuit is on. The current is routed through a 500 ohm resistor, followed by transistor Q_3 when the circuit is off. This reduces the amplifier transistors collectors current, thereby saving power, making the gain go below a factor of 1, thereby turning the circuit into an attenuator. The rise time of the switching circuit control signals, is critical for the bit sequences LHL and HLH, where the bit-length is shortest. Ideally, the positive and negative switching, happens at the same time. If the signals do not switch at the same time, the bit-length on the modulated signal is reduced, as the circuit will be in an intermediate state

Figure 4.11: *Balanced τ 2-fanout switching signal distribution tree and eye diagram*



For the eye diagram at 5 Gbps, *the eye diagram transition width (*$\leq$ 40 ps*) divided by individual risetime (*$\sim$ 30 ps*) is in excess of* 33 %. *The individual risetime limits an ideal tree structure to* $\frac{1}{\sim 30\,\mathrm{ps}\cdot 2} = 16\,\mathrm{Gbps}$, *while the realistic maximum of the circuit is near* 10 Gbps. *This is the limit in this process, because of slow CMOS, compared to the HBT devices.*

of operation, when the complementary signals are the same voltage. For the distribution tree sketched in fig.4.11, the circles represents inverters. The minimum 2-branch tree size, to give 9 outputs is 5:

$$N_{min-branches} = \lceil \log_2(9) + 1 \rceil = 5 = N_{mb}$$

And the minimum amount of inverters, is 24 for a purely symmetric tree:

$$N_{min-inverters} = 2^{N_{mb}-1} - 1 + N_{outputs} = 2^4 - 1 + 9 = 24$$

The tree in fig. 4.11 is not symmetrical (*not* every node before the leaves has a branch), so it has less inverters (21). The branches has 5 or 6 levels.

The inverters are all the same size, so a fan-out doubles the driving capacitance of the inverter, effectively doubling the propagation delay[2].

4.2.4 CMOS baseband distribution and inverter scale

The baseband signal (x) is the digital signal, from outside the chip. To isolate the baseband from the RF signal, and to have realistic driver requirements for the baseband input; a distribution network is needed. If not, much power would be required from the signal generator outside the chip (in the vicinity of 10 dBm continuous power). With the inverter tree, the driver requirement is lower ($3-4$ dBm in the switching peaks, "zero" the remaining time). The exact power required, is highly dependent on the rise time of the signal. This is obvious because the signal is driving an inverter, so power is only required while switching. The network also has the advantage that the switching waveform will have fast transitions, independent of the source signal risetime.

[2]Delay behavior is estimated using a 1st order RC model, elaborated in[56, ch. 4] ignoring the effects of wires and velocity saturation

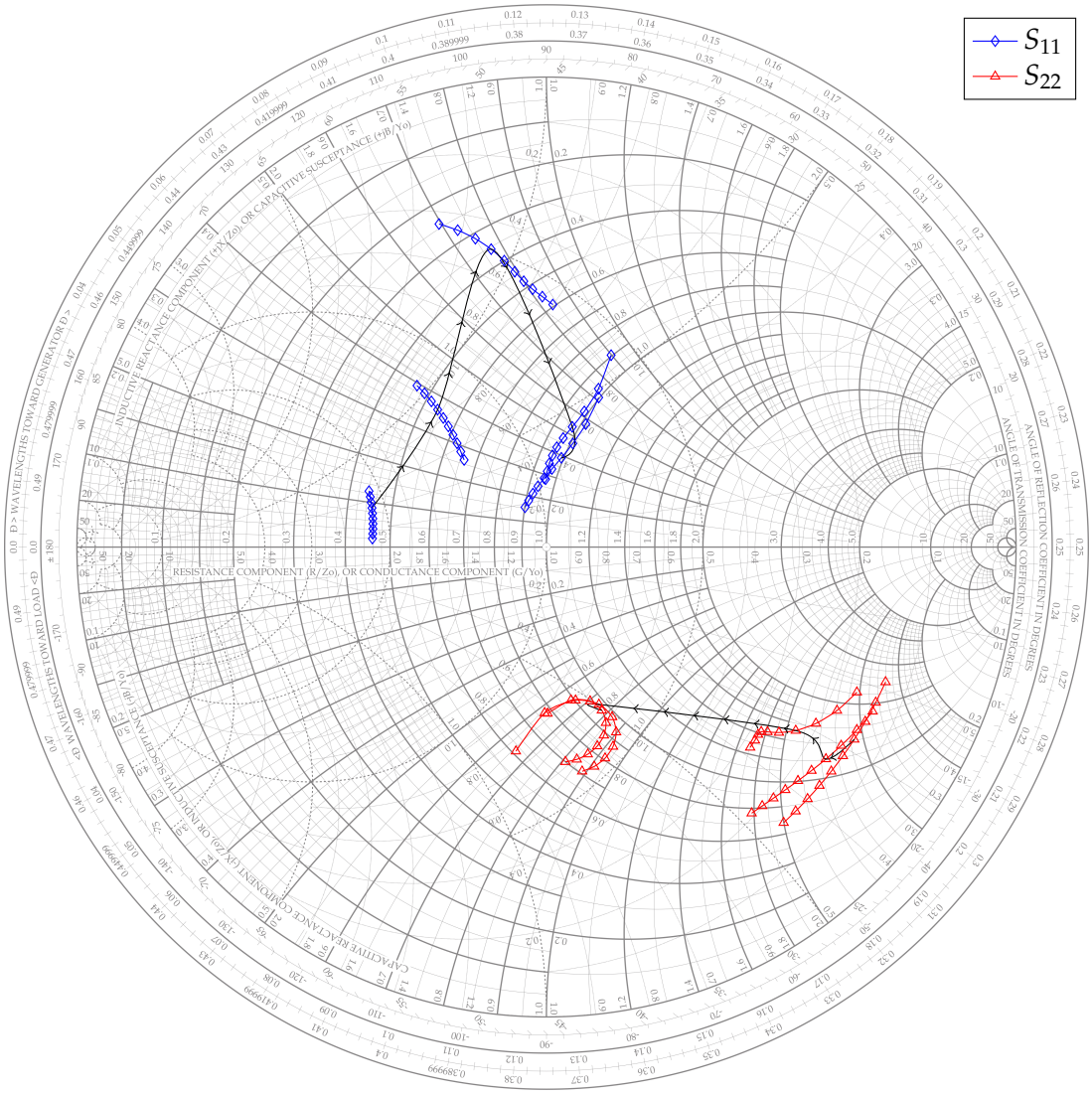


Figure 4.12: *Static approximations to dynamic reflection behavior of the circuit. Scattering parameters measured with the switching voltage held static at 5 points between 0 and 1.2* Volts*. This plot is a static approximation to the* Γ *of the circuit when switching, during the ~40* pS *duration, or almost 3 cycles of the 60* GHz *signal. Estimated uncertainty for the intermediate points is ~20% Locus of the reflection coefficients at 60* GHz *over the voltage span traced with* $\rightarrow\rightarrow\rightarrow\rightarrow$*, from low to high voltage.*

CMOS inverters are scaled to the size where they can drive a fan-out of 2, within any operating parameters. It is also scaled to be able to drive 500 ohm with fast rise-times. They are slightly over-sized, so that they will work as useful system blocks. They could be scaled down for an increase in efficiency.

4.2.5 Component sensitivity

The gain-stage transistors are the most sensitive components. Any other components, need much larger changes than the realistic process variation, to have comparable impact. The

design has high signal levels. This achieves output power stability, at the cost of some distortion.

The isolation variation in relation to the resistor above Q_3 is negligible. This resistor can vary much (fig. 4.8), and gives little effect, because of the small current passing through it. The per-stage isolation, is generally ruled by the transistor Q_1, in the low-current state.

Variation of biasing resistors showed insensitivity to gain, but sensitivity to power consumption. The power consumption varies with the resistors, so the on-mode power variance from device to device, could be 10%.

The bias voltage feed, is made so that there is more than 100 dB loss between 50 and 110 GHz, from one bias node to another. This is made possible by the combination of decoupling capacitors, the resistors, and the meandering bias path.

The Digital supply voltage feed, is on the south side of the circuit. The Analog V_{cc} supply, is on the north side. This attempts to reduce cross-talk between the digital and analog supply.

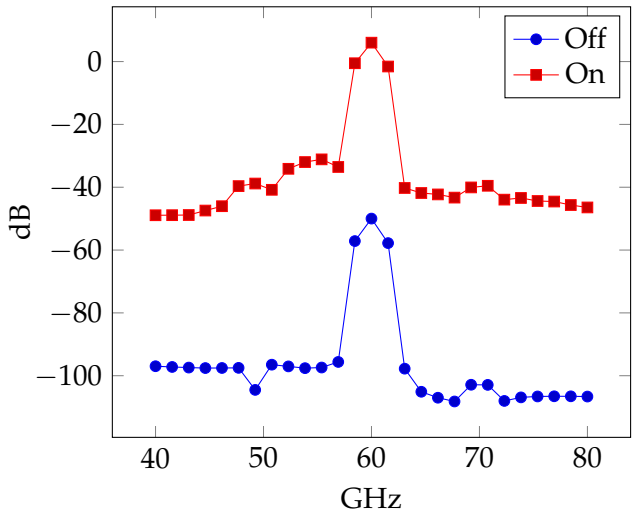


Figure 4.13: *on vs off fft from transient simulation showing a better-than expected isolation (56dB (P_{off} / P_{on})) (Hamming windowed 0.65 nS period with 100 harmonics and 7x oversampling)*

4.2.6 Efficiency

The PAE in figure 4.14, is not directly interpretable to the entire performance of the modulator, seeing as the off time for a stochastic bit sequence is 50%,. i.e., the actual efficiency is different depending on measurement conditions. This is because the modulator switches into a low-power state, when muting the signal. The reason the efficiency difference is not very large, is that the CMOS switching network requires much power, increasing the peak current usage, and average power. Optimizing the CMOS network for minimum power consumption can be done, and there is also a possibility to gain a few more percentage points in efficiency, without destroying the output signal envelope. The risk involved in minimizing the CMOS size, is that their performance may drop to unacceptable levels and reduce yield, in addition to changing the output envelope. Another compromise was found, where optimizing the power staging would require more area to the matching networks, when reducing emitter

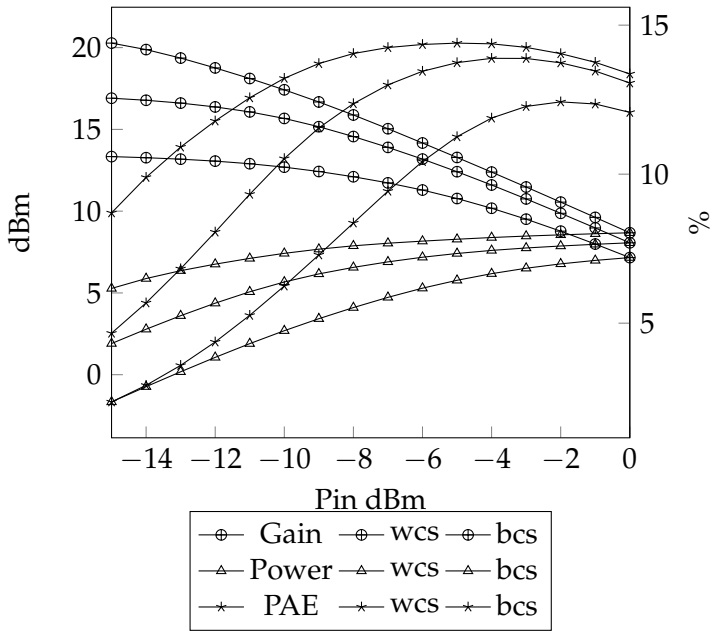


Figure 4.14: *Corners for on-state performance.*

count on the transistors. This caused an increase in area cost, and the number of transistors in the gain stages were kept the same. So; increasing PAE costs area, and keeping area cost down is preferential.

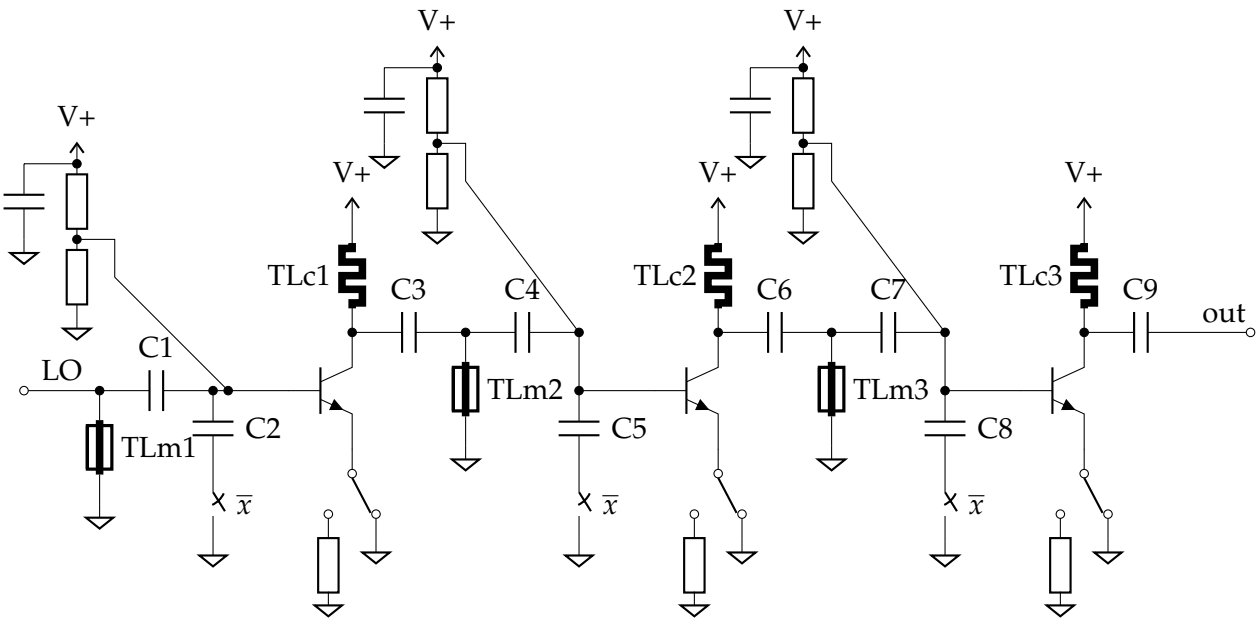


Figure 4.15: *Full switching CE schematic*

The resulting layout is $330 \times 312\,\mu m$ for an area of $0.1\,mm^2$ see figure 4.16 and 4.17.

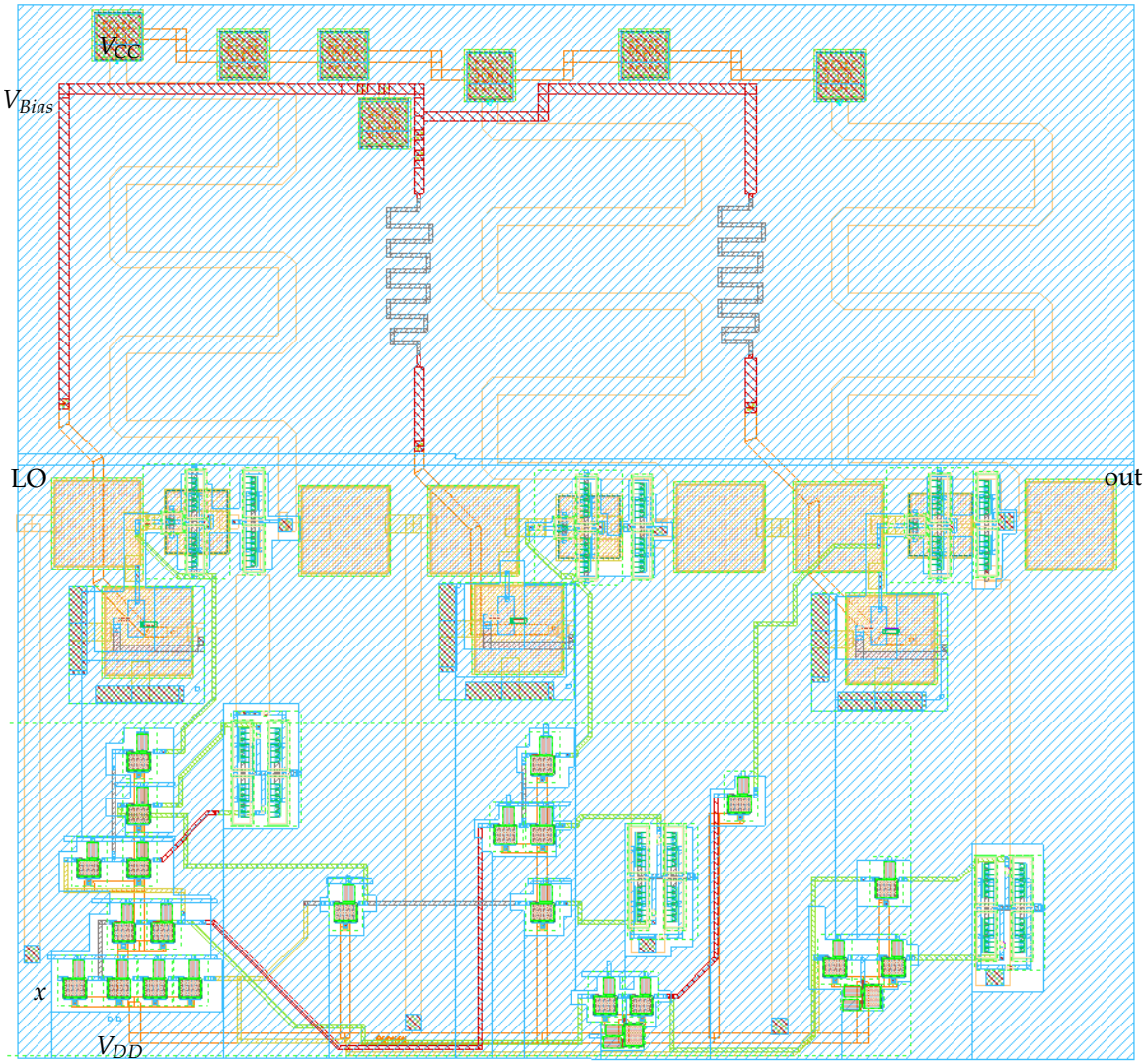


Figure 4.16: *2D drawing of the modulator layout*

4.3 Future work

Slope control could be added to the inverters, to try to reduce the spectrum, produced by the fast switching of the carrier. The CMOS inverter network can be scaled to reduce dynamic power consumption, for even lower power cost.

We have not decided the feeding source of the digital signal (x) into the chip. We have therefore assumed that there is available a rail-to-rail signal source. This could be a BiCMOS LVDS receiver, or something as simple, as a differential BiCMOS amplifier connected to a HI-skew inverter.

The emitter degeneration lines, can probably be optimized for higher gain. They can also be made a little bit shorter. An uncertainty to their length, is made by the rest of the required interconnect. This added length, can then be compensated with some shortening of the affected lines.

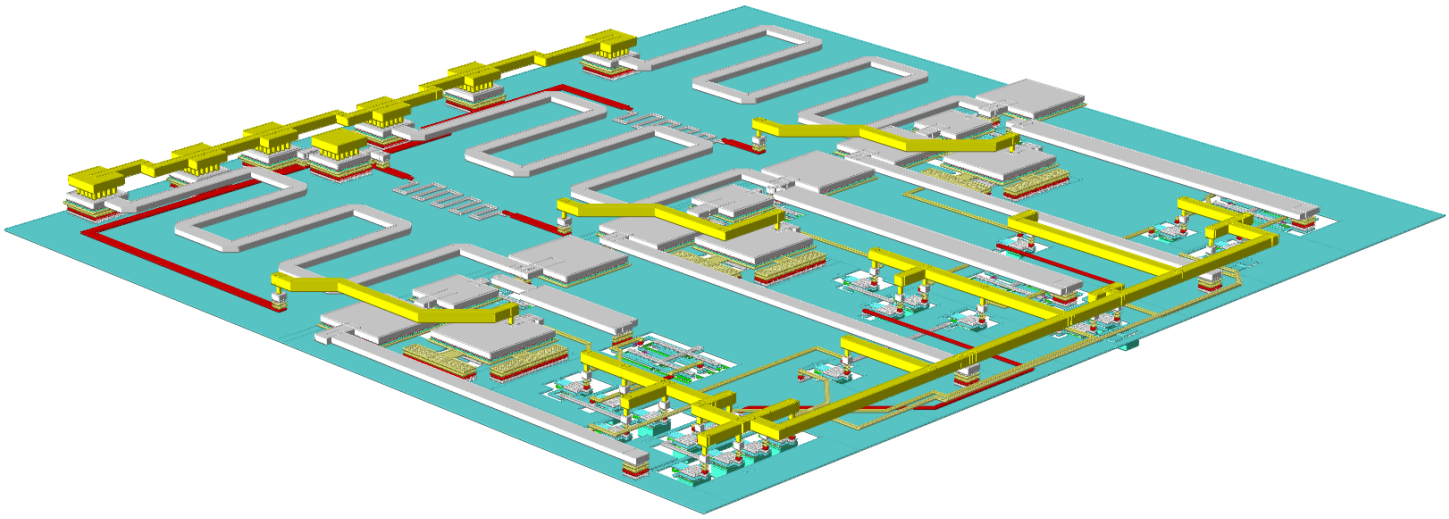


Figure 4.17: *3D modulator layout*

For EM simulation, the meandering lines and the bias network, has been simulated. This is sufficient to ensure that the circuit is working, but still leaves some uncertainty to the gain and isolation.

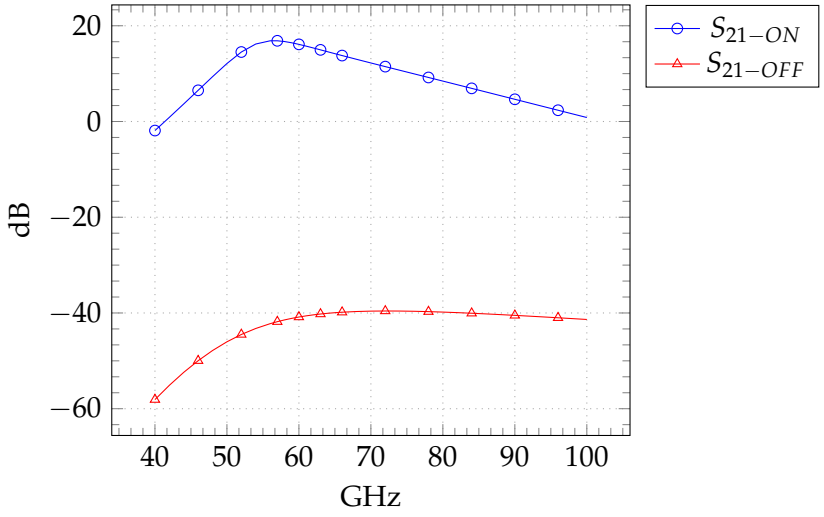


Figure 4.18: *Through S_{21} for on and off state*

4.4 Conclusion

Instead of a simple modulator, a combined modulator and power amplifier, has been designed. The simulated results are promising, and show that power is saved, by integrating the modulation function into the power-amp.

Power consumption is low, and can be optimized further. The CMOS inverters size, can be reduced for lower switching power, and they may also be scaled. This was not done in this design, as it already had acceptable performance.

This layout is quite small. The trade-off between area and other performance variables, like gain and matching, is discussed earlier. Therefore, in this layout, the total area is the most weighted variable.

The maximum modulation speed is reasonably fast, since it can modulate at 11 Gbps. Although this exceeds the 9 GHz bandwidth limit, having this speed available, exceeding the specifications, adds safety margins to the design.

A non-exhaustive simulation has been made. Power consumption varies as expected, together with corners, because of the non-compensated bias networks.

This circuit is possibly novel, as it has not yet been seen in other published works.

Table 4.2: *Comparison table*

ref	Technology	Freq(GHz)	Gbps	Isolation(dB)	mW	Pout(dBm)
[57]	0.25µm SiGe	60	20	36	54.6	$-18^{\oplus}$
[53]	90nm CMOS	60	2	28.4	14.4	$-14^{\oplus}$
[58]	90nm CMOS	60	3.3	–	≤ 100	$0^{\oplus}$
[48]	0.18µm BiCMOS	60	2.5	48	8.1	$-14^{\oplus}$
This work	0.13µm SiGe	60	11	56*	40	5.4

* : *The very high isolation is not real. It is so high because the substrate coupling and some parasitics has not been modeled.*

$^{\oplus}$: *Graphically estimated, measured on highest stated bitrate*

5 Discussion

Between 80 % and 90 % of the supplied power gets converted into heat. No simulations testing for thermal long-term stability has been made, but because of the low density of transistors in the circuit (low thermal source density), the thermal energy is assumed to convect out through the substrate, package and into the mounting PCB. From a thermal perspective, the circuit is assumed stable.

All the simulated nonlinear models assumes a well-grounded substrate. In the designs, there are no contacts explicitly connecting the substrate and the M1 return layer. These contacts may be added at the grounding pins of the chip, or placed in a designed manner to reduce stray currents. For this work, because of time limitations, a formal circuit and layout review has not been performed. This should be done at a later time, when the circuits are being prepared for manufacture.

The LNA circuit is performing as expected after modifications. It is stable and has a low noise figure, compared to other 60 GHz LNAs [4]. The new rectangular inductor was made with a defected ground structure (DGS), as this increases the performance of the inductor. The increased impedance and height from the substrate makes the inductor more susceptible to radiative losses, but this would have been seen in the simulations if that was the case.

The PA circuit had less modifications, as the meander lines were more spaced apart, the EM simulated response was close to the model. Not all the discontinuities in the signal path have been modeled, but this will have little impact, as the discontinuities are electrically small. The corners suggest that for better gain stability, more complex bias networks are required.

The Modulators input reflection (fig. 4.12), while switching, gets a higher Q-value than the on- or off-states for the circuit. This makes the matching network store some power while switching, causing different reflections or standing waves when switching. Ideally the Q value should be constant, but this is traded for simplicity of the circuit. The perforations in the ground plane (M1), made by the inverters may have some effects on the circuits behavior. Measuring and quantifying its impact is difficult because it is heavily dependent on the simulation port placements, i.e. it is difficult to know if the difference is from EM simulator setup, or physical effects.

The output stage of the modulator is operated in its full dynamic range. This shows that if higher than 5 dBm output power is wanted, a larger transistor, or a differential stage, is needed.

Interconnect of the chip between the components, is ideally a 50 Ohm line. There will also be associated some loss with the interconnect and reflections between the stages will travel on it. It is important that this interconnect is simulated, and not just assumed perfect. It may have dispersion that affects the signal, or too much loss.

In the ideal case, to gain confidence in the design tools and knowledge about the process, there should be done measurements on test structures on a fabricated IC. To reduce the cost

of these kinds of tests, test structures could be integrated on the chip, in areas where there is space. There is a required aspect ratio of the chip, and the circuits made are rectangular in shape, so it follows that the circuits cannot fill the entire area perfectly. This leaves some possible space for test structures. There has not been focus on a test strategy for the circuits. This could be couplers connected to envelope detectors, to get low-frequency test signals out of the chip without the need of expensive test equipment. The design and selection of test structures is important, but out of scope for this thesis.

6 Conclusion

Verification and tuning work has been done on the PA and LNA. The circuits were verified because it was indicated in the future work sections of the previous theses that some additional simulations should be done. This showed that after some modifications, both circuits was found to be operating within their specifications. The LNA has 20 dB of gain and a NF of 4.5 dB. The PA has 20 dB of gain and $\geq 15\,\%$ PAE. This work also includes the design of a high-power OOK modulator. This modulator can replace two components in a transmitter, the PA and modulator. This reduces area cost, and power costs, as there is used fewer transistor stages for the same functionality. The simulated modulator has 5 dBm output power, maximum bitrate of 11 Gbps and $\geq 50\,\text{dB}$ CNR.

Glossary and Abbreviations

AGC Automatic Gain Compensation

ALICE A Large Ion Collider Experiment (at CERN)

Analyst Analyst™ is the 3D Finite Element electromagnetic simulator used in AWRDE™

Anisotropy Something that has different properties in different directions. Like a paper that tears only in one direction, or the magnetic properties of a ferrite.

ASK Amplitude shift keying

ATLAS A Toroidal LHC ApparatuS (at CERN)

AWRDE Applied Wave Reasearch Design Environment (owned by NI)

AXIEM AXIEM™ is the planar full-wave electromagnetic simulator used in AWRDE™

Balun portmanteau of balanced to unbalanced. A component to convert from a single ended signal to a balanced signal.

MS Microstrip (line)

OOK On Off Keying (modulation)

BJT Bipolar junction transistor

BPSK Binary phase shift keying

CEM Computational Electromagnetics

CERN Organisation européenne pour la recherche nucléaire, previously Conseil Européen pour la Recherche Nucléaire

Chipset A set of integrated circuits designed to perform a specific function

CW Carrier wave

DGS Defected ground structure, used for minimization of geometric features

FSK Frequency shift keying

HBT Heterojunction Bipolar transistor

IQ In-phase / Quadrature

LHC Large Hadron Collider

LHCC LHC Experiments Committee

LNA Low Noise Amplifier

MIMO Multiple input Multiple output

MMIC Monolithic Microwave Integrated Circuit

Moding (unwanted) resonances or spurious behavior appearing in high frequency circuits

MoM Method of Moments used in computational electromagnetics

MWO Microwave office (AWRDE)

NI National Instruments Corp.

Nulling null : Description of an area where the measured response (e.g. attenuation or reflection) goes very low (e.g -40 dB). A response is nulled when a swept signal is severly attenuated.

OFDM Orthogonal frequency division multiplexing

OSI Open Systems Interconnection model (OSI model)

PA Power Amplifier

Pareto Pareto frontier is a state of allocation of resources from which it is impossible to reallocate so as to make any one individual or preference criterion better off without making at least one individual or preference criterion worse off. -wikipedia

PCB Printed Circuit Board (not polychlorinated biphenyl)

PSD Power Spectral Density

QAM Quadrature Amplitude Modulation

Slit or Slot modes Resonances appearing because of slits or slots (apertures) in a conductive or dielectric structure

SSB Single Sideband (modulation or spectrum)

TEM Transverse Electro-Magnetic, meaning no propagation of fields in the Z direction. Has zero cut-off frequency.

Transceiver TRANSmitter and reCEIVER

UWB Ultra Wide Band. Usually a signal with a spectral content larger than 1 GHz. Occasionaly used as a pulse-based modulation type for short-range communications

VBIC Vertical Bipolar Inter-Company model

WADAPT Wireless Allowing Data And Power Transmission

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Appendix A

Electromagnetic field theory

In microwave engineering, Maxwells equations are the fundamentals of the field. Following, a small elaboration on them is included, so that one might understand a microwave circuit in terms of the physics that define it. Hopefully, this gives better understanding of work done with computer tools and models, so that result obtained with them can be interpreted clearly.

The classical electromagnetic phenomena are described by Maxwells equations, here written in the standard vector notation format introduced by Oliver Heaviside:

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{A.1}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \tag{A.2}$$

$$\nabla \cdot \mathbf{D} = \rho \tag{A.3}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{A.4}$$

Where **E** and **H** are the electric and magnetic field intensities, units: $[\mathrm{V/m}]\mathrm{and}[\mathrm{A/m}]$. **D** and **B** are the electric and magnetic flux densities, units: $\left[\mathrm{C/m^2}\right]\mathrm{and}\left[\mathrm{Wb/m^2}\right]\mathrm{or}[\mathrm{T}]$. ρ and **J** are the volume charge density and the electric current density, units: $\left[\mathrm{C/m^3}\right]$ and $\left[\mathrm{A/m^2}\right]$. They are the sources in the equations.

In space outside of sources, the terms for the sources are zero ($\nabla \cdot \mathbf{D} = 0$, $\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t}$) . The set of differential equations can be solved for any classical electromagnetism problem, and then gives a very accurate representation of reality. The limits of validity are down on the quantum level, magnetic monopoles, and, the photoelectric effect[31]. Generally loss can be described as:

$$\frac{dP_{loss}}{dV} = \mathbf{J} \cdot \mathbf{E}\,(\text{ohmic power loss per volume})$$

and this equation shows the general expression for dissipation.

Amperes law:

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{J} \tag{A.5}$$

Equation A.1 rewritten in the integral form is the Maxwell-Faraday equation:

$$\oint_{\partial\Sigma} \mathbf{E} \cdot d\mathbf{l} = -\int_{\Sigma} \frac{\partial \mathbf{B}}{\partial t} \cdot d\mathbf{A} \tag{A.6}$$

where Σ is a surface bounded by the contour $\partial\Sigma$, $\mathbf{l}$ is the vector element of $\partial\Sigma$, $\mathbf{A}$ is the vector element of Σ.

Stoke's theorem:

$$\int_S \mathbf{B} \cdot d\mathbf{S} = \oint_C (\nabla \times \mathbf{B}) \cdot dl \tag{A.7}$$

Gauss' theorem:

$$\oint_S \mathbf{D} \cdot d\mathbf{S} = q \tag{A.8}$$

(electric flux on a surface surrounding a source is the same as the total charge of the source)

Poisson's equation:

$$\rho = \epsilon \nabla \cdot \mathbf{E} = -\epsilon \nabla^2 \phi \tag{A.9}$$

(ρ is the surface charge density, ϕ the electric potential)

For homogeneous and isotropic materials the relations of $\mathbf{D}$ and $\mathbf{B}$ to $\mathbf{E}$ and $\mathbf{H}$ are

$$\mathbf{D} = \epsilon \mathbf{E}$$
$$\mathbf{B} = \mu \mathbf{H}$$

With $\epsilon = \epsilon_0$ and $\mu = \mu_0$ in vacuum. where

$$\epsilon_0 = 8,854 \cdot 10^{-12}\,\text{Farad/m}$$
$$\mu_0 = 4\pi \cdot 10^{-7}\,\text{Henry/m}$$

and

$$c = \frac{1}{\sqrt{\mu\epsilon}},\ \eta = \sqrt{\frac{\mu}{\epsilon}} \tag{A.10}$$

shows the speed of light and the characteristic impedance of vacuum or a material [59].

$$c_0 = \frac{1}{\sqrt{\epsilon_0 \mu_0}} = 299792458 = 3 \cdot 10^{8\,\text{m}/\text{sec}}$$
$$\eta_0 = \sqrt{\frac{\mu_0}{\epsilon_0}} = 376,730313461 \approx 377\Omega$$

For a material, the permittivity ϵ and permeability μ, also known as the dielectric constant and magnetic constant (in vacuum). The dielectric constant is really a complex number,

$$\epsilon = \epsilon' - j\epsilon'' \tag{A.11}$$

, and the relative permittivity of a material is:

$$\epsilon_R = \frac{\epsilon'}{\epsilon_0}$$

The loss tangent of a dielectric (often very small) is

$$\tan\delta = \frac{\epsilon''}{\epsilon'}$$

μ_0 is defined by amperes law.

The dielectric and magnetic properties of a material are:

$$\begin{aligned}\epsilon &= \epsilon_0 (1+\chi) \\ \mu &= \mu_0 (1+\chi_m)\end{aligned}$$

where χ and χ_m are the electric and magnetic susceptibilities. They represent how much a material gets polarized by electric and magnetic fields. for the electric flux density:

$$\mathbf{D} = \epsilon\mathbf{E} = \epsilon_0 (1+\chi)\mathbf{E} = \epsilon_0\mathbf{E} + \epsilon_0\chi\mathbf{E} = \epsilon_0\mathbf{E} + \mathbf{P}$$

where $\mathbf{P} = \epsilon_0\chi\mathbf{E}$ represents the polarization in the dielectric, or the mean electric dipole moment per volume. The same applies for magnetic fields:

$$\mathbf{B} = \mu\mathbf{H} = \mu_0 (\mathbf{H} + \chi_m\mathbf{H}) = \mu_0 (\mathbf{H} + \mathbf{M})$$

where the magnetization $\mathbf{M} = \chi_m\mathbf{H}$, (mean magnetic moment per unit volume)

The refractive index can then be defined as

$$n = \sqrt{\epsilon_R \mu_R}$$

where $\epsilon_R = \frac{\epsilon'}{\epsilon_0} = 1+\chi$, and $\mu_R = \frac{\mu}{\mu_0} = 1+\chi_m$, the relative electric and magnetic constants.

For inhomogeneous materials, the situation is different. The permittivity depends on the position in the material

$$\mathbf{D}(\boldsymbol{r}, t) = \epsilon(\boldsymbol{r})\,\mathbf{E}(\boldsymbol{r}, t)$$

In anisotropic materials, ϵ is directional, and is described by a matrix $\left[D_{xyz}\right] = \left[\epsilon_{xx-zz}\right]\left[E_{xyz}\right]$, see [31, ch. 1.3]. There are also nonlinear materials, where the expression for ϵ is expanded in a power series form.

Materials can also have a frequency-dependent ϵ, this is because materials cannot respond to a field instantaneously. This gives us a convolutional expression for the flux densities:

$$\mathbf{D}(\boldsymbol{r}, t) = \int_{-\infty}^{t} \epsilon\left(t - t'\right)\mathbf{E}\left(\boldsymbol{r}, t'\right) dt' \tag{A.12}$$

or in the frequency domain:

$$\mathbf{D}(\boldsymbol{r},\omega) = \epsilon(\omega)\,\mathbf{E}(\boldsymbol{r},\omega) \tag{A.13}$$

This frequency dependence (eq.A.12-A.13) is true for all materials, so any material is dispersive.[31, 33]. Dispersion causes wide-band signals to distort as they travel, causing pulse-widening and distortion of the signals.

A.1 Simplification by harmonic time dependence

To make the solutions for Maxwells equations easier to find, the condition that all parts of the solution is harmonic-time-dependent can be applied for single frequencies. To make the full solution, the individual frequency solutions can be combined with the inverse Fourier transform.

$$\mathbf{E}(\boldsymbol{r},t) = \int_{-\infty}^{\infty} \mathbf{E}(\boldsymbol{r},\omega)\, e^{j\omega} \frac{d\omega}{2\pi}$$

Where the assumption is that all fields are time dependent with $e^{j\omega}$, and the fields become complex phasors:

$$\mathbf{E}(\boldsymbol{r},t) = \mathbf{E}(\boldsymbol{r})\, e^{j\omega t},\ \mathbf{H}(\boldsymbol{r},t) = \mathbf{H}(\boldsymbol{r})\, e^{j\omega t}$$

equations A.1-A.4 then can be rewritten as

$$\nabla \times \mathbf{E} = -j\omega\mathbf{B} \tag{A.14}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + j\omega\mathbf{D} \tag{A.15}$$

$$\nabla \cdot \mathbf{D} = \rho \tag{A.16}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{A.17}$$

For the energy density, Poynting vector and the ohmic power losses, we can use phasor notation and write

$$w = \frac{1}{2}\Re\left[\frac{1}{2}\epsilon\mathbf{E}\cdot\mathbf{E}^* + \frac{1}{2}\mu\mathbf{H}\cdot\mathbf{H}^*\right] \quad \text{(energy density)} \tag{A.18}$$

$$\mathcal{P} = \frac{1}{2}\Re\left[\mathbf{E}\times\mathbf{H}^*\right] \quad \text{(Poynting vector)} \tag{A.19}$$

$$\frac{\partial P_{loss}}{\partial V} = \frac{1}{2}\Re\left[\mathbf{J}_{tot}\cdot\mathbf{E}^*\right] \quad \text{(ohmic losses)} \tag{A.20}$$

where $\mathbf{J}_{tot} = \mathbf{J} + j\omega\mathbf{D}$ is the total current from amperes law.

With the harmonic simplification, dispersion can be written as(see [31, ch 1.9])

$$\dot{\epsilon} = \frac{1}{2\pi}\int_{-\infty}^{\infty} j\omega\epsilon(\omega)\, e^{j\omega t} d\omega$$

The model for this is the "Lorentz dielectric" model

$$\epsilon(\omega) = \epsilon_0 + \frac{\epsilon_0\omega_p^2}{\omega_0^2 - \omega^2 + j\omega\gamma}$$

where ω_p is the plasma frequency, γ is the measure of rate of collisions per unit time. The model then says that at a certain frequency, a given dielectric becomes very absortive, becoming lossy.

The same concepts of dipole moments applied to a conductor gives

$$\sigma(\omega) = \frac{\epsilon_0 \omega_p^2}{\gamma + j\omega}$$

This is called the "Drude model".

The nominal conductivity at zero frequency is:

$$\sigma = \frac{N \cdot q^2}{m\gamma}$$

where $\frac{q}{m\gamma}$ is the mobility of the conduction charges and N is the volume density of $^{\text{electrons}}/_{\text{m}^3}$. The conductivity of copper is extremely frequency independent up to about 650 GHz[31].

Rewriting for J we get ohms law

$$J = \frac{Nq^2}{m\gamma} E = \sigma E$$

For brevity, some math is skipped. The result is; at sub-Terahertz frequencies, the conductivity of metals are frequency independent.

A.2 Simple solutions

A one dimensional wave equation is of the form[33]:

$$\frac{\partial^2 E_x}{\partial z^2} = \mu\epsilon \frac{\partial^2 E_x}{\partial t^2}$$

Where the general solution is of the form

$$E_x(z,t) = f_1\left(t - \frac{z}{v}\right) + f_2\left(t - \frac{z}{v}\right)$$

where $v = \frac{1}{\sqrt{\mu\epsilon}}$ is the wave velocity. v can also be represented as

$$v = \frac{c}{\sqrt{\epsilon_R \mu_R}}$$

With phasor simplification, the one dimensional wave gives the 1D Helmholtz equation:

$$\frac{d^2 E_x}{d^2 z} = -\omega^2 \mu\epsilon E_x$$

the solution is now

$$E_x = C_1 e^{-jkz} + C_2 e^{jkz} \tag{A.21}$$

$k = \omega\sqrt{\mu\epsilon} = \frac{\omega}{v}$ is the wavenumber. It is easy to see that eq.A.21 can be converted to

$$E_x(z,t) = C_1 \cos(\omega t - kz) + C_2 \cos(\omega t + kz)$$

and the wavelength, $\lambda = \frac{2\pi}{k} = \frac{2\pi v}{\omega} = \frac{v}{f}$ [33].

A.3 Solving electromagnetic problems

Before the computer, there was a need to calculate exact solutions from Maxwell's equations, analytically changing them so that they could be more easily solved exactly and by hand. When computers became fast enough, they became able to solve problems of a much higher order, including problems with no exact solution. Several methods for calculating fields and currents have been invented, in the field called *computational electromagnetics*. The one focused on in this thesis is the *method of moments* (MOM). It is the method used for all the EM simulations in this thesis, unless explicitly specified otherwise.

The method of moments is based on restructuring a field problem into a matrix form, and then solve the matrix. To demonstrate, there is used an example from [28].

To solve an equation

$$L(f) = g$$

where L is a linear operator, g is the source and f is the field, the solution is, naturally:

$$f = L^{-1}(g)$$

if g is known. L^{-1} can be found by using Green's function techniques, not discussed here, as the computer does the work for us, and the method presented is here to illuminate the process.

Back to

$$L(f) = g$$

Let us find f. First we expand f into $f_1, f_2, \ldots$ in the domain of L

$$f = \sum_n \alpha_n f_n$$

α_n are constants, f_n is the basis functions. f can be an infinite or a finite sum, the finite form usually gives an approximation to f. As L is a linear operator, it can be substituted into the expression

$$\sum_n \alpha_n L(f_n) = g$$

It is then assumed that there is found a suitable inner product $\langle f, g \rangle$. A set of testing functions is defined, the weights $w_1, w_2, w_3, \ldots$. These are also in the same domain as L. $\langle \sum_n \alpha_n L(f_n), w_m \rangle$ is then expressed as

$$\sum_n \alpha_n \langle w_m, L f_n \rangle = \langle w_m, g \rangle$$

where m are the positive integers. To write this in matrix form:

$$[l_{mn}][\alpha_n] = [g_m]$$

where

$$[l_{mn}] = \begin{bmatrix} \langle w_1, Lf_1 \rangle & \langle w_1, Lf_2 \rangle & \cdots \\ \langle w_2, Lf_1 \rangle & \langle w_2, Lf_2 \rangle & \cdots \\ \vdots & \cdots & \ddots \end{bmatrix} \tag{A.22}$$

$$[\alpha_n] = \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \end{bmatrix}, [g_m] = \begin{bmatrix} \langle w_1, g \rangle \\ \langle w_1, g \rangle \\ \vdots \end{bmatrix}$$

If $[l_{mn}]$ is nonsingular, $\left[l_{mn}^{-1}\right]$ exists. If this is not the case the simulator fails.

α_n is then

$$[\alpha_n] = \left[l_{mn}^{-1}\right] [g_m]$$

and f, or more correctly expressed as the matrix

$$\left[\tilde{f}_n\right] = \begin{bmatrix} f_1 & f_2 & f_3 & \cdots \end{bmatrix}$$

is

$$f = \left[\tilde{f}_n\right] [\alpha_n] = \left[\tilde{f}_n\right] \left[l_{mn}^{-1}\right] [g_m] \tag{A.23}$$

Many factors affect the size of the problem and the accuracy of the solution, for simple problems the solution might be exact, for larger problems with more unknown, no exact solution exists, and the answer becomes a polynomial approximation. The largest computational resource requirement here is the determination of $[l_{mn}]$ and inverting it into $\left[l_{mn}^{-1}\right]$. To get good convergence of the problem f_n and w_n must be chosen carefully. If $f_n = w_n$ is chosen, then this is called *Galerkin's method*.

To make the problem less difficult, solutions can be chosen to be found only at certain points of interest, and then approximated by piece-wise linearity. This is the "Advanced Frequency Sweep" (AFS) method used by the AXIEM simulator. At the time of writing, a workstation used ~12 Hours solving a EM problem with ~300 000 unknowns ($45 \cdot 10^9$ simultaneously solved function indices in the uncompressed matrix per frequency). By expanding the classes of the operator L, functions that have no second derivative can be found. In [28] we also see that arbitrary 3D electromagnetic problems can be represented by network parameters.:

$$[V] = [Z] [I]$$

Where $[Z]$is found from the solution made by the method of moments, giving first the current distribution in the problem, then evaluated for port current and voltage. This gives us enough data to formulate general scattering parameters

For both 2D and 3D problems, the shapes are divided into a surface mesh. On 3D problems it is easy to see that the matrix of basis (weighting) functions is easily over-defined, so it can be simplified into a compressed matrix[26]. For now, we have seen how an electromagnetic problem is defined, and converted into a computer-solvable problem based on the method of moments with matrix notation. This has hopefully shed some light on the processes used in software designed for these problems. The description is in no way complete, but it illuminates the fundamentals of *computational electromagnetics*.

A.4 Microstrip line introduction

Microstrips (MS) are the principal structure used in this work, they consist of a metal strip, some distance from a return-plane with a large (infinite) extent. Traditionally, MS was made on a dual-layer PCB, where the components would be mounted directly on the strips, achieving low cost and a usable range of impedances. In this thesis, all the metal features are embedded in dielectric, because we are working in an IC process. The equations have slight differences, but because the majority of the **E** field is between the bottom of the conductor and the return layer (therefore in the dielectric), the numerical results for impedance and transmission constant (γ) are very close.

In the case of microstrip, the metal is the main contributor to the loss, while the dielectric losses increase with frequency [33]. The **E** field is most concentrated on the side facing the return layer. This in turn makes the current distribution in the conductor uneven, most of the current travels on the bottom face of the conductor[33]. The asymmetry of the MS also shows that the wave that travels on the MS is not TEM. Although not perfect, the propagation mode is sufficiently similar to TEM propagation, often described as Quasi-TEM, so we hold the TEM mode as a suitable approximation. MS lines are dispersive, the group velocity is frequency dependent. and they can radiate[60]. . The design of microstrips is generally made

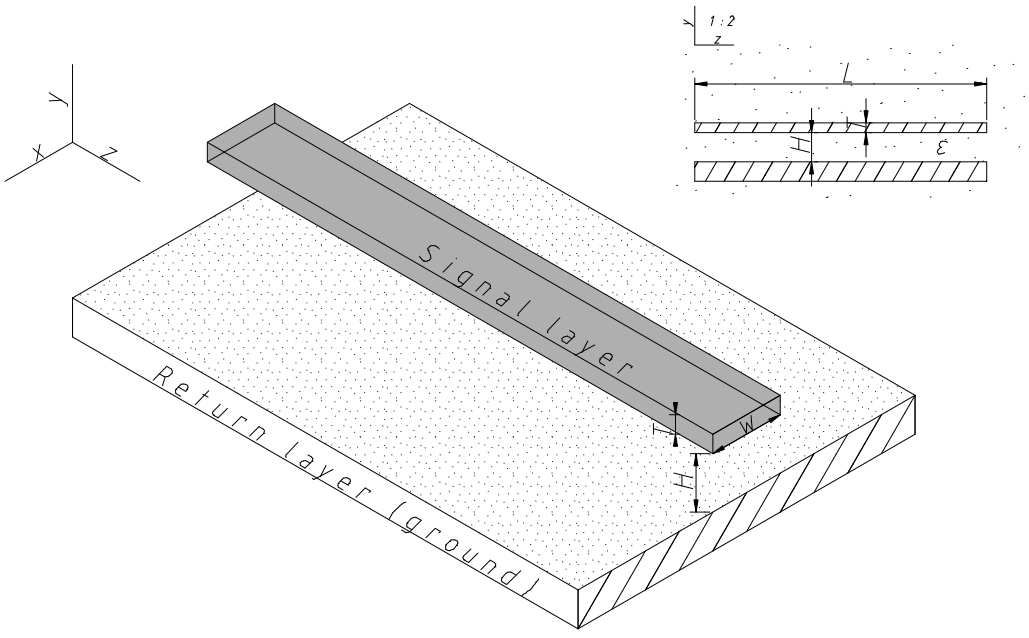

Figure A.1: *Microstrip with finite ground plane*

with the characteristic impedance Z_0 , where wider lines give lower impedance.

$$Z_0 \propto \frac{1}{W}$$

The height between the substrate(ground) and the bottom of the line also strongly affects the impedance, but is usually less free i.e. the height is usually based on the process/PCB specifications from the manufacturer. A simple formula for Z_0 is[35]:

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_e}} \ln\left(\frac{8H}{W} + \frac{W}{4H}\right) & \text{for } W/H \leq 1 \\ \frac{120\pi}{\sqrt{\epsilon_e}\left[\frac{W}{H} + 1.393 + 0.667 \ln\left(\frac{W}{H} + 1.444\right)\right]} & \text{for } W/H \geq 1 \end{cases} \tag{A.24}$$

where

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + 12\frac{H}{W}}}$$

This model uses the TEM approximation, as the equations are only dependent on the cross-section of the microstrip. Losses are determined by the conductivity of the metal line, the

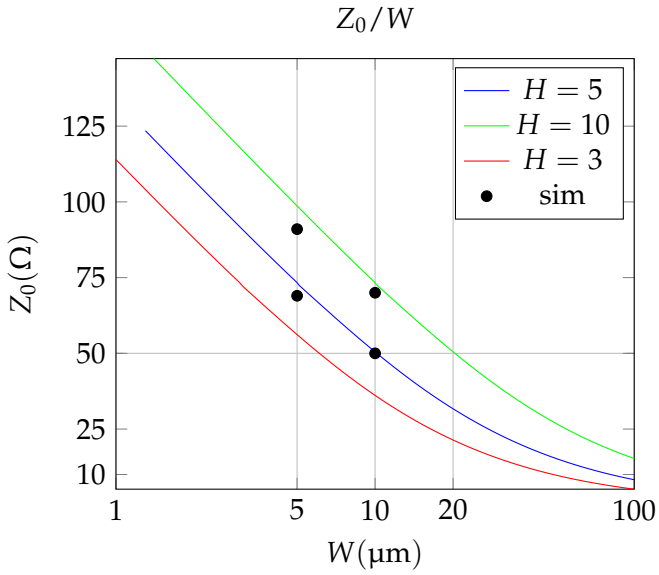

Figure A.2: *Approximate microstrip impedance as a function of width (eq.A.24), MWO impedances from table A.1 marked with points.*

cross-section and $\leq 5\%$ of the loss can be attributed to most dielectrics. For loss, a simple approximation is:

$$^{\text{Loss}}/_{\text{Length}}\,[\text{dB/m}] \approx 8.686 \cdot \frac{R_{sh}}{W} \cdot 2Z_0$$

where R_{sh} is the sheet resistance, dependent on resistivity, permeability and frequency 8.686 is a conversion ratio from nepers to decibels. The minimum RF sheet resistance is

$$\frac{\rho}{\delta_s}\,[\Omega/\square] \propto \sqrt{f}$$

so for Aluminium this minimum is 0.08 $\frac{\Omega}{\square}$ at 60 GHz[61]. For a 5 µm wide conductor in the ihp-sg13s process, with simulations we see that the loss per mm in figure A.1.

Table A.1: *Loss of selected microstrips*

H	Model,$W = 5$	loss at 60GHz per mm	Z_0
10 µm	closed form	0.38 dB	85.1 Ω
5 µm	closed form	0.66 dB	66.2 Ω
10 µm	EM simulation	1.3 dB	91 Ω
5 µm	EM simulation	1.3 dB	69 Ω
–	$W = 10$	-	-
10 µm	EM simulation	0.6 dB	70 Ω
5 µm	EM simulation	1.2 dB	50 Ω

The non-difference of the loss on 10/5 µm *and* 5/5 µm *lines is attributed to bad aspect ratio of the conductor*

A.4.1 Lossy lines

A line made of metal is lossy, it has a finite conductivity. The less resistance is in the wire, the more it looks like a perfect conductor, and the equations for TEM transmission are good approximations.

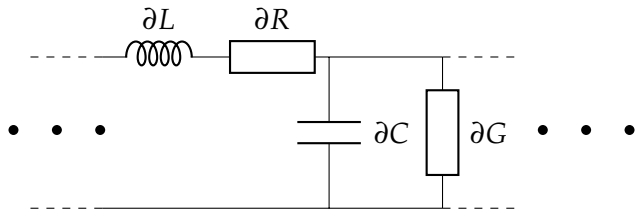

Figure A.3: *Lumped subsection model of transmission line, modeled by the telegraphers equations*

For lines that are lossy, we have dispersion, to limit the dispersion, R/L should be equal to G/C [33]. Where R is the series partial resistance, G the partial conductance, L the partial inductance and C the partial capacitance. To make a line with this property, one can periodically load the line with capacitance[1] to make an artificial transmission line[2]. This will have minimal dispersion up to a cutoff frequency called the Bragg frequency. The trade-off is that the frequency response no longer will be flat, but slightly varying. An important note about the nature of signal transmission is that the waves are traveling through the dielectric, while the conductors carry current, the fields are always zero inside of the conductor[3]. The fields are more concentrated at discontinuities (corners, gaps, steps), so these kind of features can severely impact the performance of a distributed network.

[1] Or inductance, O.Heaviside first did this to make higher speed trans-atlantic communication possible

[2] artificial transmission lines are also called a slow-wave structure, see also defected ground structures(DGS)

[3] white lie, the displacement current is more than 7 orders of magnitude smaller than the conductive current, therefore set to zero.[33]

A general expression of the partial impedances on integral form for a cross section S from[62]:

$$\partial C = \frac{1}{|v_0|^2}\left[\int_S \epsilon' \left|\mathbf{e}_t\right|^2 dS - \int_S \mu' \left|h_z\right|^2 dS\right] \tag{A.25}$$

$$\partial L = \frac{1}{|i_0|^2}\left[\int_S \mu' \left|\mathbf{h}_t\right|^2 dS - \int_S \epsilon' \left|e_z\right|^2 dS\right] \tag{A.26}$$

$$\partial G = \frac{\omega}{|v_0|^2}\left[\int_S \epsilon'' \left|\mathbf{e}_t\right|^2 dS - \int_S \mu'' \left|h_z\right|^2 dS\right] \tag{A.27}$$

$$\partial R = \frac{\omega}{|i_0|^2}\left[\int_S \mu'' \left|\mathbf{h}_t\right|^2 dS - \int_S \epsilon'' \left|e_z\right|^2 dS\right] \tag{A.28}$$

it is simple to see that eq.A.25 without the magnetic field in the z direction simplifies to Gauss' theorem.

A.4.2 Microstrip Moding

Waveguides use only a single conductor, and transmit power by the $TE_{n,n}$ and $TM_{n,n}$ modes, most often $TE_{0,1}$, or $TM_{0,1}$ for coaxial lines[4]. The TEM mode can be viewed as $TE_{0,1} + TM_{0,1}$. In circuits made on a substrate, for certain (unfortunate) combinations of dimensions and frequencies a TEM intended circuit can exhibit more of the transverse-electric or transverse-magnetic modes. This can happen, for example on a conductor wider than $\lambda/4$, quarter wavelength[5] , a dielectric volume fenced in by vias, at some frequency becoming $\frac{n\lambda}{4}$ large. The moding phenomenon generally causes extra losses and spurious responses. [61]

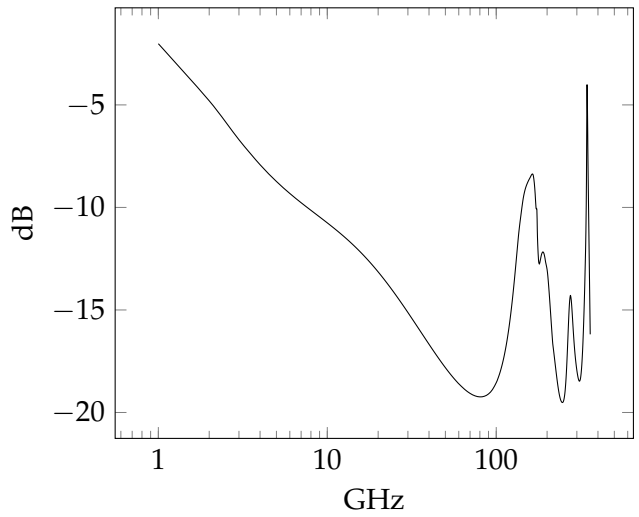

Figure A.4: *Moding caused by deliberate poor w/l and w/h aspect ratio of a microstrip (S_{21}). Moding causes convergence issues for the simulator as well as giving an ugly response on high frequencies.*

More on microstrips in [35, 63, 34].

[4] $TE_{0,N}$, $TM_{0,N}$, $TM_{1,1}$ and $TM_{1,2}$ has zero cut-off wavelength
[5] Quarter wavelength ($\lambda/4$) is the smallest dimension that supports resonance

Appendix B

System noise

Voltage noise of a resistor in a narrow bandwidth is defined as

$$V_n = \sqrt{4kTBR}$$

Noise power is

$$P_n = kTB$$

Noise spectral density is

$$S_n(\omega) = \frac{P_n}{2B} = \frac{kT}{2}$$

Where k is Boltzmanns' constant, T is temperature in Kelvin, B is bandwidth in Hertz. Path loss by the friis

Equivalent noise temperature is

$$T_e = \frac{P_n}{kB}$$

Using T_e to replace an arbitrary source with a resistor, with the same value as the load (e.g. 50 ohm) at a temperature so that the same power of noise is delivered to the load as the source.The equivalent noise temperature of an amplifier is :

$$T_e = \frac{P_{n_{out}}}{GkB}$$

In this work noise temperature is always referred to the input of a device.

B.1 Noise factor

The noise factor F of a system is defined as

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{B.1}$$

or [64]

$$F \equiv \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source}$$

The noise figure is defined as the noise factor in dB:

$$NF = 10\log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) = SNR_{in,dB} - SNR_{out,dB} \tag{B.2}$$

Noise temperature, T is the physical temperature, $T_0$is the input temperature, and $T_e$is the noise temperature of the device.

$$\frac{P}{B} = k_B T$$

The noise factor is related to the noise temperature:

$$F = 1 + \frac{T_e}{T_0}$$

For attenuators, at a physical temperature :

$$T_e = (L-1)\,T$$

$$F = 1 + \frac{(L-1)\,T}{T_0}$$

For a cascade of devices:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}} \tag{B.3}$$

Where G_n is the *linear* power gain.(not in dB)
Using

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f}$$

$$G_s \equiv \frac{\overline{i_s^2}}{4kT\Delta f}$$

Then F can be written

$$\begin{aligned} F &= 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} \\ &= 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right] R_n}{G_s} \end{aligned}$$

So that F is described in terms of a conductance G and a susceptance B

$$F_{min} = 1 + 2R_n\left[G_{opt} + G_c\right] = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right] \tag{B.4}$$

or in terms of $Fmin$ and source admittance:

$$F = F_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right]$$

Then the optimum source admittance of a device can be found to be:

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \tag{B.5}$$

B.2 MDS

The minimum detectable signal on the input of a system is[65]:

$$\begin{aligned} S_{i_{min}} &= \left(\frac{N_o}{G}\right)\left(\frac{S_o}{N_o}\right)_{min} \\ &= kB\left(T_A + T_e\right)\left(\frac{S_o}{N_o}\right)_{min} \\ &= kB\left[T_A + \left(F-1\right)T_o\right]\left(\frac{S_o}{N_o}\right)_{min} \end{aligned} \tag{B.6}$$

If the ambient temperature T_A is equal to T_0 the expression in B.6 reduces to

$$S_{i_{min}} = kBT_0F\left(\frac{S_o}{N_o}\right)_{min} \tag{B.7}$$

or in decibels:

$$S_{i_{min}}\left(dB\right) = 10\log\left(kT_0\right) + 10\log\left(B\right) + F(\text{dB}) + \left(\frac{S_o}{N_o}\right)_{min}(\text{dB})$$

Note that the minimum detectable signal is not dependent on gain, only on SNR. Additionally $10\log\left(kT_0\right) = -203,97\text{dB/Hz} \cong -174\text{dBm/Hz}$ for $T_0 = 290\text{K}$

For digital modulation we have the bit energy to noise ratio:

$$\frac{E_b}{n_o} = \frac{S_o}{N_o}\frac{B}{R_b}$$

where E_b is bit energy, n_o is noise power. R_b is bit rate.

The free space path loss is given by the Friis equation:

$$P_r = P_t \cdot \frac{G_T G_R \lambda^2}{\left(4\pi R\right)^2} \tag{B.8}$$

Efficiency in high-speed circuits is often defined as power-added efficiency

$$\eta_{PAE} = PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\eta$$

PAE describes the efficiency of a component, where the input signal counts as power added. For very large gains the PAE approaches normal efficiency η.

The Shannon-Hartley theorem states, that for a channel capacity C , there is an inherent limit given by

$$C = B \cdot \log_2\left(1 + SNR\right) \tag{B.9}$$