UNIVERSITY OF BERGEN

GEOPHYSICAL INSTITUTE

Master Thesis in Energy

Specialization in Energy Technology

Electrical Power engineering

Design of rectifier system for electric ferries

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Abstract

This study investigates the requirements and technologies to provide power from shore to ship when the electric ferry is at quay. Different rectifier systems will be evaluated in terms of requirements given by the utility grid owner BKK and the ferry company Fjord1. Two suitable rectifier systems based on voltage orientated control method will be simulated in Simulink under various load conditions. The simulation results will be evaluated with the grid parameters and requirements given by BKK. Important parameters to be considered are power factor, efficiency, harmonic distortion of current and voltage at the point of common coupling and stability of the rectifier. The voltage orientated rectifier system with L-filter is built in the laboratory where the goal is to validate the simulation results. The hardware design is based on insulated gate bipolar transistors from SEMIKRON and digital signal controller eZdsp delivered by spectrum digital.

Acknowledgement

This master thesis in Electrical Power Engineering marks the end of a six year long education and marks the starting point of my career at Siemens. I am grateful for the collaboration between The Western Norway University of Applied Science and Siemens for giving me both a deep insight in power electronics theory and practical applications used in the industry.

I wish to express my sincere gratitude towards my supervisor, Associate Professor Shujun Zhang for his knowledge, understanding and patience. In addition he has been a great contributor in my first academic paper publication, which gave me the opportunity to attend the 21st International Conference on Electrical Machines and systems in Jeju, Korea.

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List of Abbreviations

SC	Shore connection
UPF	Unity power factor
AC	Alternating current
DC	Direct current
IEEE	Institution of Electrical and Electronics Engineers
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization
SWBD	Switchboard
HVSC	High voltage shore connection
LVSC	Low voltage shore connection
HV	High voltage
THD	Total harmonic distortion
rms	Root mean square
PWM	Pulse with modulation
IGBT	Insulated gate bipolar transistor
KVL	Kirchhoff's voltage law
KCL	Kirchhoff's current law
PF	Power factor
AFE	Active front end
CB-PWM	Carrier based pulse with modulation
SVPWM	Space vector pulse with modulation

VOC	Voltage orientated control
VFOC	Virtual flux orientated control
DPC	Direct power control
VF-DPC	Virtual flux direct power control
PLL	Phase lock loop
PI	Proportional Integral
ADC	Analog to digital converter
DSP	Digital signal processor
DAC	Digital to analog converter
CCS	Code composer studio
DSC	Digital signal controller
ePMW	Enhanced PWM
MUX	Multiplexer
S/H	Sample and hold
TB	Time-base
CC	Counter compare
AQ	Action-Qualifier
GPIO	General-purpose input/output
DB	Dead band
PC	PWM-chopper
TZ	Trip zone
OSHT	One-shot-trip

ET	Event trigger
SOC	Start of conversion
op amp	Operational amplifier
GND	Ground

1 Introduction

In Norway there are approximately 180 ferry crossings where 80% are located between Stavanger and Trondheim [1]. The ferry fleet is mainly driven by combustion engines, running on diesel, liquefied nature gas or marine gas oil. Instead of conventional combustion engines it is possible to install electric motors fed by batteries on board. Some of the existing ferries use diesel electric propulsion systems, which means that it is even more convenient to go from fossil fuel to battery powered propulsion. Thus the diesel/gas generators can be removed, and the installation of battery packs which deliver electrical energy to the already installed electric motors can be conducted. For ferry crossings that have transit time less than 35 minutes and at least 20 trips per day, is it preferable with battery-powered ferries [2]. The batteries supply electrical energy for propulsion systems, shipboard technical systems and hotel services. In order to have a successful electrification of the ferry fleet, is it crucial to design a reliable shore connection (SC) system for battery charging.

1.1 Background

Due to the increased awareness of climate change and the fact that Norway signed the Paris agreement in 2015, this has led to the commitment to decrease emissions. The transportation sector is a major polluter and must decease their emissions if the Paris agreement is to be met. Ferry companies have to take their responsibility to reduce their emissions and use new technology to achieve lower energy consumption and environmental impacts. In Norway there are several new ferry contracts that either are fully electrical with batteries as energy source or hybrid vessels combined with diesel generators and batteries. In regards to electrification of the new ferry fleet, grid owners must consider to upgrade the utility grid near ferry terminals. The ferry crossings taken into account are limited to the locations in table 1. The most important parameters from the utility grid owner BKK are listed up [3]. The power capacity is limited in several locations and BKK might need to reinforce the utility grid in several areas before a electric ferry terminal can be established. The connection of the ferry terminal is regulated by supply safety

Table 1: Parameters from the utility grid near ferry terminals. Limited to the concession of the grid owner BKK. Note that $\cos\phi_{sc}$ is the relationship between the inductive and resistive short circuit capacity of the grid.

Ferry terminal	Estimated power capacity	Voltage level	Short circuit capacity	$\cos\phi_{sc}$
Leirvåg	3 MVA	22 kV	115 MVA	0.42
Sløvåg	3.5 MVA	22 kV	58 MVA	0.4
Fedje	0.5 MVA	22 kV	34 MVA	0.8
Sævrøy	0.5 MVA	22 kV	33.5 MVA	0.76
Krokeide	50kVA	11kV	31 MVA	0.62
Hatvik	4 MVA	22 kV	87 MVA	0.48
Haljem	2 MVA	22 kV	100 MVA	0.43

regulations and there are requirements to voltage quality in regards to the total harmonic distortion (THD), rapid voltage changes and flicker [4]. However the grid owners can demand stricter limits than described in the supply safety regulation [3]. BKK requires half of the parameters values described in the supply safety regulation in regards to harmonic distortion. After meeting BKK at their office in Kokstad, it was clear that the most important parameters regarding to voltage quality are the harmonic distortion and the voltage dips. The ferry charger involves power electronic components that are a source of harmonic distortion. Furthermore, electric ferries will have frequent connections to the utility grid that can lead to voltages dips. The maximum values for the harmonic components are listed up in table 2. THD are limited to 8% measured as an average value over 10 minutes or maximum 5% measured as an average value over 1 week [5]. The explanation on how to compute the distortion will be derived in section 3.1. The supply safety regulations describe voltage dips greater or equal 5% below agreed voltage rms value with a short duration (10ms-60s) to occur maximum 12 times per 24 hours.

The aforementioned requirements are important for BKK, but the ferry companies also have demands for the ferry charger application. In that regard there was conducted a meeting with Fjord1 that is the largest ferry company in Norway. They have several new ferry projects with predominantly electric ferries. Some of the important parameters that were mentioned under the meeting were power efficiency of the ferry charger, controllable power factor (PF) configured as either unity power factor (UPF) or leading PF using the ferry charger as a static compensator (STATCOM).

Table 2: Maximum values for the harmonic components drawn from the utility grid owner BKK. Parameters described in the table are restricted to nominal voltages $V \in [0.23, 35]$ kV

Odd harmonics				Even harmonics	
Not a multiple of 3		Multiple of 3			
Order h	V_h	Order h	V_h	Order h	V_h
5	3.0%	3	2.5%	2	1.0%
7	2.5%	9	0.75%	4	0.5%
11	1.75%	15	0.25%	>4	0.25%
13	1.5%	21	0.25%		
17	1.0%	>21	0.25%		
19,23,25	0.75%				
>25	0.5%				

1.2 Object of thesis

To restrict the scope of the ferry charger it was decided to investigate solutions for the rectifier system. This thesis attempts to answer the following question: Which rectifier is the most suited for charging electrical ferries? Parameters that are crucial are efficiency, controllable PF, harmonic current drawn from the utility and stability of the rectifier under several load conditions. To answer the following question, several rectifier technologies will be analyzed and simulated in Simulink. One of the rectifier topology will be built in the electric power laboratory. If the physical model is completed in time will the measured values be compared to the simulation results.

1.3 Structure of thesis

This thesis is divided in several section as follows: Section 2 gives an overview of two generic SC systems according to international standards. Section 3 analyzes different rectifier systems in regards to crucial parameters mentioned in section 1.2. Section 4 describes two rectifier systems with different filter design. Both systems are simulated in Simulink in section 5, where their parameters in regard to

voltage quality and stability are presented. Section 6 describes the physical rectifier model build in the electric power laboratory. The discussion of the results for both simulation and the laboratory model are discussed in section 7. The conclusion and future work of this thesis are presented in section 8.

2 Shore Connection Systems

Shore-to-power-systems come in a variety of names. The most common ones are cold ironing, alternative maritime power, shore-side electricity and onshore power supply. The term cold ironing originates from when ships were equipped with steam generators docked for repair. Both the pipes and steel for the boiler were cold during repair and therefore the term cold ironing is used [6]. In this text, the abbreviation shore connection systems will be used.

The world's first commercial shore connection system was installed at the port of Gotenburg in year 2000. The connection voltage varies between 400V to 10kV 50Hz [7]. Since the year 2000 several ports in the Pacific coast of North America and in Europe have installed shore connection systems. The nominal system voltage is usually 440V, 6.6kV or 11kV depending on the power requirement. The frequency is also varying between the different regions. Europe, Africa and Oceania operate with 50Hz and North America has a grid frequency of 60Hz. Asia uses mostly 50Hz and South America uses both. Over 50% of ships use 60Hz voltage systems[8]. This has lead to the need for a static or rotating frequency inverter in ac systems.

In applications, such as an electric ferry, the ac voltage has to be rectified before charging the batteries on board. Nevertheless, heavy consumers, such as the electric motors for the propulsion systems, pumps, lights and other technical services, need ac voltages to operate. One solution is to have both the rectifier and inverter in the main switchboard (SWBD) on board the electric ferry. In figure 1 the aforementioned solution is illustrated with a diode rectifier and a two-level switch-mode converter. Electrical and hybrid ferries often have a dc distribution system on board to charge the batteries. Therefore the electrical energy, either delivered from the diesel generator and/or from the utility grid on shore, has to be rectified.

To get an overview of the SC systems will the following section present different topologies according to international standards.

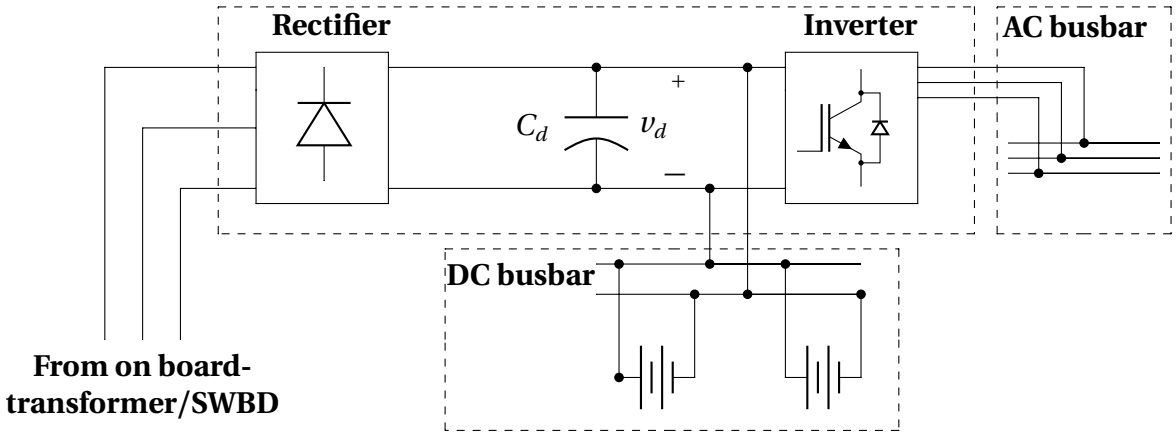

Figure 1: Three-phase diode rectifier charging the on board batteries from the dc busbar. Furthermore a two-level switch-mode inverter delivers electrical energy at a fixed frequency to the ac busbar.

2.1 Different topologies

There are several different topologies for a SC system. It depends on nominal voltage, power frequency on both grid and the ship's electrical system, cable handling devices, space requirements, harsh conditions, power requirements, local grid restrictions etc. Today's standards from IEEE, IEC, and ISO describe general requirements for high voltage shore connection (HVSC) systems [9] and a committee draft on low voltage shore connection (LVSC) systems [10]. Furthermore DNV GL provides rules of classification for electrical shore connections [11]. DNV GL does not differentiate between HVSC or LVSC and only the installation on board the vessel is covered. However some of the requirements described in the standards and classification is not applicable for ferries that have up to 30-40 connection each day. E.g. the SC solution on the battery ferry Ampere deviates from the proposed solutions in existing standards due to the requirement for a rapid and frequent connection. In order to achieve an equivalent safety level as in the standards, specialized solutions have been used.

2.1.1 High voltage shore connection

The international standard IEC80005-1 Utility connections in ports - HVSC systems defines requirement for HVSC systems. The standard highlights both general

requirements and additional requirements for different ship's classes such as Ro-Ro passenger ships. The standard recommends using high voltage (HV) when the required power rating exceeds 1MW. The study [12] states that 52 ferry crossing in Norway need power ratings between 1MW to 10MW. Therefore HV systems are the most relevant if the international standards are to be followed. A typical HVSC system is shown in figure 2. From the block diagram there are several key elements described in the standard [9]:

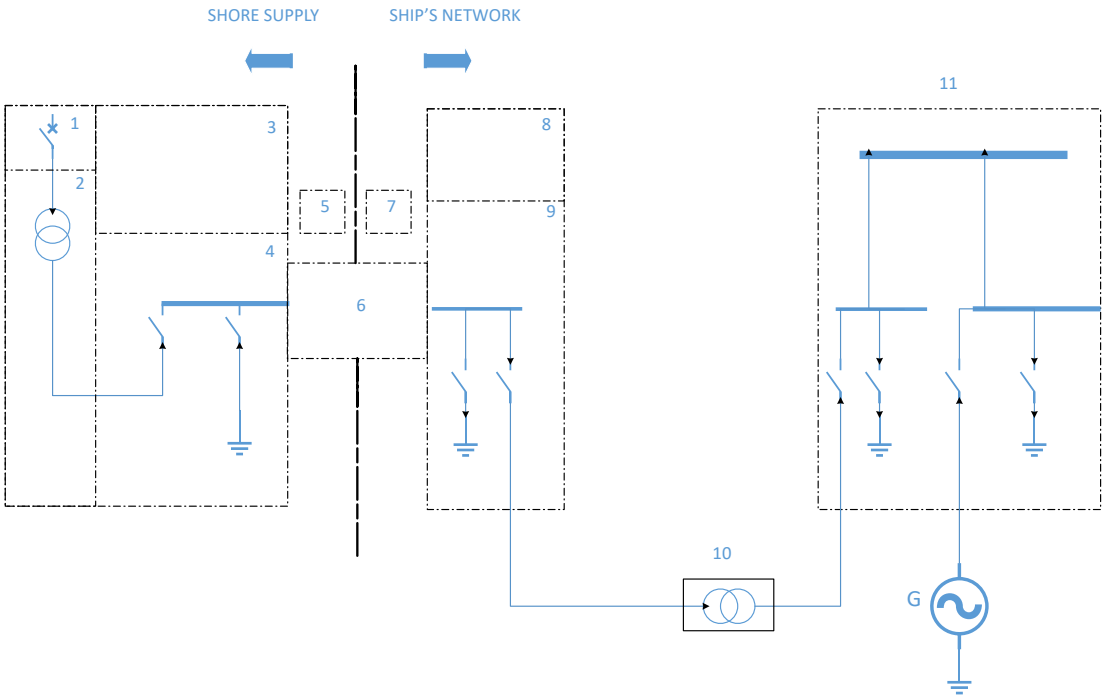

Figure 2: A generic block diagram of a HVSC system. Adapted from [9]

1. Utility supply with associated circuit breaker.

2. The neutral point of the shore side transformer, feeding the shore-to-ship power, shall be earthed through a neutral resistor. An earth fault shall not create a step or touch voltage exceeding 30V at any location between the shore and ship. The nominal voltage levels is described either as 6.6kV or 11kV depending on the power ratings.

3. Shore side protection system shall open all the poles in the circuit breaker in the event of: (a) Overcurrent, including short-circuit. (b) Over-voltage/under-voltage. (c) Reverse -power. Furthermore protection against transient over-voltage surges by means of surge arresters.

4. Shore-side earth switch and circuit breaker. The earth switch is to ensure that all energy in the shore connection cables is dissipated to ground before connection or disconnection between shore and ship side is conducted.

5. Control onshore consist of safety measures such as interlocks of HV circuit breakers, disconnectors and earthing switches.

6. Shore-to-ship connection and interface equipment. Consists of plugs and socket-outlets, cable handling equipment and connection cable. Data communication between shore and ship including information about shore transformer temperature, safety circuits, circuit breaker protection activation etc.

7. Control and monitoring of: (a) Cable tension and length. (b) Current unbalanced between multiple phases. (c) Equipotential bond created by the ship to shore connection cable shall be constantly monitored (d) Interlocks between earthing switches and circuit breakers.

8. Ship protection relaying shall be equipped with the same safety measurement as described in point 3 and also: (a) Over/under-frequency. (b) Phase sequence protection.

9. On board shore connection SWBD shall be equipped with: (a) Voltmeter in all three phases. (b) Short-circuit devices. (c) Overcurrent devices. (d) Earth-fault-indicator. (e) Unbalanced protection for systems with parallel cables.

10. Galvanic separation between the shore and ship's electrical systems is required either by a transformer on board or on shore. This is done to ensure that earth-fault-current from shore-to-ship or vice versa is eliminated. The transformer also supply the main SWBD on board with the desired voltage level.

11. The synchronization process is performed at the main SWBD on board the ship. Instrumentation necessary to transfer load via parallel connection is: (a) Two voltmeters. (b) Two frequency meters. (c) One ammeter with a selector-switch to enable the current in each phase to be read. (d) Phase sequence indicator. (e) One synchronizing device.

2.1.2 Low voltage shore connection

As mentioned in chapter 2.1 the committee draft IEC 8005-3 LVSC is the nearest international standard that exist for LVSC systems. If the apparent power ratings for the electric ferry are below 1MVA, the committee draft suggest the LVSC system. The committee draft describes a typical LVSC system as shown in figure 3. The block diagram is divided into different sections that describe key elements [10]:

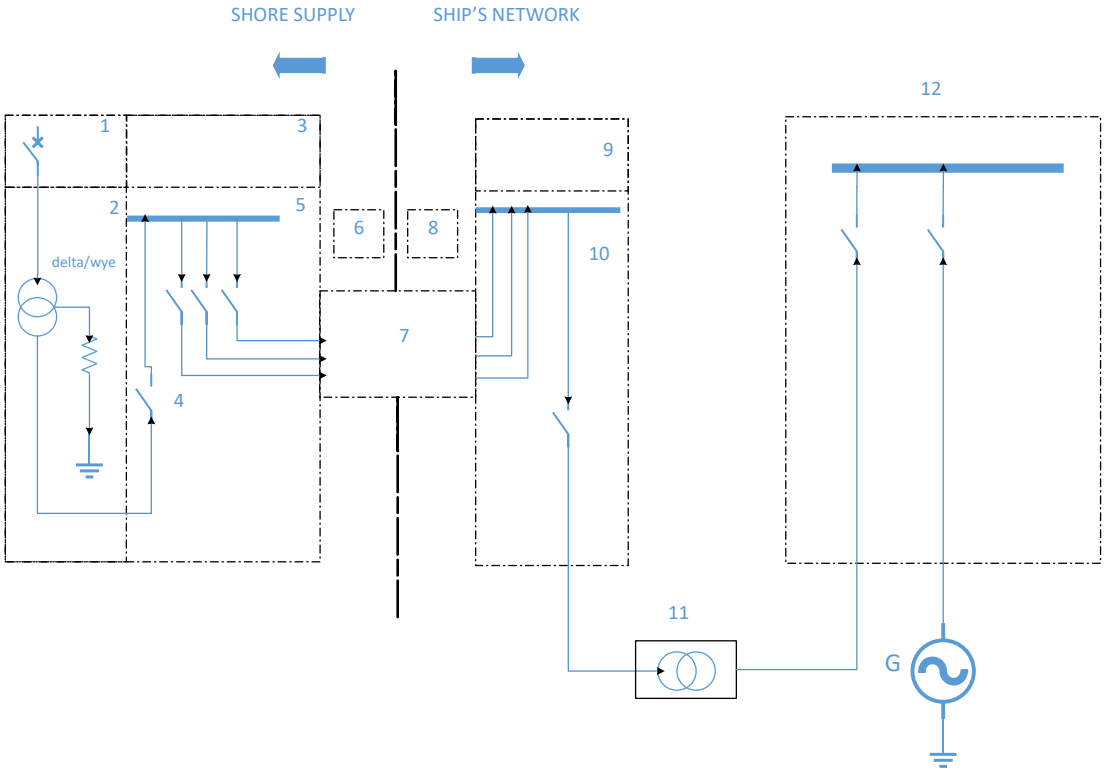

Figure 3: A generic block diagram of a LVSC system. Adapted from [10]

1. Utility supply with associated circuit breaker.

2. The shore-side transformer shall be connected to a neutral grounding resistor (resistor may be omitted in IT-systems). An earth fault shall not create a touch or step voltage exceeding 25V any location between the shore and ship. Nominal voltage is either 400V, 440V or 690V, depending on the power ratings.

3. Shore-side protection system shall open all the poles in the circuit breaker in the event of: (a) Overcurrent, including short-circuit. (b) Over-voltage/under-voltage. (c) Reverse-power. Furthermore protection against transient over-voltage surges by means of surge arresters is included.

4. Shore-side circuit breaker.

5. Shore-side feeders circuit breakers.The number of parallel connections varies according to the power transferred from shore to ship. E.g. 1000kVA power rating with a line voltage of 440V, requires 4 connections.

6. Control onshore, consist of interlocks that prevents connection of circuit breakers and disconnectors in case of: (a) Pilot contacts in the flexible shore-to-ship cable which signals correct connection. (b) Emergency-stop facilities such as push buttons. (c) Undervoltage coils both on shore and on board. (d) Others.

7. Shore-to-ship connection and interface equipment. Consists of plugs and socket-outlets, cable handling equipment and connection cable(s).

8. Control and monitoring of: (a) Cable tension and length. (b) Current unbalanced between multiple phases.

9. Ship protection relaying shall be equipped with the same safety measurement as described in point 3 but also: (a) Over/under-frequency. (b) Phase sequence protection.

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11. Galvanic separation between the shore and ship's electrical systems is required, either by a transformer on board or on shore. This is done to ensure that earth fault from shore-to-ship or vice versa is eliminated. The transformer also supply the main SWBD on board with the desired voltage level.

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3 Rectifier systems

As discussed in section 2, a SC connection system is fairly complex with many components. The need for power electronic equipment for converting the utility voltage and/or frequency is often required. In this section different rectifier systems are presented and also control techniques are explained in detail. Challenges in regards to voltage quality will be explained and a rectifier system will be chosen.

3.1 Nonsinusoidal waveform in steady state

Power electronic circuits may draw highly distorted currents from the utility. Reasons for this phenomena is non sinusoidal loads such as rectifiers, inverters and switch-mode power supplies [13]. Figure 4 illustrates such a periodic waveforms that repeat with a time period T and frequency $f = \frac{1}{T} = \frac{\omega}{2\pi}$. Harmonic distortion

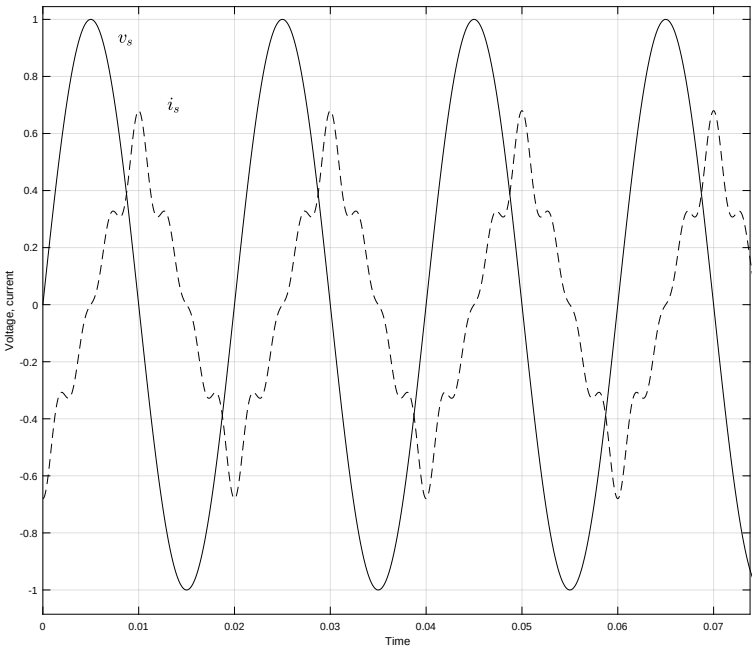


Figure 4: The example waveform shows that the voltage v_s have a sinusoidal waveform without any harmonic content. The current i_s is distorted with harmonic components.

in power systems can lead to undesirable effects such as overheating in transformers, cables, capacitors and motors. Circuit breakers may trip and equipment such

as softstarters, depending of calculating the correct zero crossover point, might malfunction or fail. For distorted waveforms such as the current i_s in figure 4, it can be divided in a fundamental frequency component and harmonic components that are multiple of the fundamental frequency. These components can be calculated by means of Fourier analysis. A non sinusoidal periodic waveform $f(t)$ with an angular frequency ω can be represented by a trigonometric series defined by [14]

$$Ff(t) = \frac{1}{2}a_0 + \sum_{h=1}^{\infty}(a_h \cos(h\omega t) + b_h \sin(h\omega t)) \tag{3.1}$$

The coefficients a_0, a_h and b_h are defined respectively by

$$a_0 = \frac{1}{2\pi}\int_0^{2\pi} f(t)\,d(\omega t) = \frac{1}{T}\int_0^{T} f(t)\,dt \tag{3.2}$$

$$a_h = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(h\omega t)\,d(\omega t) \qquad h = 0,\ldots,\infty \tag{3.3}$$

$$b_h = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(h\omega t)\,d(\omega t) \qquad h = 1,\ldots,\infty \tag{3.4}$$

It should be noted from equation 3.2 that a_0 is the average value of $f(t)$ and is zero in figure 4. The coefficients a_h and b_h can be simplified in use of waveform symmetry (respectively even and odd symmetry). Each frequency component can be represented in term of its rms value. The rms magnitude is given by [14]

$$F_h = \frac{\sqrt{a_h^2 + b_h^2}}{\sqrt{2}} \tag{3.5}$$

The total amount of distortion can be represented by a term called total harmonic distortion or simply THD. In terms of the current, it is defined as [14]

$$\%THD_i = 100 \cdot \frac{I_{dis}}{I_{s1}} = 100 \cdot \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} = 100 \cdot \sqrt{\sum_{h\neq 1}\left(\frac{I_{sh}}{I_{s1}}\right)^2} \tag{3.6}$$

The expression for THD becomes clearer from figure 5. The line current i_s, its

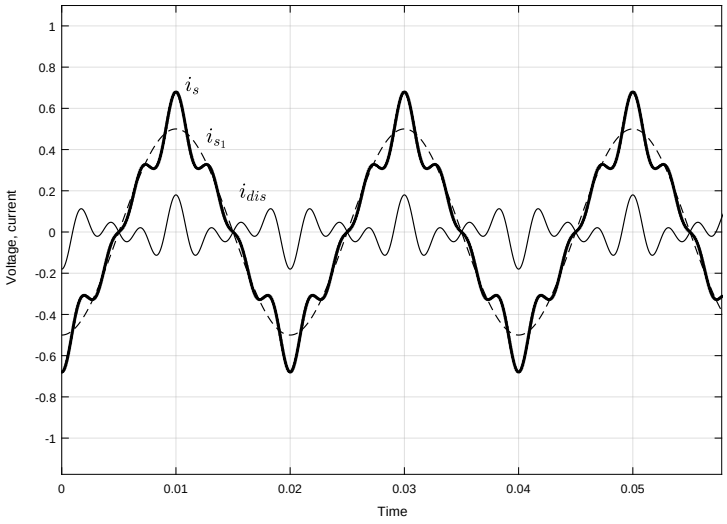


Figure 5: Example of a distorted current with its decomposed values. i_s is the line current including the fundamental frequency component i_{s_1} and the distorted harmonic component i_{dis}.

fundamental frequency i_{s1} and its harmonic part i_{dis} is illustrated as function of time. The distorted line current component is expressed as [14]

$$i_{dis}(t) = i_s(t) - i_{s1}(t) = \sum_{h \neq 1} i_{sh}(t) \tag{3.7}$$

In term of rms values,

$$I_{dis} = \sqrt{I_s^2 - I_{s1}^2} = \sqrt{\sum_{h \neq 1} I_{sh}^2} \tag{3.8}$$

It should be noted that the line voltage v_s from the utility is assumed to be sinusoidal at the fundamental frequency. Also the average value or dc component is assumed to be zero in equation 3.6-3.8. The distorted line current affect the utility line voltage v_{pcc} at the point of common coupling (PCC) as illustrated in figure 6. The PCC in a ferry charger system is typically at the high voltage side of the transformer feeding the SC system. Other loads connected at the PCC will be affected by the distorted current drawn from the ferry charger. It is therefore crucial to install power electronic equipment such as the rectifier, which generates a small amount of harmonic distortion. The rms voltage at the PCC with a harmonic component

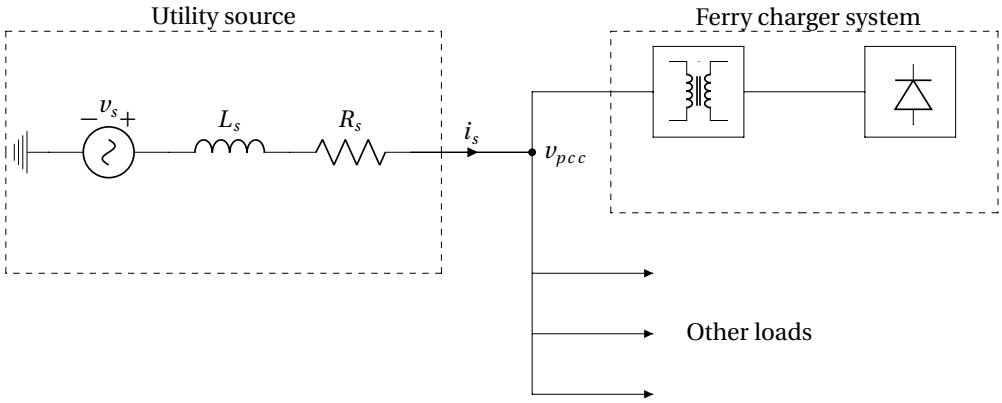


Figure 6: Interface between the utility source and the ferry charger at the PCC. Other loads connected to the PCC will be affected by the distorted current drawn from the ferry charger.

h injected to the ac source is expressed as [14]

$$V_{h_{PCC}} = h\left(R_s + j\omega L_s\right) I_h \tag{3.9}$$

The impedance Z_s can be calculated by the parameters given by the utility grid owner BKK in table 1. Considering only the scalar value of the $V_{h_{PCC}}$ and the fact that

$$Z_s = R_s + j\omega L_s = R_s + jX_s \tag{3.10}$$

$$R_s = |Z_s| \cdot \cos\phi_{sc} \tag{3.11}$$

$$X_s = |Z_s| \cdot \sin\phi_{sc} \tag{3.12}$$

$$|Z_s| = \sqrt{R_s^2 + X_s^2} \tag{3.13}$$

$$\tag{3.14}$$

yields

$$V_{h_{PCC}} = h \cdot |Z_s| \cdot I_h \tag{3.15}$$

The short circuit rms current in a per phase basis is expressed as (all three phases shorted to ground at PCC)

$$I_{sc} = \frac{\frac{S_k}{3}}{\frac{V_{LL}}{\sqrt{3}}} = \frac{S_k}{V_{LL}\sqrt{3}} = \frac{V_s}{|Z_s|} \tag{3.16}$$

where S_k is the three-phase short circuit capacity and V_{LL} is the line to line voltage. S_k and V_{LL} are given in table 1. Combining equation 3.15 and 3.16 yields

$$\%V_{h_{PCC}} = \frac{V_{h_{PCC}}}{V_s} \cdot 100 = h\frac{I_h}{I_{sc}} \cdot 100 \tag{3.17}$$

Calculating the harmonic current components I_h in equation 3.5 and the short circuit current I_{sc} in equation 3.16, yields the harmonic voltage component $\%V_{h_{pcc}}$ in equation 3.17. The calculation of total harmonic distortion is similar for the voltage compared to the current [14], and therefore by equation 3.6

$$\%THD_v = 100 \cdot \frac{V_{dis}}{V_{s1}} = 100 \cdot \frac{\sqrt{V_s^2 - V_{s1}^2}}{V_{s1}} = 100 \cdot \sqrt{\sum_{h\neq 1}\left(\frac{V_{sh}}{V_{s1}}\right)^2} \tag{3.18}$$

3.2 Rectifiers

One of the main components in a SC system and the focus in this paper is the converter. More specific the converter is used as a rectifier in this case. The rectifier converts the sinusoidal line voltage from the utility grid to dc voltage. In this section different rectifiers will be presented with their operational principle in an idealized case.

3.2.1 Diode rectifier

Line-frequency diode rectifiers are unidirectional and convert the utility ac voltage to an uncontrolled dc output voltage. A three-phase, full bridge diode rectifier is shown in figure 7. The diodes conduct in pairs, respectively D1 D2, D3 D4 and D5 D6. The diodes at the top group are at a common potential. Therefore the diode with it's anode at its highest potential will conduct i_{dc}. In the bottom group the diodes are also at a common potential and therefore the diode with its cathode at the lowest potential will conduct i_{dc}.

In an idealized case when the line inductances on the utility side $L_a = L_b = L_c = 0$ and the load is replaced by a constant dc source, the waveform of the rectifier is as seen in figure 8. As illustrated, the instantaneous waveform of v_{dc} consist of

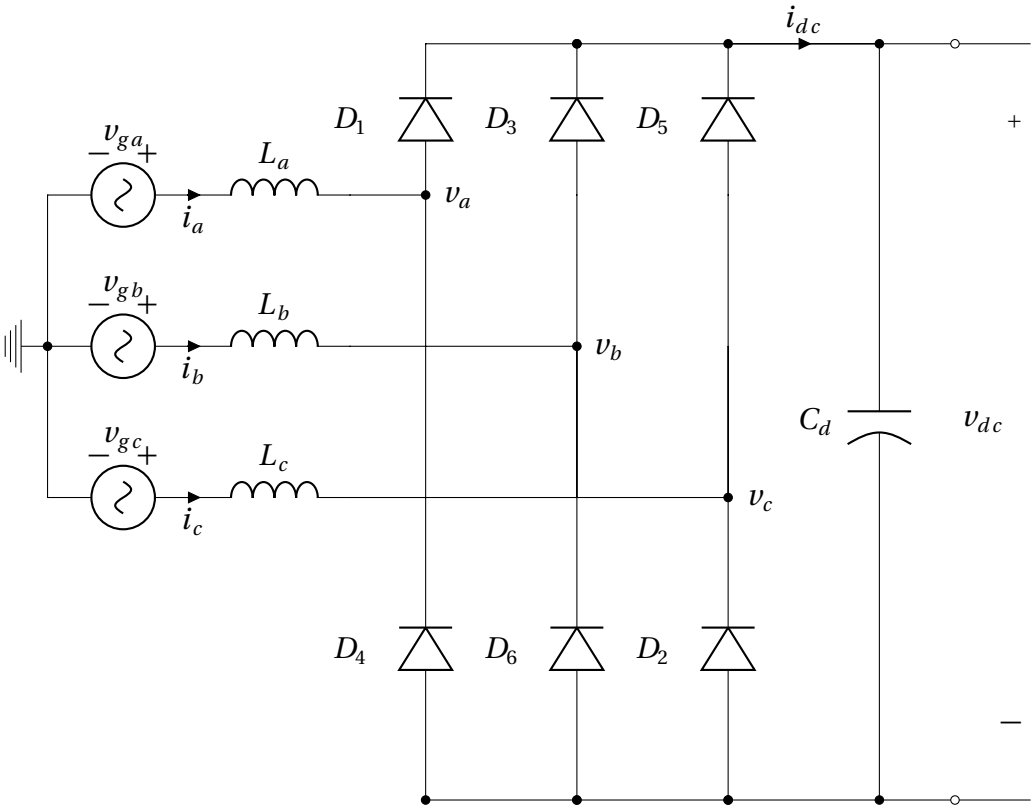


Figure 7: Three-phase full bridge diode rectifier. Adapted from [14].

six pulses and each diode conduct for 120°. The commutation interval is instantaneously in this idealized case. To obtain the average dc output value one of the six pulses is considered and its average value is calculated over an $\frac{\pi}{3}$ interval. Arbitrarily the time origin $t = 0$ is chosen. From figure 8 it can be seen that

$$v_{dc} = v_{ab} = \sqrt{2} V_{LL} \cos(\omega t) \qquad \text{where} \quad \omega t \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right] \tag{3.19}$$

and V_{LL} is the rms utility line to line voltage. The volt-second area A is averaged over the interval $\frac{\pi}{3}$ and the dc output voltage is (o denotes idealized condition)

$$v_{dc_o} = \frac{3}{\pi} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \sqrt{2} V_{LL} \cos(\omega t)\, d(\omega t) = \frac{3}{\pi} \sqrt{2} V_{LL} = 1.35\, V_{LL} \tag{3.20}$$

By using the definition of rms current and the waveform produced by the three-

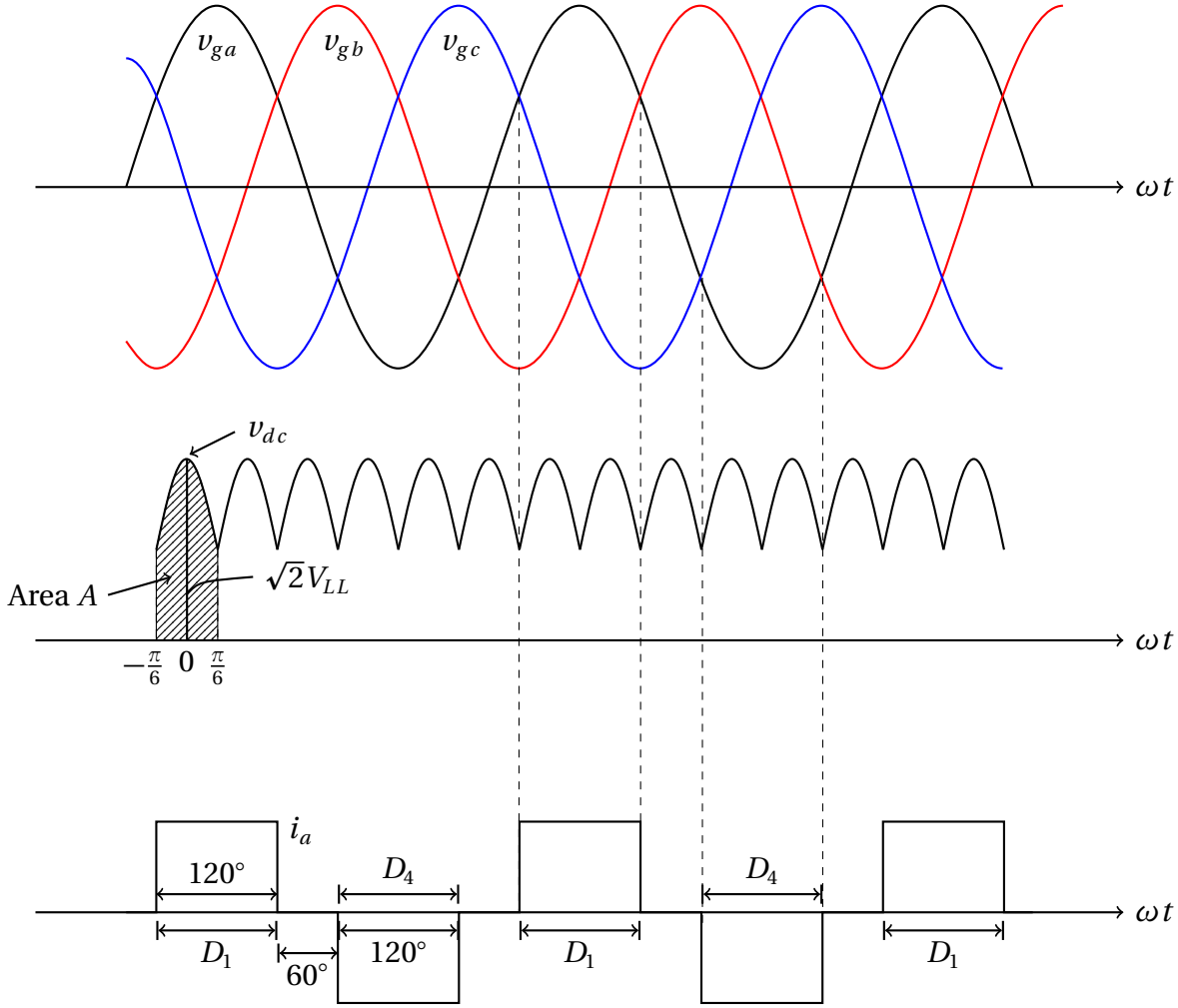


Figure 8: Waveform for the circuit in figure 7. Note that the diode D1 in phase a stops to conduct when phase voltage v_{gb} is greater than v_{ga}. Also note that diode D4 stops to conduct when v_{ga} is greater than v_{gb}.

phase bridge, the phase current is

$$I_s = \sqrt{\frac{1}{\pi}\int_{\frac{\pi}{3}}^{\pi} I_{dc}^2 \, d(\omega t)} = \sqrt{\frac{2}{3}} I_{dc} = 0.816 I_{dc} \qquad \text{where } s \in \{a, b, c\} \tag{3.21}$$

The phase currents drawn from the utility grid are rich with harmonic components as illustrated in phase a in figure 8. To compute the fundamental frequency component I_{s1}, the Fourier series is calculated. The use of odd symmetry ($I_s(-t) = -I_s(t)$)

simplifies the calculation of the Fourier coefficients and is given by

$$a_0 = a_h = 0 \tag{3.22}$$

$$b_h = \frac{2}{\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I_{dc}\sin(h\omega t)\,d(\omega t) = -\frac{2I_{dc}}{h\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} -h\sin(h\omega t)\,d(\omega t) \tag{3.23}$$

$$= -\frac{2I_{dc}}{h\pi}(\cos(h\omega t))\Big|_{\frac{\pi}{6}}^{\frac{5\pi}{6}} = \begin{cases} 0 & \text{if } h = 2,3,4,6,8,9,10,12,14,15,\ldots \\ \frac{2\sqrt{3}}{h\pi} I_{dc} & \text{if } h = 1,5,7,11,13,\ldots \end{cases}$$

Therefore the Fourier series is expressed by

$$FI_{dc}(t) = \frac{2\sqrt{3}}{h\pi}\sum_{h=1,5,7,11,13,\ldots}^{\infty} I_{dc}\sin(h\omega t) \tag{3.24}$$

Thus the fundamental frequency component in rms terms yields

$$I_{s1} = \frac{2\sqrt{3}}{\pi} I_{dc}\sqrt{\frac{1}{\frac{5\pi}{6}-\frac{\pi}{6}}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} \sin^2(\omega t)\,d(\omega t)} = \frac{1}{\pi}\sqrt{6} I_{dc} \tag{3.25}$$

One major drawback with the diode rectifier are the harmonic content and is calculated from equation 3.6 and yields

$$\%THD_i = 100\cdot\frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} = 100\cdot\frac{\sqrt{\frac{2}{3}-\frac{6}{\pi^2}}}{\frac{\sqrt{6}}{\pi}} = 31.08\% \tag{3.26}$$

Another important quantity is the PF and is given by [14]

$$PF = \frac{I_{s1}}{I_s} DPF = \frac{I_{s1}}{I_s}\cos\phi = \frac{\frac{\sqrt{6}}{\pi} I_d}{\sqrt{\frac{2}{3}} I_d} = \frac{3}{\pi} = 0.955 \tag{3.27}$$

with the assumption that the phase angle ϕ between the utility voltage and the line current is zero.

3.2.2 Thyristor rectifier

In application, such as battery chargers, it is necessary to control the dc voltage from the rectifier. To control the power flow there are several ways to produce a controlled dc voltage from the rectifiers output. A line-frequency phase-controlled thyristor is one solution and is shown in figure 9. The rectifier consists of three thyristor pairs, namely T_1 T_2, T_3 T_4 and T_5 T_6. A thyristor pair begins or ceases to conduct depending on the line-frequency ac voltage and the control inputs.

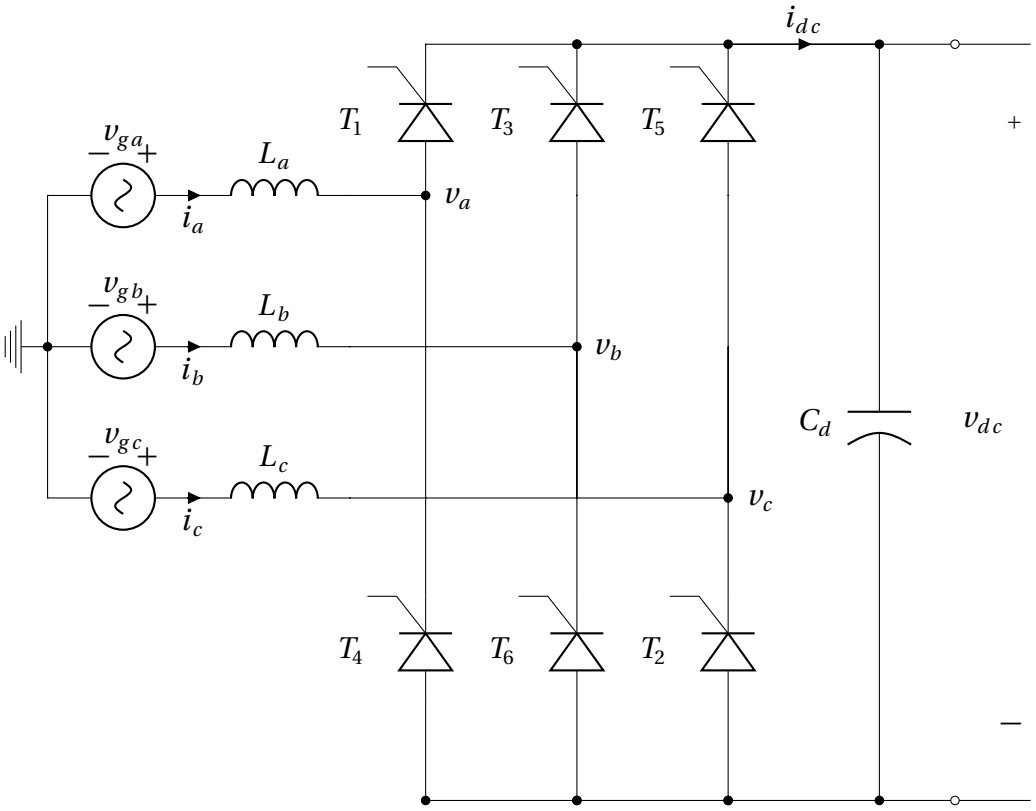


Figure 9: Three-phase full bridge thyristor rectifier. Adapted from [14].

To analyze the circuit, some simplifications are made where the line inductances $L_a = L_b = L_c = 0$ and assume that $i_{dc}(t) = I_{dc}$. The gate on each thyristor is controlled by the firing angle α. If $\alpha = 0°$ then the thyristor bridge has the same functionality as the diode rectifier in section 3.2.1 and the dc output voltage

$$v_{dc_o} = \frac{3\sqrt{2}}{\pi} V_{LL} = 1.35\, V_{LL} \tag{3.28}$$

When $\alpha > 0°$ some of the input ac voltage V_{LL} will be blocked and hence the output

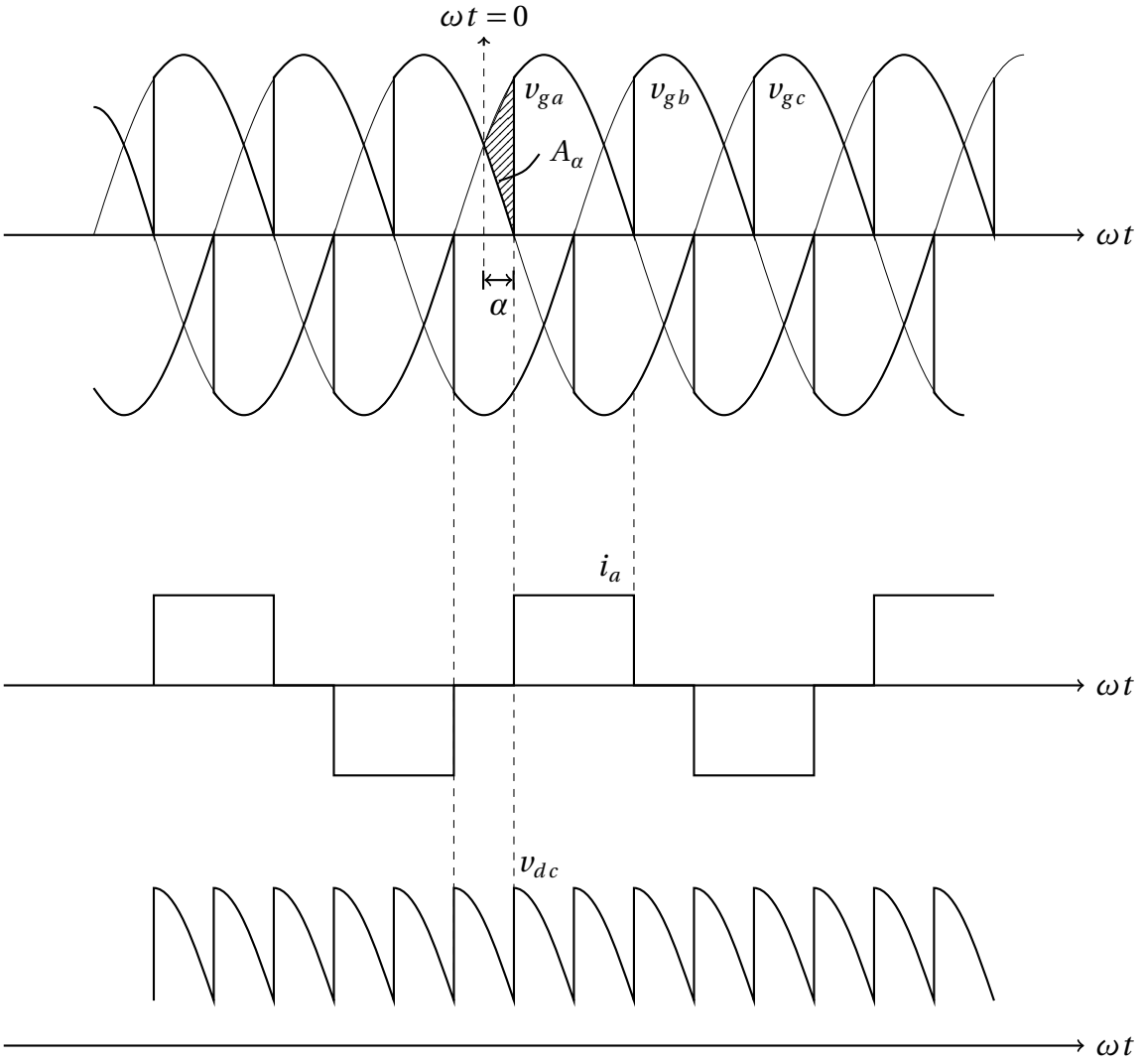


Figure 10: Waveform of the three-phase full bridge thyristor rectifier in figure 9. Note that the area A_α is blocked by the firing angle α. The phase difference between the phase current and the phase voltage is $\phi_1 = \alpha$.

voltage v_{dc} will decrease. Waveforms of the rectifier when $\alpha = 30°$ is shown in figure 10. The commutating process is delayed by the firing angle and the volt-second area A_α results in a reduction of the average dc output voltage by

$$v_{dc_\alpha} = v_{dc_0} - \frac{A_\alpha}{\pi/3} \tag{3.29}$$

The voltage reduction A_α happens every 60° and is given by the integral of $v_{an} - v_{cn} = v_{ac}$. Where

$$v_{ac} = \sqrt{2} V_{LL} \sin \omega t \tag{3.30}$$

Therefore,

$$A_\alpha = \int_0^\alpha \sqrt{2} V_{LL} \sin \omega t \, d(\omega t) = \sqrt{2} V_{LL} (1 - \cos \alpha) \tag{3.31}$$

Combining equation 3.28 and 3.31 into 3.29 yields

$$v_{dc_\alpha} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos \alpha = 1.35 V_{LL} \cos \alpha \tag{3.32}$$

When $\alpha > 90°$ the average dc voltage becomes negative and the converter acts as an inverter. The thyristor bridge is called a two-quadrant converter since it can operate as a rectifier and an inverter. This is in contrast to the diode bridge that only functions as a rectifier. This will not be discussed further.

From Fourier analysis the harmonic components is calculated from figure 10. Note that i_a is symmetric around the ωt-axis, thus simplifying the calculations. The Fourier coefficients are expressed as

$$a_0 = a_h = 0 \tag{3.33}$$

$$b_h = \frac{2}{\pi} \int_{\frac{\pi}{6}+\alpha}^{\frac{5\pi}{6}+\alpha} I_{dc} \sin(h\omega t - \alpha) \, d(\omega t) = -\frac{2I_{dc}}{h\pi} \int_{\frac{\pi}{6}+\alpha}^{\frac{5\pi}{6}+\alpha} -h \sin(h\omega t - \alpha) \, d(\omega t) \tag{3.34}$$

$$= -\frac{2I_{dc}}{h\pi} (\cos(h\omega t - \alpha)) \Big|_{\frac{\pi}{6}+\alpha}^{\frac{5\pi}{6}+\alpha} = \begin{cases} 0 & \text{if } h = 2,3,4,6,8,9,10,12,14,15,\ldots \\ \frac{2\sqrt{3}}{h\pi} I_{dc} & \text{if } h = 1,5,7,11,13,\ldots \end{cases}$$

Therefore the Fourier series is expressed by

$$F I_{dc}(t) = \frac{2\sqrt{3}}{h\pi} \sum_{h=1,5,7,11,13,\ldots}^{\infty} I_{dc} \sin(h\omega t - \alpha) \tag{3.35}$$

Similar for the diode rectifier the fundamental frequency component in rms terms yields

$$I_{s1} = \frac{2\sqrt{3}}{\pi} I_{dc} \sqrt{\frac{1}{\frac{5\pi}{6} + \alpha - \frac{\pi}{6} - \alpha} \int_{\frac{\pi}{6}+\alpha}^{\frac{5\pi}{6}+\alpha} \sin^2(\omega t - \alpha) \, d(\omega t)} = \frac{1}{\pi} \sqrt{6} I_{dc} \tag{3.36}$$

The phase current and the THD yields the same result as the diode rectifier and hence

$$I_s = \sqrt{\frac{2}{3}} I_{dc} \tag{3.37}$$

$$\%THD_i = 31.08\% \tag{3.38}$$

Furthermore the phase difference between the phase voltage and the phase current $\phi_1 = \alpha$ in figure 10. Hence the PF is calculated as

$$PF = \frac{I_{s1}}{I_s} \cos\phi_1 = \frac{3}{\pi} \cos\alpha = 0.955 \cos\alpha \tag{3.39}$$

Another important aspect is how much average power the thyristor converter can deliver to the load and is given by

$$P = \frac{1}{T} \int_0^T p(t)\, dt = \frac{1}{T} \int_0^T v_{dc}\, i_{dc}\, dt \tag{3.40}$$

Assuming $i_{dc}(t) = I_{dc}$ yields

$$P = I_{dc} \left(\frac{1}{T} \int_0^T v_{dc}\, dt \right) = V_{dc} I_{dc} = 1.35 V_{LL} I_{dc} \cos\alpha \tag{3.41}$$

The fundamental reactive power component drawn from the thyristor converter is expressed as

$$Q = 1.35 V_{LL} I_{dc} \sin\alpha \tag{3.42}$$

3.2.3 Active Front End rectifier

As briefly discussed in section 3.2.1 and 3.2.2 the rectifier schemes draw a highly distorted current from the utility grid. This is off course undesirable and can be improved in different ways. One solution is to install passive filters to filter out the low and high order harmonics. Nevertheless this makes the system bulky and costly. A more elegant solution is to install rectifiers with active filter techniques such as pulse with modulation (PWM) rectifiers. A basic circuit of a three-phase

PWM rectifier, called Active Front End (AFE) in this text, is shown in figure 11.

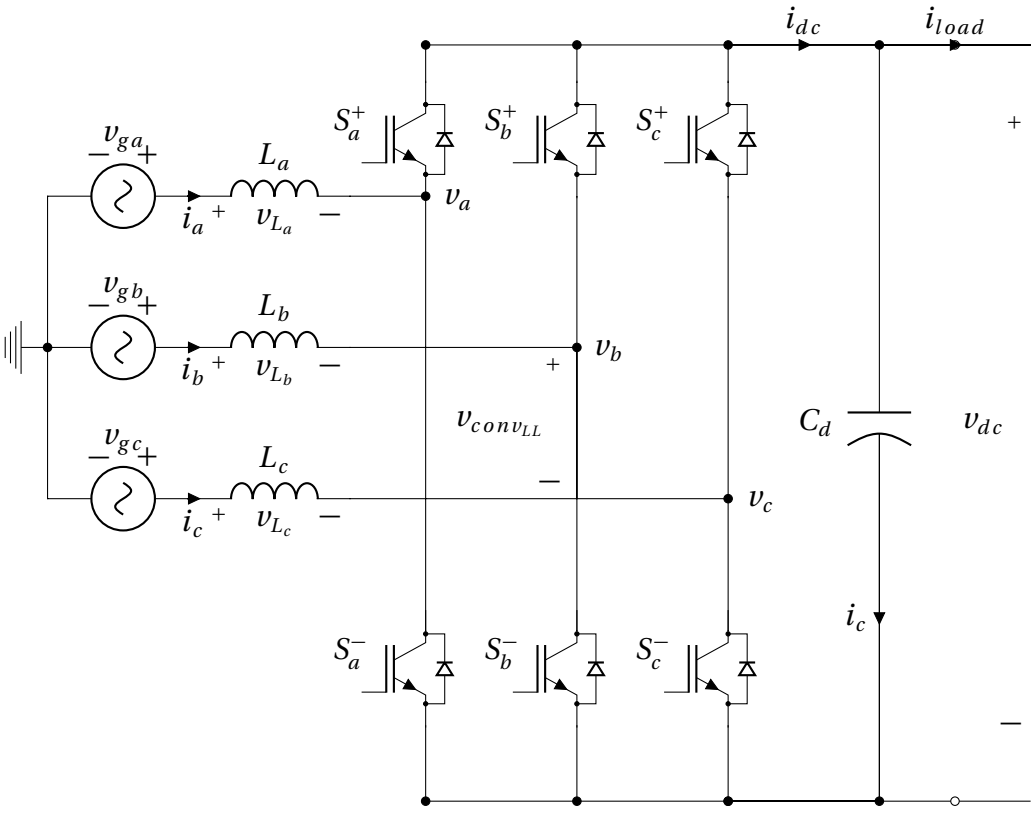


Figure 11: Three-phase Active Front End rectifier. Adapted from [14].

Each leg consists of two insulated gate bipolar transistors (IGBT), S_a^+ and S_a^- for phase a. Each IGBT is connected in anti-parallel with a flyback diode. The capacitor C_d reduces the ripple content of the output dc voltage v_{dc} and the inductors L_a, L_b and L_c represent the line inductances. The switching frequencies of the IGBTs are several kHz and therefore the voltages over an inductive load $v_L = L\frac{di}{dt}$ will become large and the potential difference between the IGBTs and the inductor will produce a voltage spike. To eliminate this problem the flyback diodes give the current i_{dc} a return path and therefore protect the IGBTs from destruction.

The voltage and current equations from figure 11 (assuming $L_a = L_b = L_c = L$) are derived from Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) and is expressed by

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_b \end{bmatrix} \tag{3.43}$$

$$C\frac{d_{v_{dc}}}{dt} = (S_a i_a + S_b i_b + S_c i_c) - i_{load} \tag{3.44}$$

S_a, S_b and S_c are the duty cycle for its respective phase. The phasor diagram for phase a is given by figure 12a, where the fundamental component of the phase current $\mathbf{i_{a_1}}$ lags the source voltage $\mathbf{v_{ga}}$ with an arbitrary angle ϕ. Switching frequency harmonics is neglected for simplicity. The net real power P supplied to the converter from the three-phase ac source is expressed by (assuming balanced supply)

$$P = 3\mathbf{v_{ga}}\mathbf{I_{a_1}}\cos\phi = 3\frac{\mathbf{v_{ga}}^2}{\omega L}\left(\frac{\mathbf{v_a}}{\mathbf{v_{ga}}}\sin\delta\right) \tag{3.45}$$

Similar from figure 12a, the net imaginary reactive power Q supplied to the converter from the three-phase ac source is

$$Q = 3\mathbf{v_{ga}}\mathbf{I_{a_1}}\sin\phi = 3\frac{\mathbf{v_{ga}}^2}{\omega L}\left(1-\frac{\mathbf{v_a}}{\mathbf{v_{ga}}}\cos\delta\right) \tag{3.46}$$

To control the supply of net power S ($S = P + jQ$) to the converter, phase voltages $\mathbf{v_a}$, $\mathbf{v_b}$ and $\mathbf{v_c}$ has to be controlled in both magnitude and phase angle δ. Operating the converter in rectifying mode, it is often desired to achieve UPF as seen in figure 12b.

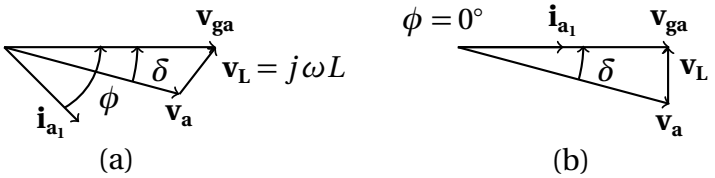


Figure 12: For phase a; (a) general phasor diagram; (b) rectifier at UPF

The dc output voltage v_{dc} is an important parameter and is regulated by the duty cycle of each IGBT switch. The switching scheme of the IGBTs can be quite complex and will be discussed in section 3.3.

3.2.4 Choosing the rectifier topology

There are several different rectifier solution that also could be considered. A particular interesting one is the Vienna rectifier. It is a three-level rectifier with the capability of PF correction and reduced switching losses [15]. However, due to limited time in this project the Vienna rectifier will not be presented in detail. The advantages and disadvantages for the rectifiers in section 3.2.1, 3.2.2, 3.2.3 and the Vienna rectifier are shown in table 3.

Table 3: Features for the different rectifier topologies discussed in this thesis.

Rectifier	Harmonic distortion	Controllable dc voltage	Power factor	Bi-directional power flow
Diode	High	No	Low	No
Thyristor	High	Yes	Low	No
AFE	Low	Yes	High	Yes
Vienna	Low	Yes	High	No

A practical diode and thyristor rectifier have a very poor PF due to the line current being far from sinusoidal and hence the need for filters is increased [14]. The Vienna and AFE rectifier on the other hand draws almost perfectly sinusoidal currents from the utility grid if the rectifier system is designed properly. It is also possible to achieve UPF with these systems. However only the AFE rectifier is capable to utilize bi-directional power flow and can be used as a static compensator (STATCOM). This can be favorable if the PF at the PCC is low and thus the STATCOM delivers reactive power back to the grid. Furthermore the reactive power contributes maintaining the grid voltage level at the PCC. Therefore were the AFE rectifier topology chosen for the ferry charger solutions.

3.3 Control of rectifiers

To control the switching scheme of the two-level AFE rectifier in figure 11 several techniques are discussed in the literature [16–20] . The IGBT switches are controlled in an on/off fashion and therefore the switch-mode rectifier is a descriptive term. However, in this text the switch-mode rectifier is called AFE rectifier. The basic conversion method applied for AFE rectifiers is PWM techniques. Historically one of the best known methods is carrier based PWM (CB-PWM). This technique is shown in figure 13.

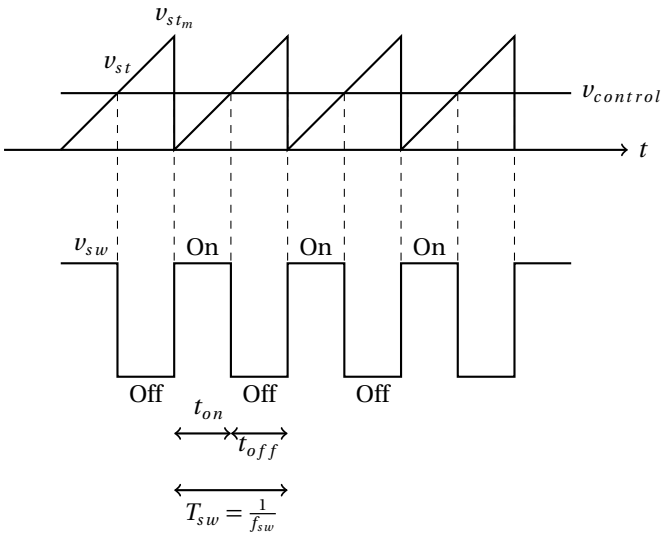


Figure 13: The control signal $v_{control}$ is compared to the sawtooth signal v_{st} and yields a digital output signal v_{sw} to the gate of the IGBTs. Adapted from [14].

The sawtooth signal v_{st} is compared with the control signal $v_{control}$. From the waveform it can be seen that the switch control signal v_{sw} is either on or off by the following expressions

$$v_{control} \geq v_{st} \qquad v_{sw} = 1 \tag{3.47}$$

$$v_{control} < v_{st} \qquad v_{sw} = 0 \tag{3.48}$$

To control phase a,b and c it requires three control signals which again sets the switch position of the IGBTs in relation to

$$v_{control_u} \geq v_{st} \qquad S_u^+ = 1 \qquad u \in \{a,b,c\} \tag{3.49}$$

$$v_{control_u} < v_{st} \qquad S_u^+ = 0 \tag{3.50}$$

Furthermore is S_u^+ always complementary according to S_u^-. Some important definitions and parameters have to be defined, which characterizes PWM methods:

$$m_a = \frac{v_{control}}{v_{st_m}} \tag{3.51}$$

$$m_f = \frac{f_{sw}}{f_1} \tag{3.52}$$

m_a is the modulation index and for sinusoidal modulation $0 < m_a < 1$. m_f is the

frequency modulation, f_{sw} is the switching frequency and f_1 is the frequency for the control signal $v_{control}$. The switching frequency f_{sw} is kept constant and is normally chosen to span from a few kilohertz to few hundred kilohertz [14]. The duty cycle is calculated from figure 13 and is expressed as

$$D_s = \frac{t_{on}}{T_s} = \frac{v_{control}}{v_{st}} \tag{3.53}$$

Today's basic power processing technique uses space vector pulse with modulation (SVPWM) after advances in microprocessing developments [21]. Several rectifier systems use SVPWM, such as voltage oriented control (VOC) and virtual flux oriented control (VFOC). Other control techniques such as direct power control (DPC) and virtual flux power control (VF-DPC), use switching tables but have several similarities to VOC and VFOC. After the work done by M. Malinowski in [22], was it decided to control the rectifier for the ferry charger with VOC. To fully understand VOC, transformation techniques and SVPWM are presented respectively in section 3.3.1 and 3.3.2.

3.3.1 Clarke and Park transformation

Several of the PWM techniques in the literature measure the phase voltages and/or the line currents from the utility grid. These quantities are controlled against set values to ensure that the dc output voltage from the rectifier is at the desired range. To ease the control system the ac values is transformed to dc values. The transformation can be done in two separated transformations named Clarke and Park transformation [23, 24]. The ac voltages and currents from the utility grid are illus-

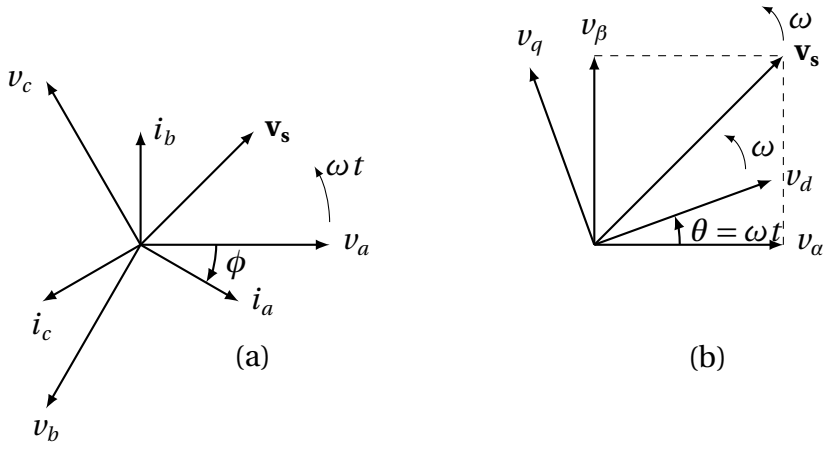


Figure 14: (a) Phase voltages and line currents in a three-phase stationary reference frame; (b) Phase voltages in a two-phase stationary reference frame compared to synchronously rotating reference frame.

trated in figure 14 (a) and are defined as

$$v_a = V_m \sin(\omega t) \tag{3.54}$$

$$v_b = V_m \sin(\omega t - \frac{2\pi}{3}) \tag{3.55}$$

$$v_c = V_m \sin(\omega t + \frac{2\pi}{3}) \tag{3.56}$$

$$i_a = I_m \sin(\omega t + \phi) \tag{3.57}$$

$$i_b = I_m \sin(\omega t - \frac{2\pi}{3} + \phi) \tag{3.58}$$

$$i_c = I_m \sin(\omega t + \frac{2\pi}{3} + \phi) \tag{3.59}$$

where V_m and I_m are the amplitude value of the phase voltages and line currents. Instead of representing the line currents and the phase voltages in a three-phase stationary reference frame, can it be transformed to a two-phase stationary reference frame, α and β also called the Clarke transformation. Only the transformation for the voltage components will be derived, but the procedure for the line currents derivation is the same. First the term space vector is defined as

$$\mathbf{v_s} = \frac{2}{3}\left(v_a + v_b e^{\frac{j2\pi}{3}} + v_c e^{\frac{j4\pi}{3}}\right) = v_s e^{j\theta} \tag{3.60}$$

The Clarke transform is directly related to the space vector and is defined as

$$\mathbf{v}_{\alpha\beta} = v_\alpha + j\, v_\beta = \mathbf{v_s} \tag{3.61}$$

where the subscripts α and β are the real and imaginary part of the complex number and are given by

$$v_\alpha = \frac{2}{3}\left(v_a - \frac{1}{2}(v_b + v_c) \right) \tag{3.62}$$

$$v_\beta = \frac{2}{3}\left(0 + \frac{\sqrt{3}}{2}(v_b - v_c) \right) \tag{3.63}$$

The space vector is rotating with an angular velocity ω in a stationary reference frame as shown in figure 14 (b). It is convenient to transform the stationary reference frame to the rotating space vector in a synchronously rotating reference frame with an angular velocity ω. This results in that both the space vector and the reference frame rotates with the same angular velocity. The foregoing discussion is called the Park transform and is expressed as

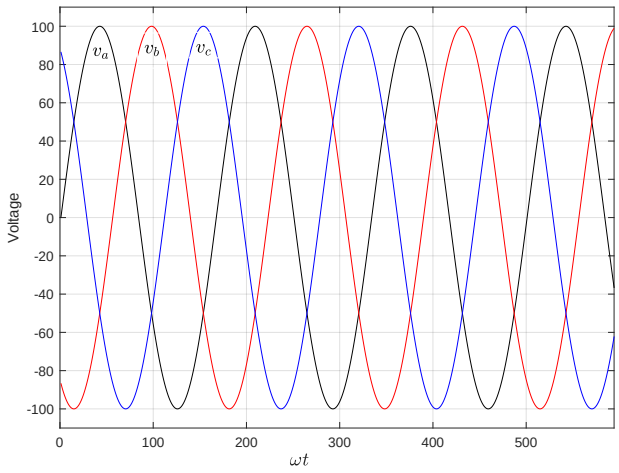
$$\mathbf{v_s} e^{-j\left(\omega t - \frac{\pi}{2}\right)} = \mathbf{v_{dq}} = v_d + j\, v_q \tag{3.64}$$

where the real and imaginary part are expressed as

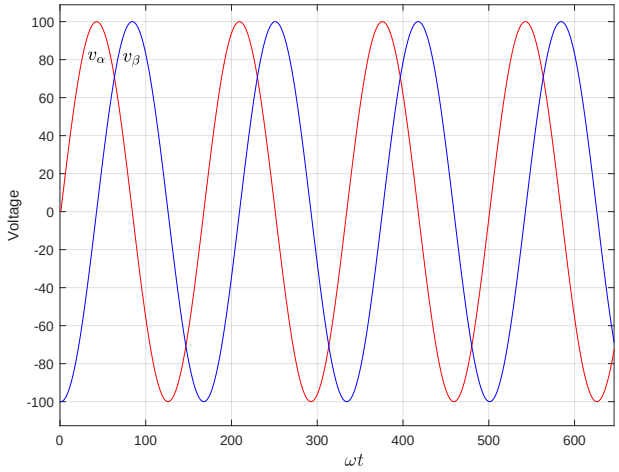
$$v_d = v_\alpha \sin\theta + v_\beta \cos\theta \tag{3.65}$$

$$v_q = -\, v_\alpha \cos\theta + v_\beta \sin\theta \tag{3.66}$$

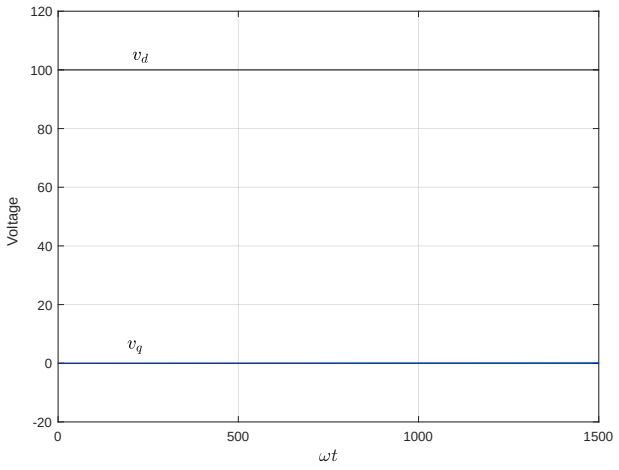
To clarify the foregoing discussion, the waveforms for $v_a, v_b, v_c, v_\alpha, v_\beta, v_d$ and v_q are plotted in figure 15. For more detailed derivation see appendix A.



(a) Three-phase ac voltages v_a, v_b and v_c as a function of ωt.



(b) Two-phase ac voltages v_α and v_β. Note that v_β is lagging 90° in respect to v_α



(c) Dc voltages v_d and v_q in a synchronous rotating reference frame. Note that v_q is zero.

Figure 15: The effect of Clarke and Park transformation on a three-phase voltage source.

3.3.2 Space vector modulation

To achieve stable dc output voltage V_{dc} at a desired PF has the control system to be reliable. Before describing complete solutions for the VOC system in section 4.1, is SVPWM discussed in detail.

The gate terminal of the IGBTs in figure 11 receives switching commands from the space vector modulator. The principle of SVPWM is to create a reference vector $\mathbf{V}^*$ in compliance with the difference or error signal between measured values on the ac side and the dc side of the rectifier. The error signal can for example be the phase currents i_d and i_q from the utility grid compared with the reference currents i_d^* and i_q^* set by the control system.

The switching states for the IGBTs are constricted to eight unique combinations. This is to ensure that the input lines cannot be shorted and continuous current flow is maintained. Each switching combination is illustrated as a vectors in figure 16. The $a\,b\,c$ three-phase reference frame is transformed to the α and β reference frame by equation 3.62 and 3.63. The plane is given by six active vectors $\mathbf{V_1}$, $\mathbf{V_2}$,...,$\mathbf{V_6}$ and two zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$ [25].

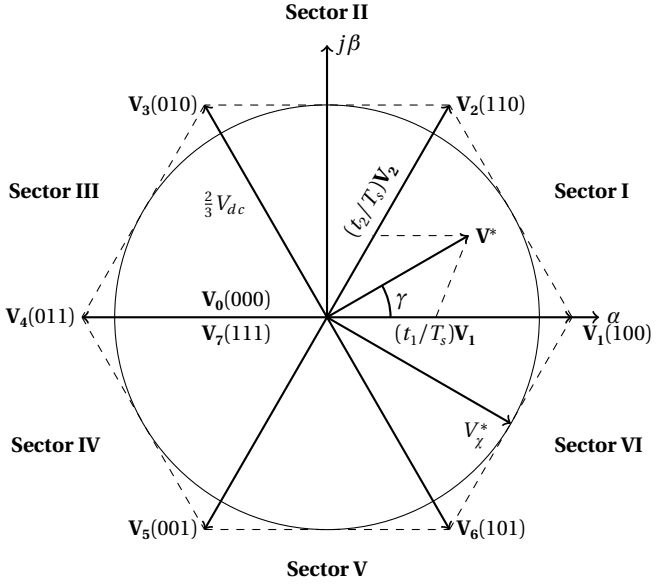


Figure 16: Space vector representation given by six active vectors and two zero vectors. Adapted from [21].

The active vector divide the plane in six sectors, where the reference vector $\mathbf{V}^*$ is

obtained by two adjacent vectors. To control the magnitude of $\mathbf{V}^*$, proper duty cycles are required for both the active adjacent vectors and the two zero vectors. The switching scheme for symmetrical modulation will be explained further in this text. The key advantages with this method is lower THD, due to the use of both zero vectors. The disadvantages is more switching losses compared to asymmetric modulation that only uses one zero vector, but also generate more THD. The general switching scheme with phase voltages and line voltages is shown in table 4. The phase voltages are calculated according to

$$V_{dc}\left(v_\alpha \cos\gamma + v_\beta \sin\gamma\right) = \tag{3.67}$$
$$V_{dc}\left[\cos\gamma\left(\frac{2}{3}v_a - \frac{1}{3}v_b - \frac{1}{3}v_c\right) + \sin\gamma\left(\frac{1}{\sqrt{3}}v_b - \frac{1}{\sqrt{3}}v_c\right)\right]$$

where γ is the angle referred to the α-axis in figure 16. For symmetrical modulation

Table 4: Switching table for SVPWM. Note that the switches in each rectifier branch are complementary of each other. Adapted from [25].

Vector	S_a^+	S_b^+	S_c^+	S_a^-	S_b^-	S_c^-	v_a	v_b	v_c	v_{ab}	v_{bc}	v_{ca}
$\mathbf{V_0}=(\mathbf{000})$	off	off	off	on	on	on	0	0	0	0	0	0
$\mathbf{V_1}=(\mathbf{100})$	on	off	off	off	on	on	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	V_{dc}	0	$-V_{dc}$
$\mathbf{V_2}=(\mathbf{110})$	on	on	off	off	off	on	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0	V_{dc}	$-V_{dc}$
$\mathbf{V_3}=(\mathbf{010})$	off	on	off	on	off	on	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-V_{dc}$	V_{dc}	0
$\mathbf{V_4}=(\mathbf{011})$	off	on	on	on	off	off	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-V_{dc}$	0	V_{dc}
$\mathbf{V_5}=(\mathbf{001})$	off	off	on	on	on	off	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	0	$-V_{dc}$	V_{dc}
$\mathbf{V_6}=(\mathbf{101})$	on	off	on	off	on	off	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	V_{dc}	$-V_{dc}$	0
$\mathbf{V_7}=(\mathbf{111})$	on	on	on	off	off	off	0	0	0	0	0	0

let's consider the reference vector $\mathbf{V}^*$ in figure 16. To determine the switching time duration of sector **I**, the reference vector is decomposed and multiplied with a given duty cycle according to

$$\int_0^{T_s} \mathbf{V}^*\,dt = \int_0^{t_0} \mathbf{V_0}\,dt + \int_{t_0}^{t_0+t_1} \mathbf{V_1}\,dt + \int_{t_0+t_1}^{t_0+t_1+t_2} \mathbf{V_2}\,dt + \int_{t_0+t_1+t_2}^{T_s} \mathbf{V_7}\,dt \tag{3.68}$$

$$\mathbf{V}^* = \mathbf{V_0}\frac{t_0}{T_s} + \mathbf{V_1}\frac{t_1}{T_s} + \mathbf{V_2}\frac{t_2}{T_s} + \mathbf{V_7}\frac{t_7}{T_s} = \mathbf{V_1}\frac{t_1}{T_s} + \mathbf{V_2}\frac{t_2}{T_s} \tag{3.69}$$

t_1, t_2, t_0 and t_7 are the time each respective switch is turned on and T_s is the switching time period. To determine the duty cycles, $|\mathbf{V_1}|$ and $|\mathbf{V_2}|$ has to be calculated

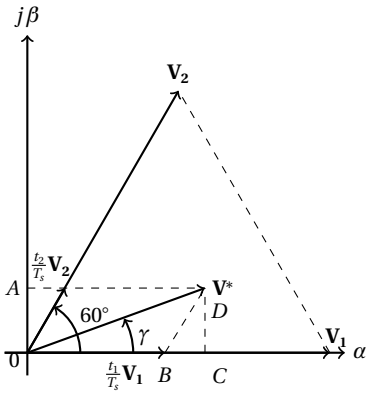


Figure 17: Adjacent boundary vectors in sector **I**.

first. Sector **I** is enhanced in figure 17 and the length of the reference vector $|\mathbf{V}^*|$ is decomposed by

$$\begin{aligned}\frac{t_1}{T_s}|\mathbf{V_1}| &= |\mathbf{V}^*|\cos\gamma - BC = |\mathbf{V}^*|\cos\gamma - DC\tan 30^\circ \qquad (3.70)\\ &= |\mathbf{V}^*|\cos\gamma - |\mathbf{V}^*|\sin\gamma\tan 30^\circ\\ &= |\mathbf{V}^*|(\cos\gamma - \frac{1}{\sqrt{3}}\sin\gamma) = \frac{2}{\sqrt{3}}|\mathbf{V}^*|(\sin 60^\circ\cos\gamma - \cos 60^\circ\sin\gamma)\\ &= \frac{2}{\sqrt{3}}|\mathbf{V}^*|\sin(60^\circ-\gamma)\\ \frac{t_2}{T_s}|\mathbf{V_2}| &= \frac{AO}{\cos 30^\circ} = \frac{2}{\sqrt{3}}|\mathbf{V}^*|\sin\gamma \qquad (3.71)\end{aligned}$$

The switching time for $\mathbf{V_1}$ and $\mathbf{V_2}$ are therefore given by

$$t_1 = \sqrt{3}T_s m_a \sin(60^\circ-\gamma) \qquad (3.72)$$

$$t_2 = \sqrt{3}T_s m_a \sin(\gamma) \qquad (3.73)$$

since $|\mathbf{V_1}| = |\mathbf{V_2}| = \frac{2}{3}V_{dc}$ and $m_a = \frac{|\mathbf{V}^*|}{V_{dc}}$. The angle γ in sector **I** is restricted by $\gamma \in [0^\circ,\ldots,60^\circ]$.

The switching pattern of $\mathbf{V}^*$ in sector **I** is shown in figure 18. The two zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$ are included to reduce THD and the magnitude of $\mathbf{V}^*$.

In principle, the generation of reference vectors in the five other sectors are much

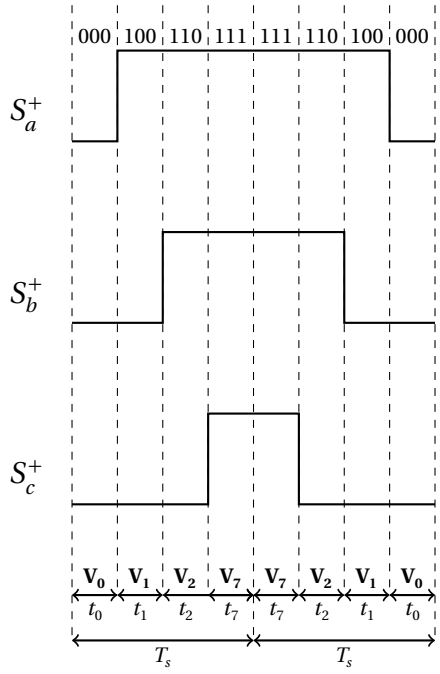


Figure 18: Pulse pattern of vectors in sector **I**. After the first switching period T_s is completed, the switching combination is reversed. Adapted from [25].

alike. The active voltage vectors are given by

$$\mathbf{V_k^*} = \begin{cases} \frac{2}{3} V_s e^{j(k-1)\frac{\pi}{3}} & \text{if } k = 1,2,\ldots,6 \\ 0 & \text{if } k = 0 \text{ or } k = 7 \end{cases} \tag{3.74}$$

The angle γ between the adjacent vectors $\mathbf{V}_k$ and $\mathbf{V}_{k+1}$ in sector k is calculated by

$$\gamma = \arctan\left(\frac{V_\beta}{V_\alpha}\right) \tag{3.75}$$

and the magnitude of the voltage vector

$$|\mathbf{V}^*| = \sqrt{V_\alpha^2 + V_\beta^2} \tag{3.76}$$

V_α and V_β are calculated by the control system and will be discussed in section 4.1. The duration of t_1 and t_2 are generally expressed by

$$t_1 = \sqrt{3} T_s m_a \sin(k60^\circ - \gamma) \tag{3.77}$$

$$t_2 = \sqrt{3} T_s m_a \sin(\gamma - k60^\circ) \tag{3.78}$$

Calculation of t_0 and t_7 are given by

$$t_0 = t_7 = \frac{T_s - t_1 - t_2}{2} \tag{3.79}$$

The switching time for each sector is given in table 5 [25].

Table 5: Switching times for sector **I** to **VI**.

Sector	Switches branch a	Switches branch b	Switches branch c
I	$S_a^+ = t_1 + t_2 + \frac{t_0}{2}$ $S_a^- = \frac{t_0}{2}$	$S_b^+ = t_2 + \frac{t_0}{2}$ $S_b^- = t_1 + \frac{t_0}{2}$	$S_c^+ = \frac{t_0}{2}$ $S_c^- = t_1 + t_2 + \frac{t_0}{2}$
II	$S_a^+ = t_1 + \frac{t_0}{2}$ $S_a^- = t_2 + \frac{t_0}{2}$	$S_b^+ = t_2 + \frac{t_0}{2}$ $S_b^- = \frac{t_0}{2}$	$S_c^+ = \frac{t_0}{2}$ $S_c^- = t_1 + t_2 + \frac{t_0}{2}$
III	$S_a^+ = \frac{t_0}{2}$ $S_a^- = t_1 + t_2 + \frac{t_0}{2}$	$S_b^+ = t_1 + t_2 + \frac{t_0}{2}$ $S_b^- = \frac{t_0}{2}$	$S_c^+ = t_2 + \frac{t_0}{2}$ $S_c^- = t_1 + \frac{t_0}{2}$
IV	$S_a^+ = \frac{t_0}{2}$ $S_a^- = t_1 + t_2 + \frac{t_0}{2}$	$S_b^+ = t_1 + \frac{t_0}{2}$ $S_b^- = t_2 + \frac{t_0}{2}$	$S_c^+ = t_1 + t_2 + \frac{t_0}{2}$ $S_c^- = \frac{t_0}{2}$
V	$S_a^+ = t_2 + \frac{t_0}{2}$ $S_a^- = t_1 + \frac{t_0}{2}$	$S_b^+ = \frac{t_0}{2}$ $S_b^- = t_1 + t_2 + \frac{t_0}{2}$	$S_c^+ = t_1 + t_2 + \frac{t_0}{2}$ $S_c^- = \frac{t_0}{2}$
VI	$S_a^+ = t_1 + t_2 + \frac{t_0}{2}$ $S_a^- = \frac{t_0}{2}$	$S_b^+ = \frac{t_0}{2}$ $S_b^- = t_1 + t_2 + \frac{t_0}{2}$	$S_c^+ = t_1 + \frac{t_0}{2}$ $S_c^- = t_1 + \frac{t_0}{2}$

The maximum amplitude of the reference vector before overmodulation mode is restricted by the radius of the circle in figure 16 and is expressed by

$$V_\chi^* = \frac{2}{3} V_{dc} \cos 30^\circ = \frac{V_{dc}}{\sqrt{3}} \tag{3.80}$$

Exceeding V_χ^* causes overmodulation and will not be discussed further.

4 Design of the onboard rectifier system

The design of the onboard charging system is limited to the design of an AFE rectifier system with UPF consideration. To satisfy the demands from BKK in regards to the voltage quality, the design must satisfy the limits in table 2. Voltage drops must not increase beyond the demand mentioned in supply safety regulation [4] and in section 1.1. From the ferry owner perspective the demand for high efficiency and UPF is also taken in consideration. This section explains two different AFE rectifier systems based on VOC with L-filter and LCL-filter design.

4.1 Voltage orientated control

VOC is based on the transformation from a three-phase stationary reference frame to a synchronously rotating reference frame. The block scheme for the VOC AFE rectifier system is illustrated in figure 19. The grid currents (i_{ga},i_{gb},i_{gc}) and voltages (v_{ga},v_{gb},v_{gc}) are measured and transformed to dc values according to the Clarke and Park transformation explained in section 3.3.1. To obtain correct angular position ωt is a phase lock loop (PLL) implemented. If the grid experiences frequency deviations from nominal value (50Hz), regulates the PLL ωt according to the deviation. Dc voltage v_{dc} is measured on the dc side of the rectifier and is fed to the controller with the grid side values included a reference value for the dc voltage $v_{dc_{ref}}$. The controller's outputs v_{rd} and v_{rq} are transformed to a two-phase stationary reference system explained in section 3.3.1. $v_{r\alpha}$ and $v_{r\beta}$ is fed to the SVPWM module which generates switching signals to the IGBTs.

The mathematical model from the block scheme in figure 19 are derived from KVL and KCL and are expressed as

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + \begin{bmatrix} v_{ra} \\ v_{rb} \\ v_{rc} \end{bmatrix} \tag{4.1}$$

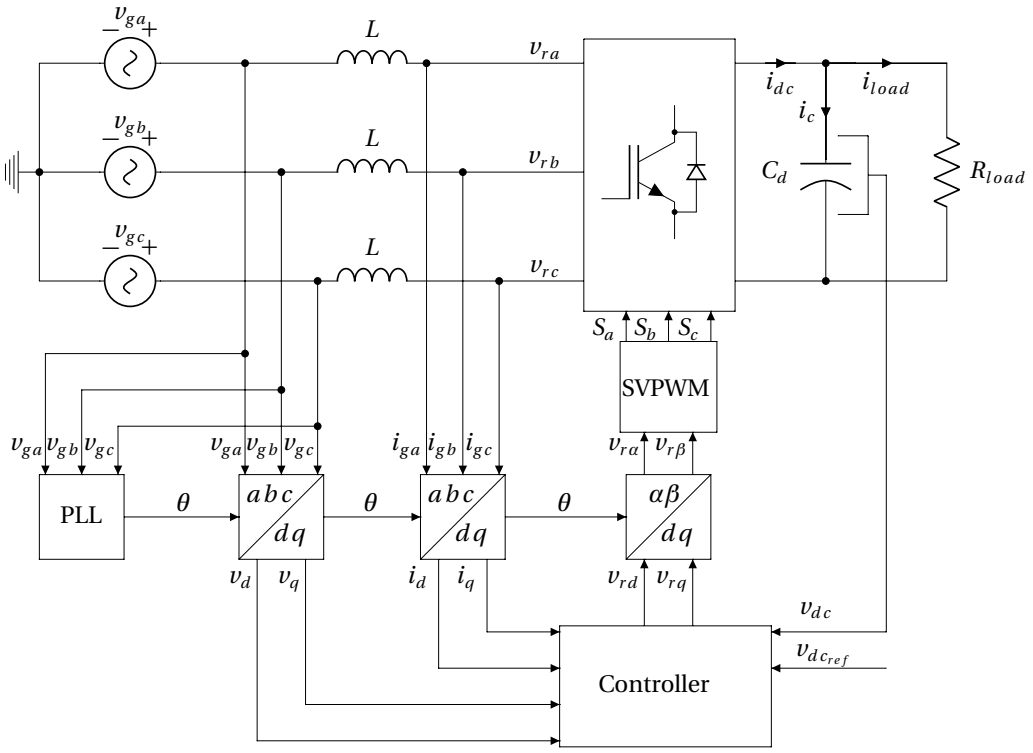


Figure 19: Configuration of VOC AFE rectifier with L-filter. The controller is described in detail in figure 20. Adapted from [21].

$$C\frac{d_{v_{dc}}}{dt} = (S_a i_{ga} + S_b i_{gb} + S_c i_{gc}) - i_{load} \tag{4.2}$$

where S_a, S_b and S_c are the switching signal to the gate terminal on each IGBT branch. The switching signal is either one or zero. Equation 4.1 and 4.2 can be transformed by the Clarke transform described in equation 3.62-3.63 and thus yielding

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} v_{r\alpha} \\ v_{r\beta} \end{bmatrix} \tag{4.3}$$

$$C\frac{d_{v_{dc}}}{dt} = \frac{3}{2}(S_\alpha i_\alpha + S_\beta i_\beta) - i_{load} \tag{4.4}$$

To ease the control system, the sinusoidal voltages and currents from the grid are converted to dc values according to the Park transform given by equation 3.65 and

thus

$$\mathbf{v_{dq}} = \mathbf{v_s} e^{-j(\omega t - \frac{\pi}{2})} = (v_\alpha + j v_\beta) e^{-j(\omega t - \frac{\pi}{2})} \tag{4.5}$$

$$\mathbf{v_{dq}} = L \frac{d}{dt}(i_\alpha + j i_\beta) e^{-j(\omega t - \frac{\pi}{2})} + (v_{r\alpha} + j v_{r\beta}) e^{-j(\omega t - \frac{\pi}{2})}$$

$$\mathbf{v_{dq}} = L\Big[e^{-j(\omega t - \frac{\pi}{2})}\big((-j\omega)(i_\alpha + j i_\beta) + \frac{d}{dt}(i_\alpha + j i_\beta)\big)\Big] + (v_{r\alpha} + j v_{r\beta}) e^{-j(\omega t - \frac{\pi}{2})}$$

$$\mathbf{v_{dq}} = L\Big[(j\omega)(i_d + j i_q) + \frac{d}{dt}(i_d + j i_q)\Big] + v_{rd} + j v_{rq}$$

$$C \frac{d_{v_{dc}}}{dt} = \frac{3}{2}(S_d i_d + S_q i_q) - i_{load} \tag{4.6}$$

The grid voltages v_d and v_q can be divided in a real and imaginary part and hence

$$v_d = \Re(\mathbf{v_{dq}}) = L \frac{d i_d}{dt} - \omega L i_q + v_{rd} \tag{4.7}$$

$$v_q = \Im(\mathbf{v_{dq}}) = L \frac{d i_q}{dt} + \omega L i_d + v_{rq} \tag{4.8}$$

From equation 4.7 and 4.8 a decoupled regulation system can be designed and is shown in figure 20. There is one outer voltage control loop that regulates the dc voltage v_{dc} on the dc busbar with a PI-controller. Moreover there are two inner current control loops which regulates the the active current i_d and reactive current i_q with their respective PI-controller. The output voltages from the controller are expressed as

$$v_{rd} = v_d + \omega L i_q - \Delta v_d \tag{4.9}$$

$$v_{rq} = v_q - \omega L i_d - \Delta v_q \tag{4.10}$$

and the error signals from the current controllers are given by

$$\Delta v_d = K_{p_1}(i_{d_{ref}} - i_d) + K_{i_1} \int_0^t (i_{d_{ref}} - i_d)\, dt \tag{4.11}$$

$$\Delta v_q = K_{p_1}(i_{q_{ref}} - i_q) + K_{i_1} \int_0^t (i_{q_{ref}} - i_q)\, dt \tag{4.12}$$

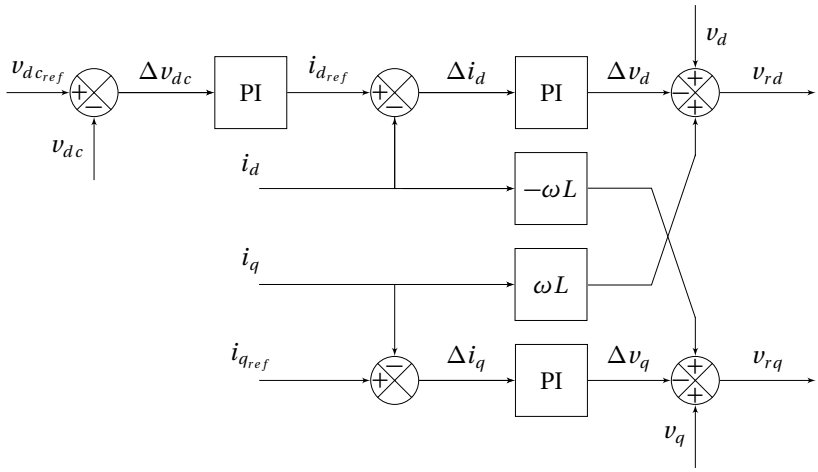


Figure 20: Synchronous controller working in dq coordinates for the VOC AFE rectifier as illustrated in figure 19. Note that there are one outer voltage control loop for the dc bus voltage and two inner current control loops for the active-and reactive current drawn from the utility grid. Adapted from [21].

The constants K_{p_1} and K_{i_1} are respectively the proportional and integration constants. The output from the voltage controller is expressed by

$$i_{d_{ref}} = K_{p_2}(v_{dc_{ref}} - v_{dc}) + K_{i_2}\int_0^t (v_{dc_{ref}} - v_{dc})\,dt \tag{4.13}$$

The parameters for the voltage controller are often set 5-29 times less sensitive to errors relative to the current controllers [26].

The tuning process for the PI-controllers parameters are according to standards rules as described in [21] page 120. There are two standard rules named modulus and symmetry criterion. However, the aforementioned rules are only valid under fast sampling conditions ($T_s \to 0$). The symmetry criterion is used when

$$\tau_L \gg \tau_0 \tag{4.14}$$

where τ_L is the time constant for the grid connected inductances. Furthermore τ_0 is the sum of the small time constants such as the power converter dead time, processing time of algorithm and delay of the feedback sampling time. The modulus

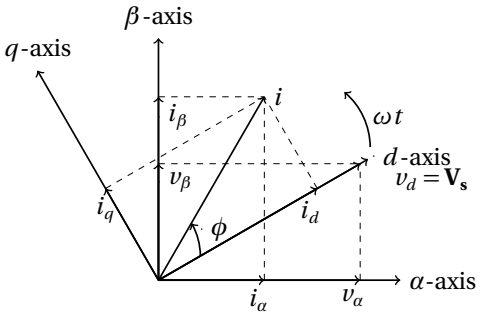


Figure 21: Vector diagram for the rectifier currents and the utility grid reference voltages in stationary and synchronous rotating reference frame. Note that $v_q = 0$ according to the definition from the Park transformation. Adapted from [21].

criterion should be used when

$$\tau_L \leq 4\tau_0 \tag{4.15}$$

However the tuning process according to symmetry and modulus criterion can only be used as broad indicators. Fine tuning with trial and error is therefore used further in this thesis.

To achieve UPF, the quadrature component i_q has to be equal to zero. The vector diagram for the measured grid voltages and grid currents are illustrated in figure 21. From the Park transformation in equation 3.64, the voltage space vector $\mathbf{V_s}$ is aligned to the direct-axis and hence the quadrature component equal to zero.

The active and reactive power drawn from the utility grid in space vector terms are given by

$$\begin{aligned} \mathbf{S_s} &= \mathbf{V_s}(\mathbf{I_s})^* \\ \mathbf{s_s} &= (v_\alpha + j\,v_\beta)(i_\alpha - j\,i_\beta) \\ \mathbf{s_s} &= v_\alpha i_\alpha - j\,v_\alpha i_\beta + j\,v_\beta i_\alpha + v_\beta i_\beta \end{aligned} \tag{4.16}$$

and the active power p_s and reactive power q_s are given by

$$p_s = \Re(\mathbf{s_s}) = v_\alpha i_\alpha + v_\beta i_\beta \tag{4.17}$$

$$q_s = \Im(\mathbf{s_s}) = v_\beta i_\alpha - v_\alpha i_\beta \tag{4.18}$$

The complex power in synchronous rotating reference frame terms is expressed as

$$\mathbf{S_{dq}} = V_d I_d - j V_d I_q + j V_q I_d + V_q I_q \tag{4.19}$$

and the active power P_{dq} and reactive power Q_{dq} are given by

$$P_{dq} = \Re(\mathbf{S_{dq}}) = V_d I_d + V_q I_q \tag{4.20}$$

$$Q_{dq} = \Im(\mathbf{S_{dq}}) = V_q I_d - V_d I_q \tag{4.21}$$

The relationship between the complex power in space vector terms and three-phase systems are given by

$$\frac{3}{2} p_s = v_a i_a + v_b i_b + v_c i_c = p \tag{4.22}$$

$$\frac{3}{2} q_s = \frac{1}{\sqrt{3}} [v_a (i_c - i_a) + v_b (i_a - i_c) + v_c (i_b - i_a)] = q \tag{4.23}$$

For derivation see appendix B.

4.1.1 L-filter design

The design of the line inductances is an optimization process considering the demands for low current ripple and operational range of the rectifier. With a large inductor the current ripple is low but the operation range is decreasing. The voltage drop across the grid side inductors controls the line currents. Furthermore the voltage drop is controlled by the rectifier voltage and is restricted by the dc bus voltage. Se also figure 12. The maximum inductor value are derived in [21] and are expressed by

$$L < \frac{\sqrt{\frac{v_{dc}^2}{3} - v_{gs}}}{\omega i_d} \qquad s \in [a, b, c] \tag{4.24}$$

The phase diagram for the L-filter is shown in figure 22. To illustrate the suppression of high harmonic frequencies the relevant transfer function must be calculated and illustrated in a Bode plot.

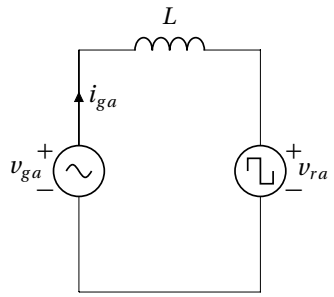


Figure 22: Phase diagram for the VOC AFE rectifier. Phase a is illustrated and the use of superposition is used to calculate the transfer function.

To calculate the desired transfer function, the use of Laplace transform and superposition principle are used. Shorting v_{ga} and setting up an expression for i_{ga} in the frequency domain yields

$$I_{ga} = -\frac{V_{ra}}{sL} \tag{4.25}$$

where s is the frequency variable. The desired transfer function are expressed as

$$G = \frac{I_{ga}}{V_{ra}} = -\frac{1}{sL} \tag{4.26}$$

The bode plot is shown in section 5.1.

4.2 Voltage orientated control with LCL-filter

In high power application it becomes expensive to use large inductors at the ac side of the VOC rectifier. With large inductance values stability problems might also arise. It is possible to rather use a LCL-filter with lower total inductance values. The switching frequency of the IGBTs can also be reduced and hence the switching losses and efficiency of the rectifier system will be increased [27]. The VOC AFE rectifier with LCL-filter configuration is illustrated in figure 23. To get the correct orientation of the reference frame in regards to the Park transformation, the voltage reference has been moved to the capacitors branches. This result in a voltage drop between the grid side and the sensed voltage. Therefore the quadrature component i_q is not equal to zero as in section 4.1. Also the sensed current is not from the grid but instead the rectifier currents are measured. It therefore implies that i_q differs

from zero [28].

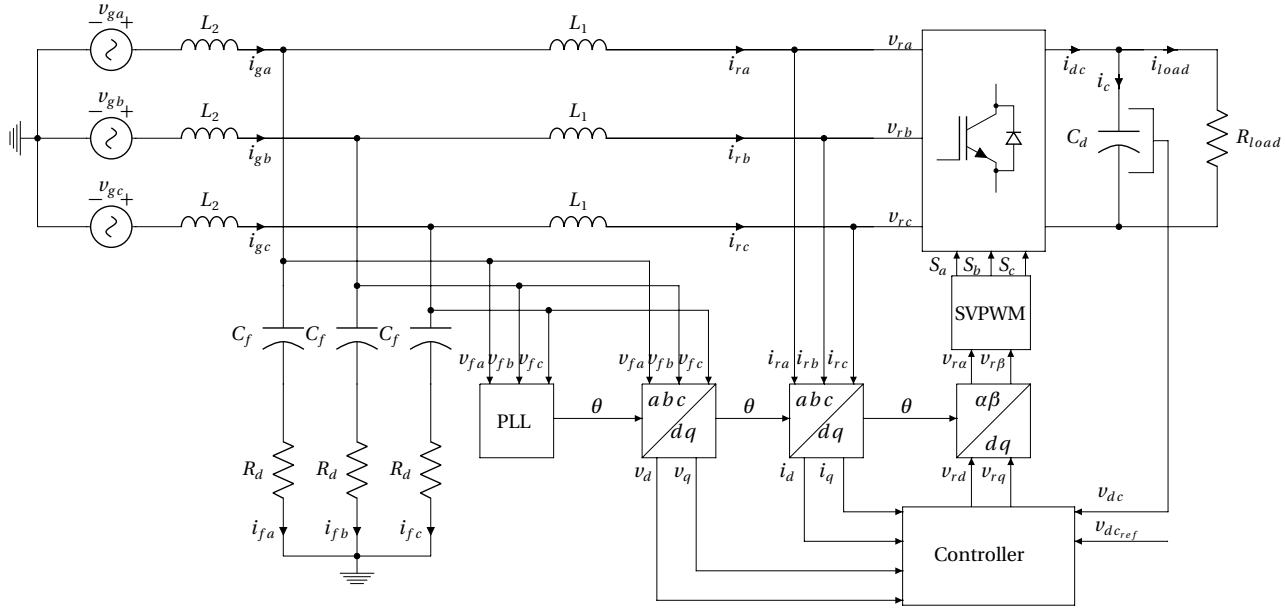


Figure 23: Configuration of the VOC AFE rectifier with LCL-filter. The controller is described in detail in figure 24. Adapted from [21, 27].

From figure 23 the mathematical description can be derived by the following relationships, neglecting the filter capacitor C_f and damping resistor R_d

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = L_t \frac{d}{dt} \begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} + \begin{bmatrix} v_{ra} \\ v_{rb} \\ v_{rc} \end{bmatrix} \tag{4.27}$$

$$C \frac{d_{v_{dc}}}{dt} = S_a i_{ra} + S_b i_{rb} + S_c i_{rc} - i_{load} \tag{4.28}$$

where $L_t = L_2 + L_1$. To ease the control system the sinusoidal voltages and currents from the grid are converted to dc values according to the Park transform given by equation 3.65. Transforming equation 4.27 and 4.28 by 3.65 and assuming balanced

operation, yields

$$v_d = L_t \frac{d\,i_d}{d\,t} - \omega L_t\, i_q + v_{rd} \tag{4.29}$$

$$v_q = L_t \frac{d\,i_q}{d\,t} + \omega L_t\, i_d + v_{rq} \tag{4.30}$$

$$C \frac{d_{v_{dc}}}{d\,t} = \frac{3}{2}(S_d\, i_{rd} + S_q\, i_{rq}) - i_{load} \tag{4.31}$$

The complex power delivered from the grid is expressed in an active and reactive component as follows

$$p = \frac{3}{2}(v_d\, i_d + v_q\, i_q) = v_{ga}\, i_{ga} + v_{gb}\, i_{gb} + v_{gc}\, i_{gc} \tag{4.32}$$

$$q = \frac{3}{2}(v_q\, i_d - v_d\, i_q) = \frac{1}{\sqrt{3}}\left[v_{ga}(i_{gc} - i_{ga}) + v_{gb}(i_{ga} - i_{gc}) + v_{gc}(i_{gb} - i_{ga})\right] \tag{4.33}$$

From equation 4.29 and 4.30 can the regulation system for the controller be realized according to figure 24. The decoupled control system have the same structure as the controller in section 4.1.

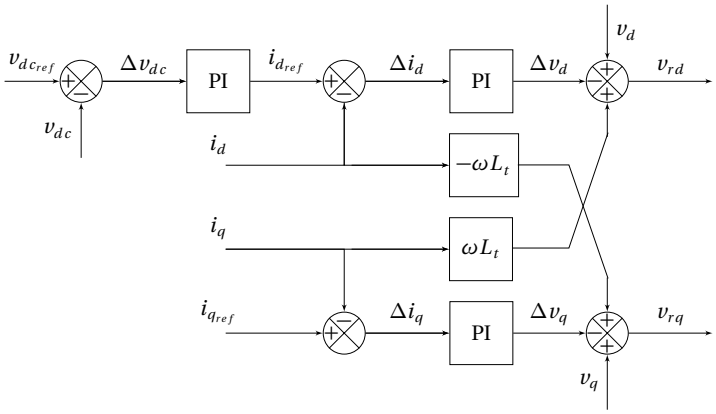


Figure 24: Synchronous controller working in dq coordinates for the VOC AFE rectifier with LCL-filter as illustrated in figure 23. Note that the only difference regrading the VOC controller in figure 20 are the inductances L_t.

To achieve UPF, the quadrature component i_q has to be equal to zero in section 4.1 [21]. In regards to the block scheme in figure 23, the branch currents i_{fa}, i_{fb} and i_{fc} will draw reactive power. Assuming that the voltage drop across L_2 is negligible compared to the grid voltage and neglecting the voltage drop across the damping

resistor R_d. Then the nominal reactive current component can be calculated by

$$i_{q_{ref}} = i_f = \frac{v_f}{R_d + \frac{1}{j\omega C_f}} \approx \frac{v_g}{\frac{1}{j\omega C_f}} \tag{4.34}$$

4.2.1 LCL-filter design

The LCL-filter design is described in [27] and the equations 4.35-4.46 are based on this work. The total inductance L_t should be as small as possible to improve the dynamic response of the rectifier and are calculated by

$$\frac{v_{dc}}{8 i_{rp_{max}} f_{sw}} \leq L_t \leq \frac{\sqrt{v_{dc}^2 - 4 v_{g_{max}}^2}}{i_{g_{max}} \omega} \tag{4.35}$$

$v_{g_{max}}$ is the amplitude value of the grid voltage and $i_{g_{max}}$ is the amplitude value of the grid current. f_{sw} is the the switching frequency for the IGBTs. The maximum ripple current $i_{rp_{max}}$ in one switching period is expressed as

$$i_{rp_{max}} = \frac{1}{8} \frac{v_{dc}}{L_t f_{sw}} \tag{4.36}$$

The inductors L_1 and L_2 are expressed as

$$L_t = L_1 + L_2 \tag{4.37}$$

$$L_1 = a L_t \tag{4.38}$$

$$L_2 = \frac{L_t}{a+1} \tag{4.39}$$

Selection of the capacitors are given by

$$C_f = \frac{1}{r \omega_{sw}^2 L_2} \tag{4.40}$$

The factors a, r and b are expressed by

$$a = \frac{b-2+\sqrt{b(b-4)}}{2} \tag{4.41}$$

$$r = x(1+a) \tag{4.42}$$

$$b = \frac{\sigma}{1+\sigma}\frac{1}{x} \tag{4.43}$$

σ is called the switching harmonic current attenuation ratio and is the ratio between the current flowing in L_2 and the main current from an imaginary voltage source with only harmonic switching components, see figure 25. The factor x is expressed as

$$x = \frac{3\omega_f v^2_{gs_{rms}}}{\omega^2_{sw} L_t P \lambda} \qquad s \in [a,b,c] \tag{4.44}$$

where P is the consumed power by the load R_{load} in figure 23, ω_{sw} is the angular switching frequency and λ is a factor for the fundamental reactive power consumed by the capacitors C_f and should be less than 5% of the rated power P.

σ have two constraints in regards to resonance phenomenon and are restricted by

$$\frac{4x}{1-6x} \leq \sigma \leq \frac{1}{3} \tag{4.45}$$

To avoid resonance the damping resistor R_d is connected in series with C_f which can absorb the switching frequency ripple and is given by

$$R_{d_{min}} = \frac{1}{\omega_{res} C_f} \tag{4.46}$$

The LCL-filter angular resonance frequency is expressed as [29]

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{4.47}$$

The phase diagram for the VOC AFE rectifier with LCL-filter is shown in figure 25. To illustrate the suppression of high harmonic frequencies the relevant transfer function must be calculated and illustrated in a Bode plot.

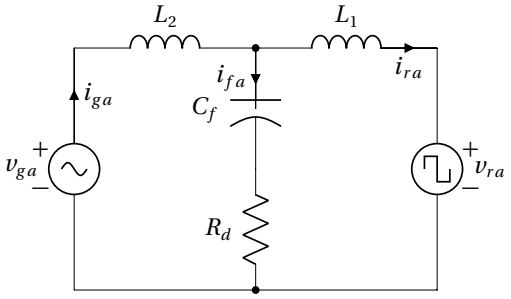


Figure 25: Phase diagram for the VOC AFE rectifier with LCL-filter. Phase a is illustrated and the use of superposition is used to calculate the transfer function.

Only the switching harmonic voltages are considered in the design. Therefore the voltage source from the grid is shorted and the fundamental frequency from the rectifier voltage source is omitted. To calculate the desired transfer function, the use of Laplace transform and the aforementioned assumption are made. Shorting v_{ga} and setting up an expression for i_{ra} in the frequency domain yields

$$\begin{aligned} -I_{ga} &= -I_{ra}\left(\frac{\frac{1}{sC_f}+R_d}{\frac{1}{sC_f}+R_d+sL_2}\right) \\ I_{ga} &= I_{ra}\left(\frac{sR_dC_f+1}{s^2L_2C_f+sR_dC_f+1}\right) \end{aligned} \tag{4.48}$$

The expression for the rectifier current are given by

$$I_{ra} = \frac{V_{ra}}{Z_{eq}} \tag{4.49}$$

Furthermore the equivalent impedance is given by

$$Z_{eq} = \left(sL_1 + \frac{s^2L_2R_dC_f+sL_2}{s^2L_2C_f+sR_dC_f+1}\right) \tag{4.50}$$

$$Z_{eq} = \left(\frac{s^3L_1L_2C_f+s^2L_2R_dC_f+s^2L_1R_dC_f+sL_1+sL_2}{s^2L_2C_f+sR_dC_f+1}\right)$$

The admittance transfer function for the LCL-filter is expressed as

$$G = \frac{I_{ga}}{V_{ra}} \tag{4.51}$$

Combining equation 4.48-4.50 into 4.51 yields

$$G = \frac{sR_dC_f + 1}{s^3L_1L_2C_f + s^2L_2R_dC_f + s^2L_1R_dC_f + sL_1 + sL_2} \tag{4.52}$$

The Bode plot will be shown in section 5.2.

4.3 Additional parameters

For both VOC AFE configuration explained in section 4.1 and 4.2, is the minimum dc bus voltage calculated in a similar fashion. For proper operation of the rectifier the following expression must be valid [21]

$$V_{dc_{min}} > \sqrt{2}\sqrt{3}V_{gs} = V_{LL_{max}} \qquad s \in [a, b, c] \tag{4.53}$$

The definition in equation 4.53 is true for a diode rectifier and must be adapted for the VOC AFE rectifier with SVPWM technique. According to the discussion in section 3.3.2 and equation 3.80 is the maximum reference voltage expressed as

$$\begin{aligned} V_\chi = V_{gs_{max}} &= \frac{V_{dc}}{\sqrt{3}} \\ V_{LL}\frac{\sqrt{2}}{\sqrt{3}} &= \frac{V_{dc}}{\sqrt{3}} \end{aligned} \tag{4.54}$$

and hence the minimum dc bus voltage is expressed as

$$\begin{aligned} \frac{V_{dc_{min}}}{\sqrt{3}} &> V_{LL}\frac{\sqrt{2}}{\sqrt{3}} \\ V_{dc_{min}} &> V_{LL}\sqrt{2} \end{aligned} \tag{4.55}$$

The choice of minimum dc bus capacitor is expressed by [30]

$$C_{min} = P\left(\frac{\sqrt{2} + \sqrt{3}\frac{V_{LL}}{V_{dc}}}{2\sqrt{3}V_{LL}f_{sw}\Delta V_{dc}}\right) \tag{4.56}$$

where P is the active power consumed by the load connected to the rectifier, f_{sw} is the switching frequency of the IGBTs and ΔV_{dc} is the maximum ripple voltage allowed.

5 Simulation and grid calculation

The simulations were implemented in Simulink and Matlab 2017b as the computational engine. Simulation according to theory explained in section 4.1 and 4.2 were conducted. Parameters were chosen according to the laboratory model explained in section 6. This was conducted to verify the simulation results to the measured results from the laboratory model. Therefore are the parameters not up to scale according to the power ratings needed for the ferry chargers (1-10 MW). Nevertheless, the simulation parameters can be scaled up to fit the power ratings for the rectifier design. The THD_v at PCC and power loss over the ac side filters are calculated for the different ferry terminals defined in table 1. For both VOC AFE rectifier systems were the simulation configuration parameters the same. To solve the differential equations of the system a fixed-step discrete solver was used. The sampling time was chosen to 1µs to get sufficient accurate results. In order to shorten simulation time the rectifier system was discretized and hence no continuous states occur under the simulation.

5.1 VOC AFE rectifier

The main circuit for the simulation for the VOC AFE rectifier is illustrated in figure 26. The main circuit is according to figure 19. On the dc busbar is the load confined to 50% to 125% of nominal load. This is realized with time triggered switches to connect parallel branches of resistors to the dc busbar. There are several subsystems including the Clarke and Park transformation, SVPWM, power factor calculation and the controller circuit. Each subsystem will be explained in section 5.1.1 to 5.1.4. The parameters used in the simulation are according to the values in table 6. The resistive load simulates the battery package for the electric ferry. In this case the connected load is 3kW. The choice of switching frequency is a trade off between lower harmonic content and switching losses and were chosen to 5kHz.

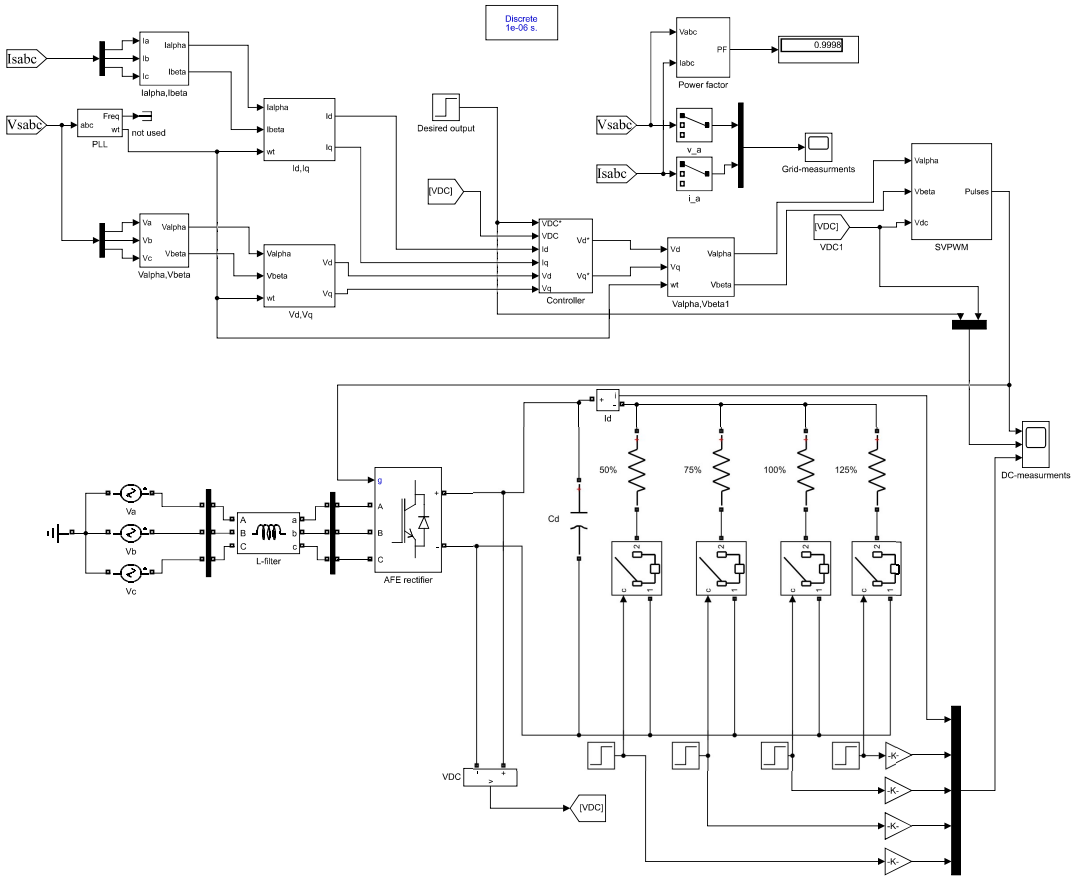


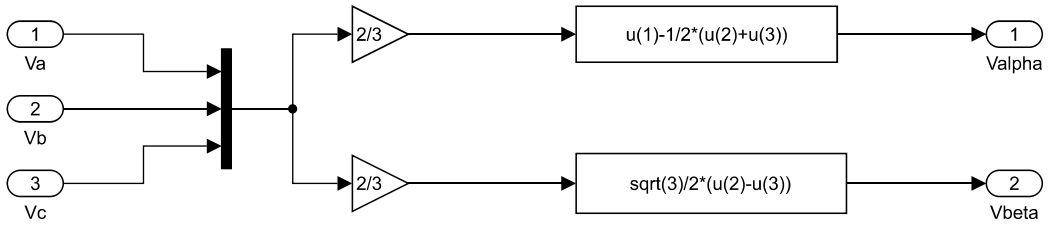
Figure 26: Simulation scheme for the VOC AFE rectifier in Simulink.

Table 6: Parameters for the VOC AFE rectifier simulation.

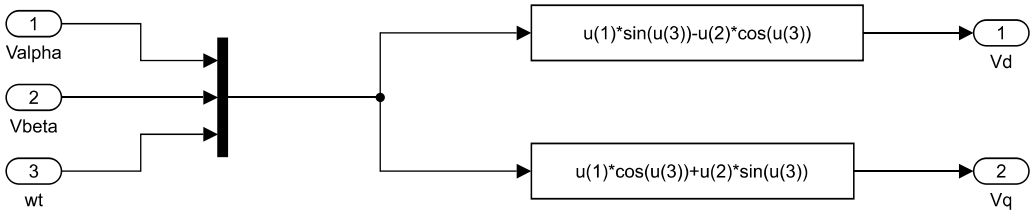
Parameter	Value	Unit
Inductor L	8.0	mH
Capacitor C_d	1500	µF
Resistor R_{load}	38.5333	Ω
DC bus voltage V_{dc}	340	V
Grid line voltage $V_{LL_{RMS}}$	220	V
Grid frequency f	50	Hz
Switching frequency f_{sw}	5.0	kHz
Sampling time T_s	1.0	µs

5.1.1 Clarke and Park transformation subsystem

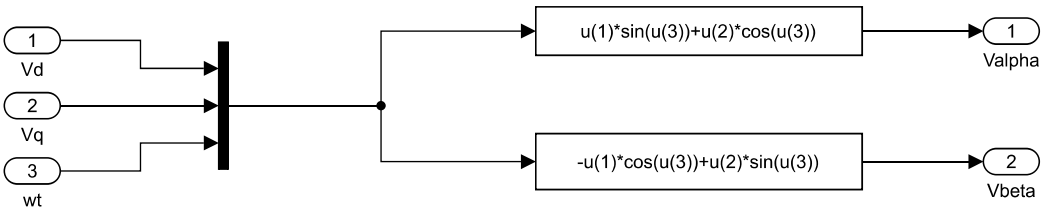
To control both the PF and the dc bus voltage, the controller needs the phase voltages and phase currents converted into dc values. The subsequent discussion explains how this is done in the simulation. The transformation block between a three-phase stationary reference frame to a two-phase stationary reference frame, hence the Clarke transformation are labeled Valpha, Vbeta and Ialpha, Ibeta in figure 26. The subsystem for the Clarke transformation is illustrated in figure 27a.



(a) Subsystem for converting three-phase voltages Va, Vb and Vc to a two-phase system.



(b) Subsystem for converting two-phase voltages Valpha and Vbeta to dc values.



(c) Subsystem for implementing the inverse Park transform for the space vector generated from the controller circuit.

Figure 27: Subsystems for converting three-phase voltages into dc values feeding the controller circuit. The output from the controller are converted back to alpha beta components and the inverse Clarke transform implementation is illustrated.

The three input voltages are converted according to equation 3.62 and 3.63. The three inputs are multiplexed and scaled with 2/3 and thereafter each function block

uses a function called $u(x)$, where x is a variable according to the numbered input. The same subsystems are used for converting the current components and is therefore not shown in figure 27a.

To convert the two-phase alternating system to dc values is the Park transform used. The Park transform blocks are labeled Vd, Vq and Id, Iq in figure 26. The subsystem for Vd, Vq is illustrated in figure 27b. The two inputs are converted according to equation 3.65 and 3.66. The same subsystem is used to convert the two-phase alpha, beta currents into dc values and is therefore not shown in figure 27b.

The inverse Clarke transformation block is labeled Valpha, Vbeta1 in figure 26. It converts the dc values from the controller block to a two-phase alternating system, feeding the SVPWM block with the space vector. The subsystem for the inverse Clarke transform is shown in figure 27c. The function blocks expressions are according to equation A.17 and the derivation of the inverse Clarke transform are derived from appendix A.

5.1.2 Controller circuit subsystem

The controller scheme is based on figure 20 and the circuit regulates the PF and the dc busbar voltage according to desired values. The subsystem labeled Controller in figure 26 is illustrated in figure 28. The input values are the direct and quadrature voltage and current measured on the grid side. These values are compared to set values and are regulated with a dedicated PI-controller. Furthermore is the dc busbar voltage measured and compared to a set value, feeding a PI-controller. The PI-controllers proportional and integration constants are given by table 7. The initial conditions are used by the integrator term in the PI-controller. To acquire the initial conditions were experimental simulation used. Measured values in front of each summation block referred to each PI-controller were conducted and hence the initial value was chosen. The proportional and integral constants were chosen by experimental simulation with trial and error. As briefly discussed in section 4.1, two methods for the tuning process according to standard rules are available. Nevertheless, these methods can only be used as broad indicators.

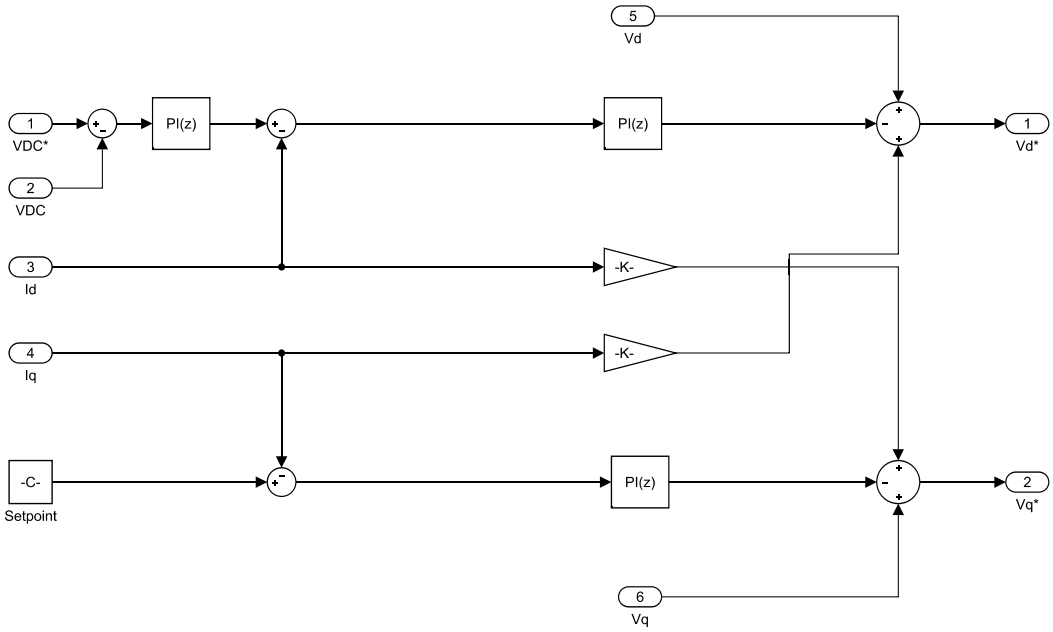


Figure 28: Controller subsystem regulating the PF and the dc busbar voltage according to desired values. Two inner current controllers are used for the quadrature and direct current. One outer voltage controller is used for the dc busbar voltage.

Table 7: Parameters for the outer voltage controller and the two inner current controllers.

Controller	Proportional constant	Integral constant	Initial conditions
Voltage v_{dc}	0.65	65	0
Current i_d	150	20	296.37
Current i_q	150	20	-1.3

5.1.3 SVPWM subsystem

The SVPWM subsystem is labeled SVPWM in figure 26 and is build up by several subsystem as shown in figure 29. The SVPWM system are according to the theory explained in section 3.3.2. The controller circuit outputs and hence the inputs for the SVPWM subsystem, are the decomposed components of the space vector. The modulus and argument of the space vector are calculated respectively in the Vref and gamma subsystem according to the Matlab script in figure 30a and 30b.

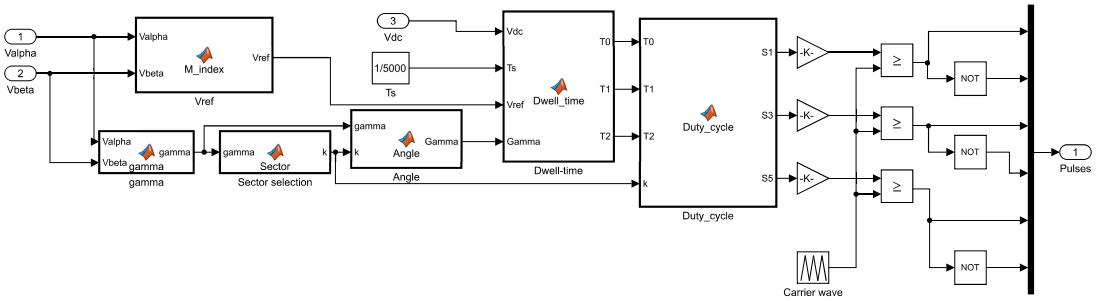


Figure 29: The SVPWM subsystem are made up by six subsystem to generate six switching signals to the IGBTs.

```
function Vref  = M_index(Valpha,Vbeta)

Vref=sqrt(Valpha^2+Vbeta^2);
```

(a) Calculation of the modulus generated by the controller circuit.

```
function gamma  = gamma(Valpha,Vbeta)
gamma=atan2(Vbeta,Valpha);
```

(b) Calculation of the argument generated by the controller circuit.

Figure 30: Calculation of the space vector according to the decomposed space vector from the controller circuit.

After the calculation of the argument and modulus, determines the sector selection subsystem which sector the space vector is located in. The Matlab script is shown

```
function k  = Sector(gamma)
k=0;
if(gamma>0)&(gamma<=pi/3)
    k=1;
end;
if(gamma>pi/3)&(gamma<=2*pi/3)
    k=2;
end;
if(gamma>2*pi/3)&(gamma<=pi)
    k=3;
end;
if(gamma<=0)&(gamma>-pi/3)
    k=6;
end;
if(gamma<=-pi/3)&(gamma>-2*pi/3)
    k=5;
end;
if(gamma<=-2*pi/3)&(gamma>-pi)
    k=4;
end;
```

Figure 31: The sector selection subsystem determines which sector the space vector is located by an if else code.

in figure 31. It determines the sector by an if else code and the sectors are separated by 60°. The Angle subsystem have both the sector k and the argument of the space vector as inputs. According to what sector the space vector is located in, calculates the if else statement in figure 32 the angle Gamma to be between 0-60°. The Dwell time subsystem calculates the modulation index m and the dwell time. Furthermore the dwell time of the two adjacent boundary vectors and the zero vector are calculated according to equation 3.72, 3.73 and 3.79. The same expression is shown in figure 33. The Duty cycle subsystem calculates the switching times for the upper arm of each IGBT half bridge. The outputs are called S1,S2 and S3. The equations used in figure 34 are given by table 5. The if else statement determines which sector the space vector is located according to the input k from the sector selection subsystem. The output S1, S2 and S3 are then multiplied according to the sampling time T_s to get a signal between zero and one. The control signals are compared to a sawtooth carrier wave signal with a frequency equal to 5kHz, which oscillates between zero and one. When the control signal is greater or equal to the carrier wave, is a high digital output signal generated which triggers the IGBTs S_a^+, S_b^+ and S_c^+. The lower arms of each IGBT half bridges have a complementary digital

```
function Gamma  = Angle(gamma,k)
Gamma=0;
if(k==1)
    Gamma=gamma;
end;
if(k==2)
    Gamma=gamma-pi/3;
end;
if(k==3)
    Gamma=gamma-2*pi/3;
end;
if(k==6)
    Gamma=pi/3+gamma;
end;
if(k==5)
    Gamma=2*pi/3+gamma;
end;
if(k==4)
    Gamma=pi+gamma;
end;
```

Figure 32: The inputs for the angle subsystem are the sector k and the modulus of the space vector. Calculation of the angle Gamma are according to the if else statement, where the angle is between 0-60°.

```
function [T0,T1,T2]  = Dwell_time(Vdc,Ts,Vref,Gamma)
ma=Vref/Vdc;
T1=Ts*sqrt(3)*ma*sin(pi/3-Gamma);
T2=Ts*sqrt(3)*ma*sin(Gamma);
T0=(Ts-T1-T2);
```

Figure 33: Determination of the dwell time for the two adjacent boundary vectors and the zero vector. The vector summation of the three vectors equals the space vector.

```
function [S1,S3,S5]  = Duty_cycle(T0,T1,T2,k)
S1=0;
S3=0;
S5=0;
if(k==1)
    S1=T1+T2+T0/2;
    S3=T2+T0/2;
    S5=T0/2;
end;
if(k==2)
    S1=T1+T0/2;
    S3=T1+T2+T0/2;
    S5=T0/2;
end;
if(k==3)
    S1=T0/2;
    S3=T1+T2+T0/2;
    S5=T2+T0/2;
end;
if(k==4)
    S1=T0/2;
    S3=T1+T0/2;
    S5=T1+T2+T0/2;
end;
if(k==5)
    S1=T2+T0/2;
    S3=T0/2;
    S5=T1+T2+T0/2;
end;
if(k==6)
    S1=T1+T2+T0/2;
    S3=T0/2;
    S5=T1+T0/2;
end;
```

Figure 34: Calculation of the switching time for the upper arm in each IGBT half bridge. The outputs S1, S2 and S3 sends a digital signal to the gate of respectively S_a^+, S_b^+ and S_c^+.

signal and are in compliance with table 5. A typical control and carrier wave signal generated by the SVPWM are illustrated in figure 35a. The generated digital output for the half bridge in phase a is shown in figure 35b.

5.1.4 Power factor subsystem

The power factor subsystem in figure 26 is illustrated in figure 36. The two inputs are the phase voltages and currents measured at the grid side. In this particular subsystem, the PF for phase a is calculated. The same calculation method is valid for phase b and c and yields the same results.

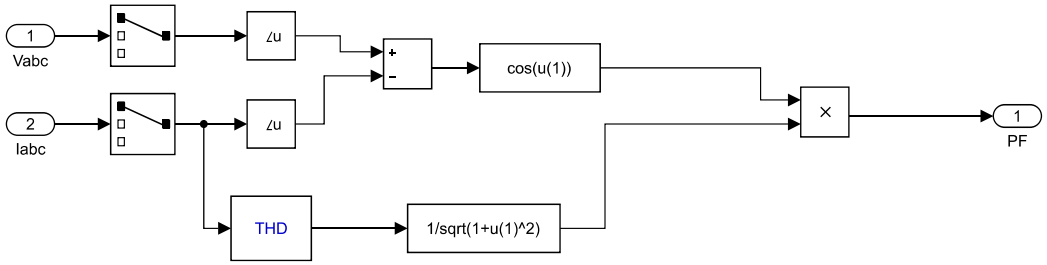


Figure 36: Subsystem for the power factor calculation. Only the result for phase a is shown.

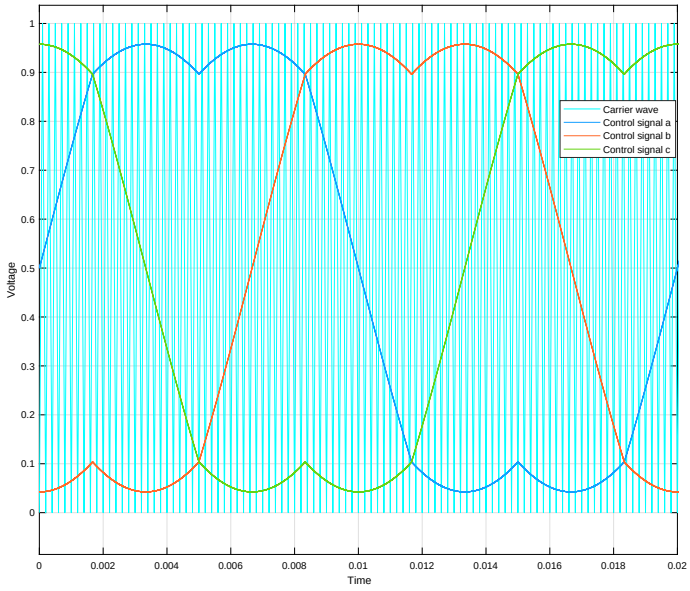
The first step to calculate the PF is to rearrange equation 3.6, yielding

$$THD_i^2 = \frac{I_s^2 - I_{s_1}^2}{I_{s_1}^2} \tag{5.1}$$
$$\frac{I_{s_1}}{I_s} = \frac{1}{\sqrt{1+THD_i^2}}$$

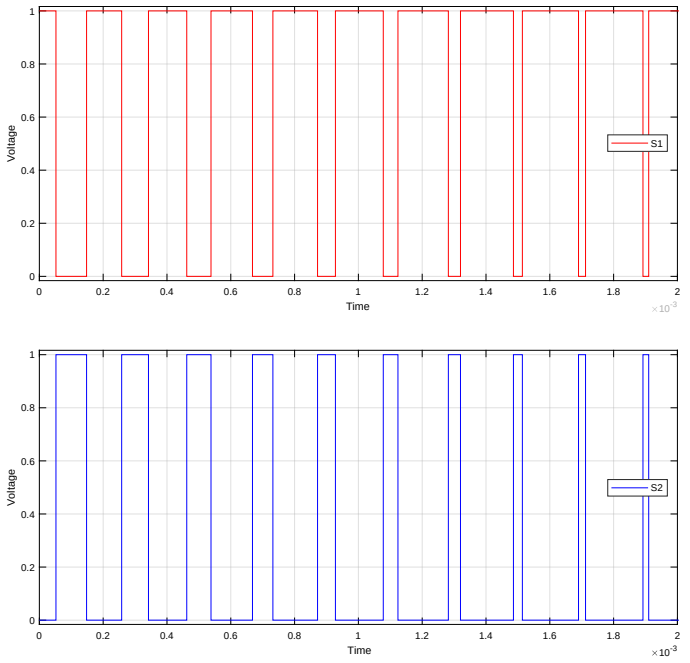
The combination of the expression in equation 3.27 and 5.1 yields

$$PF = \frac{1}{\sqrt{1+THD_i^2}} \cdot DPF \tag{5.2}$$

As shown in figure 36 the THD_i is first calculated and then scaled. The cosine between the phase angle difference regards to voltage and current yields the DPF. The product of the aforementioned discussion yields the PF.



(a) The three control signals are phase shifted from each other by 120°. The carrier signal has the same frequency as the fundamental frequency from the utility grid. The carrier wave has a frequency according to the switching frequency to the IGBTs.



(b) When the control signal is larger or equal than the carrier wave, generates the SVPWM a high digital output to the upper arm S_a^+ of the IGBT bridge. The lower arm S_a^- receives a complementary digital signal referred to the upper arm.

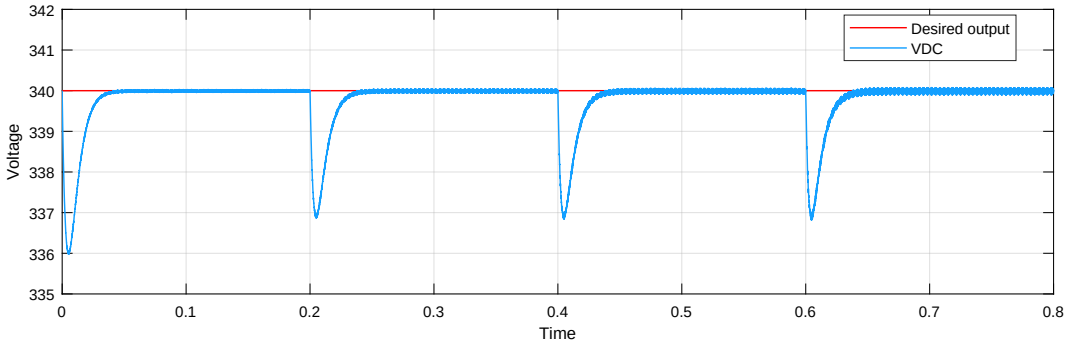
Figure 35: Typical control and carrier wave signals generated by the SVPWM. The digital outputs for phase a are shown in figure 35b.

5.1.5 Results

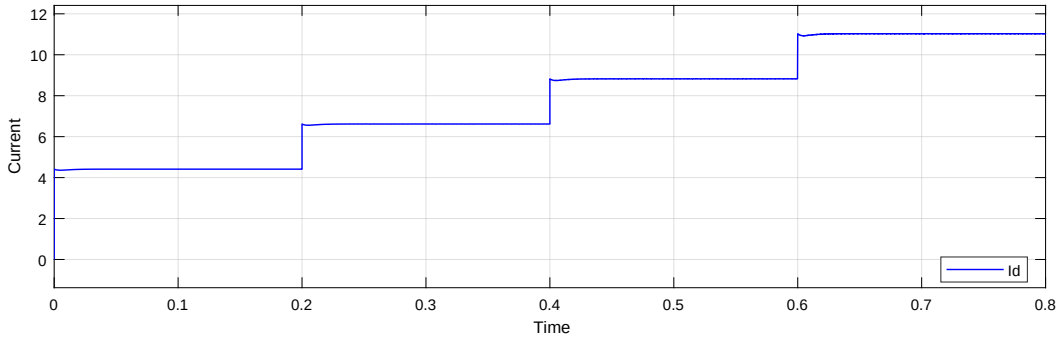
The VOC AFE rectifier is simulated under various load conditions. Loads between 50% to 125% of nominal load is simulated and the dc busbar voltage is shown in figure 37a. The desired voltage is 340V and is marked by a red solid line. The actual value is the solid blue line. When the simulation start there is a 4V voltage drop before the controller circuit regulates up the dc busbar voltage to desired value. The load changes every 0.2 seconds and hence a voltage drop occurs at these instances. Under nominal load the voltage ripple is 0.13V and is 0.04% of nominal dc voltage. In figure 37b the dc current is shown in a solid blue line. Also here it can be seen that the load changes as a step every 0.2 seconds and hence the current increases. The current ripple is 2mA under nominal load conditions and is 0.022% of the nominal dc current.

The current drawn from the utility grid should be in phase with the voltage and have a low THD_i. As illustrated in figure 38, both the phase voltage and phase current are in phase. Only the results for phase a is shown but the same results apply also for phase b and c. The phase current is enhanced by a factor nine for readability. The Bode plot for the attenuation of high order switching components influencing the grid is illustrated in figure 39. The Bode plot is based on the admittance transfer function in equation 4.26. The L-filter is a first order filter with an attenuation factor of minus 20dB/decade.

The THD_i in phase a is illustrated in figure 40a-40d. The harmonic order axis is normalized in regards to the 50Hz fundamental frequency. The harmonic components are low under all load conditions and hence the fundamental component is dominant. From figure 38 and 40 it can bee seen that the PF is approximated unity under all simulated load conditions.



(a) DC busbar voltage as a function of simulation time. Every 0.2 seconds the load increases and thus a voltage drop occurs at these instances.



(b) DC current as a function of simulation time. Every 0.2 seconds the load increases and thus the dc current increases according to the load.

Figure 37: Simulated dc voltages and dc current under load conditions from 50% to 125% of nominal load.

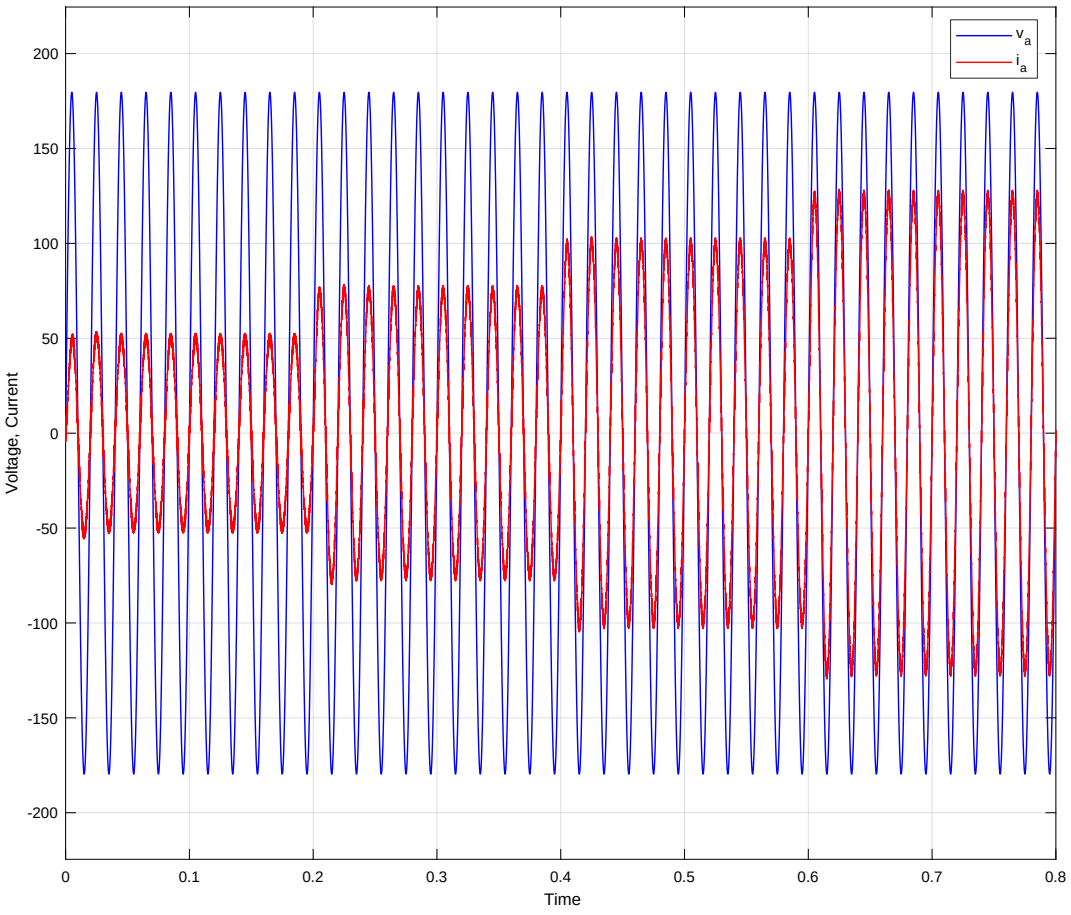


Figure 38: Waveforms for the grid phase voltage and the grid phase current in phase a. Note that the phase voltage and phase current are in phase and have almost no harmonic components. The phase current is enhanced by a factor nine for readability.

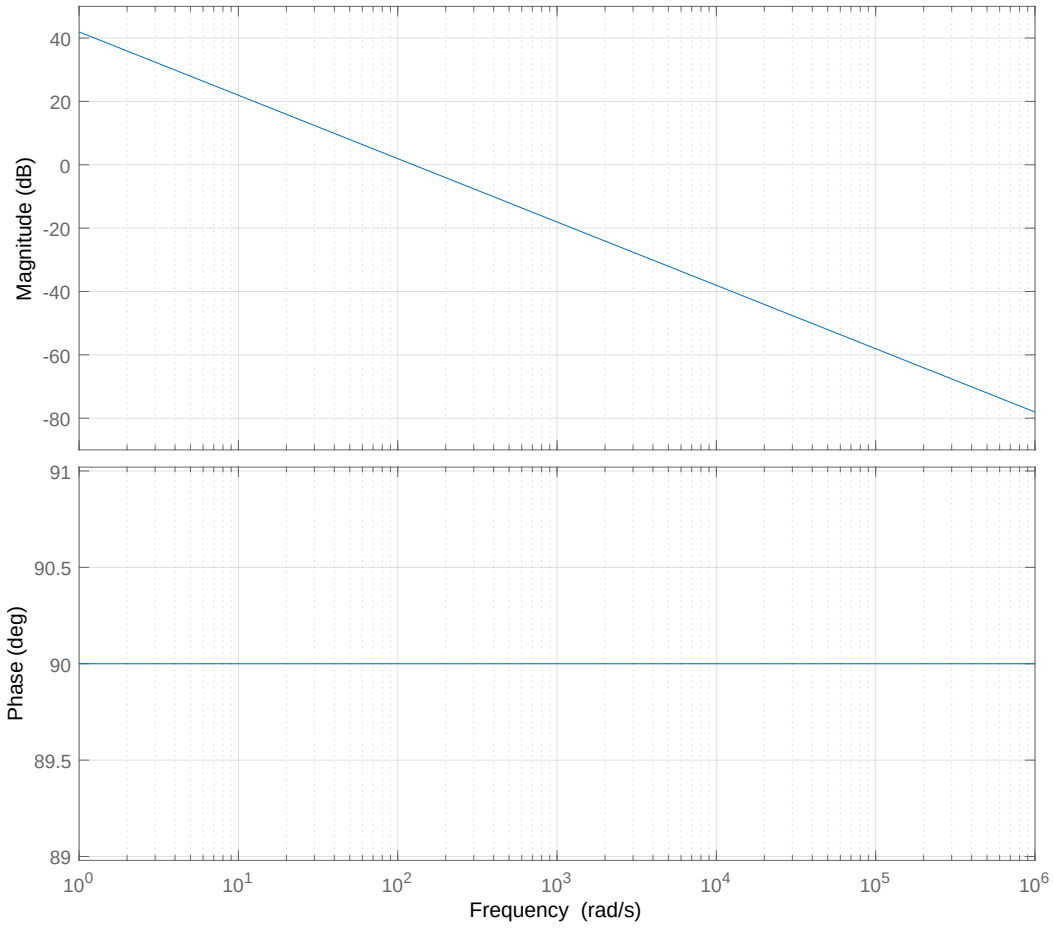
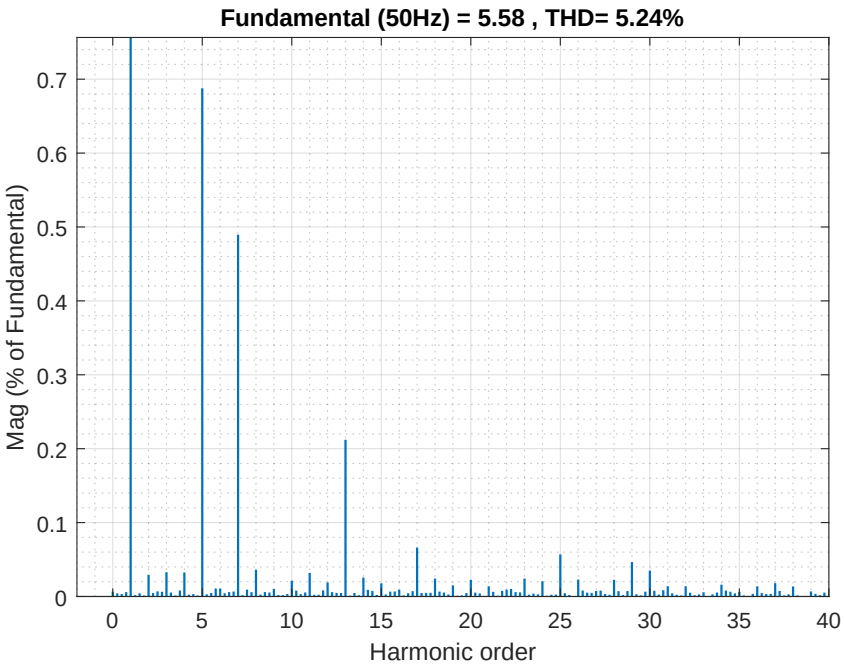
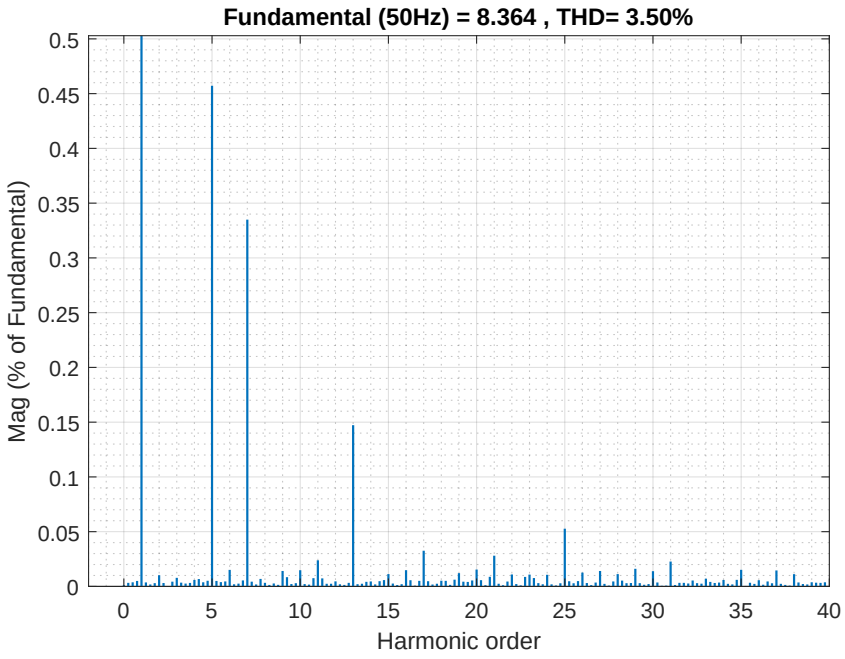


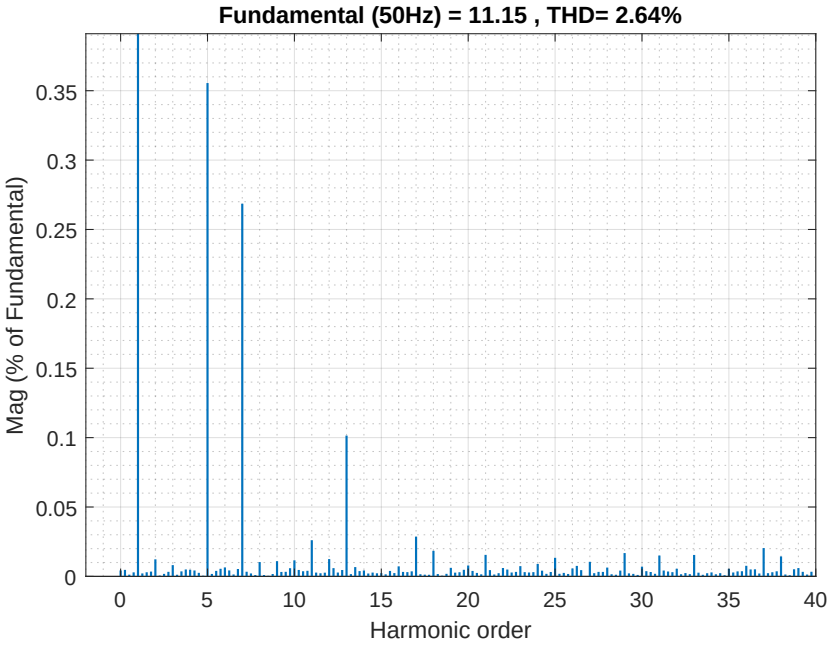
Figure 39: Bode plot for the admittance transfer function given by equation 4.26. The L-filter is a first order filter with an attenuation of minus 20dB/decade.



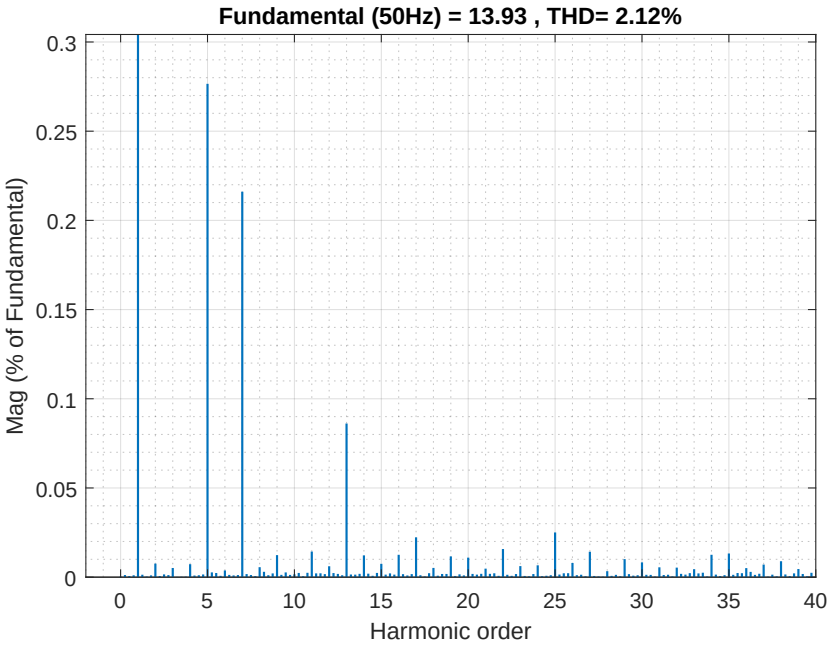
(a) THD_i for phase a under 50% load condition.



(b) THD_i for phase a under 75% load condition.



(c) THD_i for phase a under nominal load condition.



(d) THD_i for phase a under 125% load condition.

Figure 40: THD_i under load conditions from 50% to 125% of nominal load. The harmonic order axis is normalized regards to the fundamental frequency. Only phase a is shown, but similar results applies for phase b and c.

5.1.6 Grid calculations

The harmonic voltage components injected into the ac source at the PCC were discussed in section 3.1. Grid parameters given by BKK in table 1 defines the capacity of the grid at the PCC. Calculating the grid short circuit capacity I_{sc} and the grid resistance R_s and reactance X_s from respectively equation 3.16, 3.11 and 3.12, yields the grid data presented in table 8.

Table 8: Short circuit capacity, resistive and reactive components of the grid impedance at the different ferry terminals.

Ferry terminal	I_{sc} [A]	R_s [Ω]	X_s [Ω]
Leirvåg	3017.97	1.7677	3.8195
Sløvåg	1522.11	3.3379	7.6482
Fedje	892.27	11.3882	8.412
Sævrøy	879.15	10.9803	9.3899
Krokeide	1627.08	2.42	3.0625
Hatvik	2283.16	2.6703	4.8804
Haljem	2624.32	2.0812	4.3697

The grid data affects the harmonic voltage components at the PCC which is expressed by equation 3.17 and is rearranged for clarity

$$V_{h_{PCC}} = h \cdot \frac{I_h}{I_{sc}} \cdot V_s \tag{5.3}$$

The 3kW simulated load at a line voltage of 220V does not yield any interesting result in regards to $\%V_{h_{PCC}}$ and THD_v. The simulation parameters are not in compliance with realistic values in regards to the power ratings between 1 to 10MW. It can be seen from equation 5.3 that $V_{h_{PCC}}$ would be approximative zero due to the high short circuit capacity I_{sc} presented in table 8. Therefore scaling the VOC rectifier up to the range between 1 to 10MW yields a more realistic result in regards to harmonic voltage components at the PCC.

The simulation of a full range VOC AFE rectifier have however not been conducted

due to a lack of time. An approach to calculate reasonable harmonic voltage components at PCC, is to scale I_h with the increasing load current I'_{load}. This linear relation is a simplification but gives a good indication if the harmonic voltage components injected to the utility grid, are in compliance with the values described by BKK in table 2. The simulation results in regards to I_h and THD_i in section 5.1.5 have therefore been reused. Only the calculation under nominal load conditions have been assumed and thus the current components in figure 40c have been used.

A study conducted by DNV GL [12] defines a charging capacity to be 3683kW between the ferry crossing Leirvåg and Sløvåg. The same power requirement has been assumed for all ferry terminals for simplicity. The line voltage V_{LL} at the PCC are in compliance with the values in table 1 (22kV or 11kV) for the different ferry terminals. Furthermore UPF has also been assumed. The load current drawn from the utility grid is given by

$$I'_{load} = \frac{P}{V_{LL}\sqrt{3}\cos\phi} \tag{5.4}$$

$$\tag{5.5}$$

The factor in regards to the load current is expressed as

$$k_{load} = \frac{I'_{load}}{I_{load}} \tag{5.6}$$

$$\tag{5.7}$$

I_{load} is the grid rms current under nominal load conditions and is taken from figure 40c. V_s in equation 5.3 is the phase rms voltage at the PCC and yields

$$V_s = \frac{V_{LL}}{\sqrt{3}} \tag{5.8}$$

$$\tag{5.9}$$

Table 9: Parameters for calculating $\%V_{h_{PCC}}$ at the different ferry terminals. Note that only Krokeide differs from the other ferry terminals due to line voltage at 11kV.

Ferry terminal	I'_{load} [A]	k_{load} []	V_s [V]
Leirvåg	96.7	12.3	12701.7
Sløvåg	96.7	12.3	12701.7
Fedje	96.7	12.3	12701.7
Sævrøy	96.7	12.3	12701.7
Krokeide	193.3	24.5	6530.8
Hatvik	96.7	12.3	12701.7
Haljem	96.7	12.3	12701.7

The new harmonic current components are now assumed to be

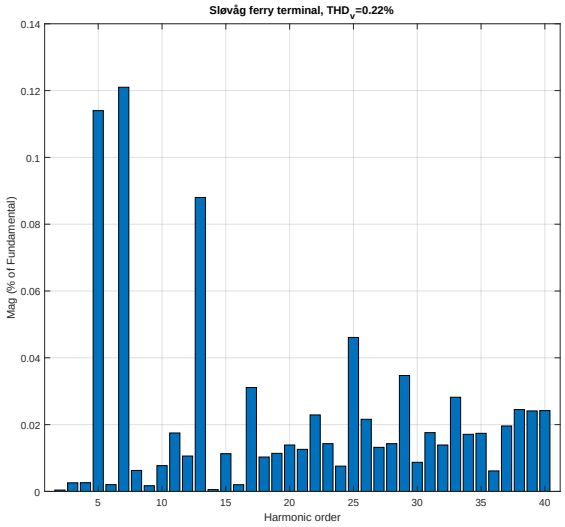
$$I'_h = I_h \cdot k_{load} \tag{5.10}$$

$$\tag{5.11}$$

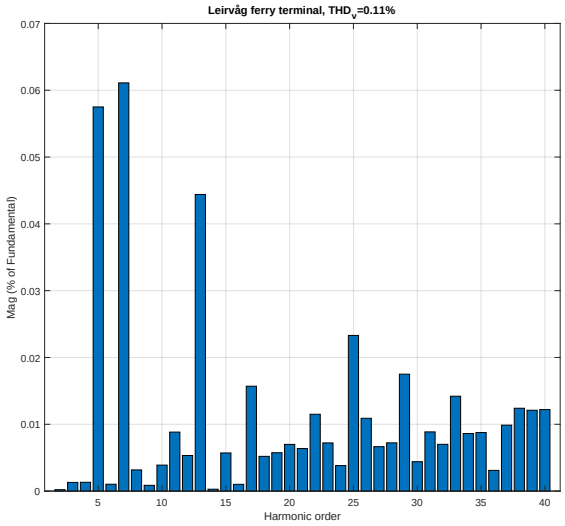
The scaled individual harmonic voltage components is expressed as

$$V'_{h_{PCC}} = h \cdot \frac{I'_h}{I_{sc}} \cdot V_s \tag{5.12}$$

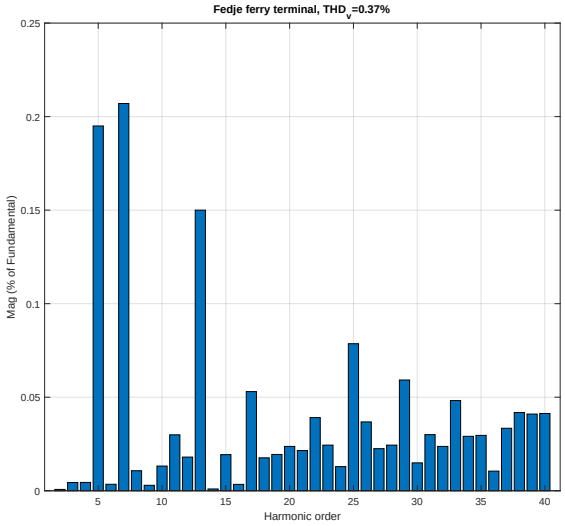
Parameters for calculating $\%V_{h_{PCC}}$ at the different ferry terminals are based on the aforementioned discussion and are shown in table 9. Extracting each individual harmonic current component from the simulation in section 5.1.5 under nominal load and scaling it by the aforementioned discussion, yields the $V'_{h_{PCC}}$ at the PCC for the ferry terminals. THD_v is calculated by equation 3.18. Figure 41a to 41g shows the $V'_{h_{PCC}}$ for the ferry terminals up to the 40th harmonic. THD_v is shown at the top of each figure and is limited to the 40th harmonic due to the definition in supply safety regulation [4]. Figure 42 compares the harmonic voltage components between each ferry terminal to the requirements defined by BKK in table 2. Note that figure 42 shall be read as the difference between the upper and lower value for the respective ferry terminal at the y-axis. The three-phase power loss over the L-filter is calculated to 70.44kW in appendix C.



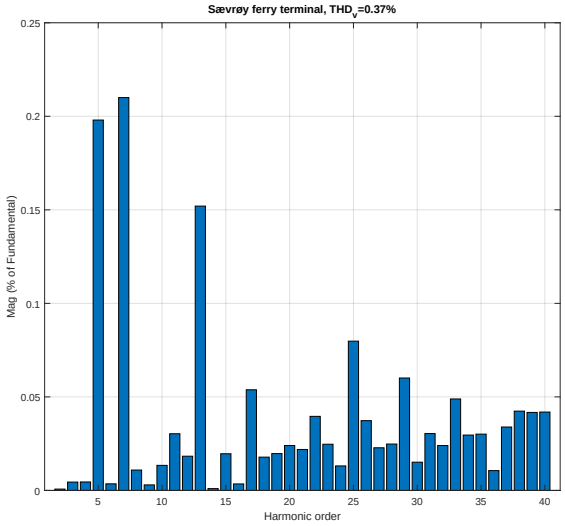
(a) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Sløvåg ferry terminal.



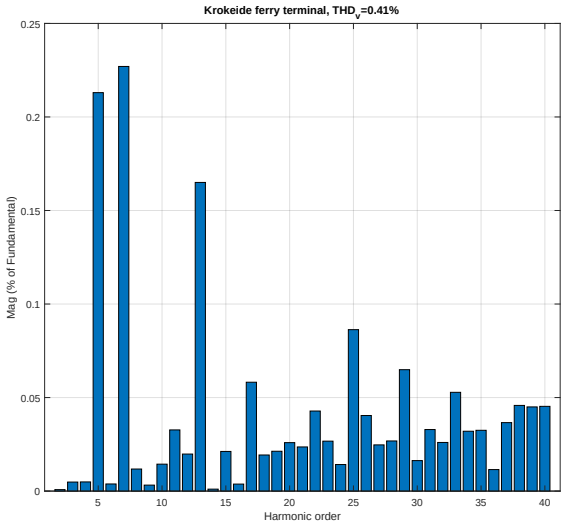
(b) Harmonic components $\%V'_{h_{PCC}}$ and THD_v for Leirvåg ferry terminal.



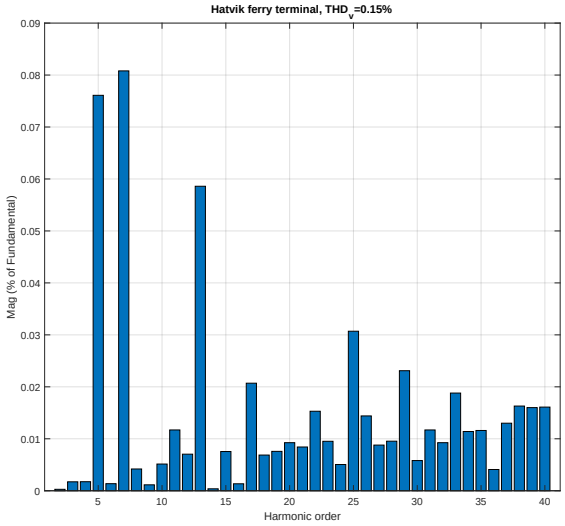
(c) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Fedje ferry terminal.



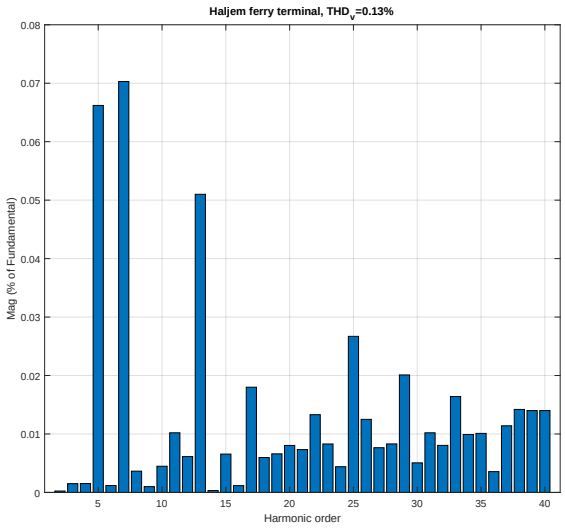
(d) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Sævrøy ferry terminal.



(e) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Krokeide ferry terminal.



(f) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Hatvik ferry terminal.



(g) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Haljem ferry terminal.

Figure 41: Individual harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for the ferry terminals in table 1. Grid parameters from table 8 and the harmonic current components under nominal load conditions were used for the calculations.

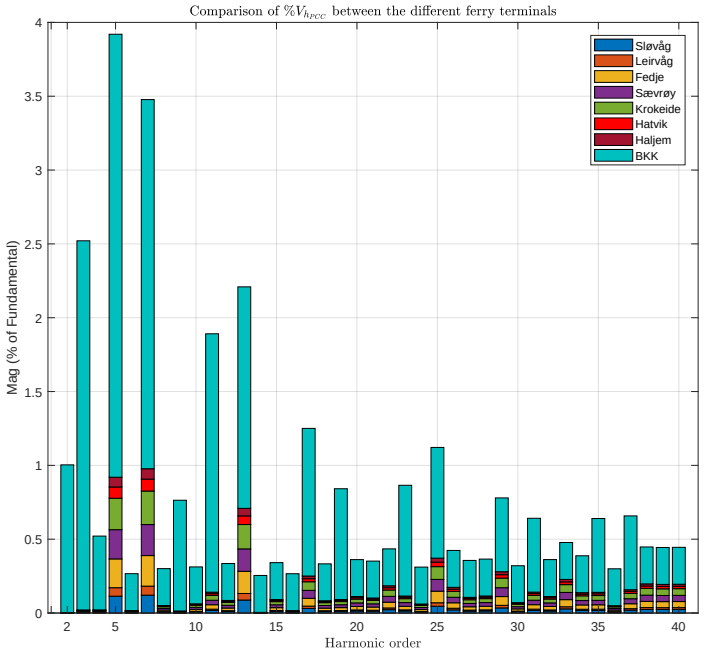


Figure 42: Comparison of the harmonic voltage components for the different ferry terminals and the requirements from BKK. Note that the figure shall be read as the difference between the upper and lower value for the respective ferry terminal at the y-axis.

5.2 VOC AFE rectifier with LCL-filter

The simulation scheme for the VOC AFE rectifier with LCL-filter is illustrated in figure 43. The main circuit is according to figure 23. Under nominal load conditions are the parameters as described in table 10. Parameters for the PI-controllers are given in table 11. Different load conditions were connected on the dc busbar. Starting on 50%, 75%, 100% of nominal load up to 125%. Load changes are simulated as a step every 0.2 seconds, starting from 0.2 to 0.6 seconds. The subsystems explained in section 5.1.1 to 5.1.4 are also valid in this section. As a result for introducing the LCL-filter, will the quadrature current i_q differs from zero and from equation 4.34, yields 0.1994A. This setpoint is configured in the controller subsystem.

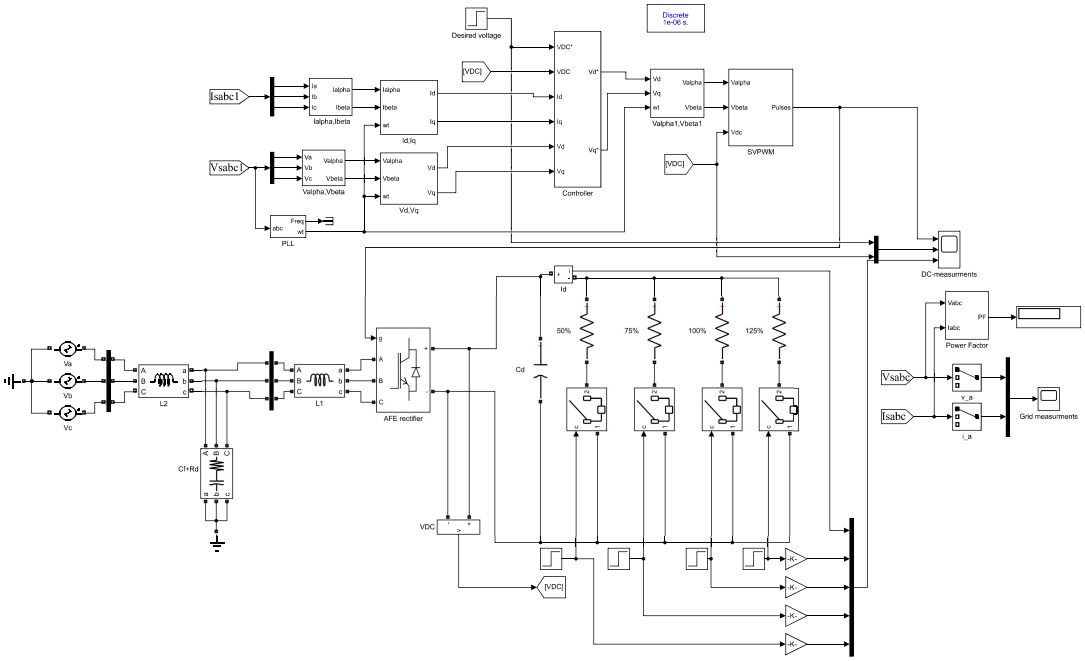


Figure 43: Simulation scheme for the VOC AFE rectifier with LCL-filter in Simulink.

Table 10: Parameters for the VOC AFE rectifier with LCL-filter

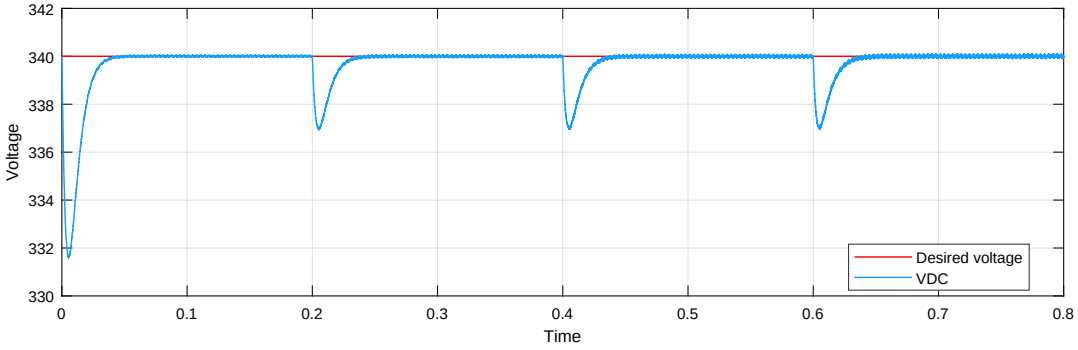
Parameter	Value	Unit
Inductor L_1	3.4	mH
Inductor L_2	1.8	mH
Capacitor C_f	5.0	µF
Resistor R_d	6.0	Ω
Capacitor C_d	1500	µF
Resistor R_{load}	38.5333	Ω
DC bus voltage V_{dc}	340	V
Grid line voltage $V_{LL_{RMS}}$	220	V
Grid frequency f	50	Hz
Switching frequency f_{sw}	5.0	kHz
Sampling time T_s	1.0	µs

Table 11: Parameters for the outer voltage controller and the two inner current controllers.

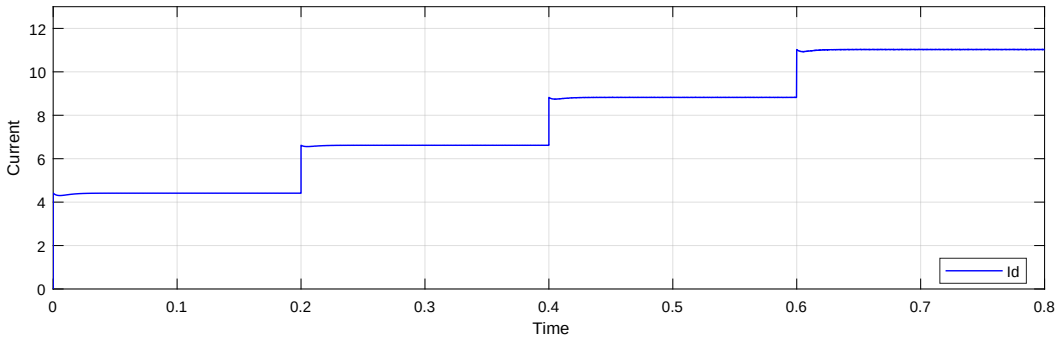
Controller	Proportional constant	Integral constant	Initial conditions
Voltage v_{dc}	0.65	65	0
Current i_d	150	20	-295.8
Current i_q	150	20	-28.708

5.2.1 Results

The dc busbar voltage is shown in figure 44a. The red solid line is the reference value and the solid blue line is the measured dc busbar voltage. Under load changes is the voltage drop approximated 3V. The steady state voltage error peak to peak is 0.11V under nominal load conditions. This is 0.03% of nominal dc voltage. Figure 44b shows the dc busbar current under the same load conditions as mentioned before. The steady state current error is approximated 0.8 mA under nominal load. Figure 45 shows the grid phase voltage and the grid phase current. As seen the voltage and current are in phase under all load conditions. For readability the phase current is scaled by a factor of nine. Only phase a is shown but the same



(a) Waveform for the dc busbar voltage. Note that the load increases at time 0.2,0.4 and 0.6 and hence a voltage drop is measured. Steady state voltage error is $\ll 1\%$.



(b) Waveform for the dc busbar load current. Note that the load increases at time 0.2,0.4 and 0.6 and hence the current increases.

Figure 44: Simulated dc voltages and dc current under load conditions from 50% to 125% of nominal load.

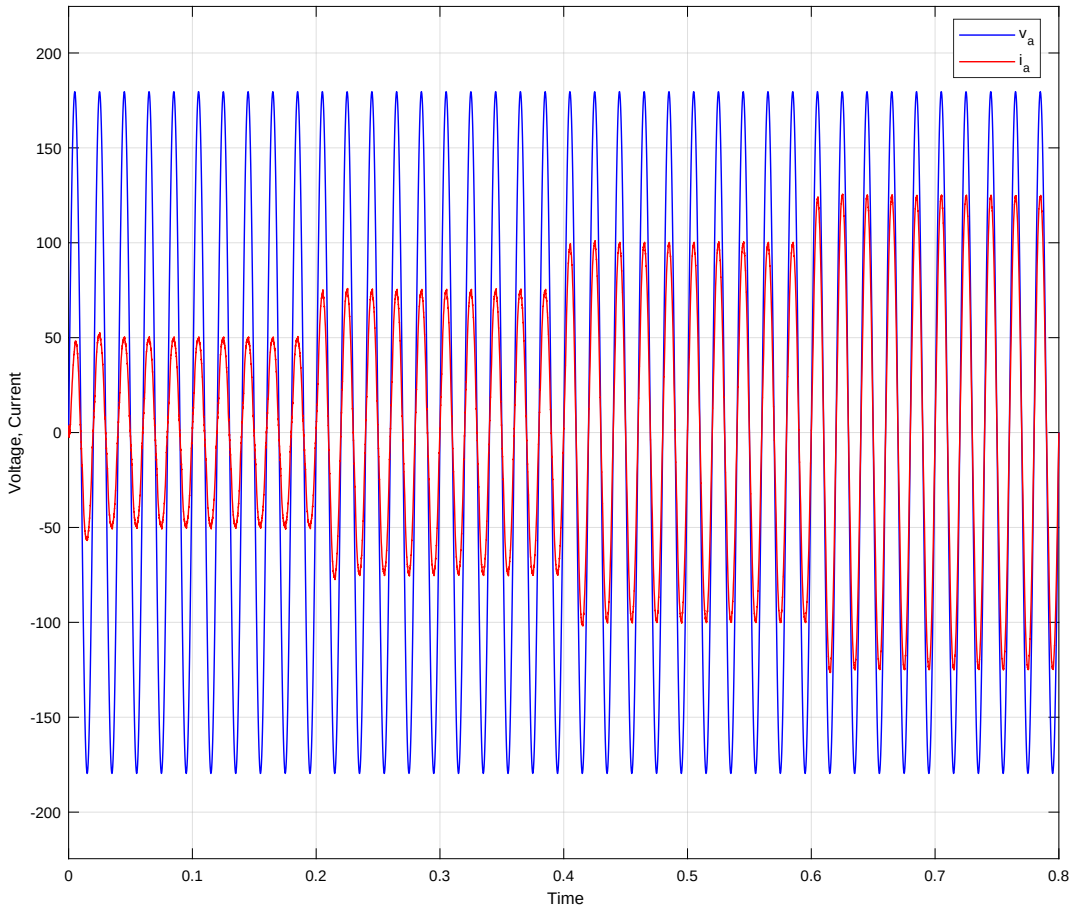


Figure 45: Waveforms for the grid phase voltage and the grid phase current in phase a. Note that the phase voltage and phase current are in phase and have almost no harmonic components. The phase current is enhanced by a factor nine for readability.

result applies for phase b and c. The Bode plot for the attenuation of high order switching components influencing the grid is illustrated in 46. It can be seen from the plot that the LCL-filter behaves as a L-filter in the low frequency region. Here the attenuation is minus 20dB/decade. In the high frequency region has the filter an attenuation factor of minus 60dB/decade. The THD measured in the phase current from the utility grid is shown in figure 47a-47d. Under nominal load the THD_i is approximated 2% and 1.6% under 125% of nominal load. Only phase a is shown but the same results applies to phase b and c. From the foregoing discussion it can bee seen that the PF is approximated unity under all simulated load conditions.

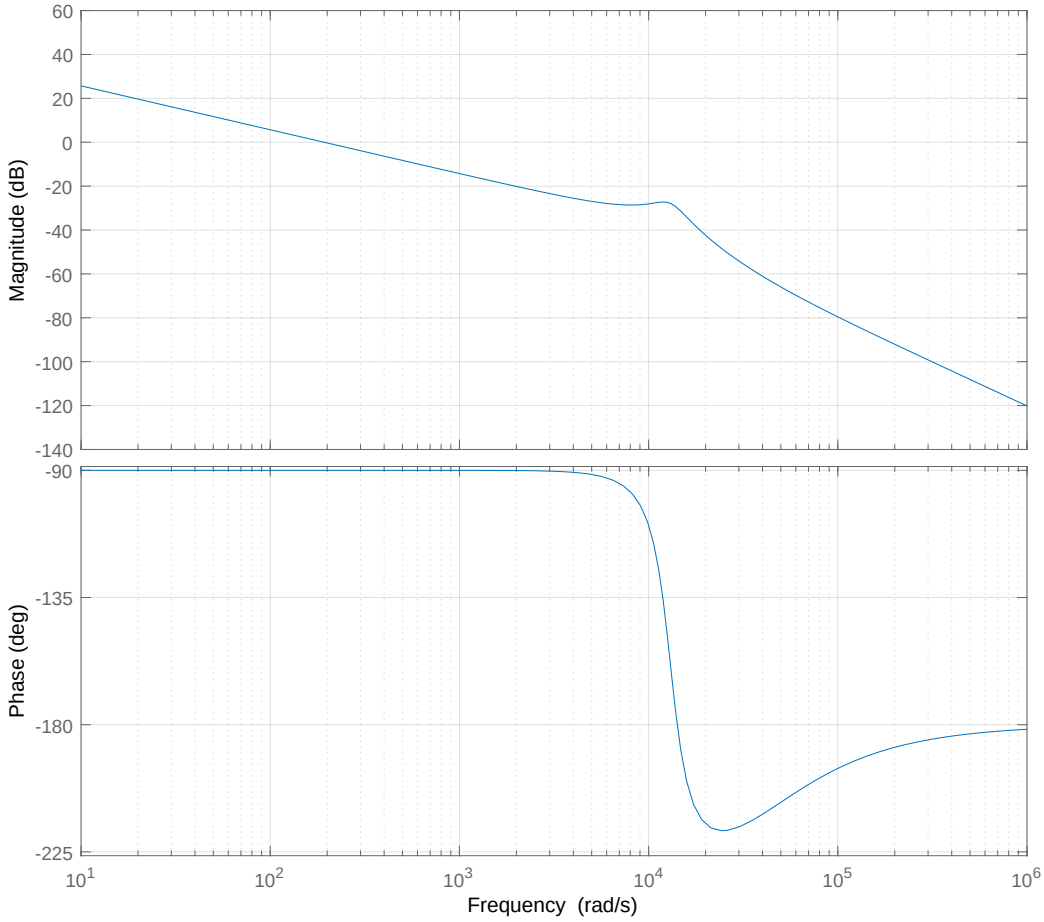
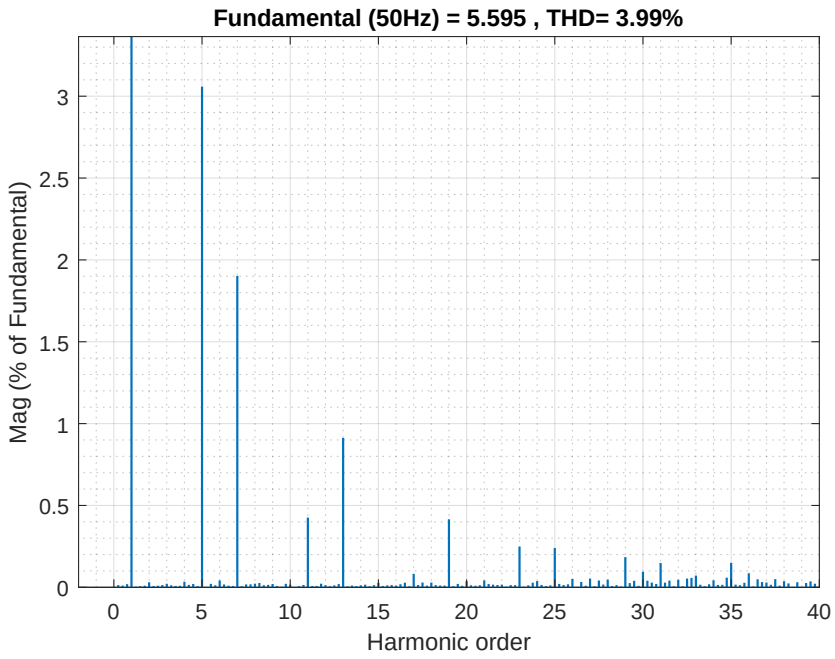
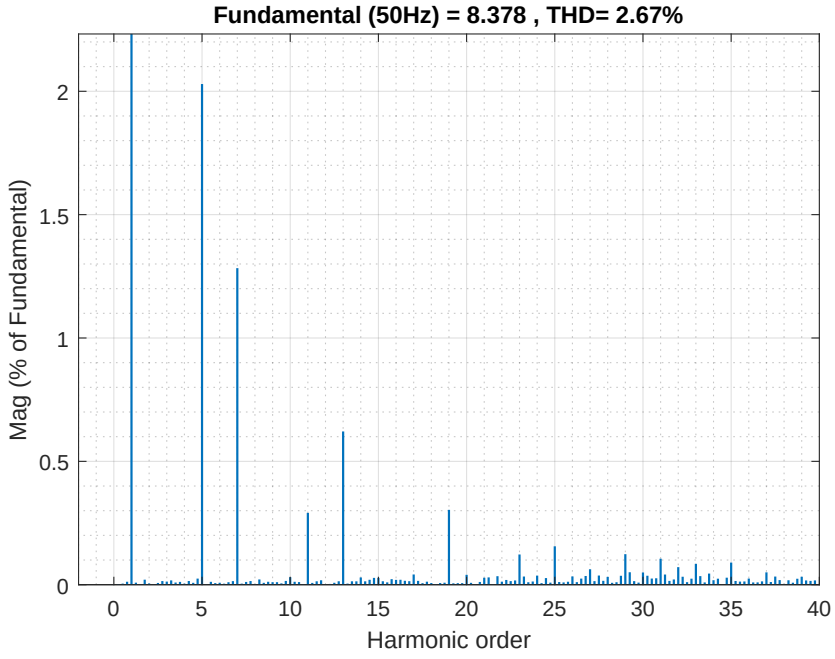


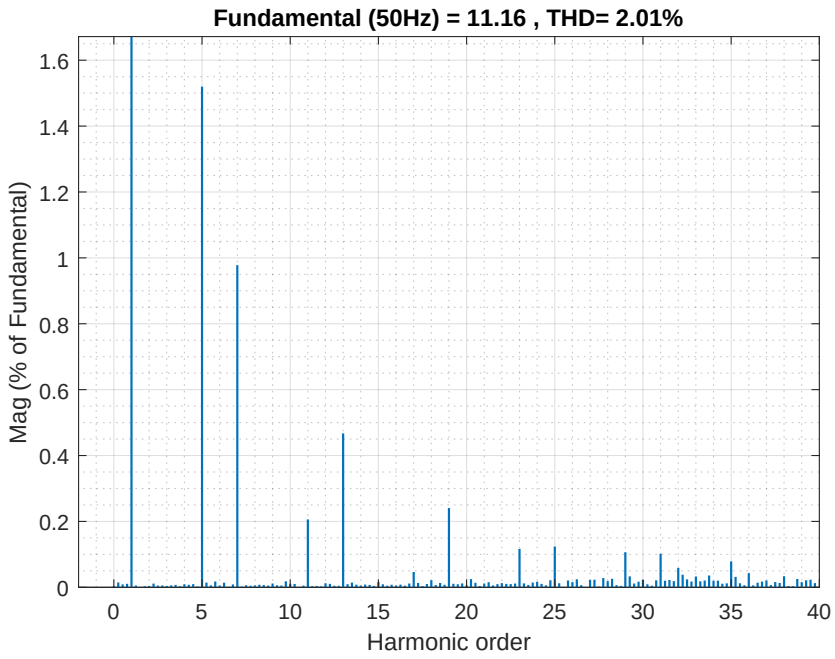
Figure 46: Bode plot for the the admittance transfer function given by equation 4.52. Note that the LCL-filter behaves like a first order filter in the low frequency region with minus 20dB/decade attenuation. In the high frequency region has the LCL-filter an attenuation factor of minus 60dB/decade.



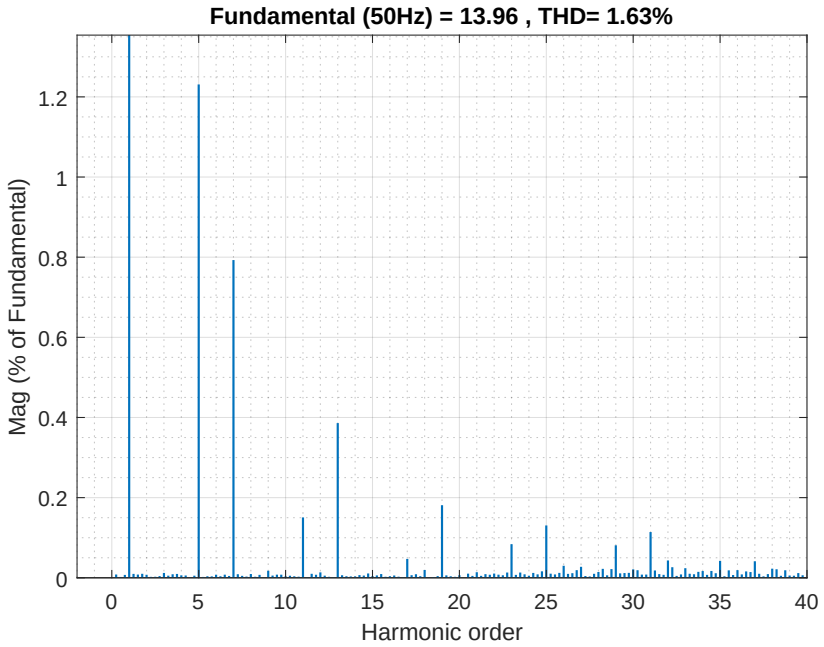
(a) THD_i for phase a under 50% load condition.



(b) THD_i for phase a under 75% load condition.



(c) THD_i for phase a under nominal load condition.

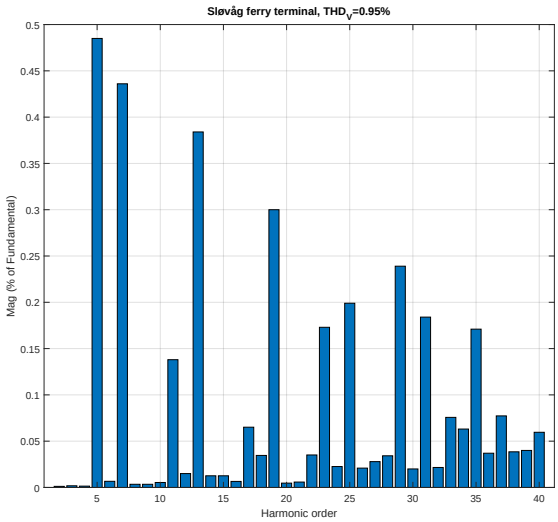


(d) THD_i for phase a under 125% load condition.

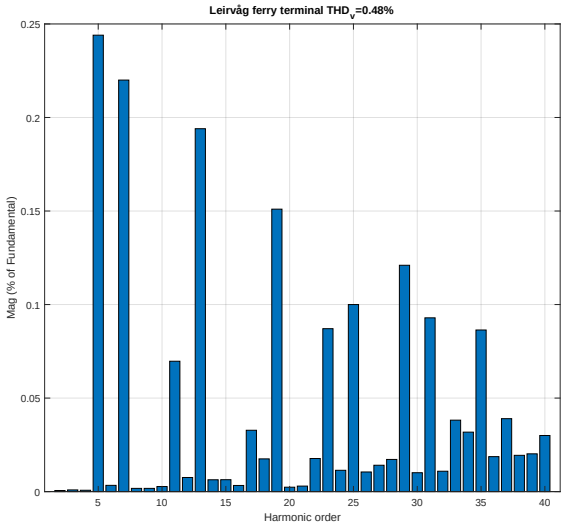
Figure 47: THD_i under load conditions from 50% to 125% of nominal load. The harmonic order axis is normalized regards to the fundamental frequency. Only phase a is shown, but similar results applies for phase b and c.

5.2.2 Grid calculations

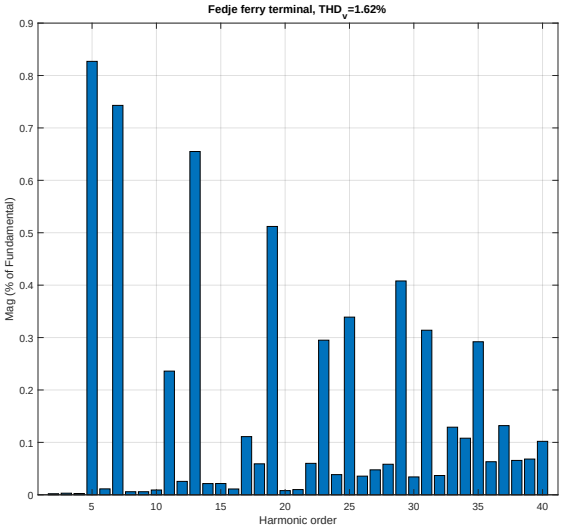
The harmonic voltage components are calculated with the same assumptions as in section 5.1.6. The only difference is that the current components used in the calculation comes from figure 47c. Figure 48a to 48g shows the $\%V'_{h_{PCC}}$ for the ferry terminals up to the 40th harmonic. THD_v is shown at the top of each figure. Figure 49 compares the harmonic voltage components between each ferry terminal to the requirements defined by BKK in table 2. The three-phase power loss over the LCL-filter is calculated to 45.8kW in appendix C.



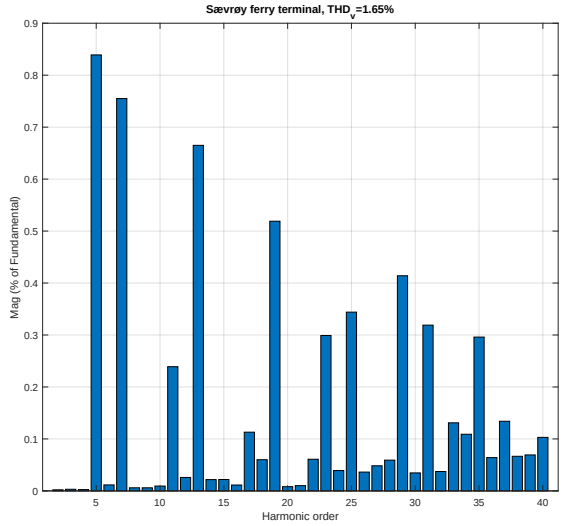
(a) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Sløvåg ferry terminal.



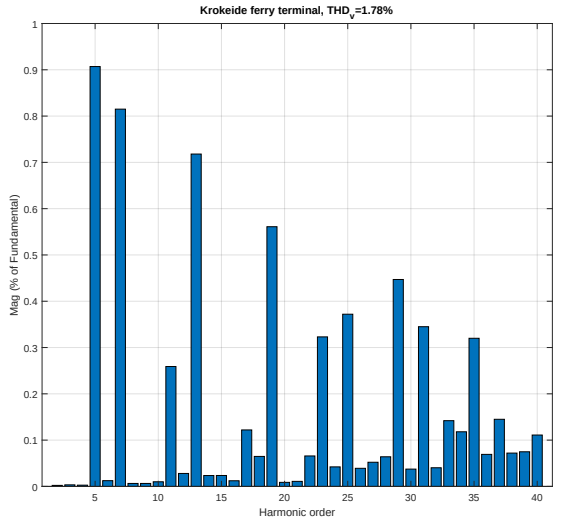
(b) Harmonic components $\%V'_{h_{PCC}}$ and THD_v for Leirvåg ferry terminal.



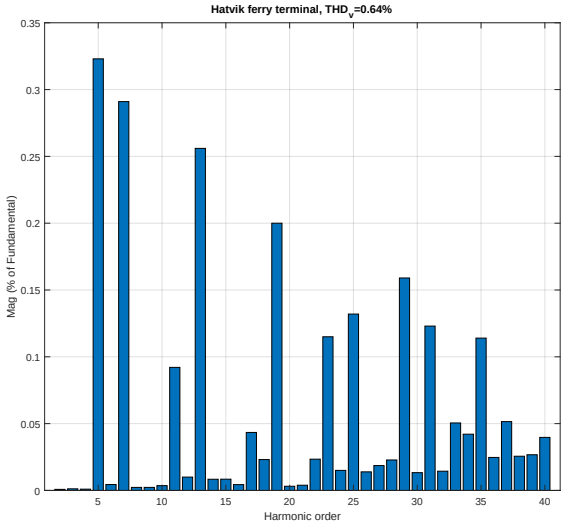
(c) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Fedje ferry terminal.



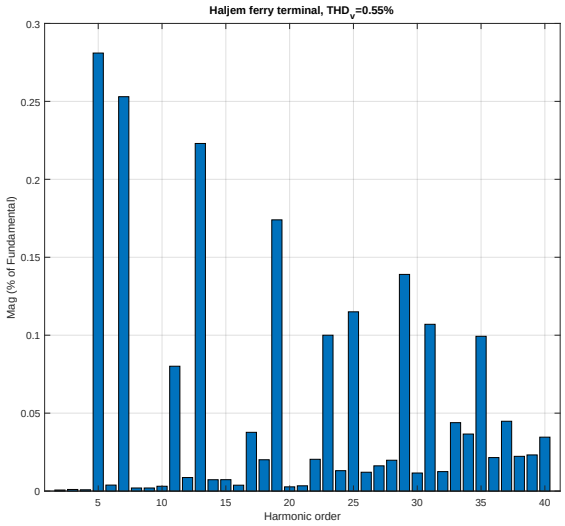
(d) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Sævrøy ferry terminal.



(e) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Krokeide ferry terminal.



(f) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Hatvik ferry terminal.



(g) Harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for Haljem ferry terminal.

Figure 48: Individual harmonic voltage components $\%V'_{h_{PCC}}$ and THD_v for the ferry terminals in table 1. Grid parameters from table 8 and the harmonic current components under nominal load were used for the calculations.

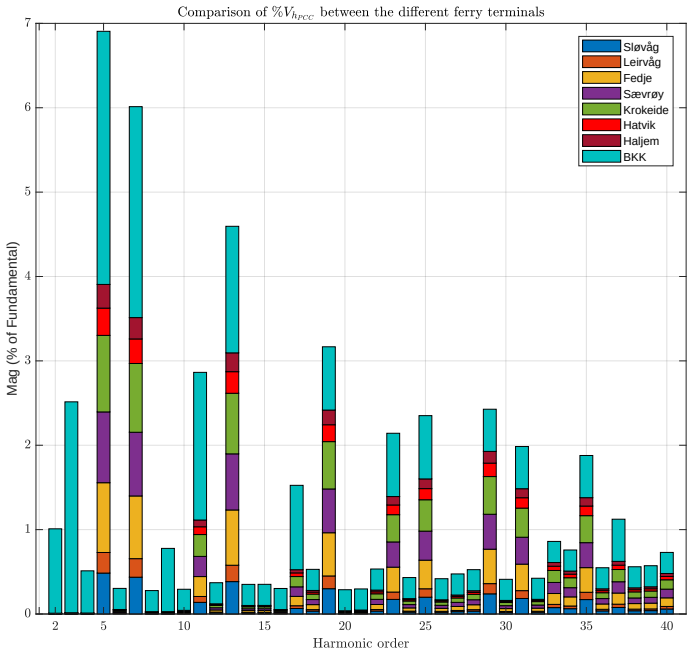


Figure 49: Comparison of the harmonic voltage components for the different ferry terminals and the requirements from BKK. Note that the figure shall be read as the difference between the upper and lower value for the respective ferry terminal at the y-axis.

6 Laboratory model

The realization of a scaled model is based on the VOC AFE rectifier discussed in section 4.1 and simulated in section 5.1. The reason for choosing the VOC AFE rectifier with L-filter instead of LCL-filter, is because of simplicity regarding available components in the laboratory. This is also the reason the maximum output power is limited to 3kW. The laboratory model is illustrated in figure 50.

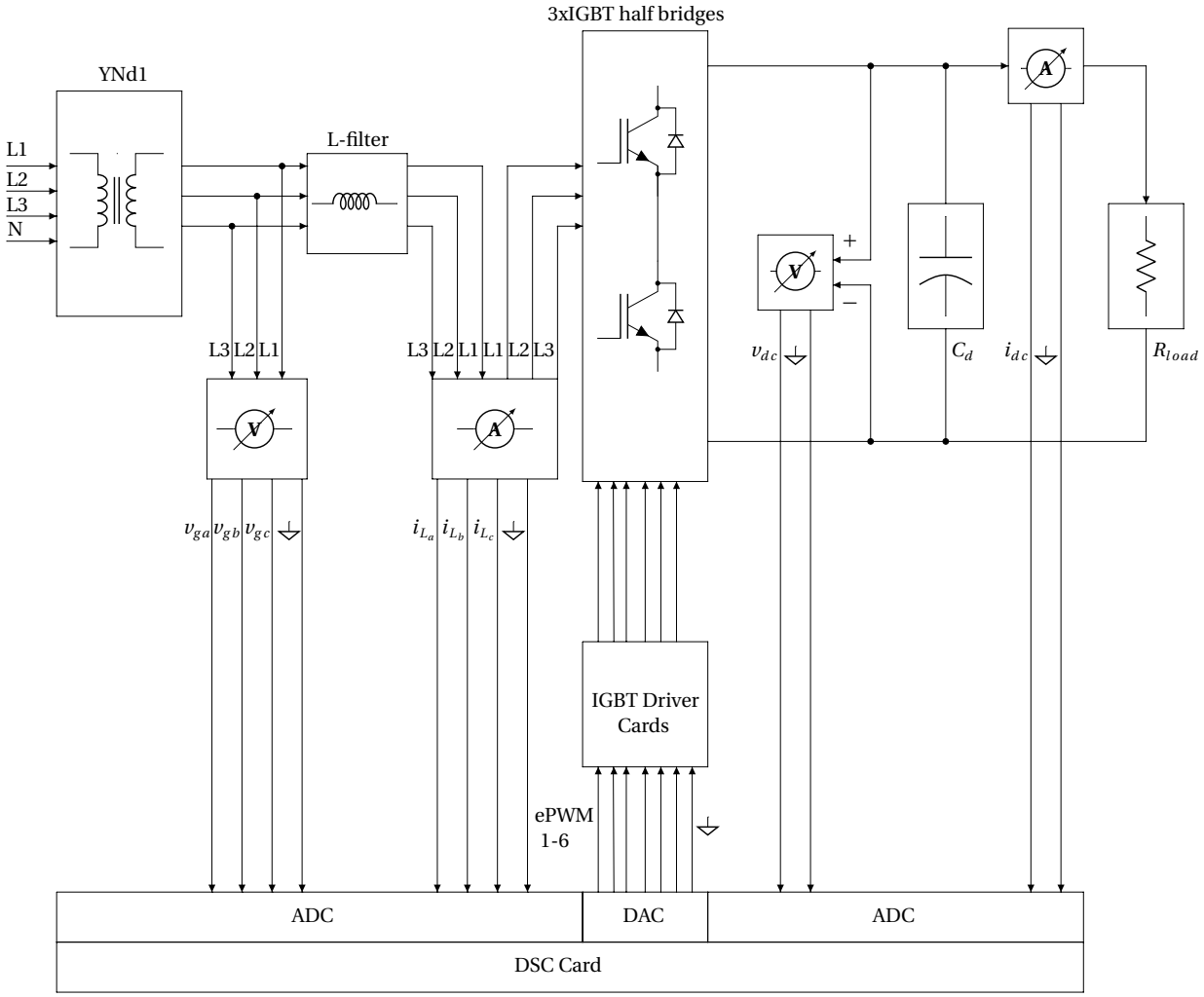


Figure 50: Block scheme of the laboratory model for the VOC AFE rectifier.

The VOC AFE rectifier system is fed by a YNd1 coupled transformer. The transformer's primary side is connected to a TN-S 3x400V system and the secondary side is transformed to 3x230V. Measured line voltages, line currents and dc components are fed to an analog to digital converter (ADC) located on the digital signal

Table 12: Parameters for the VOC AFE laboratory model.

Parameter	Value	Unit
Inductor L	10.0	mH
Capacitor C_d	1525	µF
Resistor R_{load}	38.5333	Ω
DC bus voltage V_{dc}	340	V
Grid line voltage $V_{LL_{RMS}}$	230	V
Grid frequency f	50	Hz
Switching frequency f_{sw}	5.0	kHz
Sampling time T_s	100	µs

controller (DSC). The PWM signals generated by the digital to analog converter (DAC) is fed to the IGBT driver cards, which are responsible for generating digital switching signals to the IGBTs. The DSC card is connected to a computer which loads the C-code to the target. Code generation from Simulink is used and then loaded to Code Composer Studio (CCS). Parameters for the components in the laboratory model are shown in table 12. The inductors and capacitors values deviates from the values in table 6 because of limited available equipment in the laboratory.

6.1 IGBT loss calculation and cooling demand

Three IGBT half bridges are used in the laboratory model in figure 50. The IGBTs used are the SKM100GB12T4 from Semikron. From the datasheet [31] the maximum collector emitter voltage is 1200V and the maximum continuous collector current is 100A. This is more than enough for the 3kW connected load. The IGBT half bridges are mounted on a heat sink to avoid thermal runaway. Therefore the total power losses must be calculated. The total power losses in the IGBT half bridges can be divided into conduction and switching losses in the transistors and the conduction and switching losses in the freewheeling diodes. Blocking and driver losses are omitted because they account only for a small part of the total losses [32]. Total losses for the transistors yields

$$P_{tot(T)} = P_{cond(T)} + P_{on} + P_{off} \tag{6.1}$$

The average conduction losses are given by

$$P_{cond(T)} = \frac{1}{T_{sw}} \int_{0}^{t_{cond}} V_{CE} I_{CE} \, d\,t \tag{6.2}$$

The switching losses are the sum of the turn off and turn on losses and are given by [33]

$$P_{sw} = P_{on} + P_{off} = f_{sw} \int_{t_1}^{t_2} V_{CE} I_{CE} \, d\,t + f_{sw} \int_{t_3}^{t_4} V_{CE} I_{CE} \, d\,t \tag{6.3}$$

The integration times $t_1 - t_4$ are explained in the standard IEC 60747-9. Starting with the turn on integration times where t_1 is the time when $V_{GE(on)}$ is 10% of its nominal value (1.5V) and t_2 is the time when the collector current i_c is 10% of the nominal load current. The turn off integration times where t_3 is when $V_{GE(on)}$ is 90% of its nominal value (13.5V) and t_4 is the time when i_c is 2% of the nominal load current. It can be seen that the conduction losses are dependent on the duty cycle and the switching losses are dependent of the switching frequency. Other factors like junction temperature, dc bus voltage and load type also effects the losses but are not discussed further.

The total losses for the freewheeling diode is expressed as

$$P_{tot(D)} = P_{cond(D)} + P_{rr} \tag{6.4}$$

The conduction losses for the diode is given by

$$P_{cond(D)} = f_{sw} \int_{t_{cond}}^{T_{sw}} V_F I_F \, d\,t \tag{6.5}$$

When the freewheeling diode is turned off it generates switching losses and is called

reverse recovery losses. It is expressed by [33]

$$P_{rr} = f_{sw} \int_{t_5}^{t_6} V_F I_F \, d\,t \tag{6.6}$$

The integration times $t_5 - t_6$ are explained in the standard IEC 60747-2. t_5 is the time when the diode reverse current I_F reach the zero crossing and t_6 is the time when I_F is 2% of the maximum reverse recovery current I_{rrm}.

The power loss calculation for the IGBTs in the VOC AFE rectifier can be simplified where transistors and diode switching times are omitted. Further are linear modulation and constant junction temperature assumed. From [32] are the losses for a CB-PWM converter explained and equation 6.7 and 6.11-6.13 are derived. The VOC rectifier uses SVPWM and thus omit selected switching operations. It implies that the switching looses will be lower regards to CB-PWM and hence the calculated switching losses below are conservative. However it gives a good indication for the power losses in the IGBTs half bridges. The conduction losses for each transistor is given by

$$P_{cond(T)} = \left(\frac{1}{2\pi} + \frac{m \cos \pi}{8} \right) V_{CE0}(T_j) I_{max} + \left(\frac{1}{8} + \frac{m \cos \phi}{3\pi} \right) r_{CE}(T_j) I_{max}^2 \tag{6.7}$$

V_{CE0} is the withstand voltage between collector and emitter when the load current is zero and hence the gate are open. From the data sheet [31], are V_{CE0} 0.7V and r_{CE} equals 15mΩ when the junction temperature T_j is 150 °C. The modulation index m are derived from the controller scheme in figure 20 and yields

$$m = \frac{|\mathbf{V}^*|}{V_{dc}} = \frac{\left[\left(V_d + \omega L i_q + \Delta V_d \right)^2 + \left(V_q - \omega L i_d - \Delta V_q \right)^2 \right]^{\frac{1}{2}}}{V_{dc}} \tag{6.8}$$

Under nominal load conditions with UPF

$$m = \frac{\left[230^2 - (2 \cdot \pi \cdot 50 \cdot 0.008 \cdot 10.65)^2 \right]^{\frac{1}{2}}}{340} = 0.6810 \tag{6.9}$$

and thus the conduction losses for the transistors yields ($\cos\phi = -1$ due to definition in [32])

$$P_{cond(T)} = \left(\frac{1}{2\pi} - \frac{0.6810}{3\pi}\right)0.7 \cdot 10.65 + \left(\frac{1}{8} - \frac{0.6810}{3\pi}\right)0.015 \cdot 10.65^2 \tag{6.10}$$
$$P_{cond(T)} = 0.7376W$$

The switching losses for each transistor is expressed by

$$P_{sw(T)} = f_{sw} E_{on+off} \frac{\sqrt{2}}{\pi} \frac{I_{rms}}{I_{C_{nom}}} \left(\frac{V_{CC}}{V_{CC_{nom}}}\right)^{K_v} \left[1 + TC_{E_{sw}}\left(T_j - T_a\right)\right] \tag{6.11}$$

The energy associated with turning the transistors on and off are represented by the E_{on+off} and are given in the data sheet [31]. V_{CC} are the supply voltage and TC_{sw} is a temperature coefficient of the switching losses. Given nominal load the switching losses per transistor yields

$$P_{sw(T)} = 5000 \cdot 25.2 \cdot 10^{-3} \cdot \frac{\sqrt{2}}{\pi} \frac{7.5307}{100} \left(\frac{340}{600}\right)^{1.3} [1 + 0.003(150\,^{\circ}\mathrm{C} - 25\,^{\circ}\mathrm{C})] \tag{6.12}$$
$$P_{sw(T)} = 2.8067W$$

The conduction losses per freewheeling diode is given by

$$P_{cond(D)} = \left(\frac{1}{2\pi} - \frac{m\cos\phi}{8}\right) V_{F0}(T_j) I_{max} + \left(\frac{1}{8} - \frac{m\cos\phi}{3\pi}\right) r_F(T_j) I_{max}^2 \tag{6.13}$$

V_{F0} is the withstand voltage over the freewheeling diode under blocking stage and r_F is the equivalent resistance. From equation 6.13 and parameters from the data sheet [31]

$$P_{cond(D)} = \left(\frac{1}{2\pi} + \frac{0.6810}{8}\right)0.9 \cdot 10.65 + \left(\frac{1}{8} + \frac{0.6810}{3\pi}\right)12.5 \cdot 10^{-3} \cdot 10.65^2 \tag{6.14}$$
$$P_{cond(D)} = 2.6211W$$

The reverse recovery or switching losses per freewheeling diode are expressed as

$$P_{sw(D)} = f_{sw} E_{rr} \frac{\sqrt{2}}{\pi} \left(\frac{I_{rms}}{I_{C_{nom}}}\right)^{K_i} \left(\frac{V_{CC}}{V_{CC_{nom}}}\right)^{K_v} \left[1 + TC_{E_{rr}}\left(T_j - T_a\right)\right] \tag{6.15}$$

E_{rr} is the energy associated with the stored charge that must be discharged before the freewheeling diode blocks the reverse voltage. $TC_{E_{rr}}$ is a temperature coefficient of the switching losses.

$$P_{sw(D)} = 5000 \cdot 5.9 \cdot 10^{-3} \frac{\sqrt{2}}{\pi} \left(\frac{7.5307}{100}\right)^{0.6} \left(\frac{340}{600}\right)^{0.6} [1 + 0.006(150\,^{\circ}\mathrm{C} - 25\,^{\circ}\mathrm{C})] \tag{6.16}$$

$$P_{sw(D)} = 3.5021\,W$$

The total losses per transistor, freewheeling diode and IGBT module are given by

$$P_{tot(T)} = P_{cond(T)} + P_{sw(T)} = 3.5443\,W \tag{6.17}$$

$$P_{tot(D)} = P_{cond(D)} + P_{sw(D)} = 6.1232\,W \tag{6.18}$$

$$P_{tot(M)} = 2 \cdot \left(P_{tot(T)} + P_{tot(D)}\right) = 19.3350\,W \tag{6.19}$$

The total losses with $n = 3$ modules are given by

$$P_{tot} = n \cdot P_{tot(M)} = 3 \cdot 19.3350 \tag{6.20}$$

$$P_{tot} = 58.0047\,W$$

The efficiency of the IGBT modules are therefore

$$\eta = \frac{3000 - 58.0047}{3000} \cdot 100\% = 98.0665\% \tag{6.21}$$

To ensure that the IGBT modules are not overheated it is necessary to calculate the operating temperature under nominal load. The power losses were calculated under maximum junction temperature of 150°C. This is a conservative assumption and will validate that the IGBT modules will not suffer from thermal runaway. The junction temperature is expressed by

$$T_j = P_{tot} \cdot R_{eq(j-a)} + T_a \tag{6.22}$$

where T_a is the ambient temperature and $R_{eq(j-a)}$ is the thermal resistance from the IGBT modules to the surrounding air. Each IGBT module can be modulated by four power sources corresponding to switching and conduction losses in the upper and

lower transistor and freewheeling diode. The common baseplate is represented by a thermal resistance in series with the parallel branches [34]. The foregoing discussion is illustrated in figure 51. The equivalent thermal resistance in each

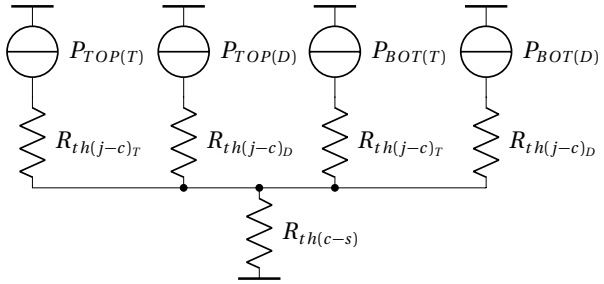


Figure 51: Calculation of thermal resistance per IGBT module. Adapted from [34].

module is calculated by

$$R_{th(j-s)_M} = \left(\frac{2}{R_{th(j-c)_T}} + \frac{2}{R_{th(j-c)_D}} \right)^{-1} + R_{th(c-s)} \tag{6.23}$$

$$R_{th(j-s)_M} = \left(\frac{1}{0.27} + \frac{1}{0.48} + \frac{1}{0.27} + \frac{1}{0.48} \right)^{-1} + 0.04 = 0.1264°\text{C}/W$$

where $R_{th(j-c)}$ is the thermal resistance between the junction to the baseplate of the IGBT and $R_{th(c-s)}$ is the thermal resistance between the IGBT baseplate and the heat sink.

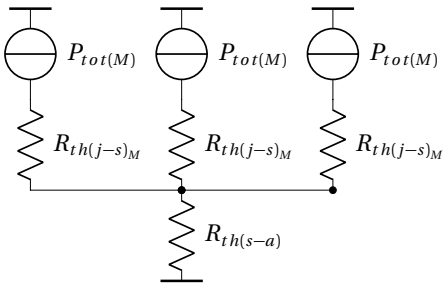


Figure 52: Calculation of the equivalent thermal resistance from the three IGBT modules to a common heat sink to ambient room temperature. Adapted from [32].

The thermal resistance between the junction of the IGBTs to the heat sink $R_{th(j-s)_M}$ for each module were calculated in equation 6.23 and all three IGBT module are connected to the same heat sink as shown in figure 52. The heat sink is illustrated in figure 53 were the length $l = 18$cm, the width $w = 12.5$cm and the height $h =$ 13.5cm. The thermal resistance from the heat sink to the surrounding air are given

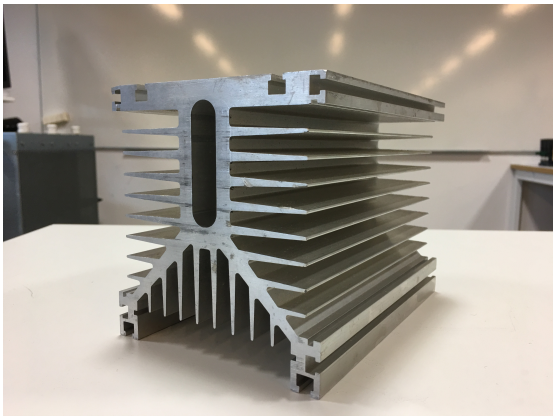


Figure 53: Heat sink used for the IGBT modules.

by a radiative and convective component. The later is expressed as [14]

$$R_{th_{conv}} = \frac{1}{1.34 \cdot F_{red} \cdot A_{conv}} \left(\frac{d_{vert}}{\Delta T} \right)^{\frac{1}{4}} \tag{6.24}$$

where F_{red} is a reduction factor related to reduced effect of convection due to the spacing d_s between the cooling fins ($d_s = 9\text{mm}$). d_{vert} is the vertical height of the heat sink. The approximate effective value of the exposed area to convection is given by

$$A_{conv} = 16 \cdot 0.18 \cdot (0.135 - 0.02 - 0.018) = 0.2794\text{m}^2 \tag{6.25}$$

It is assumed that there are only horizontal cooling fins (eight cooling fins) in full length and width of the heat sink body. The reduction factor are given in [14] and hence

$$R_{th_{conv}} = \frac{1}{1.34 \cdot 0.2794 \cdot 0.78} \left(\frac{0.097}{(150 - 25)} \right)^{\frac{1}{4}} = 0.5715^{\circ}\text{C}/W \tag{6.26}$$

The radiative thermal resistance is expressed as

$$R_{th_{rad}} = \frac{\Delta T}{P_{rad}} \tag{6.27}$$

and the heat transfer given by radiation is given by [14]

$$P_{rad} = 5.7 \cdot 10^{-8} E \cdot A \left(T_s^4 - T_a^4 \right) \tag{6.28}$$

where the emissivity E is typically 0.06 for rough aluminum finish [35]. Combining equation 6.27 into 6.28 with the $E = 0.06$ yields

$$R_{th_{rad}} = \frac{\Delta T}{0.5310A\left[\left(\frac{T_s}{100}\right)^4 - \left(\frac{T_a}{100}\right)^4\right]} \tag{6.29}$$

The outer surface area is given by

$$A = 2 \cdot 0.18 \cdot 0.135 + 2 \cdot 0.135^2 = 0.0851\text{m}^2 \tag{6.30}$$

and thus

$$R_{th_{cond}} = \frac{423.1 - 298.15}{0.5310 \cdot 0.0851\left[\left(\frac{423.15}{100}\right)^4 - \left(\frac{298.15}{100}\right)^4\right]} \tag{6.31}$$

$$R_{th_{cond}} = 11.45\text{°C}/W$$

The effect of convection and radiation yields

$$R_{th(s-a)} = \left(\frac{1}{R_{th_{cond}}} + \frac{1}{R_{th_{rad}}}\right)^{-1} \tag{6.32}$$

$$R_{th(s-a)} = \left(\frac{1}{0.5715} + \frac{1}{11.45}\right)^{-1} = 0.5443\text{°C}/W$$

From equation 6.20,6.22,6.23 and 6.32, yields the resulting junction temperature

$$T_j = 58.0047(0.1264 + 0.5443) + 25 = 63.9056\text{°C} \tag{6.33}$$

The maximum continuous operation temperature of the junction should be below 125 °C [32]. Hence a maximum junction temperature of 63.9056 °C under nominal load causes no risk of thermal runaway.

6.2 IGBT driver card

The IGBT driver card shown in figure 54 has several functions. Some are briefly presented [36]

1. Interlock function that prevent two IGBTs on each half bridge to switch on

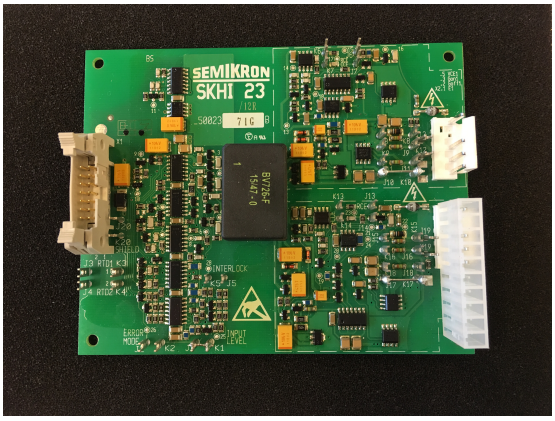


Figure 54: Driver card SKHI 23/12 (R) from Semikron. Digital input signal on the left from the DSC card and digital output signal on the right to a IGBT half bridge.

at the same time. Therefore adjustable dead time is available. By default the dead time τ_d is 10µs.

2. Error memory which prevents the transmission of turn-on signal to the IGBTs if a short circuit is detected or the supply voltage V_s to the driver card is under 13V.

3. Galvanic separation from the main circuit.

4. Output buffer providing correct current to the gate of the IGBTs.

There are three IGBT driver cards. One for each IGBT half bridge. The supply voltage for each card is 15V and the digital input voltage from the DSC card is 0-3V. Therefore a soldering between pin J1 and K1 has been done to have an input voltage range between 0-5V. High switching signal yields minimum 2.4V and low switching signal yields maximum 0.5V. If a signal is generated from the error memory it sends a logical high signal to the DSC card by default. Since the Trip-Zone (TZ) on the DSC card require a logical low signal under a short circuit event are the pin J2 and K2 bridged. Thus the error memory uses digital low logic. To realize correct switching speed of the IGBTs and short circuit monitoring, have the resistances R_{Gon} and R_{Goff} to be 15Ω. The standard value mounted on the driver card, R_x =22Ω. It is therefore possible to solder additional parallel resistance between pin J8 to K8 (R_{Gon}) and pin J9 to K9 (R_{Goff}) for the upper IGBT. This is also true for the lower IGBT in the half bridge and hence pin J15 to K15 and J16 to K17 must be bridged

with an external resistor R which is given by

$$R_{Gon} = R_{Goff} = \frac{RR_x}{R+R_x} \tag{6.34}$$
$$R = \frac{R_{Gon}R_x}{R_x - R_{Gon}} = \frac{22 \cdot 15}{22-15} = 47.1429\Omega$$

6.3 DSC card

The digital signal controller card is a microprocessor with a digital signal processor (DSP) as a core unit. Additional peripherals and memory in a single unit complete the DSC card. The DSP used in this project are the TMS320F28335 from Texas Instrument and the DSC card eZdsp are delivered by Spectrum digital. Figure 55 gives an overview of the DSC card and on the lower right corner are the 16 analog inputs.

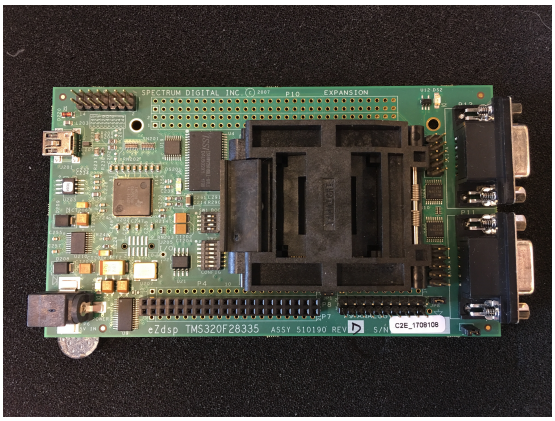


Figure 55: Overview of the eZdsp F28335 digital signal controller card.

The analog voltage and current signals from figure 50 feds the ADC on the DSC card. There are 16 analog inputs and two sequencers, working either in cascade or separately. The analog inputs can be divided into two channels of eight inputs with a dedicated multiplexer (MUX) and a sample and hold (S/H) block. Each channel starts the ADC with a start of conversion (SOC) signal from e.g the ePWM block (enhanced). The signal (voltage or current) selected by the sequencer is kept constant under the S/H acquisition window and then converted and stored in a register. The 12 bit ADC core have conversion time of 12.5MHz or 6.25MSPS

(Million samples per second). The digital value is derived by [37]

$$V_{analog} < 0V \qquad V_{digital} = 0 \tag{6.35}$$

$$0V < V_{analog} < 3V \qquad V_{digital} = 4096 \cdot \frac{V_{analog} - ADCLO}{3} \tag{6.36}$$

$$V_{analog} \geq 3V \qquad V_{digital} = 4095 \tag{6.37}$$

where $ADCLO$ represent ground on the ADC module. The inputs to the analog channels are labeled ADCINx0 to ADCINx7, where x is either channel A or B. The digital value after ADC are stored in a result register labeled ADCRESULT1 to ADCRESULT16.

The ePWM peripheral perform DAC and are located at the P8 connector in the lower middle in figure 55. There are three available channels. One channel is labeled ePWMyx, where y is either 1,2 or 3 and x is either A or B. Each channel has a complementary signal and thus EPWM1A is the opposite of ePWM1B. The ePWM block is divided into several submodules and will be briefly discussed [38].

The Time-Base (TB) submodule configures the frequency and waveform of the carrier wave signal for the SVPWM. The clock time from the CPU is labeled $T_{SYSCLKOUT}$ and can be scaled down according to

$$T_{TBLCK} = T_{SYSCLKOUT} \cdot CLKDIV \cdot HSPCLKDIV \tag{6.38}$$

where $CLKDIV$ and $HSPCLKDIV$ are prescaler bits to reduce the input frequency. T_{TBCLK} is the rate at which the time based counter increments or decrements. The CPU clock frequency is expressed as

$$T_{SYSCLKOUT} = \frac{1}{f_{SYSCLKOUT}} \tag{6.39}$$

and the generated carrier wave signal period and frequency is given by

$$T_{PWM} = 2 \cdot TBPRD \cdot T_{TBLCK} \tag{6.40}$$

$$f_{PWM} = \frac{1}{T_{PWM}} \tag{6.41}$$

The time based counter selected is an up and down counter, to generate a symmetrical triangular waveform. $TBPRD$ is the TB period register and combining equation 6.38-6.41 yields

$$TBPRD = \frac{1}{2}\frac{f_{SYSCLKOUT}}{f_{PWM} \cdot CLKDIV \cdot HSPCLKDIV} \tag{6.42}$$

The CPU clock frequency is known from [39] and selecting the prescaler to one relative to the CPU frequency yields

$$TBPRD = \frac{1}{2}\frac{150 \cdot 10^6}{5 \cdot 10^3 \cdot 1 \cdot 1} = 15 \cdot 10^3 \tag{6.43}$$

There are three ePWM modules used in the VOC AFE rectifier application. It is therefore necessary to have a phase shift of 120° between each ePWM channel. The phase shift is represented by

$$TBPHS = \frac{TBPRD}{n}(m-1) \tag{6.44}$$

where n is the number of phases and m is the ePWM module number. ePWM1x is the master module and ePWM2x and ePWM3x is the slave modules with respectively $TBPHS = 5000$ and $TBPHS = 10 \cdot 10^3$.

The Counter-Compare (CC) submodule takes the values in the TBCTR register and compares them with counter-compare A and B register (CMPA and CMPB). CMPA is the control signal generated by the SVPWM block and CMPB is the complementary control signal referred to CMPA . When CMPA is equal to the carrier wave signal, a logical high digital signal is loaded in the CMPCTL register. The Action-Qualifier (AQ) submodule takes the digital values from the CMPCTL register and generates switching signals to the IGBT driver cards according to user defined setting. In this case when the TBCTR is incrementing and CMPA is equal the carrier wave then a logical low is loaded in the AQCTLA register. When TBCTR is decrementing and CMPA is equal the carrier wave then a logical high is loaded in the AQCTLA register. The values from AQCTLA register are then sent to GPIO MUX and to the IGBT driver cards. This is also equivalent for the CMPB and AQCTLB register.

The Dead Band (DB) and PWM-Chopper (PC) submodule are bypassed. The DB submodule are not necessary because it is already configured in the IGBT driver card. The PC submodule allow a high frequency carrier signal to modulate the switching signal generated by the AQ submodule. This feature is not needed in the VOC rectifier application. The TZ submodule is a safety feature that forces the ePWM module to a high impedance level if a short circuit event occurs. Each ePWM module are configured by a one-shot-trip (OSHT), which means that the trip-zone signals has to be manually cleared after a short circuit event. Each ePWM module has its own trip-zone signal with logical low input signals. These trip signals comes from the error memory pin from the IGBT driver cards. The last subsystem is the Event trigger (ET) which specifies when the SOC event occurs for the ADC module. In this application the SOC event is triggered by the ePWM module when $TBCTR = 0$. This is to ensure synchronization between the switching and sampling process. To avoid aliasing effect must the sampling frequency respect the Nyquist Theorem

$$f_s \geq 2 \cdot f_{max} \tag{6.45}$$

where f_s is the sampling frequency and f_{max} is the carrier wave frequency (5kHz).

6.4 Measurement cards

The eZdsp card needs 8 analog measurement signals to the ADC. On the grid side are the line voltages v_a, v_b and v_c measured on dedicated measurement cards. Likewise are the line currents i_a, i_b and i_c sensed on dedicated measurement cards. The dc voltage v_{dc} and dc current i_{dc} on the dc busbar are also sensed on separated measurement cards. The voltage transducer LEM LV-25-P [40] and current transducer LEM LA-100-TP [41] are used in this project. They are capable to measure up to 500V and 100A , which is sufficient for the VOC AFE rectifier.

The input signal level on the ADC are limited to voltages between 0 and 3 volts. It is therefore necessary to change the output signal value from the voltage and current transducers. A circuit similar to figure 56 can be used for this purpose. The

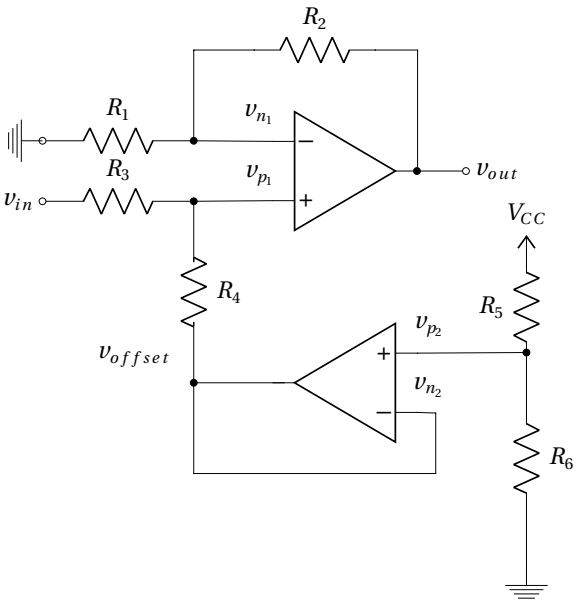


Figure 56: Scaling and offset circuit for voltage and current transducers.

lower operation amplifier (op amp) gives an offset to the incoming signal v_{in} from the voltage or current transducer. The upper op amp is a scaling circuit to assure that the correct output voltage level is achieved. The lower circuit in figure 56 can be analyzed from ideal op amp theory assuming infinite gain and infinite input resistants and thus

$$v_{p_2} = V_{CC}\frac{R_6}{R_5+R_6} \tag{6.46}$$

$$v_{n_2} = v_{offset} \tag{6.47}$$

$$v_{p_2} = v_{n_2} \tag{6.48}$$

$$v_{offset} = V_{CC}\frac{R_6}{R_5+R_6} \tag{6.49}$$

Similar assumption are assumed for the upper op amp circuit and the use of nodal analysis and voltage division yields

$$\frac{v_{in}-v_{p_1}}{R_3}+\frac{v_{offset}-v_{p_1}}{R_4}=0 \tag{6.50}$$

$$v_{n_1} = v_{out}\frac{R_1}{R_2+R_1} \tag{6.51}$$

Assuming that $R_1 = R_3$ and $R_2 = R_4$ and combining equation 6.50 and 6.51 yields

$$v_{out} = \frac{v_{in}R_2 + v_{offset}R_1}{R_1} \tag{6.52}$$

6.4.1 Line voltages

The development of the measurement card for the line voltages is illustrated in figure 57. The power supply section is fed by a PeakTech power supply unit delivering ±15V dc. For effectively filter out both high frequency and low frequency noise, the use of ceramic and electrolytic capacitors is used on the power supply section and ceramic capacitor between V_{CC+}, V_{CC-} and signal ground [42].

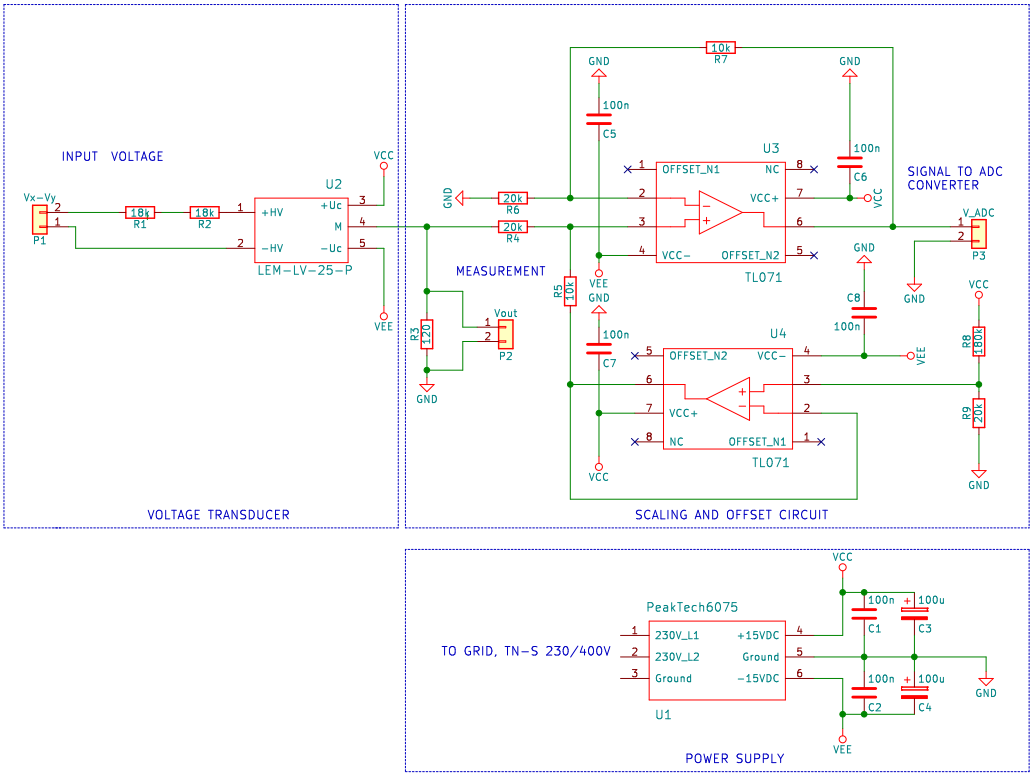


Figure 57: Measurement card for the line voltages. Note that the circuit is divided in a voltage sensing circuit, power supply circuit and a scaling and offset circuit.

The voltage transducer LEM LV-25-P uses a hall-effect sensor to measure the potential difference at the primary side. A current proportional to the measured voltage

must flow through an external resistor R_{eq} and is expressed as

$$R_{eq} = \frac{V_p}{I_{p_n}} - R_{winding} = \frac{360}{0.01} - 225 \approx 36\text{k}\Omega \tag{6.53}$$

The $R_{winding}$ was measured between HV+ and HV- on the LEM LV-25-P sensor and should be subtracted to calculate the external resistor. However due to limited available resistors the $R_{winding}$ was omitted. The nominal voltages to be measured are the line voltages v_{ab}, v_{ba} and v_{ca} and are assumed to be

$$V_n = 230\sqrt{2} = 325.2691\,V \tag{6.54}$$

However to account for higher voltages, the external resistor was calculated under a voltage V_p and nominal primary current I_{p_n} as shown in equation 6.53. Under maximum voltage conditions the primary current are calculated to

$$I_p = \frac{V_p}{R_1 * n + R_{winding}} = \frac{360}{18000 * 2 + 225} = 9.9379\text{mA} \tag{6.55}$$

In nominal conditions as explained in equation 6.54 is the primary current

$$I_{p_n} = \frac{V_n}{R_1 * n + R_{winding}} = \frac{325.2691}{18000 * 2 + 225} = 8.9791\text{mA} \tag{6.56}$$

The external resistors are divided into a series connection of two resistors to decrease the dissipated power over each resistor and each resistor R_1 to R_2 are given by

$$R_1 = \frac{R_{eq}}{n} = \frac{36000}{2} = 18\text{k}\Omega \tag{6.57}$$

Under maximum conditions the dissipated power over R_1 and R_2 are calculated by

$$P_{R_1} = \frac{\left(\frac{V_p}{\sqrt{2}}\right)^2}{R_1} = \frac{\left(\frac{180}{\sqrt{2}}\right)^2}{18000} = 0.9\text{W} \tag{6.58}$$

It was decided to use resistors that can dissipated 5W under nominal conditions due to available equipment in the laboratory. The primary and secondary circuits

are galvanic separated with winding turn ratio given by

$$k = \frac{n_1}{n_2} = \frac{2500}{1000} \tag{6.59}$$

On the secondary side of the transducer is a measuring resistance installed for thermal protection of the output stage. In regards to the maximum input voltage to the ADC converter on the eZdsp card, is the measuring resistance calculated by

$$R_3 = \frac{\text{Maximum ADC input voltage}}{I_{s_n}} = \frac{3}{0.025} = 120\Omega \tag{6.60}$$

The output voltage from the voltage transducer circuit is now a sinusoidal waveform between -3V to 3V. The offset and scaling circuit derived in section 6.4 are used to scale and offset v_{out} to v_{ADC}, which are between 0 and 3V. To determine the scaling resistors R_4 to R_7 is it assumed that the offset circuit is shorted out and a expression for the gain

$$A_{scale} = \frac{v_{out}}{v_{in}} = \frac{R_7}{R_6} = \frac{R_5}{R_4} = \frac{v_{ADC_{range}}}{v_{out_{range}}} = \frac{3V}{3V-(-3V)} = 0.5 \tag{6.61}$$

The derivation of equation 6.61 are derived from appendix D. Assuming that R_4 is 20kΩ and solving equation 6.61 for R_5 yields 10kΩ. To determine the offset resistors R_8 and R_9 in figure 57, are equation 6.52 evaluated when v_{ADC} equal 0V and v_{out} equal -3V.

$$\begin{aligned} 0 &= \frac{-3 \cdot 10k + V_{offset} \cdot 20k}{20k} \\ V_{offset} &= 1.5V \end{aligned} \tag{6.62}$$

Assuming that $R_9 = 20\text{k}\Omega$ and solving equation 6.49 for R_8, yields 180kΩ.

6.4.2 Line currents

The development for the measurement cards for the line currents are illustrated in figure 58.

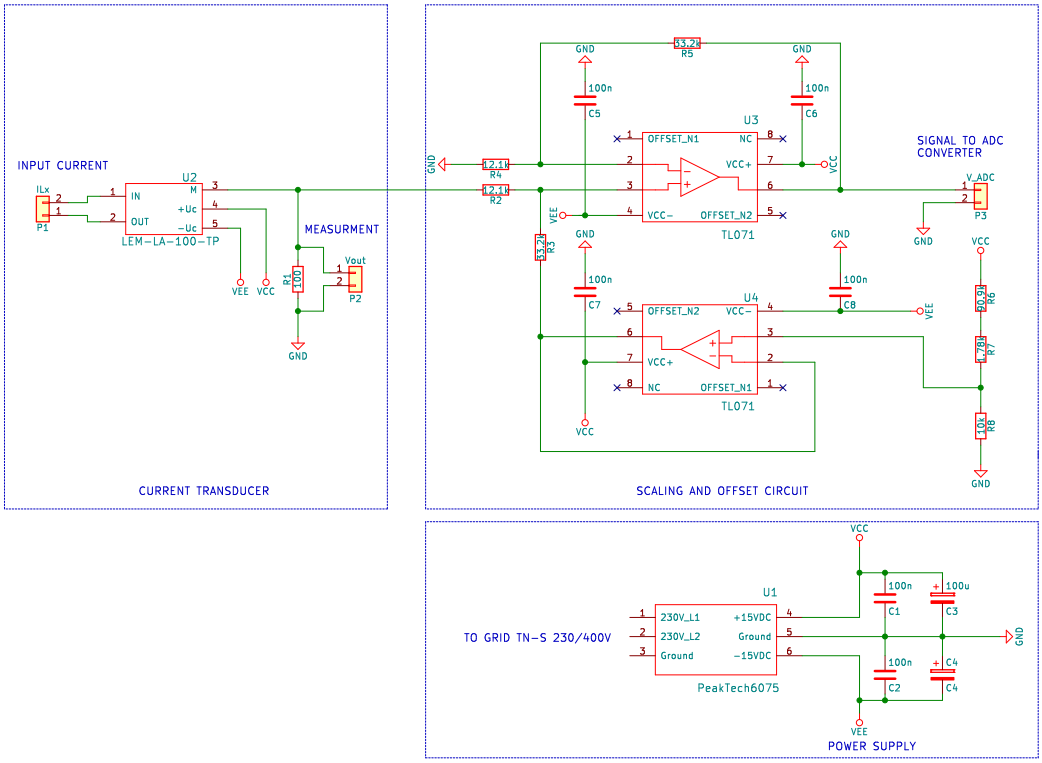


Figure 58: Measurement card for the grid line currents. Note that the circuit is divided in a current sensing circuit, power supply circuit and a scaling and offset circuit.

The amplitude value of the line currents to be measured under nominal load conditions is calculated by

$$I_{p_n} = \frac{P_n}{V_s} = \frac{3000}{230\sqrt{3}}\sqrt{2} = 10.65\text{A} \tag{6.63}$$

The primary and secondary circuit are galvanic separated by a winding turn ratio given by

$$k = \frac{n_1}{n_2} = \frac{1}{2000} \tag{6.64}$$

Thus the secondary current are given by

$$I_{s_n} = I_{p_n}\frac{n_1}{n_2} = \frac{10.65}{2000} = 0.0053\text{A} \tag{6.65}$$

On the secondary side is there a measuring resistor for thermal protection of the

output stage with a maximum value of 110Ω [41]. A measuring resistance of 100Ω was used and therefore the output voltage is

$$v_{out} = I_{s_n} R_1 = \pm 0.0053 \cdot 100 = \pm 0.5325\text{V} \tag{6.66}$$

The scaling and offset resistors were calculated under the same method explained in section 6.4.1.

6.4.3 DC voltage and current

The dc voltage and current measurement card were designed in a similar fashion as the grid voltage and current cards. However the offset circuit is not needed and is therefore not connected to the scaling circuit. Figure 59 and 60 illustrate respectively the dc voltage card and dc current card.

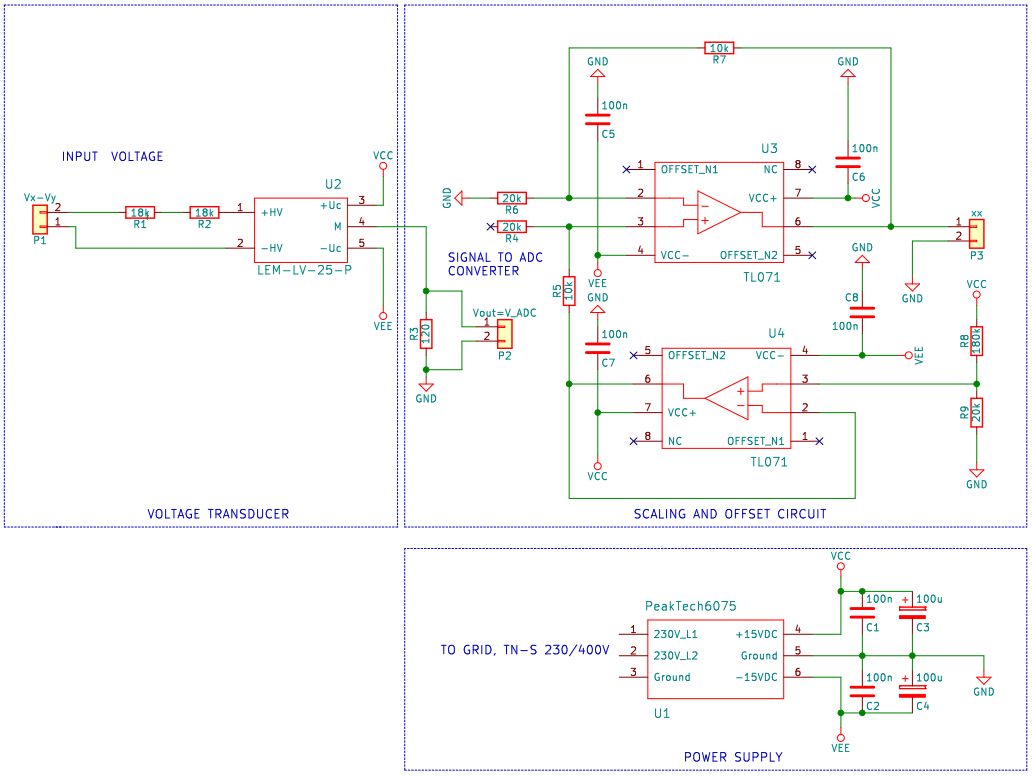


Figure 59: Measurement card for the dc voltage. Note that the scaling and offset circuit is not connected.

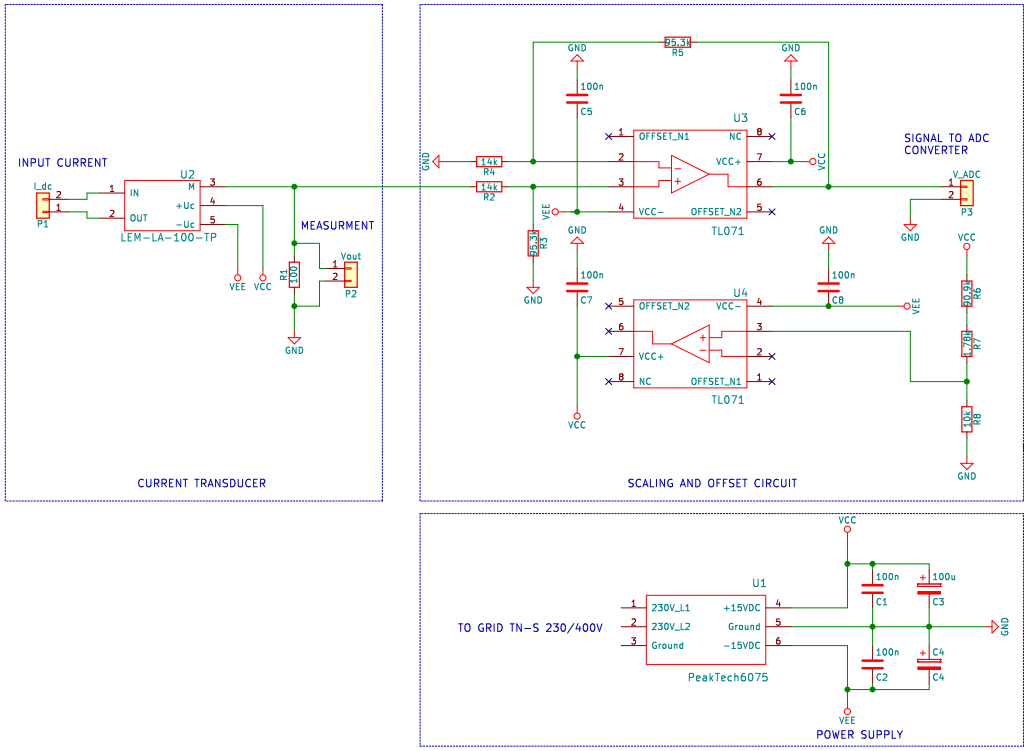


Figure 60: Measurement card for the dc current. Note that the offset circuit is not connected.

6.5 Wiring diagram

A detailed wiring diagram based on the block scheme in figure 50 is drawn in this section. The wiring schemes are divided in figure 61 to 63 for readability. Figure 61 shows the wiring of the measurement for the line/phase voltages (Δ-connected) and line currents. The delta connected transformer feds the L-filter reactors which are connected to the IGBTs in figure 62. The measurement cards voltage supply are provided by PeakTech 6075. The ±15V dc are supplied to each grid measurement card. This is also the case for the dc voltage and dc current measurement cards in figure 63. Figure 62 illustrates the incoming connections to the ADC on the eZdsp card. ePWM signals are sent to each IGBT driver card and also the error output are connected to a dedicated TZ on the eZdsp. The IGBTs are connected to the driver cards with switching signals and V_{CE} monitoring for short circuit detection.

Figure 63 shows the connection on the dc bus. The measured dc voltage and dc

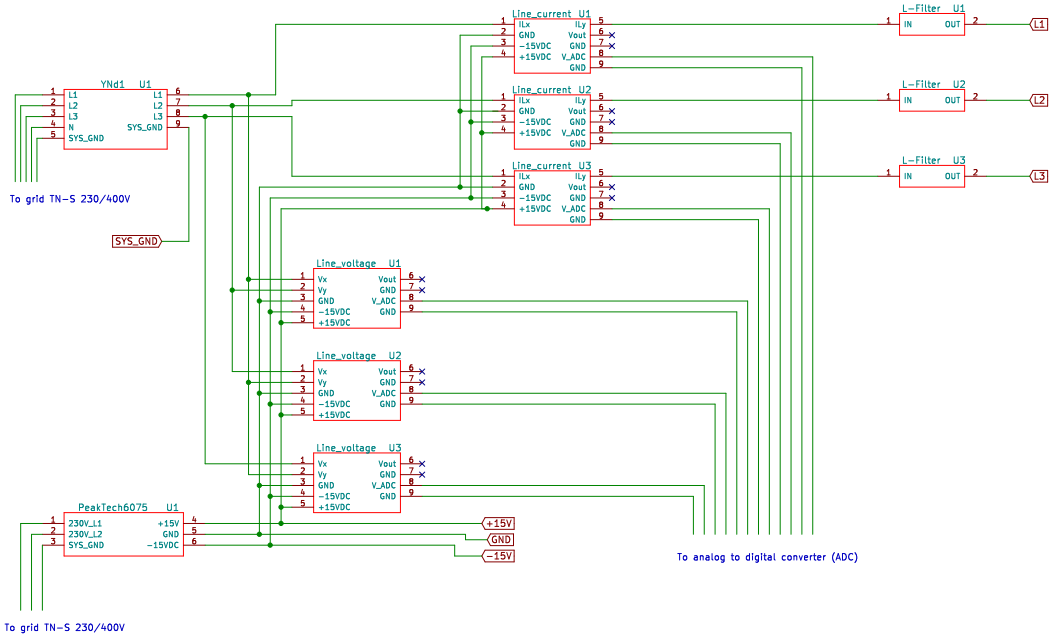


Figure 61: The wiring diagram shows the measurement of line voltages and line currents. The output from the L-filters are connected further to each IGBT half bridge as shown in figure 62. The outputs from the measurement cards are connected to the ADC in figure 62. Note that the connected GND from the PeakTech 6075 is signal ground not system ground.

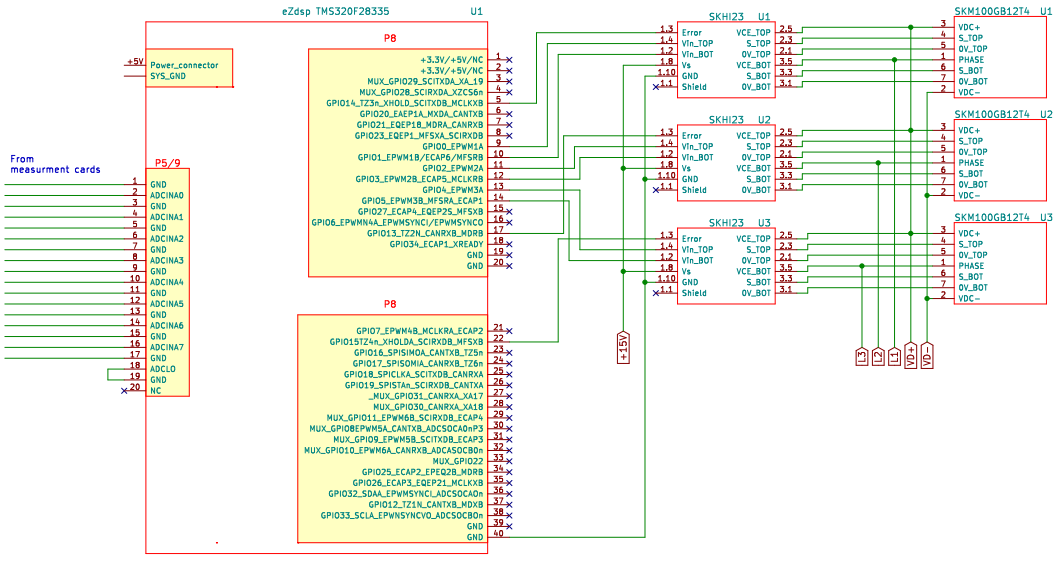


Figure 62: The wiring diagram shows the input connections to the ADC on the eZdsp card. Digital outputs generated by the three ePWM modules are sent to the IGBT driver cards. Note that the error signals from each driver card are sent to a dedicated TZ on the eZdsp card. Each driver card is connected to a IGBT half bridge as shown. Note that the pins have been rearranged for convenience regarding cable crossings.

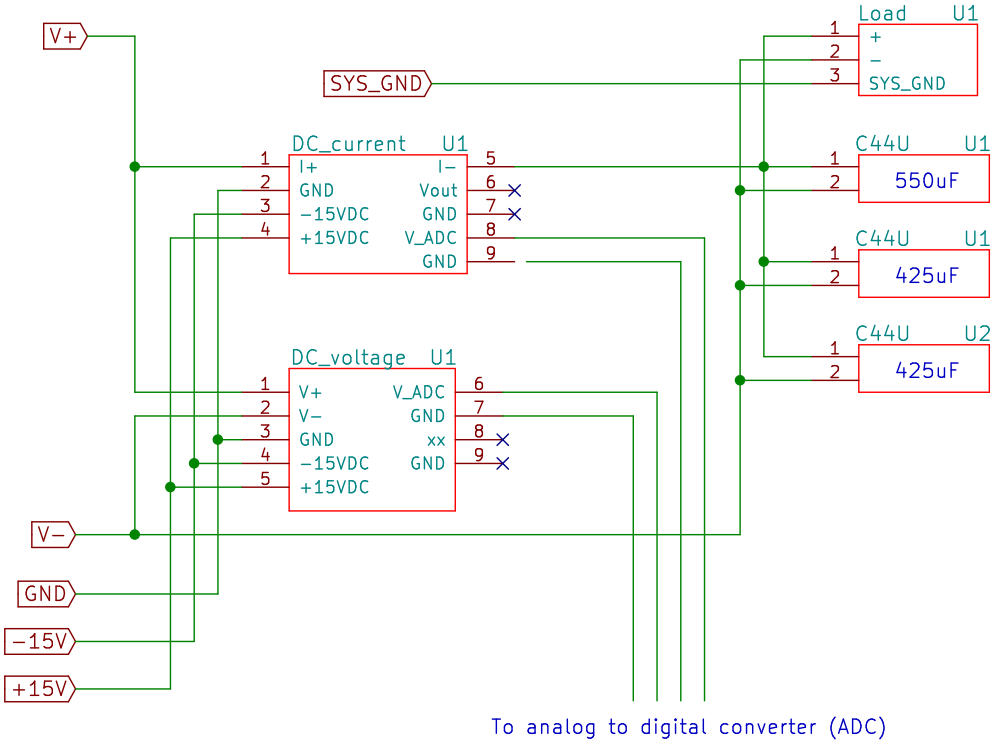


Figure 63: The wiring diagram shows the connection on the dc bus. The dc outputs from the IGBTs are labeled V+ and V- and are sent from figure 62. The supply to the dc measurement cards are sent from figure 61. The outputs from the dc measurement cards are sent to the eZdsp card.

current are sent to the eZdsp card. Note that the capacitors are connected in parallel to achieve an equivalent value of 1525µF. The connected load has several stages to regulate the connected load.

6.6 Programming

To program the eZdsp card there were two options that were considered. The first one was to write the C-code manually in CCS. The advantages of this solution is that the developer has full control over the generated C-code and troubleshooting is manageable. The disadvantages are that the development of C-code is time consuming and the developer must know C-programing. The second option was to use embedded coding in Matlab with support packages for C2000 microcontrollers developed by Mathworks. The advantages of this solution is that the user does not

need to know C-programming. It can also save the developing time of the code generation considerably. The disadvantages are that troubleshooting is difficult since the developer lacks support to control and guide the code translation process.

Due to the lack of time was it decided to try the embedded coding solution in Matlab. The installed software for code generations are

1. Code Composer Studio version 7.4
2. controlSUITE
3. Matlab 2017b
4. TI C2000 Support from Embedded Coder

In order to check if the TI C2000 Support package is installed correctly must the command matlabshared.supportpkg.getInstalled be written in the Matlab command window. The output on the command window should then yield Embedded Coder Support Package for Texas Instruments C2000 Processors 17.2.2 Embedded Coder.

6.7 Results

The laboratory model was not completed in time due to delays regarding completion of the YNd1 transformer and development of C-code to the DSC card. It was therefore not possible to test the VOC AFE rectifier system in the electric power laboratory and to validate simulation results to the physical model. Figure 64 shows the developed laboratory model.

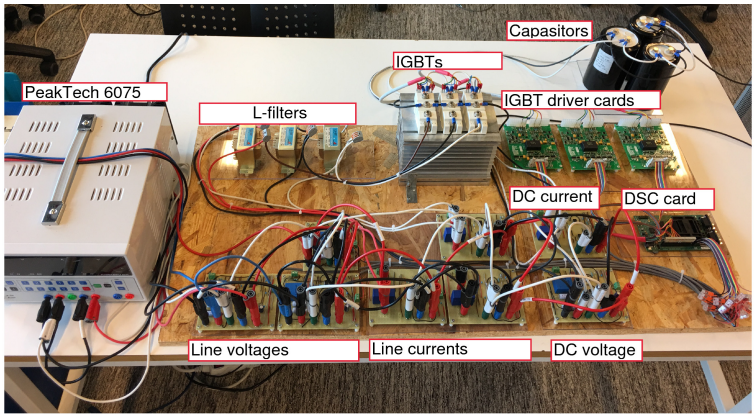


Figure 64: Physical laboratory model including the measurement cards, IGBT driver cards, eZdsp card, inductors, capacitors, power supply and the IGBTs mounted on a heat sink.

The supplementing laboratory equipment is a variable resistive load, the YNd1 transformer and a variable ac/dc source. Only tests for the measurement cards were conducted. Since the YNd1 transformer was not completed in time, were a variable ac/dc voltage source used and connected to a variable resistive load to simulate nominal conditions of the measured voltages and currents. All measurements where conducted by a PicoScope 4824 eight channels oscilloscope. Measurement results for the line voltage are shown in figure 65. Only line a is illustrated but the same results yields for line b and c with its respective phase shift. Note that v_{in} is the measured line voltage and v_{out} is the output voltage from the transducer. v_{ADC} is the outgoing signal to the ADC. The delivered voltage from the SWBD located in the electric power laboratory is highly distorted as seen in figure 65. The measured line current i_{Line} is shown in figure 66. Only ac current up to maximum 8.48A (peak) could be measured due to limitations on the variable voltage source. Similar results yields for the line current measurement card b and c. Figure 67 shows the

measured dc voltage. The input voltage is delivered from a six pulse diode rectifier in the variable ac/dc source and has a high ripple voltage. Figure 68 shows the measured dc current.

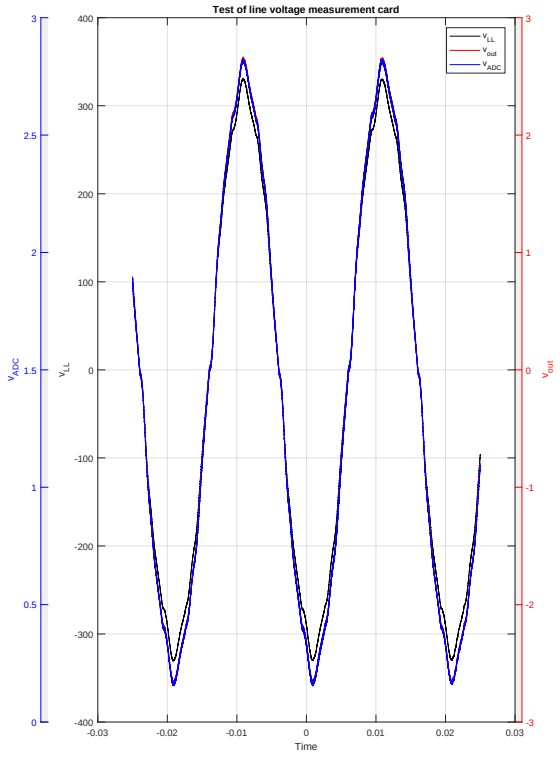


Figure 65: Measured line voltage in the laboratory. The output voltage to the ADC are labeled v_{ADC}. Not the distorted input voltage from the laboratory SWBD.

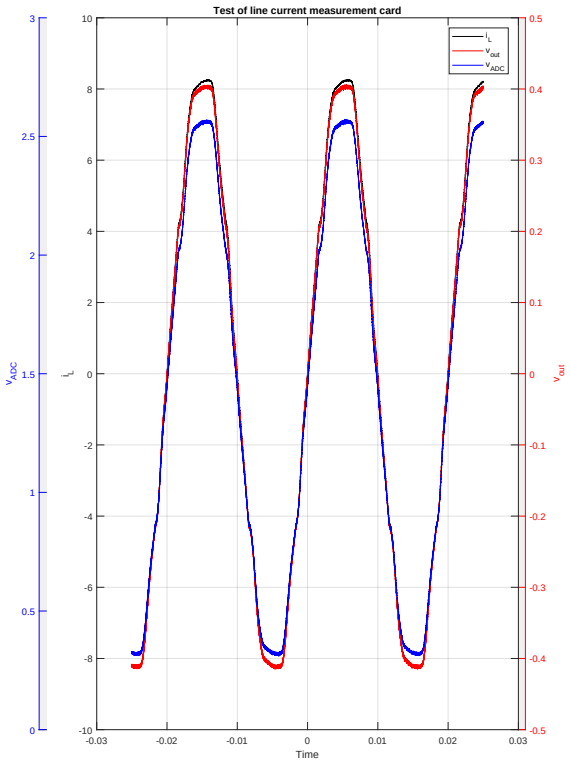


Figure 66: Measured line current from the line current measurement card.

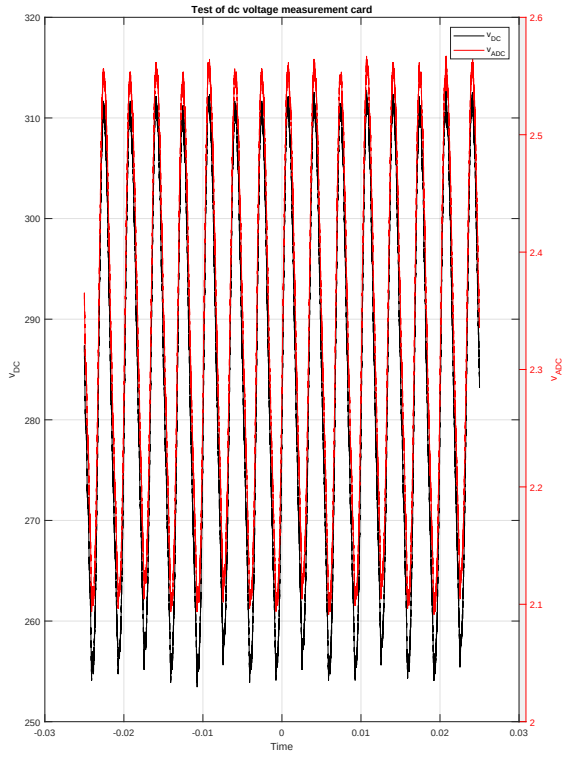


Figure 67: Measured dc voltage in the laboratory.

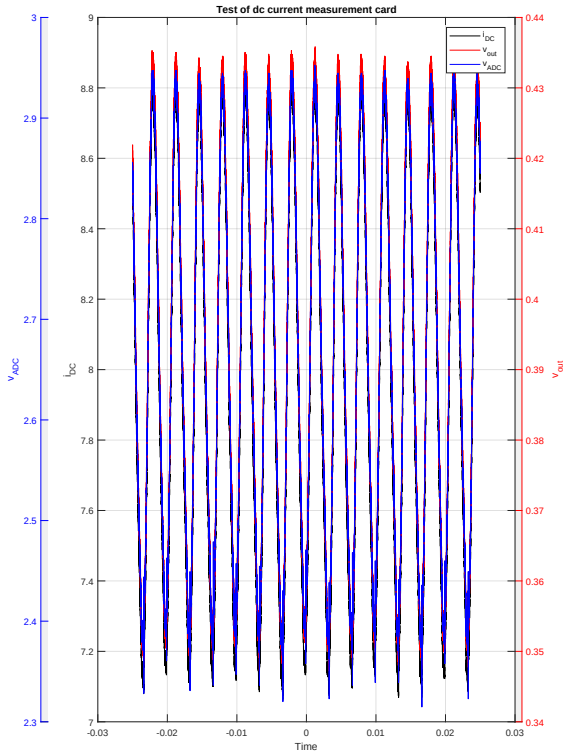


Figure 68: Measured dc current in the laboratory.

7 Discussion

Rectifier systems are one of the main components in a ferry charger system. It is therefore crucial to design a rectifier system which is reliable under different load conditions. The dc bus voltage should adjust quickly to the set value with an as small as possible overshoot and undershoot. Furthermore the steady state error should be as small as possible and thus yielding a stable dc bus voltage. UPF or leading PF are desired depending on the load conditions and it is therefore paramount that the regulators are tuned correctly. Requirements from BKK in regards to THD_v, $\%V_{h_{PCC}}$ and voltage dips must be fulfilled if the ferry charger system are to be connected to the utility grid.

The VOC rectifier with L-filter fulfills the requirement in regards to a stable dc bus voltage. The voltage dips at the dc bus under step changes for the load are approximately 0.9% and the steady state error is 0.05% of nominal dc output voltage. UPF under all load conditions are fulfilled and thus maximizing the power output from the utility grid. Leading PF were not simulated and thus the STATCOM functionality were not developed due to a lack of time. Harmonic current components I_h and THD_i are small under all load conditions and the largest I_h under 50% load is 0.69% and THD_i is 5.24%. Simulation of the VOC AFE rectifier were based on a 3kW load. This was conducted to compare simulation results to the laboratory model. Because of the small load current are the calculated $\%V_{h_{PCC}}$ and THD_v approximately zero at the PCC for all ferry terminals. The short circuit capacity I_{sc} is large compared to the load current and hence the harmonic voltage components yields unrealistic low results. Due to the aforementioned discussion, where the harmonic voltages calculated under a full scale load of 3683kW. The maximum THD_v were calculated to 0.41% and $\%V'_{7_{PCC}}$ to approximately 0.23% at Sævrøy ferry terminal. Each individual harmonic voltage component and the THD_v are in compliance with the maximum values described by BKK. However there are some shortcomings in the full scale calculation. There were assumed linear relationship with I_h and the load current. This is a simplification but gives a good indication for the harmonic voltage components injected to the PCC.

Simulation results for the VOC AFE rectifier with LCL-filter yields stable dc output voltage for all load conditions in the same manner as for the VOC AFE rectifier with L-filter. This is also true for the PF and thus yielding UPF for all load conditions. Improvements are in regards to the attenuation of high order harmonic current components drawn from the utility grid and lower power losses in the filter. Maximum I_h where 3% for I_7 compared to the fundamental component and THD_i at 3.99% under 50% load. Equivalent to the L-filter design are $\%V_{h_{PCC}}$ and THD_v approximately zero at the PCC for all ferry terminals under 3kW load. Comparing the harmonic voltage components results for the 3683kW full scale load with the L-filter design, shows that the THD_v and $\%V'_{h_{PCC}}$ yields higher values but are in compliance with the requirements from BKK. The reason for higher THD_v and $\%V'_{h_{PCC}}$, can be explained in the Bode plot for both the VOC AFE rectifier systems. It shows that the L-filters are more efficient to filter out lower harmonic current components up to approximately 10.7kHz. Higher order harmonics are attenuated more effectively by the LCL-filters in regards to the L-filters. At 2kHz the attenuation factor for the L-filters are -30dB and for the LCL-filters is it -20dB. Therefore the VOC AFE rectifier with L-filters yields better results than the LCL-filter design up to the 40th harmonic. For both the simulated rectifier systems where ideal voltage sources used. It was therefore not possible to simulate voltage dips at the PCC with the used simulation schemes.

The laboratory model were not completed in time and thus the comparison between the simulated model and the measured result from the physical model could not be conducted. There are several reasons why the laboratory model was not completed. The different components were not delivered until March and there were some shortcomings in delivered equipment considering the intended application. For the measurement cards only the transducers were delivered. It was therefore up to the author of the thesis to design and produce the different measurement cards with scaling/offset circuits and noise attenuation circuit. This took a long time, which delayed the development process for the rest of the rectifier system. It was therefore decided that the connection and development of all hardware would be completed and that the code generation of the DSC card would be developed if there was enough time at the end of the semester. All hardware connections were

completed except the YNd1 transformer. Furthermore the development of C-code to the DSC card were not completed in time which gave limited opportunities to test the physical rectifier system.

Only tests of the measurement cards were conducted. The desired output voltage waveforms to the ADC shows that it is in phase with the measured voltage or current within desired range of 0-3V. However the accuracy of the resistor network used are quite low. The 18kΩ resistor on the transducer circuit for line voltages and dc voltage measurement cards have a maximum deviation of ±5%. Also the scaling/offset circuit for all the measurement cards uses resistors with a maximum deviation of ±1%. This leads to lower accuracy of the measurement cards and thus for the VOC rectifier system.

8 Conclusion

The objective in this thesis was to evaluate and design different rectifier systems for ferry charger applications. Demands from the utility grid owner BKK and the ferry company Fjord1 was important in the design process.

The work started by getting an overview of and an examination of international standards in regards to SC systems. Both LVSC and HVSC were presented and if the international standards were to be followed the HV solution must be used in regards to power levels exceeding 1MW. However the standards are not in compliance with practical ferry chargers due to rapid and frequent connections. The international standards should be revised in collaboration with the industry if a common standard is to be used.

AFE rectifier with VOC either by L-filter or LCL-filter were examined in detail with SVPWM. The constriction of UPF consideration with a 3kW resistive connected load yields satisfactory results in regards to stability, UPF, THD_i and harmonic current components under various load conditions. However, the use of ideal voltage sources made it impossible to simulate voltage dips at the PCC. The connected battery pack were simplified with a resistive load and hence it was not possible to simulate charge and discharge of the battery pack.

The grid calculation were conducted with a full scale load of 3683kW which are the estimated charging capacity needed between the ferry crossing Sløvåg and Leirvåg. The simulated current harmonic for the VOC rectifier with L-filter and LCL-filter were scaled up in a linear relation to the load current. This simplification gave a good indication on the injected voltage harmonic at the PCC. Calculating the THD_v and $\%V'_{h_{PCC}}$ with the grid parameters and comparing the results with the demands given by BKK, yields satisfactory results up to the 40th harmonic for both VOC rectifier systems.

Power loss calculation over each filter design were conducted for the full scale load of 3683kW. It shows that the power losses over the L-filter are 53% higher in

regards to the LCL-filter design. Since both VOC AFE rectifier systems satisfies demands regrading stability, UPF and harmonic distortion, the author recommends LCL-filter design due to lower power losses over the filter.

The laboratory model was based on the VOC AFE rectifier with L-filter design. IGBTs and driver cards from Semikron and a DSC card from Spectrum digital were used in the model. Measurement cards where designed by the author and yields satisfactory result, but the use of more accurate resistors should be used. The physical laboratory model was not completed in time and it was therefore not possible to compare simulated results to the laboratory model.

Future work should initially complete the physical laboratory model. Developing the C-code for the DSC card and testing the VOC AFE rectifier system and verifying the measured results to the simulation. Moreover, scaling the VOC AFE rectifier simulations up to 3683kW with grid parameters defined directly in the simulation scheme should also be considered. Incorporating STATCOM capabilities in the simulations for the VOC rectifier systems could also be investigated.

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Appendices

A Clarke and Park transformation

The three-phase voltages and currents are illustrated in figure 69. The transformation between a three-phase system to a two-phase system is called the Clarke transformation and is calculated by the means of the space vector in α and β coordinates.

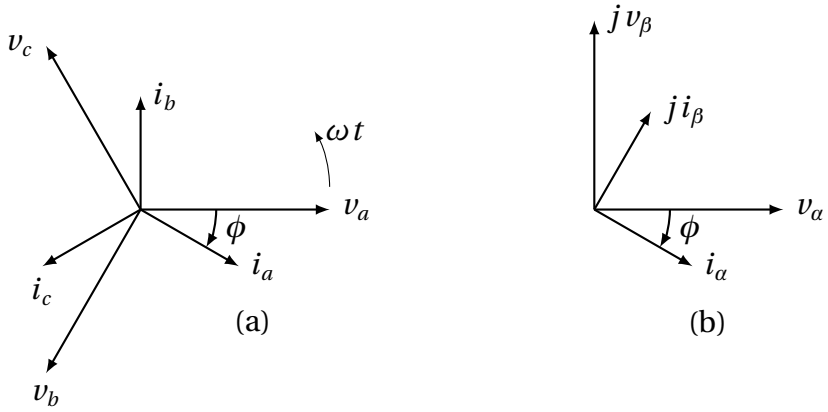

Figure 69: (a) Phase voltages and line currents in a three-phase stationary reference frame; (b) Phase voltages and line currents in a two-phase stationary reference frame.

$$\mathbf{v_s} = \mathbf{v}_{\alpha\beta} = \mathbf{v_a} + \mathbf{v_b} + \mathbf{v_c} = v_a e^{j0} + v_b e^{j\frac{2}{3}\pi} + v_c e^{j\frac{4}{3}\pi} \tag{A.1}$$

By using Euler's formula

$$e^{j\theta} = \cos\theta + j\sin\theta \tag{A.2}$$

the space vector $\mathbf{v}_{\alpha\beta}$ can be rewritten as

$$\mathbf{v}_{\alpha\beta} = v_a - \frac{v_b}{2} - \frac{v_c}{2} + j\left(\frac{\sqrt{3}}{2}v_b - j\frac{\sqrt{3}}{2}v_c\right) \tag{A.3}$$

and in matrix representation

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{A.4}$$

To ensure magnetomotive force (mmf) invariance between the fictitious α and β coils relative to the a, b and c coils, the winding turn ratio must be calculated. Therefore equation A.4 can be written as

$$N_{\alpha\beta} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = N_{abc} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = N_{abc} \cdot \mathbf{A} \cdot \mathbf{v_{abc}} \tag{A.5}$$

where N_{abc} and $N_{\alpha\beta}$ is the winding turn ratio to their respective reference frame. There are several approaches to decide the ratio $\frac{N_{abc}}{N_{\alpha\beta}}$. Two common definitions are frequently used: (1) Power invariancy: Assuming that the net power is unchanged it can be shown that

$$\frac{N_{abc}}{N_{\alpha\beta}} = \sqrt{\frac{2}{3}} \tag{A.6}$$

(2) Power non invariancy: Assumes power pr. phase is unchanged and the winding turn ratio are

$$\frac{N_{abc}}{N_{\alpha\beta}} = \frac{2}{3} \tag{A.7}$$

Power non invariancy will be used in this text, because the peak values of v_α and v_β are equal the peak value of the voltages v_a, v_b and v_c. In order to go from α, β coordinates to a, b, c coordinates must the matrix $\mathbf{A}$ be a square matrix. From symmetrical components transformation [43]

$$v_+, v_- \equiv v_\alpha, v_\beta \tag{A.8}$$

and the zero component

$$v_0 = \frac{1}{3}(v_a + v_b + v_c) \tag{A.9}$$

The factor $\frac{1}{3}$ is the average magnitude but it can generally be represented by a factor K. However in this text $K = \frac{1}{3}$ is used. The Clarke transform including the zero component are expressed as

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{2}{3}\mathbf{B}\cdot\mathbf{v_{abc}} \tag{A.10}$$

From linear algebra and from equation A.10 is

$$\mathbf{v_{abc}} = \frac{3}{2}\mathbf{B^{-1}}\cdot\mathbf{v_{\alpha\beta 0}} \tag{A.11}$$

The inverse matrix $\mathbf{B^{-1}}$ was calculated in MATLAB resulting in

$$\mathbf{B^{-1}} = \frac{2}{3}\begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \tag{A.12}$$

Summarized going from $\mathbf{v_{abc}}$ to $\mathbf{v_{\alpha\beta 0}}$ is expressed by

$$\mathbf{v_{\alpha\beta 0}} = \mathbf{B}\mathbf{v_{abc}} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{A.13}$$

and from $\mathbf{v_{\alpha\beta 0}}$ to $\mathbf{v_{abc}}$ is given by

$$\mathbf{v_{abc}} = \frac{3}{2}\mathbf{B^{-1}}\cdot\mathbf{v_{\alpha\beta 0}} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} \tag{A.14}$$

The foregoing discussion leads to a two-phase ac system. In order to transform the phase voltages to dc values, the stationary α and β reference frame has to be

related to the rotor, called the Park transformation. This relationship is derived from figure 70 and is given by

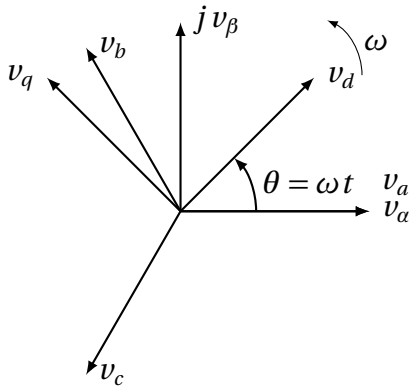

Figure 70: Correlation between phase voltages in a stationary two-phase system compared to synchronously rotating reference frame. Note that v_d and v_q are perpendicular to each other with a rotating speed of ωt.

$$\mathbf{v_{dq0}} = \mathbf{C} \cdot \mathbf{v}_{\alpha\beta\mathbf{0}} = \begin{bmatrix} \sin\theta & \cos\theta & 0 \\ -\cos\theta & \sin\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \tag{A.15}$$

The angle θ between the stationary reference axis relative to the rotor axis is expressed as

$$\theta(t) = \theta(0) + \int_0^t \omega(\tau)\, d\tau = \omega t \tag{A.16}$$

The inverses matrix $\mathbf{C^{-1}}$ ($\mathbf{C^{-1}} = \mathbf{C}^\top$) was calculated in MATLAB in order to get from $dq0$ variables to $\alpha\beta0$

$$\mathbf{v}_{\alpha\beta\mathbf{0}} = \mathbf{C^{-1}} \cdot \mathbf{v_{dq0}} = \begin{bmatrix} \sin\theta & -\cos\theta & 0 \\ \cos\theta & \sin\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \tag{A.17}$$

In most cases the zero component v_0 is neglected because we assume a balanced system ($v_a + v_b + v_c = 0$) and the foregoing equations will be simplified.

B Power calculations

The instantaneous complex power in space vector terms is given by

$$\begin{aligned}\mathbf{S_s} &= \mathbf{V_s}(\mathbf{I_s})^* \\ \mathbf{s_s} &= (v_\alpha + j\,v_\beta)(i_\alpha - j\,i_\beta) \\ \mathbf{s_s} &= v_\alpha i_\alpha - j\,v_\alpha i_\beta + j\,v_\beta i_\alpha + v_\beta i_\beta\end{aligned} \tag{B.1}$$

and the active power p_s and reactive power q_s is given by

$$p_s = \Re(\mathbf{s_s}) = v_\alpha i_\alpha + v_\beta i_\beta \tag{B.2}$$

$$q_s = \Im(\mathbf{s_s}) = v_\beta i_\alpha - v_\alpha i_\beta \tag{B.3}$$

The complex power in synchronous rotating reference frame terms are dc values and are expressed as

$$\mathbf{S_{dq}} = V_d I_d - j\,V_d I_q + j\,V_q I_d + V_q I_q \tag{B.4}$$

and the active power P_{dq} and reactive power Q_{dq} are given by

$$P_{dq} = \Re(\mathbf{S_{dq}}) = V_d I_d + V_q I_q \tag{B.5}$$

$$Q_{dq} = \Im(\mathbf{S_{dq}}) = V_q I_d - V_d I_q \tag{B.6}$$

The relationship between the instantaneous complex power in space vector terms and three-phase systems is derived as follows

$$\mathbf{s_s} = \left(\frac{2}{3}\right)^2 \left(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}\right)\left((i_a + i_b e^{-j\frac{2\pi}{3}} + i_c e^{-j\frac{4\pi}{3}}\right) = \mathbf{s} = p + jq \tag{B.7}$$

$$\begin{aligned}\mathbf{s_s} = \left(\frac{2}{3}\right)^2 \Bigg(& v_a i_a - \frac{1}{2} v_a i_b - j\frac{\sqrt{3}}{2} v_a i_b - \frac{1}{2} v_a i_c + j\frac{\sqrt{3}}{2} v_a i_c - \frac{1}{2} v_b i_a + \frac{1}{4} v_b i_b + j\frac{\sqrt{3}}{4} v_b i_b + \frac{1}{4} v_b i_c \\ & - j\frac{\sqrt{3}}{4} v_b i_c + j\frac{\sqrt{3}}{2} v_b i_a - j\frac{\sqrt{3}}{4} v_b i_b + \frac{3}{4} v_b i_b - j\frac{\sqrt{3}}{4} v_b i_c - \frac{3}{4} v_b i_c - \frac{1}{2} v_c i_a + \frac{1}{4} v_c i_b \\ & + j\frac{\sqrt{3}}{4} v_c i_b + \frac{1}{4} v_c i_c - j\frac{\sqrt{3}}{4} v_c i_c - j\frac{\sqrt{3}}{2} v_c i_a + j\frac{\sqrt{3}}{4} v_c i_b - \frac{3}{4} v_c i_b + j\frac{\sqrt{3}}{4} v_c i_c + \frac{3}{4} v_c i_c \Bigg)\end{aligned}$$

$$p_s = \Re(\mathbf{s_s}) \tag{B.8}$$

$$p_s = \left(\frac{2}{3}\right)^2 \left(v_a i_b + \frac{1}{2} v_a i_b - \frac{1}{2} v_a i_c - \frac{1}{2} v_b i_a + \frac{1}{4} v_b i_b + \frac{1}{4} v_b i_c + \frac{3}{4} v_b i_b - \frac{3}{4} v_b i_c - \frac{1}{2} v_c i_a + \frac{1}{4} v_c i_b + \frac{1}{4} v_c i_c - \frac{3}{4} v_c i_b + \frac{3}{4} v_c i_c \right)$$

$$p_s = \left(\frac{2}{3}\right)^2 \left[v_a \left(i_a - \frac{1}{2} i_b - \frac{1}{2} i_c \right) + v_b \left(-\frac{1}{2} i_a + \frac{1}{4} i_b + \frac{1}{4} i_c + \frac{3}{4} i_b - \frac{3}{4} i_c \right) + v_c \left(-\frac{1}{2} i_a + \frac{1}{4} i_b + \frac{1}{4} i_c - \frac{3}{4} i_b + \frac{3}{4} i_c \right) \right]$$

$$p_s = \left(\frac{2}{3}\right)^2 \left[v_a \left(i_a - \frac{1}{2} i_b - \frac{1}{2} i_c \right) + v_b \left(-\frac{1}{2} i_a + i_b - \frac{1}{2} i_c \right) + v_c \left(-\frac{1}{2} i_a - \frac{1}{2} i_b + i_c \right) \right]$$

$$p_s = \left(\frac{2}{3}\right)^2 \left(\frac{3}{2} v_a i_a + \frac{3}{2} v_b i_b + \frac{3}{2} v_c i_c \right) \qquad \text{see figure 71 for derivation}$$

$$p_s = \left(\frac{2}{3}\right) (v_a i_a + v_b i_b + v_c i_c)$$

$$\frac{3}{2} p_s = v_a i_a + v_b i_b + v_c i_c = p \tag{B.9}$$

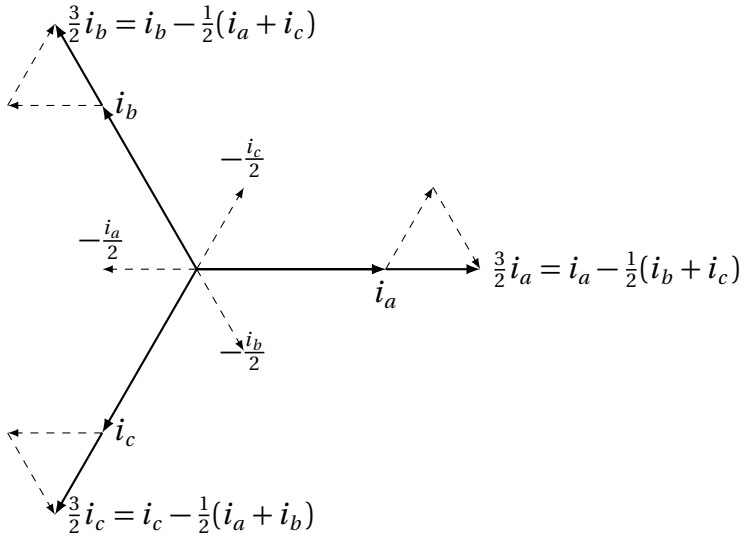

Figure 71: Vector summation of the phase currents in equation B.8.

$$q_s = \Im(\mathbf{s_s}) \tag{B.10}$$

$$\begin{aligned}
q_s =& \left(\frac{2}{3}\right)^2 \left(-\frac{\sqrt{3}}{2} v_a i_b + \frac{\sqrt{3}}{2} v_a i_c + \frac{\sqrt{3}}{4} v_b i_b - \frac{3}{4} v_b i_c + \frac{\sqrt{3}}{2} v_b i_a - \frac{\sqrt{3}}{4} v_b i_b \right. \\
& \left. - \frac{\sqrt{3}}{4} v_b i_c + \frac{\sqrt{3}}{4} v_c i_b - \frac{\sqrt{3}}{4} v_c i_c - \frac{3}{2} v_c i_a + \frac{\sqrt{3}}{4} v_c i_b + \frac{\sqrt{3}}{4} v_c i_c \right) \\
q_s =& \left(\frac{2}{3}\right)^2 \left[v_a \left(-\frac{\sqrt{3}}{2} i_b + \frac{\sqrt{3}}{2} i_c \right) + v_b \left(\frac{\sqrt{3}}{4} i_b - \frac{\sqrt{3}}{4} i_c + \frac{\sqrt{3}}{2} i_a - \frac{\sqrt{3}}{4} i_b - \frac{\sqrt{3}}{4} i_c \right) \right. \\
& \left. v_c \left(\frac{\sqrt{3}}{4} i_b - \frac{\sqrt{3}}{4} i_c - \frac{\sqrt{3}}{2} i_a + \frac{\sqrt{3}}{4} i_b + \frac{\sqrt{3}}{4} i_c \right) \right] \\
q_s =& \left(\frac{2}{3}\right)^2 \left[v_a \left(\frac{-\sqrt{3}}{2} i_b + \frac{\sqrt{3}}{2} i_c \right) + v_b \left(\frac{-\sqrt{3}}{2} i_c + \frac{\sqrt{3}}{2} i_a \right) + v_c \left(\frac{\sqrt{3}}{2} i_b - \frac{\sqrt{3}}{2} i_a \right) \right] \\
q_s =& \frac{2}{3} \frac{1}{\sqrt{3}} \left[v_a (i_c - i_a) + v_b (i_a - i_c) + v_c (i_b - i_a) \right] \\
\frac{3}{2} q_s =& \frac{1}{\sqrt{3}} \left[v_a (i_c - i_a) + v_b (i_a - i_c) + v_c (i_b - i_a) \right] = q
\end{aligned} \tag{B.11}$$

C Filter loss calculation

The power losses over the L-filter and LCL-filter are calculated in this section. Nominal load conditions for the full scale VOC rectifier are assumed with a rated power of 3683kW under UPF and a line voltage of 22kV. The phase diagram for the L-filter is shown in figure 72. The impedance and phase current are expressed as

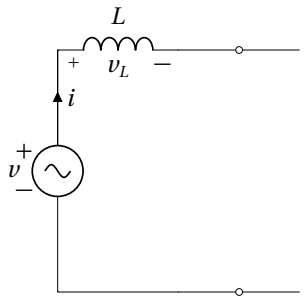

Figure 72: Phase diagram for the L-filter power loss calculation.

$$X_L = \omega L = 2\pi 50 \cdot 8 \cdot 10^{-3} = 2.5133\Omega \tag{C.1}$$

$$|Z_L| = X_L \tag{C.2}$$

$$|\mathbf{I}| = \frac{P_{load}/3}{|\mathbf{V_{LL}}|/\sqrt{3}} = \frac{3683 \cdot 10^3/3}{22 \cdot 10^3/\sqrt{3}} = 96.6537\text{A} \tag{C.3}$$

The three-phase power loss over the L-filter is calculated by

$$P_{loss} = 3 \cdot |\mathbf{V_L}||\mathbf{I}| = 3 \cdot |Z||\mathbf{I}|^2 \tag{C.4}$$

$$P_{loss} = 3 \cdot 2.5133 \cdot (96.6537)^2 = 70.44kW \tag{C.5}$$

The phase diagram for the LCL-filter is shown in figure 73. The equivalent impedance

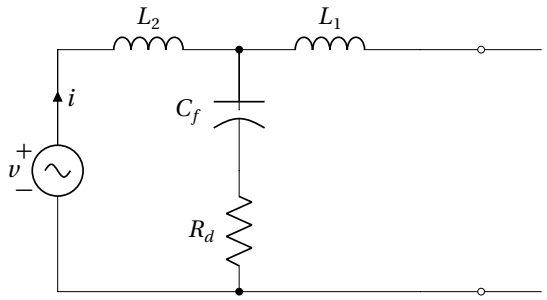

Figure 73: Phase diagram for the LCL-filter power loss calculation.

is calculated by

$$jX_{L_2} = 2\pi 50 \cdot 1.8 \cdot 10^{-3} = 0.5655\Omega \tag{C.6}$$

$$jX_{L_1} = 2\pi 50 \cdot 3.4 \cdot 10^{-3} = 1.0681\Omega \tag{C.7}$$

$$R_d = 6\Omega \tag{C.8}$$

$$jX_{C_f} = -\frac{j}{\omega \cdot C_f} = -\frac{j}{2\pi 50 \cdot 5 \cdot 10^{-6}} = -j636.62\Omega \tag{C.9}$$

$$Z_{eq} = \frac{jX_{L_2}\left(R_d - jX_{cf}\right)}{j\left(X_{L_2} - X_{cf}\right) + R_d} + jX_{L1} \tag{C.10}$$

$$Z_{eq} = 1.6341e^{j89.99^\circ}$$

The three-phase power loss over the LCL-filter is calculated by

$$P_{loss} = 3 \cdot |Z_{eq}||\mathbf{I}|^2 = 3 \cdot 1.6341 \cdot (96.6537)^2 = 45.8kW \tag{C.11}$$

D Operational amplifier derivation

Figure 74 illustrates a scaling circuit used for the voltage and current measurement cards in section 6.4. The derivation uses nodal analysis, voltage division, ideal op

amp theory and thus yields

$$\frac{v_p - v_{in}}{R_3} + \frac{v_p}{R_4} = 0 \tag{D.1}$$

$$v_n = v_{out}\frac{R_1}{R_1 + R_2} \tag{D.2}$$

$$v_n = v_p \tag{D.3}$$

Assuming that $R_1 = R_3$ and $R_2 = R_4$ and combining equation D.1-D.3 yields

$$A = \frac{v_{out}}{v_{in}} = \frac{R_2}{R_1} \tag{D.4}$$

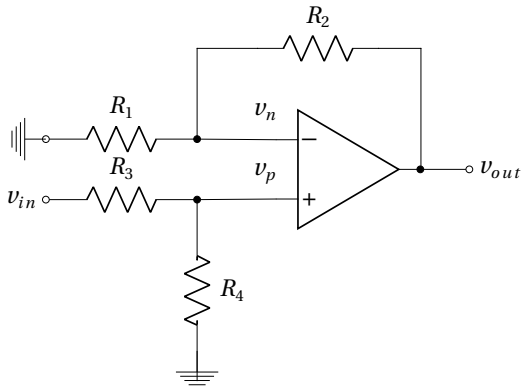

Figure 74: Scaling circuit for voltage and current transducers.