PROCEEDINGS OF SCIENCE

First irradiation test results of the ALICE SAMPA ASIC

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With the continuous scaling of the CMOS technology, the CMOS circuits are considered to be more tolerant to Single event Latchup (SEL) effects due to the reduction in the supply voltages. This paper reports the results from SEL testing performed on the first two prototypes for the new readout ASIC (SAMPA).

During RUN 3/RUN 4 at the Large Hadron Collider (LHC), the SAMPA chip will be used for the upgrade of read-out front end electronics of the ALICE (A Large Ion Collider Experiment) Time Projection Chamber (TPC) and Muon Chambers (MCH). The first prototype MPW1 and the second prototype V2 of the SAMPA chip were delivered in 2015 and 2016, respectively. The results are summarized from two different proton beam irradiation campaigns, conducted for SAMPA MPW1 and V2 prototypes at The Svedberg Laboratory (TSL) in Uppsala, and the Center of Advanced Radiation Technology (KVI) in Groningen, respectively.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

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PoS(TWEPP-17)093

1. Introduction

ALICE is one of the four LHC experiments at CERN. ALICE studies the physics of strongly interacting matter and the properties of the Quark–Gluon Plasma produced in the Pb–Pb collisions at the LHC. During RUN 1, the ALICE experiment successfully collected physics data in Pb–Pb collisions at 2.76 TeV energy per nucleon pair with the delivered luminosity of 0.146 nb^{-1} [1]. For the LHC RUN 3 and onward following the Long Shutdown 2 (LS2) period, it is foressen that the ALICE experiment will collect an integrated luminosity of 10 nb^{-1} for the Pb–Pb collisions at full magnetic field. Additionally, a dataset of 3 nb^{-1} will be recorded at a lower magnetic field [1]. With this considerable increase in the luminosity, the interaction rate will also increase to 50 kHz, which is a factor of about 100 times more than the current data acquisition rate of about 500 Hz [1]. The readout rate of several sub-detectors of the ALICE experiment is the main bottleneck for these higher interaction rates.

The Time Projection Chamber (TPC) and Muon Chambers (MCH) are among the sub-detectors which require upgrades on their Front-End Electronics (FEE) to support these higher readout rates. Thus, a custom made common readout chip, SAMPA is currently in development to adapt to the requirements from both ALICE sub-detectors [2].

2. The SAMPA chip

The SAMPA chip is designed in 130 nm TSMC technology with a nominal supply voltage of 1.2 V. The SAMPA chip is an evolution from the presently used TPC PASA (analog chip) [3] and ALTRO (digital chip) [4] where the total number of channels are doubled from 16 to 32, and both analog and digital electronics are integrated on the same die. As shown in Figure 1, the SAMPA chip includes 32 data processing channels, each containing a charge-sensitive pre-amplifier (CSA), a shaper, a 10-bit 10 MS/s Analog to Digital Converter (ADC) followed by a Digital Signal Processor (DSP). The data readout takes place, either in continuous or triggered mode, by enabling up to eleven 320 Mbps SLVS serial links, allowing a data throughput of up to 3.2 Gbps.

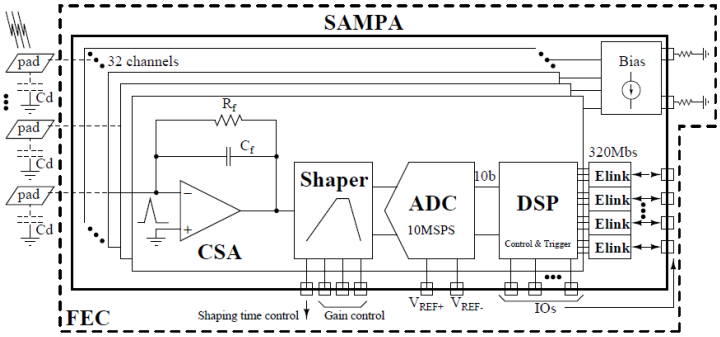


Figure 1: SAMPA block diagram [2].

3. Irradiation Environment for SAMPA chip after LS2

With the increased interaction rate expected after LS2, the radiation load on the FEE will con-

sequently also increase. New calculations from the FLUKA Monte Carlo Code shows that the SAMPA chip should withstand a Total Ionizing Dose (TID) of 2.1 kRad and a flux of 3.4 kHz/cm^2 of High Energy Hadrons (HEH) to operate safely in the worst case locations for both TPC and MCH detectors [2]. For RUN 3, the rate of hadrons with kinetic energy > 20 MeV is upto a factor 4 higher than RUN 1.

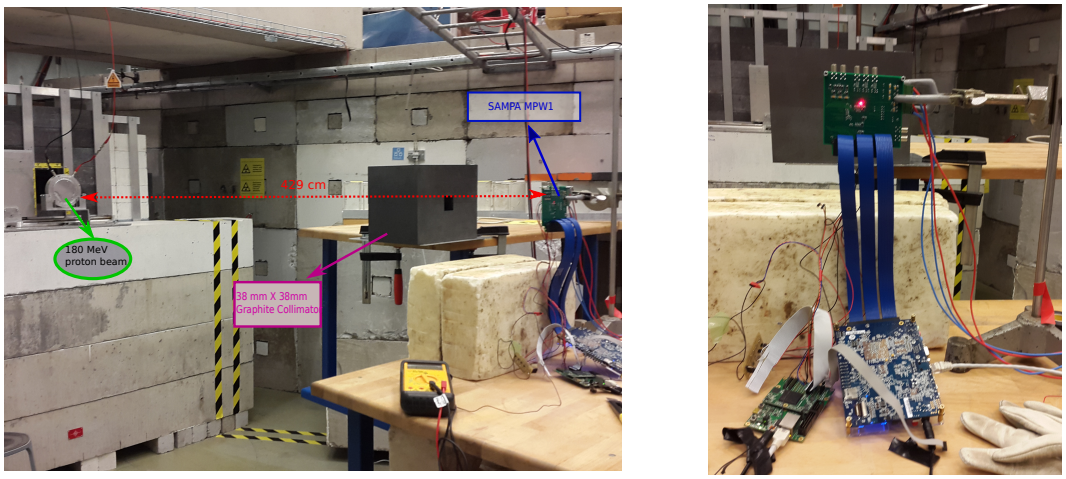
A TID of 2.1 kRad is relatively low to degrade FEE performance [5]. However, the HEH flux is the primary source of radiation induced Single Event Effects (SEE) through indirect ionization in the LHC readout electronics [5]. The SEE mainly occurs in the digital circuitry of the CMOS devices when a highly energetic particle strikes the sensitive regions of the CMOS circuits disrupting their correct operation. The SEE are mainly characterized as soft errors (Single Event Upset, Single Event Transient) and hard errors (Single Event Latchup).

A Single Event Latchup (SEL) is considered as a permanent and potentially destructive effect as it triggers the parasitic thyristor structure in the CMOS device, forming a low impedance path between the supply voltage and the ground. This leads to a high current state in the device and is typically corrected by power cycling the device. If the SEL event is left uncorrected for a longer time period, the high current path can cause melting and permanent damage to the circuit.

4. Irradiation test setup for SAMPA prototypes

The first 2 prototypes (MPW1 and V2) of the SAMPA chip were delivered in 2015 and 2016, respectively, and the results are presented in [6, 7]. SAMPA MPW1 includes 3 complete channels. SAMPA V2 prototype is a complete replica of the final mass-prodouction SAMPA ASIC which includes 32 complete processing channels.

In April 2015, the first irradiation tests were performed on the SAMPA MPW1 prototype with a 180 MeV proton beam at The Svedberg Laboratory (TSL) in Uppsala. A second irradiation campaign was performed on the SAMPA V2 prototype with a 184 MeV proton beam at the Center of Advanced Radiation Technology (KVI) in March 2017.



(a) SAMPA MPW1 in proton beam line.

(b) Configuration setup for SAMPA.

Figure 2: SAMPA MPW1 irradiation test setup at the TSL.

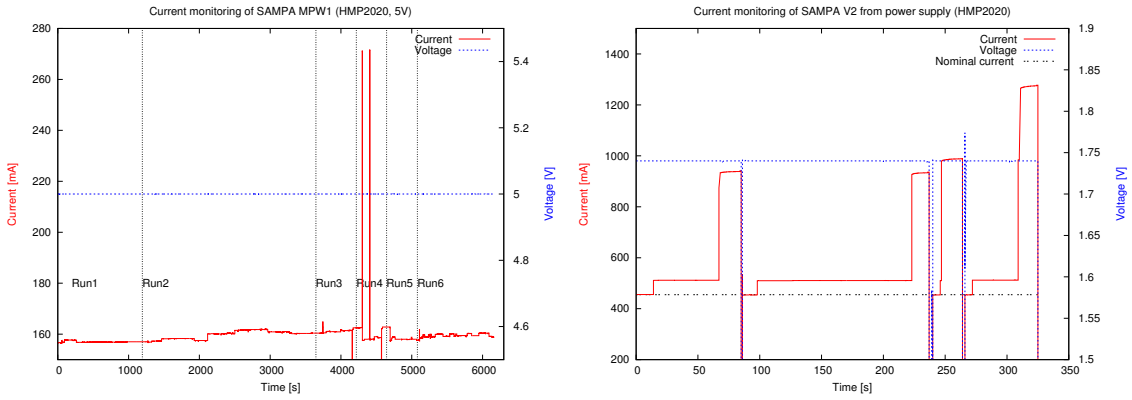
The setup for the SAMPA MPW1 proton beam test is shown in Figure 2. In order to create a broad uniform proton field, the primary proton beam is scattered by a 4 mm thick Ta foil. The MPW1 (DUT) is located at the distance of 429 cm from the foil and the average energy of the proton beam is 159 MeV at the DUT. The setup is shown in Figure 2a. An additional graphite collimator is used between the beam and DUT in order to irradiate only the SAMPA chip and protect all other electronics mounted on the Print Circuit Board (PCB).

During the irradiation tests, the SAMPA prototypes are configured using an Altera System-On-Chip development board with a Cyclone-V FPGA [8]. The FPGA has a built-in dual core microprocessor unit. Several C language scripts are developed on the Linux system of the System-On-Chip to communicate with the SAMPA chip through the Linux system of the FPGA. Figure 2b shows the configuration setup of the SAMPA chip. The data packets from the chip are transferred via a custom made HSMC cable to the FPGA where the data is stored in a memory shared with the microprocessor. A program running on the Linux system compresses and transmits the data over Ethernet to the host computers.

The SAMPA chip is powered by a programmable DC power supply (HMP2020). A set of python scripts are developed to communicate remotely with the power supply over the USB interface. The supplied voltage and the current consumption are monitored and saved during the tests. A significant and rapid increase in the current consumption during irradiation is considered to be a SEL event.

5. Irradiation test results

The results from both irradiation campaigns are summarized in Figure 3. The MPW1 was irradiated for $\approx$ 1.3 hr with a proton flux ranging from $6.5{\cdot}10^6$ to $6.4{\cdot}10^7$ p/cm^2/s, reaching a total fluence of $\approx 1.7{\cdot}10^{11}$ p/cm^2. Figure 3a shows the overall current consumption of the MPW1 prototype as a function of the irradiated time. The plot indicates no signs of high current events in 5 of the 6 runs. The two current jumps in run 4 are due to an initial non-nominal operation setting. In addition, a stable DC supply voltage is seen during the tests.



(a) Current log of the MPW1 prototype.

(b) Current log of the V2 prototype.

Figure 3: Current monitoring from the power supply during the SAMPA irradiation tests.

The V2 prototypes were irradiated with a proton flux ranging from $7.4{\cdot}10^6$ to $3.8{\cdot}10^8$ p/cm^2/s, reaching a total fluence of $\approx 1.2{\cdot}10^{12}$ p/cm^2. The current/voltage from the power supply is plotted as a function of irradiated time in Figure 3b. Several current jumps were detected during the V2 irradiation tests. The DUT needed power cycle to return back to its nominal current (450 mA). These current jumps are considered to be SEL events in the V2 prototypes.

6. Summary and Future work

No SEL was observed during the SAMPA MPW1 proton tests. However, the SAMPA V2 prototypes were susceptible to the proton induced SEL events. Consequently, design improvements are implemented in the SAMPA V3/V4 prototypes and the chips are submitted for the production. More irradiation campaigns are planned to verify that the SEL sensitivity of the future SAMPA prototypes has been reduced or even completely removed.

In both proton beam campaigns, the SAMPA prototypes accumulated a dose of ≈ 12 kRad(Si). No significant changes were observed in pre-irradiation and post-irradiation performance with respect to the TID effect. This makes the SAMPA chip qualified for the expected TID of 2.1 kRad in the ALICE detectors after LS2.

Acknowledgement

The authors wish to acknowledge all the people that have been actively participating in the SAMPA project. In partcular, the SAMPA design team from Sao Paulo for providing the SAMPA prototypes and the IPN Orsay team from Paris for preparing the carrier boards of these prototypes.

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