Western Norway University of Applied Sciences

University in Bergen

MASTER THESIS

HIGH VOLTAGE DIRECT CURRENT TRANSMISSION

Martin Solberg

ENERGI 399

Department of Electrical Engineering

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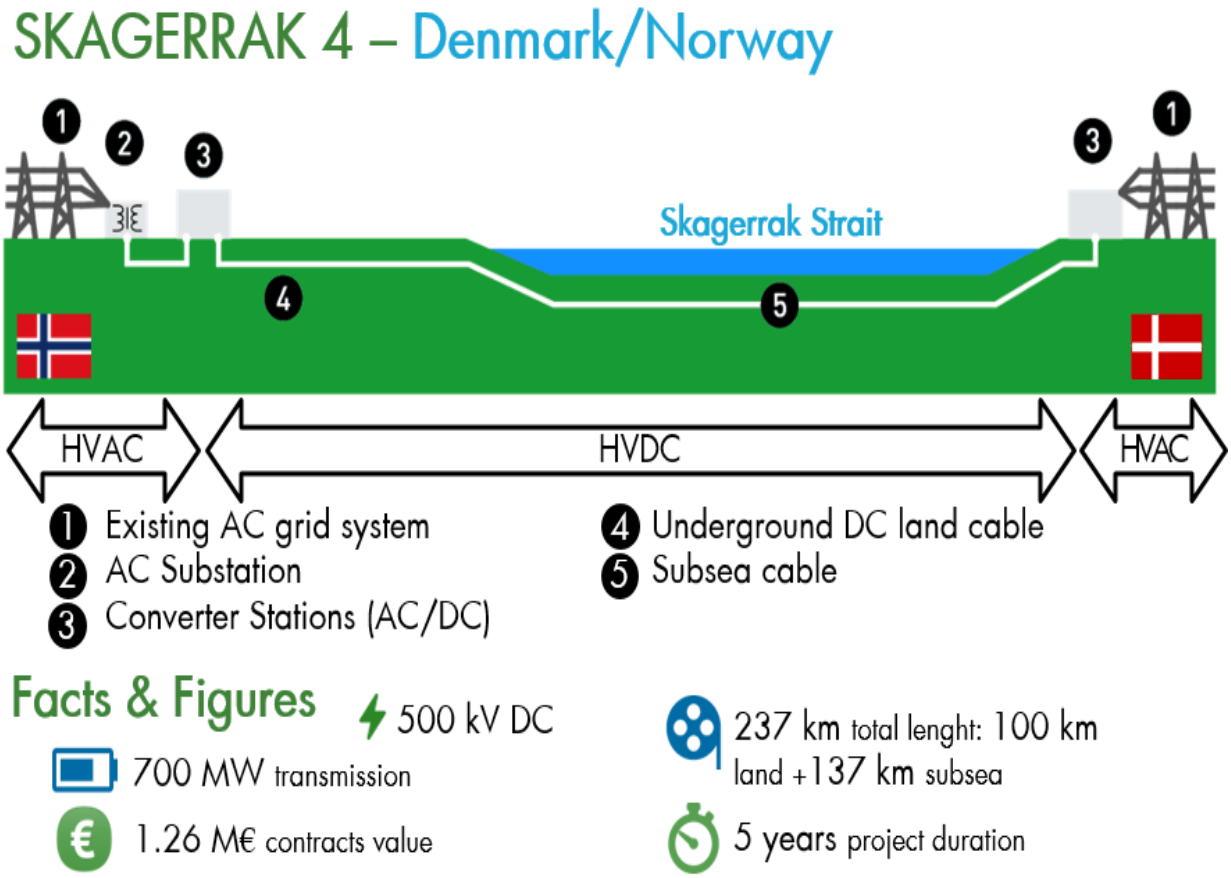

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SUMMARY

HVDC Transmission Solution

High-voltage direct current (HVDC) transmission systems are becoming more and more important in an energy landscape that is characterized by increasing digitalization, decarbonization, and distributed generation. They offer the most efficient means of transmitting large amount of power over long distances, help connect green power to the grid, and stabilize three-phase-grids.

A **high-voltage, direct current** (**HVDC**) electric power transmission system (also called a **power superhighway** or an **electrical superhighway**) uses direct current for the bulk transmission of electrical power, in contrast with the more common alternating current (AC) systems.

The high voltage direct current (HVDC) technology has been increasingly developed and applied in the recent years. Mainly within the voltage source converters, the technology has come a long way since the first two-level converters. **Modular multi-level converters (MMC)** operates with IGBTs connected in submodules. This way the converter-generated AC voltage can be collected in smaller steps, and further on significantly reducing losses which has been a main concern with the VSC solution. The **Insulated gate bipolar transistors (IGBTs)** is frequently being evolved as well, primarily in concern to voltage levels and current ratings. Line commuted converters (LCC) still offer a reliably choice, since they represent a reliable and proven technology. This converter technology is mainly used in the operational cables in the Northern sea. However, the new subsea cables under development studied in this paper plan to use the more technically advanced VSC technology. The development of this technology as well as the developing of HVDC subsea transmission cables in the Northern sea is the subject of this paper. A proposed simulation of the planned North Connect interconnection between the Norwegian and British (Scottish) power grid is illustrated in the paper. Here proposed with a half bridge MMC symmetric monopolar system, using data from the public concession application.

Why high-voltage direct current?

HVDC systems are ideally suited to support and improve the sustainability, efficiency, and reliability of power supply systems. They supplement the existing AC infrastructure through highly efficient long-distance power transmission grid access for onshore and offshore renewables transnational grid connections provision of fully controlled power supply in either direction the connection of asynchronous grids and grids with different frequencies performance improvements and firewalling of AC grids against cascading blackouts A pioneer in HVDC technology, Siemens provides a comprehensive portfolio of efficient and sustainable solutions for all HVDC applications.

Contents

Preface

At the time of writing, there are over 170 high-voltage direct -current (HVDC) links installed worldwide. The larges installations operate at ±800 kV DC voltage and the highest DC current rating are over 4500 A. Although alternating current was the predominant method for transmitting electrical energy in the twentieth century, HVDC

Was demonstrated to be the best solution for many specific application areas and the number of installations per year has been constantly increasing at the beginning of twenty-first century. *Despite significant converter-station costs, HVDC is techno-economically preferred in general applications for*:

- ✓ Long -distance, large-scale power transfer;
- ✓ Subsea and long-distance cable-power transmission;
- ✓ Interconnecting asynchronous AC system or system with different frequencies;
- ✓ Controllable power transfer between different nodes in an electricity marked or markets;
- ✓ AC grid-stability support, ancillary service provision and resilience to blackouts;
- ✓ Connecting isolated system like offshore wind farms oil platforms.

DC transmission technology was used in many instances in very early power system but modern HVDC transmission begins with the 1954 Sweden-Gotland installation.

This system and all the other HVDCs commissioned until the mid-1970s were based on mercury arc valves. A significant technical advance came with the introduction of solid-state valves (thyristors), although they only support the line-commutated converter (LCC) concept. In the first decade of the twenty-first century there has been very rapid development of fundamentally new technologies and an increasing demand for HVDC technology. The introduction of voltage-source converters (VSCs) requires new valves, which use insulated-gate bipolar transistors (IGBTs) and also new protection and control approaches. The modular multilevel converters have eventually emerged as the most cost effective VSC converter concept, which practically eliminates filtering needs with HVDC and removes voltage limits with VSC valves.

In the second decade of the twenty-first century it has become apparent the DC transmission grids are a technically feasible and variable solution to large-scale energy challenges. The primary application drivers come from initiatives like the North Sea DC grid, MedTech, Deserted, the European overlay super grid and Atlantic Wind. It is accepted that the DC transmission grids must have levels of reliability and technical performance that are similar to or better than an AC transmission system. This level of performance, security and reliability is technically feasible, although, in many aspects, DC grids will be substantially different from traditional AC systems. The development of DC grids brings significant technical advances in HVDC technologies, in particular related to DC circuit breaker (CBs), DC/DC converters and DC protection system, and substantial further research and development are anticipated.

Nowadays, HVDC and DC grids are associated with green energy, as facilitators of large-scale renewable energy plants. This helps with public acceptance and image and facilitates further investments in large public projects. HVDC is perceived as the technology that avoids pylons by using long underground cables, further strengthening arguments for further funding decisions.

The project is organized in three parts in order on order to study all three major HVDC concepts **– line commutated HVDC**, **VSC HVDC** and **DC grids** current research developments. Each part will review theoretical concept and analyse aspects of technology, interaction with AC grids, modelling, control, faults and protection, with practical implementation aspects and on reported operational issues. The technical field of HVDC transmission and DC grids straddles three major traditional electrical engineering disciplines:

- ✓ ***Power transmission engineering.*** The impact of HVDC systems on the connecting AC transmission system and the national grid is of primary importance. The influence of AC system on HVDC is also of significance in terms of technical performance, stability, protection and power transfer security in general. Harmonic interaction will be studied in some depth.
- ✓ ***Power electronics***. Each HVDC link involves at least two AC/DC converters whereas DC grids will have many more, including semiconductor DC CBs and DC/DC converters. These converters have features that are similar to those of traditional low-power converters, but many other unique requirements exit to develop valves and converters is very important and is a defining power electronics feature in HVDC.
- ✓ ***Control engineering***. Modelling and simulation og HVDC is essential for design and operation and several different modelling approaches exit, depending on the model application.IN particular, because of the high costs 0f HVDC testing and the and the consequences of any design issues, model accuracy and simulation speed play crucial role in the system design. The control system for HVDC have evolved into very complex technologies, which are always multivariable, nonlinear and with multiple control layers.

The above three technical disciplines will be employed in this project in order to analyse all essential technical aspects of HVDC and DC grids which aimed to facilitate learning by researchers and engineers who are interested in this field.

The material in this project includes contributions from many HVDC researches and engineers and it is developed from research projects funded by several research councils and private firms. More importantly, the studies are inspired by and build on previous work by numerous great HVDC engineers.

Martin Solberg

Part A: HVDC with Current Source Converters

1 Introduction to Line-Commutated HVDC

1.1 HVDC Application

Thyristor-based high-voltage direct-current (HVDC) transmission has been used in over 150 point-to-point installations worldwide. In each case it has proven to be technologically and/or economically superior to AC transmission.

Typical HVDC applications can be grouped as follows:

- ✓ ***Submarine power transmission***. The AC cables have large capacitance and for cables over40–70km there active power circulation is unacceptable. This distance can be extended somewhat with reactive power compensation. For larger distances, HVDC is more economical. A good example is the 580km, 700MW, ±450kV Nor Ned HVDC between Norway and the Netherlands.

- ✓ ***Long-distance overhead lines***. Long AC lines require variable reactive power compensation. Typically600–800 km is the breakeven distance and, for larger distances, HVDC is more economical. A good example is the1360km, 3.1GW, ±500kV Pacific DC intertie along the west coast of the United States.

- ✓ ***Interconnecting two AC networks of different frequencies***. A good example is the 500MW, ±79kV back-to-back Melo HVDC between Uruguay and Brazil. The Uruguay system operates at 50Hz whereas Brazil's national grid runs at 60Hz.

- ✓ ***Interconnecting two unsynchronized AC grids***. If phase difference between two AC systems is large, they cannot be directly connected. A typical example is the 150MW, ±42kV McNeill back-

to-back HVDC link between Alberta and Saskatchewan interconnecting asynchronous eastern and western American system.

- ✓ ***Controllable power exchange between two AC networks (for trading)***. The AC power flow is determined by the line impedances and it cannot therefore be controlled directly in each line. In complex AC networks it is common to observe loop power flow or even overloading or underutilization of some AC lines. Many HVDC systems participate directly in trading power and one typical example is the 200MW, ±57kV Highgate HVDC between Quebec and Vermont.

There are other less common applications of **LCC** (line-commutated converter) HVDC technology, including the 300MW Levi's De-Icer HVDC project. Here, one standard HVDC converter station – a converter from a Static Var Compensator (**SVC**) – is used to provide a very high DC current of up to 7920A (feeding essentially a DC short circuit) to enable heating of remote Canadian overhead lines in order to prevent ice build-up.
An important argument for selecting HVDC instead of an AC for a new transmission line is the contribution to the short-circuit level. High-voltage direct current is able to limit the fault current and therefore, it will not require the upgrading of substation equipment.

Figure 1.1 shows a comparison of costs for DC and AC transmission lines. In the case of HVDC the initial capital investment is much higher because of the converter costs. As the transmission distance increases, the benefits of DC offset the capital investment and at certain distance the total cost of an HVDC system is same as an AC line. The breakeven distance is in the range of 40–70 km for submarine cables and in the range of 600–800km for overhead lines.

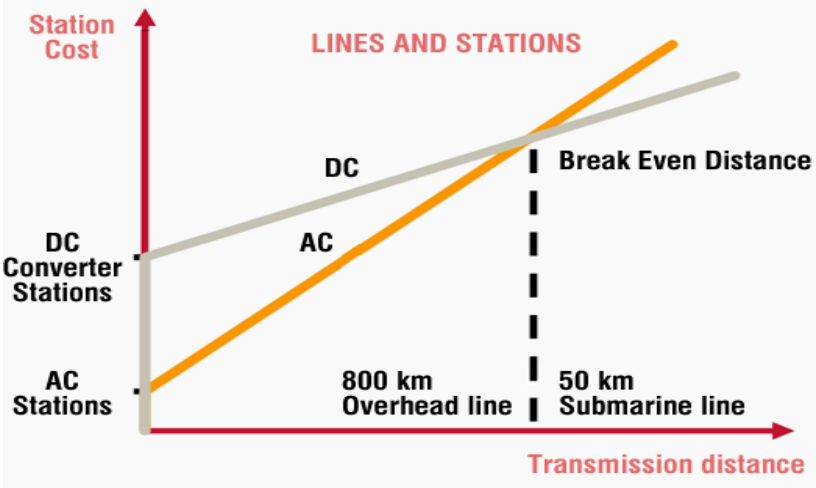

Figure 1.1 *HVDC and HVAC transmission cost comparison.*

Figure 1.2 shows an aerial view of the terminal station of the 500 MW Moyle HVDC link. This HVDC enables a controllable bidirectional power exchange between Scotland and Northern Ireland.

Figure 1.2 *Terminal station of Moyle HVDC interconnector (Bipole 2×250MW, ±250kV, with light triggered thyristors, commissioned in 2001). Reproduced with permission of Siemens.*

1.2 Line-Commutated HVDC Components

Figure 1.3 shows a typical ***LCC HVDC*** schematic interconnecting AC systems 1 and 2. It consists of two terminals and a DC line between them. Each terminal (converter station) includes converters, transformers, filters, reactive power equipment, control station and a range of other components. There are two DC lines in this figure while one line is at ground potential.

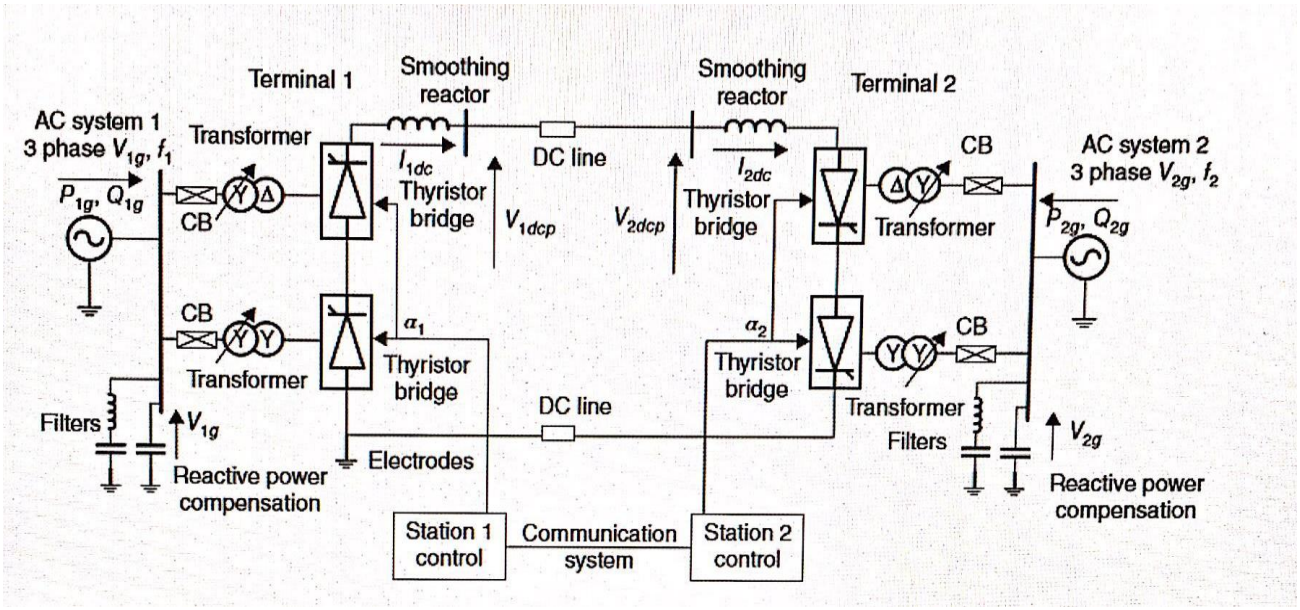

Figure 1.3 Typical HVDC schematic (12-pulse monopole with metallic return).

As shown in Figure 1.3, the major components of an HVDC system include:

- ✓ ***Converters***. They typically include one or more six-pulse thyristor (Graetz) bridges. Each bridge consists of six thyristor valves, which in turn contain hundreds of individual thyristors. With large systems, bridges are connected in series in12-pulse or 24-pulse configuration. The12-pulse converters can be connected into poles or bipoles.
- ✓ ***Converter transformers*.** These are a special converter transformer type, which is somewhat more expensive than typical AC transformers of the same rating. The converter transformers are designed to operate with high harmonic currents and they are designed to withstand AC and DC voltage stress. In most cases converter transformers will have tap changers, which enable

optimization of HVDC operation.

- ✓ ***Smoothing reactors on DC side***. Typical inductance for large HVDC systems is 0.1–0.5H, which is determined considering DC fault responses, commutation failure and dynamic stability. The reactors are of air-core, natural air-cooling type and costs are modest.
- ✓ ***Reactive power compensation***. The converters typically require reactive power of around 60% of the converter power rating. A large portion of this reactive power is supplied with filter banks and the remaining part with capacitor banks. Reactive power demand varies with DC power level, so the capacitors are arranged in switchable banks.
- ✓ ***Filters.*** A typical 12-pulse thyristor terminal will require 11th, 13th, 23rd and 25th filters on the AC side. A high-pass filter is frequently included. In some cases, third harmonic filters are required. Some HVDC systems with overhead lines also employ DC-side filters.
- ✓ ***Electrodes.*** Some old HVDC systems normally operate with sea/ground return but most grid operators no longer allow permanent ground currents for environmental reasons. Electrodes demand ongoing maintenance costs. Many new bipolar systems are allowed to operate with ground return at half power for a short time (10–20minutes) in case of loss of an HVDC pole. This implies that electrodes are designed for full current but carry no current in normal operation.
- ✓ ***Control and communication system***. Each terminal will have a control system consisting of several hierarchical layers. A dedicated communication link between terminals is needed but speed is not critical. An HVDC link can operate in the event of a loss of a communication link.

1.3 DC Cables and Overhead Lines

1.3.1 Introduction

Line-commutated converter HVDC has been implemented using overhead lines and underground/ subsea DC cables. Overhead lines are vulnerable to lightning strikes, which are essentially DC faults. Never the less DC faults only cause transient disturbances and they are readily managed by LCC HVDC. On the other hand, with voltage source converter (VSC) HVDC, as will be discussed later, DC faults cause much more serious disturbances.

***The most common cable technologies that have been developed so far include*:**

- ✓ mass-impregnated **(*MI*)** cables;
- ✓ low-pressure oil-filled ***(LPOF)*** cables;
- ✓ extruded cross-linked polyethylene ***(XLPE)*** cables.

The above cable types have same conductors and their construction is similar but the insulation material is substantially different. The cable voltage rating depends on the capability of the insulation (dielectric) material, and there are two main types of dielectrics, namely lapped and extruded.

1.3.2 Mass-impregnated (MI) Cables

Since 1895, MI cables have been used in power transmission. In MI cables, the dielectric is lapped paper insulation, which is impregnated with high-viscosity fluid. For bulk power transmission, mass impregnated cables still prove to be the most suitable solution because of their capacity to work up to 500kV DC. These cables also tolerate fast DC voltage polarity reversal, making them suitable for LCC HVDC. The MI cables have a long record of field operation at voltages of 500 kV and transmission capacity of over 800 MW (1.6 kA) for monopole HVDC but 600 kV and 1000 MW ratings have been announced.. An HVDC with a bipolar connection is therefore able to transmit up to2000MW with MI cables. These cables can be installed at depths to 1000m under the sea level and with nearly unlimited transmission length. The capacity of this system is limited by the conductor temperature, which can reduce overload capabilities.The580km-long700MW,450kVcablelinkbetweenNorway and the Netherlands represents the greatest power and length for this cable type. At present over 90%of submarine cables are of the MI type.

1.3.3 Low-pressure Oil-filled Cables

Low-pressure oil-filled cables are similar in construction to MI cables, but the cables are insulated with paper impregnated with low viscosity oil under an overpressure of a few bars. The technology available today ensures voltages up to 500kV and powers up to 2800MW for underground installation. It can be used for both AC and DC transmission applications*. As oil flow is required along the cable, cable length*

is limited to around 80km. ***The risk of oil leakage must be taken into account for environmental reasons****.*

1.3.4 Extruded Cross-Linked Polyethylene (XLPE) Cables

Extruded cross-Linked polyethylene cables cannot withstand fast polarity reversal and they are not normally used with LCC HVDC (unless it is unidirectional). They will be discussed further with VSC HVDC. The above three types of cables are used for both underground and submarine cables and their basic properties are shown in Table 1.1. The difference between the underground and submarine cables is in the conductor material and the armour layer. Armour strengthening is used in submarine cables to withstand the axial mechanical tension during laying and operation.

Table 1.1 DC cable types for underground and submarine application.

Type	**Mass impregnated**	**Oil Filled**	**XLPE**
Conductor	Cu/AL	Cu/AL	Cu/AL
Insulation	Paper and mass	Paper and fluid	Cross-Linked PE
Voltage (kV)	600	500	320 (525 kV is available)
Capacity per cable (MW)	1000	2800	1000
Converter type	LCC or VSC	LCC or VSC	VSC or unidirectional LCC
Distance	Unlimited	Limited because of oil	Unlimited

conductors are generally preferred for underground. Copper has high electrical conductivity and mechanical properties. It is also simpler to implement strong joints using copper. However, it is heavy and more expensive and for these reasons it is used when the mechanical properties are mandatory, as in submarine cables. Aluminium has low conductivity and low mechanical properties. Splicing is more difficult. It is lighter and less expensive than copper.

1.4 LCC HVDC Topologies

High-voltage direct-current systems are divided into ***transmission systems*** and ***back-to-back HVDC***.

High-voltage direct-current transmission can be (*Bipolar)* or (*Monopolar).*

Monopolar **HVDC** is typically used for smaller systems and the topology is shown in **Figure 1.4**. Typically, positive DC voltage is adopted because of less corona issues. The return current can run through ground or a dedicated cable can be employed. If a return cable is used (metallic return) it will be at ground potential with low insulation level (typically around 10kV) and costs are therefore lower than positive-pole DC cable. A 12-pulse topology is shown with two six-pulse converters in series.

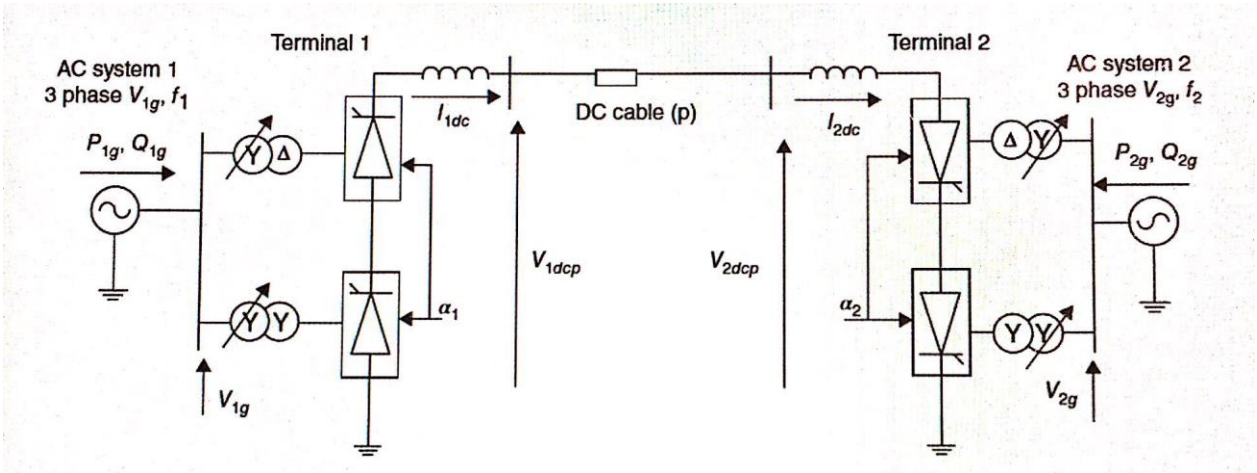

Figure 1.4 *Twelve-pulse monopolar HVDC with ground return.*

Figure 1.5 *shows a bipolar HVDC. Bipolar HVDC has two independent poles and it can operate at half* power if one DC cable or pole is out of service. Normally the poles are balanced and there is no ground current but ground return would be used if one pole is out of service. In modern grid codes, ground current would not be allowed because of environmental concerns. In some national standards ground currents are allowed only for short periods of time in emergency situations (e.g. secondary reserve start up for 10–20minutes). Instead of ground return a third cable or DC cable from the faulted pole can sometimes be used.

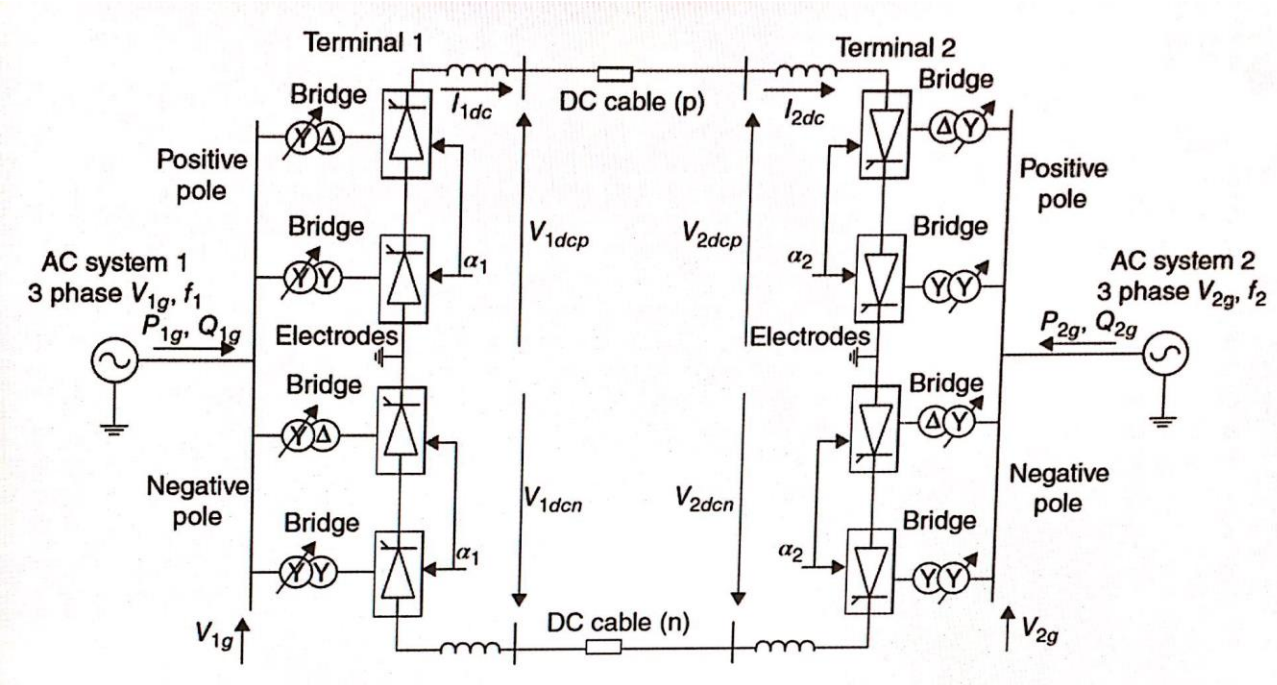

Figure 1.5 *Bipolar HVDC (12-pulse) with ground return.*

Figure 1.6 *shows a* **back-to-back HVDC**, *which is frequently monopolar*. In this topology both converter terminals are located in a single station and DC cables are very short. The main purpose of back-to-back HVDC is to provide controllable power transfer between two asynchronous AC systems or AC systems with different frequency. As DC cables are very short and therefore transmission losses are low, back-to-back HVDC are designed at low voltage (as high current as possible) in order to reduce costs (costs are proportional to insulation level). The smoothing reactors are very small or not required because there is a low probability of DC line faults. Back-to-back HVDC allows for operation with variable DC voltage and this facilitates some limited reactive power control capability.

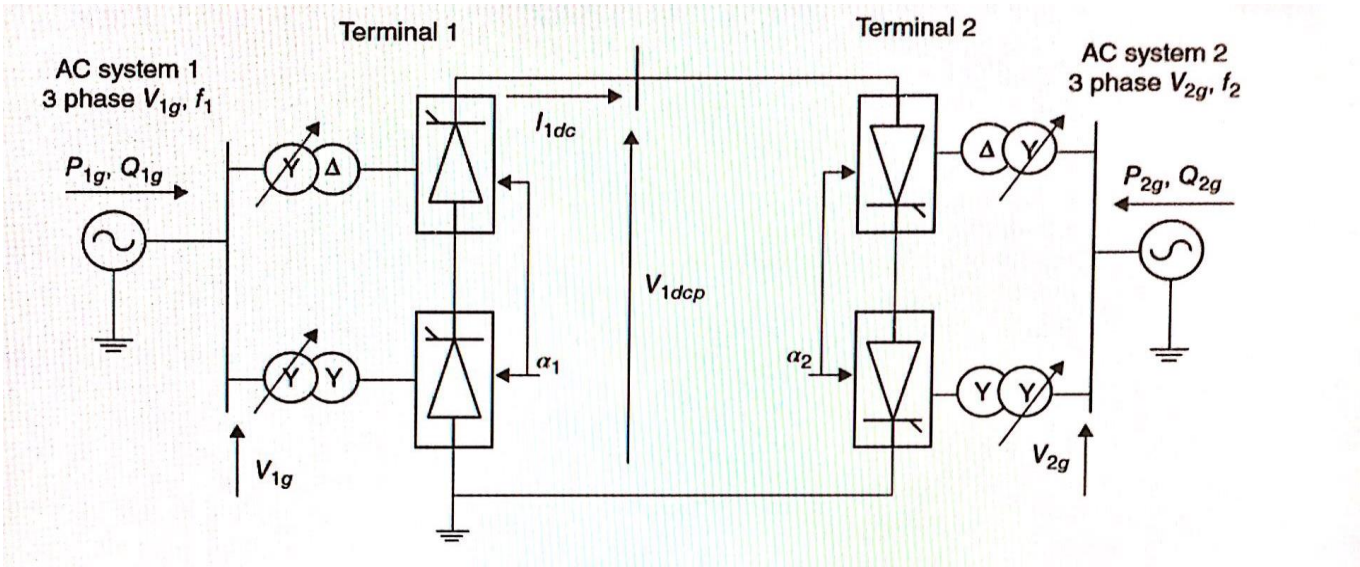

Figure 1.6 *Back-to-back HVDC topology.*

1.5 Losses in LCC HVDC Systems

The losses in HVDC systems will include converter station losses and DC cable losses. Figure 1.7 shows the main components of typical HVDC station losses. The total LCC HVDC station losses will depend on the size of HVDC station, the voltage level, configuration and typically may amount to 0.5–1% of the power transfer.

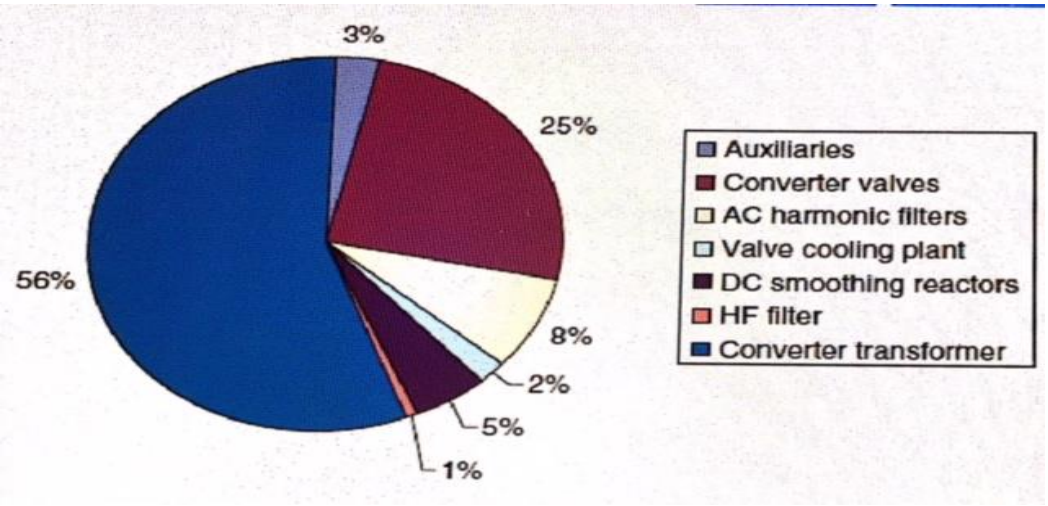

Figure 1.7 Breakdown of typical LCC HVDC station losses at 1pu power

At partial loading the percentage losses will generally increase. Figure 1.8 shows the load dependence of major loss components. As an example, magnetizing current in converter transformers will be constant irrespective of loading and at 10% loading the transformer losses are 20%.

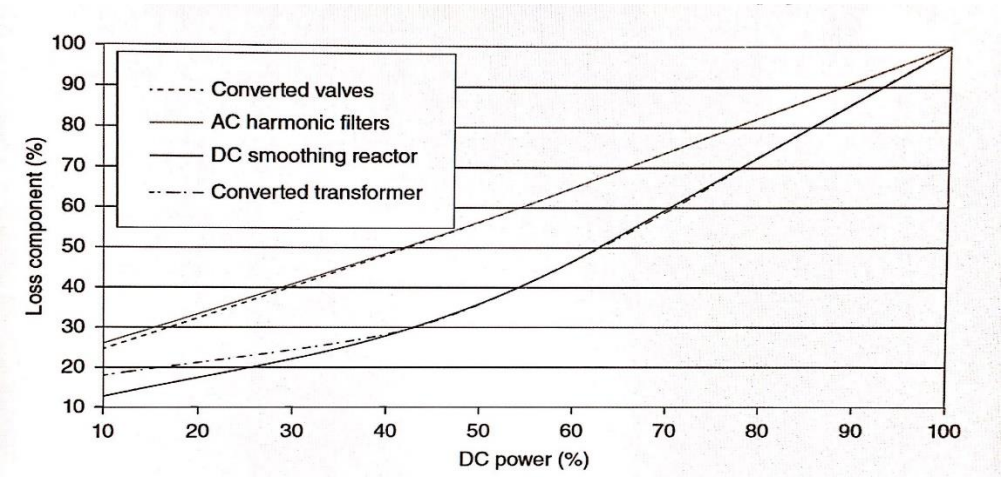

Figure 1.8 Variation of HVDC station losses with the DC power, shown relative to 1pu losses.

1.6 Conversion of AC Lines to DC

There have been many studies worldwide on converting existing AC lines into DC. This mainly results from the desire to increase AC line capacity or to remove stability constraints. These issues usually require costly line upgrades/reconductoring, series compensation or installing a device from the flexible AC transmission systems (FACTS) family. In such cases, conversion to HVDC can usually offer the highest capacity increase and a range of other benefits. Typically towers and conductors will not be changed but insulators may need to be upgraded to operate with DC lines.

The *main advantages* of converting existing AC line to HVDC are:

- ✓ an increase in capacity;
- ✓ fewer corona issues and a generally higher operating voltage;
- ✓ better control of active and reactive power and other system-level benefits;
- ✓ better stability limits and active stabilization of the grid;
- ✓ lower transmission losses

Some of the *disadvantages* of conversion to HVDC include:

- ✓ more pollution is attracted to insulators energized with DC – insulator upgrade is recommended;
- ✓ converter station costs.

Figure1.9 shows some common options for converting a single-circuit three-phase AC transmission into DC which include:

- ✓ The first option employs all three conductors for a single DC pole while the ground is used for return.
  This method will significantly increase current carrying capacity, but ground return will not be allowed in many modern systems.
- ✓ The second option adopts DC bipolar with metallic return. The neutral conductor can be used for monopolar operation.
- ✓ The third option is based on the triple HVDC concept. This method uses the third conductor alternatively as a positive or negative pole, which exploits the long thermal constants of conductors. The capacity increase of around 37% is achieved (over bipole configuration) using lines and the RMS values of current in the conductors (over10 minutes) are equal to the conductor rating. An additional bidirectional converter is required.

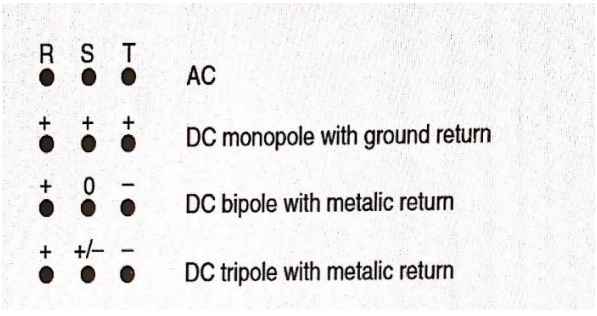

Figure 1.9 Options for conversion of three-phase AC lines into DC.

1.7 Ultra-High Voltage HVDC- UHVDC

The standard DC voltage for HVDC is 500kV and the Itaipu3150MW, ±600kV HVDC has used the highest DC voltage for a long period. However, the emerging requirements for bulk power transmission over long

distances of 5–10GW in Asia, Africa and South America in late 1990s have resulted in the progressive development of UHVDC (ultra-high voltage direct current).

Xiangjiaba–Shanghai 6400MW, ±800 kV UHVDC, implemented in 2010, was the first commercial UHVDC, and four others ±800kV systems have been implemented in 2011–2013, while studies are underway for 1100kV DC voltages. The progress towards UHVDC has demanded a lot of research and development effort and the main challenges are summarized below:

- ✓ improving insulation, in particular in polluted areas;
- ✓ transformer development, including bushings;
- ✓ developing ultra-high voltage (UHV) test centres.

It is important to appreciate that all the equipment, including auxiliaries that connect to DC lines, must be changed to UHV. In practice this translates to longer units – bushings, arresters, VT (voltage transducers), CT (current transducers), and so forth – with more series-connected basic elements. Frequently, the main challenge is the need for mechanical strength in the face of increased forces from seismic requirements, wind and other factors.

The use of new insulating materials and corona shields becomes a standard method of increasing insulation levels, although developing UHV insulators and bushings remains challenging. The UHV valve design is not considered to be a significant obstacle.

2 Thyristor

2.1 Operating Characteristics

The thyristor is an essential component in high-voltage direct-current (HVDC) valves and it is still one of the most common devises used in power-switching applications in all industries. This is attributed to its high-power ratings, robustness and high efficiency. Single devices have up to 8500V, 4500A capability, they are built on single wafers of up to 150mm in diameter and have been in existence since the 1950s.

The thyristor is a four-layer, three-terminal device as shown in Figure 2.1. The three connection A anode, K-cathode and G -gate. When gate current is applied, the layer between J2 and J3 becomes negative (N) and the thyristor becomes a PN device similar to a diode, also shown in figure 2.1. Functionally, it is similar to a diode, but the start of conduction can be delayed using the gate circuit.

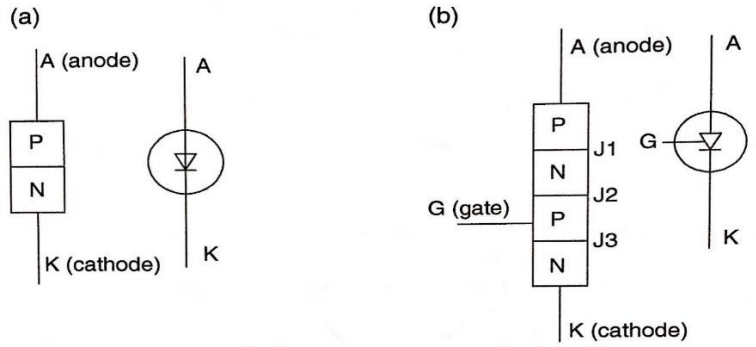

Figure 2.1 Structure and symbol for (a) diode and (b) thyristor.

A thyristor can be considered as controllable diode, as shown in operating curves in figure 2.2. With no gate current $i_g = 0$ it behaves like an open circuit (OFF state) both in forward and reverse directions. A forward voltage across the device (A positive with respect to K) results in junction J1 and J3 being forward biased, whereas J2 is reverse biased, and therefore only a small leakage current flow. If V_{AK} is increased to a critical limit, the device switches suddenly to a conducting state as the result breakdown or breakover of J2. If a gate current i_g is applied, then the magnitude of V_{AK} needed for breakover is dramatically reduced the device behaves like a diode. The level of i_g required is small compared to the main power current. The current I_1 is called the latching current, which is the anode current required to ensure thyristor switches to the ON state. Once the anode current reaches I_1, the gate current can be removed. The gate current is therefore a short pulse of 10-50μs. Theoretically, gate pulse is required once per half cycle but, in practice, gate pulses are sent multiple times per half cycle to ensure firing under all operating conditions.

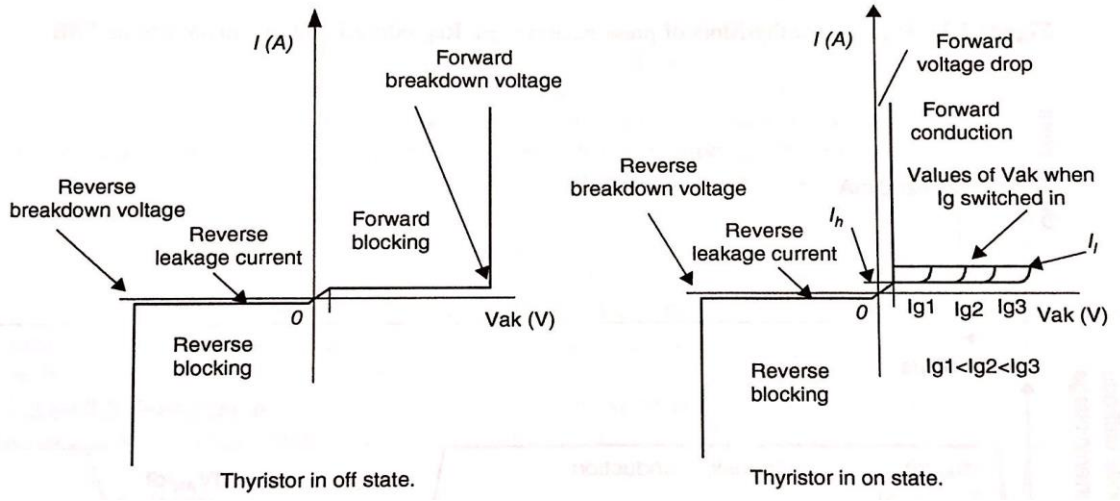

Figure 2.2 *Thyristor operating curves.*

Once the device is conducting, i_g can be reduced and the device remains in the ON state. When the device is in conduction, its state is determined solely by the anode current. If the anode I_A falls below some critical value, the holding current I_h (typically few milliamperes), the device switches off reverting to the blocking OFF state.

If a reverse voltage is applied across the device, (*negative* V_{AK}), J1 and J3 become reverse biased, only J2 is forward and therefore only a small leakage current flow. If negative V_{AK} is increased sufficiently, then eventually avalanche breakdown occurs across J1 and J3 resulting in damage to the device unless steps are taken to limit the current. The reverse breakdown may not be destructive. The forward and reverse blocking capability are similar for a given thyristor and they have good temperature stability for typical operating temperatures below 125^{o}c. However, forward-blocking capability deteriorates very fast with temperature above 125^{o}c.

Figure 2.3 High power thyristor and diode.

2.2 Switching Characteristic

A typical switching characteristic for an operating cycle of a thyristor is shown in Figure 2.4. The top graph shows the gating circuit current and the bottom graph shows the anode current and V_{AK} voltage. If a device is forward biased (V_{AK} positive) and a gate-current pulse is applied, the device switches on. Once a thyristor is in conduction, the gate has no control over the device. The device conducts even if the gate

pulse is now turned off. There is a delay while the device switches on, which is termed the *on time,* t_{on}. During the time $t_{on,}$ which is in the order of few microsecond, the voltage across thyristor reduces and the current increases. The rate of current rise at turn on should be limited (to around 100/μs), in order to allow current spreading across the entire PN junction surface. If the current rise too fast the thyristor can be destroyed because of local thermal melting. For a large thyristor it may take around 1ms for current to spread across whole surface area, in which interval the conduction loss is high.

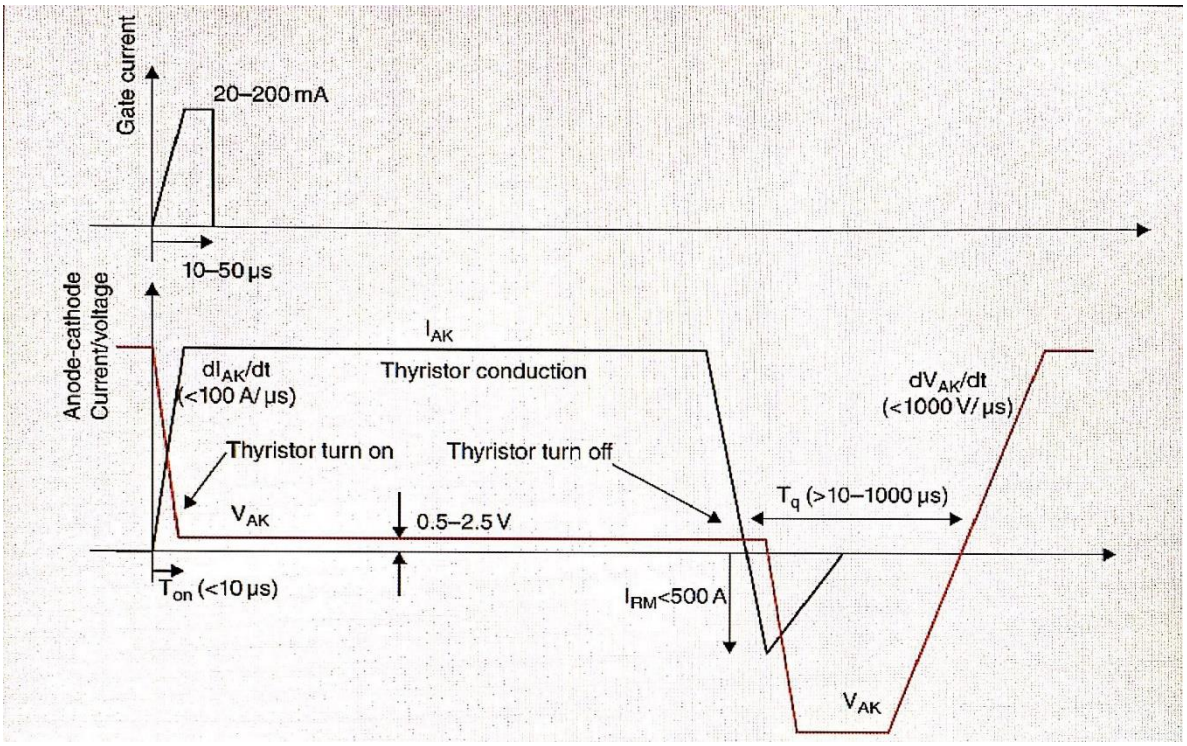

Figure 2.4 *Thyristor switching characteristic.*

In the conduction state, a typical voltage drop across am large thyristor is 1.5-2.5 V.

The device turns off when the anode current reduces to zero, which is driven by the external circuit in which thyristor is connected. There are two possible turn-off conditions:

- ✓ The current can fall to zero naturally, as would be the case in some resonant converters or with pulse power applications. The current can also naturally fall zero in discontinuous converter mode, as for example in case of HVDC converter operation with very low DC current. Thyristor

turn off during normal conduction interval is not desirable and this is prevented by sending repeated gate pulses.

- ✓ The thyristor current can fall to zero if another thyristor in the converter is fired and consequently the load current commutates to the other thyristor. This is a common commutation with HVDC converters.

On turning off thyristor, is reverse biased in the converter circuit and it can immediately withstand full reverse blocking voltage. However, a thyristor cannot immediately withstand forward blocking voltage. After the current falls to zero it is necessary to keep the device reverse biased for a short period of time in order to allow full recombination of charge carrier on the PN junction. After this period, the thyristor is able to gain forward-blocking capability, as required in the next cycle. The minimum reverse bias time after current falls to zero is called the extinction time t_q. The extinction time is typically 10-50μs for small thyristors but for those used with HVDC it is 300-1000μs. If this condition is violated (a forward voltage is reapplied immediately after I_A goes to zero) the device will switch to ON state even without a gate pulse. This unwanted turn on can be destructive for a thyristor. A special firing logic will normally intentionally fire thyristors if such conditions are detected.

The rate forward-blocking voltage increase should also be limited (typically to around 1000 V/μs) to prevent unwanted triggering. The PN junction behaves as a capacitor and therefore a sufficiently large *dv/dt* will generate node current *(i =c(dv/dt))*, which can cause latching.

Figure 2.5 illustrates thyristor operation in the simplest AC/DC converter with an inductive-resistive load. In this **single-phase**, **half-wave converter** thyristor can be fired only in positive half cycle giving a crude DC voltage consisting of positive and negative segments. The operation with firing angle of around 40^0 is shown in this figure. It should be observed that current lags voltage and therefore the thyristor conducts for periods while it is forward biased but also for some interval while it is reverse biased. The thyristor is turned off when anode current naturally falls to zero.

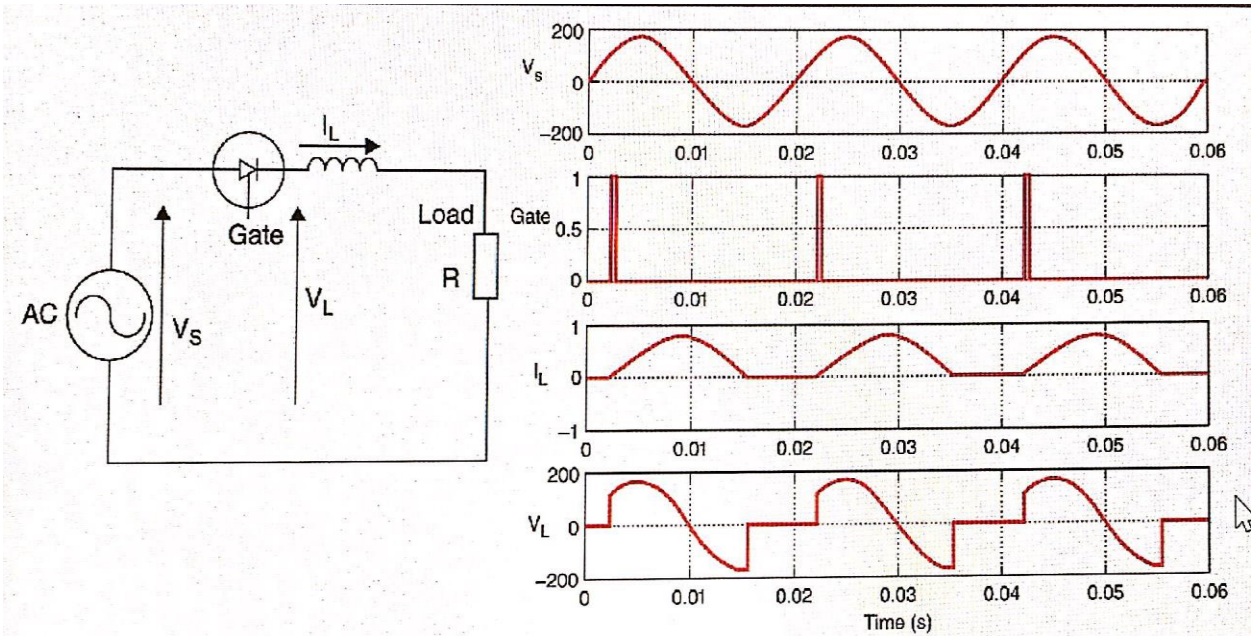

Figure 2.5 *Thyristor in a single-phase half-wave converter. Firing angle is 40^0.*

Example 2.1

Study a single-phase half-wave rectifier, with a circuit as in Figure 2.5. and, and with same $V_s = 120v$,

$f_s = 50$ HZ but assume a purely resistive load $R = 50\ \Omega$. Assume that firing angle is 80^o . Sketch the load voltage and compare with Figure 2.5. Explain whether such circuit would be feasible in practice. Calculate the value of required snubber L_s.

Solution:

Figure 2.6 shows the circuit and the waveforms. It can be seen that the load current is in phase with voltage and the load voltage has no negative segments.

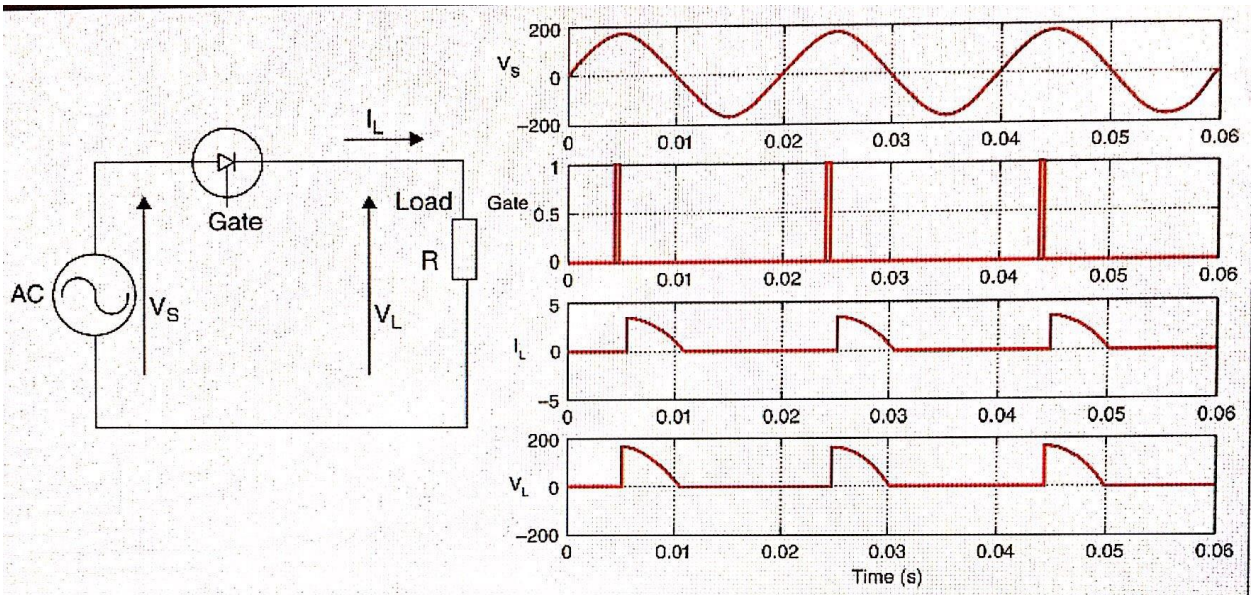

Figure 2.6 *Thyristor in a single-phase half-wave converter with resistive load in Example 2.1.*

The problem with this circuit it that current derivative at turn-on is very high and in particular at high firing angles. This might destroy the thyristor, so a di/dt protective snubber would be needed.

In order to calculate Ls the current equation is studie: $i_L(t) = V_s / R\ (1 - e^{R/Lst})$

Assuming that the supply voltage is constant for the duration of switching transient, and considering worst case peak voltage, and therefore $V_s = 169$ *V, while the current derivative is:*

$$di_L / dt = (V_s\ R / R\ L_s) e^{R/Lst}$$

And the initial current derivative for t = 0 is: $di_L / dt\ (t = 0) = V_s / L_s$

Therefore to limit the current derivative to di / dt = 100 A /μs , an inductor of at least $L_s > 1.69$ *μH*

2.3 Losses in HVDC Thyristors

Losses in a semiconductor component occur as a product of the current through the device and the voltage across the device. The losses are dissipated as heat and, in large HVDC converters, the total requirement for heat removal can be significant, approaching several megawatts. High-voltage direct-current converters typically use special liquid cooling system, which have an effect on losses, costs and system reliability.

The main losses in HVDC converter thyristors include:

- ✓ Conduction losses;
- ✓ Turn-off losses;
- ✓ Snubber losses;

- ✓ Reverse-leakage current loss;
- ✓ Forward-leakage current loss;
- ✓ Gate driver loss.

The principal loss components in HVDC converters include conduction and turn-off losses. Figure 2.7 shows the shape of ON-state curves for a thyristor. The voltage across thyristor can be expressed as:

$$V_T = V_{T0} + R_{on} i_T \tag{2.1}$$

Where V_{T0} is the threshold voltage (at zero current), which is typically $1<V_{T0}<1.5V$ depending on thyristor voltage rating; R_{on} is the on state resistance, which is typically $0.5<R_{on}<2m\Omega$, depending on current rating; and i_T is the anode instantaneous current.

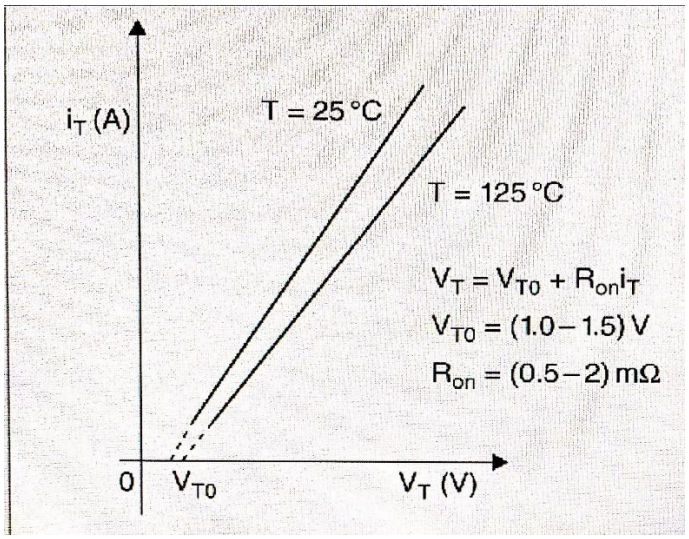

Figure 2.7 *Typical on-state characteristic for a high-power thyristor.*

The on-state loss power can be determined by integrating the product of the current and the voltage.

$$P_{con} = \frac{1}{T}\int_0^T v_T i_T = \frac{1}{T}\int_0^T \left(V_{T0} i_T dt + R_{on} i_T^2 dt\right) = V_{T0} I_{TM} + R_{on} I_T^2 \tag{2.2}$$

Where T is period, I_M is the average thyristor current, which can be determined by instantaneous

Current or using the duty ratio δ (i.e. conducting period as a percentage of the full cycle) and I_T is the RMS value of thyristor current. In a six-pulse bridge each thyristor conducts for 120^o and therefor $\delta = 0.33$.

A typical turning-off curve of a thyristor is shown Figure 2.8. The current overshoots to a small negative value to recover charge in the P-N junctions, and the element switches off after period of time. The peak

reverse current I_{RM} depends on the current falling derivative (di_T/dt) and the peak conducting current I_{TRM}. There are detailed methods to calculate the reverse-recovery loss, but simplest method is to use the reverse-recovery charge Q_{RR} or turn-off energy loss E_{off} , which is supplied in the thyristor manufacturer data sheets. The reverse recovery loss power is:

$$P_{off} = \int_0^{t_{off}} i_T v_t dt$$

$$P_{off} = E_{off} f_s \qquad (2.3)$$

Where f_S is the thyristor switching frequency.

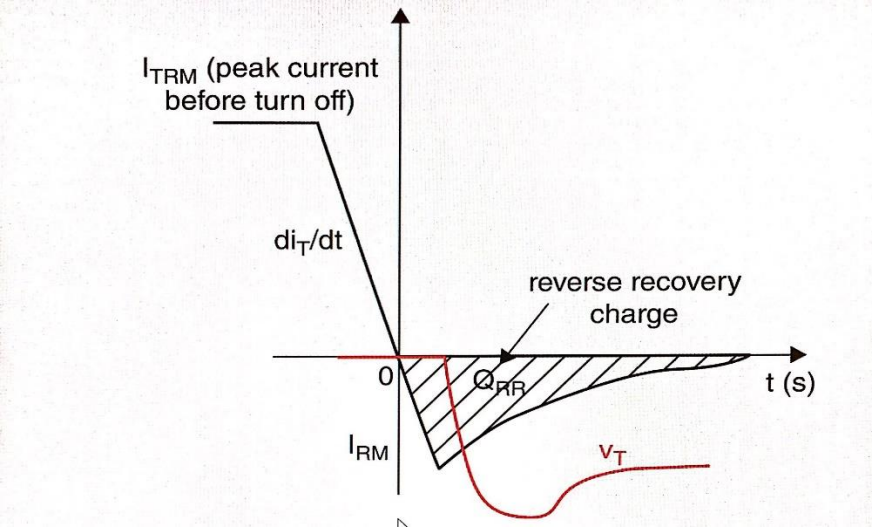

Figure 2.8 *Thyristor turning OFF.*

Example 2.2

A six-pulse 2000 A,500 KV HVDC converter employ thyristors with the characteristics shown in Figure 2.9. These thyristors have a 6500V, and 2800A rating and 170 devices are used in each valve. The blocking voltage across each thyristor is therefore 2941V. Assume that the series inductor is designed to di/dt to 10A /μs. The converter operates in a typical six-pulse pattern with 120^o conducting intervals. Calculate the total losses in this converter.

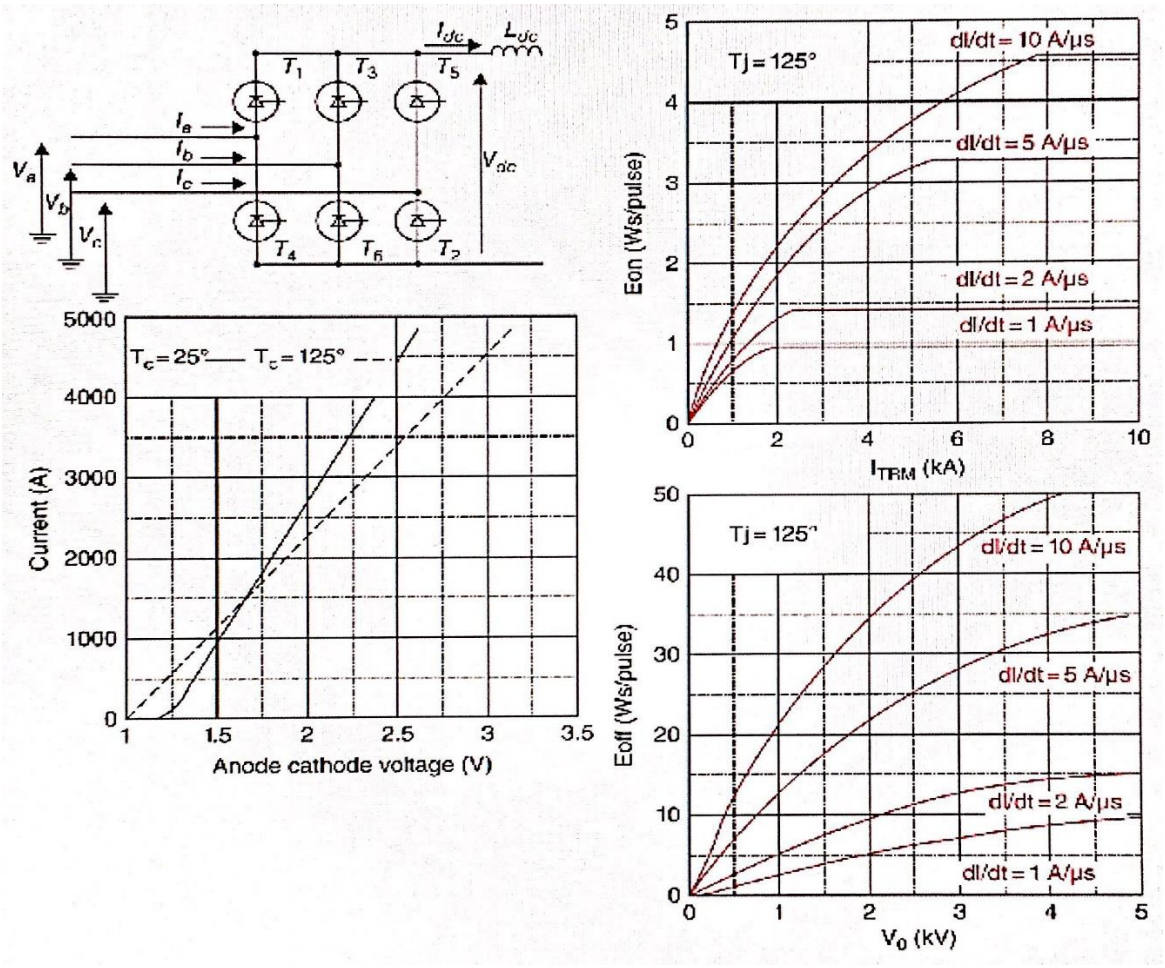

Figure 2.9 *Test thyristor on-state and turn on/off energy curves.*

Solution:

From Figure 2.9, $V_{T0} = 1V$, $R_{on} = (1.7 - 1) / 2000 = 0.00035\ \Omega$, $E_{on} = 2.2Ws / pulse$, $E_{off} = 43Ws / pulse$,

The total ON-state loss is:

$$P_{con} = 2n3\left(V_{T0}I_{TM} + R_{on}I_T^2\right) =$$

$$P_{con} = 2 \times 170 \times 3\left(1 \times \frac{2000}{3} + 0.00035 \times \left(\frac{2000}{\sqrt{3}}\right)^2\right) = 1.144\,\text{MW}$$

The turn-on loss is:

$$P_{on} = E_{on} f_s = 6 \times 170 \times 2.2 \times 50 = 0.112\ MW$$

The turn-off loss is:

$$P_{off} = E_{off}\ f_s = 6 \times 170 \times 43 \times 50 = 2.19\ MW$$

The total percentage loss is:

$$P_{loss} = (P_{con} + P_{on} + P_{off}) / (I_{dc} \times V_{dc}) = (1.144 + 0.112 + 2.19) \times 10^{6} = 0.34\%$$

2.4 Valve Structure and Thyristor Snubbers

Figure 2.10 shows the converter valve structure, which may include hundreds of individual thyristor assemblies, ground in a number of valve racks. Figure 2.11 illustrates the design of a thyristor valve rack and Figure 2.12 shows valve racks forming six valves, which are suspended from the ceiling in a valve hall. The thyristor assembly includes a thyristor, driver, passive, driver-protection circuits and monitoring electronics. Three protections are shown in the figure: L_s for di/dt protection, RC for dv/dt and overvoltage protection and R_{dc} grading resistor for balancing voltages across switches in a valve.

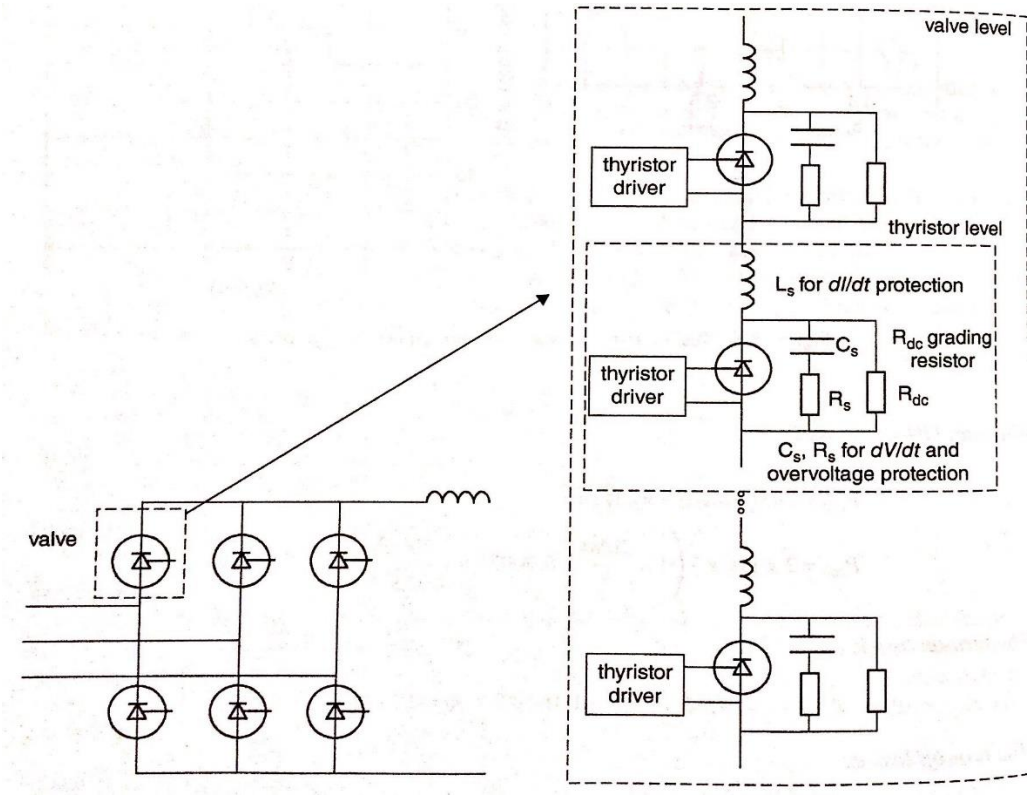

Figure 2.10 *Thyristor valve structure and protection for dv/dt and di/dt.*

Figure 2.11 *Thyristor valve rack assembly. Reproduced with permission of Siemens.*

Figure 2.12 *HVDC Thyristor valves hall of the Celillio converter Station in the Dalles, Oregon*

When a gate pulse is sent, the thyristor starts conducting initially in the PN region around the gate connection and the conducting area gradually spreads. If the current gradient is too large, the initial area around the gate will be overhead before current spreads across full thyristor may be destroyed. In order to limit *di/dt,* a small inductor is used in series with the thyristor, as shown by *Ls.*

The device is also susceptible to large rates of voltage change. Too great a *dv/dt* can result in the device turning on without a gate pulse, which can be destructive. The *dv/dt* applied to the device can be limited using a parallel snubber circuit comprising an RC combination in series. The same snubber also limits the magnitude of reverse voltage at the turn-off instant. A capacitor is sufficient to limit the voltage but this capacitor discharge through the thyristor at the next turn on. A series resistor, R_s, is the therefore employed to limit the capacitor discharge current at the next turn on. This resistor causes losses but, overall, the RC snubber reduces losses in the switch, and the RC snubber transfers losses from the switch to the snubber resistor.

An HVDC valve may consist of hundreds of individual thyristors connected in series, which should ideally be all stressed to the same voltage during all operating conditions. A small difference in thyristor on-state resistance or switching-on speed will be subjected to overvoltage and may be destroyed. The grading resistors are used to help equalized voltage sharing between the thyristors in a valve.

2.5 Thyristor Rating Selection and Overload Capacity

Thyristor current rating is commonly specified as average ON-state current, I_{TM}. The current rating is influenced by the junction temperature and therefore it depends on the thermal management. Normally rating is optimized and there will be no overload capability unless this is considered in the design rated. If thyristor temperature exceeds rated values, the forward-blocking capability reduces rapidly, which can lead to unwanted triggering, excessive currents and thermal runaway.

Thyristor manufacturers also specify in their datasheets the peak nonrepetitive surge current $I_{TSM,}$ which is typically around ten times the rated current. This current peak is specified on a 10ms half-sine pulse at rated temperature, however it is nonrepetitive. The temperature of the junction will rise significantly during such a high pulse and the thyristor will not be able to withstand further blocking voltage. On detection of overcurrent, the protection system will block the thyristor driver for a period of time until the temperature is sufficiently reduced to resume normal operation. The manufacturers also specify limiting load integral I^2t, which can be used to calculate nonrepetitive peak pulse for a different duration.

The thyristor voltage rating is specified as maximum repetitive peak forward voltage V_{DRM} or V_{RRM} are exceeded even for a very short time. Because of voltage variations during normal operation and the presence of harmonics, typical operating voltage stress for a thyristor will be selected at around 50% of the maximum repetitive forward/reverse voltage.

3 Six-Pulse Diode and Thyristor Converter

3.1 Three-Phase Uncontrolled Bridge

A three-phase full bridge (Gratz bridge) diode converter is shown in Figure 3.1. This is the simplest three-phase topology, which will illustrate three-phase AC/DC conversion. This converter operates in the same way as a thyristor converter with zero delay angle.

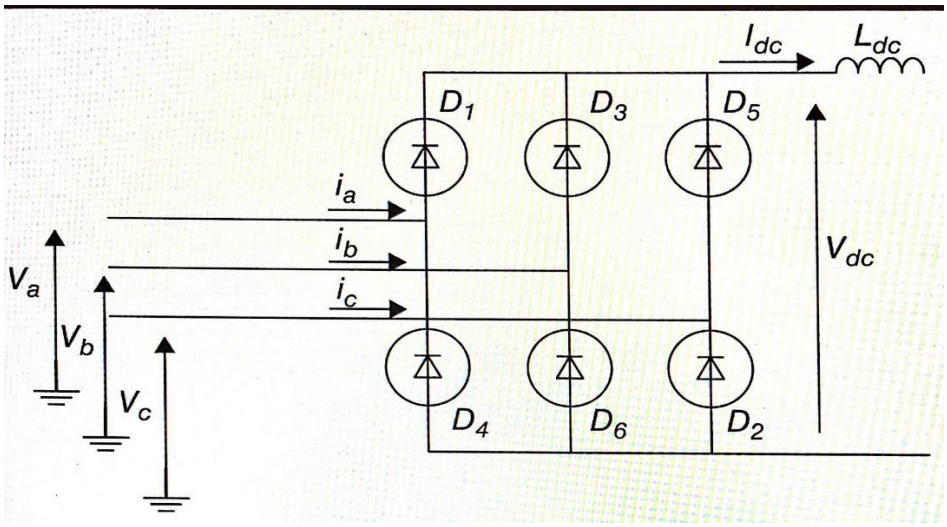

Figure *3.1* *Diode six-pulse AC/DC converter*

The AC system is assumed to be symmetrical and balanced and the voltages are defined as:

$$v_a = V \cos(\omega t) \tag{3.1}$$

$$v_b = V \cos\left(\omega t - \frac{2}{3}\Pi\right)$$

$$v_c = V \cos\left(\omega t + \frac{2}{3}\Pi\right)$$

Where *V* is the line-neutral peak magnitude voltage. Note that the switches are connected to the positive DC pole and the remaining three switches to the negative pole where the label numbers correspond to the sequence of conduction. The diodes will start conducting when node voltage is higher than cathode. Therefore, diodes conduct when the respective phase voltages are at highest value, as shown in figure 3.2, for a test system consisting of diode converter between AC system V_{LL} = 410 kV and DC source of 500 kV. Each diode conducts for 1/3 of a cycle (120°). At any time one diode conducts on the positive rail and one on the negative.

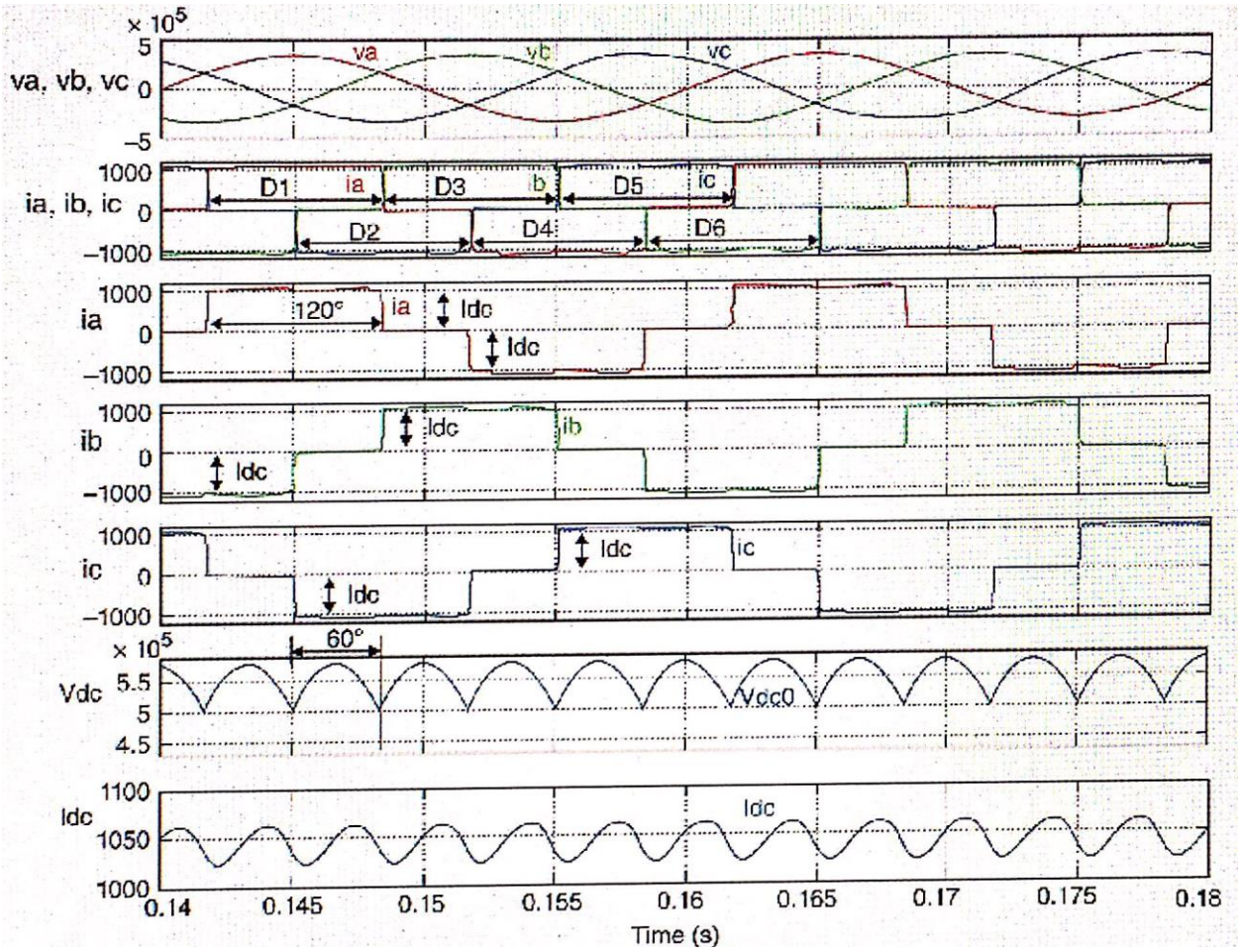

Figure 3.2 *Three-phase diode bridge plots.*

The DC-side inductor ensures that DC current stays approximately constant for one pulse, and therefore Dc current commutates form one switch to another every 60º. The commutation occurs every 120º on the positive rail and on the negative rail, however commutation instants on the negative rail are lagging by 60º.

The diode bridge average DC voltage can be calculated by averaging the surface below the V_{dc} curve:

$$V_{dc0} = 2\frac{3}{2\pi}\int_{\pi/6}^{\pi/6+2\pi/3} V\cos\omega t\, d(\omega t) \tag{3.2}$$

$$V_{dc0} = \frac{3\sqrt{3}}{\pi}V = \frac{3\sqrt{6}}{\pi}V = \frac{3\sqrt{2}}{\pi}V_{LL} \tag{3.3}$$

Where V is the-neutral RMS voltage and V_{LL} is the line-line RMS voltage. The above DC voltage V_{dco} is called the ideal no load voltage. It corresponds to the voltage of a thyristor rectifier with zero firing angle. This is also the maximum DC voltage that a six-pulse thyristor converter can achieve.

The AC current in each phase consists of 120º long squares per each half cycle. The peak magnitude of fundamental component of AC current is obtained using the Fourier series:

$$I = 2\frac{1}{\pi}\int_{\pi/6}^{\pi/6+2\pi/3} I_{dc}\cos(\omega t)d(\omega t)$$

$$I = 2\frac{\sqrt{3}}{\pi}I_{dc} \tag{3.4}$$

The RMS value of fundamental component of AC current is from Eq. 3.4:

$$\mathrm{I} = \frac{\sqrt{6}}{\Pi}I_{dc} \tag{3.5}$$

3.2 Three-phase Thyristor Rectifier

This section considers three-phase bridge topology as in the previous section, but thyristor delay angle is considered and a commutation overlap (resulting from transformer inductance) is included. Figure 3.3 shows the converter topology.

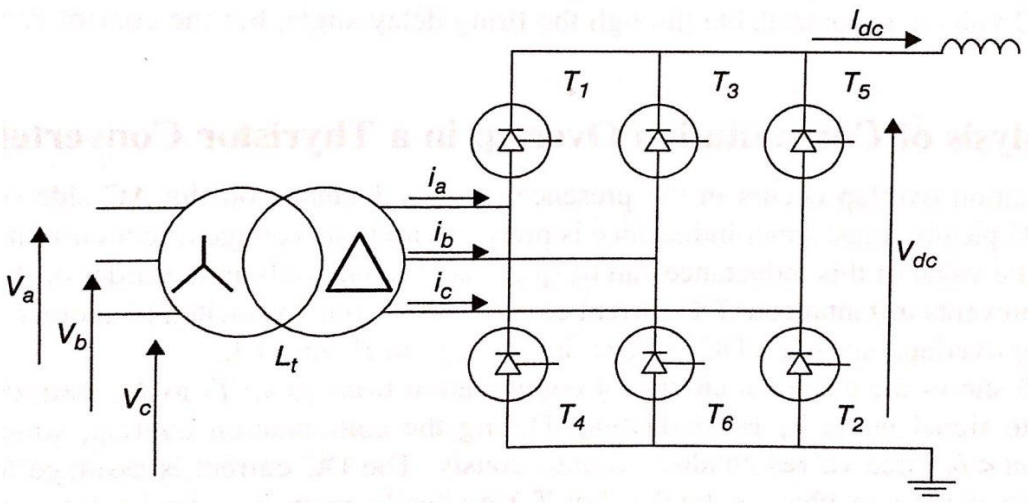

Figure 3.3 *Thyristor six-pulse AS/DC converter with a transformer.*

Figure 3.4 shows the voltage and current waveforms, assuming similar parameters as in Figure 3.2 but thyristors are employed, and converter is interfaced using L_t = 0.1H The operation is similar to that in Figure 3.2, however a firing-delay angle α introduced. The delay angle is measured from the instant of positive thyristor forward voltage (intersection of two phase voltages), which corresponds to 30° on phase α voltage.

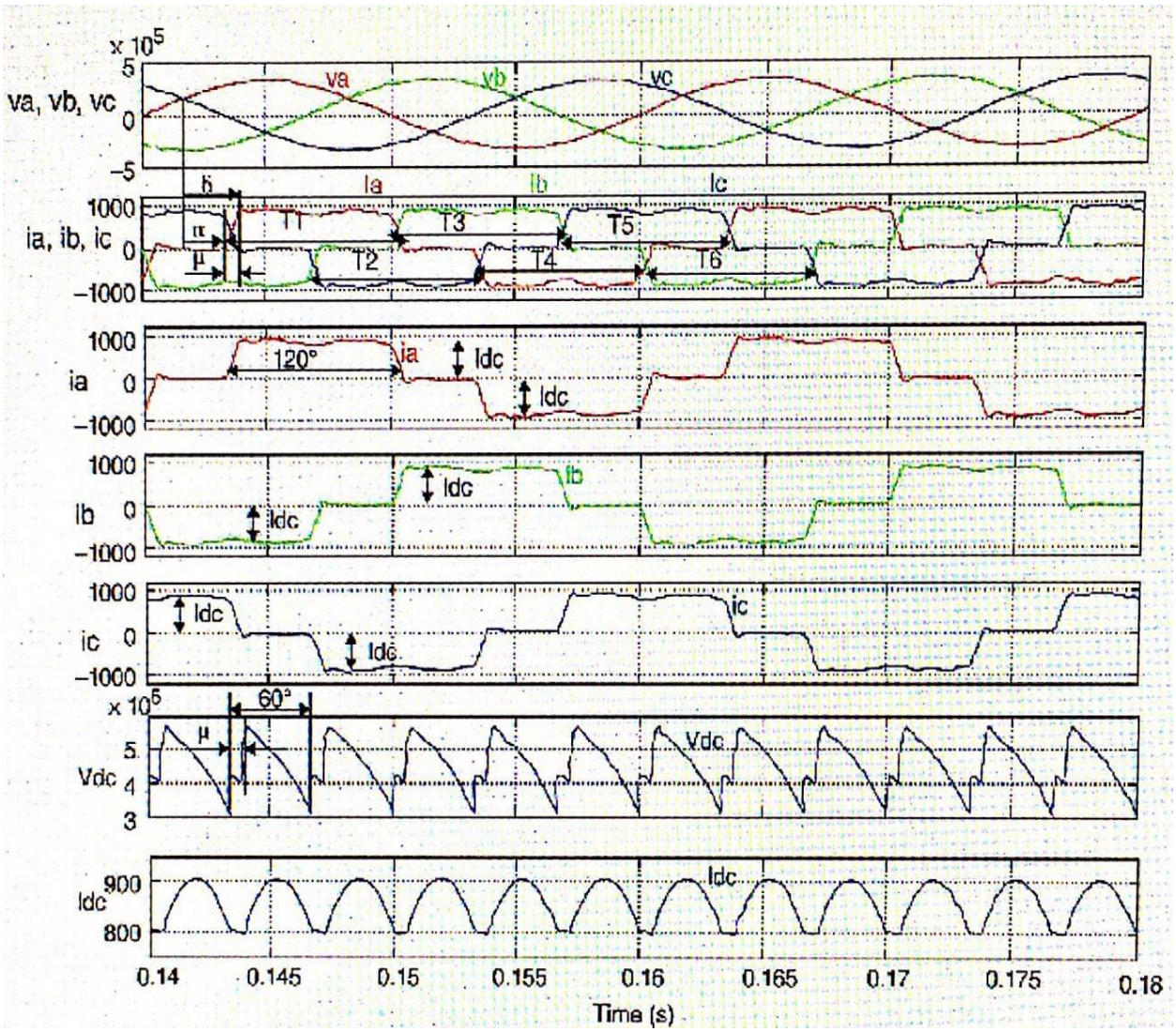

Figure 3.4 *Thyristor six-pulse AC/DC converter with transformer (L_t = 0.1H) and ignition delay (α = 30)*

Figure 3.4 also shows the commutation overlap μ, resulting in a DC voltage dip each time the commutation occurs. Neglecting initially the commutation overlap, the average DC voltage DC voltage can be obtained considering surface below the DC voltage curve:

$$V_{dc} = 2\frac{3}{2\pi}\int_{\pi/6+\alpha}^{\pi/6+\alpha+2\pi/3} V\cos\omega t\, d(\omega t) \tag{3.6}$$

$$V_{dc} = \frac{3\sqrt{3}}{\pi}V\cos\alpha = \frac{3\sqrt{6}}{\pi}\mathrm{V}\cos\alpha = \frac{3\sqrt{2}}{\pi}\mathrm{V_{LL}}\cos\alpha \tag{3.7}$$

The above DC voltage is also expressed as:

$$V_{dc} = V_{dc0} \cos\alpha \qquad (3.8)$$

Where V_{dco} *is* the diode bridge ideal DC voltage defined in Eq.(3.3). This formula illustrates that the converter DC voltage is controllable through the firing delay angle, but the gain is nonlinear.

3.3 Analysis of Commutation Overlap in a Thyristor Converter

The commutation overlap occurs in the presence of an inductance on the AC side of the thyristor converters. Typically transformer inductance is present with high-voltage direct-current (HVDC) converters and the value of this inductance can be quite large, commonly in the order of 0.1-0.2pu. This inductance prevents instantaneous DC current commutation from one switch to another. The result is a commutating overlap, causing a DC voltage dip, as seen in Figure 3.4.

Figure 3.5 shows the electrical circuit for commutation from valve T_1 to T_3, assuming that T_3 has received gate signal while T_1 is conducting. During the commutation overlap, which lasts in the period $\alpha < \omega t < \delta$, three valves conduct simultaneously. The DC current assumed to be constant. The outgoing current in phase α (and valve T_1) gradually reduces, whereas the current in phase B (and valve T_3) gradually increases, as shown in the time-domain converter variables during the commutation process in Figure 3.6. Table 3.1 shows how the main variables evolve during the commutation process. Note that the converter voltage (V_{g_LL}) is measures on the grid side of the transformer and it is appropriately scaled for the transformer ratio.

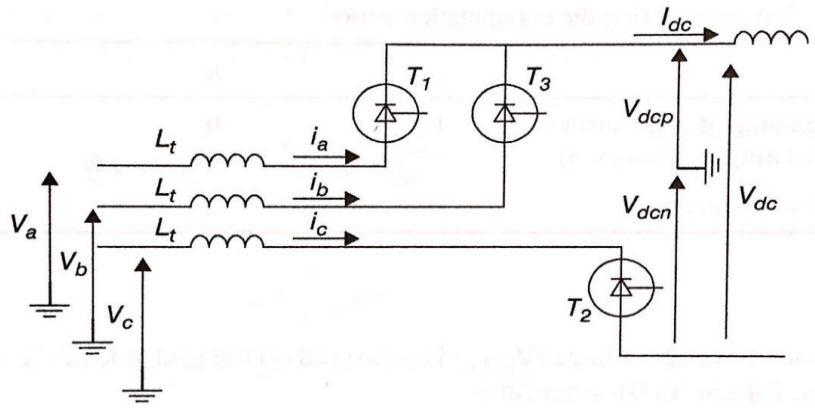

Figure 3.5 *Converter equivalent circuit during commutation.*

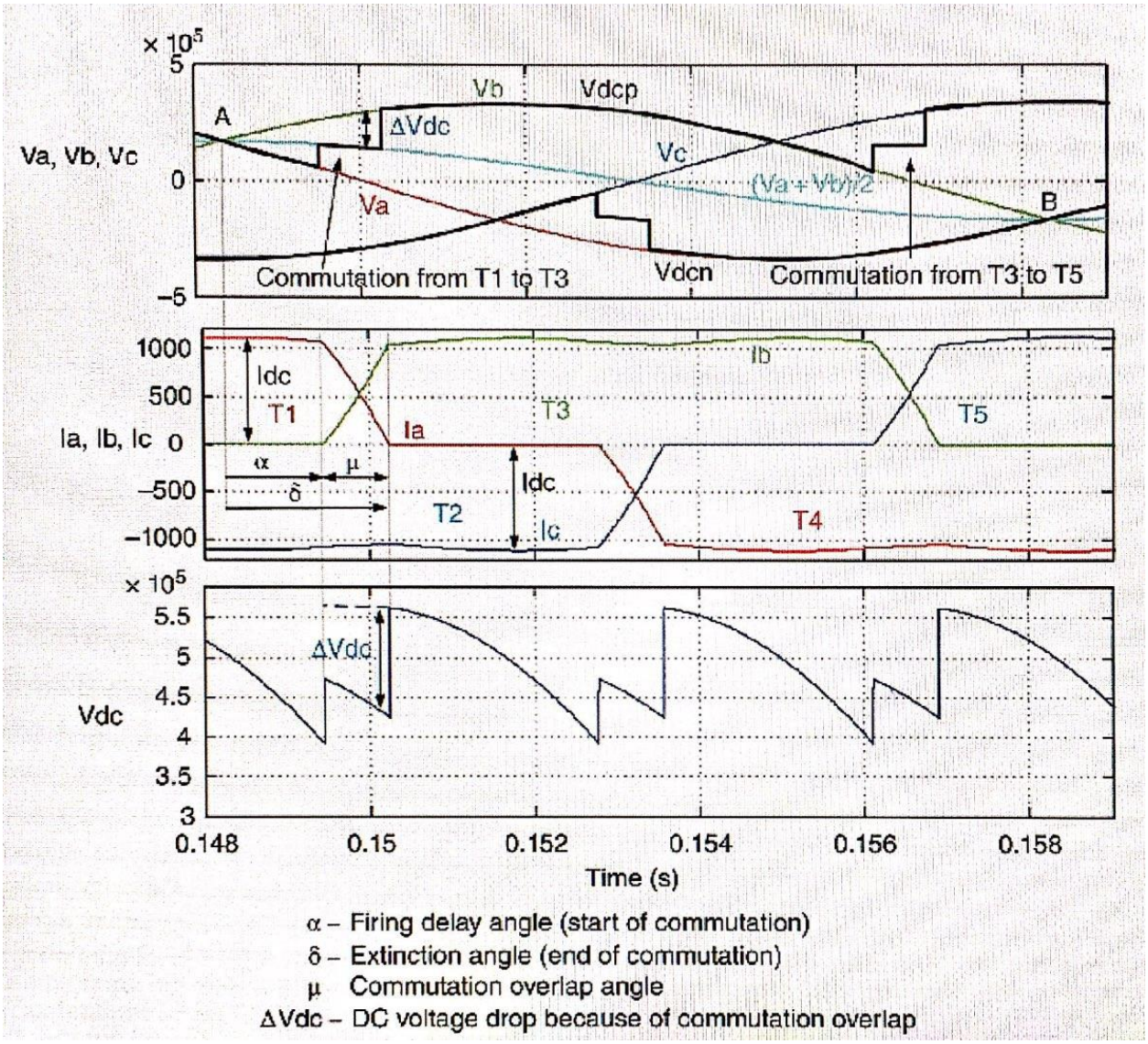

Figure 3.6 *Commutation from valve T_1 to T_3 (phase A to phase B) in rectification mode.*

Table 3.1 *Variables during the commutation period.*

Variable	i_a	i_b	V_{dcp}
ωt = α (beginning of commutation)	I_{dc}	0	V_a
α < ωt < δ (during commutation	$\frac{\sqrt{6}V_{g-ll}}{2Lt} = dia/dt$	$\frac{\sqrt{6}V_{g-ll}}{2Lt} = dib/dt$	$(V_a + V_b)/2$
ωt = δ (end of commutation)	0	I_{dc}	V_b

The commutation can only happen between points A and B, while $V_b > V_a$. In rectification mode, commutation happens close to point A, where in inversion the converter is operated with large firing angles, close to point B. This section considers rectification only.

With reference to the circuit in Figure 3.5, the Kirchhoff's voltage equation along the commutation loop ($\alpha < \omega t < \delta$) is:

$$V_a - V_b = L_t (di_a / dt) - L_t (di_b / dt) \quad (3.9)$$

From the above formula, assuming a balanced system, the current equation can be derived:

$$\frac{\sqrt{6}V_{g-ll}}{2Lt} = dia/dt \quad (3.10)$$

Integrating, the phase α current during commutation is:

$$\frac{\sqrt{2}V_{g-ll}}{2\omega Lt} = (cos\alpha - cos\omega t) \quad (3.11)$$

Since $i_a = 0$ for $\omega t = \alpha$ and $i_a = I_{dc}$ for $\omega t = \delta$, as seen in Table 3.1, the above equation become:

$$\frac{\sqrt{2}V_{g-ll}}{2\omega Lt} = (cos\alpha - cos\delta) \quad (3.12)$$

$$\frac{\sqrt{2}V_{g-ll}}{2\omega Lt} = (cos\alpha - \cos(\alpha + \mu))$$

Equation (3.12) enables the prediction of the end of commutation (angle $\delta = \alpha + \mu$), if the start of commutation (control angle α), AC voltage V_{LL} and DC current I_{dc} are known:

$$Cos\ (\alpha + \mu) = cos\alpha - \frac{I_{dc} \cdot 2\omega l_T}{\sqrt{2} v g_{-lL}} \quad (3.13)$$

This analytical result is important and is used with inverter controllers to predict the extinction agle, as discussed in Chapter 5. The commutation process has the effect of reducing DC voltage by the value V_{dc_com}, as seen in Figure 3.6. This voltage drop can be calculated considering the surface area below the curve as:

$$V_{dc\_com} = \frac{1}{2\Pi / 3} \int_{\alpha}^{\delta} \left[v_b - \frac{v_a + v_b}{2} \right] d(\omega t) \quad (3.14)$$

$$V_{dc\_com} = (V_{dc0} / 2) \times (\cos\alpha - \cos\delta)$$

$$V_{dc\_com} = 3/\pi \times (I_{dc}\, \omega L_t)$$

From the above equation, the conclusion is derived that the commutation voltage drop depends on the direct current and has an effect equivalent to a fictitious resistance $R_c = 3\omega L_t / \pi$. Using Eqs (3.8) and (3.14):

$$V_{dc} = V_{dc0} cos\alpha - \Delta V_{dc} \quad (3.15)$$

$$V_{dc} = V_{dc0} \times (cos\alpha + cos\delta) / 2$$

$$V_{dc} = \frac{3\sqrt{2}}{\pi} v g_{-lL} \cdot cos\ \alpha - \frac{3}{\Pi} \omega L_t I_{dC}$$

Example 3.1

A six-pulse HVDC converter is connected to 220 kV AC grid using a 220 kV, 800 MVA, X_t = 12% transformer.

- ✓ Determine the commutation overlap if the rectifier is operating at 20° firing angle and an 1800A DC current.
- ✓ Determine the commutation overlap if the converter is operating 15° and with same DC current (tap-changer adjustment).
- ✓ Discuss how an increase transformer reactance will affect the commutation overlap.

Solution:

Transformer inductance is:

$$L_t = X_t \frac{V_{cll}^2}{S_t} \frac{1}{2\pi 50} = 0.12 \frac{330\,000^2}{800\,000\,000} \frac{1}{2\pi 50} = 0.052\,H$$

The turn-off angle and commutation overlap are calculated as:

$$\alpha + \mu = a\cos\left[\cos(20) - \frac{1800 \times 2 \times 314.15 \times 0.052}{\sqrt{2} \times 330{,}000}\right]$$

$$\alpha + \mu = 35.5°$$

$$\mu = 15.5°$$

With firing angle of 15°:

$$\alpha + \mu = 32.9°$$

$$\mu = 17.9°$$

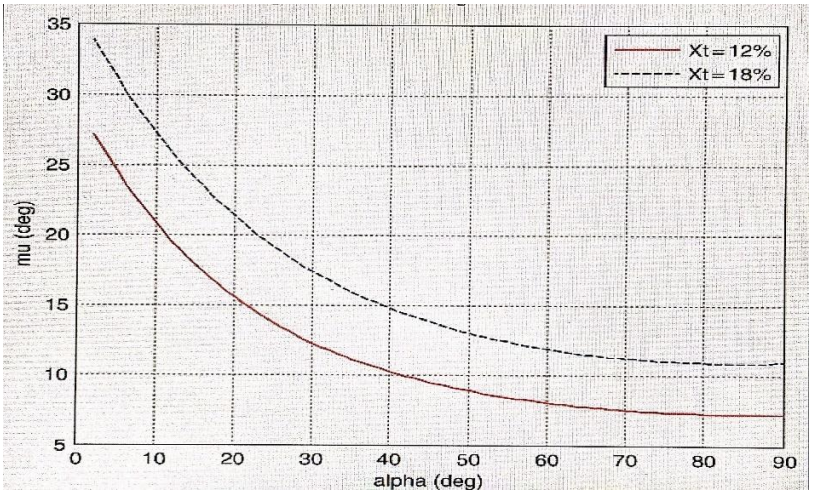

Figure 3.7 *Commutation angle as the function of operating angle in Example 3.1*.

Using Eq. (3.12), Figure 3.7 shows the commutation angle as the function of the operation angle for two values of transformer inductance. Larger transform leakage reactance will generate a larger commutation angle.

3.4 Active and Reactive Power in a Three-Phase Thyristor Converter

In order to get accurate expression for converter AC current and the power factor consider the power-balance equation:

$$P_{ac} = P_{dc0} \tag{3.16}$$

$$3VI\cos(\phi) = V_{dc} I_{dc}$$

Where ϕ is the power factor angle. Using Eq. s (3.15) and (3.16):

$$\text{I cos}(\phi) = \frac{\sqrt{6}}{\Pi} I_{dc} \frac{cos\,\alpha + cos\,\delta}{2} \tag{3.17}$$

The expression for AC current in Eq. (3.5) is obtained for $\mu = 0$, but it is accurate to within 5% even for a very large μ, and therefore it is justifiable to approximate:

$$I \approx \frac{\sqrt{6}}{\Pi} I_{dC} \tag{3.18}$$

Replacing Eq. (3.18) in Eq. (3.17), the following results.

$$\text{Cos}(\phi) \approx \frac{cos\,\alpha + cos\,\delta}{2} \tag{3.19}$$

Or using Eq. (3.15):

$$\text{Cos}(\phi) \approx V_{dc} / V_{dc0} \tag{3.20}$$

The power-factor angle is therefore directly dependent on firing angle and the overlap angle. It is concluded that the power factor is better if converter operates at low firing angles. For this reason the line-commutated converter (LCC) HVDC controllers optimize operating conditions to minimize a firing angle of around 15-20^o which leaves sufficient room for action in each direction. If the power factor angle is known, the reactive power can be calculated as:

$$Q = P\tan(\phi) \tag{3.21}$$

3.5 Inverter Operation

Figure 3.8 shows the converter DC voltage as a function of the firing angle, using Eq. (3.8), and the same test system as in previous sections. As the firing angle increase over 90^o, the DC voltage become negative and the converter moves into inversion mode. Current cannot change direction in thyristor converters, so negative DC voltage implies power reversal.

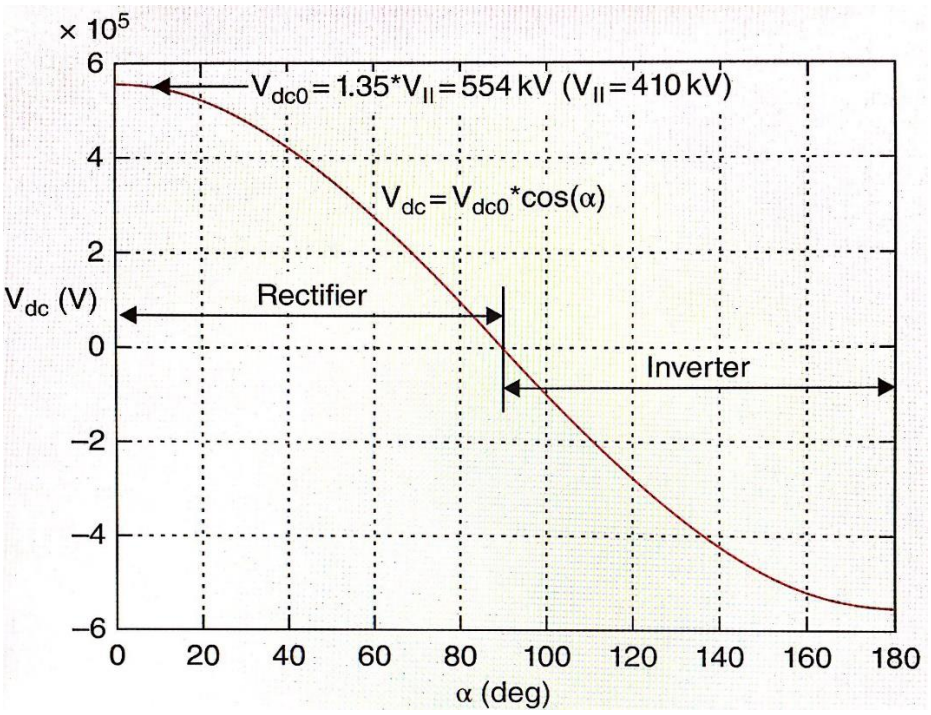

Figure 3.8 *Thyristor converter DC voltage as the function of firing angle.*

When the commutation overlap is considered, the condition for the inversion mode is from Eq. (3.15):

$$\text{Cos}\alpha + \cos\delta = 0 \qquad (3.22)$$

$$\alpha = (\pi - \mu)/2$$

Figure 3.9 shows the plot of converter variable in inversion mode. The firing angle 90<α<180, and the following angles are commonly used for inversion mode:

- ✓ Ignition advance angle β = 180 – α, and therefore cos(β) = - cos(α)
- ✓ Extinction advance angle γ = 180 – δ, cos(γ) = - cos(δ). Note that the overlap angle is: μ = δ – α = $\beta - \gamma$.

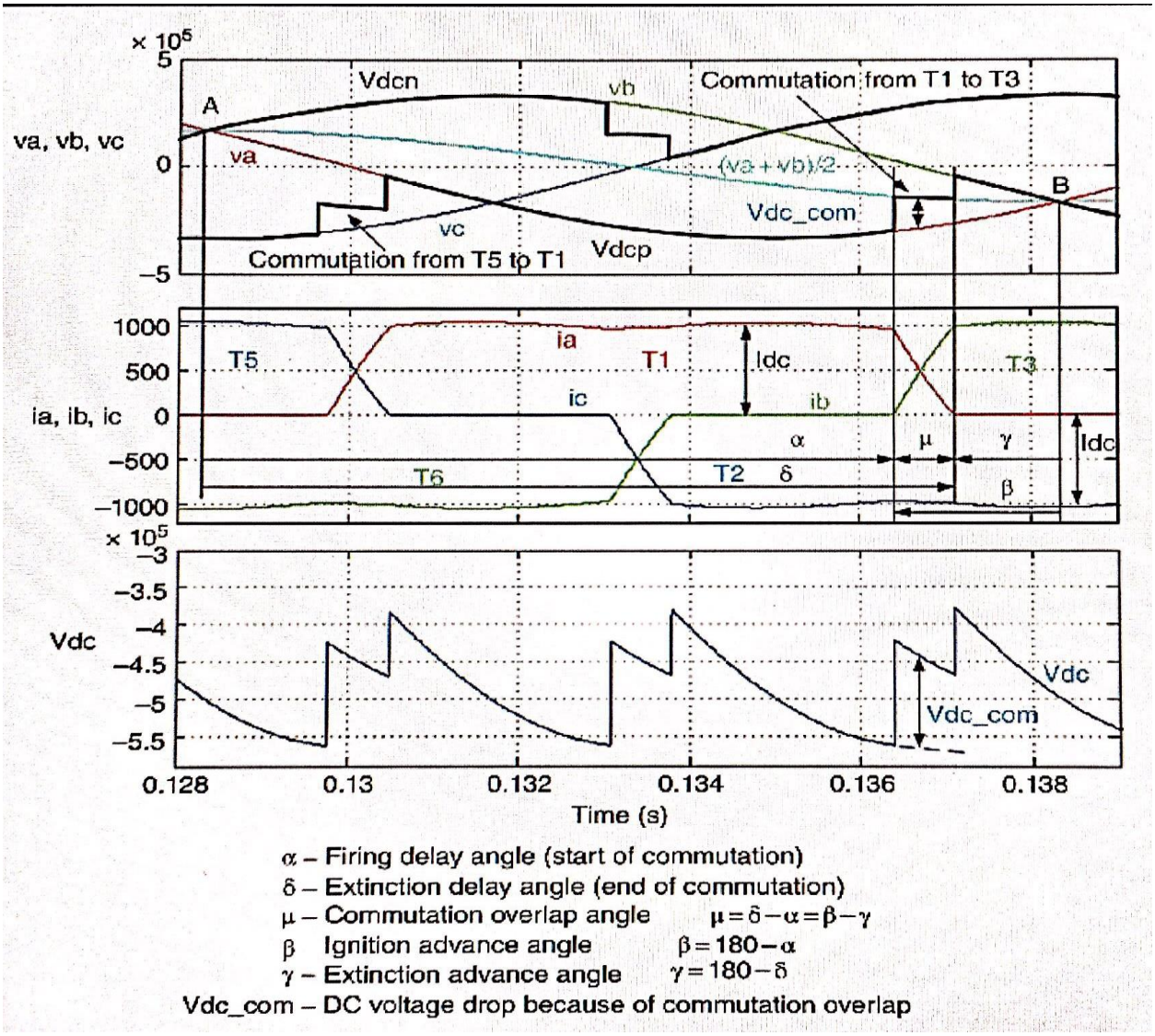

Figure 3.9 Commutation from valve T_1 to T_3 (phase A to B) in inversion mode.

The extinction angle is very important for inverter operation because it defines the safe period for thyristor reverse recovery. Referring to the plots in Figure 3.9, thyristor T_1 (connected to phase a) will turn off in the interval between points A and B. After turning off, it must recover the forward blocking state before point B. At point B it will become forward biased. Thyristor T_3 (connected to phase b) firing must also happen before point B, while it is forward biased. Therefore, the thyristor T_3 must be fired sufficiently early, because commutation overlap and the reverse recovery time must be completed point B. The control challenge at the inverter is how to determine firing angle α in order to achieve a balance between a sufficiently large Y and to avoid large reactive power caused by an excessively large Y. For a desired Y it is possible to calculate required firing angle αin steady state, but this is very difficult in transient conditions

Writing Eq. (3.15) with the above inverter angles:

$$V_{dc} = - V_{dc0} \cos \beta - V_{dc\_com} \qquad (3.22)$$

$$V_{dc} = - V_{dc0} (\cos \beta + \cos \gamma) / 2$$

Replacing further Eq. (3.3) in Eq. (3.23), and considering that the negative sign is usually omitted with inverter equation:

$$V_{dc} = \frac{3\sqrt{2}}{\pi} V g_{-lL} \cdot cos\, \beta - \frac{3}{\Pi} \omega L_t I_{dC} \qquad (3.24)$$

Rearranging further Eq. (3.23), DC voltage is obtained as the function of the extinction angle:

$$V_{dc} = \frac{3\sqrt{2}}{\pi} V g_{-lL} \cdot cos\ \gamma - \frac{3}{\Pi} \omega L_t I_{dC}$$

The above two equations are important because they describe the effect of different control strategies at the inverter. It is seen in Eqs. (3.24)-(3.25) that the commutating resistance a different effect (sign) on V_{dc} depending on whether control angle β or γ is kept constant:

- ✓ If firing angle β = *const* in Eq. (3.24), then a DC current increase implies a DC voltage increase. This will have stabilizing effect on the HVDC system.

- ✓ If γ = *const* in Eq. (3.25) (β is manipulated in order to maintain γ = *const* in an appropriate feedback loop) then a DC voltage. This will have destabilizing effect on the HVDC system.

The Eq. (3.12) for commutation overlap for inverter operation becomes:

$$I_{dc} = \frac{\sqrt{2} v g_{-ll}}{2\omega L_T} (\cos\, \gamma - \cos\, \beta) \qquad (3.26)$$

$$I_{dc} = \frac{\sqrt{2} v g_{-ll}}{2\omega L_T} (\cos\, \gamma - \cos(\ \gamma + \mu))$$

Example 3.2

An HVDC inverter uses thyristor that have 700 μs turn-off time. Determine the safe extinction angle for this converter. Analyse how the extinction angle depends on the turn-off time.

Solution

The minimum γ equals the turn-off time in 20 ms period (50 Hz system);

$$\gamma_{min} = t_{off} \times 50 \times 360 = 12.6^o$$

The actual extinction angle in the HVDC converter would be maintained at around 15-18^o to allow for some operating margin. Figure 3.10 shows the γ_{min} fora range of typical turn-off times.

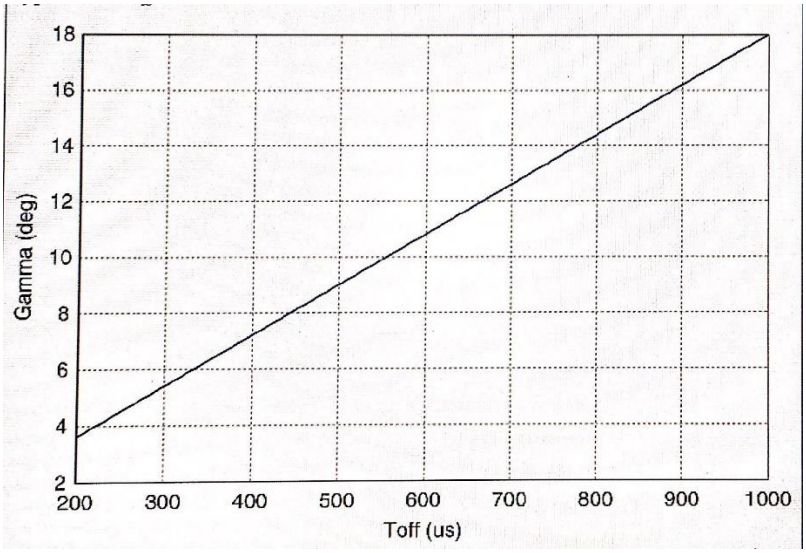

Figure 3.10 *Gamma angle for a range of thyristor turn off Example 3.2.*

4 HVDC Rectifier Station Modelling, Control and Synchronization with AC System

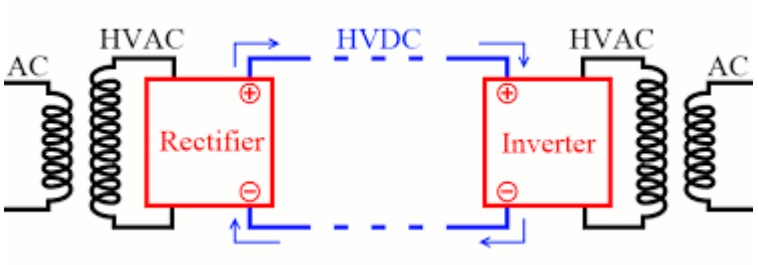

Figure 4.0 *Rectifier in HVDC system.*

4.1 HVDC Rectifier Controller

The principal thyristor converter control equation is given in Eq. (3.15), which demonstrates that DC voltage can be manipulated directly by varying firing angle α. For a multibridge high-voltage direct current (HVDC) rectifier, the DC voltage becomes:

$$V_{dcr} = B\frac{3\sqrt{2}}{\pi}V_{g\_LLr}\cos\alpha_r - B\frac{3}{\pi}\omega L_{tr}I_{dc} \tag{4.1}$$

Where subscript (r) stands for rectifier and *B* represents the number of series-connected six-pulse bridges. Most often B = 2 or 4. It is common practice to connect multiple bridges in series (appropriately phase shifted) in order to reduce harmonic. The DC voltage waveform in Figure 3.2 has six pulses per cycle and therefore the dominant harmonic on the DC side the sixth harmonic. A 12-pulse system can be created if two six-pulse converters with 30^{o} phase shifted transformer secondaries are connected in series. Such a 12-pulse system has a dominant 12th harmonic on the DC side and 11th and 13th on the AC side.

The HVDC system DC current system is expressed using rectifier and inverter voltages as:

$$I_{dc} = \frac{v_{dcr} - v_{dci}}{R_{dc}} \qquad (4.2)$$

Where R_{dc} is the total DC -side resistance and V_{dci} is the inverter-side voltage. The DC current, therefore, can be controlled either by using rectifier or inverter DC voltage but most commonly it is controlled on the rectifier side, as analysed in Chapter 6. Figure 4.1 shows a simplified controller schematic for a rectifier converter. It includes a feedback PI controller for DC current in the inner loop. As DC voltage responds according to the *cosine* function of the firing angle as shown in Eq. (4.1), the system is nonlinear gain a linearization element is introduced in the controller (shown as linearize). This element performs an inverse *cosine* function which is further studied in Chapter 7. The phase-locked loop (PLL) provides information on the AC bus phase angle to the controller, as discussed below. The switch firing provides six pulses, which are 60^{o} spaced (on to each valve), delayed from AC voltage zero crossings by angle α_r.

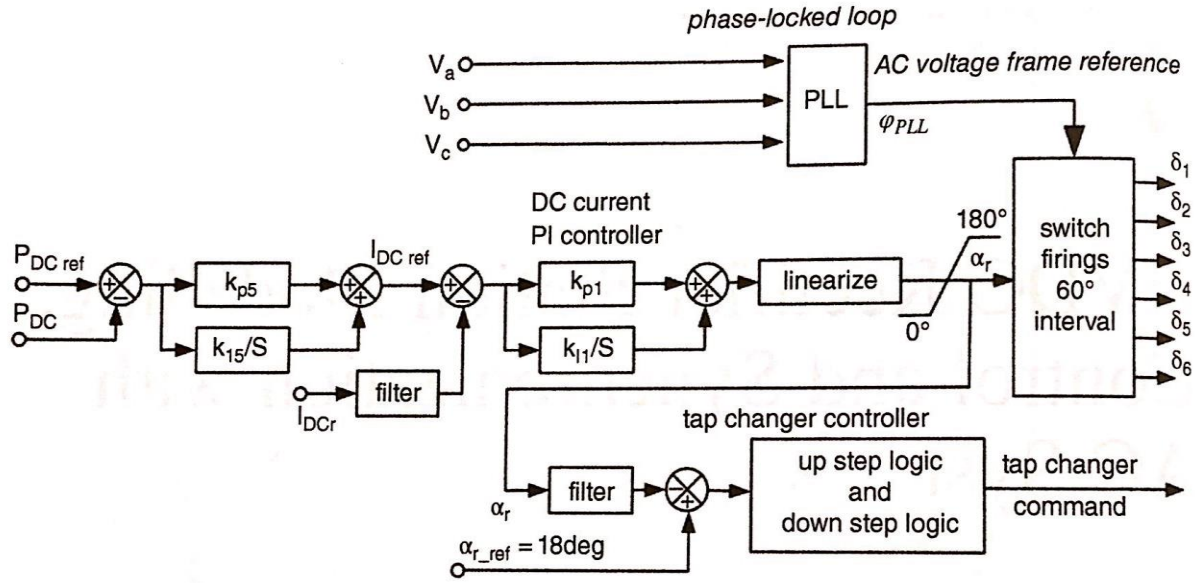

Figure 4.1 *Rectifier controller*

The nominal rectifier operating angle is typically α_r = 150-20^{o}. It is desirable to have a low operating angle to reduce reactive power and harmonics, but a sufficient margin must be allowed to compensate for disturbances to the AC voltage. In some operating conditions, high values for the firing angle will result – for example when DC current is low or when AC voltage is high. A slow acting transformer tap changer is provided in order to optimize valve – side AC voltage. The tap-changer controller will measure the firing angle and make adjustments to the tap-changer position in order to increase or decrease the transformer ratio typically in steps of 1.25% and the total adjustment range is around 40%. This is a very slow-

operating controller (it has a time a constant of the order of minutes), which ensures that converter variables are optimized but is does not react to fast disturbances. A deadband of around 2% is normally used to prevent unwanted up/down hunting and wearing of mechanical components.

4.2 Phase-Locked Loop (PLL)

The main role of a PLL in HVDC system is to give a reference signal for a converter controller, which is synchronized with the AC commutation voltage. As the operation conditions in the AC system change, the zero crossing of AC voltages will move. A thyristor can only be fired when it is forward biased, and in inversion mode it should be fired sufficiently early to allow reverse recovery for a given AC voltage magnitude. Precise information about the AC voltage position is therefore required for converter firing control.

The earliest HVDC system used zero crossing detection on AC voltages for firing synchronization. This synchronization was vulnerable harmonic instabilities. Figure 4.2 shows the transvector PLL, which is commonly used with the latest HVDC. This PLL tracks positive sequence of three-phase AC voltage in order to derive the phase angle reference signal. It includes three segments:

- 3/2 phase transformer ($ABC \rightarrow \alpha\beta$);
- Controller, which ensures tracking;
- Voltage-controlled oscillator (VCO), which converter frequency into a position angle (a resettable integrator generating sawtooth waveform).

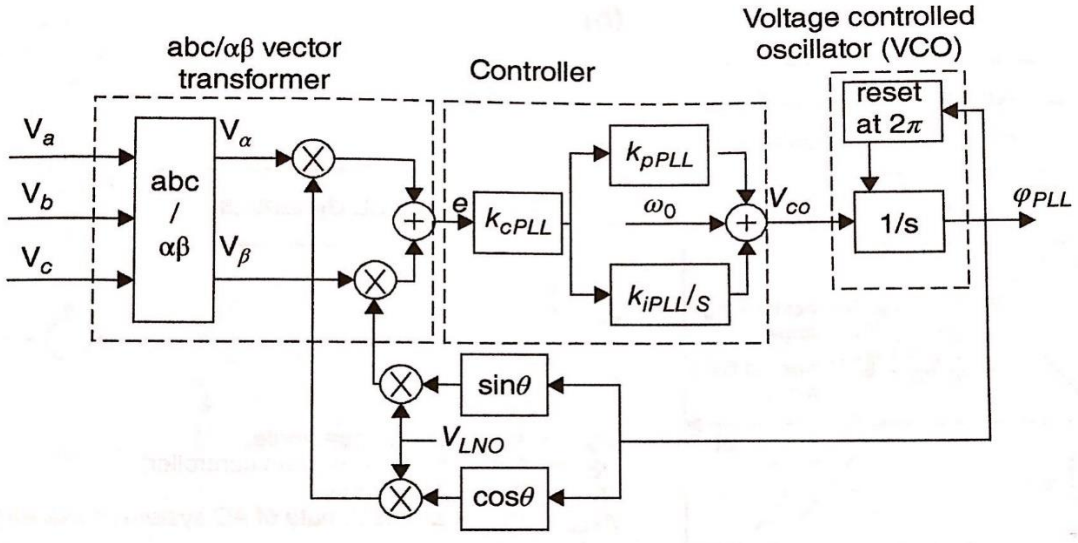

Figure 4.2 *Transvector PLL.*

The input to the PLL is the measured voltage signal from the three-phase AC voltage (V_a, V_b, V_c), as shown in Figure 4.2. The PLL output is a reference sawtooth waveform with frequency and phase angle closely following the AC voltage. If the inner controller in the PLL is turned for fast tracking of the AC system dynamics then the reference signal will be closely following the change in the AC system voltage angle. In this case, the actual firing angle will not deviate from the ordered firing angle. In the opposite

case, with low PLL controller gains, the reference signal will have only slow dynamic changes with very loose tracking of the AC system dynamics.

Figure 4.3 shows how the actual firing depends on the ordered firing angle and the AC system dynamics. The firing angle ordered from the controller is α_c. The solid line shows the AC voltages in the nominal state. When the AC system is perturbed, as shown by the dotted line, the actual position of the voltage crossings will change. In this perturbed state the actual firing angle seen by the converter (α) become different from that ordered from the controller (α_c) because of the change in the reference point. This happen because PLL internal dynamics are not able to track the AC system position instantaneously. A PLL works like a Kalman filter by indirectly adjusting the output to track the input signal position. This indirect tracking provides excellent immunity from noise on the AC voltage signal large PLL gains can improve tracking, but the system becomes more sensitive to harmonics and may lose synchronism during large disturbances. The value ω_o is the expected frequency of the AC system ($2\pi F$).

(a) (b)

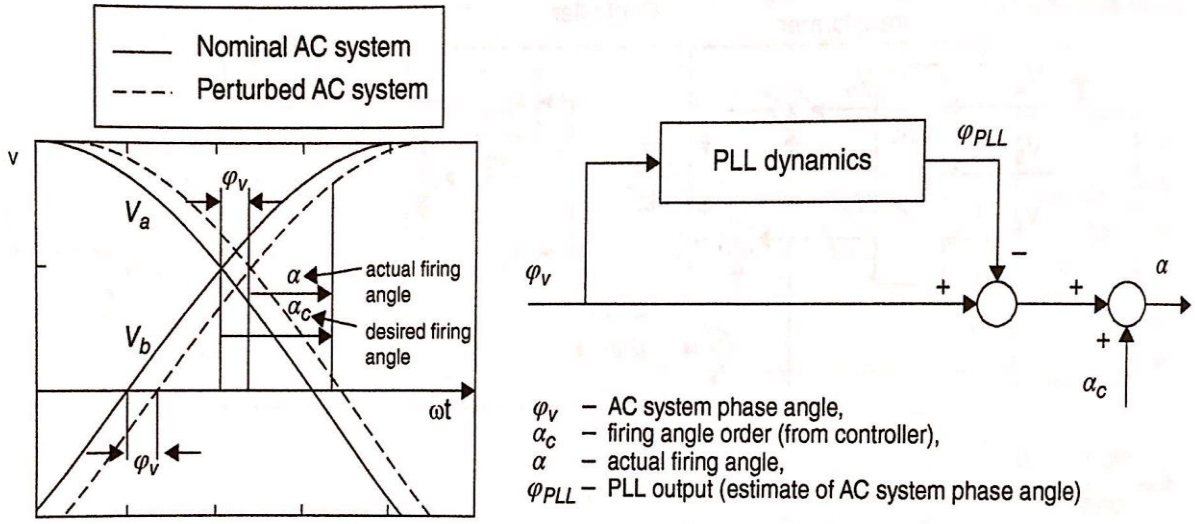

Figure 4.3 *Influence of AC system dynamics on the converter firing angle. (a) Time domain and (b) small model.*

Figure 4.3 b uses small-signal block-diagram representation to depict the role PLL in deriving the actual converter firing angle. The PLL output (ϕ_{PLL}) cancels (with some delay) any changes in AC system position (ϕV).

The α and β components of AC voltages for transvector type PLL in Figure 4.2, are defined as:

$$V_\alpha = \frac{2}{3}Va - \frac{1}{3}Vb - \frac{1}{3}V_c \quad (4.3)$$

$$v_\beta = \frac{1}{\sqrt{3}}(v_b - v_c) \quad (4.4)$$

The control error is defined as:

$$e = V_a V_{sin} + V\beta V_{cos} \quad (4.5)$$

After substituting Eqs (4.3)-(4.4) in Eq. (4.5):

$$e = V^2 \sin(\varphi_{P_{LL}} - \varphi_v) \quad (4.6)$$

It can be seen that the PLL controller will respond to the difference between the actual phase position of the AC system and the PLL output-phase angle. However, the error signal also depends on the AC voltage magnitude V^2 . This is not desirable because, for low AC voltage. The PLL controller gain will be low and it will respond slowly. Some new PLL systems use adaptive gain to compensate for the dependency on AC voltage magnitude.

4.2.1 Master Level HVDC Control

Figure 4.4 shows the topology of master-level controller at the rectifier. This control is at a higher (and slower) level, which gives DC current reference to the primary DC current control shown in Figure 4.1. There are several possible control modes but not all modes are used at each HVDC system:

- Power control is the primary control mode, which is employed in most HVDC system.

- Frequency stabilization may be used to improve stability in a particular bandwidth where known weakly damped oscillatory modes may exist in the AS system. The frequency range may include unwanted machine-machine regional oscillations (0.1-5Hz). This signal is typically limited to ±3-5% of the current order and added to the power controller output. If stabilization is required for an HVDC remote station (inverter) then the controller should compensate for delay incurred by signal transfer. This function is similar to power oscillation damping on generators.

- Frequency control may be possible with HVDC, for example if it operates in isolated mode, in which case power control is disabled. If a line -commutated converter (LCC) HVDC is supporting isolated AC system operation, it is required to provide synchronous condenser or a static VAR compensator (SVC) for reactive power support at the terminal bus. This is rarely used as the normal mode of operation with (LCC) HVDC, but it may be included as an emergency control configuration.

- The power-demand override includes a range of limiters and rate limiters for DC power controller. These limiters are active during start-ups, postfault recoveries and other events.

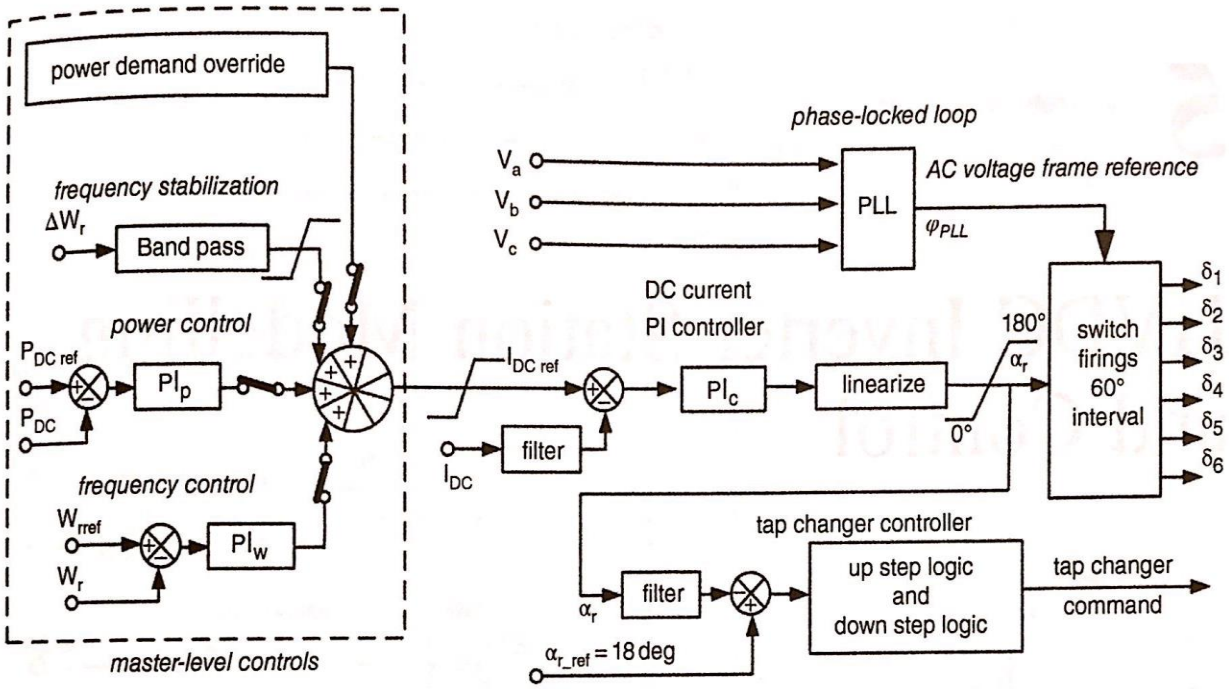

Figure 4.4 *Master-level and low-level HVDC controls at rectifier*

5 HVDC Inverter Station Modelling and Control

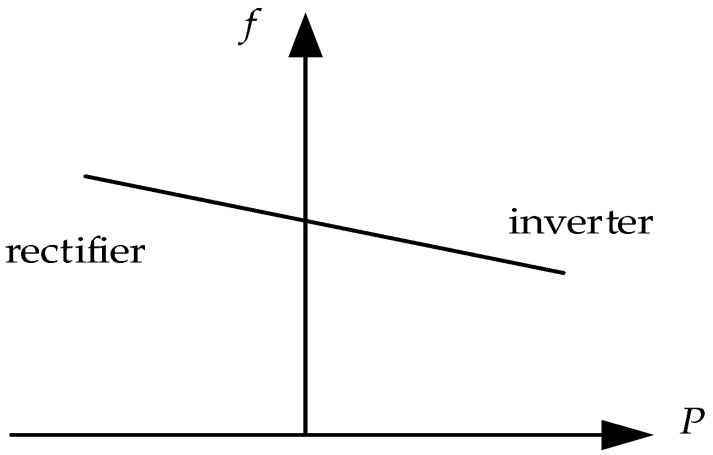

Figure 5.0 *About relation between Inverter and Converter*

5.1 Inverter Control

5.1.1 Control Structure

The basic equation for the inverter terminal is similar to that for the rectifier – see Eq. (4.1):

$$V_{dci} = B\frac{3\sqrt{2}}{\pi}V_{g\_LLi}\cos\beta + B\frac{3}{\pi}\omega L_{ti}I_{dci} \qquad (5.1)$$

Where subscript (i) stand for inverter. Note that sign with the commutation overlap drop is positive (opposite to rectifier), and normally inverter angles β and γ are used. The angle $\propto = 180 - \beta$ is the only control variable whereas several different control goals exist. The primary control aim is to prevent commutation failure as this would cause system collapse. In addition, the goal is to maintain inverter DC voltage close to optimal values and also to ensure system operation case that the rectifier terminal loses control capability. Figure 5.1 shows the basic inverter control – which compete through the ***minimum*** element and the one that gives minimal angle defines the operating mode.

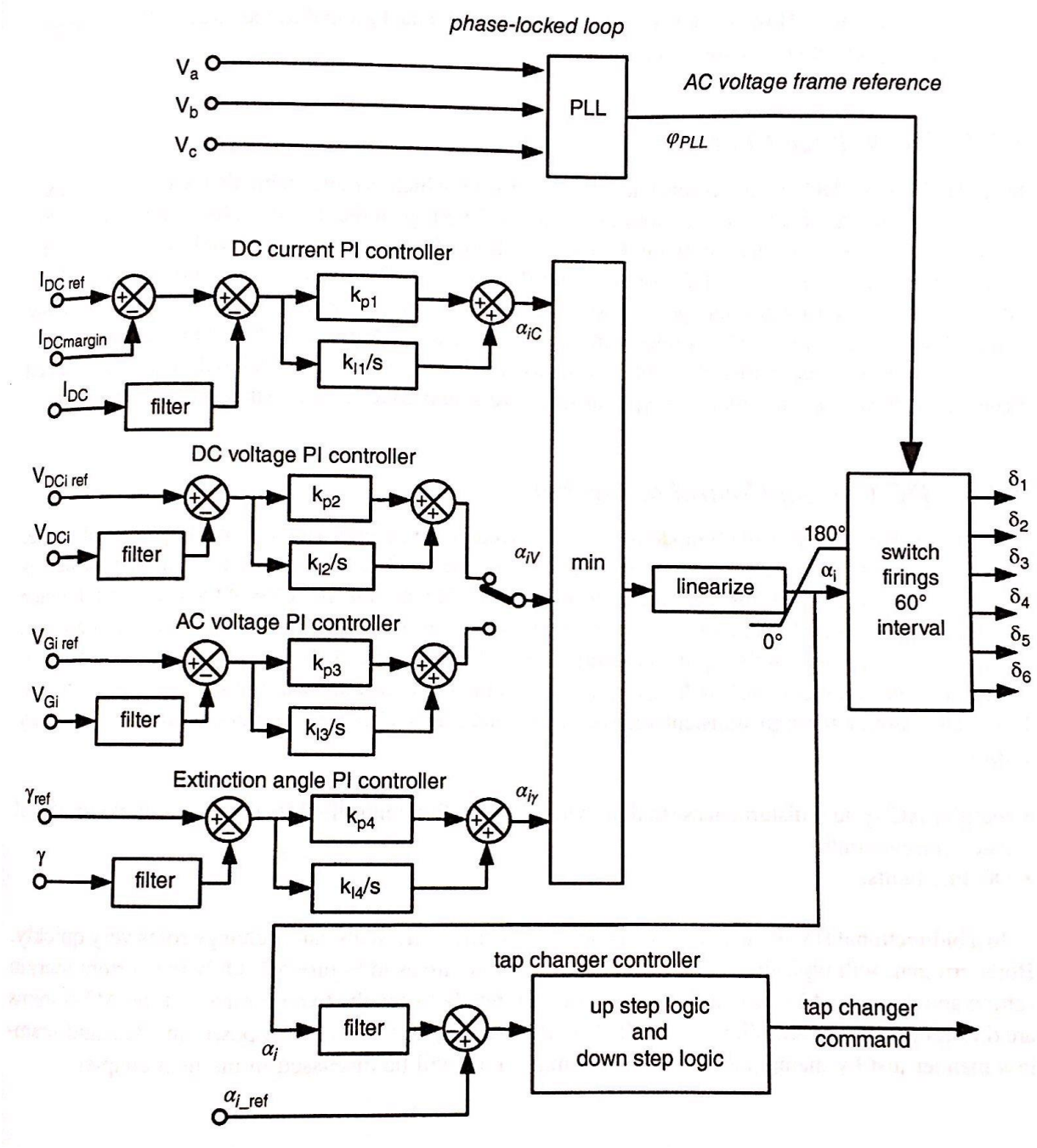

Figure 5.1 *Inverter controller schematic.*

5.1.2 Extinction Angle Control

In the inversion mode, as demonstrated in Figure 3.9, it is important to keep a safe extinction angle, γ, in order to prevent commutation failure. It is also desirable to maintain γas low as possible in order to minimize reactive power consumption, harmonics and losses. The minimum γ required for safe commutation with high-power thyristors is around 10^{o}-15^{o}. Typically, γ harmonics and losses.

The control challenge with inversion mode is that controller can only influence the beginning of thyristor conduction, which is the firing angle β. After thyristor is triggered there is a commutation overlap period (typically 10-30^o) while current reduces in the outgoing thyristor and current increases in the triggered thyristor. Control is not possible during commutation overlap. However, the length of commutation overlap depends on the external conditions like AC voltage and DC current and cannot and be predicted at the firing instant. It is therefore necessary to allow a certain safety margin in the γ reference value.

Gamma minimum control is also called constant extinction angle (CEA) control. This is a default control mode at the inverter. Typically, γ is controlled in a feedback manner as shown in Figure 5.1 and by using thyristor voltage sensors, which rapidly measure the extinction angle for each thyristor. The minimum angle for a six-pulse bridge is passed to the controlled and compared with the reference angle to make adjustments in the firing angle. The CEA control, however, is the least stable control mode for inverter and for this reason CEA control is not used on HVDC systems with weak AC systems or during disturbances. However CEA will always run in the background as the largest allowed angle, $\propto_I$, in order to prevent commutation failure.

5.1.3 DC voltage control

Many HVDCs use DC voltage control at the inverter side, which is more stable than CEA. Typically, a proportional integral (PI) feedback control regulates DC voltage at the desired value. Alternatively, AC voltage control can be used as shown in Figure 5.1, although this is rarely employed. In Figure 5.1 the controller normally operates in DC voltage control but during disturbances it can move to one of the other two modes. During normal operation $\propto_{i\gamma}$ will be only a few degrees larger than $\propto_{iv}$, allowing some margin for the regulation of DC voltage without switching to CEA mode. If, for example, inverter AC voltage depression occur, than the actual extinction angle will reduce and CEA will request advanced firing angle (lower $\propto_{i\gamma}$) in order to keep γ at safe levels, and control will change to CEA mode.

5.1.4 DC current control at Inverter

current controller (CC) mode is also employed at the inverter side as a backup control mode, which is not active during normal operation. The inverter CC receives current reference, which is reduced by the current margin. The current margin is typically around 10-15% of the rectifier reference current. During normal operation, the inverter CC will be in saturation, demanding firing angle $\propto_{ic}$, which is much larger than the $\propto_{iv}$ demanded by DC voltage controller. However, during disturbances, the DC current can reduce below I_{DCref} -$I_{DCmargin}$ and the CC controller will reduce $\propto_{ic}$ in order to stabilize DC current through transient recovery. The inverter CC control is beneficial and necessary during:

- Rectifier AC system disturbance (fault), when the rectifier controller hits minimum angle limit and loses current control;
- DC line fault.

In a bidirectional HVDC system, the inverter and rectifier terminals can exchange roles very quickly. Both terminals will typically have the same control structure as in Figure 5.1. Only the current margin setting and the sign of DC voltage reference are different between the two terminals. If the AC system are different then the controller gain will also differ. The system can reverse power in a fast and seamless manner just by manipulating the current margin, as will be discussed in the next chapter.

5.2 Commutation Failure

In a normal inverter operation, it is necessary that each valve receives reverse blocking voltage for a safe turnoff time (extinction angle) and after the commutation overlap is completed, in order for the thyristor to regain forward blocking capability. This may not happen if, for example, commutation overlap is longer than normal or does not complete before the next forward voltage. IN such case the thyristor will not gain a blocking state and it will continue to conduct for the full next cycle. This is an unwanted operating condition because the thyristor on the opposite pole on same converter leg will be fired in the next 120^{o} and this will create a short circuit across the DC voltage.

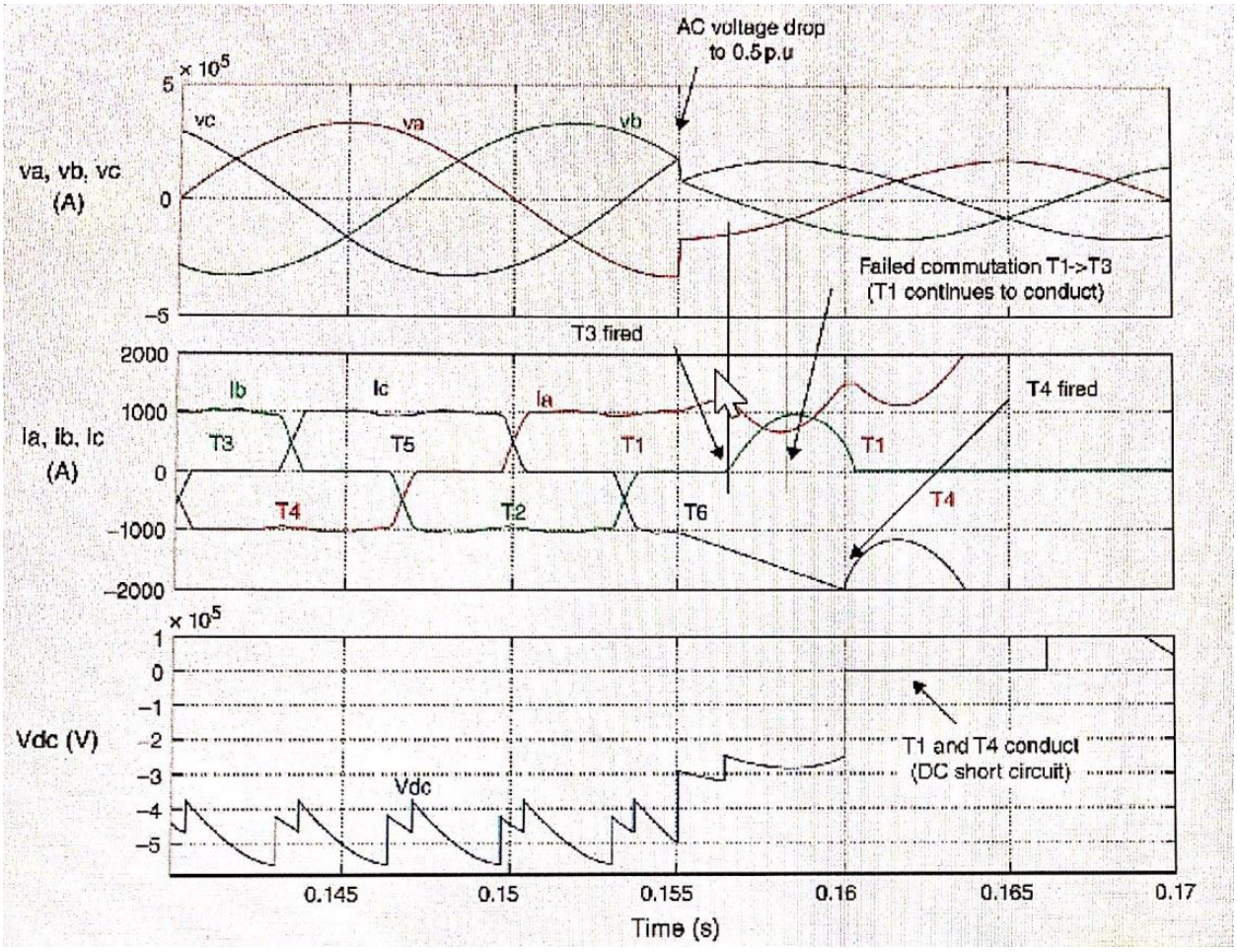

Figure 5.2 *Inverter commutation failure simulation*

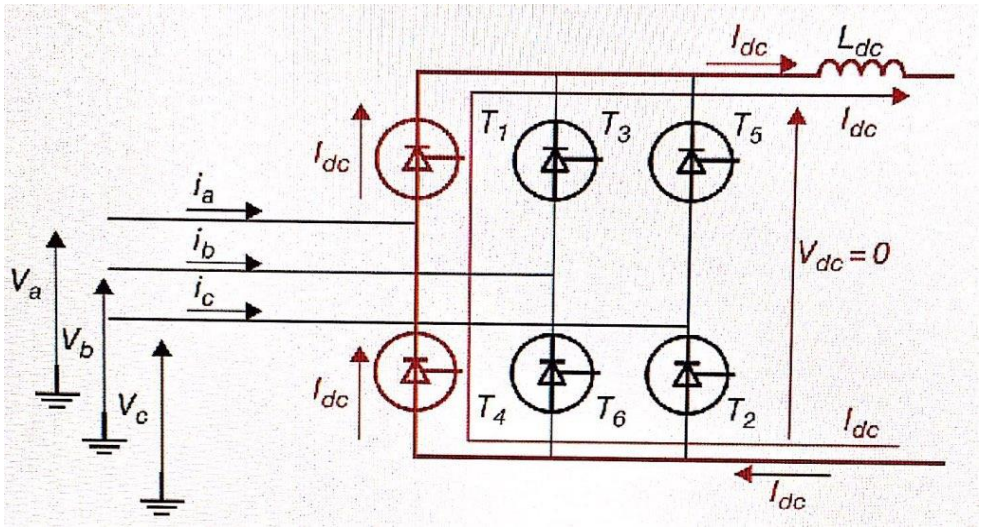

Figure 5.3 *DC current path after commutation failure*

Commutation failure and DC short circuit are not destructive for HVDC; the system will recover in few cycles assuming that the AC voltage has recovered. The commutation failure is a localized DC phenomenon where DC voltage collapses and DC current increases, but it is limited by smoothing inductors. The commutation failure does not cause a direct disturbance on the AC side: there is no high AC current or AC voltage drop (the AC side will not see a fault). The main problem with commutation failure is that the power flow to the inverter AC system is interrupted and, if the AC system is weak, this can cause a significant disturbance. Furthermore, the recovery process after a commutation failure implies large transient inverter firing angles, which draw significant reactive power from the AC system while the active power injection is reduced. These conditions make AC system recovery more difficult.

The commutation failure is primarily caused by the increased commutation overlap (μ). The commutation overlap is defined by Eq. (3.26), and this enables establishing two main conditions for the commutation failure:

- Inverter AC voltage drop;
- DC current increase.

The CEA controller is capable of adjusting operation angle $\propto_I$ to avoid commutation failure for any steady-state operating conditions (like gradual reduction in inverter AC voltage). However, it is not possible to completely eliminate commutation failure in case of sudden AC voltage drops. The problem arises because it is possible to control only the beginning of commutation overlap but once a thyristor is fired the conduction is solely determined by the circuit conditions. Increasing the reference extinction angle can only reduce the probability of commutation failure.

Commutation failure is commonly studied using statistical methods and it is expressed as a probability, which depends on the percentage voltage drop on the inverter AC system. Typically, a sudden AC voltage drop of 5-15% will cause commutation failure. Single-phase faults are as onerous as three-phase faults as far s commutation failure onset is connected. AC system with larger impedance are more vulnerable to commutation failure because AC voltage swing more when the load changes.

6 HVDC system V-I Diagrams and operating Modes

6.1 HVDC -Equivalent Circuit

The equivalent circuit of The DC side of a HVDC system is shown in Figure 6.1. There are two equivalent controllable DC sources, which represent the two converters. If the inverter is operated in a constant extinction angle, the inverter equivalent resistance becomes negative as shown in Figure 6.1b.

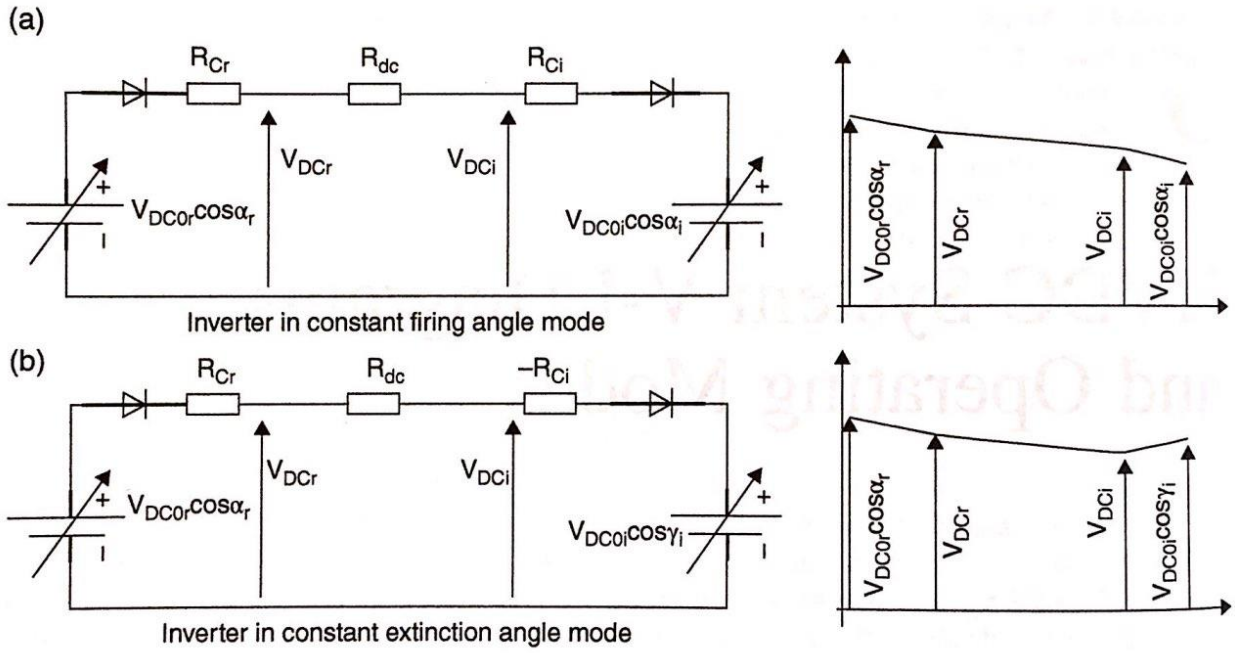

Figure 6.1 *HVDC system equivalent electrical circuit.*

The DC current is proportional to the difference between rectifier and inverter DC voltages, as shown in Eq. (4.2). Analysing this equation, DC current can be controlled either using a rectifier or an inverter controls DC voltage as this method results in the optimal HVDC design. Some HVDC systems with extremely weak inverters operate with DC current control at the inverter side.

6.2 HVDC V-I Operating Diagram

Figure 6.2 shows the HVDC system static operating point as the intersection of the rectifier and the inverter V-I operating curves. The rectifier is typically in the constant current mode and the curve is a vertical line in the HVDC V-I diagram. Three different curves are shown for the inverter, representing three common modes.

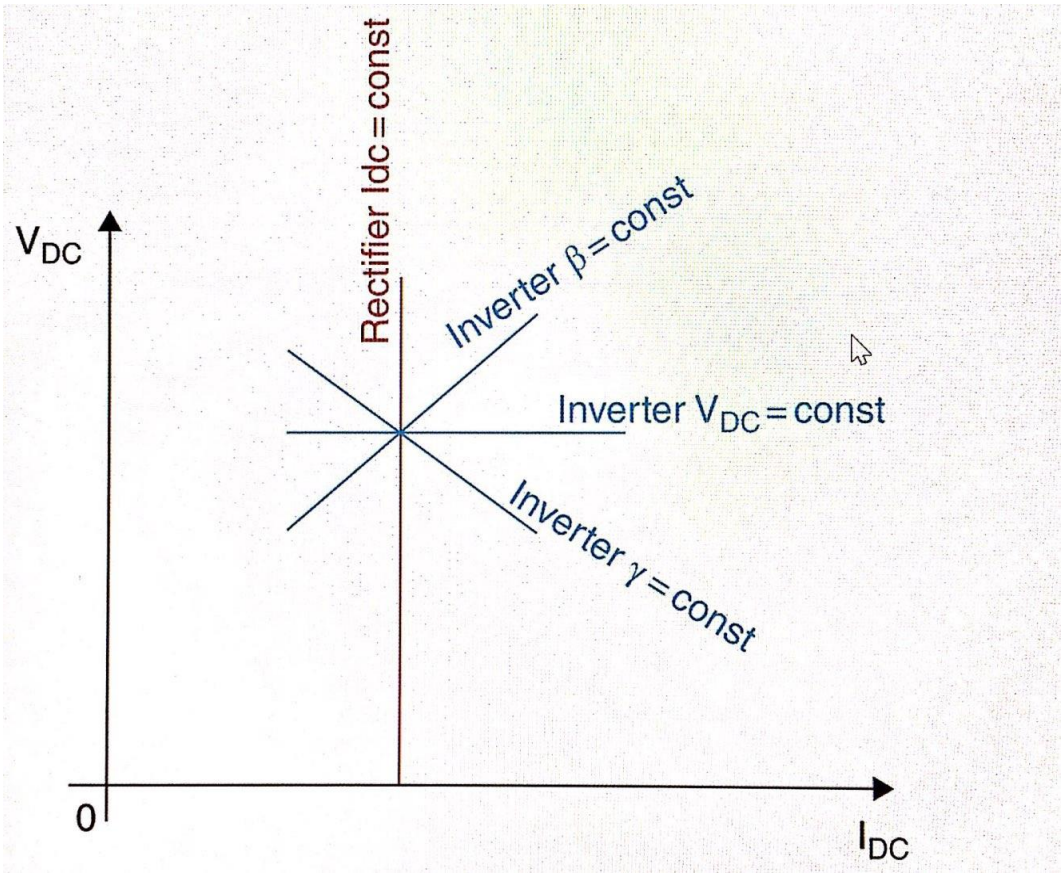

Figure 6.2 HVDC *operating point as intersection between rectifier and inverter curves.*

The inverter curve β_I = *const* provides a good, natural stabilizing response. Assuming that DC current is perturbed so that increases, The HVDC operating point would move along β_I = *const* curve and therefore the inverter DC voltage increases. This increase in the inverter DC voltage implies a DC current reduction from Eq. (4.2), thus counteracting (stabilizing) the original disturbance.

Figure 6.3 shows a more detailed V-I operating diagram for an HVDC system. The rectifier in constant control of the current, but the rectifier voltage can only be increased until the firing angle reaches the minimum limit. Typically, a small margin of $\propto_{min} = 2^o$ is provided to prevent the thyristor triggering while it is reverse biased. The inverter in this diagram includes three modes. In normal operation, DC voltage control is employed, which is a horizontal curve and establishes a stable operating point with rectifier constant current control.

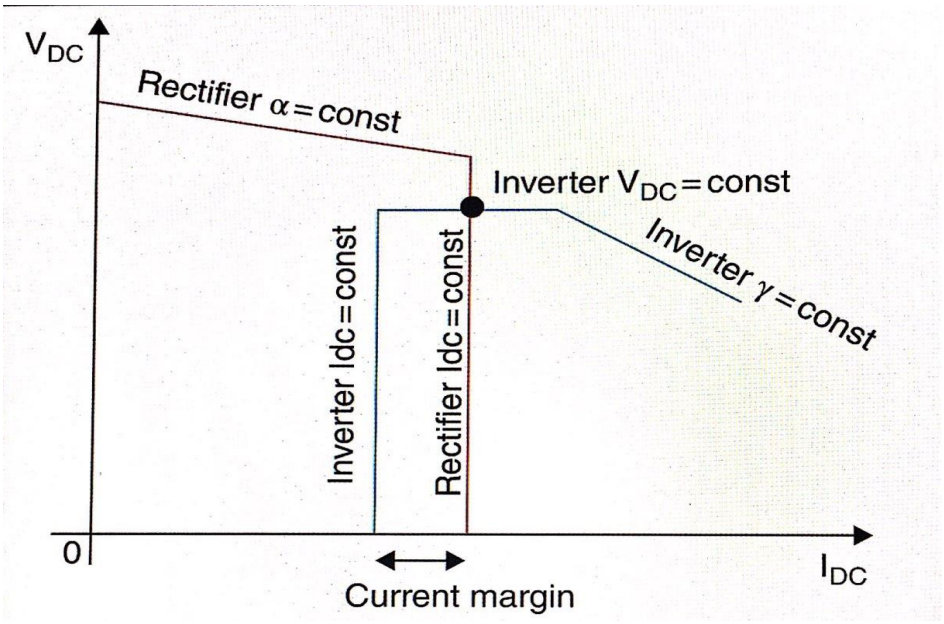

Figure 6.3 *HVDC full V-I operating diagram (inverter in V_{dc} control mode).*

Figure 6.4 shows the operating point when the rectifier AC reduces. If the rectifier AC voltage reduces sufficiently, the rectifier will operate along an $\propto = const = 2^o$ curve and the intersection with the inverter curve may not be defined. For this reason, the inverter also has a constant current mode but the reference current is reduced by the current margin.

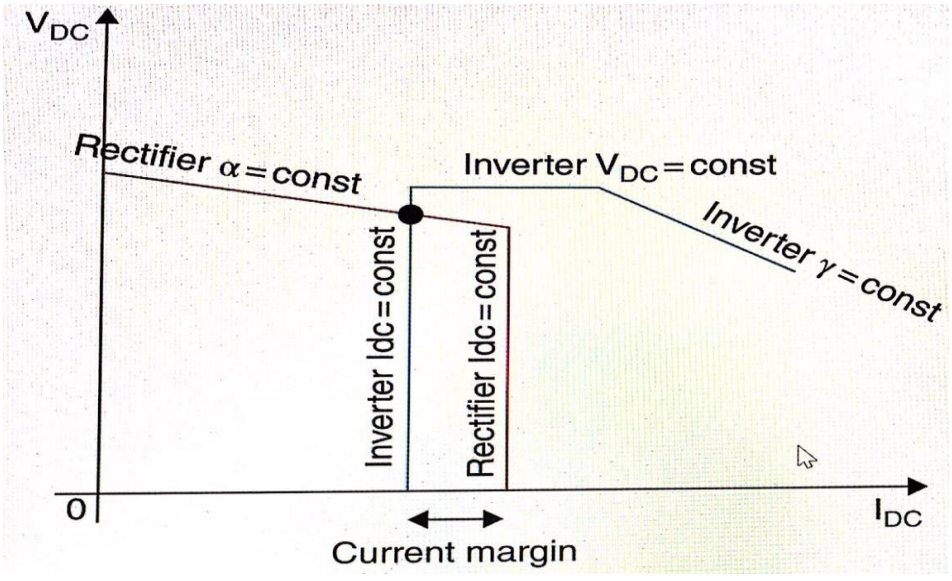

Figure 6.4 *HVDC operating point for reduced rectifier AC voltage (inverter in CC mode)*

If the inverter AC voltage reduces, the inverter controller moves to constant extinction angle mode in order to prevent commutation failure, as shown in Figure 6.5. This operating mode ensures that the minimum extinction angle is preserved under all external circuit conditions.

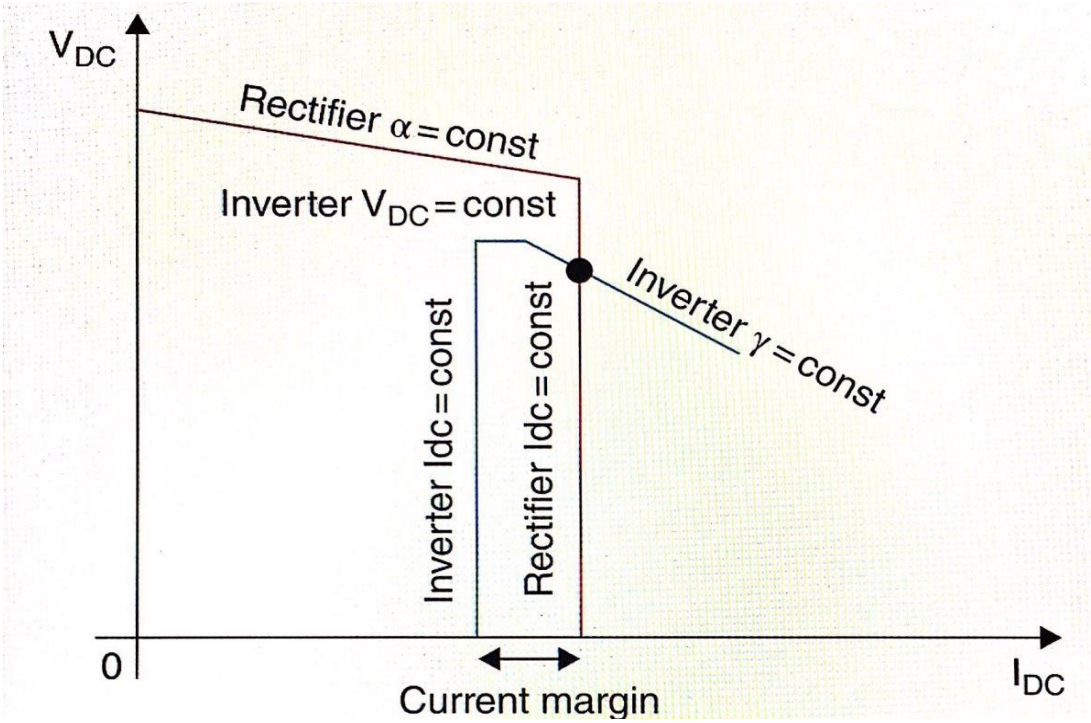

Figure 6.5 *HVDC operating point for reduced inverter AC voltage (inverter in constant extinction angle (CEA) mode).*

6.3 HVDC Power Reversal

The control topology at the two HVDC terminals is identical because the rectifier and inverter roles are interchange. There are two differences.

- The terminal that receives the current margin operates as an inverter;
- The sign of the DC voltage reference is different (but stays unchanged) at the two terminals.

Figure 6.6 shows the HVDC test system, which is used in all further simulations. This is a 500 MW monopolar bidirectional HVDC with a typical medium length (100-300km) DC cable parameters.

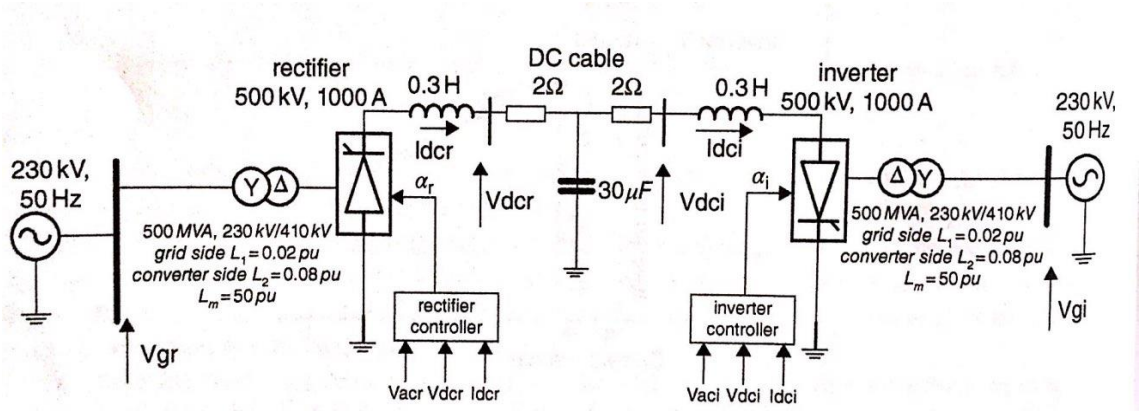

Figure 6.6 *HVDC test system.*

Figure 6.7 illustrates power reversal on the test HVDC system. The top three graphs show rectifier variables and the lower three graphs show inverter (the roles are interchanged at 1.9 s). At 1.1s, the power reversal process is initiated by sending the current margin to the rectifier and removing the current margin from the inverter controller. At the rectifier side, the DC current reference drops by 0.1 pu while at inverter controller the DC current reference increases by 0.1 pu. The rectifier controller now experiences too high current and keeps increasing the firing angle in an attempt to bring the current to the reference level. Simultaneously, the inverter controller experience too low current and keeps reducing the firing angles, trying to increase the to the reference level. During this process the rectifier firing angle increases to over 90^o and it starts inverting while the inverter, s firing angle reduces to below 90^o and it moves into rectification. The second graph shows that the DC voltage polarity reverse at both sides. The slope of the curves is identical in this case as the two controllers have the same proportional integral (PI) gains.

The third graph shows the three controller firing angles, which are competing in the *minimum* element. The rectifier current controller cannot lower the current to a new setting and it will saturate as the voltage controller takes over control at 1.9 s. As seen in the third graph, for inverter variables, the inverter current controller takes over from the DC voltage controller as soon as the current margin is removed. It is noted that the DC current stays approximately constant during the reversal process. IN modern HVDC systems, the power-reversal process can be shorter than in Figure 6.7, and possibly within 0.2 s. In some systems the speed of power reversal will be limited, considering limitations on other equipment like cables and filters and limitations on the AC system ramp rates.

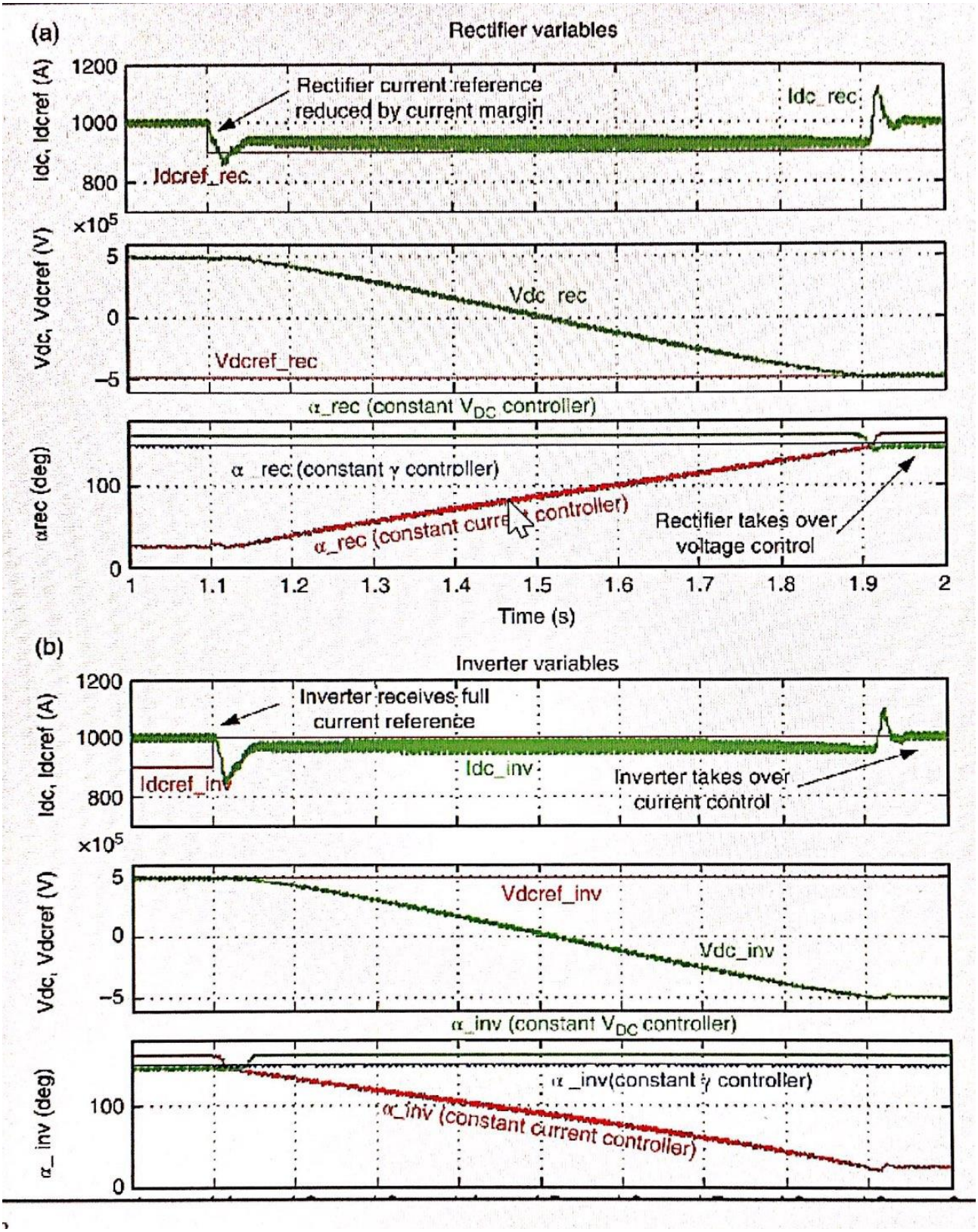

Figure 6.7 *HVDC power reversal process. At 1.1 s current margin is removed from the inverter and sent to the rectifier. Power reversal is completed 1.95 s.*

Figure 6.8 shows the full V-I diagram including the positive and negative power direction. The diagram is symmetrical around the abscissa axis and illustrates the interchangeable roles of rectifier and inverter.

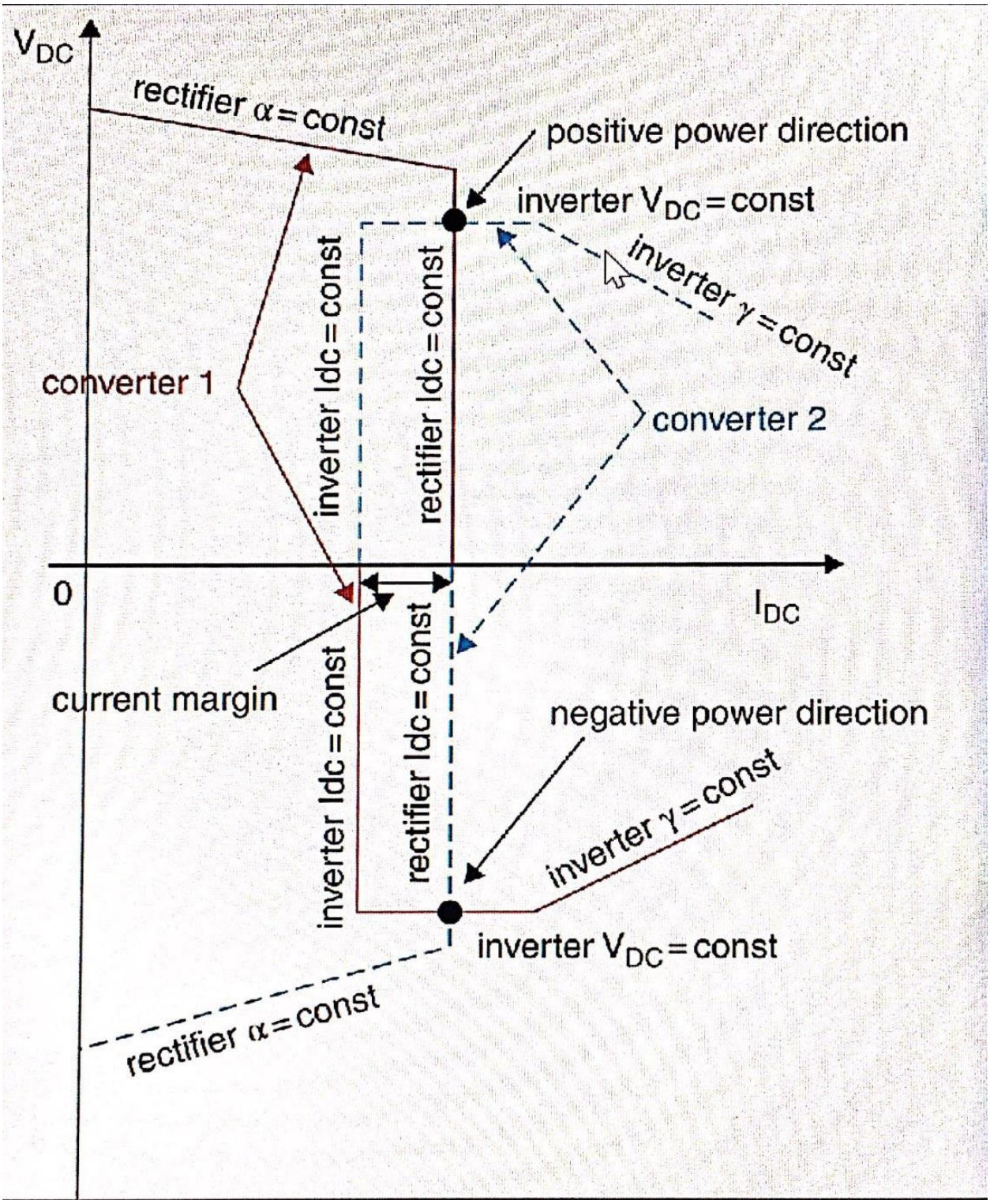

Figure 6.8 *HVDC V-I diagram with positive and negative power direction.*

7 Fault Management and HVDC System Protection

7.1 Introduction

With thyristor HVDC system, the HVDC controls are generally capable of resolving most transient fault situations in a very short time. On a longer time, scale (over 50 ms), if the fault situation persists, various mechanical circuit breakers (CBs) will react. A number of mechanical CBs are associated with an HVDC system, but they are used only as a final means of protection – that is, when HVDC controls cannot solve disturbance and permanent isolation is required. The tripping of CBs implies loss of capacity.

Figure 7.1 shows some typical fault locations and the means of protection. The HVDC controls always react to a disturbance first. A tap changer may also react when a modest AC voltage deviation persists for a long time (remote AC fault or tripping).

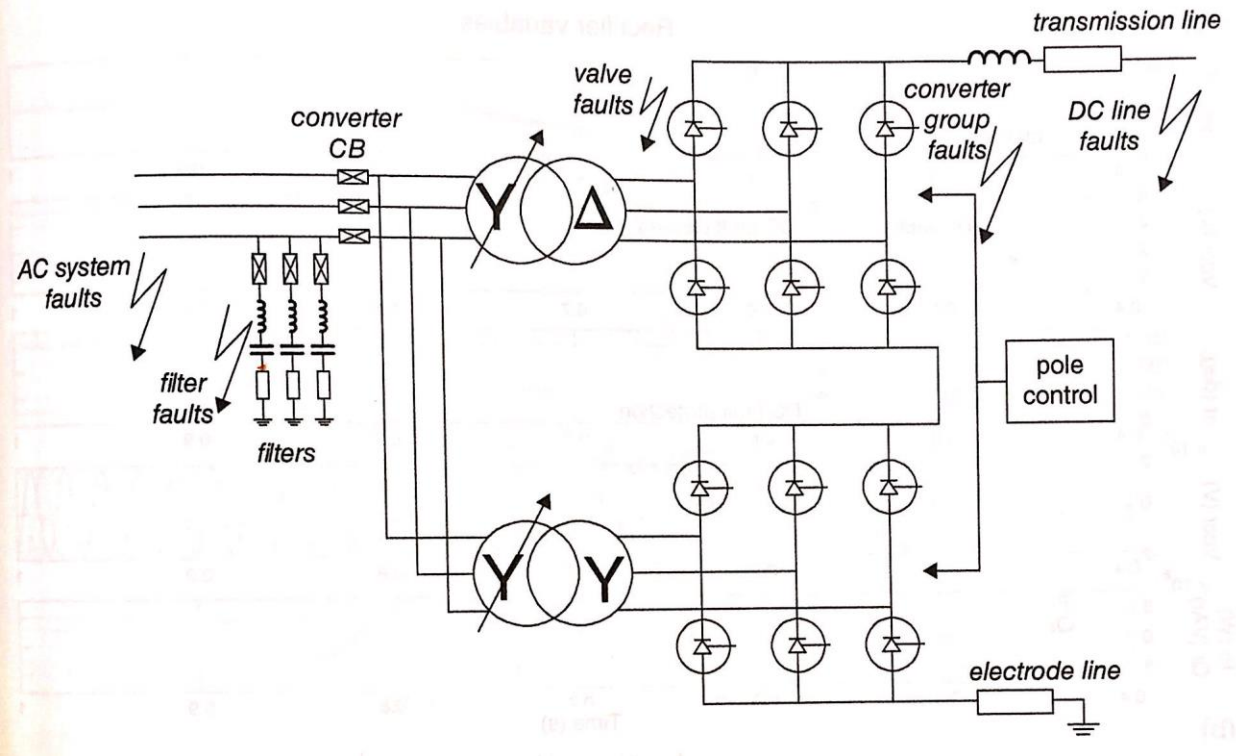

Figure 7.1 *Fault Location and protective means with HVDC system*

7.2 DC line Fault

Line – commutated HVDC is capable of rapidly controlling voltage in positive or negative region and it can therefore react to DC fault according to fault-control strategy. The fault-control strategy includes Limiting the DC current magnitude and changing DC voltage polarity in order to extinguish the DC current.

Figure 7.2 shows system variables (rectifier and inverter) for a DC fault, at 0.45s using the same 500 MW HVDC test system as in chapter 6. The fault is cleared by special HVDC controls. Firstly, the normal HVDC control response is studied before 0.57 s in order to analyse shortcoming in dealing with DC faults:

- ✓ The rectifier regulates the DC current at reference value (I_{dcref_ref} = 1pu). Which continuously feeds the fault. This requires substantial reduction of rectifier DC voltage and therefore the rectifier firing angle $\propto_r$ is just below 90^o. Reactive power demand is excessive (600 MVAr) because of operating conditions with rated DC current and a very large firing angle.
- ✓ The inverter current reduces below inverter reference value ($I_{dcref\_\ inv} = d_{dcref\_ref} - I_{margin}$) and the inverter moves to current control mode by reducing inverter firing angle $\propto_{1.}$ However, in order to keep the same DC current polarity, the inverter DC voltage polarity change and the inverter firing angle settles to just below 90^o. The inverter station now also operates a rectifier and feeds the DC fault. Inverter reactive power demand is over 500 MVAr.

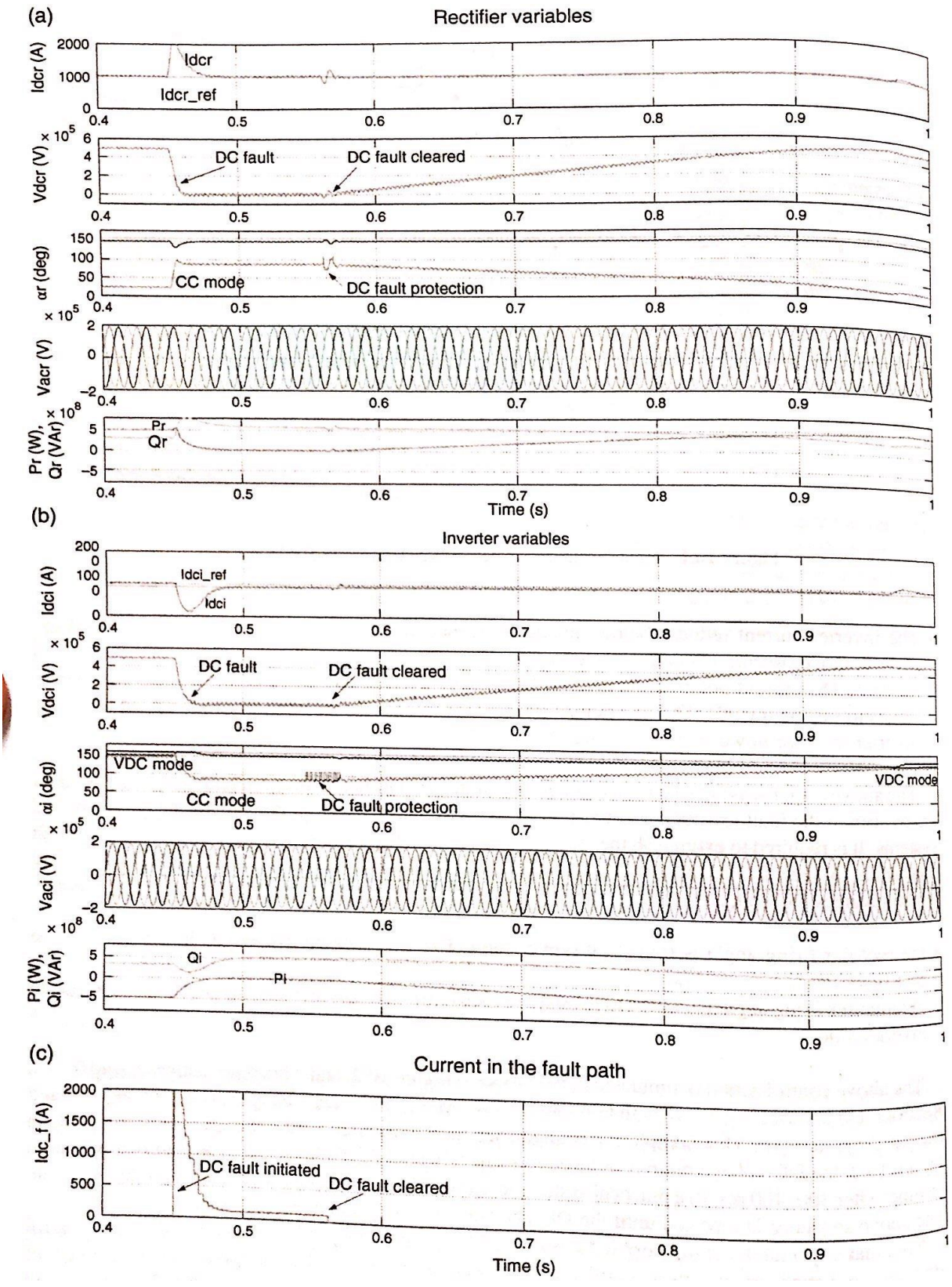

Figure 7.2 *HVDC system response to a DC fault at 0.45 s. Fault is cleared by HVDC controls.*

The above response is not suitable as a long-term strategy to DC faults since converters still feed DC fault arc as seen in the fault resistor current response. Excessive reactive power demand may also disturb AC system. It is required to extinguish the fault current (to break the arc) by discharging line energy through converters. A special DC fault-protection control strategy is therefore initiated on detection of DC faults which changes DC voltage profile as shown in Figure 7.3. This special control strategy is as follows:

- The rectifier firing angle is forced into inversion (110-120^{o}), which discharge line energy on the rectifier side;
- The inverter firing angle is limited to inversion mode (110-120^{0}), which discharge line energy on the inverter side.

The above control action is simulated in the model in figure 7.2, and it becomes active around 0.57 s. Rectifier and inverter Rectifier and inverter angles are both temporarily advanced to 110^{o}, DC voltage is reversed and the fault current drops to zero. This completely extinguishes the fault current and naturally clears the fault. In Figure 7.3, the DC voltage ramp is initiated immediately after the fault is cleared and normal operation resumes after 300-400ms. In a practical system, restart would be attempted after a delay for deionization. The above sequence is repeated until the DC voltage is recovered to nominal values.

Note that a special discriminatory logic is needed for the detection of DC faults, as the above control strategy is not appropriate in the case of commutation failures (which also bring DC voltage to zero). In DC system with overhead lines, most DC faults will be transient, and they are cleaned with fast DC control action. However, with cable systems, DC faults are usually permanent and slightly different fault management is used. A special DC fault protection control strategy is initiated on detection of DC faults, which changes the DC voltage profile as shown in figure 7.3.

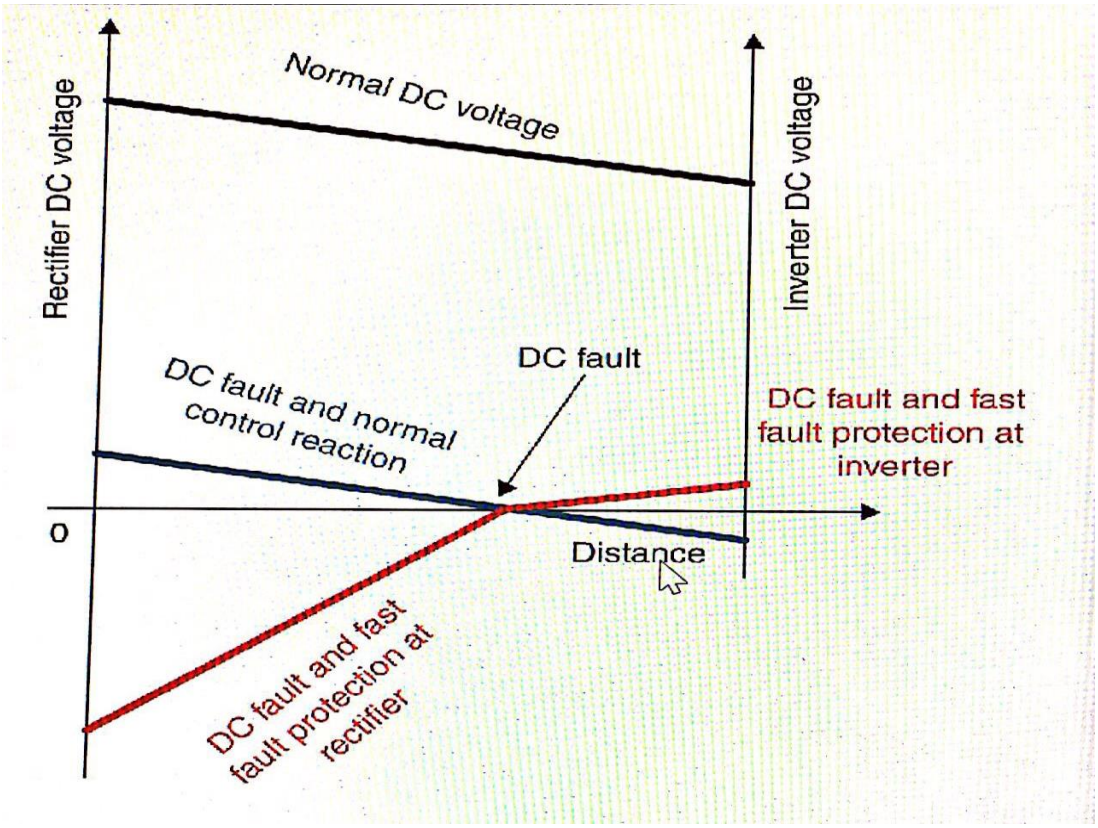

Figure 7.3 *Steady-state DC voltage profile for DC faults effect of DC fault protection*

7.3 AC System Faults

7.3.1 Rectifier AC Faults

AC voltage depression on the rectifier side will result in DC current reduction. The rectifier controller can counteract small AC voltage depression (a few per cent) by reducing the firing angle the minimum angle limit is reached ($\propto_r = 2^o$). In case of further rectifier AC voltage depression, the DC current will be reduced, and the inverter will finally move to constant current mode by reducing inverter DC voltage. The HVDC system will now operate at a DC current equal to $I_{dcref\_r} - I_{margin}$, which is typically 85-90% of the rated current.

However, if the rectifier AC (and consequently DC) voltage is particularly low it would be inappropriate to operate at 90% of DC current because firing angles are large and reactive power demand become excessive. The experience with weak AC system has shown very different recoveries when converters demand large reactive power. For this reason, a special voltage-dependent current order limiter (VDCOL) is introduced as shown in Figure 7.4. The VDCOL shape and the whole V-I curves are different for different manufacturers and they are also optimized for particular HVDC installations. The main purpose of VDCOL is to reduce current order for lower DC voltages.

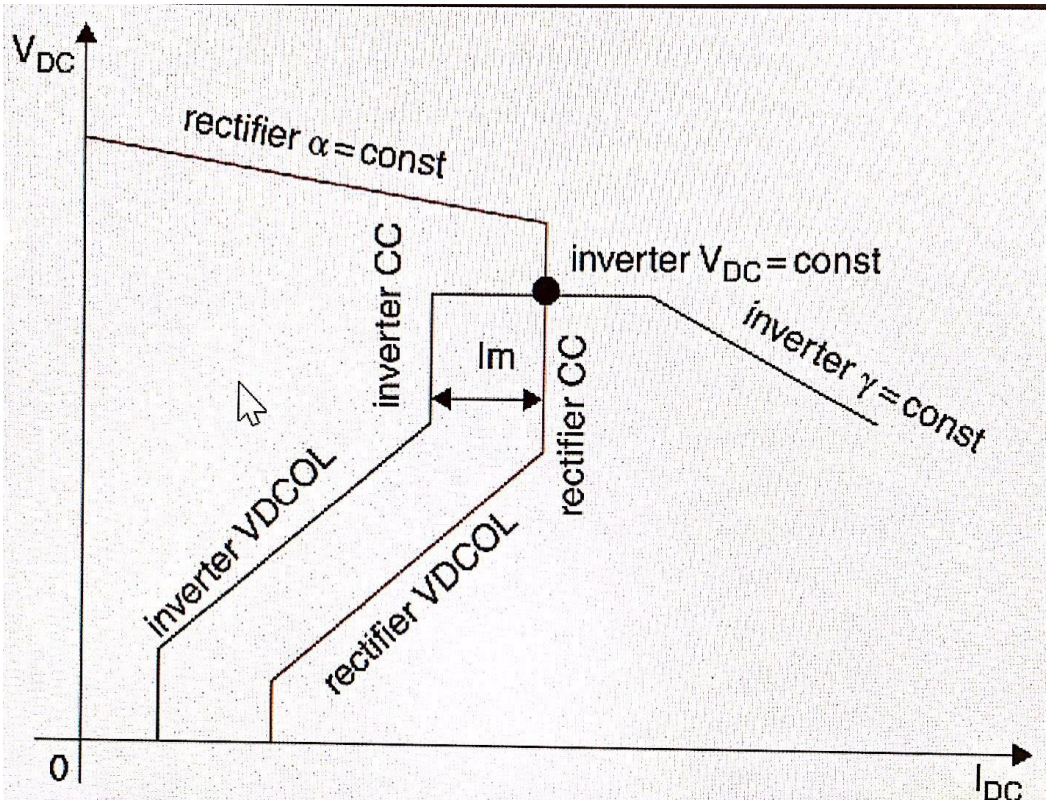

Figure 7.4 *HVDC V-I diagram with VDCOL.*

7.3.2 Inverter AC Faults

Inverter AC system faults will always result in commutation, except for very small voltage disturbances (a small percentage). A commutation failure is a DC short circuit and result in temporary loss of HVDC power transfer. However, commutation failure will not be seen as a short circuit on the AC side. Following the detection of commutation failure, the HVDC controls will increase inverter gamma (gamma kick) and initiate gradual power ramp climbing up the V-I curve, using also the VDCOL slope, until normal operating point is reached to nominal values following successful recovery. In some cases, repeated commutation failure is encountered and recovery attempt are repeated with progressively lower recovery slopes. Figure 10.5 shows a typical commutation failure recovery process, which can be completed in 200-500ms. DC voltage drops to zero, which is sure sign of commutation failure. On detecting low extinction angle, inverter moves to CEA mode which establishes normal commutation and power is slowly ramped.

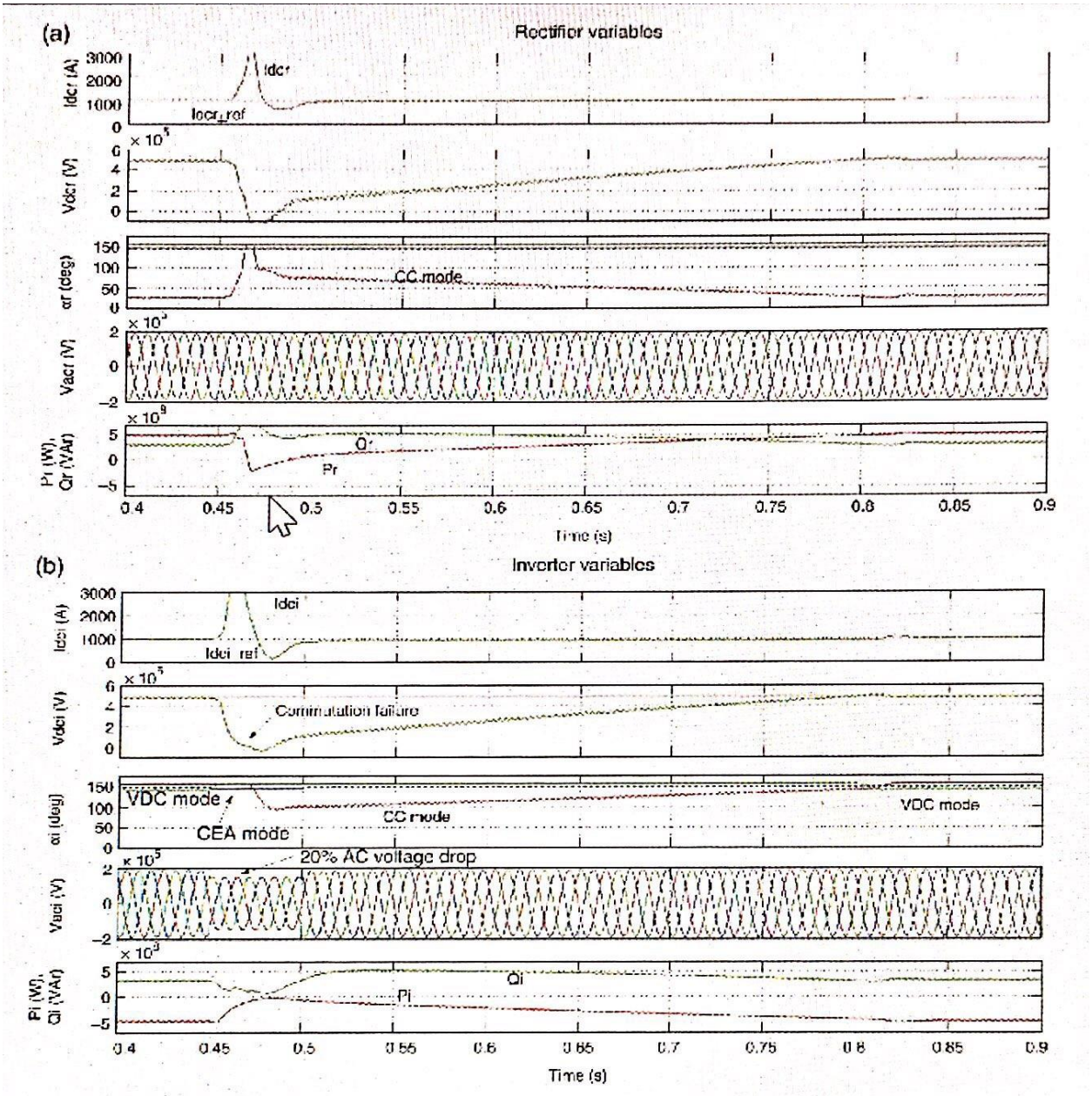

Figure 7.5 *HVDC commutation failure recovery (after 20% AC voltage drop for 50ms at 0.4s).*

7.4 Internal Faults

The internal faults include thyristor faults, valve faults, bridge faults and a range of other faults inside the valve hall, which in turn can be caused by many factors.

Each valve consists of many individual thyristors connected in series and fired simultaneously. There are several redundant thyristors in each valve, and a valve will operate normally in case of a thyristor failure (a thyristor always fails in a short circuit). The voltage stress on the remaining thyristors will marginally increase but the failed thyristors will be replaced at the next scheduled maintenance.

The most severe internal fault is the valve fault, which can occur as a flashover between valve external connections. Such a fault will bring extreme current and voltage stress across the other valves. The protection response is bypass and converter tripping, but the components must be designed to withstand fault conditions for the protection operating time. The bypass involves two steps: firstly, two valves on the same converter leg are fired to provide fast redirection of fault current (extinguish fault arc) and to prevent negative DC voltage. In the second stage, if the fault is not cleared, the mechanical bypass switch (BPS) is closed to provide a permanent DC current path.

In should be recalled here that with current source systems, like the line-commutated converter (LCC) HVDC, there is a large inductance on the DC side, which prevents fast current change. Inductors also store energy, and, in case of disturbances, a current path must be provided to ensure discharge of inductor energy. For these reasons, the fast converter bypass is normally the first protection step, which is achieved by firing simultaneously two valves on the same converter leg.

7.5 System Reconfiguration for Permanent Faults

The HVDC controls and the temporary overrating of switches are adequately designed to deal with all transient faults. If the fault condition persists for a longer time, then isolation or reconfiguration is required. As shown in figure 7.1 and 7.6, each HVDC pole can be isolated using pole CBs and filter CBs.

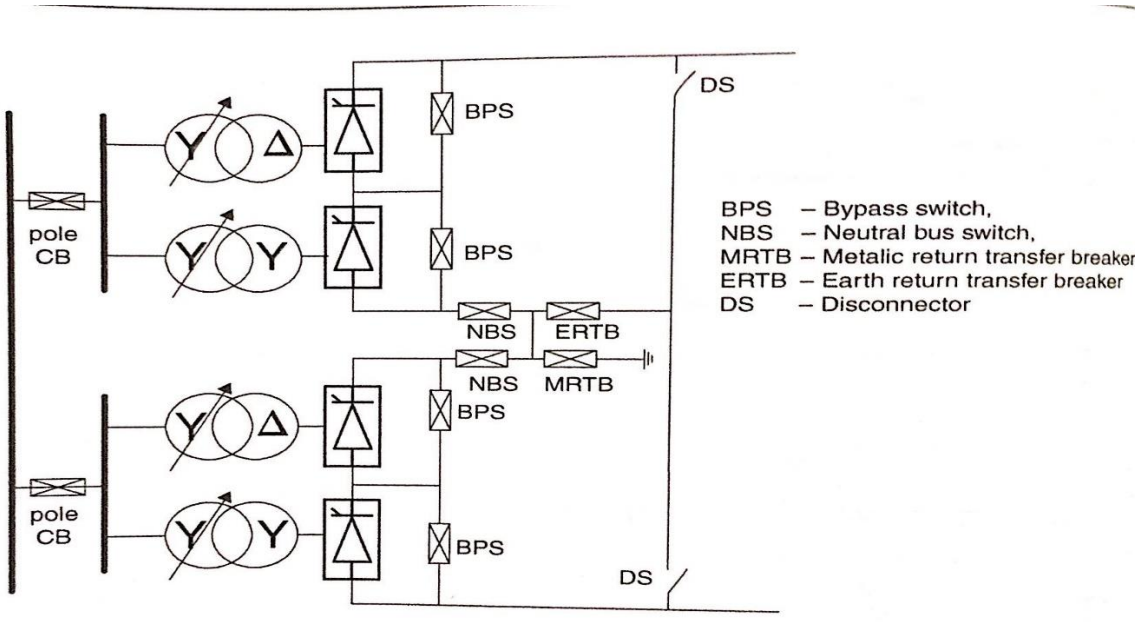

Figure 7.6 *Arrangement of DC breakers for system protection and reconfiguration.*

Figure 7.6 shows the arrangement of DC CBs, but not all of these breakers will be required on all HVDC Links. The DC CBs employed for reconfiguration of a bipole HVDC have very low current rating (not fault levels) and have similar construction to AC CB (common SF_6 AC CBs suffice in many cases). Figure7.7 shows some practical DC circuit breakers. The DC CB technology will come in future.

Figure 7.7 *DC circuit breaker (GL 317 / GL 317X- Live tank circuit breaker up to 550 KV)*

The function of DC CBs is explained below:

- The bypass switch (BPS) is located across a bridge or pole and it open normal operation. In the event of valve or bridge faults it is required to trip the affected bridge and to provide a bypass path for the current. The fast bypass is achieved, firstly, by firing two thyristors on the same converter leg, and this is followed by a permanent bypass using a mechanical BPS, after which the converter is tripped. If the BPS is installed at bridge level, it is possible to operate pole on a single bridge, at half the pole voltage, in order to minimize the loss of power. The BPS enables the converter to be taken in and out of service without power interruption.

- Neutral bus switches (NBSs) are closed and carry rated current in normal operation. In the event of pole faults the current may still flow through a faulted-pole NBS this current path has lower resistance than the electrode path. In such an event, protection will trip NBS to redirect current to the electrode through a metallic return transfer breaker (MRTB). This enable the isolation of the faulted pole and an uninterrupted power flow through the heathy pole.

- A metallic return transfer breaker (MRTB) is normally closed but carries no current. It will carry a rated current if a pole fault occurs and the NBS is tripped. In most HVDC installations it is not allowed to operate a system with an earth return for a prolonged period of time. If both DC lines are available after a pole fault, then return current is transferred to the DC line on the faulted pole using the following sequence: NBS open, DC close, ERTB close and MRTB open.

- An Earth return transfer breaker (ERTB) is open in normal operation and has the opposite function to an MRTB. It transfers the earth current to the DC line on the faulted pole.

7.6 Overvoltage Protection

The HVDC system include numerous semiconductor-based components, which have high costs and limited voltage withstand abilities and therefore must be protected from overvoltage's. The stakes are high with converter system and it is more expensive to provide large overvoltage margins comparing with other electro-mechanical components. For this reason surge arrester (SAs) are extensively used with HVDC systems, at valve level, bridge level and pole level as transformer protection, as DC cable protection and in other places as shown in Figure 7.8.

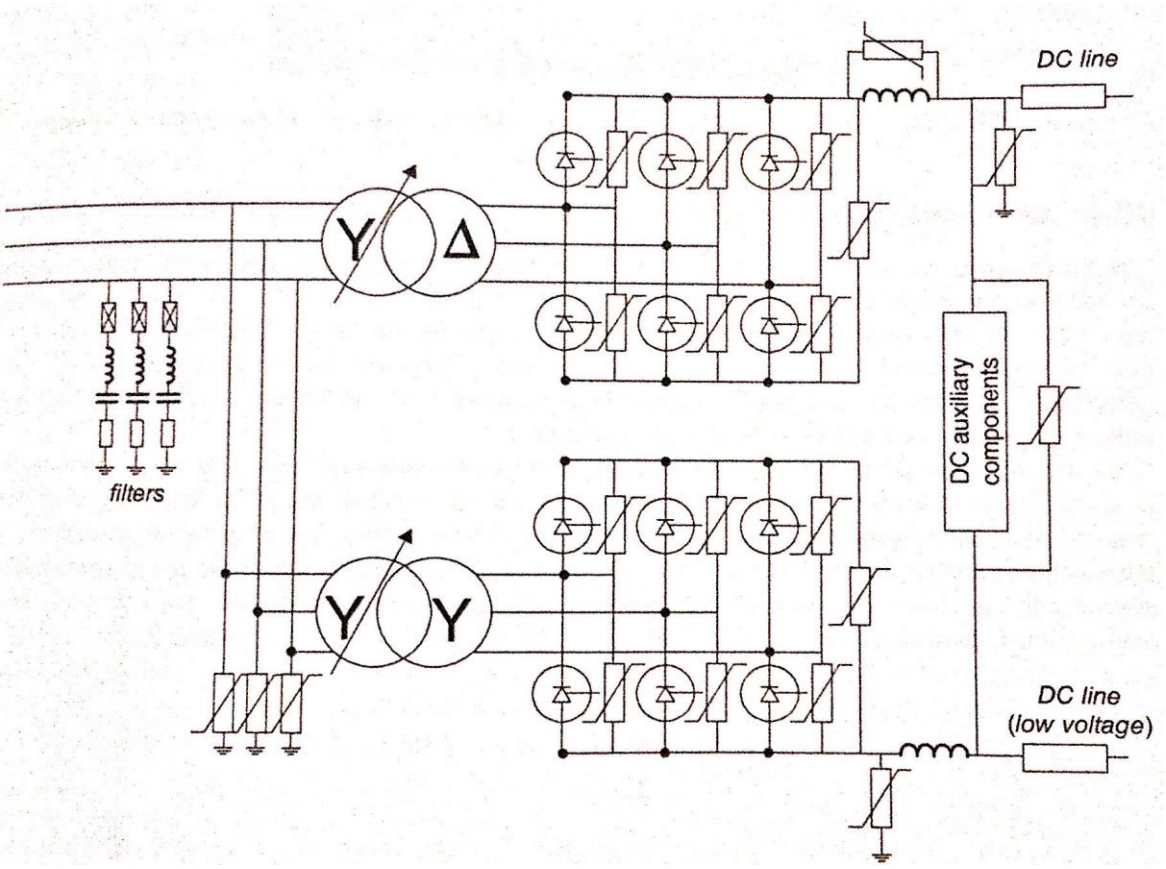

Figure 7.8 *Location of surge arrester at an HVDC station.*

Surge arrester will be rated according to insulation coordination strategies. They will always have a protective voltage level below the component rated voltage. A SA protective level that is too low would lead to large leakage current, which can cause SA overheating. The purpose of a SA is to clip the voltage spike but they are not normally designed to damp large energy. If the SA is operated, the current will increase and then converter controls and protection methods will be activated to manage the fault current. Figure 7.9 shows some practical HVDC surge arresters. The arresters are installed all over the world in all type of climates. The designs are type tested according to the **IEC 60099-4, ANSI/IEEEC62.11** and also comply with customer specific standards.

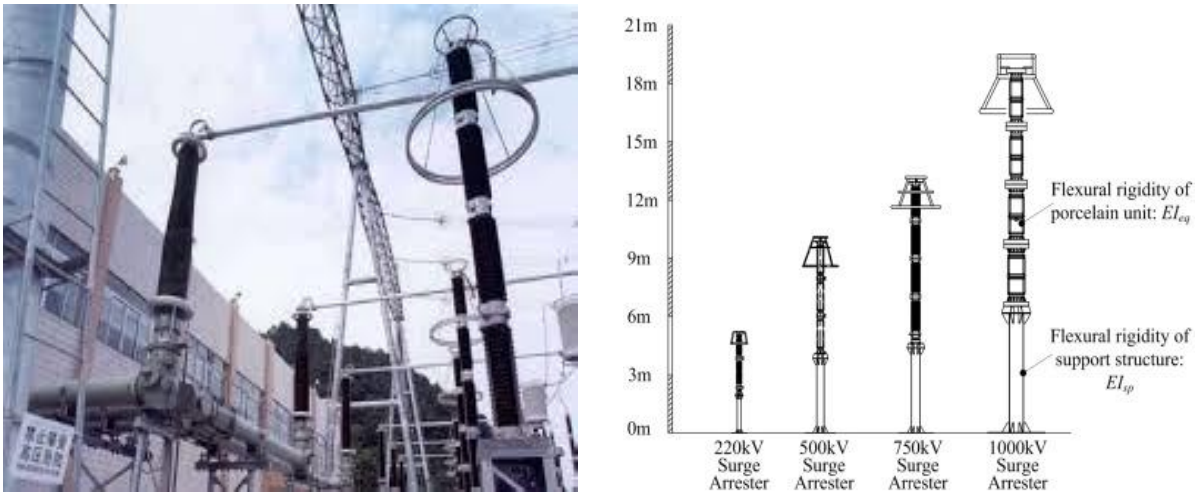

Figure 7.9 *surge arrester HVDC* (ABB).

8 LCC HVDC System Harmonics

8.1 Harmonic Performance Criteria

The AC current injected by a line-commutated converter (LCC) has been assumed as in ideal *sine* at fundamental frequency in previous chapters. This current, however, contains harmonics and the quality of converter power is normally evaluated in terms of the following performance parameters: harmonic factor (HF), total harmonic distortion (THD) and distortion factor (DF).

The HF_n, is a measure of individual harmonic magnitude, and it is defined as:

$$HF_n = \frac{v_n}{v_1} \tag{8.1}$$

Where V_1 is the RMS value of the fundamental component and V_n is the RMS value of the *nth* harmonic component.

The *THD*, is a measure of closeness between the actual waveform and its fundamental component, and it defined as:

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=2}^{\infty} V_n^2} \tag{8.2}$$

When calculating the THD the largest harmonic is normally set to 50.

The THD gives the total harmonic content, but it does not indicate the level of each harmonic component. If a common low pass filter is used at the inverter AC terminal, the higher order harmonics would be attenuated more effectively. Knowledge of both the frequency and magnitude of each harmonic is therefore important. The DF indicates the amount of harmonic distortion that remains in a particular waveform after harmonics of that waveform have been subjected to a second order attenuation. Thus, DF is a measure of effectiveness in reducing unwanted harmonics without having to specify the values of a second order filter and it is defined as:

$$DF = \frac{1}{V_1}\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n^2}\right)^2} \qquad (8.3)$$

The DF of an individual nth harmonic component is defined as:

$$DF_n = V_n / V_1\, n^2 \qquad (8.4)$$

It is desirable to have as low value as possible for all of the above harmonic performance indicators.

8.2 Harmonic Limits

The harmonics in AC systems cause a range of problems and must be limited. Some common problems resulting from high harmonics include: machine heating and pulsation, insulation stress, overloading of capacitor banks and interference with electronic and telecommunications equipment. With HVDC systems harmonics can also cause control and stability issues. There are also other issues like telephone-line interference and audible noise, which led to cost implications with some HVDC systems but they are not examined in detail.

Table 8.1 shows the voltage harmonic limits according to ***IEEE*** and **Table 8.2** shows ***IEC*** limits.

Voltage at PCC	**Individual harmonic magnitude HF (%)**	**Total voltage distortion-THD (%)**
69 KV and below	3	5
69-161 KV	1.5	2.5
161KV and above	1	1.5

Table 8.1 ***IEEE*** standard 519 harmonic limits.

Odd harmonics			**Harmonics multiples of 3**			**Even harmonics**		
Order	**Harmonic voltage (%)**		**Order**	**Harmonic voltage (%)**		**Order**	**Harmonic voltage (%)**	
	MV	**HV**		**MV**	**HV**		**MV**	**HV**
5	5	2	3	4	2	2	1.8	1.4
7	4	2	9	1.2	1	4	1	0.8
11	3	1.5	15	0.3	0.3	6	0.5	0.4
13	2.2	1.5	21	0.2	0.2	0.8	0.5	0.4
			$21< n <45$	0.2	0.2			

Table 8.2 ***IEC*** *standard 61000 3-6 harmonic limits*.

On the DC side of an HVDC system, there are no loads (customers) and the above limits do not apply. There are, however, two main criteria that influence the design magnitude of DC harmonics:

- Telecommunication interference.

- DC cable insulation limits in harmonics. According to GIGRE brochure 219, for DC extruded cables, the maximum DC voltage distortion should be 3% Note, however, that many thyristor HVDC system use mass-impregnated DC cables, which have better harmonic tolerance.

8.3 Thyristor Converter Harmonics

A thyristor converter behaves as a current source on the AC side. At full power, the AC current for a six-pulse converter bridge, as shown in Figure 3.3 and connected through a Y-Y transformer, can be expressed using the Fourier series (neglecting commutation overlap) as:

$$I_g = 2\frac{\sqrt{3}}{\pi} I_{dc}\left[\sin\omega t - \frac{1}{5}\sin 5\omega t - \frac{1}{7}\sin 7\omega t - \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t + \ldots\right] \tag{8.5}$$

Which can also be expressed as:

$$I_g = 2\frac{\sqrt{3}}{\pi} I_{dc}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega t),\quad n = 6k \pm 1,\quad k = 1,2,3,\ldots \tag{8.6}$$

It is concluded that all harmonics of the order 6 $k \pm 1$ are present on the AC side, where k is any integer. The magnitude of harmonics is inversely proportional to the harmonic order.

The AC current generated by a converter with a $Y - \Delta$ transformer is:

$$I_g = 2\frac{\sqrt{3}}{\pi} I_{dc}\left[\sin\omega t + \frac{1}{5}\sin 5\omega t + \frac{1}{7}\sin 7\omega t - \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t + \ldots\right] \tag{8.7}$$

The $Y - \Delta$ transformer therefore gives 180^o phase-shifted 5th, 7th harmonics and multiples. The HVDC systems use a 12-pulse series connection, which consists of one Y-Y converter. The current in a 12-pulse converter system is the sum of Eqs (8.5) and (8.7)

$$I_g = 4\frac{\sqrt{3}}{\pi} I_{dc}\left[\sin\omega t - \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t - \frac{1}{23}\sin 23\omega t + \frac{1}{25}\sin 25\omega t + \ldots\right] \tag{8.8}$$

And therefore the 12-pulse system has 11th, 13th and all 12 $k \pm 1$ harmonics:

$$I_g = 2\frac{\sqrt{3}}{\pi} I_{dc}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega t),\quad n = 12k \pm 1,\quad k = 1,2,3,\ldots \tag{8.9}$$

If a commutation overlaps of the angle μ is present, the current "squares" are rounded and the harmonic magnitude is lower. The harmonic magnitude with overlap I_{nov} is reduced compared to a case with no overlap I_n for *n-th* harmonic:

$$\frac{I_{nov}}{I_n} = \frac{\sqrt{H^2 + K^2 - 2HK\cos(2\alpha + \mu)}}{\cos\alpha - \cos(\alpha + \mu)}$$

$$H = (\sin(n+1)\mu/2)/(n+1)$$

$$K = (\sin(n-1)\mu/2)/(n-1) \qquad (8.10)$$

On the DC side, a thyristor converter appears as a DC voltage source with a DC waveform, shown in Figure 3.4. This voltage source will have 6 *k* (*k* = 1, 2, …) voltage harmonics in the case of a six-pulse bridge. With 12-pulse systems, only 12 k (*k* =1, 2, …) harmonics will be present.

The above harmonics are called characteristics harmonics. They occur according to the theoretical study of ideal current/voltage waveform. The non-characteristic harmonic (i.e. second, third, …) are not present in theoretical studies but may occur in practical HVDC systems. Some of the causes of non-characteristic harmonics are:

- An unbalanced AC system caused by small difference in the line impedances in three phases;
- Converter transformer asymmetry, and phase difference in transformer ratios;
- Converter asymmetry, because of the controller firing angle, or driver or thyristor asymmetry.

AC grid unbalance is quite common cause of non-characteristic harmonics. An unbalance on the AC grid will cause the thyristor converter to produce the following AC harmonics:

$$n = kp \pm 3 \qquad k = 0, 1, 2, \ldots \qquad (8.11)$$

where *p* is the pulse number of the thyristor converter. The same unbalance will produce on DC side:

$$n = kp \pm 2 \qquad k = 0, 1, 2, \ldots \qquad (8.12)$$

In general, a *nth* harmonic on DC side will produce an $n \pm 1$ harmonic on the AC side.

8.4 Harmonic Filters

8.4.1 Introduction

At each HVDC station there will be harmonic filters on the AC side and perhaps also on the DC side, which are designed to reduce harmonic distortion to within the specified limits. The filters have capacitive reactance at fundamental frequency and they also help to supply the reactive power requirement from converters. Since HVDC reactive power is variable (it is proportional to active power) the capacitors and/or filters will be arranged in switchable banks, which are switchgear, they can occupy over 50% of the HVDC station footprint.

Most systems use shunt filters, but some systems use a combination of shunt and series AC filters. In case of capacitor-commutated converter (CCC) HVDC systems, the HVDC receives full reactive power compensation from series capacitors and therefor shunt filters are small.

Typically, Ac-side tuned filters will be used for the two to four lowest order AC harmonics, like 11th and 13th on 12-pulse systems, or 23rd and 25th on 24-pulse terminals. Damped (high-pass) filters will also be employed for higher order harmonics. Figure 8.1 shows the possible filters arrangement for a 12-pulse HVDC terminal while Figure 8.2 shows photograph of some practical AC filters at the HVDC terminal.

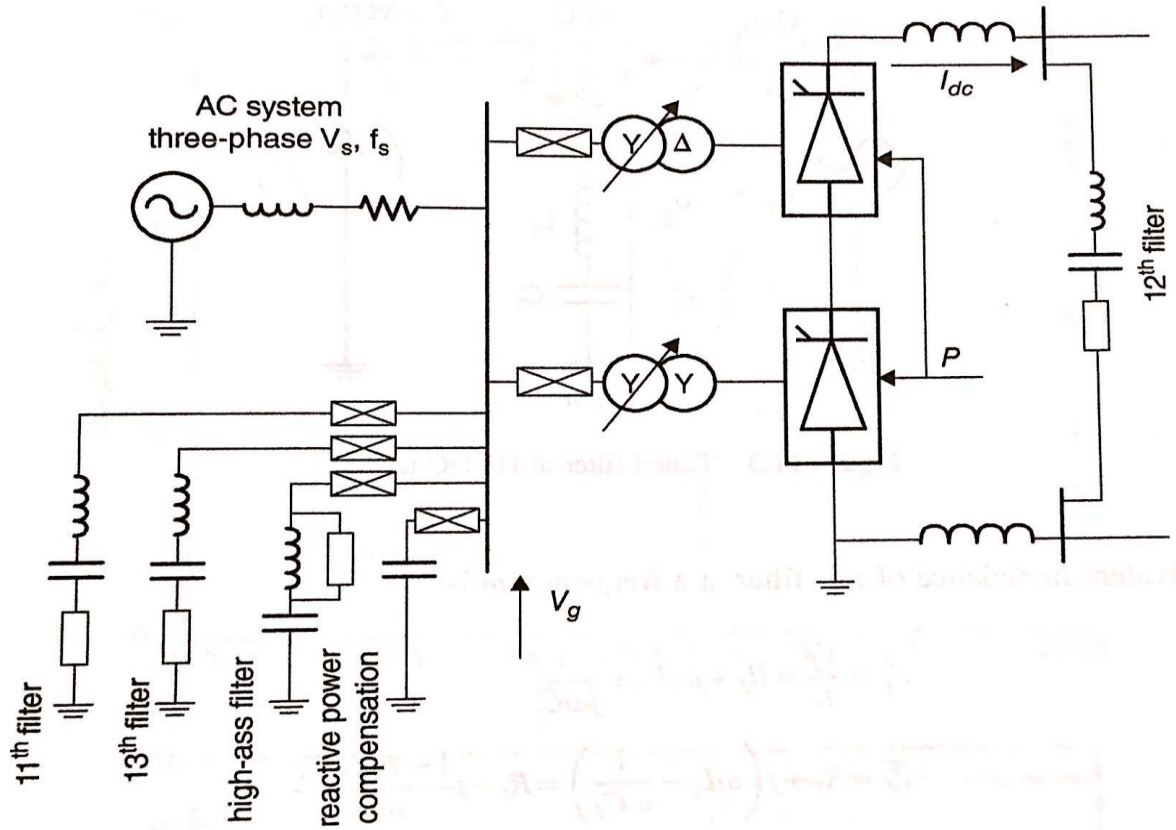

Figure 8.11 *HVDC station with harmonic filters.*

Figure 8.2 AC filters at Moyle HVDC station (2001). From Siemens.

An HVDC with overhead lines will commonly have DC -side 12th or 24th filters. The DC cables have high capacitance and they naturally reduces harmonics.

8.4.2 Tuned Filters

The simplest single tuned filter is shown in Figure 8.3, where the converter is shown as a harmonic current source. The other commonly used filters are double tuned, and triple tuned. The filters in this figure consists of a series LC circuit and a resistance of the inductor.

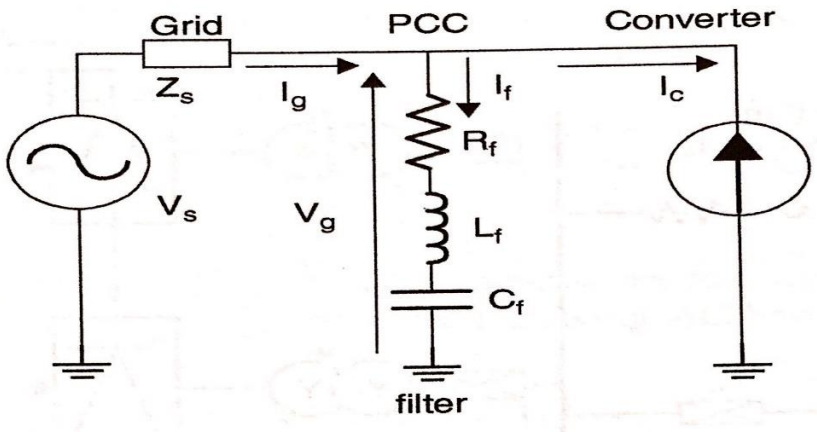

Figure8.3 *Tuned filter at HVDC terminal*

The equivalent impedance of this filter at a frequency ω is:

$$\overline{Z_f} = \frac{V_f}{I_f} = R_f + j\omega L_f + \frac{1}{j\omega C_f}$$

$$\overline{Z_f} = R_f + j\left(\omega L_f - \frac{1}{\omega C_f}\right) = R_f - j\frac{1-\omega^2 L_f C_f}{\omega C_f} \qquad (8.13)$$

The characteristic frequency ω_f (where capacitive impedance equals inductive impedance) of this filter is:

$$\omega_f = \frac{1}{\sqrt{L_f C_f}} \qquad (8.14)$$

And the quality factor is q_f *is defined as:*

$$q_f = \frac{\omega_f L_f}{R_f} = \frac{\sqrt{\frac{L_f}{C_f}}}{R_f} \qquad (8.15)$$

Typical values for the quality factor are in the range $50 < q_f < 100$. The band pass (BP) for the tuned filter is defined as:

$$BP = \pm\frac{1}{2q_f}\omega_f \qquad (8.16)$$

Figure 8.4 shows the Bode plot for two different q_f larger q_f (lower R_f) implies better tuned frequency characteristics, which provide lower impedance for current harmonics. The filter impedance at characteristic frequency is:

$$\overline{Z_{ff}} = R_f \qquad (8.17)$$

And therefore the magnitude of the harmonic voltage at frequency ωf is directly proportional to Rf.

$$V_{gf} = I_{ff} R_f \qquad (8.18)$$

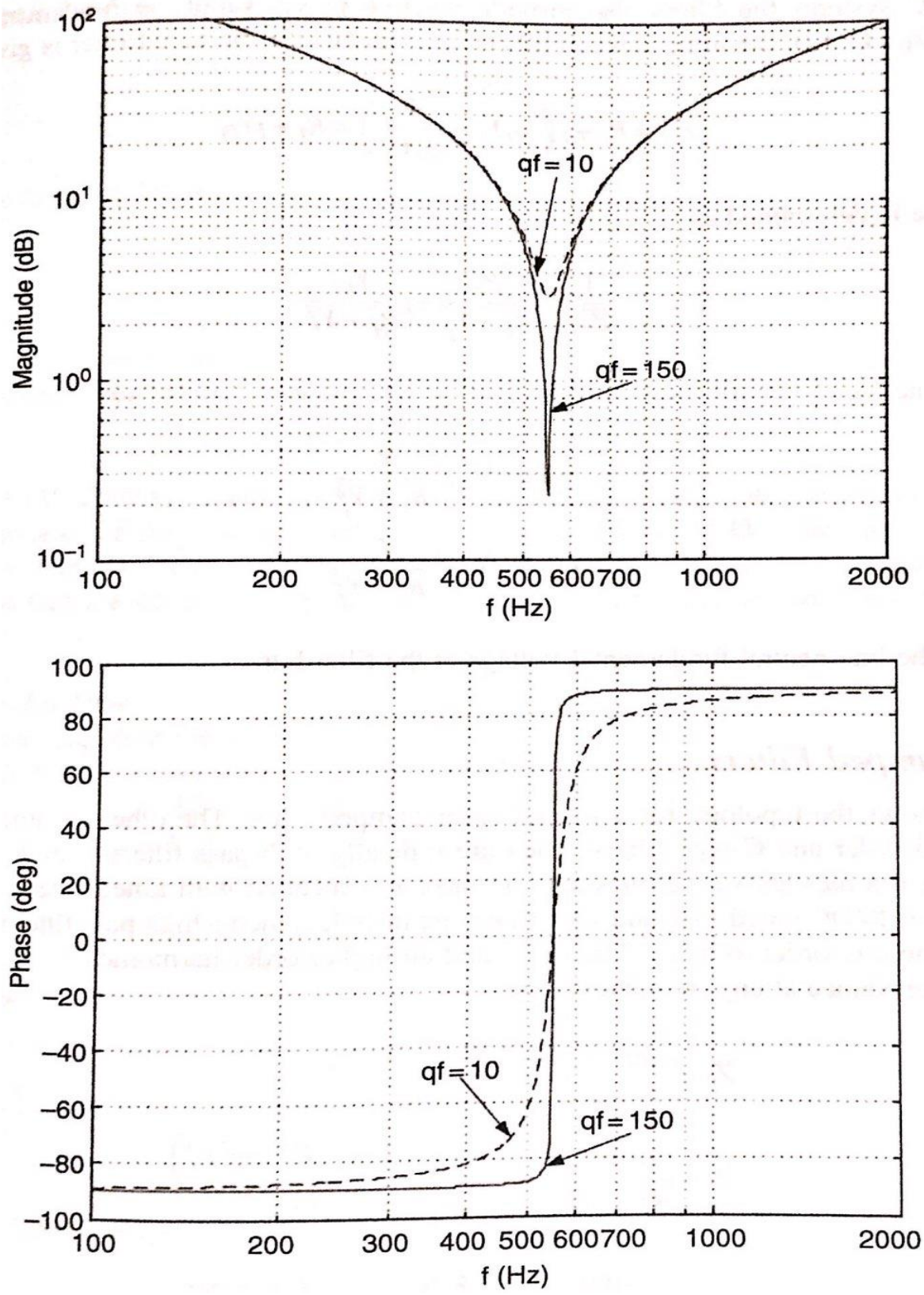

Figure 8.4 *Bode plot for 11th harmonic tuned filter with two different q_f.*

Where I_{ff} is the injected current at ωf. The filter loss at ωf frequency is:

$$P_{ff} = I_{ff}^2 R_f \tag{8.19}$$

It is desired that the impedance at the characteristic frequency is as low possible in order to reduce the bus-voltage harmonic distortion at this frequency. However, there are physical constrains related to parasitic resistance like inductor size and losses. The filter parameters may also change with the ageing of the components, in which case filters with higher *qf* become more detuned.

With HVDC system the filters also provide reactive power supply at fundamental frequency. Considering Eq. (8.13), the impedance at 50 Hz ($\omega_1 = 2\pi 50$) for the tuned filter is given by:

$$\overline{Z_{f1}} = R_f + j\left(\omega_1 L_f - \frac{1}{\omega_1 C_f}\right) = R_f + jY_{f1} \tag{8.20}$$

And the inverse is determined as:

$$\frac{1}{\overline{Z_{f1}}} = \frac{R_f}{R_f^2 + Y_f^2} - j\frac{Y_{f1}}{R_f^2 + Y_f^2} \tag{8.21}$$

Therefore the active P_f (filter Losses) and reactive Q_f filter power at 50 Hz are

$$P_{f1} = 3V_{g1}{}^2 \frac{R_f}{R_f^2 + Y_f^2} \tag{8.22}$$

$$Q_{f1} = 3V_{g1}{}^2 \frac{Y_{f1}}{R_f^2 + Y_f^2} \tag{8.23}$$

Where V_{g1} is the line-neutral fundamental voltage at the filter bus.

8.4.3 Damped Filter

Figure 8.15 shows the topology for a second-order damped filter. The other commonly used tuned filters are third-order and C-type filters. They are typically high-pass filters, which are designed to eliminate all harmonics above the ones that are directly cancelled with tuned filters. As an example, if with 12-pulse HVDC tuned 11th and 13th filters are installed, then a high pass filter will be designed for 24th harmonic in order to damp 23rd, 25th and all higher order harmonics.

The filter impedance at any frequency ω is:

$$\overline{Z_f} = \frac{j\omega R_f L_f}{R_f + j\omega L_f} + \frac{1}{j\omega C_f}$$

$$\overline{Z_f} = \frac{R_f \omega^2 L_f^2}{R_f^2 - \omega^2 L_f^2} + j\frac{\omega C_f \left(\omega R_f^2 L_f - R_f^2 + \omega^2 L_f^2\right)}{R_f^2 - \omega^2 L_f^2} \quad (8.24)$$

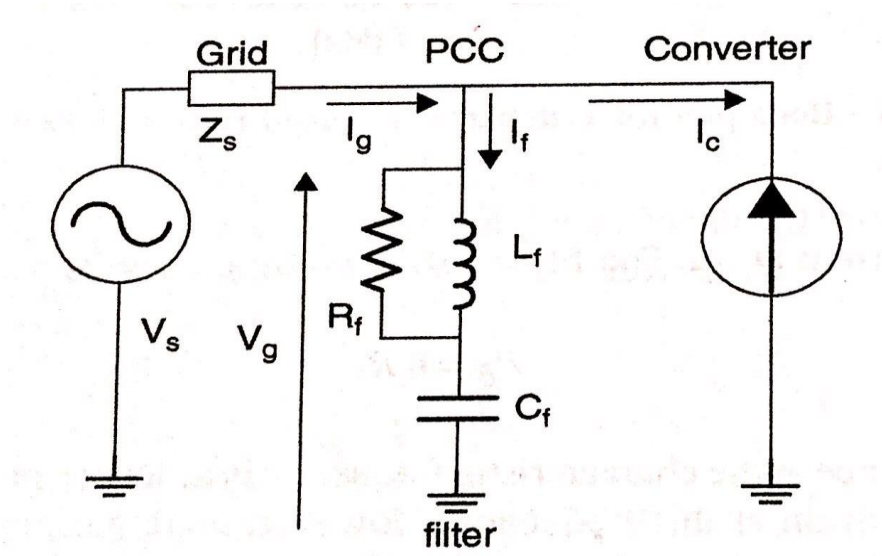

Figure 8.5 *Second-order damped filter at HVDC terminals.*

The characteristic frequency ω_f of this filter is:

$$\omega_f = \sqrt{\frac{q_f^2 + 1}{q_f^2}} \frac{1}{\sqrt{L_f C_f}} \quad (8.25)$$

And the quality factor is defined as:

$$q_f = R_f / \omega_f L_f \quad (8.26)$$

The quality factor typically low $1 < q < 10$, in order to provide damping at wide range of frequencies. Figure 8.6 shows the Bode plot for a high pass filter designed for 24th harmonic.

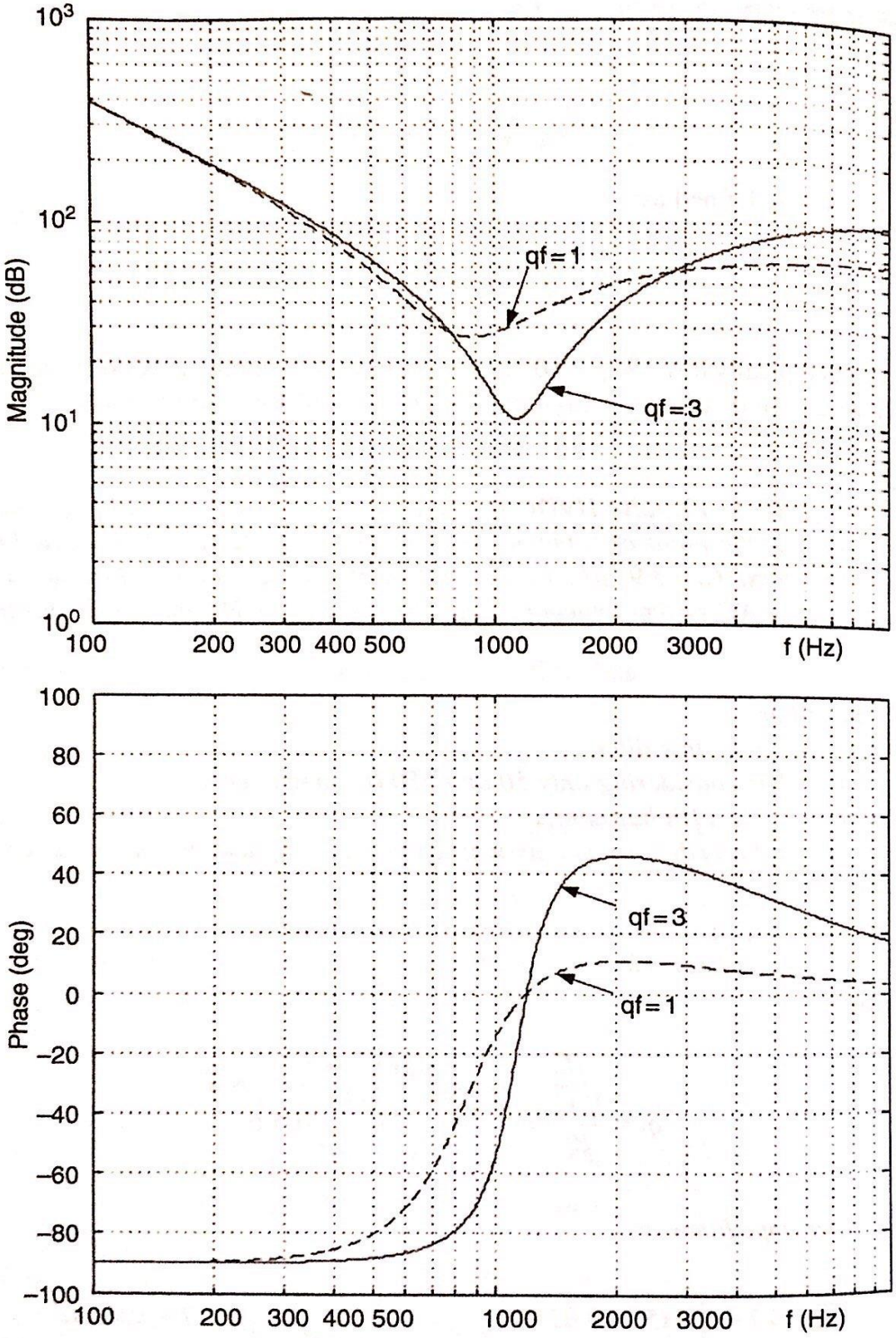

Figure 8.6 *Bode plot for 24th harmonic high-pass filter with two different* Q_f.

8.5 Non-characteristic Harmonic Reduction Using HVDC Controls

Some HVDC system use special supplementary control to reduce particular low order non-characteristic harmonics. This can potentially be an effective and low-cost method, but careful studies are required to avoid control instabilities. The scheme can be used with low-order DC-side harmonics that cause problems, like second harmonic resonance.

Figure 8.8 shows the HVDC (rectifier) control schematic with the supplementary control employed for eliminating harmonics at frequency ω_f. As normal HVDC controls have low bandwidth, they are not cable of regulating harmonic voltages. A special oscillator at frequency ω_f is used and the magnitude of the injected oscillation is controlled in a feedback manner using fast fourier transformation (FFT) processing of the measured DC voltage. The method is used only at a single frequency ω_f because any other frequency would require different and carefully tuned gain K_{wf}.

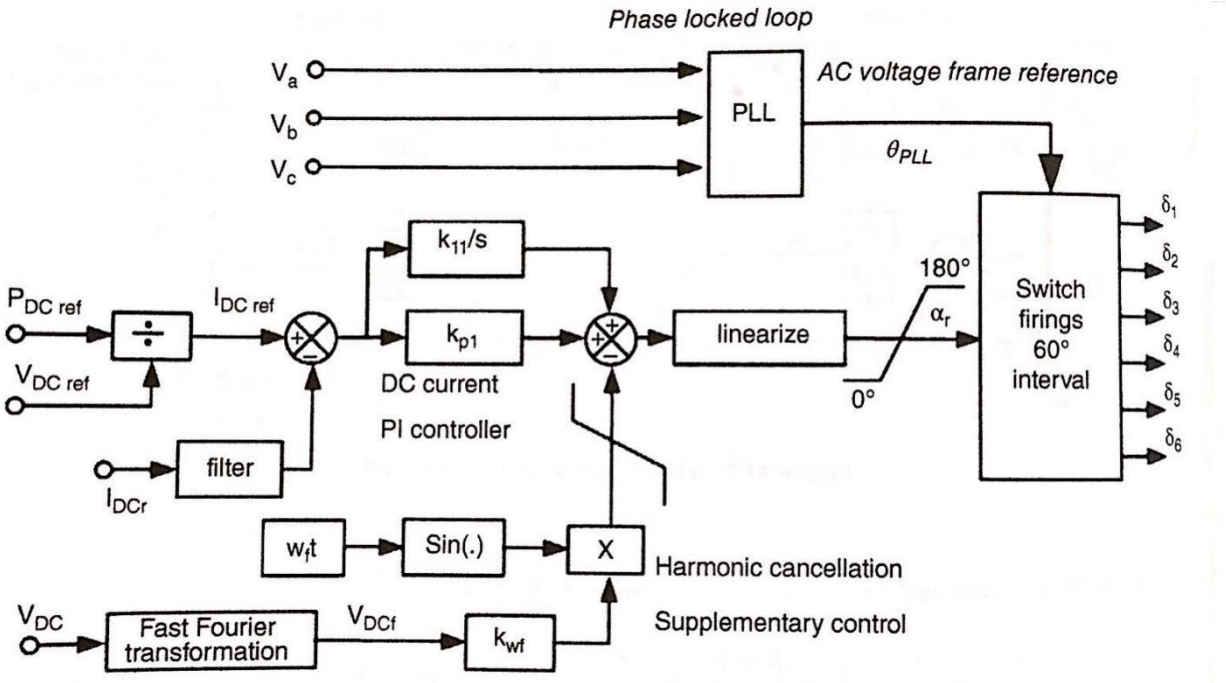

Figure 8.8 *HVDC supplementary control for DC harmonic elimination.*

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Part B: HVDC System Harmonic

9 VSC HVDC Applications and Topologies, Performance and Cost Comparison with LCC HVDC

9.1 Voltage Source Converters (VSC)

Voltage source converter (VSC) systems are based on self-commutating switches, typically insulated-gate bipolar transistor (IGBT) technology, which have several advantages compared with thyristors. The use self-commutating devices allows the application of high-frequency (over 1 kHz) pulse width modulation (PMW) techniques, which have been in use in the industrial drives sector since the early 1990s. By the use of PWM, the VSC may synthesize a fully controlled AC voltage, which enables precise control of active and reactive powers. This voltage appears a fundamental frequency *sine* with harmonics at the switching frequency and its multiples. The control is very fast, and, with appropriate feedback, the voltage source inverter may respond as a current source. Because of higher switching frequencies, harmonics are lower and therefore filtering requirements are reduced.

The use of VSCs for DC power transmission (VSC transmission) was introduced with the MW,±10 kV demonstrator at Hellsjön, Sweden in 1997. Figure 9.1 shows the basic schematic of a two-level VSC high-voltage direct current transmission system.

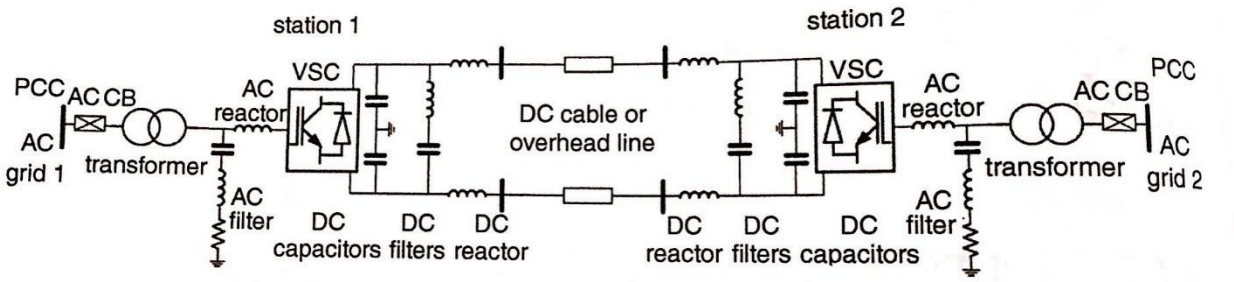


Figure 9.1 *A symmetrical monopolar VSC-HVDC transmission system based on a two-level converter.*

The main ***advantages*** of **VSC** converters, compared with ***line-commutated converters (LCCs)*** are summarized as:

- Active and reactive power can be controlled independently. The VSC is capable of generating leading or lagging reactive power, independently of the active power level. Each converter station can be used to provide voltage support to the local AC network while transmitting any level of active power, at no additional cost.

- If there is no transmission of active power, both converter stations operate as two independent static synchronous compensators (STATCOMs) to regulate local AC network voltages.

- The use of PWM with a switching frequency in the range of 1-2 kHz is sufficient to separate the fundamental voltage from the sidebands and supress the harmonic components around and beyond the switching frequency components. Harmonic filters are at higher frequencies and therefor have low size, losses and costs.

- Power flow can be reversed instantaneously (50-100 ms) without the need to reverse the DC voltage polarity (only DC current direction reverses). This implies that simpler cross-linked polyethylene (XLPE) DC cables can be used.

- Good response to AC faults. The VSC converter actively controls the AC voltage/current, so the VSC-HVDC contribution to the AC fault current is limited to rated current or controlled to lower levels. The converter can remain in operation to provide voltage support to the AC networks during and after the AC disturbance.

- Black-start capability, which is the ability to start or restore power to a dead AC network (network without generation units). This feature eliminates the need for a start-up generator in applications where space is critical or expensive, such as with offshore wind farms.

- VSC-HVDC can be configured to provide faster frequency or damping support to the AC network through active power modulation.

- Connection to passive AC system. A VSC converter can generate AC voltage using an internal independent oscillator. This facilitates transition from the grid mode to an intended or unintended islanded mode, as is required in the development of smart grids. Some VSC HVDC are used to drive dead loads (no active power generation).

- It is more suitable for paralleling on the DC side (developing multiterminal HVDC and DC grids) because of constant DC voltage polarity and better control.

- It facilitates modular development using basic constant-voltage cells. In particular, the latest modular multilevel converters (MMCs) use standard low voltage cells with capacitors.

The limitations and ***disadvantages*** of ***VSC*** technology are summarized as:

- Improved control is achieved at the expense of increased losses in the power converter. Increased losses are the result of:
  - Application of high frequency switching leads to increased switching loss.
  - Insulated-gate bipolar-transistor devices exhibit significantly higher on-state voltage drop compared to thyristor of similar voltage ratings. For a given power level, this will lead to increased conduction loss.
- Higher costs than LCC converters. A VSC requires a larger number of semiconductors and in particular with modular systems the number of switches is much higher than with an LCC.

- IGBT switches/modules have lower power capability than available thyristor packages, leading to an increased power component count. The semiconductor footprint is larger than with thyristors.

- IGBT devices have lower current overload capability than thyristors.

- High *dv/dt* transitions may be present at the connecting points (both AC and DC). This can cause problems with dominantly capacitive cable systems and also electromagnetic interference.

- DC-side faults are a serious issue because a VSC behave like an uncontrolled diode bridge during a DC fault. Diode overrating is typically required, and the fault is cleared by AC circuit breakers (CBs). The VSC converter reconnection after AC CB tripping may take a long time.

- The development of multiterminal DC and grids requires very fast DC CBs.

- Insulated-gate bipolar transistors naturally fail in open circuit. A failure in a short circuit can be achieved at the expense of special packaging or using much more complex valve design compared with thyristors.

9.2 Comparison with line-Commutated Converter (LCC) HVDC

High-voltage direct-current systems are currently implemented using both LCC and VSC technologies. Despite evident technological advantages, VSC HVDC did not completely replace LCC HVDC. Line-commutated HVDC systems retain some advantage, in particular related to costs and ratings, but also, importantly, LCC represents a well-established technology with many years of experience. LCC HVDC provides a practical solution using robust devices and well proven circuits. At highest power levels (over 2 GW) they are exclusively used. The DC systems with overhead lines are exposed to frequent DC faults and LCC converters are preferred in these applications because of good handling of such faults. Moreover, LCC HVDC generally has lower costs, and so it is still preferred in applications where performance and station space are not critical.

The IGBT converters used in voltage-source HVDC are still in a state of development with relatively limited operation experience. Voltage-source converter HVDC has evolved in several different technologies, which have shown progressively improving performance, namely: two level, three-level and MMC (half bridge or full bridge). The latest generation of MMC VSC HVDC has converter station losses, which are not significantly larger than those with LCC HVDC.

The LCC HVDC has been studies in part A, while only the main advantages are summarized in this section in order to provide comparison with VSC HVDC:

- Thyristor devices are available in robust voltage (6-10 kV), high-current (3-4 kA) capacity single wafer capsules.

- Thyristor have excellent overcurrent capability.

- Thyristors naturally fail in a short circuit, which is desirable for series strings in high-voltage valves.
- Thyristors have a lower on-state voltage drop and costs are lower than with IGBT. Line-commutated converters require switches for one current direction while VSC converters have semiconductors for two current directions.

- LCC HVDC have an established track record at transmission voltage and power levels.
- Resilience to DC-side short circuit faults. The system can operate well at low DC voltage and DC fault recovery is well controlled. Direct current faults do not affect the AC system.

- LCC HVDC provides AC system frequency stabilization in many installations but performance in limited because of reactive power issues. The AC voltage control is also implemented in some installations, but performance is very limited.

The notable shortcoming of LCC HVDC are:

- Line-commutated thyristor-based system inject significant low order harmonics, which must be eliminated using large passive filter arrangements. The presence of filters may lead to circulating harmonic current and stability issues which must be, mitigated by damping networks may have to be designed specifically for each location and may not be optimal for all operating conditions.

- Line-commutated converters are inherently limited in their response time (limited to line-frequency switching). The control response time is in the order of 100-200ms.

- They require large reactive power compensation. This reactive power is supplied using passive filters and switched capacitors and reactors. The switched banks are required since the amount of reactive power needed varies with the active power magnitude and operating mode (inversion or rectification). As a result, the LCC HVDC station has larger footprint that VSC HVDC station.

- The power reversal requires the DC link voltage polarity to be reversed. This limits the range of DC cables that can be used (XLPE cables cannot be used if voltage reversal is needed). The time required to reverse the power flow is also limited to around 500ms, which imposes operational constraints.

- There is a practically minimal power flow of around 10%.

- It cannot to connect to very weak AC networks (with a low short circuit ratio, *SCR < 2.0).*

- Suffers from commutation failure, which is caused by 5-10% voltage drop on the inverter side. A commutation failure causes transient (0.5-1 s) interruption in power transfer. This can be partially mitigated with a capacitor-commutated converter (CCC) HVDC.

- Vulnerable to DC-side open-circuit conditions. This is very unlikely event and cause overvoltage, which can be limited by surge arresters.

- Multiterminal topologies can be built but with serious performance and cost penalties. Generally, only three-terminal systems are accepted in practice. DC grids are very challenging.

Table 9.1 provides a detailed comparison between high-voltage DC transmission system technologies. The comparison focuses on most important aspects, listed in the first column, such as control flexibility, fault ride through capability, conversion losses, electromagnetic compatibility (EMC) issues, and provision of auxiliary functionality such as voltage, frequency and damping support.

Table 9.1 Comparison between different HVDC technologies

	Current source converter based		**Voltage source converter based**		
	LCCs (line commutated converters)	**CCCs (capacitor commutated converters)**	**Two/three-level**	**MMC half bridge**	**MMC full bridge**
Switching device	Thyristor	Thyristor	IGBT	IGBT	IGBT
Switching Losses	Negligible	Negligible	High	Low	Low
On-state losses	Low	Low	Moderate	Moderate	Moderate, higher than with half bridge
Station size	Large	Large but reactive power banks and their circuit breakers are lower	Significantly reduced (around 50% of LCC)	Significantly reduced (around 50% of LCC)	Significantly reduced but higher than with half bridge
Active power control	Continuous with fast reversal but cannot operate within $\pm$10%	Continuous with fast reversal but cannot operate within $\pm$10%	Continuous from 0 to $\pm$100%	Continuous from 0 to $\pm$100%	Continuous from 0 to $\pm$100%
Active power reversal	DC voltage polarity must be change (0.5-1 s)	DC voltage polarity must be change (0.5-1 s)	Instantaneous (0.1 s) and no change of DC voltage polarity	Instantaneous (0.1 s) and no change of DC voltage polarity	Instantaneous (0.1 s) and no change of DC voltage polarity
Independent control of active and reactive power	No	No	Yes	Yes	Yes
Reactive power demand	50-60%	20-40%, but additional series capacitors are required	No	No	No
Reactive power control	Limited (lagging VAr only) and discontinuous using switch shunt capacitors for leading VAr	Limited (lagging Var only)	Continuous and inherent within converter control at no additional cost	Continuous and inherent within converter control at no additional cost	Continuous and inherent within converter control at no additional cost
Power levels	Up to 6400 MW	Up to 6400 MW	Up to 1200 MW	Up to 6400 MW	Up to 6400 MW
			Higher current by paralleling converters	Higher current by paralleling converters	Higher current by paralleling converters
Controllability (response time(s))	Fast (0.1-0.2)	Fast (0.1-0.2)	Very fast (0.03-0.05)	Very fast (0.03-0.05)	Very fast (0.03-0.05)
AC filters	Large	Large	Small	No	No
DC filter	Might be required	Might be required	No (rarely used)	No (rarely used)	No (rarely used)
Converter transformer	Expensive with high insulation requirement to withstand harmonics and voltage stress during power reversal	Expensive with high requirement to withstand harmonics and voltage stresses during power reversal, but with reduced MVA rating	Expensive with high requirement to withstand switching of large voltage steps with high frequency. Additional large AC inductor is needed	Standard AC transformer might be used	Standard AC transformer might be used
				Additional Large AC inductor is needed	Additional Large AC inductor is needed
Dc cable	Must withstand fast voltage polarity reversal during power reversal	Must withstand fast voltage polarity reversal during power reversal	Less expensive and light weight extruded cable	Less expensive and light weight extruded cable	Less expensive and light weight extruded cable
HVDC with overhead lines	Yes	Yes	Yes, but DC CBs might be needed	Yes, but DC CBs might be needed	Yes
Commutation failure	Present for AC disturbances (5-10%)	Present but significantly reduced	No	No	No

Applications with weak AC systems	Connection of strong systems (SCR>3); connection of weak system is possible but at additional cost by using STATCOM or synchronous condenser	Connection of strong and weak systems with SCR> =2	Very weak and network without generation can be connected	Very weak and network without generation can be connected	Very weak and network without generation can be connected
AC fault ride through capability	Possible, undergoing commutation failure and 0.5-1 recovery if inverter	Possible, undergoing commutation failure and 0.5-1 recovery if inverter	Excellent (three-level has issues with asymmetrical faults)	Excellent	Excellent
DC fault ride through capability	Excellent	Excellent	Difficult	Difficult	Excellent
			AC CB tripping	AC CB tripping	
Multiterminal configuration	Feasible but with performance limitation. Three-terminal topologies are preferred	Feasible but with performance limitation. Three-terminal topologies are preferred	Extension to any number of terminals is feasible assuming single protection zone	Extension to any number of terminals is feasible assuming single protection zone	Extension to any number of terminals is feasible. Mechanical DC CBs can be used
			DC side isolation is very difficult	Fast DC CB are needed	
Redundancy at switch level	Yes	Yes	Yes	Yes	Yes

9.3 Overhead and Subsea/Underground VSC HVDC Transmission

To transmit electrical energy using direct current over a distance, cables and overhead transmission lines can be used. The choice is influenced by environmental constraints as well as an overall optimization that considers total capital cost, performance, losses and transmission system reliability. There is also a small difference between underground and submarine DC cables. The cost of cables is considerably larger

than overhead lines – perhaps an order of magnitude larger – but there are also other aspects of cable projects that may influence the choice:

- Cables often have less impact on the environment than overhead transmission lines.

- In the recent years, it has become increasingly difficult to secure right of way for new overhead line corridors, or the permission process takes many years, and this has influenced decisions to use underground cables in some projects.

- Since VSC allow only one DC voltage polarity, the cable does not need to be designed for voltage polarity reversal. This allows use of less expensive and simpler XLPE DC cables.

- Cables are less likely to experience faults than overhead transmission lines. Since overhead transmission lines are always exposed to lightning strikes and pollution, faults are likely. Most line outages are transient, and transmission recommences once air insulation is restored, which can be readily managed with LCC HVDC. With VSC HVDC (expect full-bridge MMC) even transient DC faults may require tripping whole DC system with significant power-flow disturbance. If overhead line faults are permanent they are typically easier to locate and repair. In the event of a cable fault, the outage would be permanent and repair time may be significant.

- VSC HVDC converters have difficulties with DC faults and most of the exiting links operate with DC cables. It is accepted that if a cable fault occurs, the DC system will be tripped.

Manufacturers have traditionally been reluctant to offer VSC HVDC with overhead lines. The 300 MW, 350 kV, 2010 Caprivi VSC HVDC with overhead DC lines. The challenge with VSC overhead transmission is to avoid tripping the whole HVDC system (by AC CBs) for transient DC line faults (lightning strikes), which might be frequent on some corridors. A DC arc on overhead lines will not clear until the circuit is interrupted, and this is only achieved using AC CBs with VSC converters. Even when AC CBs are tripped, the high-impedance DC circuit will continue to conduct DC fault current through converter anti-parallel diodes. Caprivi HVDC link has an additional DC-side technology for managing DC faults.

With the introduction of full bridge MMC topologies (and other new MMC concepts) the VSC HVDC will be in much better position to operate with overhead lines.

9.4 DC Cable Types with VSC HVDC

The most common cable technologies have been discussed in Chapter 1, and include:

- Mass-impregnated cables (MI);
- Low-pressure oil-filled (LPOF) cables;
- Extracted cross-linked polyethylene (XLPE) cables.

Mass-impregnated and LPOF cables can also be used with VSC HVDC but, so far XLPE cables have been mostly used. Extruded polyethylene cables are less expensive, their construction is simpler, they allow a lower bending radius and have a number of other installation/transport advantages when compared with MI or LPOF cables. The insulation material (extruded polyethylene), conductor screen and insulation shields are extruded and chemically cross Linked. Most XLPE DC cable installations

are at voltages up to 320 kV, but currently XLPE cables are available at 525 kV. Figure 9.2 shows HVDC cables.

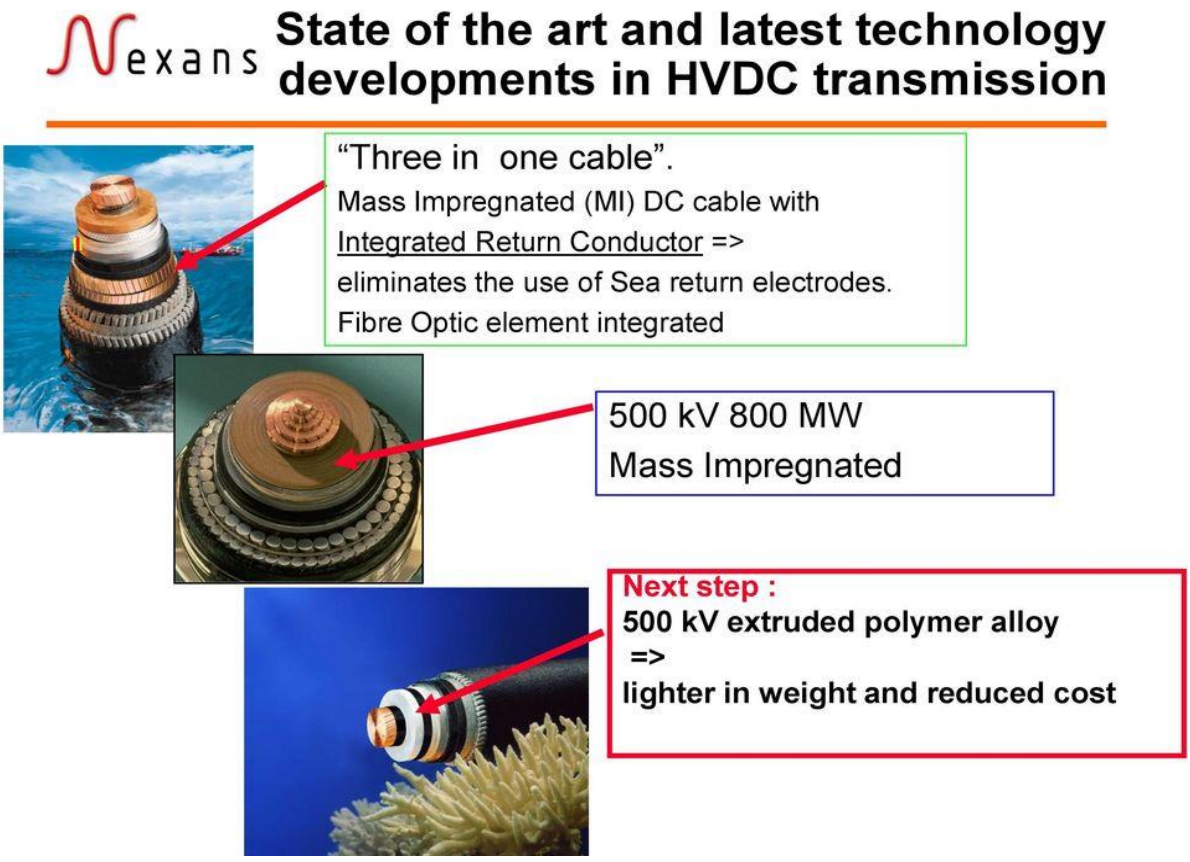


Figure 9.2 *HVDC cables from Nexans*

XLPE DC cable technology has been closely linked with the development of VSC HVDC. Extruded polyethylene cables have influenced VSC technology and VSC technology has opened a market for XLPE cables. Ongoing research and development aimed at increasing the rating of XLPE cables and reducing its cost may also make VSC transmission more attractive for a number of applications. Figure 9.3 shows typical XLPE DC cable.

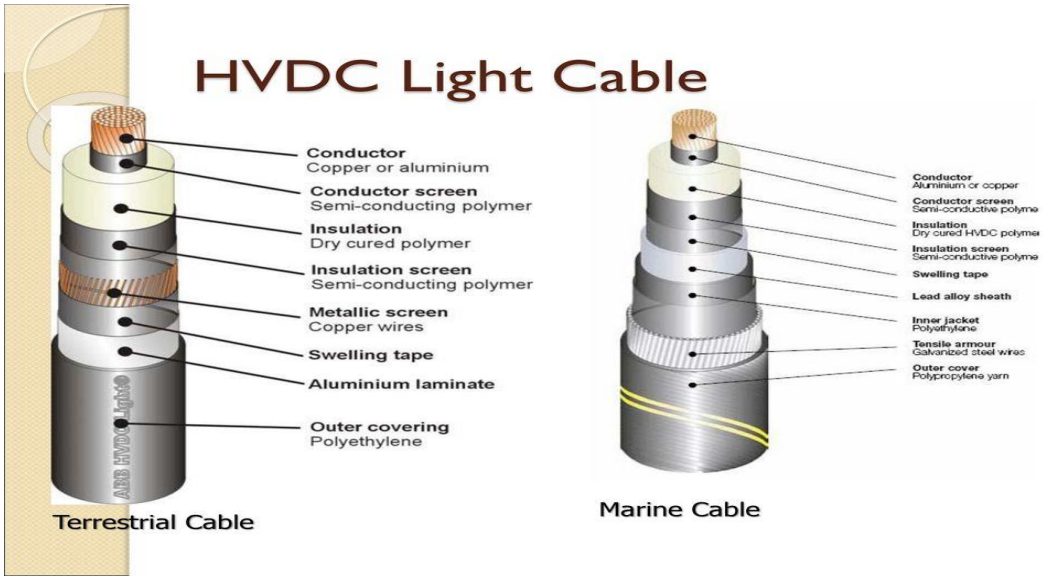


Figure 9.3 *Terrestrial og Marine cables for HVDC from ABB.*

9.4.1 Nexans achieves a triple technology milestone in HVDC cable systems

Nexans unique technology portfolio of world class cables meet the needs of high voltage direct current (HVDC) links through cross-linked polyethylene (XLPE) insulation designs now fully qualified for 320 kV, mass impregnated paper insulation and superconductor systems.

XLPE cable technology qualified for 320 kV and type tested at 525 kV

Nexans has fully qualified land and submarine XLPE cable system technology for 320 kV through the combination of type tests and long-term pre-qualification tests, all carried out according to international standards. The same technology principle was applied to achieve a step up in voltage, which led to the successful completion of a type test at 525 kV. This world-class result demonstrates the potential of the Nexans technology for DC links at all voltage levels currently requested by customers and lays the ground for further achievements.

Figure 9.4 *XLPE HVDC cables from Nexans (Cu & AL).*

Mass impregnated cables now ready for 600 kV

Mass impregnated HVDC cables are the preferred solution for long-distance submarine transmission large amounts of electrical energy at the highest voltages. Recent examples include the 100 km subsea element of Canada's new 900 MW interconnection to be constructed between Labrador and Newfoundland. The same cable design is also being used for the Skagerrak 4 interconnector between Denmark and Norway.

Through the decades mass impregnated cable technology has delivered excellent service for a large number of power transmission links operating at voltages up to 525 kV and a power rating exceeding 800 MW per cable. To meet the demand for even higher power ratings, Nexans has qualified the first 600 kV mass impregnated cable with a paper-based insulation providing a power transmission capacity of 1900 MW in a bipole configuration. This achievement consolidates Nexans' leading position in the mass impregnated HVDC cable business and proves that such cables are highly competitive for the future realization of high-power HVDC transmission systems.

Figure 9.5 *Mass impregnated cable from Nexans (Cu).*

Superconducting power cables for DC systems

Nexans is also the world leader in the field of superconducting power cables. Further to successful tests some years ago at 200 kV, Nexans is engaged in the European project Best Paths aiming at developing a 320 kV DC cable system with a capacity of 6,4 GW per bipolar, which represents the combined production of multiple nuclear reactors.

This ongoing project will set the basis for the next generation of electric highways and offers innovative solutions to transfer the full transmission power of a HVDC overhead line corridor into one cable system.

"*These technological achievements demonstrate the efficiency of the organization we recently put in place to speed up developments in the field of HVDC systems*", said Jean-Maxime Saugrain, Chief Technical Officer of Nexans High Voltage and Underwater Cables Business Group. "*The cable systems we have developed and successfully tested up to 525 and 600 kV are just the tip of the iceberg. A major effort was made to address specific issues in HVDC systems, in particular issues related to accumulation and mobility of electrical charges. This is of key importance for the long-term reliability of HVDC cable systems and therefore for the satisfaction of our customers."*

Figure 9.6 *Superconducting power cable from Nexans*

9.5 Monopolar and Bipolar VSC HVDC System

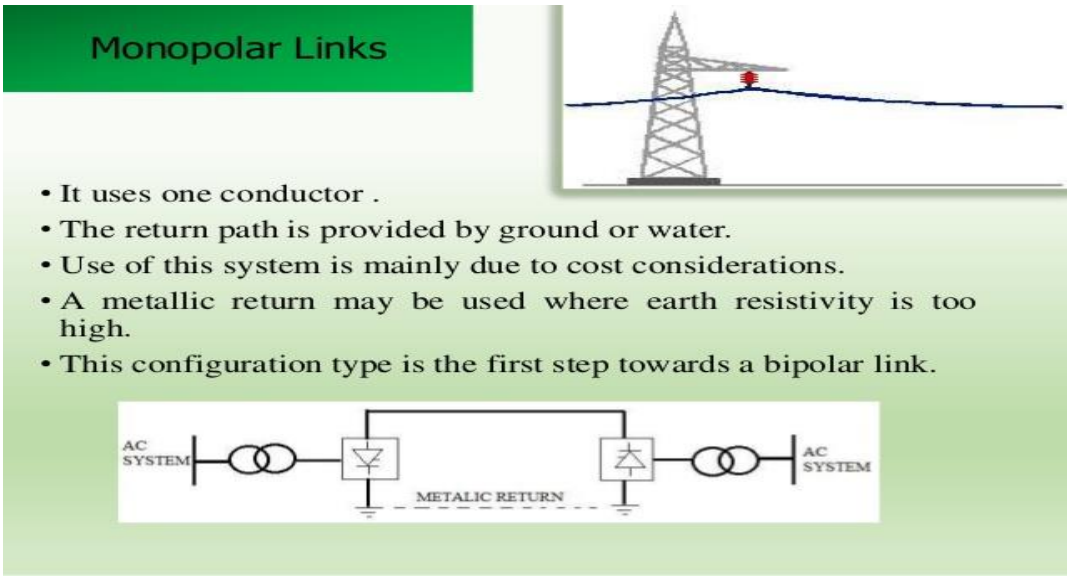


Figure 9.7 *HVDC Monopolar*

All the HVDC topologies, including monopolar figure 9.7) and bipolar(figure 9.8), discusses with LCC HVDC in section 1.4 can also, be used with VSC transmission. However, most installed VSC HVDC system are symmetrical monopoles. Symmetrical monopoles have positive and negative DC cables (as bipoles) but the system is controlled/operated as a single unit (as a monopole), as schematically shown in figure 9.1. There are a number of reasons for using symmetrical monopole (which is not used with LCC HVDC) with the early VSC HVDC. Most VSC HVDC are cable system and considering that XLPE cables have been available with limited voltage rating (320 kV) only symmetrical configuration achieves required pole-pole DC voltage. The power rating and voltage levels with installed VSC transmission have also been relatively low to justify full bipolar topologies.

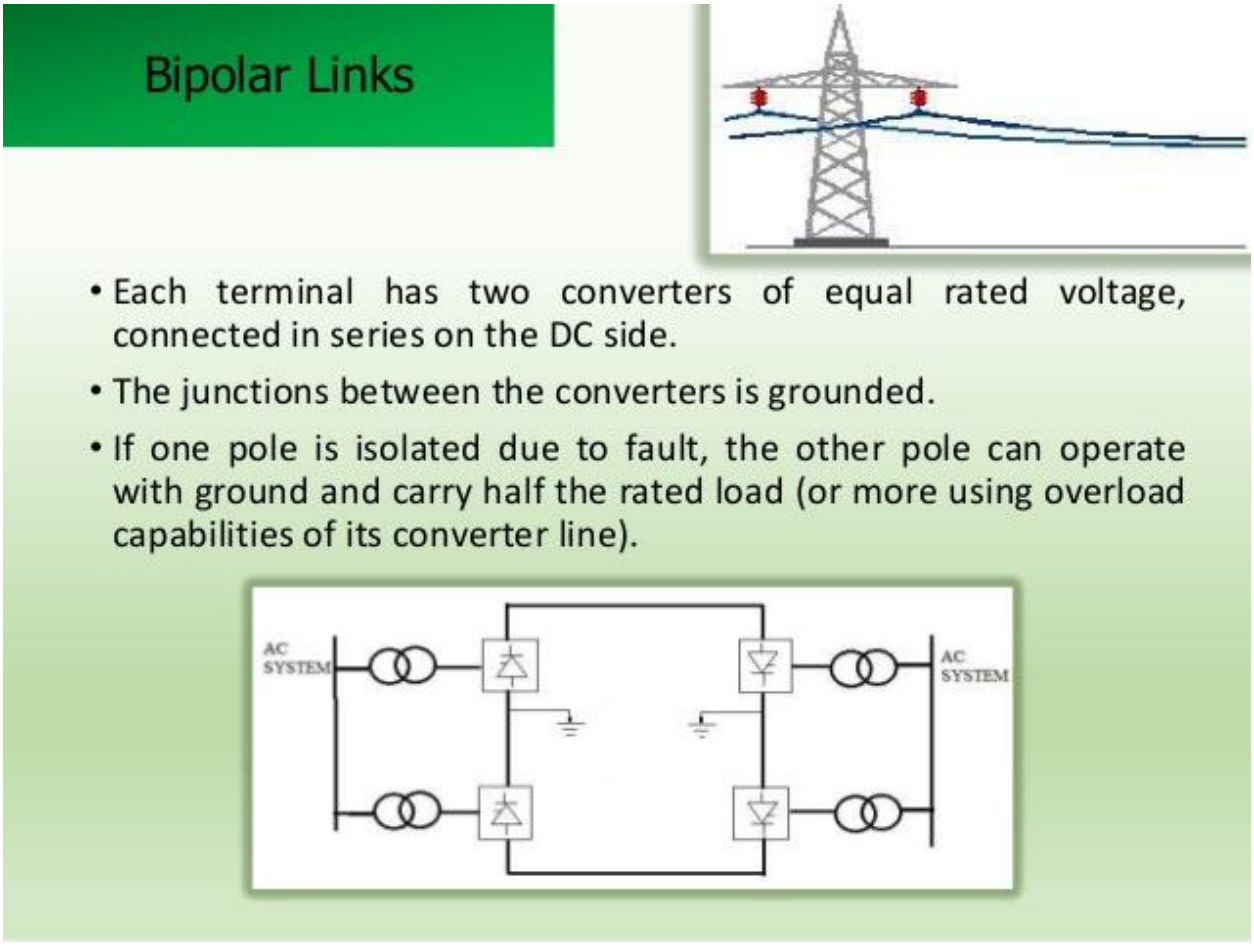


Figure 9.8 *HVDC Bipolar*

The Caprivi overhead link is one of the few monopolar VSC HVDC in operation, which is planned to become a bipolar when the second pole is added in the future. The 78 MW, 150 kV, 2011 Valhalla HVDC also employs monopolar topology. The Skagerrak 4 is a unique topology, since it is a monopolar VSC HVDC, which will operate with another pole of LCC HVDC type (Skagerrak 3).

9.6 VSC HVDC Converter Topologies

The VSC-HVDC transmission system has been implemented using two-level VSCs (Figure 9.9), three-level VSCs (figure 9.10), and multilevel VSCs (Figure 9.11)

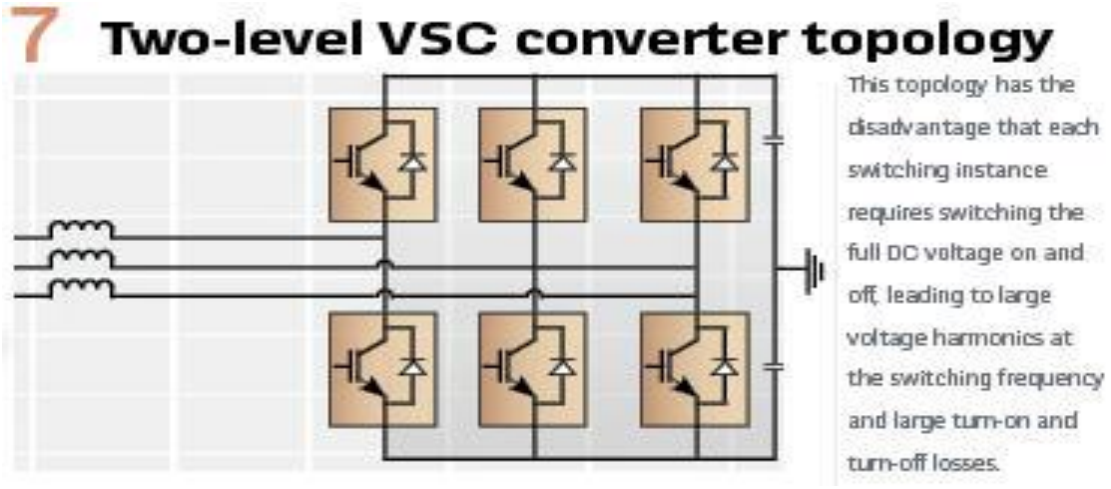


Figure 9.9 *two-level VSC-HVDC Converter.*

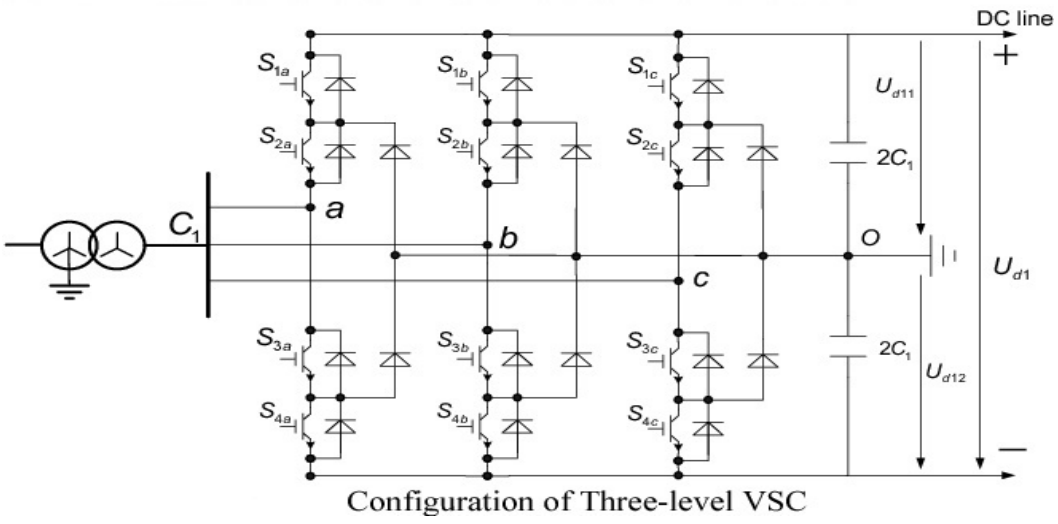


Figure 9.10 *Three-level VSC-HVDC Converter.*

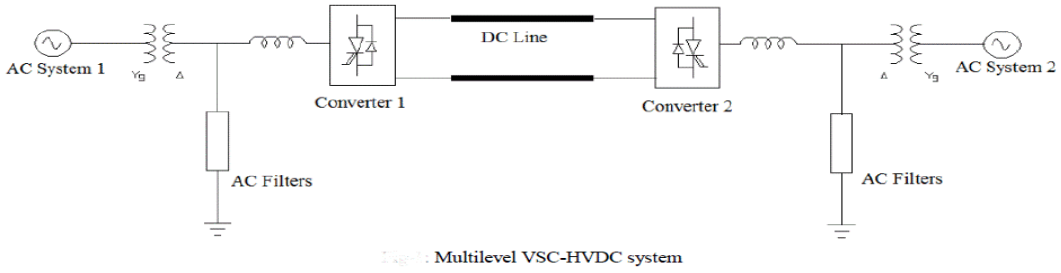


Figure 9.11 *Multilevel VSC-HVDC system*

9.6.1 HVDC with Two-level Voltage Source Converter

Two-level Sinusoidal pulse width Modulation (SPWM) topology was used in the first generation of VSC HVDC in the period 1996-2006, and table 9.2 shows some example HVDC installations. It is also currently available in addition to MMC HVDC but mainly for lower power rating.

Table 9.2 Examples of the VSC-HVDC transmission system based on the two-level converter.

Project	***Rating***	***PMW-strategy***	***Application***	***Distance (km)***	***Commissioning year***
Terranora (Australia)	*180 MW, V_{dc} = ±80 kV*	*SPWM*	*Controlled asynchronous connection for trading*	*59*	*2000*
Tjareborg (Denmark)	*8 MW, V_{dc} = ± 9 kV*	*SPWM*	*Wind-power connection*	*4.3*	*2000*
Gotland (Sweden)	*50 MW, V_{dc} = ± 80 kV*	*SPWM*	*Permission for underground cable*	*70*	*1999*

Practically, the maximum switching frequency with two-level HVDC converters is around 1.5 Hz (27-33 frequency modulation ratio). Figure 9.12 shows a two-level VSC that uses self-commutated switching device, mainly IGBTs. The capacitor C_{dc} of the VSC must be sized to maintain a constant DC voltage. The size (footprint) of the two-level VSC-HVDC terminal is around 50% size of the LCC HVDC station.

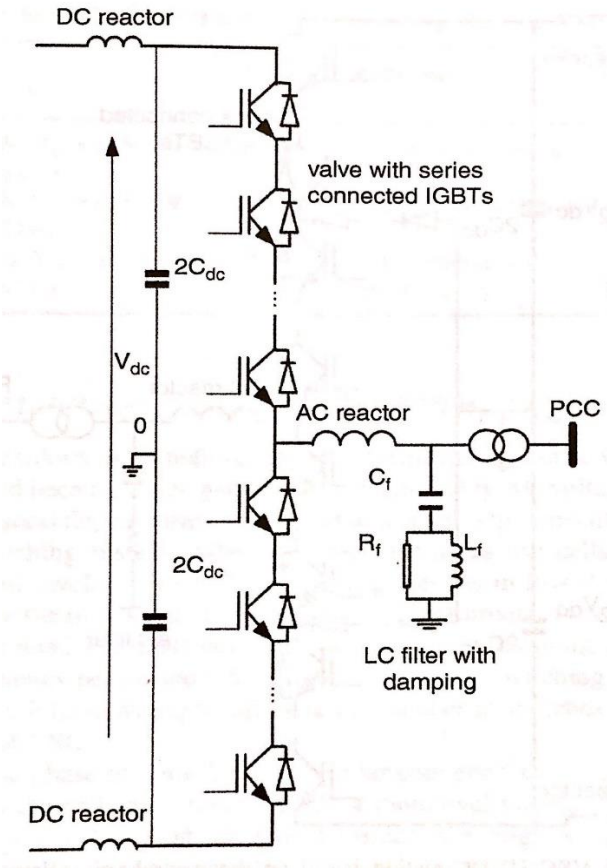


Figure 9.12 *One phase of VSC-HVDC station based on the Two-level converter topology.*

The main characteristics of this technology are:

- Simple converter construction that require a simple control strategy to guarantee stable operation over the entire operation range.
- Lowest number of switches.
- High switching losses and relatively high filtering requirements (requires relatively large AC with damping, which adds losses). Note that filters are still much smaller than with LCC HVDC.
- High *dv/dt* because of large voltage difference at each switching, with a relatively high switching frequency and high common mode voltage. These impose high insulation requirements on the interfacing transformers, and also generate high electromagnetic interference.
- Poor DC fault ride through capability. This represents a major obstacle to the development of multiterminal HVDC, especially with the absence of reliable and proven DC CBs.

9.6.2 HVDC with Neutral Point Clamped Converter

As the second generation VSC HVDC, the three-level diode clamped converter (also known as neutral point clamped (NPC) converter) was developed around 2000, with the following objectives:

- To reduce effective switching frequency per device (consequently, lowering switching losses).
- To lower dv/dt enabling the use of a transformer with reduced insulation requirements. It also enables low total harmonic distortion at the point of common coupling (PCC) (achieves a further reduction in filter size).

Figure 9.13 shows one -phase leg of the neutral-point clamped converter, which halves the voltage stress and the effective switching frequency per device compared to the two-level converter in Figure 9.12. As an additional benefit, the converter station loss is reduced significantly. However, with the NPC converter it is difficult to meet some grid code transient requirements, for example that the converter must remain in operation during AC grid faults in order to provide reactive power to support the grid. This is an issue because the NPC converter DC capacitor voltage balancing (at ½ V_{dc}) is challenging under asymmetrical AC faults, such as a single- phase open circuit fault, single-phase-to-ground and line-to-faults.Table 9.3 Lists NPC VSC HVDC transmission installation.

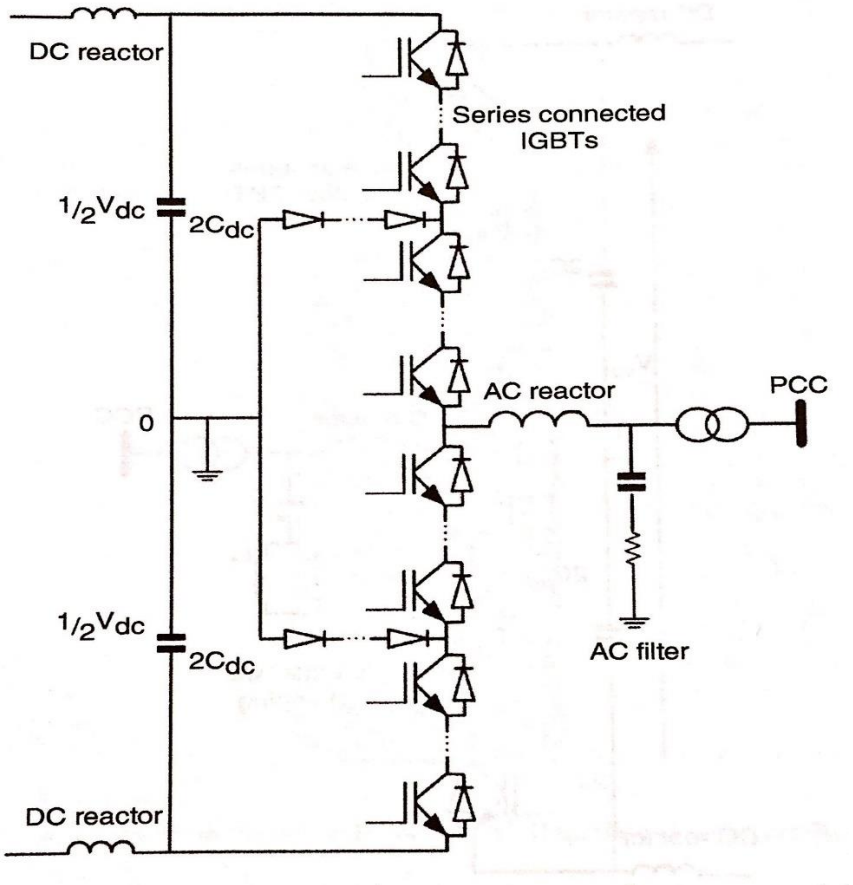


Figure 9.13 *One phase of VSC HVDC station based on the neutral-point clamped (NPC) voltage source converter.*

Table 9.3 Examples of the VSC-HVDC transmission system based on the NPC converter.

Project	Rating	PMW strategy	Applications	Distance	Commissioning Year
Cross sound (USA) cable	330 MW, V_{dc} = ±150 kV, f_s = 1.26kHz	SPWM	Grid Re-enforcement	40 Km	2002
Murray Link (Australia)	220 MW, V_{dc} = ±150 kV, f_s = 1.35kHz	SWPM	Grid Re-enforcement	180 km	2002
Eagle Pass (USA)	36 MW, V_{dc} = ±16 kV, f_s = 1.26kHz	SWPM	Power trading and power quality	Back-to-back	2000

9.6.3 Modular Multilevel Converter VSC-HVDC Transmission Systems

This converter concept exploits the benefits of the multilevel structure and PMW. The filtering requirements are greatly reduced because of the generation of high-quality AC voltage (small AC filters might be required). One cell (module) per arm is switched at a time, which results in only 1-2 kV voltage increments at each switching instant, although some topologies use cells of higher voltage. The use of a large number of levels with small voltage steps results in low *dv/dt* at each switching and reduced voltage stress on the insulation of the interfacing transformers. This allows the use of standard transformer without the need to withstand the DC link voltage or harmonic currents. Furthermore, the effective switching frequency per device is low, resulting in lower switching losses and lower harmonics. On the downside, modular converters require larger number of switches, at least twice the number compared with two-level VSC.

Figure 9.14 shows one-phase of a *n+1* level modular converter, consisting of n cells arm. This converter relies on the cell capacitors to create a multilevel voltage waveform at the converter terminal. Each cell has low voltage, which is of the order of a single switch rating or it is built up of a small number of series connected switches. Typically, hundreds of cells are required to build a single valve for DC transmission requirements. As the number of levels increases, the quality of AC voltage waveform becomes better and the harmonic content reduces. The DC link capacitors are not required as individual modules have capacitors. However, some small DC capacitors (around a few microfarads) might be installed in a typical symmetrical monopole configuration in order to create ground reference for the AC voltages. As this topology benefits from the redundant combination of module connections for each required AC level, the balancing capability is better than with NPC converters. The MMC performs better than the NPC converter during unbalanced operation and symmetrical/asymmetrical AC faults which reduces the risk of device failure and system collapse.

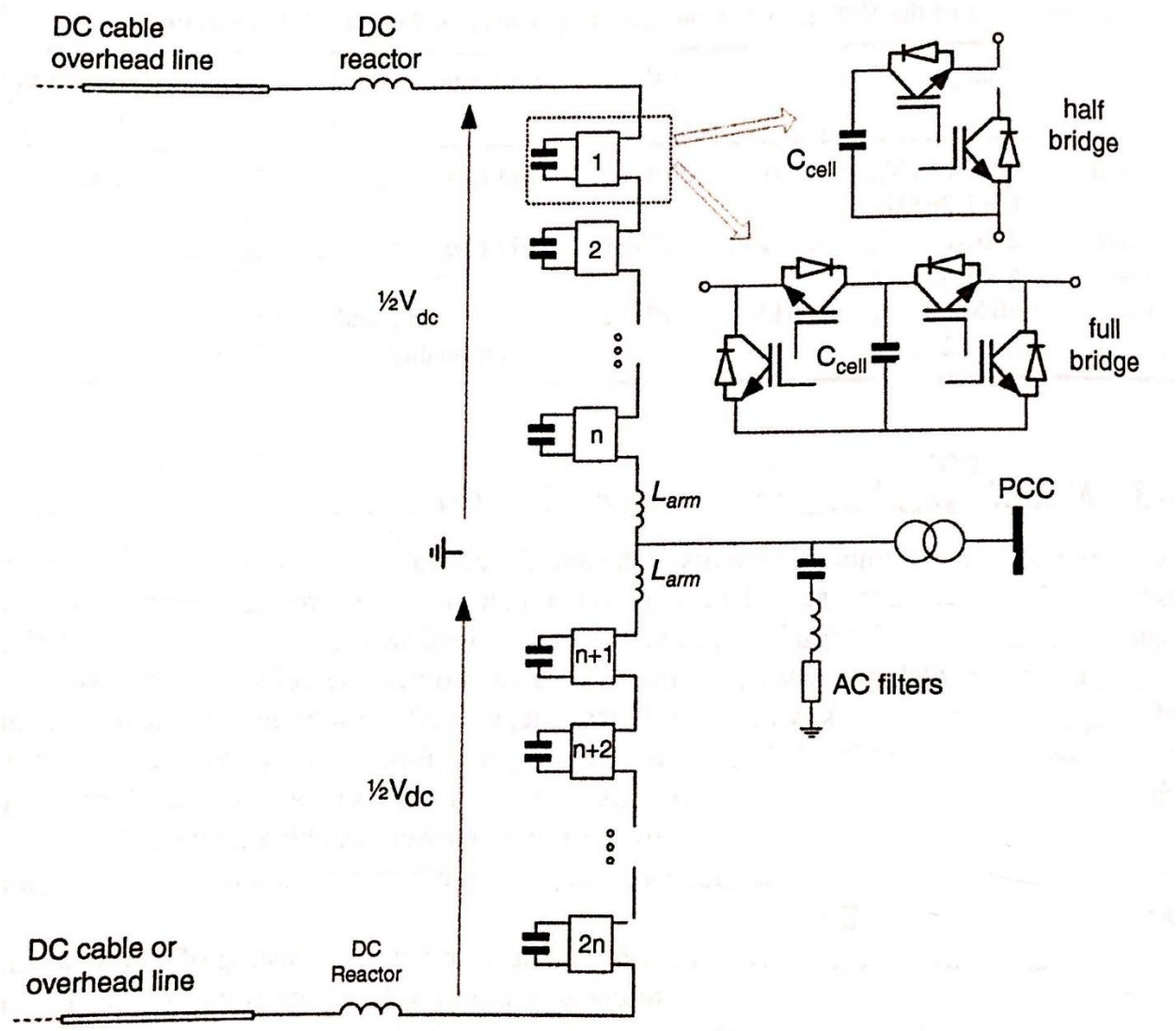


Figure 9.14 *One-phase of a n+1 level MMC HVDC converter*

The ability of the modular converter to ride through different types of AC faults makes it suitable for applications subjected to stringent grid codes requirements. If there is an issue with one phase on the AC system, the remaining two phases of the converter will operate unaffected, potentially at full per-phase power, since there is no common DC capacitor to transfer ripple between phases. The absence of DC capacitors also reduces issues with DC faults, considering that MMC cell capacitors will not discharge into DC fault and this leads to faster post fault recovery. With 2/3 level VSC, post-DC fault recovery requires a period of DC capacitor charging.

The sizing of the cell capacitors requires careful considerations. They dominate the volume requirement for the modules, but they are required to store sufficient energy to support the converter DC voltage during transient events. Otherwise the system may fail to meet transient requirements. It will be shown in the modelling section that the cell capacitors behave as series connected AC-side components.

The first commercial MMC based HVDC transmission system project is the 85 km, 400 MW, ±200 kV (±170 MVAr STATCOM functionally) Trans Bay cable project, commissioned in the United States in 2010, and some other example projects are listed in Table 9.4.

Table 9.4 Examples of the VSC-HVDC transmission system based on the MMC converter.

Project	Rating	PMW Strategy	Applications	Distance	Commissioning Year
Trans Bay (USA)	400 MW, V_{dc} = ±200 kV	MMC	Network upgrade using cable supply	85	2010
INELFE (Spain-France)	2x1000 MW, V_{dc} =± 320 kV	MMC	Interconnector between two AC system	65	2014
SylWin1 (Germany)	864 MW, V_{dc} =± 320 kV	MMC	Offshore windfarm	204	2014

9.6.4 MMC HVDC Based on Full Bridge Topology

MMC HVDC with full bridge converters is commercially available, however it has not been implemented at the time of writing. The full bridge MMC HVDC converter has similar overall structure as a half-bridge MMC, but each cell uses four switches in full H connection, as shown in Figure 9.15. The full bridge cell facilitates either positive or negative voltage at the cell terminals while the half bridge gives only positive voltage. Therefore, full bridge gives more control flexibility, although at the expense of twice the number of switches. Note that least ¾ of the (but not all) cells are required to assume full bridge topology in order to achieve system-level benefits. There are some important operational advantages of full bridge over half bridge MMC:

- Full bridge topology can actively control and interrupt DC fault current. It need not be tripped for DC faults. If it is tripped the full bridge converter become open circuit for DC faults.
- It can operate with reduced DC voltage. This implies that full bridge MMC can supply full reactive power to the AC system during DC fault conditions.
- The overrating of antiparallel diodes (which is required with half-bridge cells) may not be needed because a high fault current cannot occur. The cell design is further discussed in Section 9.7.
- Direct current voltage polarity reversal is possible. This is very important to rapidly extinguish the DC fault current path (it can deionize and extinguish arcs in the overhead DC lines as is done with an LCC HVDC in Figure 7.2). The postfault DC voltage ramp up can be controlled.
- It is possible to provide higher (typically by up to 20-30%) AC voltage for the for the same DC voltage using overmodulation feasible only with full bridge topology. This implies that for a given IGBT current and DC voltage limitation, full bridge topology can transfer more power, at the expense of increased of cells.

9.7 VSC HVDC Station Components

The basic structure of a VSC-based HVDC system station (terminal) is shown in figure 9.1. The function and design of the major components will be summarized the following sections.

9.7.1 AC Circuit Breaker.

The AC CB employed to connect and disconnect the VSC-HVDC system during normal and fault conditions. There are no special design requirements compared to normal AC CB used systems. During a DC fault, VSC converter cannot interrupt fault current, since free-wheeling diodes inside VSC converter will uncontrollably feed the fault from the AC system. Therefore, the AC CB is tripped to disconnect the HVDC terminal to prevent feeding the fault from the AC side. In the case of a temporary DC fault, power transmission can be resumed after a normal start-up sequence of the HVDC system. This can be achieved in a time-frame of a few second. (Figure 9.15 shows HVDC CB from schnidergroup)

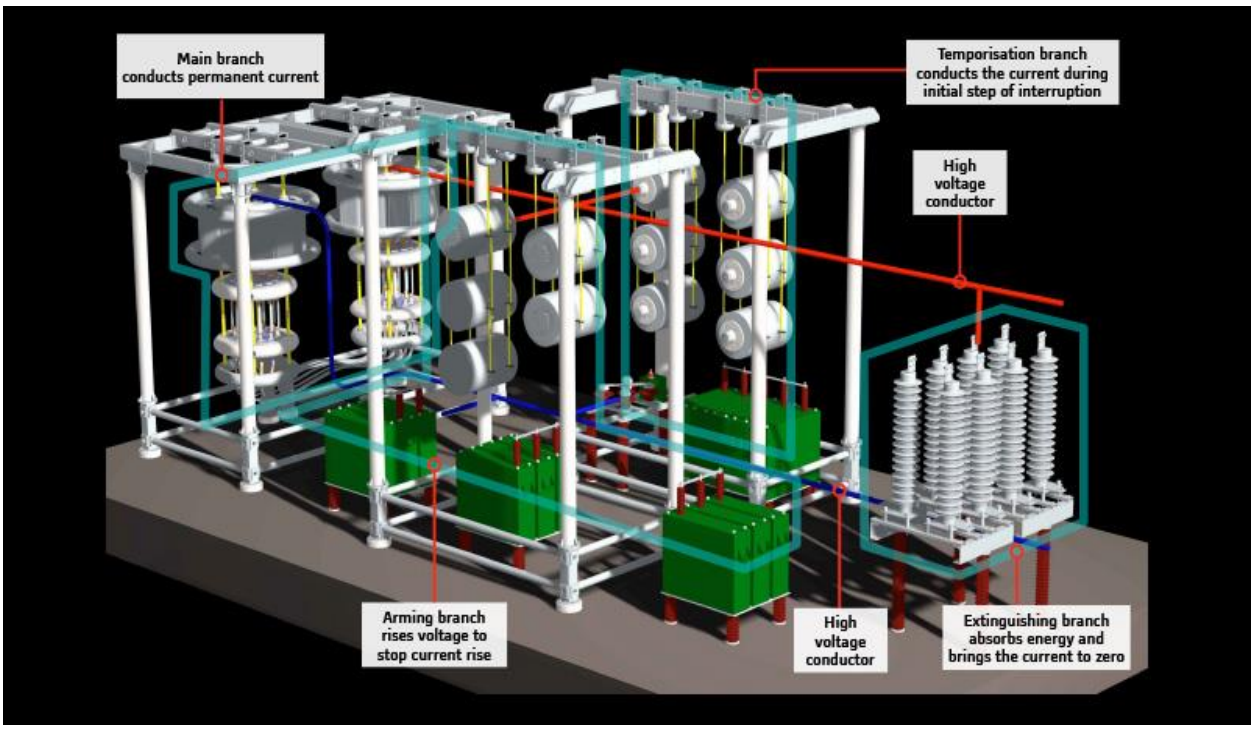


Figure 9.15 *HVDC Circuit Breaker (driving toward the super grid)*

9.7.2 VSC Converter Transformer

A three-phase 50 Hz / 60Hz converter-grade transformer with tap-changer is used (with MMC HVDC standard transformers can be employed). The converter-side voltage (filter bus voltage) is commonly controlled by the tap changer to achieve the maximum active and reactive power from the VSC, both consumed and generated. The tap changer can be located at any side though. The transformer sometimes has a tertiary winding, which feeds the station auxiliary power system and if delta connected it suppresses any core triple fluxes. With the use of the AC filter and the VSC PMW, the current in the transformer winding contains minimal harmonics and is not expected to any DC voltage. **The converter transformer can provide the following functions:**

- ❖ It provides coupling reactance between the VSC and the AC system, which also reduces fault current and can decrease size of the AC filter.
- ❖ It matches the voltage between the AC system and the VSC converter, which in turn is determined by the DC voltage. This results in optimum use of the switch ratings and DC cable insulation.
- ❖ It provides galvanic isolation, enabling optimized grounding of the DC link.

- ❖ It prevents a flow of zero sequence current between the AC system and VSC.

During the transformer design, the specific transformer requirements include.

- ✓ The fundamental current stresses;

- ✓ Saturation characteristics of the transformer magnetic field;

- ✓ Low and medium frequency harmonic stresses;

- ✓ Dielectric stresses caused by the normal/transient operating voltage especially with PWM VSC, and harmonics.

9.7.3 VSC Converter AC Harmonic Filters

Ac filters VSC HVDC converters have lower ratings than those for LCC HVDC converters and are not required to provide reactive power compensation. Contrary to filtering with LCC HVDC, VSC filters are permanently connected to the converter bus (they are not switched with power loading). A low-pass LC-filter is typically used to suppress high-frequency harmonic components and avoid interaction with fundamental frequency components. An MMC HVDC may not require AC filters.

9.7.4 DC Capacitors

The DC capacitor is the energy storage element in VSC. It provides VSC with stiff DC voltage between switching instants, which is an essential presumption with all VSC topologies**. The primary function of the DC-side capacitor is:**

- ❖ To provide a low-inductance path for switch turnoff current. Because of the stray inductance, the turnoff commutating current results in transient voltage stresses on the switching devices.

- ❖ Temporary energy storage between the switching instants, stabilizing high frequency dynamics, which allows the VSC closed loop control to adjust the control signals in lower frequencies.

- ❖ Reduce the DC voltage harmonic ripple. The HVDC capacitor commonly uses a dry, self-healing, metallized film design, which has advantages over oil-filled technologies. Dry capacitor design is safer, it offers high capacity and low inductance, in no corrosion, no radiating plastic housing.

- ❖ Decrease the harmonic coupling between different VSC substations connected to the same DC bus.

The design requirements for the DC capacitor include:

- ✓ Continuous operating DC voltage;
- ✓ The limits of DC voltage ripple under transient conditions, such as faults to the AC system;
- ✓ Harmonic current passed to the DC side;
- ✓ Peak discharge current for DC faults.

A requirement for a small voltage ripples a large capacitor. On the other hand, a small capacitor has advantages considering the control and dynamics of the converter, which result in fast active power control. Selecting the size of the DC capacitor is a trade-off between voltage ripple, lifetime, costs and the fast control of the DC voltage. Based on the ripple specification, a lower limit can be established for the capacitor value:

$$C_{dc} > (S_{VSC} / 2\omega V_{dc} \Delta V_{dc}) \quad (9.1)$$

where, C_{dc} is DC capacitance, S_{vsc} is the converter MVA rating, V_{dc} is rated DC voltage, ω is electrical frequency and ΔV_{dc} is the allowed voltage ripple (peak-peak). DC cable manufactures typically specify DC voltage ripple of around 3-10% but other limits may also apply. Based on the control speed requirements, it is possible to set the upper limit:

$$C_{dc} > (2\tau S_{VSC} / V^2_{dc}) \quad (9.2)$$

Where, τ is the time constant of DC capacitor charging. This time constant is commonly selected to be less than 10ms meet the required performance for speed of transient response.

Commonly, however, the high-power converter capacitor size is determined considering the total energy stored. The energy-to-power ratio E_s [*J / VA]* is defined using capacitor energy E_c *[J]* and the converter power S_{SVS} [*VA*]:

$$E_S = E_C / S_{VSC} \quad (9.3)$$

The energy to power ratio in practical converter is: 10 (kJ / MVA) < E_S < 50 (kJ / MVA), which is a good trade-off between harmonic penetration and control performance. Therefore, using the expression for capacitor energy:

$$E_S = (1/2) \times C_{dc} V^2_{dc} \quad (9.4)$$

It is possible to obtain a practical formula for capacitor size:

$$C_{dc} = 2S_{VSC}E_S / V^2_{dc} \quad (9.5)$$

Example 9.1

Calculate pole-neutral DC capacitor for a two-level 800 MW, 640 kV VSC.

Solution

Assuming $E_S = 20\ kJ / MVW$:

$$C_{dc} = 2S_{VSC}E_S / V^2_{dc}$$

$$C_{dc} = (2 \times 800\ MVA \times 20000J / MVA) / 640000^2$$

$$C_{dc} = 78\ \mu F$$

The required pole-neutral capacitance is 156 μF *at 320 kV DC.*

9.7.5 DC Filter

Instead of increasing the size of the DC capacitor, a DC filter can be used to eliminate the targeted harmonics, which may be injected into the DC line. It is connected in parallel to the DC capacitor to decrease the total equivalent impedance of the DC circuit. Direct-current cables naturally have a good low-frequency attenuation, but they may amplify high-frequency harmonics. In some VSC HVDC systems special high-frequency tended DC filters are installed to avoid DC-side harmonic resonance. The design criteria of the DC filter for the VSC HVDC are similar to those for LCC HVDC systems.

9.7.6 VSC HVDC Cell and Valves

IGBTs have been used in low-and medium-power applications for many years. **However, in developing high-voltage VSC HVDC converter valves, there are two new challenges:**

- ✓ A valve in VSC HVDC converter requires numerous series connected cells (or individual IGBTs with two-level designs) to achieve the required blocking voltage. Several redundant cells are typically provided in each valve chain which ensure that voltage stress is within acceptable range even when a single (or few) cells fail. When a cell fails, the valve should still be able to commutate ON and OFF. The failed cell can then be replaced at the next scheduled maintenance period. However, an ordinary IGBT will normally fail in an open circuit, which would be a dangerous valve open-circuit fault in an HVDC converter. A valve design must ensure that IGBT failure leads to short circuit across the individual cell/IGBT. During normal operation, all cells (including redundant units) in a valve are operated normally, and the presence of redundant cells means that voltage stress on all cells is slightly lower than rated valve.

- ✓ The DC fault current is much larger than the rated current. A valve design must ensure that IGBTs are not thermally destroyed under DC fault currents. Diodes take fault current, and this implies that the antiparallel diode must be rated for a much larger current than the IGBT switch.

There are two different MMC cell designs, as shown in Figure 9.16:

- Press-pack design. In this case special press-pack IGBT packing is used. The IGBTs are physically located in a string and clamped together in a manner that resembles thyristor press-pack packaging. These IGBTs are designed to always weld themselves to a permanent short-circuit fault. The IGBTs also have antiparallel diodes with higher current rating than the active switch, which allows for large DC fault current. All two-level VSC HVDC valves use this design method.
- Modular design. In this case standard commercially available IGBT switches are employed. An external thyristor is added in parallel with the diode on one of the switches, which is triggered in case of DC faults. This provides adequate total semiconductor rating for dc fault currents. An external fast vacuum switch is also added, which is closed in case of IGBT failure. This is a one-use mechanical vacuum switch, which will permanently weld its contacts, thus bypassing the IGBT in both directions if a large voltage is detected across the IGBT under a gate pulse.

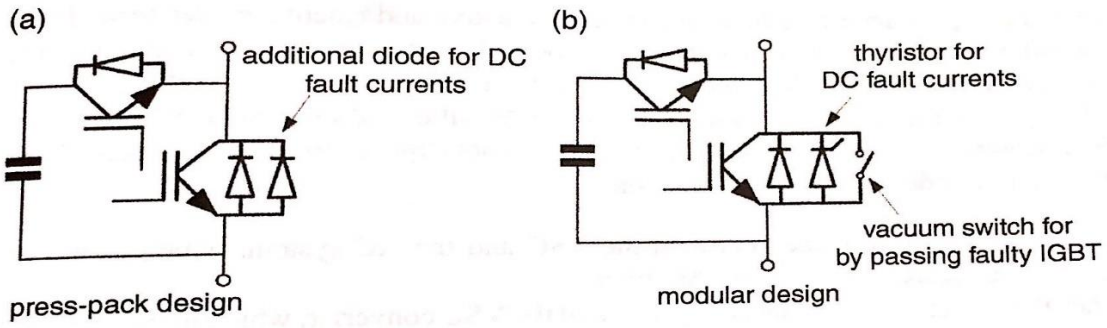


Figure 9.16 *MMC cell design.*

Some other auxiliary components are also present in the cells (not shown in Figure 9.16) like:

1. Discharge resistors, which ensure that cells are discharged 20-30 minutes after tripping converter to enable safe handling.
2. Overvoltage protection, which may require another small IGBT and a resistor.

9.8 AC Reactors

AC reactors are commonly added in series with VSC converter transformers on the converter side. They increase series reactance where it would be difficult to achieve such large transformer leakage inductance.

The main purpose of AC reactors are:

- They reduce DC fault currents. This is required to prevent over currents in diodes for DC faults, in particular with strong AC systems. The alternative is to increase diode ratings, which is costly and has size/volume implications.
- They reduce peak switch currents for AC faults. AC faults are managed by converter controls, but control delays require certain minimal AC reactance in order to limit peak transient currents to within IGBT ratings.

At HVDC power levels the inductors are always of air-core design, most often dry type but some are oil immersed. The textbook theory of electromagnetism with concentrated conductors gives good estimates

for magnetic circuits with small number of turns, whereas for large inductors with high currents experimental design formulae are usually used.

9.9 DC Reactors

In VSC HVDC systems, a DC reactor may be connected after the DC capacitor, as shown in Figure 9.12 for the following reasons:

- ✓ To reduce gradient of DC fault current in order to protect freewheeling diodes and capacitors;
- ✓ Harmonic current reduction in the DC overhead line or cable;
- ✓ Critical resonance detuning within the DC circuit.

A DC reactor in a VSC HVDC system is considerably smaller than those used in LCC HVDC schemes and typically it is below 5mH. However, the design methodology is quite similar.

The following study will present one practical approach in designing a high-power air core inductor, for either AC or DC circuit. Figure 9.16 shows the topology of a solenoid inductor. The inductance can be reasonably well estimated with the following formula:

$$L = 0.2 \times 10^{-6} \pi^2 a(2a/L_{th}) N^2 K \tag{9.6}$$

Where N is the total number of turns and K is Nagaoka's constant

$$K = \frac{1}{1 + 0.9\frac{a}{l_{th}} + 0.32\frac{t}{a} + 0.84\frac{t}{l_{th}}} \tag{9.7}$$

And where parameters are defined in Figure 9.17. The maximum value of L Equation (9.6) is obtained 2a = 3t, however this design option would lead to a densely wound coil, implying the smallest surface for heat dissipation and likely high temperature of inner turns for high-power designs. With high current designs the current density is usually taken as 1-4 A/mm^2 depending on the cooling arrangements. The cross section will be large and the wires similarly to those used with transformer designs. For high frequency applications (HF filters or DC/DC converters), Litz wire used.

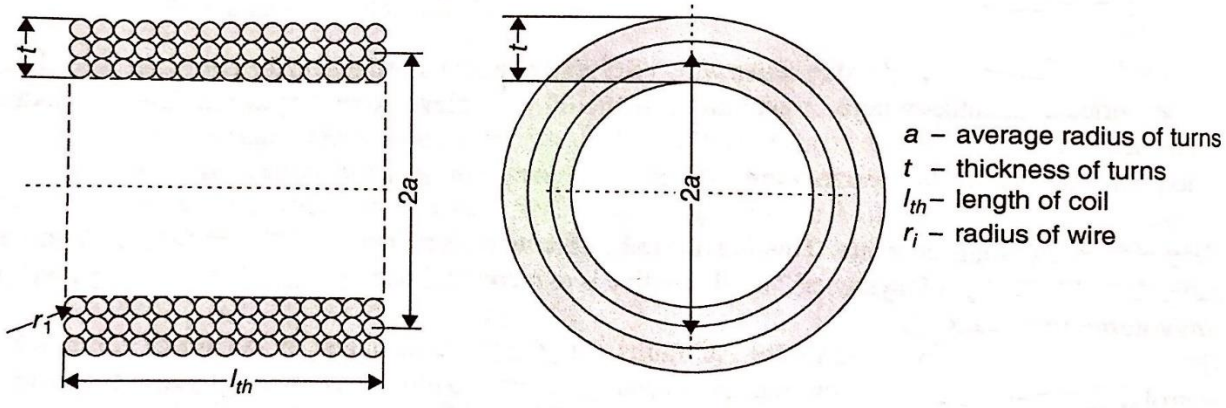


Figure 9.17 *Solenoid air-core inductor.*

The total length of wire can be determined from the above geometry of the solenoid and knowing the number of turns. Once length is known, the inductor mass can be obtained multiplying specific mass and multiplying with specific resistance to determine the total resistance.

Example 9.2

Design 200mH inductor for 1200A LCC HVDC converter. Calculate the total inductor mass, resistance and determine inductor loss assuming that copper wire is used. The density of copper is $\rho_m = 8930\ kg/m^3$ *and specific resistance* $\rho_r = 1.73 \times 10^{-8}\ \Omega/m$

Solution

Assuming that current density is $2A/mm^2$*, this gives the conductor a cross section of* $600\ mm^2$ *, or a radius of* $r_1 = 13.8$ *mm. A 10% enamel insulation thickness is also assumed. Taking the average radius of turns a = 0.918 m, with 14 layers and 25 turns in each layer (N = 350) the length is obtained* $l_{th} = 0.759m$*, with t = 0.43m, giving L = 0.193 H.*

The total length of wire is approximately 2007 m. The total mass is $M_t = 10756\ kg$ *and the total resistance is* $R_t = 0.0579\ \Omega$*. Therefore, at the rated current the total inductor loss is:* $P_{loss} = 83.347\ kw$.

10 IGBT Switches & VSC Converter Losses

10.1 Introduction to IGBT & IGCT

High-power self-commutated **v**oltage **s**ource **c**onverter (VSC) converters can be built can be using switches from one of the two power electronic device families: 1) the **i**nsulated **g**ate **b**ipolar **t**ransistor (IGBT) or **i**njection-**e**nhanced **g**ate **t**ransistor (IEGT) and 2) **i**ntegrated **g**ate **c**ommutated-**t**hyristor (IGCT), or **g**ate-**c**ommutated **t**hyristor (GCT). Although IGBTs and IGCTs are available with broadly similar voltage ratings, they represent significantly different device technologies- Insulated-gate bipolar transistors are voltage-controlled devices characterized by fast switching times and simple gate drive requirements. Individual semiconductor chip size for IGBTs is constrained, with the consequence that high-power switches consist of numerous internal parallel connected units. IGBTs are asymmetrical devices (have no reverse blocking capability) and therefore cannot be used with current source converters.

IGCT devices comprise an improved gate turn-off thyristor with an integral gate drive board. Single-chip solutions for the main power device are available to high current ranges. For a given rating, IGCTs achieve lower conduction loss than IGBTs at the expense of a large and complex gate drive, and high gate current requirements. IGCTs are also available as symmetrical devices (with reverse blocking) but such devices will have an increased ON-state voltage drop. IGCTs do not have active gate control (they are either on or off like all thyristors) and consequently are more difficult for connecting in series compared with IGBTs. Furthermore, IGCTs have lower switching speeds, consequently higher switching

losses, and for these reasons they have not been used with two-level pulse width modulation (PWM) VSC HVDC converters.

IGBT and IGCT devices are reported with maximum blocking voltage in the region of 6.5 kV, with recommended DC operating voltages between 50% and 70% of this value. The rated current of the commercially available 6.5 kV IGBT is only 750 A. Because of lower conduction and switching losses, medium voltage IGBT devices in the 3.3-6.5 kV range, are most often used in HVDC valves and have current ratings of around 1200-1500 A. These current ratings are significantly lower than those with the comparable IGCT devices.

13.2 General VSC Converter Switch Requirements

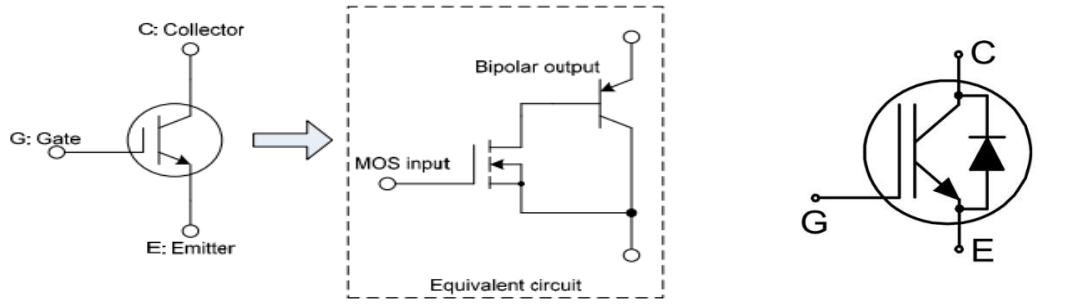
A power semiconductor switch is a component that can either conduct current when it is commutated ON or block a voltage when it is commanded OFF through a control input. This change of conductivity in a semiconductor is made possible by specially arranged device structures the control the carrier transportation. ***Generally, the following properties are important for a semiconductor switch in power conversion applications***:

- ✓ Maximum current-carrying capability;
- ✓ Maximum voltage-blocking capability;
- ✓ Forward voltage drops in ON state and its temperature dependency;
- ✓ Leakage current in OFF state;
- ✓ Thermal capability;
- ✓ Switching transition times during both turn on and turnoff;
- ✓ Capability to sustain *dv/dt* when the switch is OFF or during turnoff;
- ✓ Capability to sustain *di/dt* when the switch is ON or during turnoff;
- ✓ Controllable di/dt or *dv/dt* capability during switching transition;
- ✓ Ability to withstand both high current and voltage simultaneously (operating area);
- ✓ Ability to conduct in reverse direction;
- ✓ Low switching losses;
- ✓ Control power requirement and control circuit complexity.

10.3 IGBT Technology

The history of IGBTs started in the early 1980s but a major technological advance was made in the early 1990s when several generations of IGBT devices were developed by a number of companies. The IGBT is a voltage-controlled device from the transistor family. It can be switched on with a + 15V gate voltage and turned off when the gate voltage is zero. In practice, a negative gate voltage of a few volts may be applied during the device-off transient to increase its noise immunity. The IGBT does not require any gate current when it is fully turned on or off. However, it does need a peak gate current of a few amperes during switching transients because of the gate-emitter capacitance. Insulated-gate bipolar transistors combine the on-state voltage characteristics of bipolar transistors with the low power gate characteristics of (**m**etal-**o**xide **s**emiconductor **f**ield-**e**ffect **t**ransistor) MOSFET devices. Fast switching speeds and a near rectangular safe operating area (SOA) allow the use of IGBTs without external snubber circuits. A

circuit symbol for the IGBT is shown in Figure 10.1, where the symbols are: C-collector, E-emitter, G-gate. Figure 10.2 shown commercially available modular type IGBTs.



(a) IGBT symbol

(b) IGBT with antiparallel diode to enhance reverse current capability

Figure 10.1 *IGBT circuit symbol*

An IGBT is developed by exploiting best properties of a power MOSFET and a bipolar junction transistor (BJT), with the following advantages:

- *It has a low ON-state voltage drop and has superior on-state current density. A smaller chip size it therefore possible and the cost can be reduced.*
- *Low driving power and a simple drive circuit because of the input **m**etal-**o**xide gate **s**tructure (MOS). It can be controlled easily in comparison with current-controlled devices (thyristor, BJT) in high-voltage and high-current applications.*
- *Wide SOA. It has superior current-conduction capability compared with the bipolar transistor. It also has excellent forward-blocking capabilities.*
- *The IGBT is suitable for scaling up the blocking voltage capability. In case of power MOSFET, the on-resistance increases sharply with the breakdown voltage because of an increase in the resistivity and thickness of the drift region required to support the high operating voltage. For this reason, the development of high-current power MOSFET with high-blocking voltage rating has been abandoned. In on-state current conduction.*

The drawbacks of high power IGBTs are:

- ✓ Switching speed is lower than power MOSFET but still better than of a BJT.
- ✓ There is possibility of latch-up because of the internal PNPN thyristor structure.
- ✓ IGBTs normally fail in an open circuit, which is a significant problem in HVDC applications where numerous switches are series connected in each valve. Manufacturers have now developed IGBTs (cell assemblies) that fail in short circuits, but complexity and cost increase.

Figure 10.2 *IGBT switch modules for high-power converters. ABB*

10.3.1 IGBT Operating Characteristics

The main characteristics of IGBT s listed below:

10.3.1.1 Forward Blocking or Conduction Modes

When a positive voltage is applied across the collector to emitter terminals with the gate shorted to the emitter, the device enters into forward-blocking mode. An IGBT in the forward-blocking state can be transferred to the forward-conducting state by removing the gate emitter shorting and applying positive voltage of sufficient level.

10.3.1.2 Reverse Blocking Mode

When a negative voltage is applied across the collector to emitter terminals, the junction becomes reverse biased and its depletion layer extends. The breakdown voltage for the reverse blocking is determined by an open-base BJT. The desired reverse voltage capability can be obtained by optimizing the resistivity and thickness of the N-drift region. However reverse blocking is not required in typical VSC topologies, and reverse blocking voltage with high-power IGBT is very low (around 20V). The full output characteristic for a range of gate voltage is shown in Figure 10.3. In most commercial switches, a fast recovery antiparallel diode is integrated inside the switch module as shown in Figure 10.1. This diode is essential in all VSC applications in order to prevent destruction of IGBTs under reverse voltage.

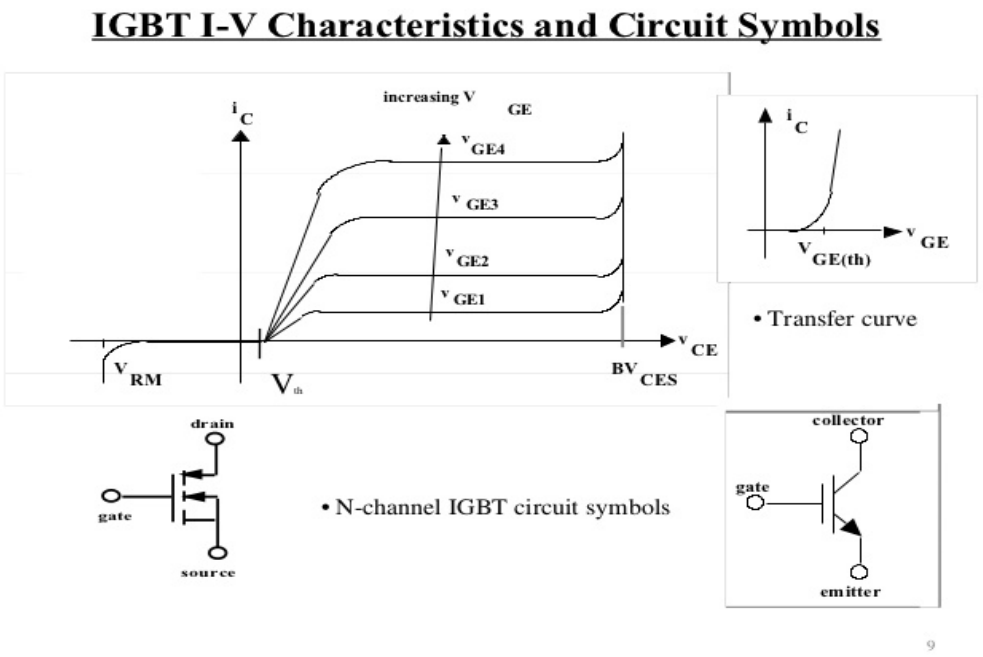


Figure 10.3 *Shape of full output characteristic of the IGBT*

10.3.1.3 Transfer Characteristic

The transfer characteristic is defined as the variation of I_C with V_{GE} values at different temperatures, namely, 25, 125 and-40°C. A typical transfer characteristic is shown in Figure 10.3a. The gradient of transfer of transfer characteristic at a given temperature is a measure of the transconductance (gf_S) of the device at that temperature. A large gf_S is desirable to obtain a high current handling capability with low gate drive voltage. The channel and gate structures dictate the gf_S value. Both gf_S and R_{DS} (*on*) (on resistance of IGBT) are controlled by the channel length, which is determined by the difference in diffusion depths of the P base and N+ emitter. The point of intersection of the tangent to the transfer characteristic determines the threshold voltage (V_{GEth}) of the device (gate voltage for switching on).

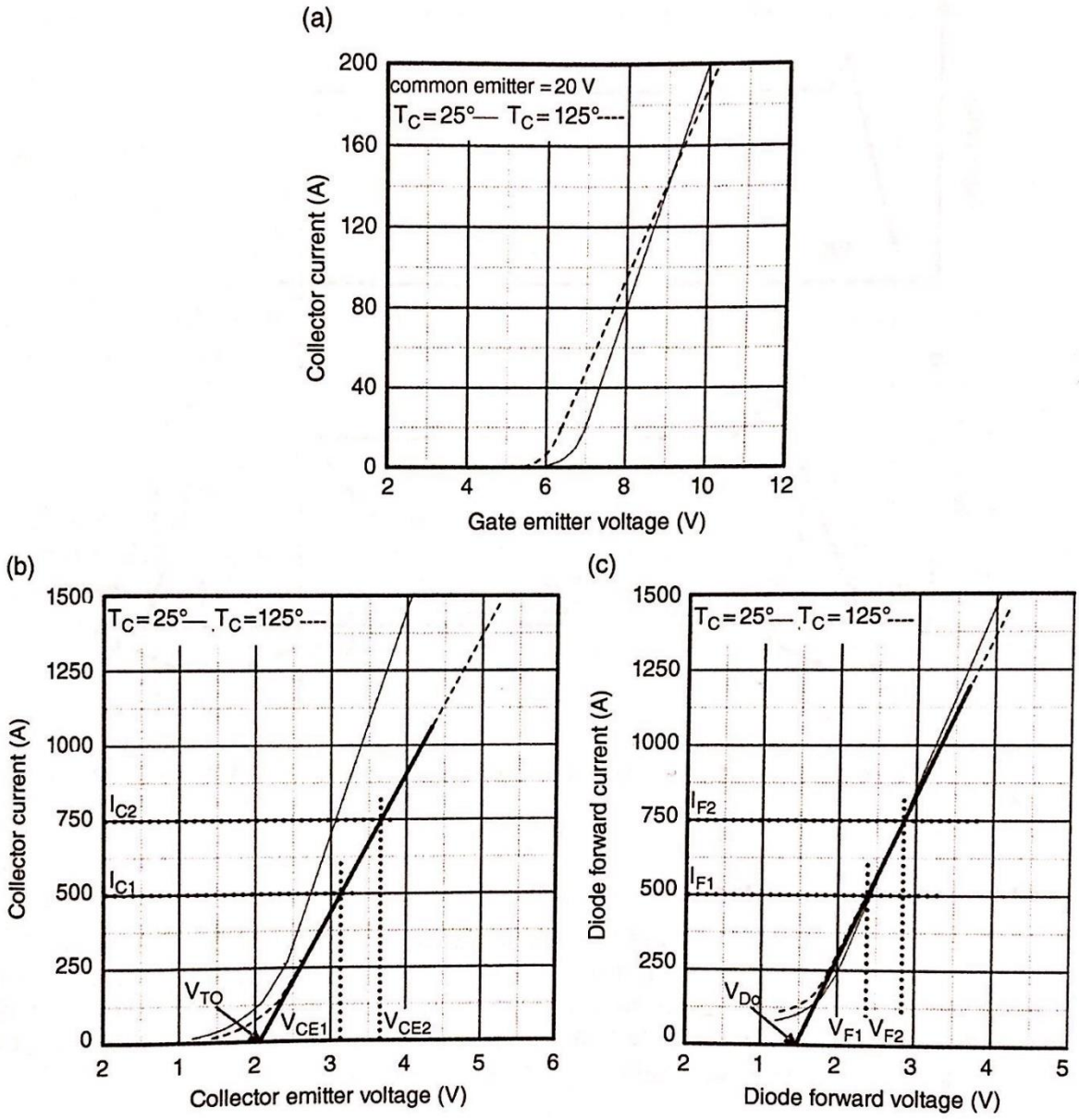


Figure 10.4 Characteristics for a typical high-power (6.5 kV /750A): (a) transconductance, (b) IGBT output characteristics and (c) antiparallel freewheeling diode ON characteristics.

10.3.1.4 Output Characteristics

The plot of a typical forward output characteristics of an IGBT is shown in Figure 10.3. It has a family of curves, each of which corresponds to a different gate-to-emitter voltage (V_{GE}). The collector current (I_C) is measured as a function of the collector-emitter voltage (V_{CE}) with the gate-emitter voltage (V_{GE}) constant. In high-power applications, the IGBT is always operated in a saturated region (operates as a switch in either ON or OFF state). Although current control is possible using the gate signal, this would lead to excessive losses. The output characteristic in saturated region is shown in Figure 10.4b. Note that gate control also enable variation in switching speed, which is very useful in balancing turn-on stress in series connected switches.

10.3.1.5 Switching Characteristics

The switching characteristics of an IGBT are quite similar to those of a MOSFET. The major differentiating characteristics is that the IGBT characteristic has a tailing collector current. The tail current increases the turnoff loss and require an increase in the dead time between the conduction of the two devices in a converter leg. Figure 10.5 shows typical IGBT device waveforms during one cycle of switching on and off, where the following parameters are defined:

Turn-on delay time ($t_{d(on)}$): this is defined as the time between 10% of gate voltage to 10% of the final collector current.

- *Rise time (t_r): this is the time required for the collector current to increase to 90% of its final value from 10% of this final value.*
- *Turn-off delay time ($t_{d(off)}$): this is the time between 90% of gate voltage to 10% of final collector voltage.*
- *Fall time (t_f): this is the time required for the collector current to drop from 90% of its initial value to 10% of its initial value.*

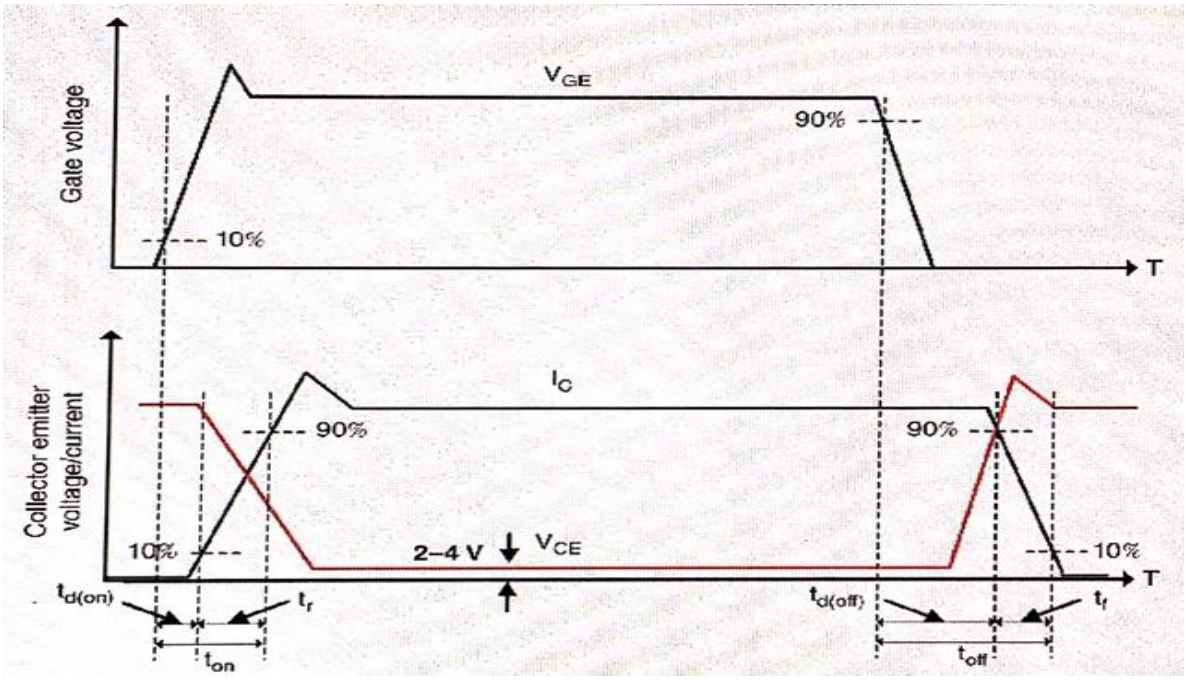


Figure 10.5 Switching waveform of the IGBT gate-emitter voltage, collector-emitter voltage and collector current.

10.3.1.6 IGBT Parameters

The following general parameters for an IGBT are introduced:

- *Maximum power dissipation (PD).* This parameter represents the power dissipation required to raise the junction temperature to its maximum value of 150^{o} C, at a case temperature of 25^{o}C. Normally, a curve is provided to show the variation of this power with temperature.
- *Junction temperature* (*Tj).* This specifies the allowable range of the IGBT junction temperature during its operation.
- *Collector-emitter leakage current (I_{CEL}).* This parameter determines the leakage current at the rated voltage and specific temperature when the gate is shorted to the emitter.
- *Gate-emitter threshold voltage (V_{GEth}).* This parameter specific the gate-emitter voltage range when the IGBT is turned on to conduct the collector current. The threshold voltage has a negative temperature coefficient.
- *Total gate (Q_G).* This parameter is important in designing a suitably sized gate drive circuit and to and to approximately calculate its losses. It varies as function of the gate emitter voltage.
- *Safe operating area (SOA).* The SOA determines the current and voltage boundary within which the IGBT can be operated without destructive failure. At low current the maximum IGBT voltage is limited by the open-base transistor breakdown. A forward biased SOA is defined during the turn on transient of the inductive load switching when both electron and hole current flow in the IGBT in the presence of high voltage across the device. The reverse biased SOA is defined during the turn off transient, where only a hole current flows in the IGBT with high voltage across it. If the time duration of simultaneous high voltage and high current is long enough, the IGBT failure will occur because of thermal breakdown. However, if this time duration is short, the temperature rise caused by the power dissipation may not be sufficient to cause thermal breakdown.

10.3.3.2 Fast Recovery Antiparallel Diode

In additional to the power switch, all self-commutating converter systems (based on voltage source principles) require a reverse current path at each switch. Commonly with asymmetrical devices, an antiparallel diode of similar rating is provided to conduct the reverse current. These devices differ from rectifier diodes in that they must be compatible with the operating frequency (in the order of kilohertz) and switching speed of the switches in the converter.

These devices must have suitably fast turn-off behaviour (good reverse recovery characteristic). Of primary interest is the reverse current that is passed by the diode and circulates in the switch, and also the transient over voltage during diode turn-off, because this same voltage is experienced on the main switch. Fast recovery diodes satisfy the above requirements but, on the downside, they display significantly higher conduction loss and reduced transient overload capability when compared to rectifier diodes. In HVDC applications, transient diode ratings are commonly a limiting factor, considering for instance DC side faults.

Recently, there have been significant developments in silicon carbide diodes which are now commercially available with voltage ratings around 1.7 kV, 10A. Although these devices offer much superior characteristics to silicon diode devices they have yet to achieve the ratings required for transmission applications. The diode reverse recovery characteristics is analysed in a similar way to the thyristor, which is studied in Part A.

10.4 High Power IGBT Devices

Table 10.1 shows technical details of some commercially available IGBTs and IGCTs for high-voltage, high current modules. This table indicates the advantage of IGCT in terms of the current rating and on-state losses. As a further comparison, a 8 kV, 2 kA phase-control thyristor (ABB 5STP 20 N8500) has only 2.2 V on state voltage.

Table 10.1 *IGBT/IGCT devices ratings for high-voltage, high-current applications.*

Device	Rated voltage (kV)	Rated current (kA)	On-state voltage
IGBT-MG1200FXF1US53 (Toshiba)	3.3	1.2	3.7 V
IGBT (ABB 5SNA 1200G50300)	4.5	1.2	3.5 V
IGBT (ABB 5SNA 0750G650300)	6.5	0.75	3.8 V
IGBT (Infineon FZ750R65KE3)	6.5	0.75	3.7 V
IGCT (ABB 5SHY 35L4522)	4.5	4.0	1.8 V

The high current IGBTs use multiple *p-n* junctions in parallel inside a device to achieve high current ratings. The positive temperature coefficient and the use of single driver enable internal paralleling. Note, however that paralleling at device level is not normally used, and the maximum current ratings are not likely to increase much beyond 1.5 kA. If higher current is required for an HVDC terminal, then complete VSC converters can be connected in parallel.

IGBT technology requires significantly more silicon surface area for a given current rating than IGCT technology because of the parallel connection of multiple devices in press-pack IGBTs. This brings some advantage since there is more surface area available for cooling though this has to be balanced against the increased conduction loss.

High-power IGBTs are available in press-pack and single-sided modules, as discussed with cell design in Figure 9.16. Insulated-gate bipolar transistor press-pack technology brings the same advantages as press pack thyristor as it provides an opportunity to cool the IGBT devices on both sides thereby improving heat dissipation and reducing junction temperatures. Press pack IGBTs can be mechanically configured to fail in a short circuit. The design requires paste, foil or component that melts and fuses with the silicon wafer and the pressure plate contact. Under fault current conditions, this material creates a low-resistance conducting path (a short circuit) between the external collector and emitter terminals of the device. This device design is employed by some HVDC manufacturers.

A conventional module package IGBT technology is also employed with some VSC HVDC. In case of device failure, the fault current breaks the bond wires and the device will fail to an open circuit. When this switch is employed in HVDC valves, a specially developed parallel bypass vacuum switch is used to provide current continuity in case of a switch failure. This is discussed with cell analysis in Section 9.7.

10.5 IEGT Technology

Some manufactures have made IEGT available. It represents improved IGBT technology for medium-voltage applications. By optimizing the gate structure, it is claimed that the IEGT achieves a reduction in both on-state voltage and switching loss. A 42 chip, 4.5 kV, 5.5 kA press pack IEGT is manufactured in both press pack and single sided modular version.

10.6 Losses Calculation

This section will review the different loss components occurring in VSC semiconductor devices.

10.6.1 Conduction Loss Modelling

Conduction Losses occur because of the voltage drop across switching devices during conduction, similarly as discusses with thyristors. The voltage V_{FT} is a function of the current, and can be approximated by:

$$V_{FT} = V_{To} + r_{FT} i_{ce} \tag{10.1}$$

Where V_{T0} is the forward voltage drop across the device at no load, r_{FT} is the on resistance of the switch and i_{ce} is collector emitter flow through the device during conduction.

A typical output characteristic for the high-power IGBT is shown in Figure 10.4b. The values of V_{T0} and r_{FT} can be obtained from this output characteristic as follow:

$$r_{FT} = \frac{\Delta V_{CE}}{\Delta I_{CE}} = \frac{V_{CE2} - V_{CE1}}{I_{CE2} - I_{CE1}} \tag{10.2}$$

Using EQS (10.1) and (10.2), the conduction loss is calculated as

$$P_{cT} = \frac{1}{T}\int_0^T V_{FT} i_{ce} dt = \frac{1}{T}\int_0^T [V_{To} + r_{FT} i_{ce}] i_{ce} dt = \frac{1}{T}\int_0^T V_{To} i_{ce} dt + \frac{1}{T}\int_0^T r_{FT} i_{ce}^2 dt \tag{10.3}$$

$$P_{cT} = V_{To} I_{avT} + r_{FT} I_T^2 \tag{10.4}$$

Where T is fundamental period, I_{avT} and I_T are the average and RMS currents in the switching device over one fundamental period.

Similarly, the antiparallel diode conduction losses can be calculated as:

$$V_{DT} = V_{Do} + r_{FD} i_d \tag{10.5}$$

Where V_{Do} is the forward voltage drop across the device at no load, r_{FD} is the on resistance of the diode of the diode and i_d is current flow through the device during conduction. Therefore, the diode conduction loss is:

$$P_{cD} = \frac{1}{T}\int_0^T V_{FD} i_d dt = \frac{1}{T}\int_0^T [V_{D0} + r_{FD} i_d] i_d dt = \frac{1}{T}\int_0^T V_{FD0} i_d dt + \frac{1}{T}\int_0^T r_{FD} i_d^2 dt \quad (10.6)$$

$$P_{cD} = V_{Do} I_{avD} + r_{FD} I_D^2 \quad (10.7)$$

The values of V_{Do} and r_{FD} can be obtained from the diode specific output characteristics (Figure 10.4c) with the same calculation method in Eq.(10.2). Note that diodes will have ON-state characteristics different from IGBTs.

10.6.2 Switching Loss Modelling

The switching losses in semiconductors such as the IGBT can be divided into two components:

- *Turn-on switching loss (E_{on})* is the total energy lost during turn on of an inductive load. In practice, it is measured from when the collector current begins to flow to when the collector-to-emitter voltage completely falls to zero (ON-state level) in order to exclude any conduction loss.
- *Turn-off switching loss (E_{off})* is the total energy lost during turn off of an inductive load. In practice, it is measured from when the collector-emitter voltage begins to rise from zero (ON-state level) to when the collector current falls to zero.

The total switching loss in one cycle is the sum of the E_{on} and E_{off}. In all VSC HVDC converters, the switching losses can be substantial and must be considered in the thermal design. The switch and antiparallel diode should be considered separately but note that diode turn-on loss is typically neglected.

The average switching losses in the IGBT can be computed using:

$$P_{swT} = f_s(E_{on} + E_{off}) \quad (10.8)$$

Where f_s is the switching frequency. E_{on} and E_{off} represent energy loss a single event at voltage V_{CE} and current I_C. They can be calculated as:

$$E_{on} = E_{on\_test} \frac{V_{CE}}{V_{CEtest}} \frac{I_C}{I_{Ctest}} \quad (10.9)$$

$$E_{off} = E_{off\_test} \frac{V_{CE}}{V_{CEtest}} \frac{I_C}{I_{Ctest}} \tag{10.10}$$

Where E_{on_test} *and* E_{off_test} are the switching losses manufacturers sheets I_{Ctest} and V_{CEtest}.. Figure 10.6 shows the tests.

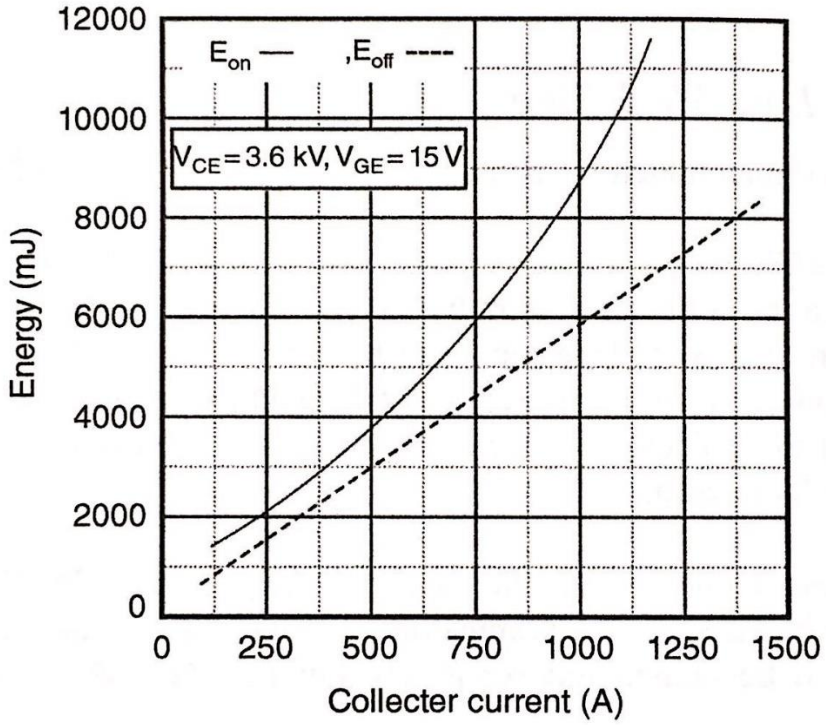


Figure 10.6 *Switching energy characteristics for the test IGBT.*

The switching in the antiparallel diodes is primarily the reverse recovery loss:

$$P_{swD} = f_s E_{rec} \tag{10.11}$$

$$E_{rec} = E_{rec\_test} \frac{V_{DC}}{V_{DCtest}} \frac{I_C}{I_{Ctest}} \tag{10.12}$$

Where E_{rec_test} is the loss at test conditions which is shown in Figure 10.7 for the test diode.

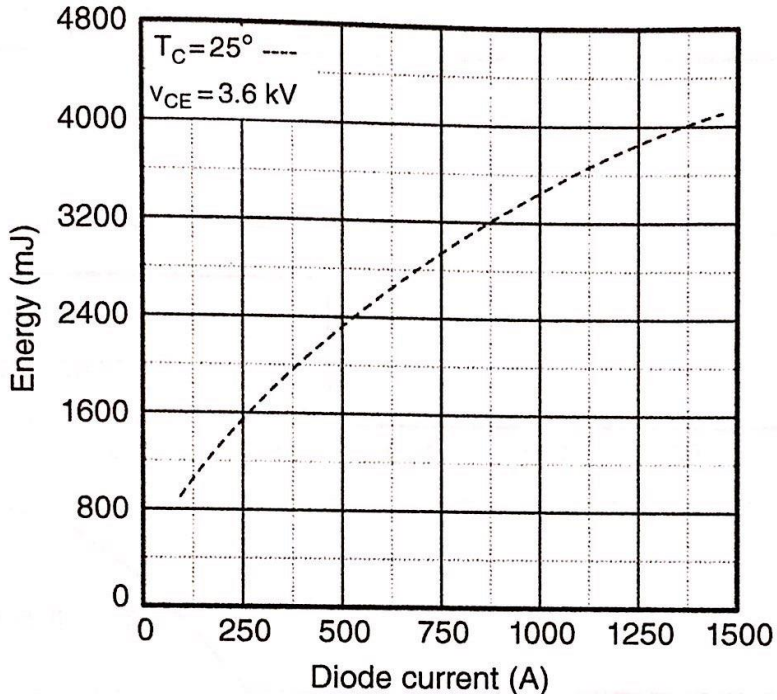


Figure 10.7 Reverse recovery energy characteristics for the antiparallel diode in the test switch.

10.7 Balancing Challenge in Series IGBT Chains

At present, the voltage ratings of IGBT devices are limited to 3.5-6.5 kV, depending on required current and there is little scope for significant increase in these figures. For HVDC converter applications, a series connection of devices or cells is required in order to achieve the necessary operating voltage . In case of two-level pulse width modulation converters, each valve should be rated for full DC voltage. Up to 200 series connected IGBTs have already been used in HVDC installation.

It is required to balance the switch voltage in a valve in conduction (static) and during switching (dynamic balancing). Static balancing is resolved using large resistors in parallel R_g (grading resistors similarly as with thyristor chains) with each switch in the chain as shown in 10.8. This in turn increases the power loss. Dynamic balancing is a more difficult issue because of very short time frames for the switching transients. If dynamic balancing is not used then the switch that turns off first (or turns on last) would have to sustain full valve voltage . The problem is normally reduced by the use of snubbers, which slow down the switching process at the expense of additional costs and reduced efficiency. Another more commonly

used solution is to control actively the switching speed in IGBTs. As transistors have capability of active control of emitter current, the gate voltage can be regulated in fast local (driver-level) feedback loop to make minor adjustments during the switching interval in response to on-line voltage measurements. This method is also called asynchronous firing control. Figure 10.9.

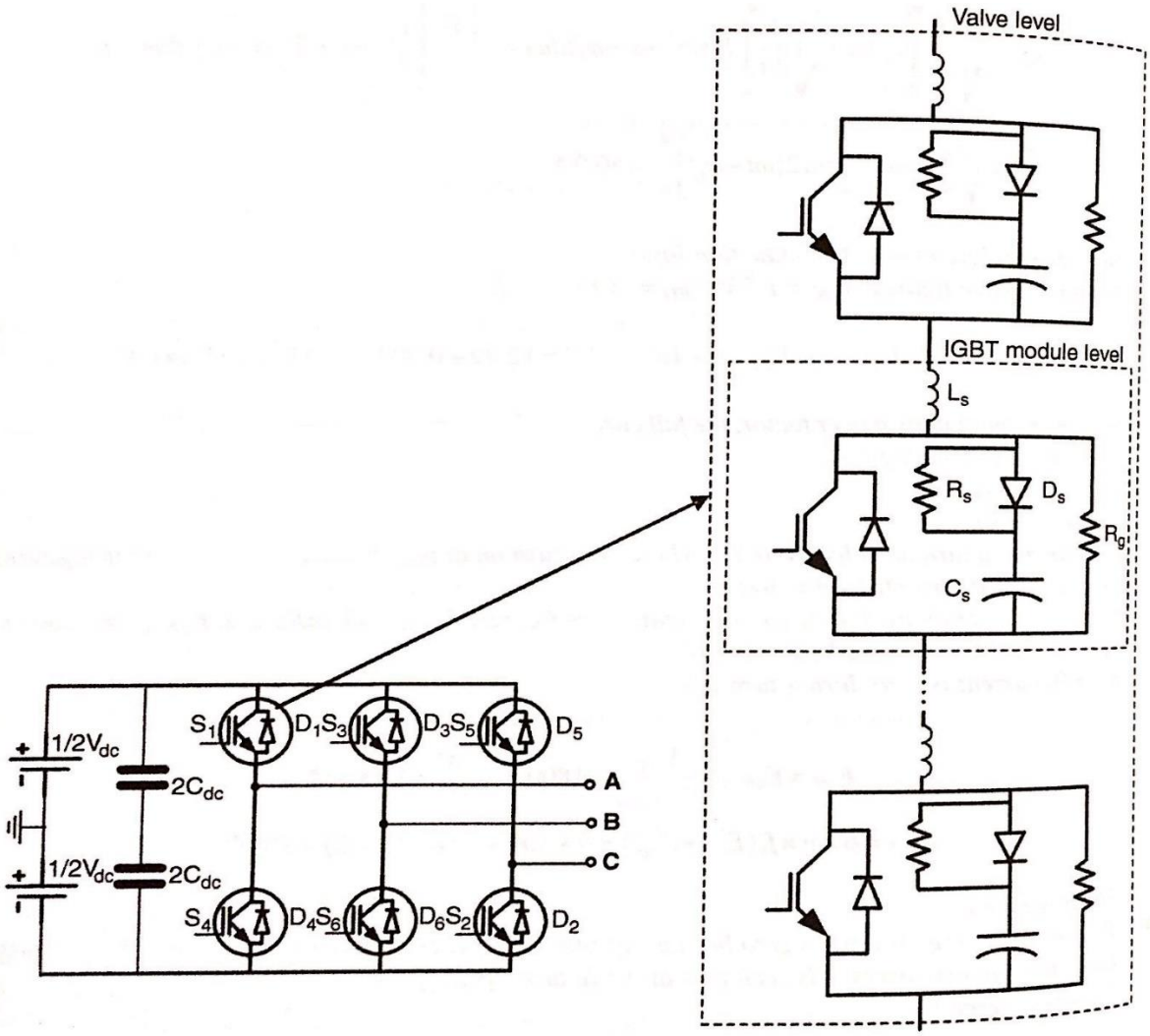


Figure 10.8 VSC with RCD voltage clamp snubbers for *dv/dt* protection, and L_S for *di/dt* protection.

The emergence of multilevel topologies eliminates / reduce the need for series connection of switches and can provide more cost-effective solution because cells in a valve switched on a time.

10.8 Snubbers Circuit

Snubbers are used to protect the semiconductors from the voltage and current transient stress that occur during the turn-on and turn-off switching events. They limit the voltage and current magnitudes as well as their rates of rise. The reduction of *dv/dt* and *di/dt* also lowers the electromagnetic interference (EMI)

levels. Snubber circuit can also help in reducing the static and dynamic balancing problem, but they add complexity and may increase the power losses.

Snubbers will shift the switching losses from the silicon to a low-cost passive component where it can be dissipated further away from the main switching device or recovered back into the supply or load. The reduction in losses in turn results in lower junction temperatures. Thus, for a given rating, snubbers may allow the use of higher switching frequencies.

IGBT snubbers are required to limit the switching overvoltage that occurs because of the wire inductance between the IGBT and the DC capacitor. Different snubber configurations can be used in VSC-converters. The resistor-capacitor -diode (RCD) voltage clamp snubber, as shown in Figure 10.8, is preferred over resistor-capacitor (RC) snubbers for medium and high-current VSC applications because it gives reduced losses in the snubber resistor. Also, a small inductor (L_S) may be added in series with the switch in order to limit the *di/dt* for transient turn-on voltage protection.

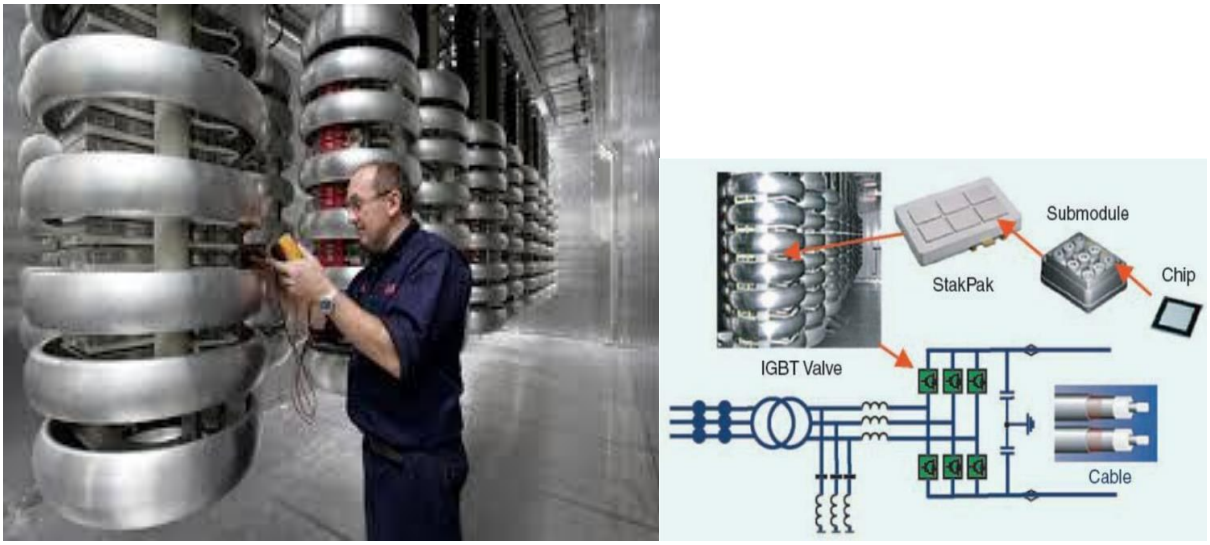


Figure 10.9 Testing VSC HVDC Rectifier Station IGBT Valves on BorWin 1 project from ABB.

Reference Part B

Voltage Source Converter HVDC

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Part C DC Transmission Grids

11 Introduction to DC Grid

11.1 DC versus AC Transmission

Transferring electrical power between two location some distance away can be achieved using direct or alternating current. Considering only power transfer at a single voltage level, DC power transmission considerably better than AC, ***and the main advantages of DC include*:**

- Higher power transfer (up to 30%) for the same copper size and same insulation level. The AC cables must be insulated for peak AC voltage, but power transfer is related to the RMS value of voltage.
- The losses of AC current (RMS value I_g) are equal to losses of the same magnitude of DC current ($I_{dc} = I_g$). However, AC current will contain active current (which determines power transfer) and also reactive current. As it is impossible to eliminate reactive current circulation completely, the losses with AC transmission will always be larger. Therefore, DC cables have smaller copper size and smaller insulation.
- The AC current is pushed toward the surface of the conductor and the skin depth at 50 Hz is around 9 mm. This increases losses therefore the cross section of AC cables limited while DC cables have no limitation in size except for the thermal management.

As consequence of smaller wires/cables, the support towers (pylons) and transmission corridor (right of way) are smaller with DC transmission.

The reactive current circulation is the central issue with AC transmission. It deepens on the voltages at the line ends but also on the line impedance. Transmission lines have dominant inductive reactance whereas cables have large capacitive reactance, which depends on the length. These reactance's will, in either case, cause reactive current circulation if the AC current is transferred. The reactive current may become very large - even larger than the active current - and beyond a certain length AC power transmission may not be possible. In the case of long AC lines, the voltages at the line ends must be kept constant within a very narrow range to enable to enable decent utilization of the lines thermal rating. The problem is particularly difficult with varying loading, in which case long AC cables may require power electronic systems (like Static VAR Compensators or static synchronous compensators (STATCOMs)) to keep AC voltages constant, or power electronics controllers for line impedance like thyristor-controlled series capacitors (TCSs).

The main *disadvantages* with DC transmission are related to fault isolation in networks. This required for system reliability. Voltage stepping is also complicated DC systems. Alternating current transmission has been the dominant technology for power transmission and distribution networks because of the simplicity of voltage stepping and fault isolation, which is achieved with inexpensive electro-mechanical components (transformers and circuit breakers (CBs)). In DC systems, it will be necessary to use power electronics for the components required for DC fault isolation and DC voltage stepping. While this implies higher costs, it also brings many performance benefits and operational flexibility.

11.2 Terminology

High voltage direct current (HVDC) transmission is the term used solely for a two-terminal system. It can assume monopolar or bipolar configuration, but power is exchanged between only two AC terminals/systems. The power is same at each terminal and it is coordinated.

Tapping on HVDC involves a small third terminal (or ,more terminals) along the HVDC lines. The tap terminal is very small compared with power level of the main HVDC line and the main HVDC needs no control modifications. No HVDC tap has been implemented but substantial demand exists, and many studies have been completed. In particular, with very long HVDC lines passing close to communities with no access to power (Itaipu HVDC, Nelson River HVDC, etc), HVDC tapping becomes an attractive option.

Multiterminal HVDC signifies a DC system of more than two terminals arranged along a single HVDC line. There are no meshed lines. If a DC line is in fault, there will be loss in power-trading capability. Typically, a multiterminal HVDC will have a single protection zone, which implies the whole system for any DC fault. However, DC line protection may be implemented on larger systems in order to isolate the smallest faulted segment in case of DC faults, thus allowing the remaining part to operate normally. There is a single DC voltage level. Control system will be different from HVDC controls because power balancing within the system is required.

Normally, there is no possibility for adding further terminals, unless substantial redesign is undertaken. Multiterminal HVDC has been implemented both with line-commutated converter (LCC) and voltage-source converter (VSC) HVDC and new projects are in the planning/design stages.

DC Grid denotes a DC transmission system of more than two terminals with at least one meshed DC line. With DC grids there are multiple power-flow paths between two grid terminals. Power flow between two DC grid terminals may not be affected (or partially affected) by tripping a single DC line. DC grids will require some protection technology in order to isolate faulted lines/units allowing remaining part of the grid to continue power transfer. Tripping whole DC grid will not be allowed. Multiple nominal DC voltage levels may exist. Normally, any number of new terminals can be added to an existing DC grid. The control system will be considerably more complex than with two-terminal HVDC.

Node in a DC grid is any station where two or more DC lines connect.

Terminal is a DC grid station where power is exchanged between DC grid and a n AC system or another DC system (for example, when a DC/DC converter two DC systems). A terminal is a node with a converter.

11.3 DC Grid Planning, Topology and Power-Transfer Security

The primary motivation for DC grid development is the need to interconnect multiple HVDC Links Located in close proximity, and to enable power trading between all DC terminals. This brings benefits of better utilization of assets, better reliability and security of power transfer, better efficiency, enhanced power trading and operating flexibility, and all the advantages of interconnected systems (reserve sharing, control, etc.). The principle application drivers arise from the initiatives like the North Sea DC grid, Medtech, Desertec, European overlay Super grid and Atlantic wind.

It is expected that future DC grids will have similar level of security, reliability and performance as the existing AC grids. Although DC gird codes do not exist at present the underlying principle of power trading, market access, security in power transfer and performance will be based on AC grid codes. The common *n*-1 criterion (unaffected power transfer for loss of any single component) with AC systems is a valid expectation but an *n*-2 or higher criteria would require significant capital investments because of

high costs of converters and DC grid components. Note that no has been used with traditional HVDC (except at valve and control levels). On the other hand, if a bipolar DC grid is built with neutral return than there is an option to operate terminals at 50% power in case of a DC cable outage. This is different from AC systems where a line fault (any line in a three-phase system) is always a circuit outage. A bipole is also different from an AC double circuit and requires considerably lower investment.

It is important that a DC grid provides access to all market participants, including renewable energy sources and this complicates regulatory aspects and imposes some high technical demands on the grid. The technical requirements for new entrants will also include stringent speculations (Likely more demanding than with AC grids) in order not to disturb the DC grid under all foreseeable scenarios.

The rating of DC grid terminals will be dictated by the cable capacity but also by the operating codes of the AC grid where the terminal connects. The maximum acceptable single-unit loss is defined by the secondary reserve, which is different for each country. As an example it is 1500 MW in France , 1800 MW in the United Kingdom and 1300 MW in spain.

Ideally, terminal control should be able to separate/isolate disturbance on AC side from those on DC grid. A VSC terminal will also be will also be expected to contribute to system stabilisations on DC and/or AC side, which will present a major technical challenge and requires careful planning of DC and AC grid codes.

11.4 Technical Challenge

Direct-current grids will require substantial technical advances from the existing HVDC technology. The main challenges include DC grid protection and DC grid control:

11.4.1 DC Grid Protection

Developing both: DC protection components and protection system is much more challenging compared with AC systems. A DC fault current has no zero crossing and therefore DC CBs are more complex. The protection coordination at grid level will be very challenging because the absence of reactive impedance on DC cables introduces complexities in finding the location of DC faults. The protection trip decision time window should be shorter than with AC systems. The overcurrent and overvoltage capability of DC grid components is lower than with AC grids.

11.4.2 DC Grid Control

Direct current grid dynamics are an order of magnitude faster than dynamics of AC systems, and converters can respond two orders of magnitude faster than electromechanical AC components. There is no inertia or any energy storage in DC systems and therefore energy balancing must be fast. Contrary to a unique frequency value across the whole AC system, DC voltage will be different at each terminal and cannot be used as a definite power balance indicator. Voltage-source converters are quite sensitive to DC voltage excursion and very fast DC grid control is essential. A VSC converter must be tripped if local DC voltage drops below 80-85%.

11.5 DC Grid Building by Multiple Manufactures

High-voltage direct-current systems are commonly developed by a single vendor coordinating works, perhaps with local suppliers. The technology is optimized and various subsystems (protection, control, value design, etc.) are interdependent within HVDC topology for each different HVDC supplier. In only a few cases of HVDC station refurbishment, a vendor has been different from the supplier of the original equipment. In several other cases, the two poles in a large bipole HVDC have been built by different vendors. These are exceptional cases while in general there is no interoperability between inner HVDC subsystems or units by different supplies.

Development of DC grids will involve multiple manufactures. This is an essential requirement to facilitate proper functioning of the new market, to ensure public and political support and to establish competition, which lead to better performance. If a complete terminal is developed by a single manufacturer there is still a significant challenge to integrate such a terminal into an existing Dc grid that might contain terminals by several other manufacturers. Considering interoperability al lower component levels, for example interchangeable DC CBs by various manufacturers, there is need for substantial further work on standardization.

The development of DC grid codes and, in particular, international codes is essential to enhance interest in connecting to DC grids by various new, which in turn will underpin DC grid development in the power industry.

11.6 Economic Aspect

A DC grid must be economically viable. The initial capital investment is likely to be higher than AC grid options (where technically feasible) because of high converter capital costs. However, cost of DC lines/cables is generally lower than comparable AC lines. The lower DC grid losses should be considered in the long-term studies of return on investment. The control of power flow will be much better much better in DC grids, which will enable better utilization of lines (closer to thermal limits) and which can eliminate problems of loop flow or overloading/underutilization of lines as experienced in AC grids.

The topology of future DC grids is not certain and different protection/control approaches are favoured by the main manufacturers. The grid planning will be a complex process considering technical performance, market aspects, security, reliability, safety. Environmental considerations, economics and other factors. As a rough initial guide, **Table 11.1** provides cost comparison for the basic building blocks of DC grids. Only the AC/DC VSC converter cost (assumed 1 pu) can be regarded as reliable because it is based on numerous existing projects and it has been publically endorsed by the Conseil International des Grands Reseaux Electriques (GIGRE). The DC cable cost is also derived from the public data on the recent HVDC projects. The other costs are estimates without market experience and based on relative comparison of components with VSC converters. Note that the additional costs of offshore installations for converters should also be considered, if applicable.

Table 11.1 Estimated cost of DC grid components.

Component	Cost (M€/MW)	Cost for 1 GW
AC/DC VSC converter	0.11 (1 pu)	110 M€
Hybrid DC CB (unidirectional)	0.25-0.35 pu	27-38 M€
Mechanical DC CB	0.002-0.005 pu	0.23-0.55 M€
DC/DC converter (low stepping ratio)	1 pu	110 M€
DC/DC converter (high stepping ratio)	1.5-1.8 pu	165-200 M€
DC-hub (multiport IGBT-based DC/DC)	0.8-0.9 pu/port	88-100 M€ $/port$
Offshore platform for VSC (wind farm)	1.2-1.5 pu	130-165 M€
DC cable (pair)	0.13 pu/km	140 M€ $(\boldsymbol{for\ 100\ km})$

12 DC Grids with Line-Commutated Converters

12.1 Multiterminal HVDC

The multiterminal high-voltage direct current (HVDC) has been studied since the first HVDC installation in 1950s but very few systems have been implemented. Numerous incentives exist for connecting a third terminal to an exiting HVDC system, in particular when the DC line is long or when it passes close to load/generation centres.

There are two possible approaches in developing a multiterminal line-commutated converter (LCC) HVDC system: parallel and series connection, as schematically illustrated in **Figure 12.1**.

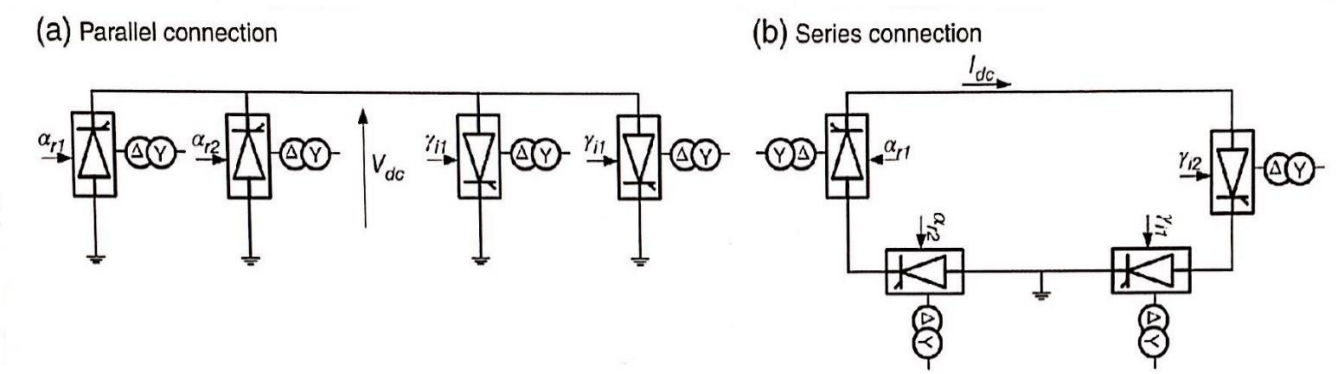

Figure 12.1 Four-terminal LCC HVDC in parallel and series connection.

Some basic properties with parallel multiterminal HVDC system are:

- ✓ All terminals have the same DC voltage and it is assumed that DC voltage is tightly controlled.
- ✓ DC voltage is not allowed to change polarity. Note that some small systems (three terminals) can be configured to change DC polarity simultaneously on all terminals.

- ✓ One terminal controls DC voltage and all the other terminals regulate local DC current. The current-controlling terminals should also have DC voltage support function through local droop feedback.

- ✓ As all terminals are rated for full DC voltage, the low power terminals will be costly.

- ✓ A DC voltage fault (or a converter fault) will imply power interruption on all terminals.

- ✓ A commutation failure at any terminal implies DC voltage collapse and power interruption on all terminal.

- ✓ All terminals will operate with larger (ignition or extinction) angles in order to provide adequate control margin. This implies larger reactive power consumption, harmonics and switching losses.

- ✓ Fast power reversal is not possible at any terminal (as this would require voltage polarity reversal). Special mechanical switches may provide slow offline power reversal. Alternatively, at higher costs, bidirectional thyristor valves can be employed for fast current polarity reversal.

The basic properties of series connected multiterminal HVDC are:

- ➢ All terminals have the same DC current. The DC current should be kept at a rated value at all times in order to provide full power control capability at all terminals. This implies large losses at partial loading.

- ➢ One (large) terminal controls the DC current and all the order terminals control local DC voltage. Small terminals will use low voltage rating, which has cost benefits.

- ➢ The DC voltage insulation will be unequal, dependent on operating conditions and complicated. It is likely that all segments will be insulated for highest DC voltage in order to provide operating flexibility when some terminals are out of service. This implies that costs will be similar as in a parallel connection.

- ➢ A commutation failure on any terminal implies only local power interruption, while all other terminals will operate normally. This is a major advantage of series connection.

- ➢ DC-side faults can be managed as partial power interruption.

- ➢ Power reversal on each terminal is readily achieved with independent reversal of local DC voltage, but restrictions may apply. No additional equipment is required.

It is generally accepted that in a typical high-power transmission application a parallel multiterminal connection is, overall, more attractive. A series connection might be suitable in case of small taps.

12.2 Italy-Corsica-Sardinia Multiterminal HVDC Link

The Italy-Corsica-Sardinia HVDC is the only multiterminal HVDC with long operating experience and it will be analysed in some depth. Note that the Quebec-New England HVDC has been designed as a multiterminal system, but it does not have significant operating experience in multiterminal configuration. It is mentioned that the Indian four-terminal North-East Agra project should be commissioned in 2015.

The top-level schematic of the Italy-Corsica-Sardinia HVDC is shown in **Figure 12.2.** The Corsica converter was installed at a later stage with the intention not to disturb the operation of the main Italy-Sardinia link. The main operating mode of this link is the frequency control of Sardinia system. This implies that power transfer is highly variable (DC voltage is kept constant) and fast power reversal is feasible within 300 ms, which makes it difficult to add new terminals. Also, DC current on the main line is variable, and this has further eliminated the possibility of a series tap at Corsica.

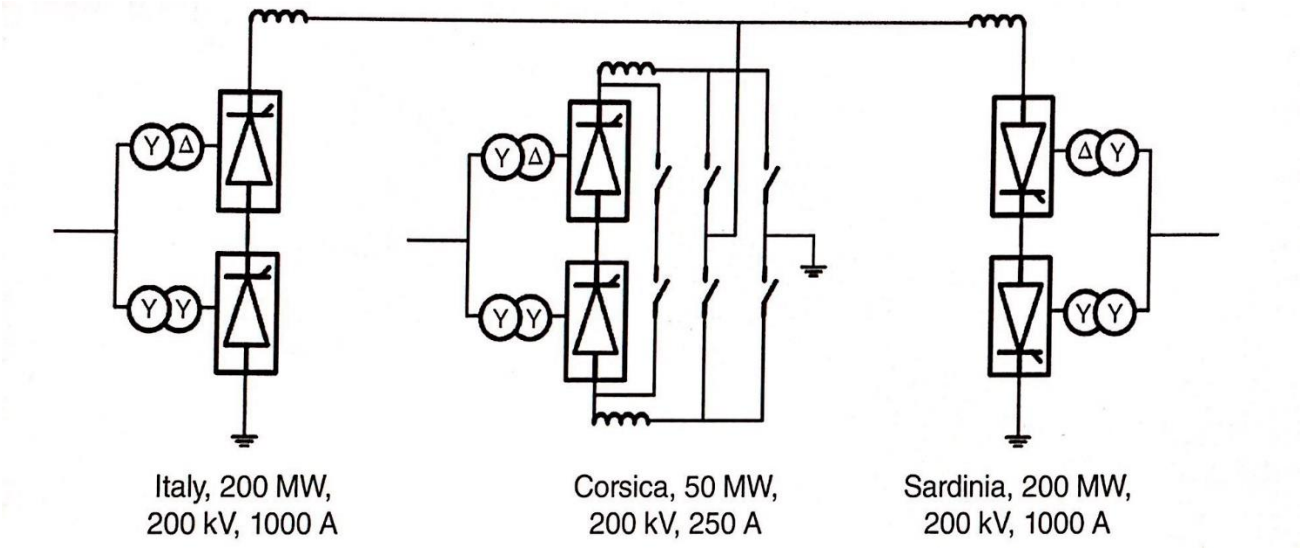

Figure 12.2 Italy-Sardinia HVDC with Corsica tap.

The selected topology is shown in Figure 12.2 and the main characteristics are:

- ✓ The Italy station is a rectifier and controls the DC current.
- ✓ The Sardinia station is the main inverter, which controls DC voltage.
- ✓ The Corsica tap controls DC current (either as rectifier or inverter). Power reversal at Corsica is achieved using mechanical switches as main DC voltage polarity is assumed to be constant. This requires Corsica power interruption for a short period.
- ✓ If the main stations (Italy and Sardinia) change power direction by reversing DC voltage then the Corsica converter (in order to keep same local power direction) should change DC connections with mechanical contacts. This implies temporary Corsica power interruption.
- ✓ The Corsican converter is operating with a very large extinction/ignition angle of around 40^{o}. This enable resilience to commutation failure for up to a 20% voltage drop on the local AC system voltage. On the downside, this solution implies large reactive power demand (equal to active power) and increased converter losses.

12.3 Connecting LCC Converter to a DC Grid

12.3.1 Power Reversal

This section assumes an established DC grid, which can be regarded as an infinite bus with AC systems. The DC grid has firm DC voltage of constant polarity, which is labelled $\pm V_{dc}$. It is capable of delivering or absorbing the DC current as an infinite DC bus, and the grid may contain LCC or voltage source converters (VSCs). The study is concerned with the methods of connecting a thyristor converter to DC grid. **Figure 12.3** shows the thyristor converter connection to a DC grid where mechanical switches used to reverse power direction by changing current direction. The switches are low-power mechanical DC circuit breakers (CBs), which can break or make only limited current (essentially zero current). In order to change power direction, the converter will bring current to zero and it will be blocked. The mechanical DC CBs will change over the connection and then the converter will be restarted in either rectification or inversion mode, depending on voltage polarity. The complete power reversal may take several second.

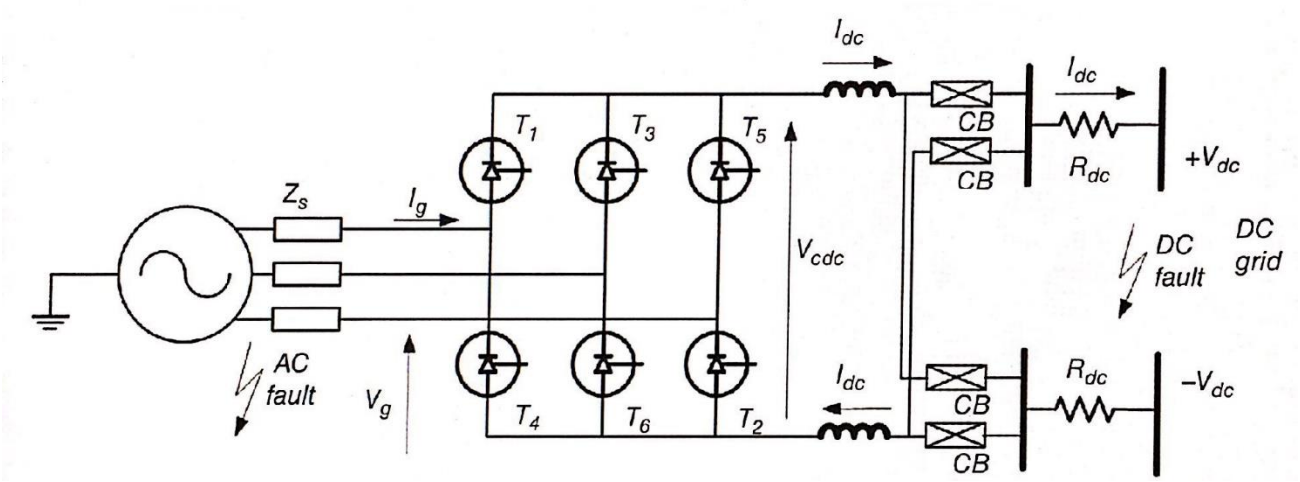

Figure 12.3 Connecting thyristor converter to a DC grid using mechanical switches for changing DC current direction.

Figure 12.4 shows the thyristor converter with bidirectional thyristor valves connected to a DC grid. This converter is capable of rapidly changing DC current direction (100-200 ms). Although this converter has twice the number of semiconductors, compared with topology in **Figure 12.3;** the two antiparallel switches in a valve are not operated simultaneously and they will share many common components. Some estimates show that the station cost may not exceed 150% of the cost of the station in **Figure 12.3**.

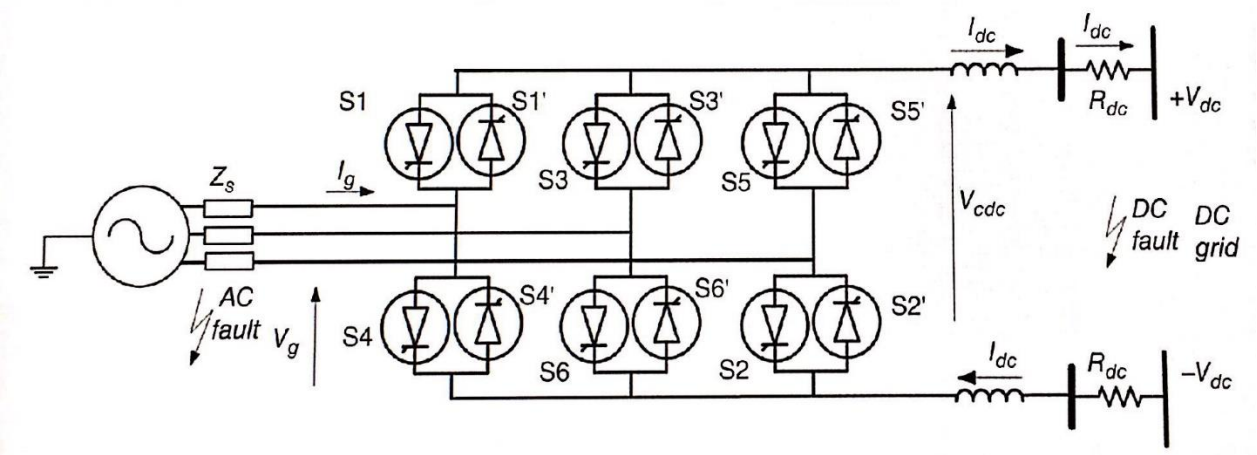

Figure 12.4 Connecting a thyristor converter with bidirectional valves to a DC grid.

Figure 12.5 shows another interesting integration option for a LCC converter. A DC/DC converter is used at the grid connection point. The DC/DC converter provides DC voltage stepping which can substantially reduce costs of DC cable and the new terminal in particular with low power terminals. Some DC/DC topologies may provide voltage reversal on the side of LCC converter and current on the DC grid side. A suitable DC/DC converter can provide power control and firewall against fault propagation. Although DC/DC topologies are not used with high-power DC networks; they are known from low-voltage DC applications and there are cocuraging research results on D/DC converters in DC grids.

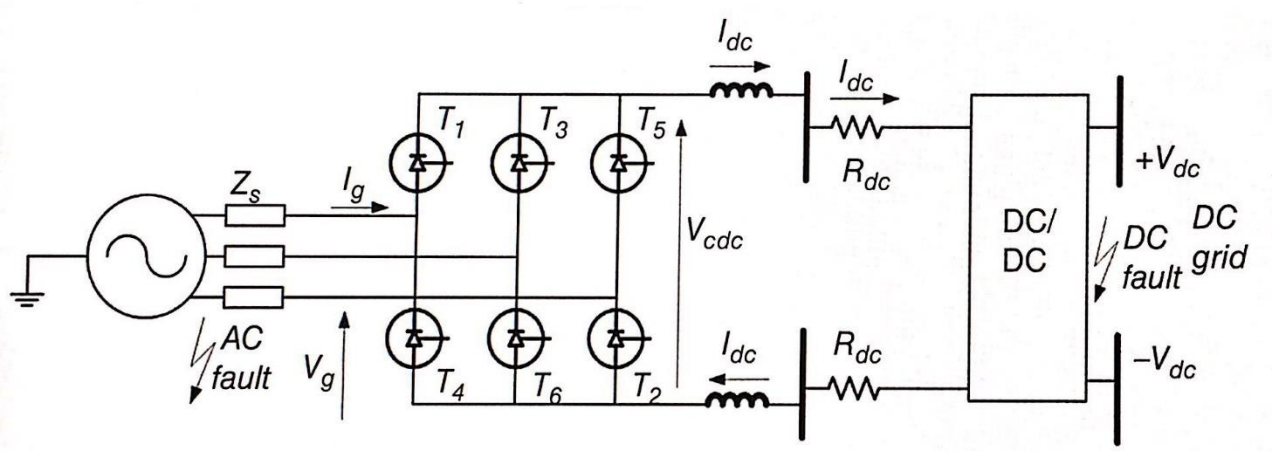

Figure 12.5 Connecting a thyristor converter to a DC grid using a DC/DC converter.

12.3.2 DC Faults

If a DC fault happens in a DC grid, the LCC converter can rapidly control the fault current close to zero or to the rated converter output. There will therefore be no high current on the AC side and AC voltage/grid will be unaffected. Note, however, that reactive power demand will transiently increase because of large firing angles.

Referring to **Figure 12.3**, if $V_{dc} = 0$, the LCC converter operating as a rectifier can reduce V_{cdc} in order to keep I_{dc} at rated values. If the LCC is operating as an inverter then the magnitude of V_{cdc} should be kept below V_{dc} in order to sustain the power transfer. This is feasible except in the case of very low impedance DC faults, which reduce $V_{dc} = 0$. *An LCC converter, therefore, can readily operate through DC faults and it does not transfer DC faults to the AC side.*

12.3.3 AC Faults

If an LCC operates as a rectifier, a small AC voltage depression will be compensated for by reducing the firing angle. For a nominal firing angle of 15^{o} , the firing angle control can compensate for up to a 3.5% AC voltage drop. A more severe AC fault will imply reduction in power transfer. A fast voltage drops of over 20% will completely cease conduction in thyristors. This can have severe consequences if the LCC converter connects a large generation plant (loss of a generator). However, such AC fault is not transferred to the DC side and DC voltage will not collapse. Note that slow AC voltage depression can be compensated with a transformer tap changer.

In the case of an LCC inverter, AC voltage depression of over 5-10% will certainly cause commutation failure. Commutation failure is a short circuit on the DC side, which inevitably interrupts DC power transfer. Therefore, an AC fault at an LCC inverter would cause power interruption and temporary DC voltage collapse in the entire DC grid. Typical recovery from DC commutation failure takes several cycles (50-100 ms) and, assuming that original AC fault is cleared, the power transfer is resumed in 200-500 ms. There are other ways to reduce commutation failure (like capacitor commutated converters or higher extinction angles) but they require further investments.

12.4 Control of LCC Converters in DC Grids

Figure 12.6 shows a simplified schematic for a LCC converter controller in a DC grid, which is very similar to a LCC converter controller in an HVDC and relates to both rectifier and inverter modes. If the converters is in power/current control mode is necessary to add a stabilizing droop control loop. This control loop modifies the power order in response to DC voltage variation , as discussed further below.

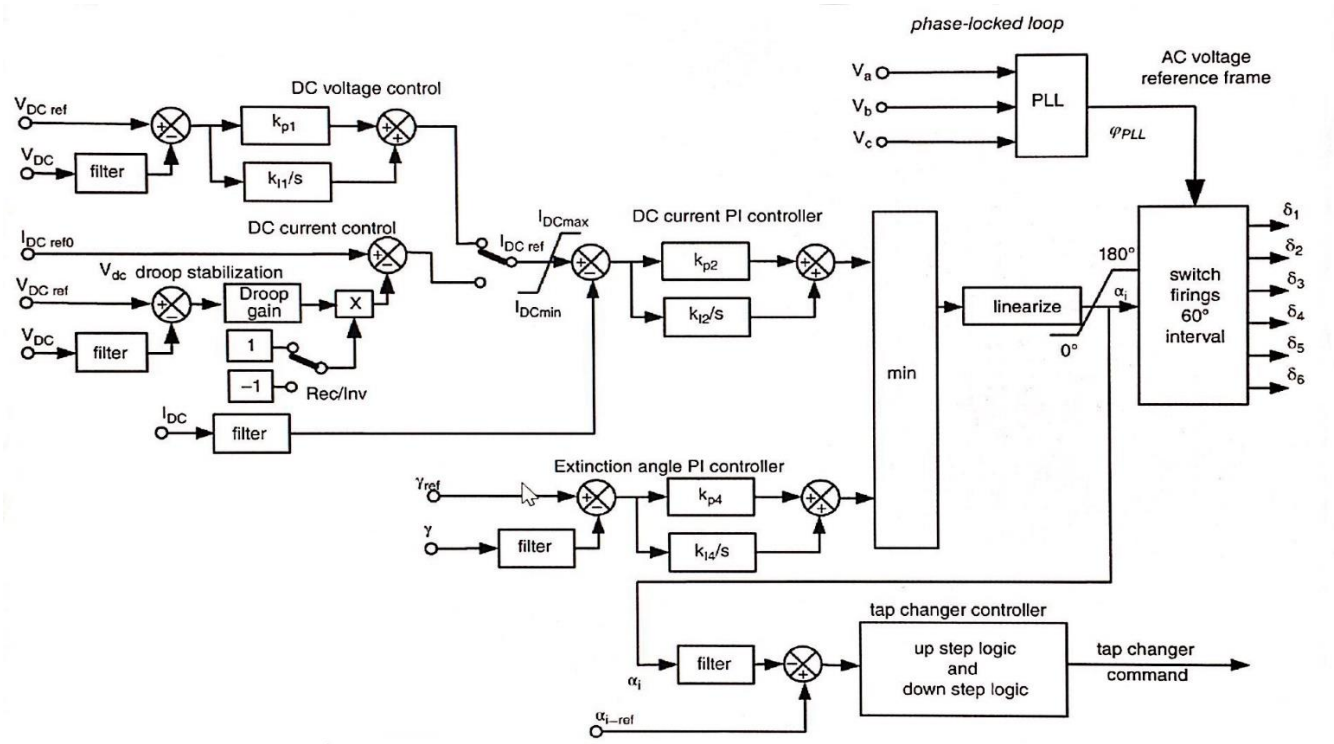

Figure 12.6 Control schematic for an LCC converter in DC grids.

If the converter is controlling DC voltage it would operate with an internal DC current control loop. This current loop limits DC currents in the case of DC faults.

A gamma controller is included as a safeguard from commutation failure and to aid postfault recoveries. A converter in the DC grid will not normally operate in gamma control mode and therefore the extinction angle will be larger than optimal.

12.5 Control of LCC DC Grids through DC Voltage Droop

The power balancing on a conventional, two-terminal HVDC is straightforward, as there is one rectifier supplying full power (into the DC line) as demanded by a single inverter. There is no possibility for power imbalance.

In the case of complex DC networks there will be many rectifiers supplying power to the DC grid and many inverters drawing power from the grid. Some converters will be uncontrollable by the DC grid operator (equivalent to load on conventional AC grids) and they draw power as required by the local control entre or by other factors (e.g. wind speed). The remaining converters, therefore, must instantaneously balance power flow in the DC grid. A power imbalance may happen because of many other reasons like faults, converter tripping or other outages.

A power imbalance in DC grid will imply a DC voltage excursion. This mechanism is similar to frequency balancing on conventional AC grid.

In large DC grid, one (large) rectifier station will have a proportional-integral DC voltage controller, which will be capable of maintaining DC voltage exactly at the reference value with zero error. Because of the

rating limitation, this converter cannot balance DC grid power on its own.. The remaining converters will operate in power control mode where the power reference will be scheduled from the grid control centre (dispatching and scheduling in conventional AC grid). It is also important that the converters in power-control mode respond to DC voltage variations for two reasons: (i) to ensure power balancing and (ii) to dynamically support DC grid stability and transient responses. This control response requires droop DC voltage feedback, just as droop frequency feedback is used with conventional AC grids. The droop gain $K_{DCdroop}$ adjust the power reference in response to DC voltage variations, and it is calculated as:

$$K_{DCdroop} = 2P_{DCmax} /(V_{DCmax} – V_{Dcmin}) \qquad (12.1)$$

Where V_{DCmax} and V_{DCmin} are the allowed limits for the DC voltage deviation and P_{DCmax} is the maximum power deviation allowed for system support (up to the converters rated power). The droop feedback operates in such way that a depression on the DC voltage will lead to lower power demand from an inverter or increased power injection for a rectifier. Rectifiers will normally be required to participate in automatic power balancing, except, perhaps, if they connect to uncontrollable sources (wind farms or other renewable parks). Depending on the grid topology, inverters should also contribute to automatic power balancing, although some inverters may have a droop gain set to zero. The control scheme with the local DC voltage droop feedback will be able to balance DC grid power without commutation terminals.

If a dynamic DC grid support is also required (because of DC grid strength) the DC droop gain should be designed considering dynamic stability. The DC droop feedback can be developed using dynamic filters (frequency dependent transfer function) to enhance stability in a particular frequency range. This likely to be an important requirement with small DC grids.

It is noted that the DC voltage magnitude will be different at points in the DC grid because of the voltage drop along the DC lines. This implies that voltage limits in Eq. (12.1) will be different for different converters. The most important issue, however, is that the DC reference voltage V_{DCref} will be dependent on the DC node and on the operating condition, which will complicate grid control significantly. This issue is not seen when a frequency droop is used with AC grid because is equivalent throughout the grid. **Figure 12.7** shows steady-state operating curves four-terminal DC grid shown in **figure 12.8**. In this figure the rectifier 1 keeps DC voltage at a constant level (within its operating range). Each of the other three terminals regulates local current but the current reference depends on the DC voltage. For clarity of illustration, all currents are shown with positive sign, however inverter currents will have a negative sign and the sum of all currents will be zero at any instant.

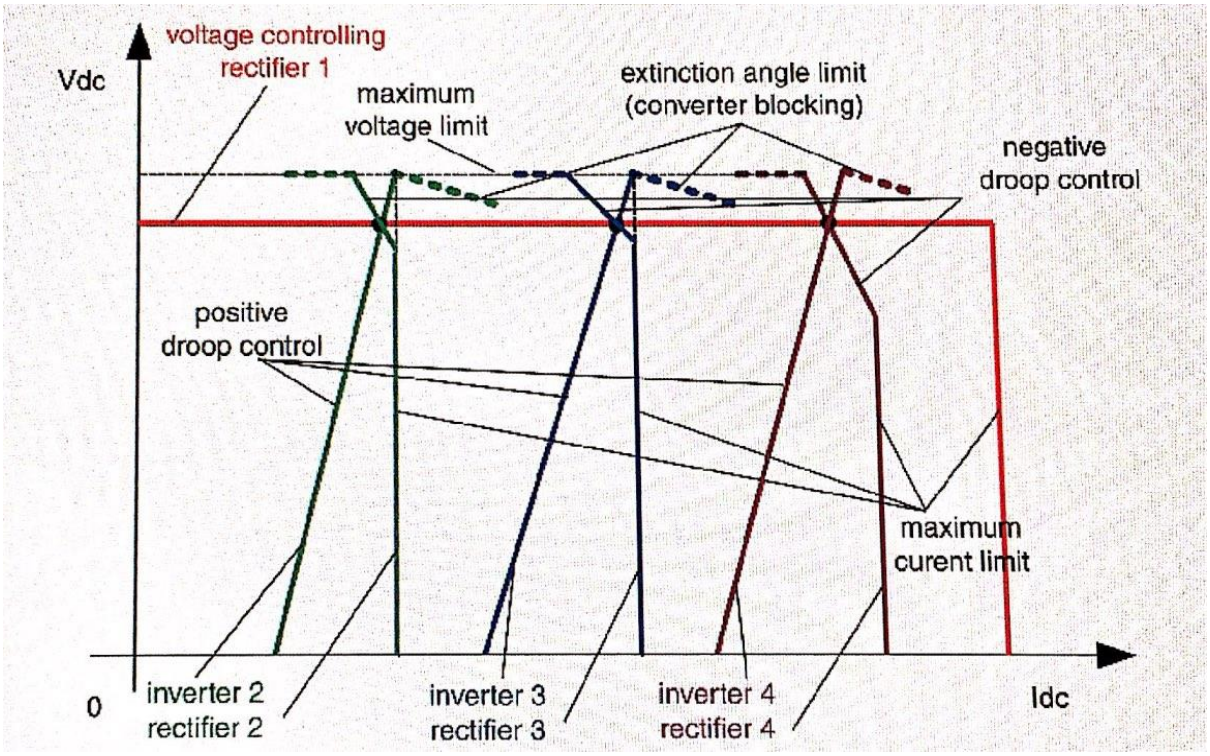

Figure 12.7 Steady-state VI characteristic of four-terminal LCC-based DC grid.

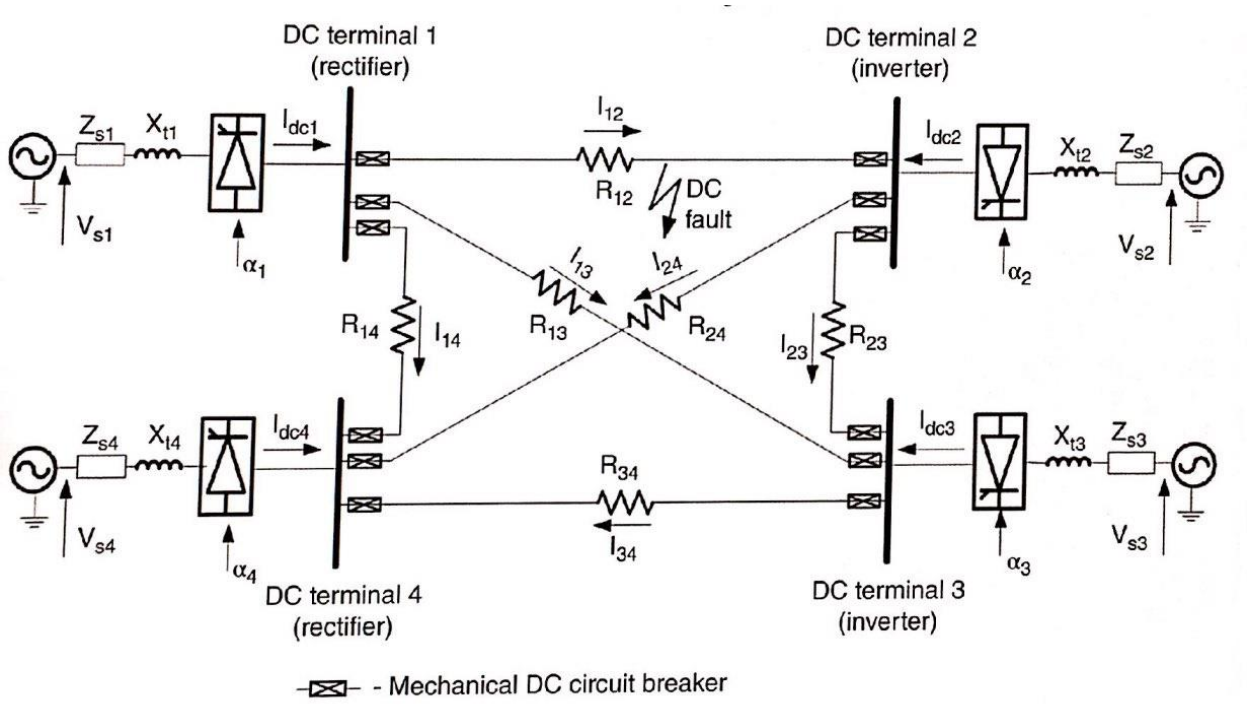

Figure 12.8 A four-terminal DC grid with LCC converters.

12.6 Managing LCC DC Grid Faults

ADC grid with LCC converters will not have high DC fault current as each LCC can regulate infeed from local AC grid. For permanent DC line or cable faults it is necessary to isolate the smallest segment of the grid (the faulted line) in order to enable normal operation of the remaining parts of the grid. This can be done using low-cost mechanical CBs considering that fault currents are low and clearance time is not critical.

If there is a fault on cable 12, as indicated in Figure 12.8, the two rectifier terminals will rapidly reduce local DC voltage in order to keep the local DC current below rated values. Within the controller time response, say 20-100 ms, the DC current on all rectifiers can be brought to zero. The inverter controllers will maintain the operating angles in the inversion range to avoid feeding the fault. The fast converter controllers can therefore reduce DC current in all DC lines to zero and this should clear all transient DC faults.

If a fault is permanent, the DC grid protection system can resolve the fault location and trip the two mechanical CBs at the ends of the affected line. Note that these CBs will be opening at zero or very low DC current. On isolating the fault, the grid DC voltage will be recovered, and the grid assumes normal operating in a postfault topology.

12.7 Reactive Power Issues

An LCC converter in a DC grid may have more reactive power issues (compared with LCC in HVDC for the following two reasons:

- ✓ An LCC converter will be operating with larger firing angles to enable an adequate control range, which requires more reactive power (both in rectifier or inverter modes).
- ✓ An LCC converter will operate with frequently varying firing angles. The angle variation is the result of active power change and power balancing with the droop control. This implies requirement for variable reactive power support and frequent operation of CBs on capacitor/filter banks.

Some of these issues can be eliminated with DC/DC converters that provide variable DC voltage level, with the topology shown in Figure 12.5.

12.8 Large LCC Rectifier Station in DC Grids

A DC grid may have a combination of VSC and LCC converters because each topology has advantages in certain applications. An LCC converter will cost less and has lower losses compared with a VSC converter.

A large rectifier station perhaps connected to a nearby power station is a good candidate for LCC converter topology in DC grids. Assuming that the station is only operated as rectifier, the power direction change is not required, and commutation failure is not an issue. The nearby generator should be able to supply fast-varying reactive power demand. A strong generator-based AC grid is also not likely to suffer AC voltage depression and therefore no adverse impact on the DC grid is expected. Line-commutated converter technology may therefore have overall advantages for large rectifier.

13 DC Grid Control

13.1 Introduction

If an AC/DC converter is installed with the main purpose of facilitating power trading between the local AC grid and the DC grid, the local AC system operator might primarily be interested in the exchange of active and reactive power through the converter. However, when connected in a DC grid, the voltage source converter (VSC) controllers will be required to contribute to DC grid stabilization in addition to local control. Because of the importance of DC grid integrity, the DC grid power balancing and stabilization may assume high priority in control system at each terminal and some control functions may contradict local AC controls and may require trade-offs on performance.

The DC grid control will involve local converter control at each terminal and a central dispatcher, as shown in Figure 13.1. The local controller at each terminal will receive local measurements to regulate local variables, but it will also receive commands /reference values, gain settings, etc. from the dispatcher. Any communication with the dispatcher will involve delays (in each direction), depending on the grid size. The speed of the control signal propagation in optical cables is close to the speed of light and therefore the delay will be at least 1 ms per 300 km, plus processing delay, in each direction. It is also important to considered that dispatcher signals may not be available. The grid control must be developed to ensure integrity/stability for all foreseeable outages, with and without the dispatcher. The dispatcher can be best viewed as an optimized of DC grid performance.

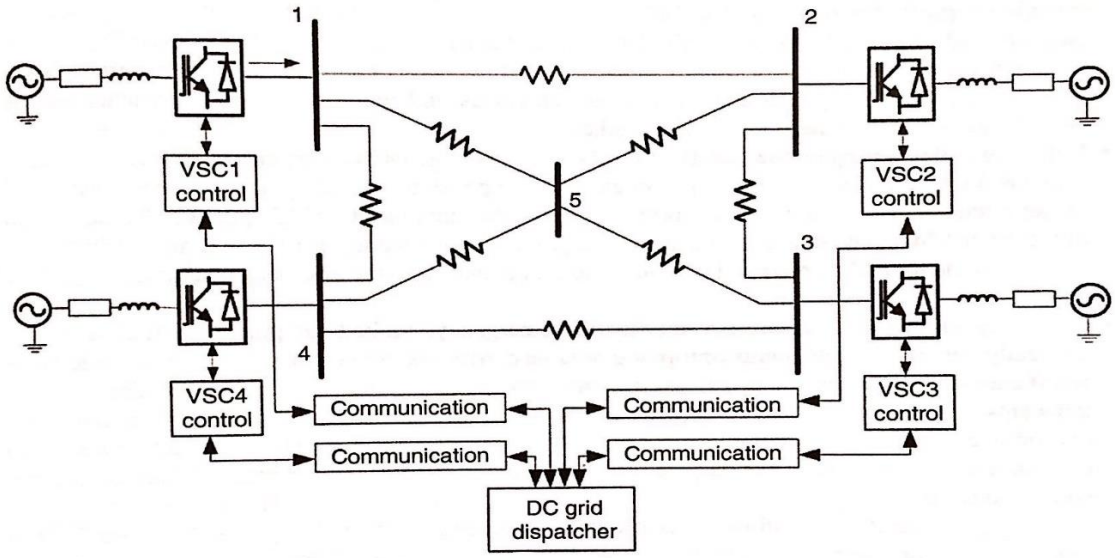

Figure 13.1 *DC grid control structure*

13.2 Fast Local VSC Converter Control in DC Grids

Connecting to the DC grid will impose a range of demands on the VSC converter controller:

- ✓ The highest priority is the DC grid dynamic small-signal stability. Small-signal stability is the systems capability to return to an equilibrium state (all variables are bounded) following a

disturbance. Aperiodic or oscillatory instability will imply the loss of grid segment or loss of the whole grid. All the variables in a DC grid will be closely coupled dynamically because of low impedance of DC lines and low inherent inertia or energy storage (capacitances). Consequently, a growing oscillation on one variable will be observed widely across the whole DC grid. This is different from AC grids, where dynamic instability may develop locally and typically can be alleviated locally. DC grid dynamics will be very fast and the time constants will be of 1-2 orders of magnitude smaller than with AC grids. This implies considerably less time for corrective control action. It is therefore essential that a controller for each converter connecting to a DC grid has the capability of enhancing the stability of the DC grid. It will not be appropriate to develop converter controls using traditional assumptions of infinite DC bus and AC impedance. Steady-state approaches like V-I diagrams and droop gain study are the first steps towards developing controls for DC grid stability but they are not sufficient. In addition, the dynamics of the overall DC grid including converter-converter interactions should be considered and ideally the eigenvalue studies across all frequencies and transient time domain response should be researched for all operating conditions.

- ✓ Maintaining DC voltage within the operating limits. The DC voltage operating limits will typically be within 5-10% around the DC grid nominal voltage. The upper DC voltage limit will be determined considering the component insulation requirements and it must be coordinated with surge arrester characteristics (insulation coordination) on the entire DC grid. As the cost of semiconductors is high and much higher than cost of electromechanical components in the AC grids, the upper DC voltage limit will be tight and very important. Theoretically, all VSC converters can operate with high DC voltage (unless current ratings are exceeded) and therefore the upper limit is not crucial for functionality. However, depending on the designed control margin, as VSC converter loses control capability (control variables are in saturation) for a DC voltage drop of around 10-20%. If DC voltage falls further, the converter current increases and semiconductors will be tripped to prevent overheating.

- ✓ Receiving reference signals and control parameters from the dispatcher and reacting accordingly. Typically, these signals will be changing slowly over a longer time period (secondary and tertiary control). The exact signals from the dispatcher will be defined by the DC grid code but they will likely include set points for power and/or DC voltage, which will be adjusted over longer time periods (second and minutes). If may be required that the dispatcher also requests a change in control parameters, depending on the prevailing grid condition. All the references and parameters from dispatcher can be considered constant in the fast-transient studies.

- ✓ Detecting and reporting on the quality of local control. A large DC voltage error (difference between actual and reference DC voltage) or power error will imply abnormal DC grid operation (unbalance power references or outages). This information should be sent to a DC grid dispatcher. The saturation of the inner VSC converter current control will prevent the converter from responding to dispatcher demand in the normal manner and therefore should be relayed to the grid dispatcher (and/or to other terminals).

- ✓ Capability of operation in various modes like emergency, limited ramping, transient recovery. Typically, large transients (faults or tripping of large converters) will change DC-grid characteristics significantly and grid operation will be different from nominal steady-state conditions. During these transients, a VSC controller may be required to change topology (typically to introduce various limiters and overrides) or locally override set points (like reducing transiently DC-node voltage set point) or change controller gains, or other parameters, in order to ensure DC grid recovery within required performance indicators.

- ✓ Capability of islanded operation and black start. Islanded operation or segmentation of a DC terminal may occur during transient events, or permanent faults, when all the connecting lines are tripped by grid protection logic. Under these circumstances, the grid voltage control should still satisfy all the above requirements (stability , limits, etc.). It is therefore essential that the VSC controller has the capability to reduce power to zero in response to fast DC voltage variation. A black-start capability is desired on all DC grid terminals and can be readily incorporated with typical VSC converter technologies. Note that a DC-grid black-start function will be very different from and AC grid black start, which is commonly incorporated in VSC HVDC controls.

It is understood that some VSC converters will not be able to satisfy some or all of the above requirements. A typical example is a VSC converter connected to an isolated (offshore) wind farm. Such a VSC will be a controlling power according to the wind-farm requirements because a wind farm has no means to regulate (it is dependent on wind speed). Another example is a VSC connected to a passive, weak or critical AC system (offshore platform perhaps). The priority of such VSC controller will be the stability of the AC system and it cannot be expected to contribute to DC grid stabilization.

13.3 DC Grid Dispatcher with Remote Communication

A dispatcher will be required with DC grids and, in particular, this is important if international trade is involved. DC grids will be designed to operate safely without dispatcher intervention but, as with AC grids, a dispatcher will be assigned to coordinate, optimize and reconfigure the grid.

The main roles of the dispatcher include:

- ✓ Sends DC control reference (power and/or voltage) to all terminals. The factors that determine power dispatching include the operating situation, the desired power trade at each terminal, DC grid constrains, dispatch merit order, loss minimization and other requirements. The power reference should be balanced (the sum of powers at all terminals is zero); however, this will never ideally be achieved because grid losses cannot be accurately determined. Furthermore, the tripping of any converter, cable or substation can happen locally at any time and such an event would lead to a significant power reference unbalance in the grid. Such an unbalance would be temporary, lasting only until the dispatcher receives accurate information on the situation and the availability of all grid components. In the meantime, the DC should be able to operate in a stable manner with unbalanced power references. The balancing of DC grid powers will be simpler than with AC grids because most terminals(sources and loads) are controllable. Some terminals may have a high-priority local AC power demand, not responding to dispatcher power demands or only weakly responding to dispatcher demands for grid stabilization.

- ✓ Sends other operating parameters, like droop gains, DC voltage controller limits or operating mode requests, in order to optimize DC grid operation and ensure the required disturbance sharing among terminals for future events.

- ✓ Continuously monitors the DC grid-operating conditions and reschedules power flow in any safe operating limits are violated. The VSC converters can automatically and independently control only local variables like converter current and DC terminal voltage. The currents in DC grid cables and voltages on uncontrolled nodes cannot be directly controlled and they will be the dispatcher's responsibility. The large cables will have thermal time constants in the order of tens of minutes and therefore there is no need for urgent control action. All these constrains will be incorporated in the grid models at the dispatcher, which will be running continuously under inputs from the terminals. The dispatcher may use alert-state labelling to indicate an operating condition that may

not ensure adequate responses to future disturbances (n – 0 condition). In such a case, more severe actions are required from the dispatcher, which should transform the grid to (n – 1) or (n – 2) operating conditions.

13.4 Primary, Secondary and tertiary DC Grid Control

At the fastest control level (within 10 ms), all the converters have a number of feedback control loops that ensure that valve currents and converter voltages are within rated values and numerous other functions (balancing, harmonic reduction, etc.). These control loops are connected with converter safety and cannot be removed. Typically, they received current references from the higher control levels, including the primary response DC grid control. The interface between converter control and DC grid control will be at current reference as schematically shown in Figure 13.2.

The primary system response in commonly described as converter reaction to a DC grid disturbance within the initial time window, spanning perhaps up to 100 ms. In this period all power and DC voltage reference signals are constant and no new communication signals have arrived to converter stations from the dispatcher. Only local are active. It is essential that the primary response acts to dynamically stabilize the DC grid – that it acts towards balancing power in the DC grid and keeps DC voltages within rated limits. However, the primary response alone will not be able to establish a new optimal state for the DC grid.

The secondary response involves adjustments of DC power and/or DC voltage reference points at each terminal in order to ensure that DC voltages are within the required margins and that power flow is as close as possible to the desired values. Secondary control will typically involve some communication between the dispatcher centre and the terminals, and this will happen with at least a 5-10 ms but the entire transient may involve hundreds of milliseconds or longer. The secondary response will not involve direct human intervention. The control will be implemented as a DC power/voltage reference change, control override, control limit setting, control mode change or similar. In the event of limited-magnitude disturbances (wind power change, load adjustment or similar), primary and secondary control will be adequate.

The tertiary control may include human intervention and will happen within minutes and perhaps tens of minutes. It will be activated following a significant outage on the DC grid, like a large converter or line tripping. Tertiary control may include the following: significant changes in power reference at terminals, tripping of terminals, tripping/connecting of terminals, changes in droop gains and others.

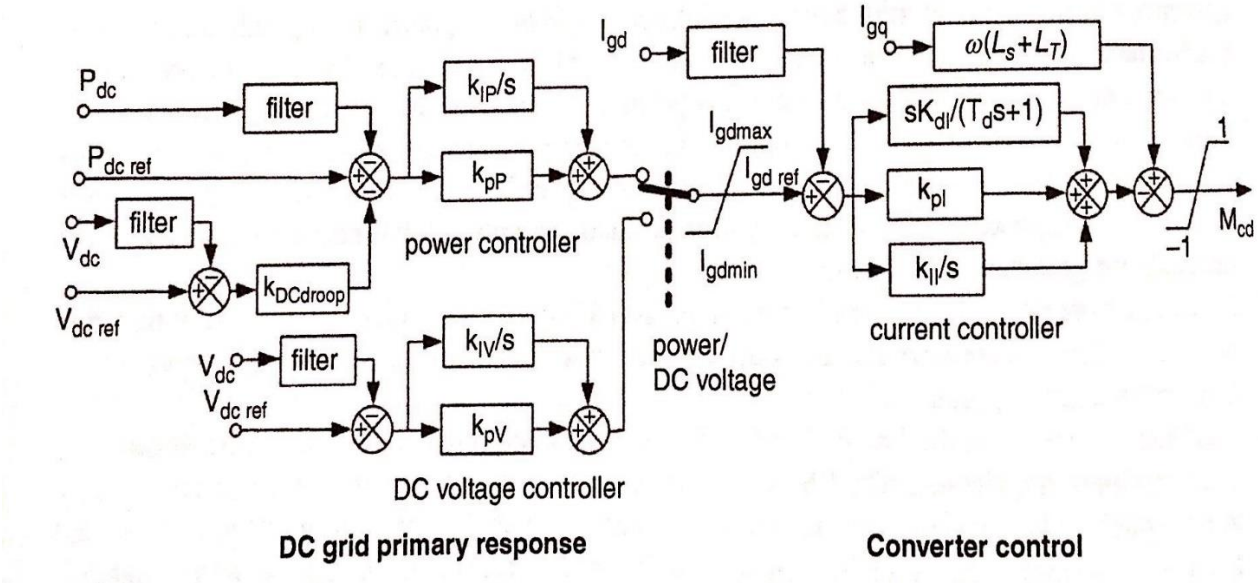

Figure 13.2 *VSC converter with droop feedback for DC grid stabilization.*

13.5 DC Voltage Droop Control for VSC Converters in DC Grids

The DC voltage is the single most important variable which determines integrity of the whole DC grid, the power flow and also the capability of all VSC converters to normally operate. DC voltage drop (even very short) of 10-20% will initiate tripping of VSC converters. Because of lack of any energy storage elements in DC grids, DC voltage will rapidly increase for a power flow unbalance (say inverter tripping). It is therefore essential that the DC voltage is robustly controlled throughout the DC grid for all operating conditions and outages, and DC voltage becomes bedrock of DC grid control. This implies that all converter stations (VSC terminals and DC/DC converters) should respond to DC voltage variations in a stabilizing manner. The DC voltage is an indicator of power balance in the DC grid, similarly as frequency is indicator of power balance in AC systems.

Figure 13.2 shows a simplified controller (only active power control, while reactive power control is unchanged) for a VSC converter in a DC grid. It is very similar to an ordinary VSC HVDC controller, but a droop feedback loop is added to the power controller. This droop feedback constitutes the primary response function and it is required for the VSC converter to contribute to improving stability of DC grid. The converter detects DC voltage variation through *Vdc* droop feedback and adjusts the power exchange in such a way as to stabilize DC voltage.

The central challenge with the above method is what DC voltage reference V_{dcref} to use at each terminal and under particular operating conditions.

The second challenge with the droop feedback is the dynamic stability. The same droop gain is used for power balancing and also it will significantly influence dynamic responses. It is desired to have high droop gains in order to suppress steady-state DC voltage limits. However, high droop gains may have a

negative impact on small-signal stability, which will be reflected in poorly damped oscillatory modes during transient responses.

13.6 Three - Level Control for VSC Converters with Dispatcher Droop

13.6.1 Three-Level Control with VSC Converters

Figure 13.3 shows the VSC converter control with three levels, which is a possible solution for converter control in DC grids. The controller includes:

- ✓ At the fastest level, there is inner current controller. The reference signal is the $I_{gdref,}$ which is limited between $-I_{gdrated}$ and $I_{gdrated}$.

- ✓ A DC voltage controller is permanently operating at the middle level. The local DC voltage is controlled to a reference, which is derived from the power controller at the higher level. The voltage reference has hard limits, which are typically set to $-0.95V_{DCrated}$ and $1.05V_{DCrated.}$ These limits are required to ensure DC grid integrity in case local power differs widely from the power reference (a power reference unbalance in the DC grid).

- ✓ At the highest level is the power controller. This controller is only active if the DC voltage is within $\pm$ 5%. The power reference signal will be received from a dispatcher. However, a provision is made for local power reference, which might be used as an example in case of local emergency situations. The two control loops (DC voltage and power) jointly constitute primary response.

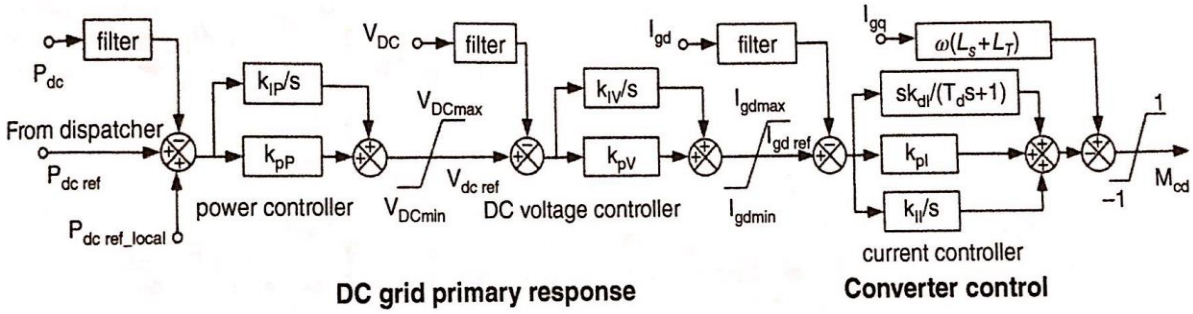

Figure 13.3 *VSC converter controller with three levels.*

The main advantages of the three-level controller are:

- ✓ DC voltage control has two gains (proportional and integral) at each terminal. This enables fast DC voltage control with excellent dynamic responses at each terminal. Integral gain ensures steady-state tracking with zero error, while proportional gain is used to adjust transient responses. Under all operating conditions , DC voltage control has priority and control should respond similarly in all conditions.

- ✓ There is a hard limit on V_{dcref} at each terminal (typically around $\pm$ 5%). As DC voltage is controlled at each terminal with a proportional-integral type controller, this method ensure that DC voltage will always stay within the limits at all terminals.

- ✓ The control method is very robust against unbalanced power orders and outages as any large demands by the power controller will be moderated by the hard limits on the hard limits on the DC voltage reference. Normally power reference will be balanced by the dispatcher (sum of all power order is 0). However , unbalanced power references may happen transiently if a communication link is broken or in the case of a terminal outage.

13.6.2 Dispatcher Controller

If three-level control is used at VSC terminals, then a dispatcher should be equipped with a droop-based power-reference calculation algorithm, as shown in Figure 13.4. This controller maintains the average DC voltage (for the whole DC grid) at the reference value of 1 pu, which is constant for all operating conditions. If average DC voltage deviations are detected then power orders are adjusted for all terminals according to the droop gains, d_1- d_n.

The advantage of this approach is that the global DC voltage average, which is a good indicator of power balance, is used for power adjustments.

Moreover, power balancing (which can be slow) is separated from the fast-dynamic DC voltage stabilization at each terminal that must be fast.

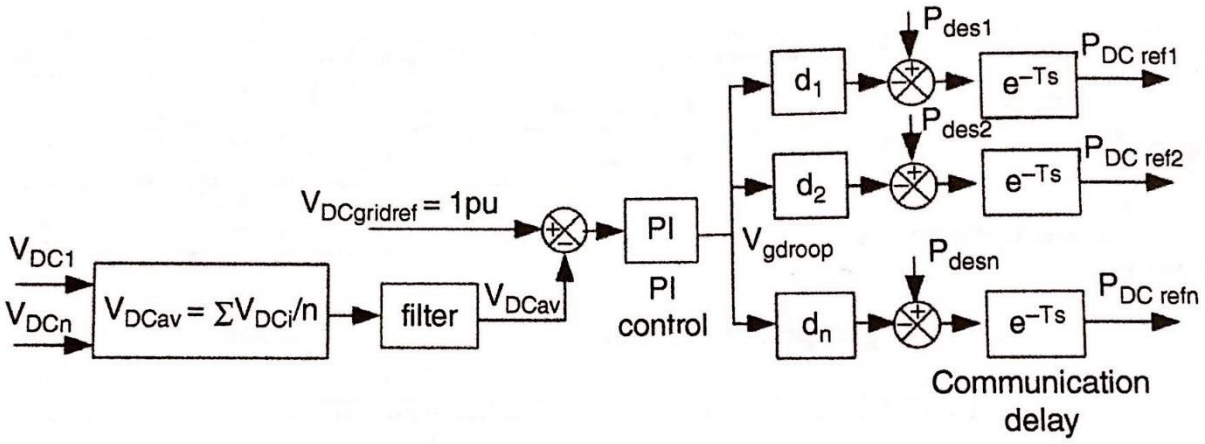

Figure 13.4 *Dispatcher controller when VSC converters use three-level control.*

13.7 Power Flow Algorithm When DC Powers are Regulated

This section will expand further the DC grid power-flow algorithm to include power regulation at each terminal, as this would correspond to power-controlling VSC converters in DC grids.

When DC power feedback is used (either proportional or integral) it is required to use an iterative algorithm in order to determine converter DC currents, as currents are now dependent on the grid DC voltages in the model in Eq. (13.1). An iterative algorithm, like Newton-Raphson, can be developed that has similar structure to the method for DC fault conditions.

$$I_{dc1} = I_{12} + I_{13} + I_{14} + I_{15} + V_1 / R_{11}$$

$$I_{dc2} + K_{d2}\, I_{dc2rated} / V_{2ref}\,(V_2 - V_{2ref}) = -I_{12} - I_{23} + I_{24} + I_{25} + V_2 / R_{22} \qquad (13.1)$$

$$I_{dc3} + K_{d3}\, I_{dc3rated} / V_{3ref}\,(V_3 - V_{3ref}) = -I_{13} - I_{23} + I_{34} + I_{35} + V_3 / R_{33}$$

$$I_{dc4} + K_{d4}\, I_{dc2rated} / V_{4ref}\,(V_4 - V_{4ref}) = -I_{14} - I_{24} - I_{34} + I_{45} + V_4 / R_{44}$$

$$I_{dc5} + K_{d5}\, I_{dc5rated} / V_{5ref}\,(V_5 - V_{5ref}) = -I_{15} - I_{25} - I_{35} - I_{45} + V_5 / R_{55}$$

13.8 Power Flow and Control Study of CIGRE DC Grid – Test System

13.8.1 CIGRE DC Grid Test System

The Conseil International des Grands Reseaux Electriques (CIGRE) DC grid test system is developed jointly by the B4.57 and B4.58 working groups to enable more harmonized DC grid studies and benchmarking within CIGRE and in a wider professional community.

Figure 13.5 shows the CIGRE DC grid with a nominal power flow. The system consists of:

1. Two onshore AC system: system A (busses: A_0 and A_1). And system B (Busses: B_0, B_1, B_2 and B_3).

2. Four offshore AC system: system C (busses: C_1 and C_2), system D (bus: D_1), system E (bus E_1) and system F (bus F_1). One offshore system (bus E) is a load (oil platform).

3. Three DC grids: DCS_1 ($\pm$200 kV monopolar HVDC with busses A_1 and C_1), DCS2 ($\pm$200 kV monopolar five-terminal DC grid with busses B_2,B_3, B_5, E_1 and F_1) and DCS3 ($\pm$400 Kv bipolar eight-terminal DC grid with busses A_1, C_2, D_1, E_1, B_1, B_4 and B_2).

4. Two DC/DC converters: Cd-E1, which enables a power exchange between 800 kV and 400 kV DC system, and C_d-B1, which regulates power flow in the line between busses B1and E1.

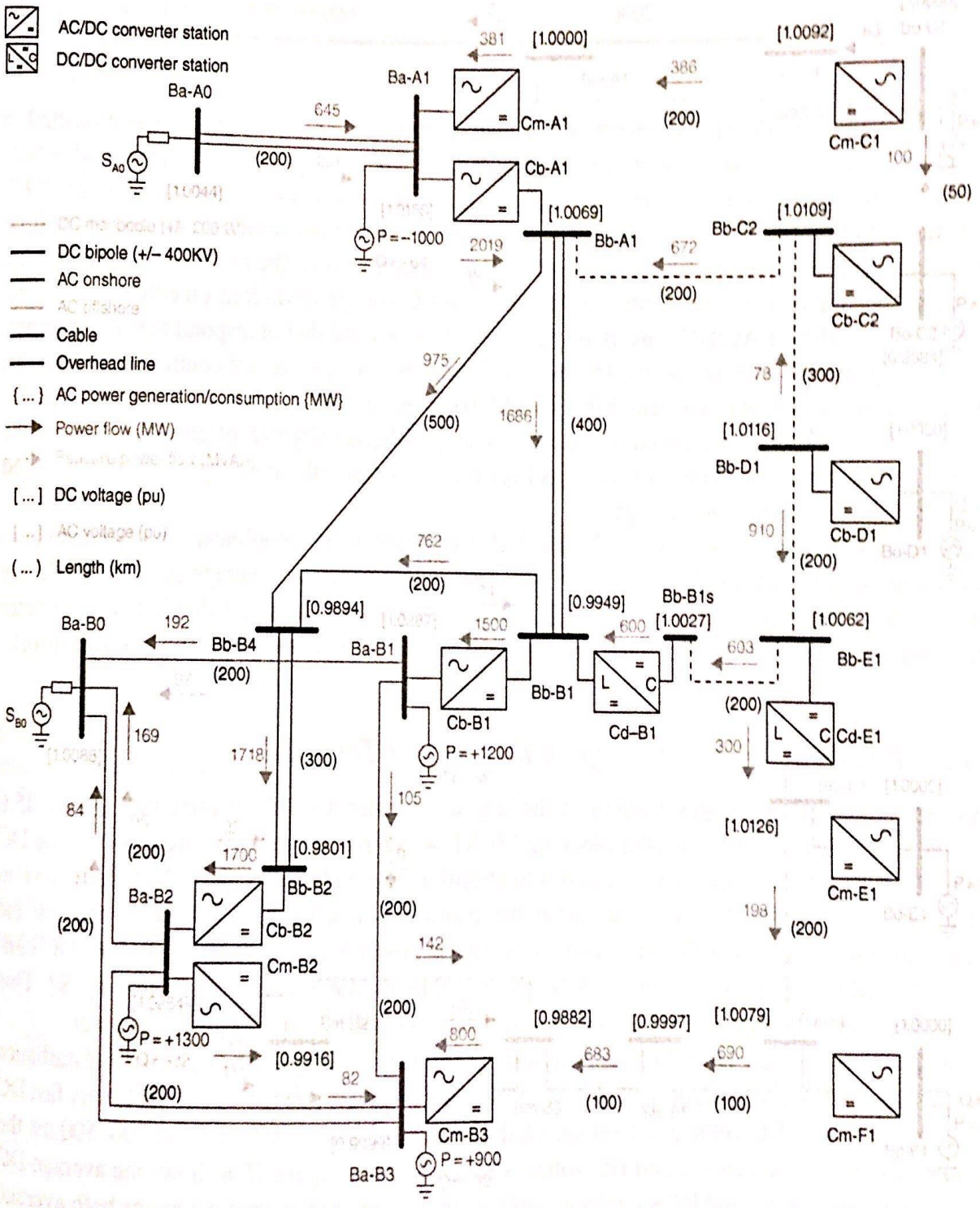

Figure13.5 *CIGRE DC grid benchmark with nominal power flow.*

Table 13.1 power reference values for the CIGRE DC grid

Convert station	Power rating (MVA)	Power reference (MW)
Cm-A1	800	DC voltage control
Cm-C1	800	AC Slack (P = 500 MW)
Cm-B2	800	150
Cm-B3	1200	-900
Cm-E1	200	AC Slack (P = -100 MW)
Cm-F1	800	AC Slack (P = 500 MW)
Cb-A1	2 × 1200	2000
Cb-B1	2 × 1200	-1500
Cb-B2	2 × 1200	-1700
Cb-C2	2 × 400	500 MW
Cb-D1	2 × 800	AC Slack (P = 1000 MW)
Cb-E1	1000	300 (from Bb-E1 to Bm-E1)
Cb-B1	2000	600 (from Bb-E1 to Bb-B1)

The AC system include infinite source, fixed loads (or both) and transmission lines as indicated I the figure. Figure 13.5 also shows all the line lengths. A systematic labelling notation is adopted, where C stands for converter, B for bus, subscript m stands for monopolar, b for bipolar and d for DC/DC. The proposed power set point are shown in Table 13.1. All the converters connected to onshore grids are equipped with the 3L (three-level)control from 13.6.1. The DC/DC converter Cd-E1 also employs a similar three-level control and responds to DC voltage deviations on either side (DCS2 and DCS3). The offshore AC/DC converters regulate local power and do not respond to the dispatcher. There is dispatcher at each of the two DC grids and they use average voltage controller as shown in Figure 13.4 with 1 pu reference voltages (800 kV and 400 kV) and a 20 ms delay is included on all signals. The actual power flow is influenced by the droop setting and gives slightly different values from the reference powers for the onshore converters, as Figure 13.5 shows. All the voltages are shown scaled with respect to the nominal DC voltage.

The CIGRE test system power flow in Figure 13.5 is obtained using a nonlinear time-domain simulation where AC/DC and DC/DC converters use ABC frame nonlinear average models, while the controllers are modelled in detail, AC and DC cables are represented using distributed parameters models and locals are fixed power sources (using local active and reactive power feedback control).

13.8.2 Power Flow after Outage of the Largest Terminal

In this section, one of the outages, tripping of the largest converter (Cb-A1), is presented. Figure 13.6 shows the steady-sate power flow after blocking Cb-A1, which results in 2 GW infeed loss in the DC grid DCS3. The grid establishes a balanced postfault power flow and that all DC voltages are close to rated values in a new steady sate. The dispatcher controllers reschedule power references on the onshore converters while the offshore converters keep the power level unchanged. The DC/DC converter Cd-E1 reduces the power infeed to DCS2 (from 300 to 55 MW) in order to stabilize DCS3. This causes a disturbance to DCS2 and therefore the dispatcher on DCS2 also reschedules power.

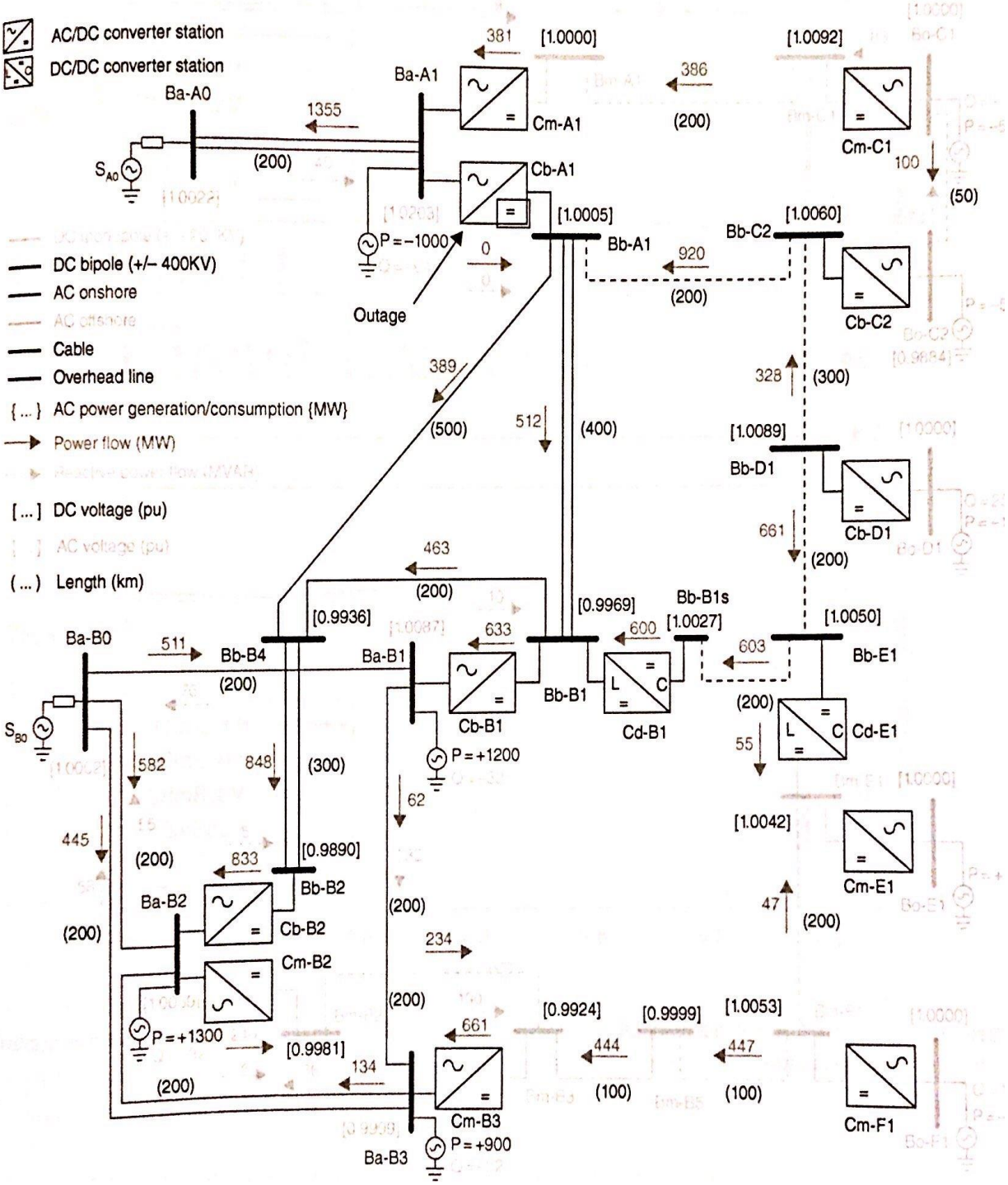

Figure 13.6 *CIGRE DC grid benchmark after terminal Cb-A1 outage, assuming 3L converter control control and dispatcher droop control.*

Figure 13.7 examines the quality of transient responses on DC voltages. This significant disturbance causes an immediate DC voltage drop of almost 15% but the local DC voltage loops enable very fast DC voltage regulation and DC voltage is soon elevated to within ±limits. After around 300-500 ms the

dispatcher action becomes visible and DC voltages return to 1 pu. Figure 13.8 shows the average DC voltages on the grid DCS2 and DCS3, which confirms that dispatcher control maintains both average voltages at 1 pu after this outage.

If dispatcher communication is lost for the above outage (not shown in figures), the DC grid also establishes a stable new operating point but one of the DCS3 DC voltages settles at 0.95 pu limit and the average DC voltage will be below 1 pu.

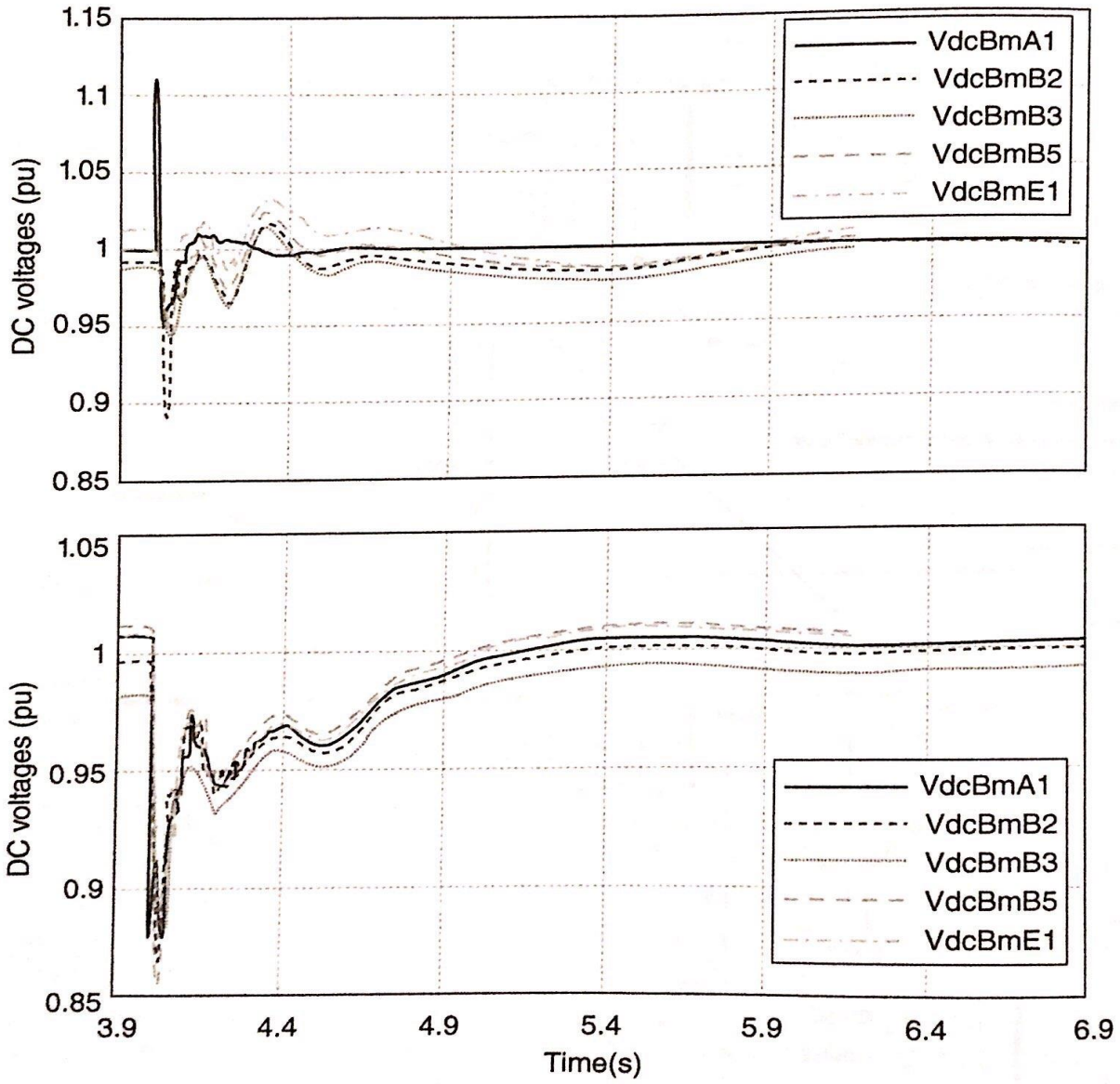

Figure 13.7 *CIGRE DC grid benchmark DC voltages after terminal Cb-A1 outage, assuming 3L converter control and dispatcher droop control.*

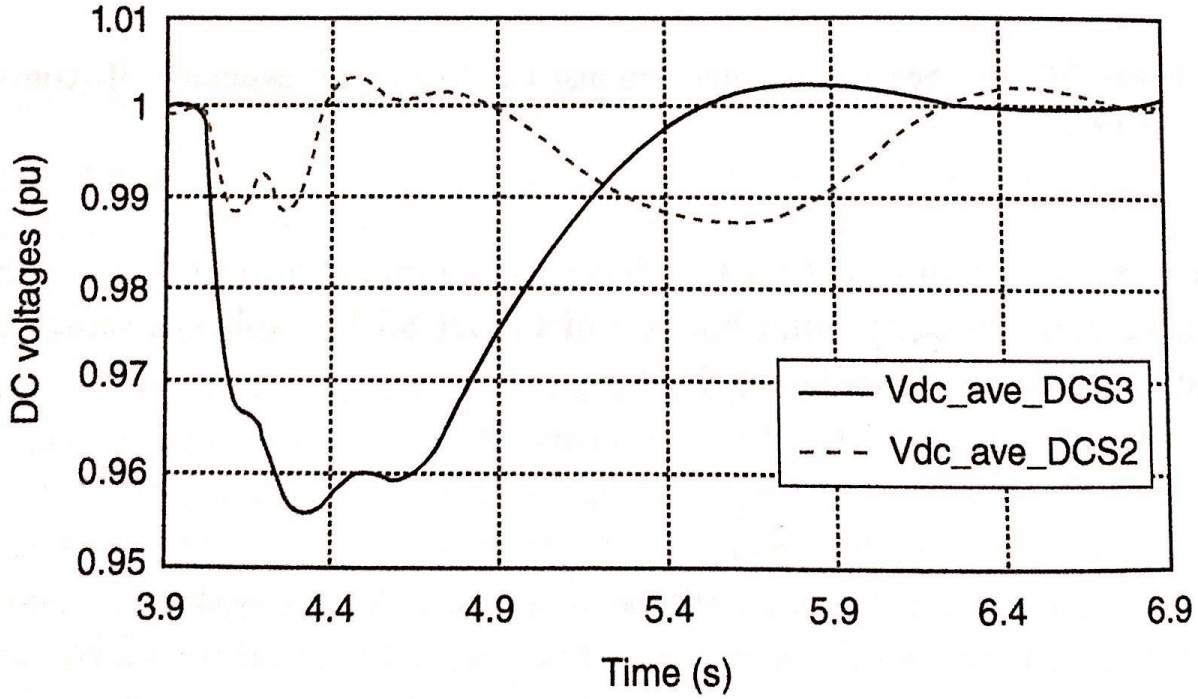

Figure 13.8 *CIGRE grid benchmark average DC voltages after terminal Cb-A1 outage, assuming 3L converter control and dispatcher droop control*.

14 DC Grid Fault Management and DC Circuit Breakers

14.1 Introduction

The protection system for fault management in traditional AC system evolved into very reliable, flexible and cost-effective technologies. It is feasible to develop a protection system for any new AC system topology that designers and operators might demand. The management of faults in a DC grid, however, is considerably more difficult. The main challenge with DC grid protection include:

- ✓ Direct-current fault current has no zero crossings. This creates problems because all mechanical DC circuit breakers (CBs) exploit natural zero crossing to interrupt the current arc. Mechanical DC CBs can be developed based on AC CB technology, but they become more complex and costly.

- ✓ Direct-current line impedances are significantly lower. In AC system the impedances consist of resistive and reactive parts, where reactive component ($2\pi\mathcal{F}\ell$) may reach 10-20 times the resistive part. Zero frequency means that the DC grid impedance have only a resistive part, and

the impedance magnitude is considerably smaller. This implies much larger fault current magnitudes and a low voltage level across the entire grid for a DC fault.

- ✓ Locating a fault in DC grid in DC grid is more difficult because of flow impedances.

- ✓ The semiconductor-based components in a DC grid – voltage-source converters (VSCs), DC/DC converters, DCCBs – have very small thermal constant and a very small overcurrent rating. Considering, too, that costs of semiconductor components are high, there is a strong requirement to clear DC faults in a short time and therefore the fast speed of protection system operation is very important.

- ✓ Voltage source-source converters are blocked if DC voltage drop to around 80-90% of nominal value. This implies loss of a terminal and potentially loss of the whole DC grid for any DC fault. Converter reconnection involves the full start up sequence (charging, synchronization, etc.), which may take a long time (measured in seconds). In general, DC faults should be cleared within 3-5 ms to avoid tripping of VSC converters.

- ✓ Many DC system involve cables that have significant amount of shunt capacitive impedance and further capacitance is present with converter DC-side capacitors and DC-filters. Shunt capacitors will discharge into DC faults, increase fault currents and may cause oscillations. These capacitors only contribute to the fault current in the first few milliseconds but as DC protection requires a short operating time, the capacitances increase the requirement for current rating of DC circuit breakers.

The above challenge make development of DC protection system and protection components considerably more challenging and costly than AC grids.

In a large DC grid the primary role of protection will be to ensure power transfer security and grid stability following DC faults. This is achieved by isolating the faulted segments in such way that the remaining part of the grid can continue to operate normally. In this aspect the protection should be:

- ❖ *Selective*. Only the smallest faulted segment should be isolated.

- ❖ *Sufficiently fast.* If the grid remains under a faulted condition for too long, the converters will be blocked, there will be large loss in capacity and AC machine stability may be endangered according to the angular stability criteria.

- ❖ *Reliable and robust.* In case of protection component failure a backup protection should isolate progressively larger grid segments.

An equally important role of the protection system is safety – both safety of personal and prevention of component damage. The major components in DC grids that should be protected include AC/DC converters, DC capacitors DC cables/Lines and possibly DC/DC converters. Note that fault-protection equipment, that is DC CBs, cannot sustain fault conditions indefinitely and should also posses self-protection (in case of the failure of the main protection system). All semiconductor-based components have very short thermal time constants, small overcurrent capability and generally small I^2t energy store capability, which influences DC grid-protection speed requirements. DC cables, on the hand, involve a significant mass of material and will not suffer a destructive temperature increase even under considerable I^2t energy over the rated values (time constant is in minutes).

14.2 Fault Current Components in DC Grid

A complex DC grid may have numerous VSC converters and numerous DC lines. However, a DC grid will have only three energy sources that can feed a DC fault:

- ✓ The AC grids, which contribute to a steady-state fault current through AC/AC converters;
- ✓ The DC capacitors, which contribute to a transient fault current;
- ✓ The energy stored in DC lines, which contribute to a transient fault current.

This is an important conclusion because a steady-state fault current in a DC grid can only be supplied from the joining AC grids and therefore the fault level in connecting AC grids will ultimately determine the magnitude of DC fault currents. Under a fault condition in the DC grid only the back electromotive force (EMF) voltage on rotating machines in the AC grid can be assumed as constant voltage (the machine speed stays at the rated values for the fault duration).Therefore the total impedance in the fault path (including DC lines and AC lines) determines the fault current. A DC cable, depending on its location inside a DC grid, could have a fault current magnitude larger than any single VSC converter because several AC systems could be contributing to the cable fault current.

Depending on the type of AC/DC converter, there may exist one or two sources of DC fault current on each DC terminal, as summarized in Table14.1. The last two rows indicate the converters ability to drain power from the DC cable by reversing voltage polarity, and to interrupt DC cable energy discharge, which are particularly important for recovering from transient DC faults (on overhead lines).

Converter type	LCC	Two and three level LCC	MMC VSC (half bridge)	MMC VSC (full bridge)
Uncontrolled DC fault current from AC system	No	Yes	Yes	
Uncontrolled DC fault current from DC system	No	Yes	No (assuming no DC filters)	No (assuming no DC filters)
Capability to reverse DC voltage to extinguish DC fault current	Yes	No	No	Yes
DC circuit continuity can be interrupted	Yes	No	No	Yes

Table 1.1 *DC fault current contribution through AC /DC converter*

The shunt capacitors have been extensively used on AC systems and their impact on fault currents and protection requirements are well understood. The DC capacitors and lines, especially cables, will increase the initial peaks of transient fault currents but they do not contribute to the steady-state fault current.

The typical VSC converters will have small DC side inductors. The purpose of these inductors is to limit the capacitor discharge current and also to limit the slope of increase of main fault current from AC grid.

The presumption with this protection principle is that there will never be DC faults between the converter and the inductors (in the value hall).

Direct-current CB costs are high, so it is desirable to have as low interrupting current as possible.

One possible strategy to reduce DC CB duty is to operate DC CB in the short time before the fault current reaches high values. In order to reduce the rate of rise of the transient discharge current, and also to prolong the time for the current to reach steady-state values, additional inductors can be introduced at each end of the line. In practice, inductors will be placed in series with the DC breakers in the same way as inductors are placed on the DC side with VSC converters. This extra time will also enable the protection system to selectively make the trip decision to isolate only the faulted line. Introducing inductors will increase the overall losses in the system and increase the magnetic energy that needs to be cleared by the energy damps in DC breakers. A compromise needs o be found when installing coils: the lower derivative, the additional time and the subsequent gains in selectivity that can be gained by

installing coils, must be weighed against the size and cost of the coils and the effect on the breaker requirement.

Example 14.1

Consider the six-node 640 kV grid as shown in Figure 14.1. Approximately, without detailed calculations, determine the worst case steady-state DC fault level at node 5.

Solution

Using the formula (I_{dcf_pu}) = 4SCR / π (1+ $SCRX_{tpu}$)

Terminal	1	2	3	4
Idcfpu (pu)	5.87	4.1	*5.09*	*6.7*
Idcf (A)	*9182*	*3197*	*11937*	*10471*

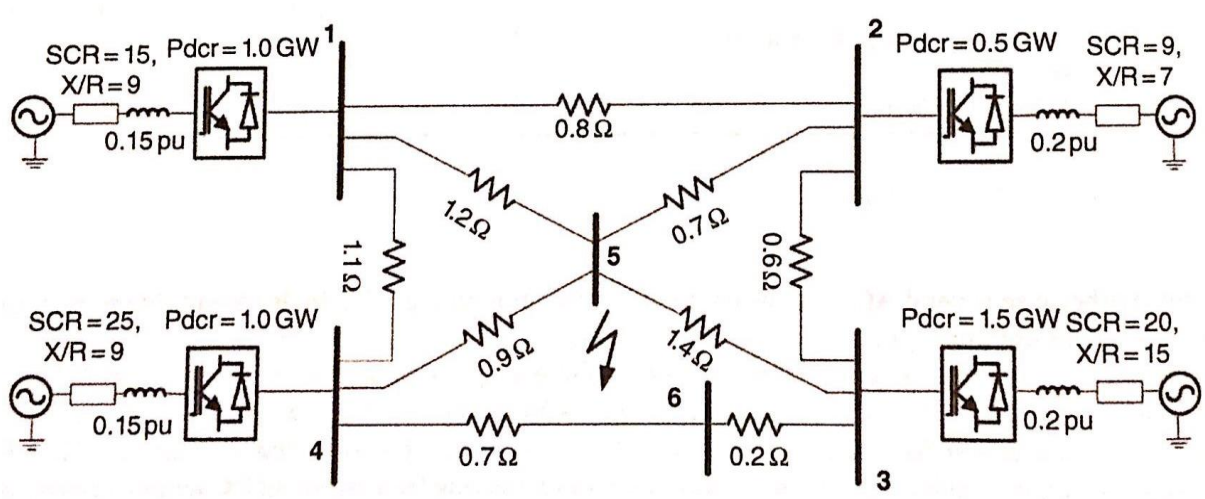

Figure 14.1 Six-node DC grid in Example 14.1

Therefore, neglecting all DC resistances (they are small compared to AC side reactance's) the maximum steady-state DC fault current at any point in the grid is the sum of the fault infeeds from the four terminals:

Idcft = Idcf1 + Idcf2 + Idcf3 + Idcf4 = 34787 A

Note that this approach in only valid if each terminal connects to a separate AC system.

14.3 DC system Protection Coordination with AC System Protection

The faults in DC grid should be cleared by using DC protection. The whole process of isolating a faulted DC cable should be completed before AC CBs (which will also see fault current) start tripping. In general DC CBs will have faster operating times than AC CBs, as will be discussed below. The VSC converter might be blocked under a DC fault and it should be possible to restart VSC converter after the DC fault is cleared. The whole process can happen while are discussed below, are capable of interrupting a fault current within few milliseconds and possibly even before VSCs are tripped. However in complex DC grid the process of finding the fault location and coordination between various DC CBs might take a longer time. The overview of protection operating timeframes for AC and DC sides is illustrated in Figure 14.2.

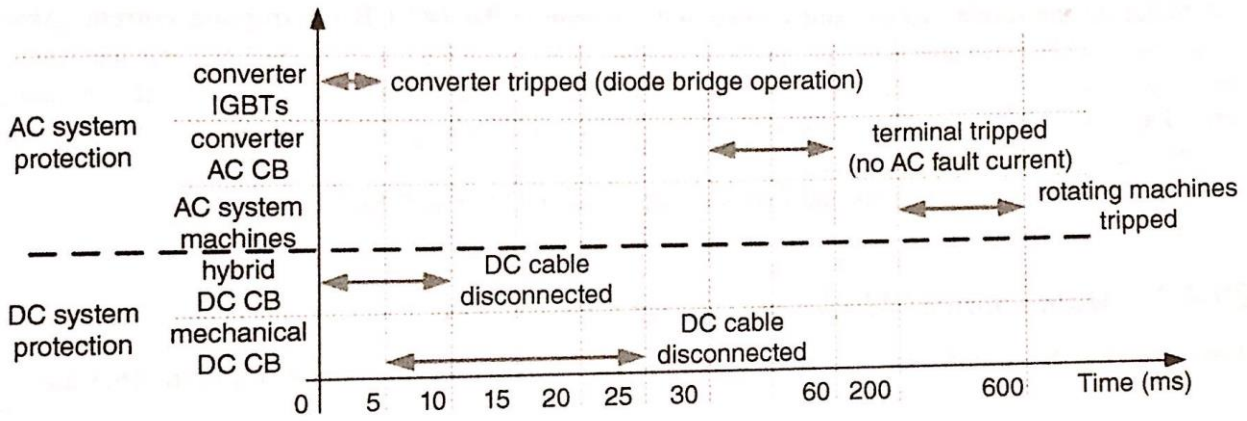

Figure 14.2 Operating timeframe for AC and DC system protection.

14.4 Mechanical DC Circuit Breaker

14.4.1 Operating Principles and Application

The mechanical kilovolt-range DC CBs are commercially available, and they have been used in some industrial DC systems and as neutral switches with high voltage direct current (HVDC). The largest commercial DC CB have a DC voltage rating of around 1-3 kV with nominal DC current of several kiloamperes and DC current interruption capability of 50-100 kA. In 1980s EPRI developed a prototype 250 kV mechanical DC CB but they have not been used commercially. With studies of DC grid in 2010-2015, there has been renewed interest in this technology and several manufacturers have already demonstrated prototype mechanical DC CB products with ratings of 50-100 kV, 5-10 kA. Figure 14.3 shows the mechanical DCCB topology. *It consists of the following components:*

- ✓ Main CB1 and auxiliary CB2, which are similar to common AC CBs. The main circuit breaker CB1 is normally closed and it is rated for full DC voltage and peak interrupting current. The auxiliary CB2 is normally open and it has similar rating as CB1.
- ✓ Surge arrester Zno, for preventing overvoltage and for damping energy stored in the DC system.

- ✓ Resonant circuit (L_1 and C_1), which generates AC current when CB2 is closed. This AC current is superimposed on the main DC current in order to create current zero crossing in CB1.
- ✓ Charging resistor R1, which enables charging of C1 to the rated voltage.

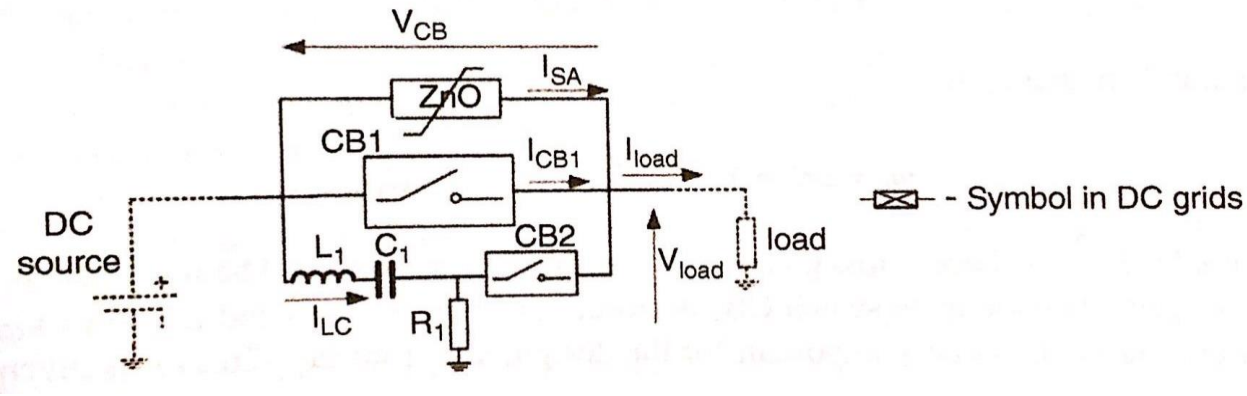

Figure 14.3 Mechanical DC circuit breaker

sufficiently to provide isolation distance for CB1 and fully close for CB2. This time is typically in the range 20-30 ms; however, the latest designed use very fast mechanical systems and multiple manufactures have recently reported clearing times below 10 ms. The inner AC circuit resonant frequency will be in the order of kilohertz and this also helps achieving faster operating speed than 50 HZ AC CBs. In general, mechanical DC CBs will be able to operate faster than AC CBs, which is important for protection coordination. The mechanical DC CBs will be operating after VSC converters are tripped and therefore the diode bridge fault current. Also if mechanical DC CBs are used, the diode bridge must be overrated (to sustain DC fault for 10-20 ms) or some other means of fault current limiting will be used on all DC grid terminals. If very large series DC inductors are used it might be theoretically possible to keep VSC converters operating until the mechanical DC CBs are tripped.

On the positive side, the costs and losses of the above DC CB will be low.

14.4.2 Mathematical Model and Design Principles

Assuming that the initial current is zero, the basic equation for the LC circuit in Figure 14.3 are:

$$i_{LC} = (v_{CB} – V_{c1o} / z_o) \sin(\omega_o t) \quad (14.1)$$

$$v_c1 = v_{CB} – (v_{CB} - V_{c1o})\cos(\omega_o t) \quad (14.2)$$

where the natural frequency is:

$$\omega_o = 2\pi f_o = 1 / \sqrt{L1C1}\,,\ z_o = \sqrt{L1 / C1}\,, \quad (14.3)$$

V_{c1o} is the initial value of voltage across C_1 and V_{CB} is the voltage across CB. The study here is econcerned with the LC circuit when the main swith CB_1 is closed (prior to opning) and therefore V_{CB}=0. The peak current is particularly important for the design, and from Eq. (26.1) it is given by:

$$I\ i_{LCmax} = V_{c1o} / z_o \quad (14.4)$$

The first derivative of the current and voltage are important for the practical design constraints, and from Eqs (14.1)-(14.2) they are given by:

$$di_{LC} / dt = \omega_o (- V_{c1o} / z_o) \cos(\omega_o t) \quad (14.5)$$

$$dv_{c1} /dt = \omega_o V_{c1o} \sin(\omega_o t) \quad (14.6)$$

The maximum values of the current derivative $(di_{LC}/dt)_{max}$ and voltage derivative $(dv_{c1}/dt)_{max}$ in Eqs (14.5) and (26.6) are:

$$(di_{LC}/dt)_{max} = \omega_o (V_{c1o} / z_o) = \omega_o i_{LCP} \quad (14.7)$$

$$(dv_{c1}/dt)_{max} = \omega_o V_{c1o} \quad (14.8)$$

Dividing Eq. (14.7) by Eq. (14.8) it is possible to obtain a relationship that links the peak values for current and voltage derivatives:

$$(dv_{c1}/dt)_{max} = (di_{LC}/dt)_{max} * (V_{c1o} / i_{LCP}) \quad (14.9)$$

The above equation has practical significance as hardware limitation on mechanical switches (ability to provide isolation and prevent restriking) are linked to current and voltage derivatives.
The equation for L_1 and C_1 can be obtained by rearranging Eqs (14.1)-(14.3).

$$L_1 = V_{c1o} / (di_{LC}/dt)_{max} \quad (14.10)$$

$$C_1 = 1 / L_1 w^2_o \quad (14.11)$$

A test system is developed to illustrate calculation of the values for CB parameters assuming that DC voltage is $V_{CB} = V_{c10} = 400$ kV. Two values for peak interrupting current are considered: $i_{LCP} = 3000$ A and $i_{LCP} = 9000$ A. Figure 14.6 shows the design graphs. In this figure, the 'practical limit' curve shows maximum values for current and voltage derivatives to enable successful commutation (below the curve), which is drawn taking into account the prototype tests with EPRI's 250 kV, 9000 a DC CB, but might be very different with modern mechanical designs. It is seen that the larger interrupting current will imply a requirement for a lower resonant frequency for the LC circuit and it will demand a larger capacitor. The inductor value does not depend on the peak interrupting current, but it depends very much on the current derivative.

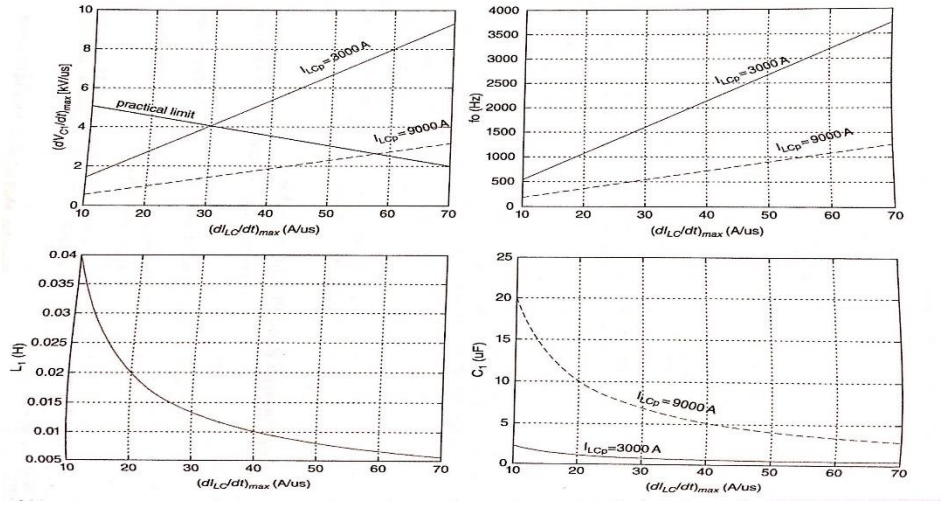

Figure 14.4 Selection of parameters for a mechanical DC CB, assuming $V_{CB} = 400$ kV and two peak interrupting currents $I_{LCP} = 3000$ A and $I_{LCP} = 9000$ A

Figure 14.5 shows the simulation of DC fault clearing using a mechanical DC CB . A DC fault occurs at 0.5 s and the DC voltage drops. The DC fault current is kept approximately constant by a grid-connected LCC (line commutated converter) converter; however , there is small initial peak, which is the result of a grid/cable capacitor discharge and converter controller delays. A delay time of 20 ms is purposely introduced in the DC CB opening to simulate practical delays in the reaction of the mechanical system. At 0.52 s DC CB2 contacts fully close and DC CB1 contacts open. Closing of DC CB2 initiates oscillations (around 1 kHz) in the current that circulates through DC CB1. The peak of these oscillations must exceed the DC fault current in order to drive the summing current to zero in DC CB1. In the lower plot it is seen that the current in DC CB1 reaches zero crossing after approximately 1 ms (period of $\mathcal{F}_0$) and the DC CB1 current extinguishes. DC CB2 opens soon after, enabling the charging of the capacitor in preparation for the next trip signal. DC CB1 may reclose after a period of time depending on the higher-level protection strategy.

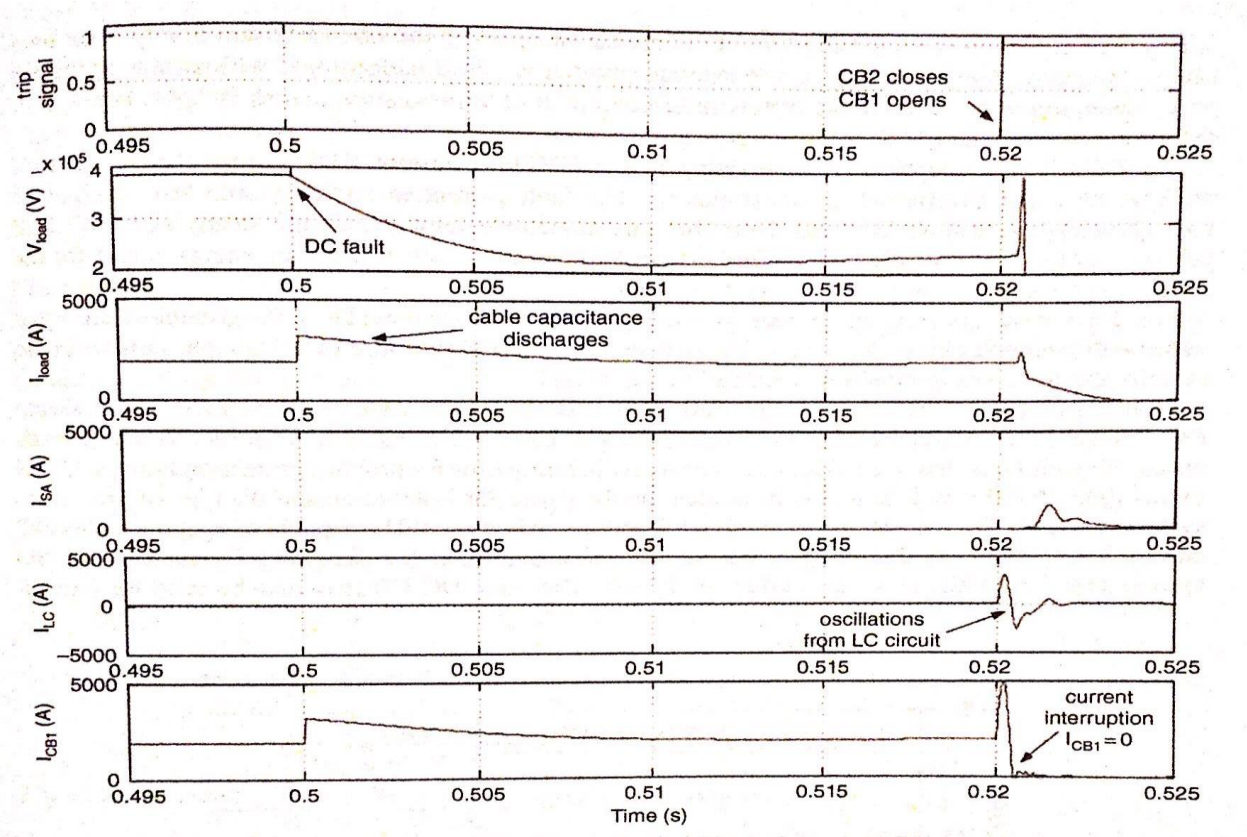

Figure 14.5 Mechanical DC CB simulation for a DC fault at 0.5 s, assuming 20 ms breaker opening delay.

14.5 Semiconductor Based DC Circuit Breaker

Semiconductor DC CBs are developed to improve performance over the mechanical DC CBs. *In particular the following properties are desired:*

- ✓ *Faster operation*. The intention is to operate DC CB before VSC converter IGBTs are tripped under DC fault conditions.
- ✓ *Lower DC interrupting current.* Since DC CB operation is fast (few ms), the fault current will not reach full steady-state value, and therefore the rating of DC CB will be lower.
- ✓ Unlimited number of open-close operations.

- ✓ Theoretically, if fast semiconductor DC CBs are used through the DC grid, the AC/DC converters may not require diode overrating. However, the consequence of protection failure would be catastrophic for the AC/DC converters.

A semiconductor-based DC CB is shown in Figure 14.6, which includes the following components:

- *A valve S_1 with integral antiparallel diode D1.* It may consist of numerous high-power IGBTs or insulated-gate commutated thyristors (IGCT) connected in series.
- *An inductor, L,* which limits the fault current derivative.
- A surge arrester, Zno, which dumps all fault energy in DC circuit.

The topology in Figure 14.6a is capable of interrupting fault current in only one direction, whereas diode D1 conducts uncontrollably in the opposite direction. If bidirectional protection is required then another valve is required, as shown in Figure 14.6b.

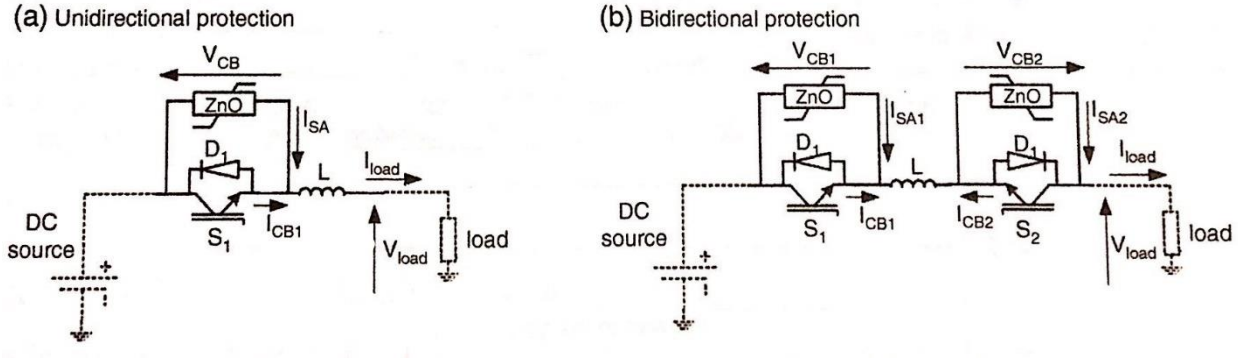

Figure 14.6 Semiconductor-based DC CB

If a high current is detected the switch is capable of opening the circuit within a very short time (the microsecond range). However, the external protection coordination logic will require additional time, which might be in the range of few millisecond. If communication across DC grid is required, this time is even longer.

This DC CB will be operating on the rising slope DC fault current. The purpose of inductor, L, is to limit current derivative which constrains the DC fault current to an acceptable level within the protection operating time (2-5). Note that is inductor reduce the steady-state DC fault current. A large inductor can reduce further current derivative, but it increases energy rating for the surge arrester and it complicates DC grid dynamic.

This DC CB has considerably higher costs compared with mechanical DC CB. Also the steady-state losses will be much higher. Valve cooling will also be required (because of continuous current in the switch)and therefore it should be located in a valve hall.

Figure 14.7 shows the response of a semiconductor switch to a DC fault at 0.1 s. The nominal DC current is 1,2 kA and the trip level is set to 1.9 kA. The slope is set to 1.33 kA/ms, which depends on the inductor L and the line inductance. The total operating time for primary protection logic is 2.2 ms in this figure but this will be highly dependent on the particular installation and the type of protection system. The peak DC current in this case is 4 kA and the switch should be capable of opening at this DC current level. Typically this requirement will be more important for designing the switch than the requirement for nominal on-state current of 1.2 kA. The same DC CB may also be used for backup protection in the event that another DC CB (on another line) fails to operate, and this further increases operating time and raises demand for peak interrupting current.

It is noted that a semiconductor switch will also have internal protection logic implemented as a hard-wired circuit at driver level. This is indiscriminative logic, which serves as the last line of protection in order to open switch before the current reaches levels that the switch can no longer interrupt. This is manufacturer-specified maximum interrupting current, which is presented as 5 kA limit in Figure 14.7.

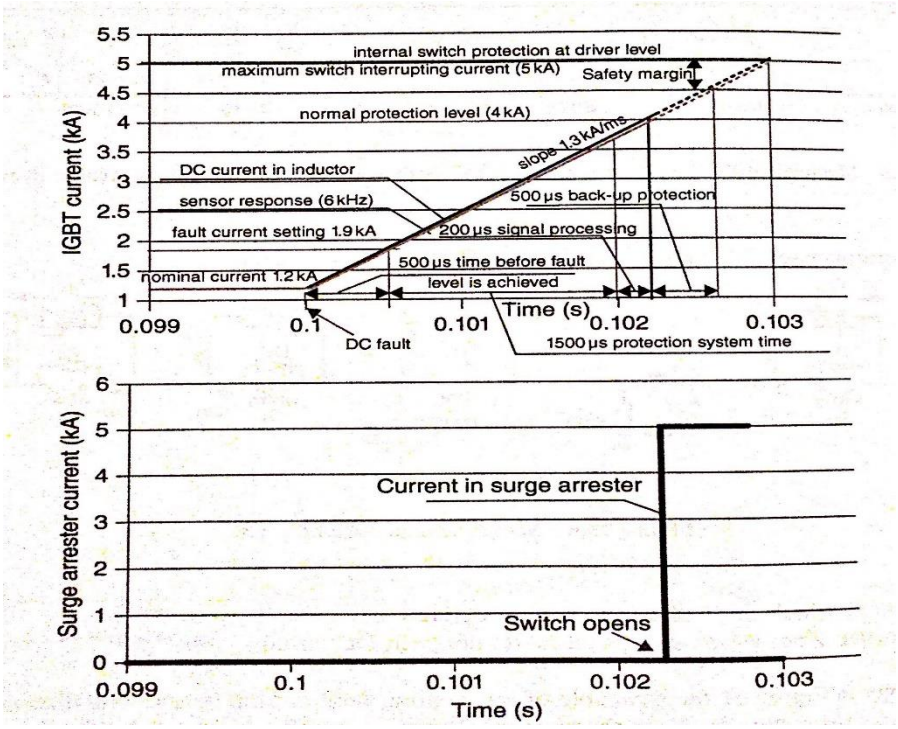

Figure 14.7 Response of a semiconductor DC CB.

14.6 Hybrid DC Circuit Breaker

A hybrid DC CB is developed eliminate on-state losses with the semiconductor DC CB. This is beneficial in reducing direct energy loss, but it also simplifies auxiliary system requirements (like cooling systems). The basic schematic of one possible topology is shown in Figure 14.8. It consists of the following components:

- ✓ *Main semiconductor valve*. This valve is normally but it does not take load current. It is rated for peak interrupting DC fault current and for surge arrester DC voltage.

- ✓ *Auxiliary semiconductor valve with surge arrester*. This valve is normally ON and it is rated for nominal DC current, for interrupting DC fault current and for voltage equal to the voltage drop across the main valve under fault current. This valve is commonly a single 3-4 kV IGBT.

- ✓ *Mechanical CB, which is normally closed and rated for nominal DC current and for full DC voltage.* It opens at zero DC current and can be called a fast disconnector. In some designs the auxiliary valve is not included and therefore the mechanical CB will have some interrupting DC current duty.

- ✓ *Surge arresters that will dissipate the fault energy and prevent overvoltages*. The reted DC voltage is a design trade-off because too low voltage will cause a large leakage current.

- ✓ *The residual CB permanently isolates the unit to eliminate surge arrester leakage current*: It is rated for leakage surge arrester current and full DC voltage.

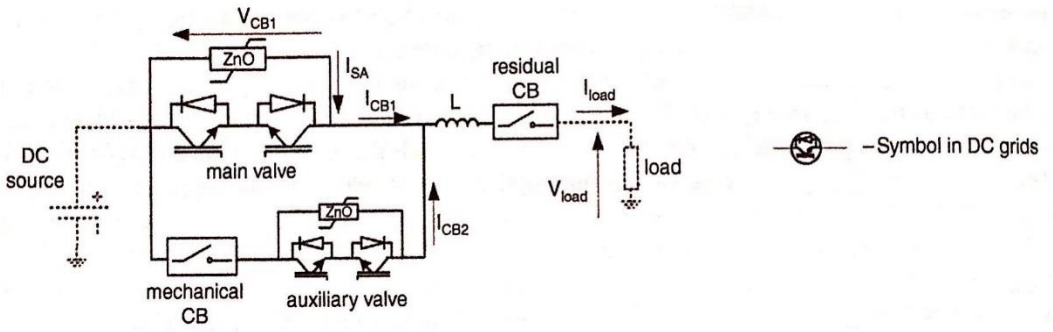

Figure 14.8 Hybrid DC circuit breaker for bidirectional protection

The nominal DC current runs through the mechanical DC CB and the auxiliary valve. This implies than the on-state loss is small as the auxiliary valve has low on-state resistance. *In case of a DC fault the following sequence of events occurs:*

- ✓ The auxiliary valve and mechanical CB take full fault current. The main valve is closed, but it takes no current since it has large internal resistance (many IGBTs in series).

- ✓ The auxiliary valve opens redirecting the fault current to the main valve. At this stage the auxiliary valve blocks the voltage equal to the voltage drop across the main valve (few kV).

- ✓ The mechanical CB opens at zero current. This is necessary to provide isolation of the auxiliary valve. These first three steps can be executed proactively, even before final trip decision is received from higher protection levels.

- ✓ The main valve opens interrupting the full fault current. At this stage the element operates as a semiconductor DC CB described in the section above. The fault current is interrupted, and the fault energy is dumped in the surge arrester.

- ✓ After a certain delay, when the fault current drops to SA leakage level, if no reclosure is required, residual CB will open for long-term isolation.

The manufacturers have demonstrated high-power prototypes , which are capable of interrupting current in the range 7-16 kA within 2 ms. The interrupting current capability of hybrid DC CB will be much larger than that of semiconductor DC CB for the same main valve. This can be achieved since the main valve in hybrid DC CB is not conducting nominal current and therefore it is a cold state before current interruption. The current interrupting capability from cold state is considerably higher than headline figures in manufacturers sheets, which apply to a switch at operating temperature in a than headline figures manufactures' sheets, which apply to a switch at operating temperature in a typical converter.

Another advantage of hybrid DC CB is that it may not require active cooling. The loss in the auxiliary switch is small and natural convection may suffice, which implies simpler and more reliable auxiliaries and valve hall (if needed).

The hybrid DC CBs further offer the possibility of actively limiting the fault current magnitude, which has been demonstrated on some prototypes. This feature might be attractive since such fault current limiting can be applied immediately on local detection of fault conditions, without danger of tripping the DC cable unnecessarily. DC CB tripping action must be coordinated with other DC CBs in the grid, but fault current limiting action needs no coordination, and this implies fast and reliable limiting of fault currents. The fault current limiting however requires higher rated DC CB components.

14.7 DC Grid-Protection System Development

The DC grid-protection system must be capable of locating fault within reasonable time and sending trip signal only to DC CBs that isolate the faulted cable. This is not a simple task because, commonly, all DC cables will have high fault current for a DC fault at any location in the DC grid. This is clearly seen in the example in Figure 14.4, where only cable 34 should be tripped but all cables evidently have high current during the fault.

Figure 14.9 shows the DC CB location on a four-terminal meshed DC grid. Each DC cable has two DC CBs, one at each end. Protection from DC ground faults in the converters (if required) will demand an additional converter DC CB at the connection with the DC bus, as shown the figure. Converter faults are cleared by converter DC breakers together with the AC breaker. It is essential that the converter protection can distinguish between faults in the converter and faults on a line to prevent unnecessary AC CB tripping, which normally implies loss in capacity.

The central bus is spilt into two section connected through two CBs to provide bus bar and back-up protection. All the CBs are assumed to be unidirectional (they allow current in both directions but can interrupt in only one direction). The two DC CBs between bus-bar sections may be replaced with a single bidirectional DC CBs. However, unlike with AC CB, hybrid DC CB for bidirectional operation will have similar cost as two unidirectional devices.

The backup protection on DC grids may be required for high reliability systems. Taking, as an example, a fault on cable 34, then protection logic should trip CB34 3 and CB34 4. This will isolate the faulted cable and the grid can continue to operate without any loss in capacity (assuming that all the other cables have an adequate rating to take the redirected power flow).If a DC CB fails to trip, say CB34 3, then the backup logic will isolate the next wider area by tripping in this cases: CB3b, CB23 2 and CB35 5, which would imply loss of one VSC. Backup protection will require additional overrating of components to allow for longer fault-clearing time.

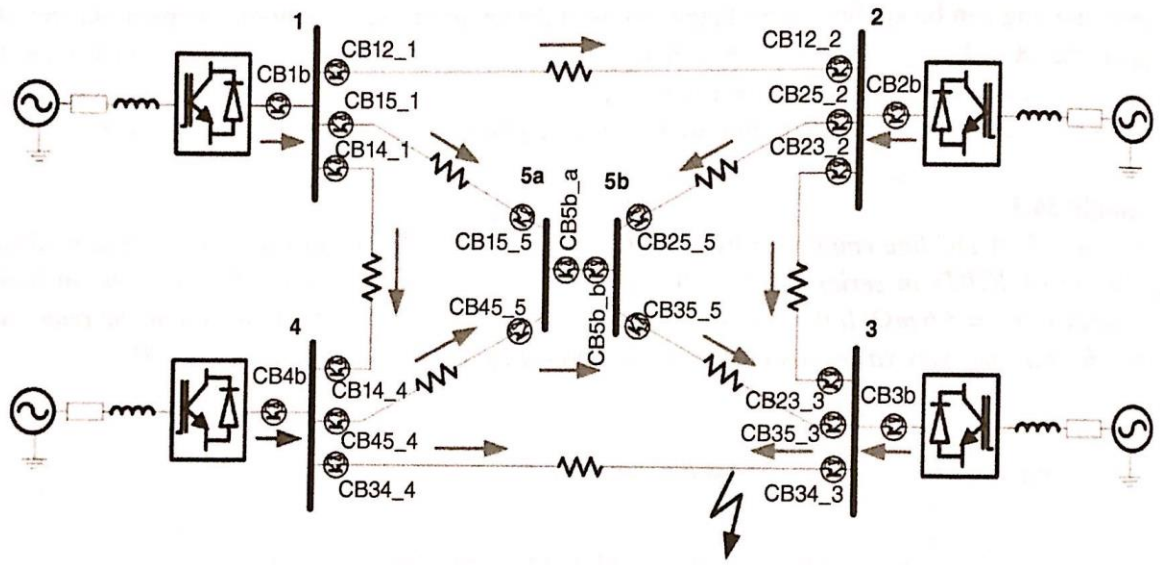

Figure 14.9 Protection system for a four-terminal meshed DC grid.

14.8 DC Grid Selective Protection System Based on Current Derivative or Travelling Wave Identification

In large grids, as in AC systems, it is desired to use only local sensor signals to determine fault location. If controller (relay) at each DC CB determines location of the fault accurately then the decision on tripping can be made locally at each DC CB. No communication between DC CBs would be required which is significant benefit in terms of reliability and speed of protection operation.

Most AC system use distance protection relays where current rise versus time is compared with a specific preset curves. This method uses only current magnitude versus time signal for locating faults.It is suitable with AC systems as AC reactance provides sufficient discrimination between current-time signals at various locations. This method is much more difficult with DC system because of very low DC line impedance.

Figure 14.10 shows the simulation of a DC fault at one end of a 600 km cable. A detailed frequency-dependent 2000 mm^2 three-layer DC cable model is used and four sensors are located at each 200 km points. It is seen that the four sensors read largely different signal in the first 15 ms after the fault. This is the consequence of a finite speed of travelling -wave propagation and different impedance between the sensor and the fault location. The speed of travelling wave propagation depends on the cable parameters. Theoretically therefore it is possible to program the current-time curves or current derivative values for each distance and by comparing with the measured current-time waveform it is possible to determine location of the fault. This method has the potential for fast fault location using only local measurements and adoption of AC grid protection practice. In practice, however, as cable length becomes shorter, the steep current pulse on low-impedance DC cables and the noise content on the measured signals. An additional difficulty is the travelling wave reflections that will happen at cable termination and discontinuity.

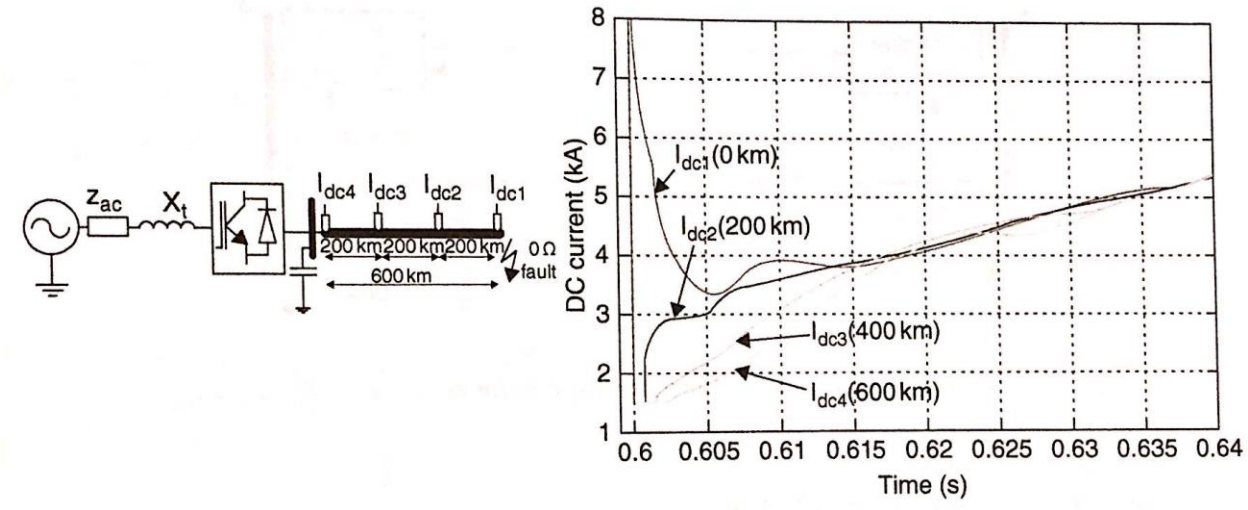

Figure 14.9 Fault currents in four sensors located at different places on a 600 km DC cable (number in brackets is distance from the fault).

14.9 Differential DC Grid Protection Strategy

If all current sensors are direction sensitive it is possible to develop robust protection system for DC grid. However, with large systems some communication between DC CBs will be required, as many DC CBs will have same direction of fault current. Consider CB at bus 2 (CB25 2) and CB at bus 3 (DC CB34 3) in Figure 14.9, which both see large positive fault current (towards the centre of the cable that they protect) for a fault on cable 34. These two CBs have no means to determine if the fault is on the local cable or on a remote cable. Only DC CB34 3 and DC CB 34 4 should be tripped to clear this fault.

Differential protection using pilot wire is a well-developed method for component protection in AC systems. It can be expanded for reliable protection of DC cables, as shown in Figure 14.11. The protection system consist of a direction sensitive sensor (S34), controller (C34) and a Circuit Breaker (CB34)at each cable end. Each controller communicates only with the controller at the opposite end of the same DC cable using a dedicated optical cable. No communication with DC CBs on other cables in the grid is required. The trip decision is made in at each controller if the sum of current on the two sensors on a cable exceeds a threshold positive value for a specified period of time. This logic provides very reliable selectivity because for each DC fault location there will be only two controllers (those on the same cable) receiving positive differential signal.

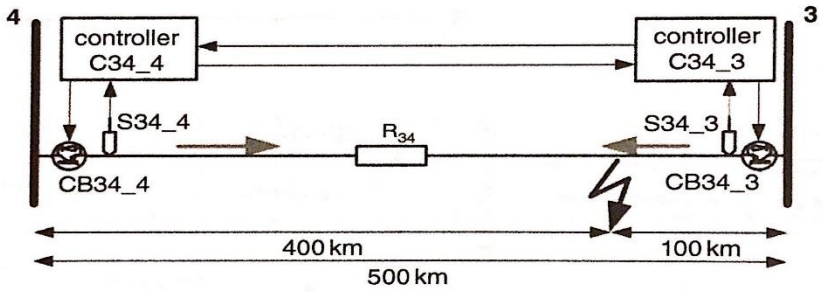

Figure 14.11 Differential protection system for the DC line 34.

The primary drawback of the differential protection is the delays associated with the geographical separation of sensors. Firstly, there will be a detection is the delay in the sensor caused by the travelling wave delay. In the example shown in Figure 14.10 , if the threshold is set to 3 kA (2 pu), the sensor at the opposite end, 600 km away, would be able to detect fault current level after around 12 ms. On the other hand the local sensor can detect fault current level instantaneously.

Additionally, there will be a delay associated with the signal transfer through pilot write between the controllers at the two cable ends. It is assumed that the speed if signal transfer in the optical communication cables will be close to the speed of light (300 000 km/s), not considering optical attenuation. This implies at lest 1 ms delay for each 300 km of cable length. The processing delays in microcontrollers and A/D signal conditioners may account for additional delays.

Figure 14.12 illustrates the signal path in the differential protection system of cable 34 for a fault on cable 34 in the DC grid in Figure 14.9. Fault happens at time0, as shown on the *x-axis* and it is located 100 km from the bus 3 as shown on the *y-axis*. Each controller needs to receive information from two sensors (local and remote) in order to make positive trip decision. The signal from the local sensor will include only travelling wave delay (around 1 ms for controller C34 3 in Figure 14.12) but the signal from the opposite end will involve two delays: travelling wave delay and communication delay (around 4 ms for controller C34 3 in Figure 14.12). The travelling wave delays will be different for each sensor and will be dependent on the fault location, but the communication delays will stay constant regardless of the fault location. It is

seen in the particular example that the total time to trip DC CB34 4 is around 3 ms while trip time for DC CB34 3 is around 4 ms. The DC CB at the cable end further away from the fault will always be first to receive the trip signal.

The fact that DC CBs at the two cable ends will not be tripped simultaneously may further complicate the situation in large DC grids. When the first DC CB is tripped, the system topology changes and now all the remote AC sources begin to feed the fault through the DC CB on the other end of the faulted cable and therefore this DC CB may take a larger trip current.

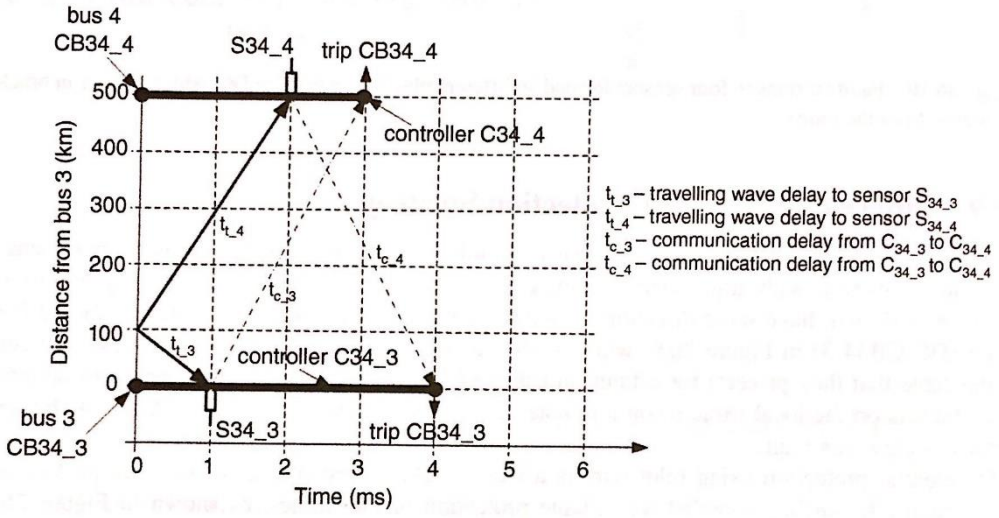

Figure 14.12 Communication and wave delays with DC line differential protection

14.10 DC Grid Selective Protection System Based on Local Signals

It is very advantageous to have a DC fault-location logic signals. Such logic would be very fast and reliable. Fast protection logic, in turn, implies that interrupting fault current will be lower, and this has cost benefits for all components and protection units.

A reliable protection logic based on local sensors is, however, feasible only with special star-grid topology, which has performance limitation. Figure 10.13 shows as four terminal DC grid based on star topology. All the DC CBs at the AC side of converter, as it would be normal case with HVDC converters. A fault on cable 35 is shown and such fault would be cleared by DC CB35 5 and AC CB ACCB 3. The direction of fault currents is given in red arrows. It is seen that only one of the main DC CBs has fault current in the positive direction (CB35 5).

There is an independent protection system for each DC cable. It consists of a DC CB protection Controller/relay and a local direction-sensitive current sensor. The protection logic is decentralized, uses only local signals and trip criterion is simple. A trip decision is made if the local current sensor detects current over a threshold and in positive direction. This implies that protection can operate as fast as

hardware dynamics and processing speed will allow. As hybrid C CBs are employed, the protection speed will be a few milliseconds.

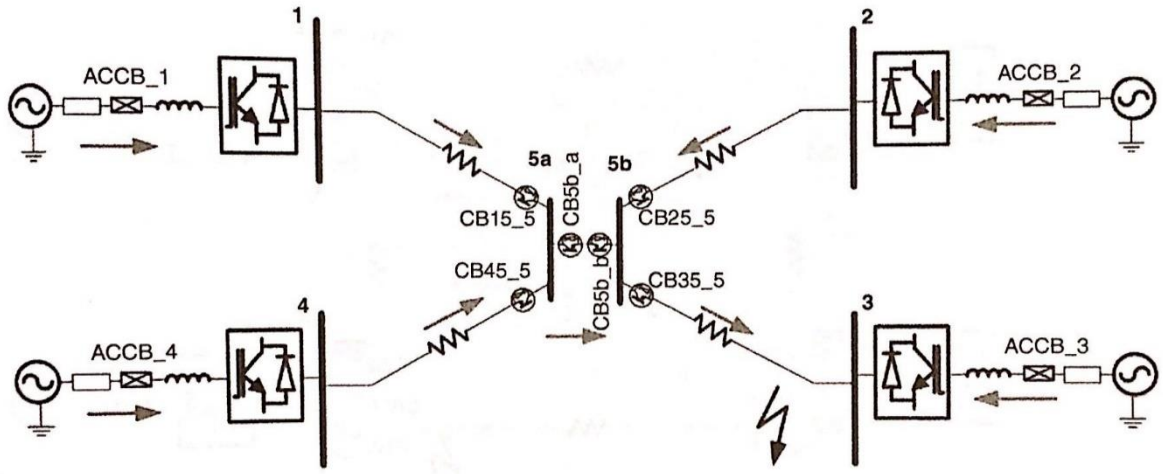

Figure 10.13 Protection system for a four-terminal star-connected DC grid.

A fault on any DC cable is cleared by one hybrid DC CB and one mechanical AC CB.

A spilt bus at terminal 5 is used to increase reliability. There are two CBs at bus 5, which serve as backup protection. Their protection logic is same as for other DC CBs but a delay is added in the control circuit. If, as an example, CB35_5 fails to operate for a specified time interval then CB5b a will operate and isolate bus5b. Also ACCB 2 will isolate fault infeed from AC grid at terminal 2. The AC CBs will need a small delay in control logic if backup protection is used.

The above protection is applicable only to radial topologies and clearly cannot be used with meshed DC grids. The number of DC lines connecting to a single DC bus will also be limited by the DC CB as each DC CB rating as each DC CB in an *n*-terminal system will have fault current summing from *n* – 1 VSC converters.

10.11 DC Grids with DC Fault-Tolerant VSC Converters

10.11.1 Grid Topology and Strategy

The fault current in DC grids ultimately comes from AC systems through VSC converters. The study in this section aims to reduce magnitude of DC fault current through VSC converters, ideally to values comparable to the rated DC current. Such VSC converters would bring multiple benefits:

- ✓ The IGBTs need not be tripped for DC faults. This means that control is retained through DC faults and postfault recovery is fast.

- ✓ The VSC converters would be able to indefinitely sustain DC fault situation, and therefore fault-clearing time time can be extended to the range similar as with AC systems (20-100 ms). This implies that simpler and more reliable gridwide protection systems can be used.

- ✓ The reverse parallel diodes need not be overrated, implying cost savings in VSC converters.

- ✓ If all VSCs in a DC grid can limit the fault current, then the magnitude of fault currents in all cables inside will be low. This implies less costly DC CBs.

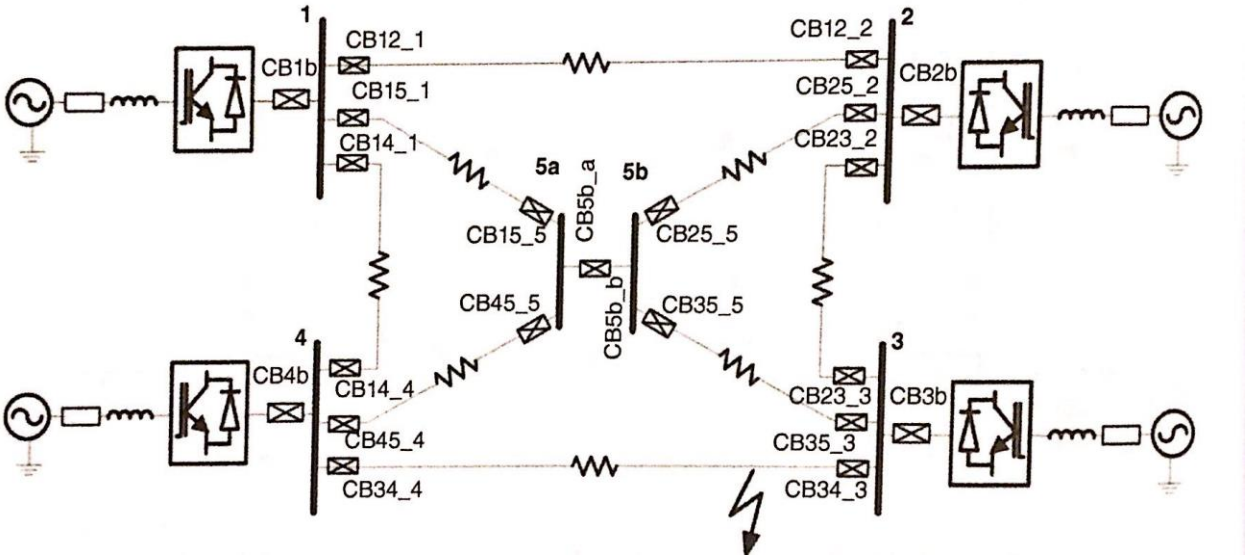

Figure 10.14 Four terminal DC grid with DC fault tolerant VSCs.

Figure 10.14 shows a four-terminal DC grid, which employs four DC fault-tolerant VSCs. If each VSC limits the fault current to 1 pu then the worst-case fault current magnitude anywhere in the grid can reach 4 pu. There are 21 DC CBs, like mechanical DC CBs, is significant. The total cost of 21 hybrid DC CBs would amount to around 7 pu (where 1 pu is VSC converter cost), according to data in Table10.1, which is almost twice the total cost of all VSC AC/DC converters in this grid. The total cost of mechanical DC CBs may amount to 0.1 pu. Therefore further investment in making VSC converters fault tolerant should be carefully explored.
The sections below will review some options for limiting DC fault current in VSC converters.

10.11.2 VSC Converter with Increased AC Coupling Reactors

Figure 10.15 shows a VSC converter (a two-level, three-level or half-bridge modular multilevel converter (MMC) topology) connected to an AC grid through a reactor X_t, which can represent joint impedance of transformer and series reactor. It will be explored if an increased X_t can sufficiently limit the fault current and what drawbacks would occur.
The equation that gives the converter phasor current is:

$$jX_t\overline{I_{gdq}} = \overline{V_{gdq}} - \overline{V_{cdq}} \qquad (10.12)$$

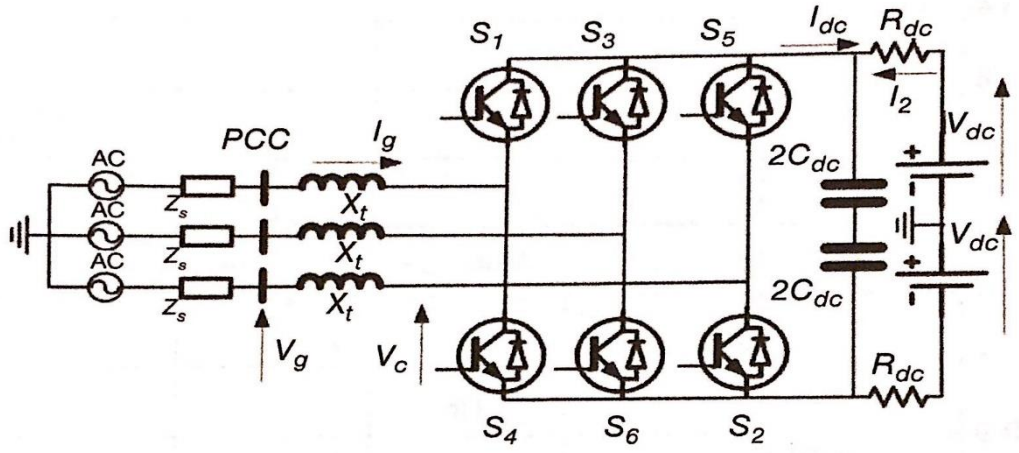

Figure 10.15 L VSC converter

and when separated into real and imaginary components, assuming coordinate frame is linked with V_g:

$$I_{gd} = -\frac{V_{cq}}{X_t} \tag{10.13}$$

$$I_{gq} = \frac{V_g - V_{cd}}{X_t} \tag{10.14}$$

Assuming normal operation with $Q_g = 0$, the reactive current becomes $I_{gq} = 0$. From Eq. (10.14) it is seen that $V_{cd} = V_g$, and therefore this converter cannot achieve any stepping ratio V_g/V_c (transformers must be used if voltage stepping is required). Dividing Eq. (10.14) by Eq. (10.13), the current angle can be obtained and it can be concluded that this angle cannot be equal to the voltage V_c angle, and therefore this converter cannot this converter cannot have $Q_c = 0$ (reactive power at converter AC bus). Consequently converter voltage or current will be larger than the optimal value. Introducing the converter utilization ratio, U_r:

$$U_r = \frac{S_{grid}}{S_{conv}} \tag{10.15}$$

Where S_{grid} is the required power at the grid-coupling point (S_1 in the above example) and S_{conv} is the required converter rating, enables study of the required converter rating. The ideal utilization ratio value is $U_r = 1$, which implies that converter can be determined as:

$$I_g^{fault} = \frac{V_g}{\sqrt{R_s^2 + (X_s + X_t)^2}} \tag{10.16}$$

Figure 10.16, in the top graph, shows the required converter DC voltage (in pu relative to optimal DC voltage) and the utilization ratio U_r, as the function of coupling coupling reactance X_t. Larger reactance will imply a larger q component of AC voltage V_c and consequently larger DC voltage. As the DC voltage increases, the converter rating increases, the utilization ratio will be lower and, practical terms, this implies higher capital costs and also higher operating losses. Normally, $0.1 < X_t < 0.2$ and it is seen that the DC voltage will be only 2-3% larger than optimal, plus perhaps few percentages for control room.

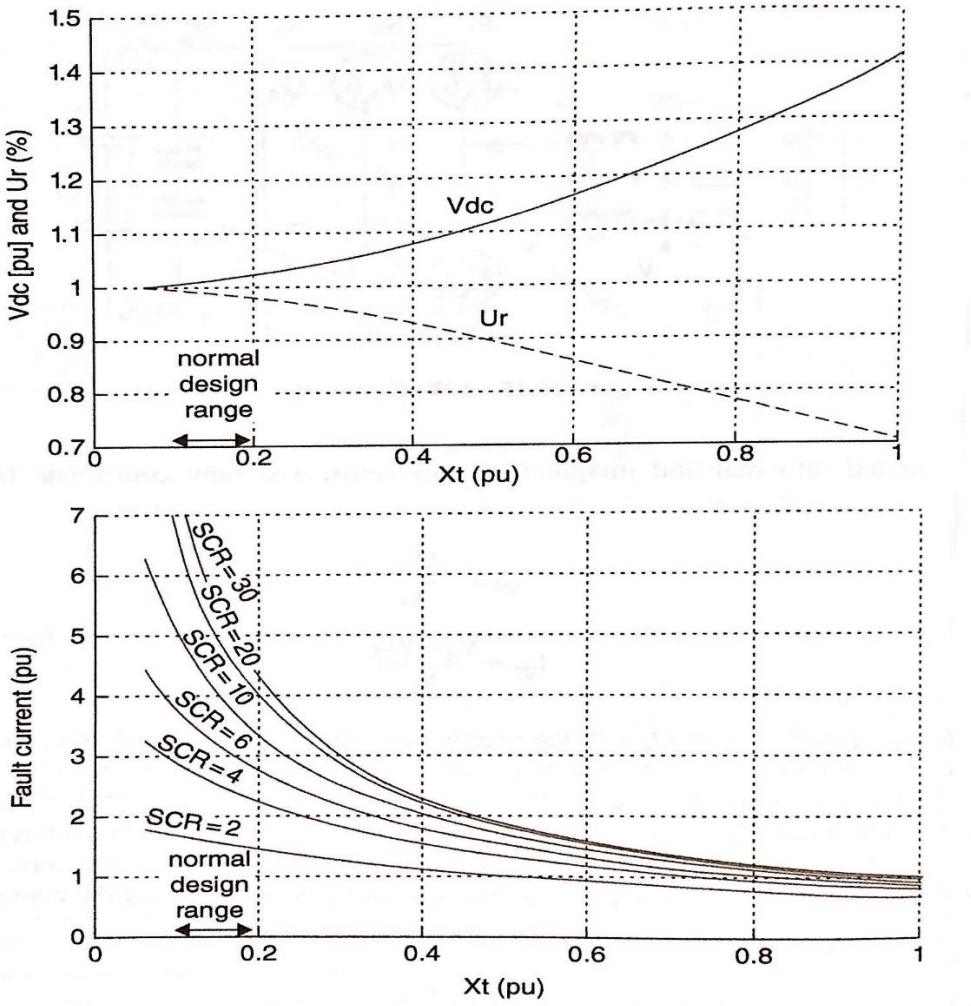

Figure 10.16 Converter utilization ratio and per-unit fault current as the function of interface reactance.

Figure 10.16 on the lower graph shows the fault current relative to converter-rated current I_g^{fault}/I_g for a range of grid strength and coupling reactance values. It is clear that it is possible to reduce the fault current significantly by increasing coupling reactance. For example, with a short-circuit ratio (SCR) = 6 and X_t = 0.9pu the fault current will be 1 pu. Such converter would have around 35% larger costs and operating losses. On the positive side, such design will imply a range of benefits as discussed above (no requirement for additional antiparallel diodes, a lower rating for all DC CBs, simpler protection, etc.)

10.11.3 LCL VSC Converter

Figure 10.17 shows the LCL VSC converter. It includes an AC/DC converter, which can assume any topology (two-level, three-level or half-bridge MMC) and an LCL interface. Compared to the L interface, the LCL interface bring more design flexibility – for example, the possibility of voltage stepping, i.e. V_g/V_c feasibility of achieving zero reactive power at both V_g and V_c, and reduced fault currents (the fault current is limited to a level close to the rated current).

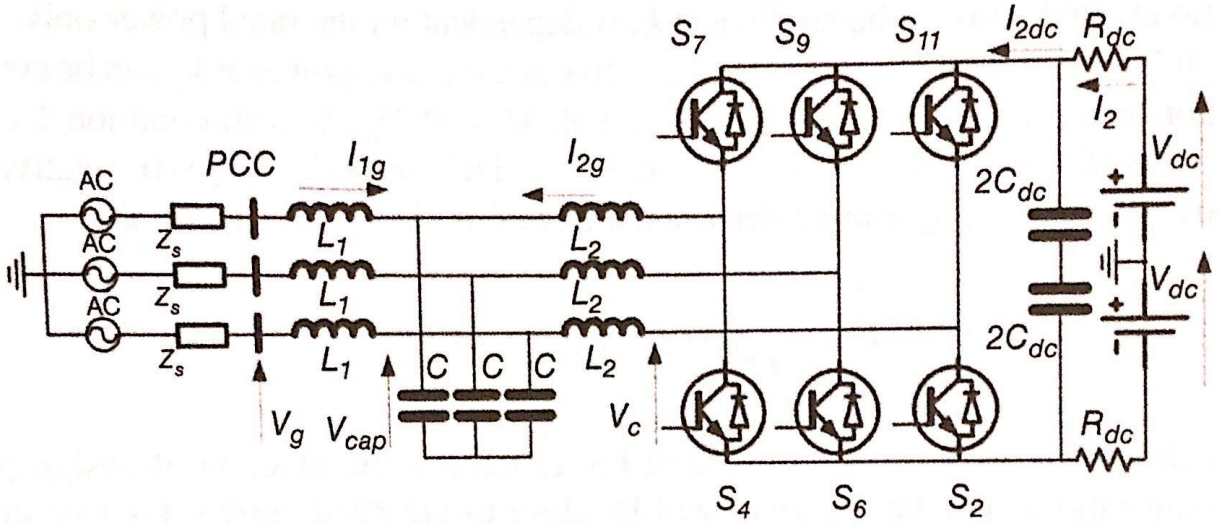

Figure 10.17 LCL VSC converter

The basic phasor equations for the LCL circuit in Figure 10.17 are:

$$j\omega L_1 \overline{I_{1gdq}} = \overline{V_{1gdq}} - \overline{V_{capdq}} \qquad (10.17)$$

$$j\omega L_2 \overline{I_{2gdq}} = \overline{V_{cdq}} - \overline{V_{capdq}} \qquad (10.18)$$

$$j\omega C \overline{V_{capdq}} = \overline{I_{1gdq}} + \overline{I_{2gdq}} \qquad (10.19)$$

The above equation can be more conveniently written using parameters $K_1 – K_3$ as:

$$\overline{I_{1gdq}} = \frac{V_g k_1 - \overline{V_{cdq}}}{j\omega \times k_3} \qquad (10.20)$$

$$\overline{V_{capdq}} = \frac{V_g(k_1 - 1) + (k_2 - 1)\overline{V_{cdq}}}{k_2 k_1 - 1} \qquad (10.21)$$

$$\overline{I_{2gdq}} = \frac{\overline{V_{cdq}} k_2 - V_g}{j\omega \times k_3} \quad (10.22)$$

Where:

$$k_1 = 1 - \omega^2 L_2 C \quad (10.23)$$

$$k_2 = 1 - \omega^2 L_1 C \quad (10.24)$$

$$k_3 = L_1 + L_2 - \omega^2 L_1 L_2 C \quad (10.25)$$

$$k_1 < 1, \quad k_2 < 1, \quad k_3 < L_1 + L_2 \quad (10.26)$$

The above parameters are introduced to enable the study of fault currents. In Eq. (10.20), the parameter K_1 is the gain between V_g and I_{1g} and , similarly, in Eq. /10.22), parameter K_2 is the gain between V_c and I_{2g}. The final design parameters are L_1 , L_2 and C, which can be obtained from Eqs (10.23) to (10.25) once K_1 , K_2 and K_3 are finalized.

The converter losses will be minimal when reactive power $Q_c = 0$, implying $<V_c = <I_{2g}$, and it can be shown that this is achieved if $K_2 = K_1 S^2$, where $S = V_g/V_c$ The LCL VSC converter can achieve a 100% utilization ratio at rated power. The coefficient K_3 is dependent on the rated power only, and therefore K_1 is the only independent design parameter. The active power at V_g can be controlled using the DQ components of the converter voltage (through M_d and M_q) as with common L converters. The magnitude of current through the converter for a DC fault ($V_{dc} = V_c = 0$) relative to the rated converter current $r = I_{2g}^{fault} / I_{2g}$, can be determined from Eqs (10.20) to (10.22) as:

$$r^2 = \frac{1}{-k_1^2 s^2 + 1} \quad where \quad s = V_g / V_c \quad (10.27)$$

Figure 10.18 shows the fault current ratio from Eq. (10.27) as the function of design parameter K_1 and the stepping ratio s. The fault current will be close to the rated current for any stepping ratio and for a wide range of K_1. In general it is always possible to design the converter will be able to operate under DC voltage.

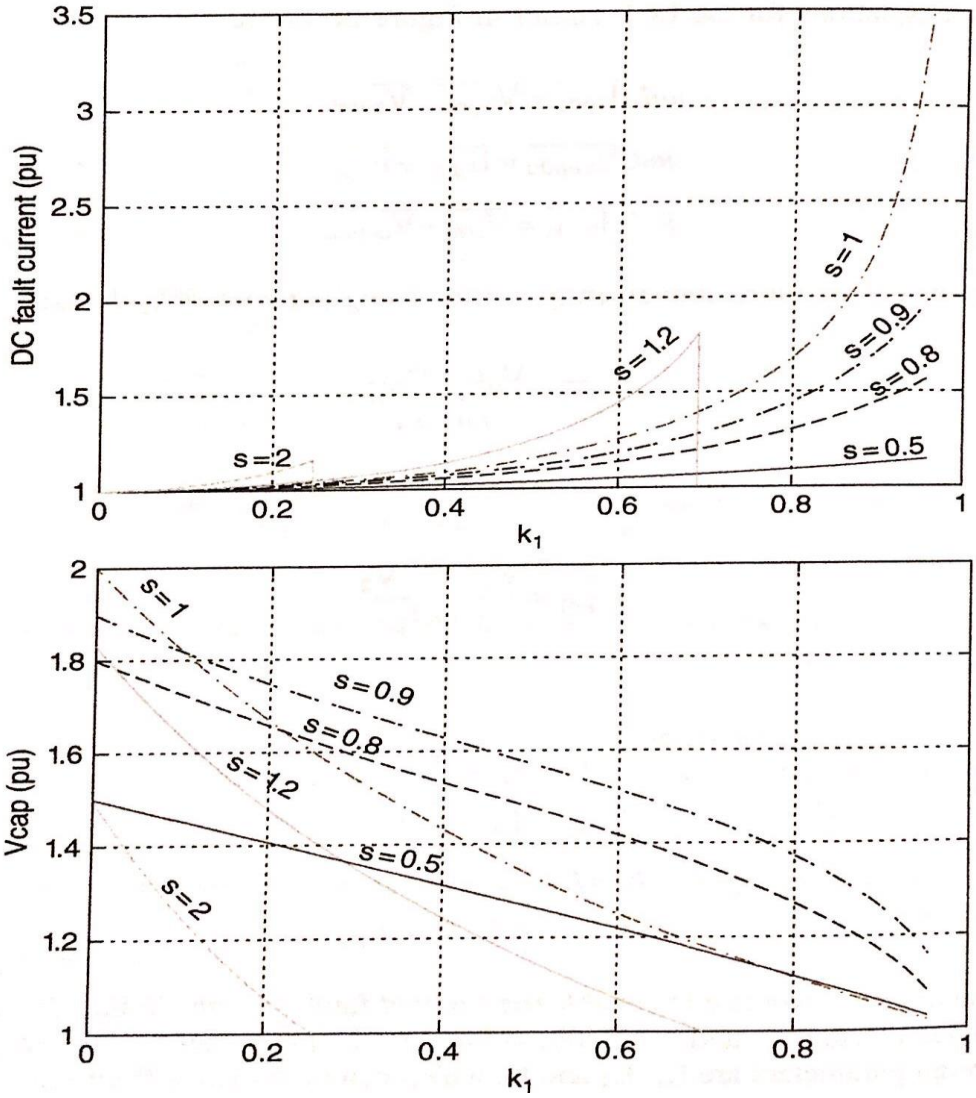

Figure 10.18 Converter DC fault current (pu) capacitor voltage (pu) (base is largest of V_g and V_c) as the function of design parameter K_1 *and* stepping ratio $s = V_g / V_c$.

On the downside, as shown in the lower graph of Figure 10.18, the capacitor voltage V_c will be typically 1.2-1.4 pu (relative to the larger of V_g and V_c), which implies some cost penalties. Another drawback of this topology is that, at a partial load, it will not be possible to maintain $Q_c = 0$, which implies which can be achieved with switchable capacitor banks.

If DC fault reduction is a high priority, it is likely that an LCL converter will have overall advantages over a common L converter.

10.11.4 Full Bridge MMC Converters

Full-bridge MMC converters can operate with low DC voltage, they can limit the DC fault current, or bring DC fault current to zero, as has been discussed in section 10.8. Therefore if all VSCs use FB MMC topology in a DC grid, like that in Figure 10.14, then the protection system would require low rated DC CBs.

The FB MMC VSC topology can reduce a DC fault current to zero and this opens the possibility of using fast DC disconnectors (zero current devices) on DC cable. Nevertheless, many further challenges would arise if the protection precondition is that current is brought to zero in all cables in a complex DC grid. The time frame for the protection operation might be increased. It could be beneficial not protection logic to accurately determine fault location.

On the downside, FB MMC topology has higher costs and operating losses.

10.11.5 VSC Converter with Fault Current Limiter

It has been is explained in section 10.6 that semiconductor or hybrid DC CBs can be used as fault current limiting devices. In such cases, the DC CB active switch is operated periodically, not unlike the DC chopper, under an active feedback current control loop. The current can be controlled to low values, even under the worst case DC faults, but the duration of this operating mode is limited by the energy capability of switches, surge arresters and the cooling equipment.

Figure 10.19 shows the VSC the converter with the DC CB acting as a fault current limiter. Jointly with the DC CB, this converter can limit the fault current like any of the topologies in the previous sections. Some manufacturers are planning to standardize a seven-switch VSC converter, as in Figure 10.19, which has capability of DC fault-current limiting and interrupting.

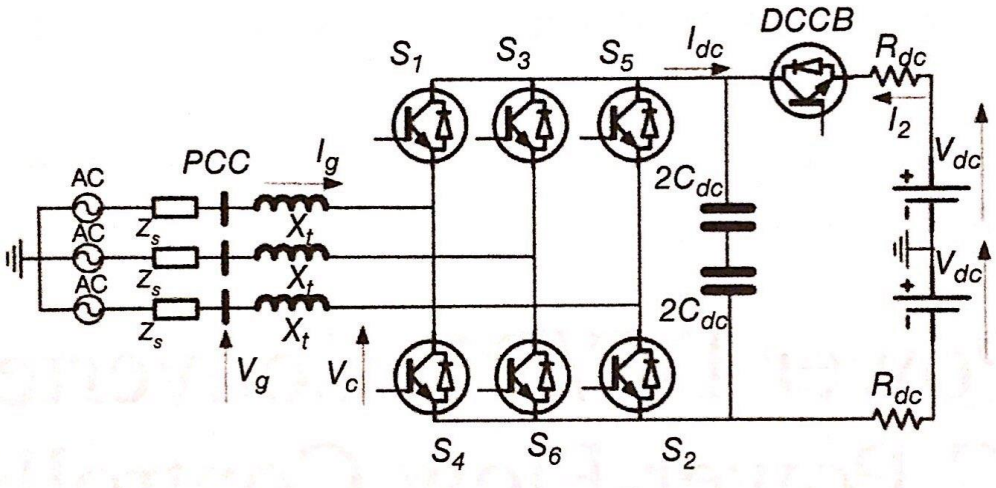

Figure 10.19 VSC converter with a DC CB operating as a fault-current limiter.

Reference Part C

DC Transmission Grids

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