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MASTERS THESIS IN ENERGY

Electrical Power Engineering

Bidirectional DC-DC Converter for Supercapacitor as DC-bus Stabilization Element

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Abstract

The demand for renewable energy from wind and solar is increasing. These energy sources are intermittent and unpredictable to a degree and require a stable but fast responding DC-grid. This is achieved by extending the requirements of the DC-grid to its stabilization element and introducing high power density energy storage. The supercapacitor is investigated in this regard to be utilized as a stabilization element. Its fast electric response makes the supercapacitor an excellent energy storage device that works well with other energy storage devices like batteries and fuel cells but also standalone. An isolated bidirectional DC-DC converter is necessary to control the supercapacitor's power flow and utilize its advantages fully.

Firstly, an isolated bidirectional DC-DC converter is simulated and integrated with a supercapacitor in Matlab®/Simulink® to meet a specific system requirement. The DC-DC converter is presented with the dual active bridge topology and single-phase-shift control strategy. Based on the results, it is investigated if the supercapacitor is a good stabilization element for a DC-microgrid.

Secondly, a supercapacitor system with integrated cell management, current and voltage sensing, over-voltage protection, and compact design is developed. The design is flexible, where one module can be connected in series or parallel to fit a custom design. In this thesis, six modules are necessitated to meet the system requirement. It is desirable to first test a prototype of one module before assembling the entire energy storage. The supercapacitor prototype is tested in the lab with a DC-load, and its transient response is compared with a simulated supercapacitor.

A conference paper on the topic of supercapacitor and lithium-ion batteries is submitted for IEEE ICECCME 2021. This paper presents our results that visualize the difference in transient response between the simulated and physical energy storage devices.

Acknowledgment

In regards to finishing my M.Sc. thesis, it is my pleasure to express the deepest gratitude towards the people who have contributed to my work during this time.

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I would also like to thank Fredrik Storebø for close collaboration and healthy discussions during a difficult time of the covid-19 pandemic. The excellent collaboration made it possible to achieve a scientific paper for ICECCME 2021. The development process for the scientific paper has been very educational and will help me participate in other collaborative works in the future.

M.R.

(MR)

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Acronyms

General

BDC Bidirectional DC-DC Converter 2
CCS Code Composer Studio 20
DAB Dual Active Bridge 2, 3, 5, 11–13, 16, 17, 21, 24, 31, 35, 36, 46, 49–53, 57–59
EC Electrochemical Capacitor 1
ESR Equivalent Series Resistance 1, 7, 8, 27, 54, XXX, XXXII
IBDC Isolated Bidirectional DC-DC Converter 3–5, 12, 21, 28, 35, 46, 52, 58
IC Integrated Circuit 29–31
IGBT Insulated-Gate Bipolar Transistor 10
Li-ion Lithium-Ion 4, 6
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor 9, 10, 16–18, 22, 24, 31, 34
OVP Over-Voltage Protection 30, 34
PCB Printed Circuit Board 20, 28, 30, 32–34
PID Proportional, Integral and Derivative 12
PLC Programmable Logic Controller 52
PWM Pulse-Width Modulation 19
RMS Root Mean Square 18
SC Supercapacitor 1–9, 12, 21, 23–30, 33–59
Si Silicon 10
SiC Silicon Carbide 5, 10
SMD Surface Mount Device 4, 30, 33
SOC State Of Charge 6, 28, 37, 50, 51, 58
SPS Single-Phase-Shift 13, 14, 16, 58
UC Ultra Capacitor 6
ZVS Zero-Voltage Switching 13, 16, 22

Signalprocessing

ADC Analog-to-Digital Converter 19
CPU Central Processing Unit 19
GPIO General-Purpose Input/Output 19

MCU Microcontroller Unit 3, 19, 31, 34, 52

Symbols

Components

C (F) Capacitance 6, 7, 16

C_{ess} (F) Required capacitance for energy storage 7

C_{tot} (F) Total capacitance 8

D (−) Duty-cycle 13

W_c (J) Energy or DC capacitance 7

E_C (J) Energy required to charge/discharge MOSFET 16

E_L (J) Energy stored in inductor 16

L (H) Inductance 16

L_k (H) Leakage inductance 14, 15, 17

$R_{DS,on}$ (Ω) MOSFET on-resistance drain to source 17, 18

R_{AC_1} (Ω) Transformer primary AC resistance 19

R_{AC_2} (Ω) Transformer secondary AC resistance 19

R_{DC_1} (Ω) Transformer primary DC resistance 18

T_{av} $(year)$ Supercapacitor average life expectancy 8

T_{exp} $(year)$ Supercapacitor life expectancy 8

ϑ (K) Supercapacitor cell temperature 8

U (V) Supercapacitor cell voltage 8

P_v (mW cm^{-3}) Transformer core loss per unit volume 18

A_e (m^3) Transformer core volume 18

Electrical

i_{AC_1} (A) Primary AC current 18, 19, 50

i_{AC_2} (A) Secondary AC current 18, 19, 50

I_{DS} (A) Drain to Source current 17

i_L (A) Inductor current 14, 15

I_L (A) Instantaneous inductor current 14–16

I_o (A) Instantaneous switching current at t_0 17, 18

I_φ (A) Instantaneous switching current at t_1 17, 18

I_1 (A) Instantaneous switching current at the end of dead time 18

I_p (A) Primary current 22

$I_{D,RMS}$ (A) RMS current through diode 18

$I_{M,RMS}$ (A) RMS current through MOSFET 17, 18

I_s (A) Secondary current 22

E_{req} (J) Required energy 7

P (W) Average power 15

P_{in} (W) Input power 14, 37, 51, 52

P_{sw} (W) Power loss from switching 17

P_{max} (W) Maximum power 15

P_{DC} (W) Diode conduction loss 17, 18

P_{MC} (W) MOSFET conduction loss 17

P_1 (W) Positive power 15

P_2 (W) Negative power 15

P_{nom} (W) Nominal power 22

P_{out} (W) Outpot power 14, 15, 37, 51, 52

P_{AC} (W) Transformer AC loss 19

P_{copper} (W) Transformer copper loss 18

P_{core} (W) Transformer core loss 18

v_{AC_1} (V) Primary AC voltage 13, 50

v_{AC_2} (V) Secondary AC voltage 13, 50

V_{DC} (V) DC Voltage 7

V_1 (V) DC voltage into the converter 14–17

V_2 (V) DC voltage out of the converter 14–17

$V_{DC,ref}$ (V) Diode forward voltage 7, 18

V_{DS} (V) Drain to source voltage 16, 17

V_L (V) Voltage across inductor 14

V_p (V) Primary voltage 22

V_s (V) Secondary voltage 22

V_{tot} (V) Total supercapacitor voltage 8, 27

d (−) Voltage transfer ratio 16

General

A (m^2) Area of capacitor plates 6

l (m) Distance between electrodes 6

η (−) Efficiency 37

ε ($F\ m^{-1}$) Permittivity of material 6

f_s (Hz) Switching frequency 14, 15, 17, 22

OS (%) Overshoot 47, 55

φ (rad) Phase-shift 13–15, 17, 22

K_P (−) Proportional constant 12, 13, 23

K_I (−) Integral constant 12, 13, 23

K_D (−) Derivative constant 12, 13

T_s (s) Period 13

T_R (s) Rise time 47

T_S (s) Settling time 47

t_{off} (s) Time interval during OFF switching 17

t_{on} (s) Time interval during ON switching 17

n (−) Turn-ratio between primary and secondary 14–16, 22

1 Introduction

1.1 Background

Renewable energy is a growing trend in today's society. Power electronics become increasingly more advanced, and renewable energy sources become more integrated into the electrical grid through microgrids [1], [2]. With intermittent energy sources like wind [3]–[6] and solar [7], [8], fast-responding energy storage is usually required to keep the DC-microgrid stable [9], [10]. For heavy loads during short intervals, a high power density storage device is a realistic option. Bidirectional power flow between the microgrid and the energy storage devices is necessary to handle the intermittent power intervals [11]. Introducing an isolated bidirectional DC-DC converter between the energy storage device and the DC-microgrid enables high switching frequency and fast response, and ensures electric isolation [12].

1.2 Literature Review

The technology behind the Supercapacitor (SC) has existed for a long time. The first Electrochemical Capacitor (EC) or SC was patented in 1957 by H.I. Becker of General Electronic. This device had to be immersed in an electrolyte pool and therefore was not very practical. It could only be applied with a low voltage of 2.5 V or less and had porous carbon electrodes utilizing a high specific surface area [13]. More patents of similar designs came through over the years [14]. It was a slow start for the SC, but in 1978, Panasonic marketed a brand called Goldcaps [15] designed as an energy source for memory backup applications. In 1982 the Pinnacle Research Institute launched a product called "PRI Ultracapacitor". It was the first SC with a low Equivalent Series Resistance (ESR) [14], [16]. Later in 1987, a Japanese company called ELNA launched a product similar to Panasonic. They introduced better electrode materials and made it possible to increase the capacitance further and decrease internal resistance in the SC [14]. By 1992, Maxwell Laboratories launched the Department of Energy Ultracapacitor Development Program [14].

1.2.1 Energy Storage

Introducing energy storage into microgrids and renewable energy is a broadly discussed topic. New trends in power electronics for the integration of wind and photovoltaic power electronics are presented in [2], and the SC is included as one of the multiple energy storage devices presented. In [4], the importance of managing intermittency in wind energy applications is discussed, and a SC is proposed as high power density short term storage. It also mentions that the SC can reinforce the DC-bus during transients to prevent low voltage drops. Other energy sources like the lead-acid battery and high-speed flywheel are also considered. A SC is presented in [5], together with a doubly-fed induction generator, to compensate for the demanded active energy output and the available wind energy input. Another similar paper in [6] investigates how a SC is used to increase the battery lifetime. The SC can undergo an order of 10^6 discharge cycles, while a lead-acid battery has a typical service life of fewer than 1000 complete cycles. Battery replacement costs can therefore be drastically reduced by introducing a hybrid energy storage system and utilizing the SC for large power fluctuations. The topic of introducing small-scale energy storage into residential areas with photovoltaic solar systems is investigated in [7]. The rooftop solar system with energy storage can potentially be cost-saving compared to large-scale plants and infrastructure investments related to energy transportation.

1.2.2 Bidirectional DC-DC Converter

For electrical energy storage devices, a Bidirectional DC-DC Converter (BDC) is essential. It enables the ability to charge and discharge the energy storage by controlling the direction of power flow. In [11], a three-port DC-DC converter is presented to control power flow between the energy storage, load, and a renewable source. The design is flexible, and bidirectional power flow is limited to the ports between the energy storage and load. High efficiency in the converter is achieved by soft-switching of all three bridges. The DC-DC converter technology is known for a long time, and in [12] from 1991, a paper on a three-phase BDC is presented with soft-switching analysis. A large number of BDC typologies are presented in [17], together with suitable control schemes for the different topologies. The reasonably popular topology Dual Active Bridge (DAB) is introduced in [18] and presents updated findings on today's technology regarding the topology with control. The DAB with switching frequencies at or below 100 kHz is widely discussed in [19]–[21]. The experimental results in [22] propose a DAB with 1 MHz switching frequency and low power, and can maintain a 90% efficiency over 16.7% load.

1.3 Objective

This thesis intends to create a simulated Isolated Bidirectional DC-DC Converter (IBDC) model integrated with a SC, implement a control system, and analyze the transient response of a simulated SC against a physical SC energy storage system.

- Develop a simulated IBDC model to control the supercapacitor power flow and be a stabilization element for a larger DC-microgrid system.
- Integrate a control system to meet the SC's unique characteristic, with pre-charge, DC-bus stabilization mode, and SC charging mode.
- Investigate the SC further by developing a simulated model to understand the required level of cell balancing.
- Develop an integrated SC system, assemble a prototype to test in the lab, and investigate the differences between the simulated SC and the physical SC's transient response.

1.4 Structure

2. **Theory**: This chapter supplies relevant theories regarding this thesis. It starts by showing the main system components to better understand the system before reading the relevant theory. The SC is explained first, followed by different DC-DC converter topologies. The DAB is expressed as the primary topology, and appropriate control method and switching strategies are introduced. Losses related to the DAB are also presented, followed by the utilized Microcontroller Unit (MCU) and relevant software tools.
3. **Method**: The method chapter is divided into three parts. First, the methods used in developing the DAB model in Matlab®/Simulink®. Second, the SC is investigated further by simulating a small part of the DAB SC with integrated cell balancing. Lastly, methods used for developing the physical SC prototype.
4. **Results**: Results are presented in chronological order based on the method chapter. Firstly, the simulated IBDC results are displayed and aim to show the DABs functionality when integrated with a SC. Following, the simulated SC module, consisting of 12 cells, is developed with passive cell balancing, followed by the physical SC prototype result.
5. **Discussion**: This chapter discusses the results from the previous chapter and compare the findings. The DAB results are compared with each other and analyzed to give an educated validation regarding to the SC. The main objective is concluded by having

the SC successfully stabilizing a DC-bus with several levels of charge. The simulated and physical SC transient response are compared, and an appropriate conclusion is made.

6. **Conclusion**: The last chapter summarizes the findings and essential developments. Future work is suggested based on the goal of achieving a physical IBDC prototype and assembling a complete SC prototype of higher voltage level.

Appendices: The appendices contains IEEE conference paper submissions and the full description of the developed simulation models and prototype design documentation.

A **ICECCME 2021 Conference Paper**: The first appendix contains the conference paper submitted for review to IEEE ICECCME 2021. It aims to present a comparison between SCs and Lithium-Ion (Li-ion) batteries and their difference transient response to a DC-load.

B **SEST 2021 Approved Conference Paper Abstract**: This abstract is approved for the SEST 2021 conference and includes the same content as the paper submitted for ICECCME 2021. Due to the covid-19 lockdown of the campus, the physical model development was postponed, which resulted in not making the conference deadline.

C **Matlab®/Simulink® Diagrams**: Complete selection of Matlab®/Simulink® diagrams related to the developed models.

D **Component Parameters**: Tables visualizing the datasheet parameters for the relevant components used in all models.

E **Source Code**: Initializing code for the Matlab®/Simulink® models, and source code for the Power/Phase-shift graph in fig. 4.2.

F **Integrated Supercapacitor System Design**: In this appendix the complete schematic for the integrated SC system design, is included. It also display the layout of the different copper layers and Surface Mount Device (SMD) components, and finally a 3-D diagram of the complete design.

G **Supercapacitor Module Component List**: Lastly, the components used in the physical SC development, are presented.

2 Theory

This chapter presents the relevant theories regarding this thesis. Firstly, the SC is explained together with essential aspects of the energy storage device. Secondly, a brief description is given of the potential DC-DC converters. This is done to show the selection process of the most suitable converter before choosing the DAB. The switching device used is mentioned together with the semiconductor material Silicon Carbide (SiC), which is excellent for high switching speeds. The control method and switching strategy used are described in great detail. Aspects regarding the DAB and the chosen switching strategy are also specified to understand the topology limitations. Improvements to the design can then be realized. Lastly, the control card used in the physical implementation is described, followed by the relevant software for the whole thesis.

The block diagram in fig. 2.1 aims to provide an overall understanding of the central elements in this thesis before reading the following theories. This consists of the SC, the IBDC, and a DC-bus.

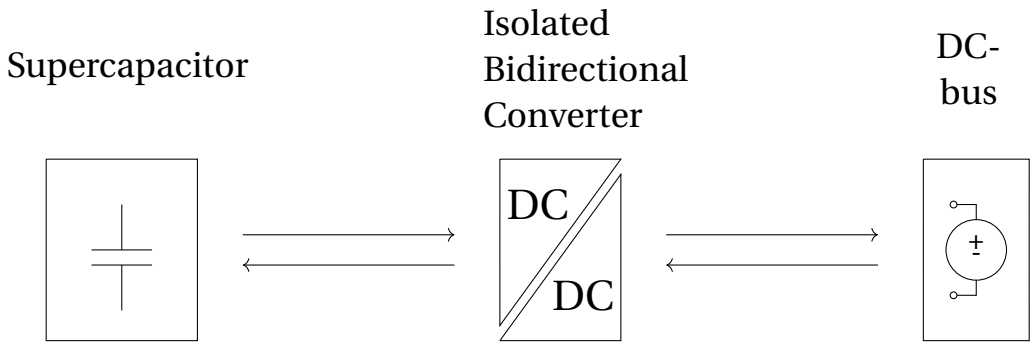


Figure 2.1: Block diagram of the main system components with the supercapacitor, the isolated bidirectional DC-DC converter, and a DC-bus

2.1 The Supercapacitor

Batteries have for a long time been the main power supply in high power electronics due to their significant energy density. They have been the best solution even with a low power density, relatively long charging time, and limited charging cycles [23]. With the SC/Ultra Capacitor (UC), it is possible to achieve similar energy storage capabilities of the battery while maintaining the charge/discharge characteristics of the capacitor [2], [24], [25]. The voltage of a Li-ion battery has minimal variation in voltage between 20% and 80% State Of Charge (SOC). For the SC, this is very different, as the voltage will increase linearly with its SOC. The linear charge makes it easy to predict its SOC but complicates the SC's control and use as a controlled energy storage device. The control either has to adjust the power transfer or compensate for the decreasing voltage with increased current.

The conventional capacitors used in electronics are usually either electrostatic or electrolytic and have much smaller capacitance than the SC. Capacitance (C) is calculated in

$$C = \frac{\varepsilon A}{l}, \tag{2.1}$$

where ε is the permittivity of the dielectric material, A denotes the area of the plates and l represents the distance between them [25], [26].

A capacitor of one farad will store one coulomb (C) of charge when charged with one volt [25]. SC consists of two electrodes, a separator, and an electrolyte. When charged, ions in the ionic electrolyte are forced towards the oppositely charged electrodes. The two types of ions are called anions and cations, respectively, to the anode and cathode. These are located inside the electrolyte right next to the electrode. This way, the excess charge from the electrically conducting side of the phase boundary is balanced [27].

Across each phase boundary, there are two layers of opposite polarity of access charge. The electrodes are made of activated carbon and provide a high surface area leading to large capacitance. The distance between them is also much smaller in SCs than regular capacitors [27].

Usually, SC are placed in two groups: double-layer capacitors and electrochemical capacitors. The double-layer capacitor applies double-layer effect, a phenomenon originating on both electrodes from ions in the electrolyte. The electrochemical capacitor also uses double-layer effect but stores electrical energy by redox reactions on the electrode surfaces to increase the capacitance. The reversible redox reaction is a combination of oxidation and reduction where electrons are exchanged between electrolyte and electrode [28], [29].

The extensive practical difference between a battery and a SC is power density versus energy

density. While a SC can release large amounts of energy in a short period, a battery can store more significant amounts of energy. This is why a SC has high power density while a battery has high energy density [30]. The energy stored, denoted by W_c, can be calculated by

$$W_c = \frac{1}{2} C {V_{DC}}^2, \tag{2.2}$$

where C indicates total capacitance and V_{DC} expresses total DC voltage [31].

2.1.1 Charging

Charging of a SC is done with either constant voltage or constant current. Both methods are also used for rechargeable batteries [23]. Constant voltage is usually simpler but takes a longer time considering the charge current will decrease as the SC voltage increases. With this method, the current needs to be limited by a pre-charge resistor. The charge current is limited until the voltage reaches a certain level and the pre-charge resistor is bypassed with a switch. The SC has a very low ESR which is why the charging current must be limited. Constant current is more reliable than the constant voltage since the charging current remains constant. Hence, the SC voltage will increase continuously. This method requires a charger/converter which adjusts the charging voltage.

2.1.2 Sizing

When sizing a SC energy storage, it is important to map the required energy amount. The energy amount stored in a SC depends on the capacitance, as expressed by eq. (2.2). In [4], the required energy is chosen to supply enough energy during a low voltage condition. This energy storage sizing method will vary depending on the target system. The capacitance of the energy storage system, denoted C_{ess}, can be calculated using

$$C_{ess} = \frac{2\ E_{req}}{{V_{DC,ref}}^2}, \tag{2.3}$$

where E_{req} indicates the energy required and $V_{DC,ref}$ is expressed as the maximum voltage across the device [4]. Noting that eq. (2.3) is a rearrangement of eq. (2.2).

2.1.3 Aging

SC can undergo a much higher number of charge and discharge cycles than batteries due to no chemical reaction in the electrodes. However, the organic electrolyte material used has a low decomposition voltage. A single SC, referred to as one cell, has a limited cell voltage of around 2.7 V, and necessitates the connection of multiple cells in series to achieve a

higher voltage. When doing so, it becomes a real challenge to balance the voltage of each cell. Alterations in capacitance and ESR of each cell will affect the charging time. Therefore, cell balancing is crucial to prevent the cells from experiencing overvoltage, which can significantly reduce its lifespan [27].

2.1.4 Supercapacitor in Series

When connecting multiple cells in series, a higher voltage is reached while the capacitance is reduced [32], [33]. The total voltage equals the voltage of each cell added together. The total capacitance equals the capacitance of each cell divided by the number of cells if these are identical. Both the total voltage, V_{tot}, and the total capacitance, C_{tot}, are calculated by

$$\begin{aligned} V_{tot} &= V_1 + V_2 + V_3 + \cdots V_n \,, \\ C_{tot} &= \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \cdots \frac{1}{C_n} \right)^{-1} , \end{aligned} \tag{2.4}$$

where V_i and C_i for n number of cells are valid for $i = 1,\ 2,\ 3,\ \cdots,\ n$ [34]. It must be noted that this capacitance will never be completely identical in every cell.

2.1.5 Life Expectancy

The main factors that will reduce the lifespan of a SC is overvotlage and temperature. In [27], T_{exp} is expressed as the life expectancy of a SC and is presented by

$$T_{exp}(U, \vartheta) = c_1 e^{\left(\frac{U}{c_2} + \frac{\vartheta}{c_3}\right)}, \tag{2.5}$$

where ϑ and U are introduced as the temperature and cell voltage, respectively. $c_1 - c_3$ are constant parameters of negative value, derived from a linear relationship between cell-voltage and life expectancy [27]. By measuring the wear on a SC over a longer time period, the average life expectancy, T_{av}, of a dynamic voltage profile, $u(t)$, can be calculated by

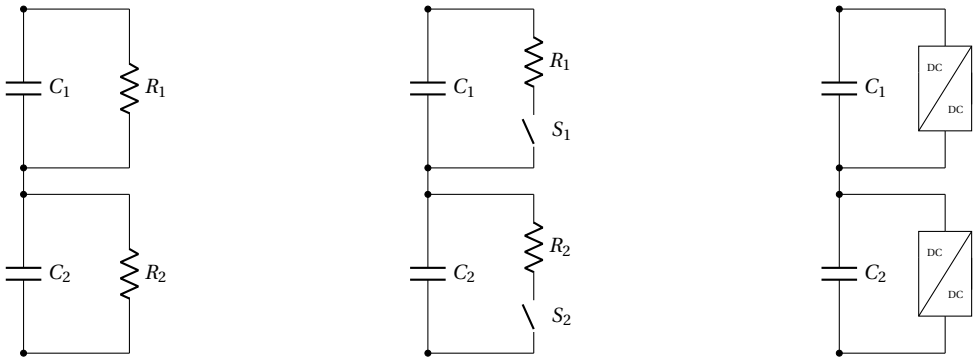
$$T_{av}(u(t), \vartheta) = \frac{t_1 - t_0}{\int_{t_0}^{t_1} \frac{1}{T_{exp}(u(t), \vartheta)}\, dt}, \tag{2.6}$$

where the times t_0 and t_1 indicate start and finish of the dynamic voltage profile.

2.1.6 Cell Balancing Circuits

As explained in section 2.1.3, it is important to make sure the voltage of each cell does not exceed maximum voltage when connecting multiple cells in series. A balancing circuit is added in parallel to each cell to prevent the SC from experiencing over-voltage. The type of method can be divided into passive and active, as shown in fig. 2.2. Each circuit shows two SCs in series for simplicity, which can be a quite large amount [27], [34]–[36]. The passive method, often consisting of a single resistor in series with a switch, is a cheap and easy way to protect a SC, seen in fig. 2.2b. When the voltage across a cell reaches a certain voltage, the switch closes and dissipates some of the energy through the resistor, preventing the voltage from rising too quickly [35]. It is also common to drop the switch and have a constant power draw through the resistor, as in fig. 2.2a. The balancing current will increase as the cell voltage increases.

Active cell balancing requires more work and is more expensive. This method will usually consist of a DC-DC converter in parallel to each cell, like in fig. 2.2c, actively moving current between cells when they charge un-even. This method is usually not necessary when using capacitors of about the same capacitance and quality [32], [34]–[36].



(a) Resistor (b) Switched resistor (c) Active

Figure 2.2: Cell balancing methods

2.2 Power Transistor

A switching device with a high switching speed is required to utilize the fast response of the SC. The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), is a switching device used in many high-power applications. It is a device that has been used since the early 1980s and is known for its fast switching capabilities [37].

2.3 Silicon Carbide

SiC is a semiconductor material and a contender to the traditional Silicon (Si) used in switching devices. With SiC it is possible to produce MOSFETs at voltage levels up to 10 kV with die areas greater than 0.64 cm^2. According to [38], SiC DMOSFETs can offer a 50% reduction to power losses with less than half the die size compared to a Si Insulated-Gate Bipolar Transistor (IGBT). Due to large tail losses and reverse recovery charge of Si devices, the switching frequency is limited. Higher switching frequencies can be realized with SiC devices [39], [40].

2.4 DC-DC Converter Type and Topology

There are many different types of converters, and it is vital to decide the specific design based on the desired result. They are classified into two main categories: Isolated and un-isolated [17]. The different power supplies must be electrically isolated from the DC-grid and loads in electric vehicles [21] or marine vessels [41]. Another critical decision is to choose between a basic topology or a full-bridge/half-bridge topology.

2.4.1 Buck-boost

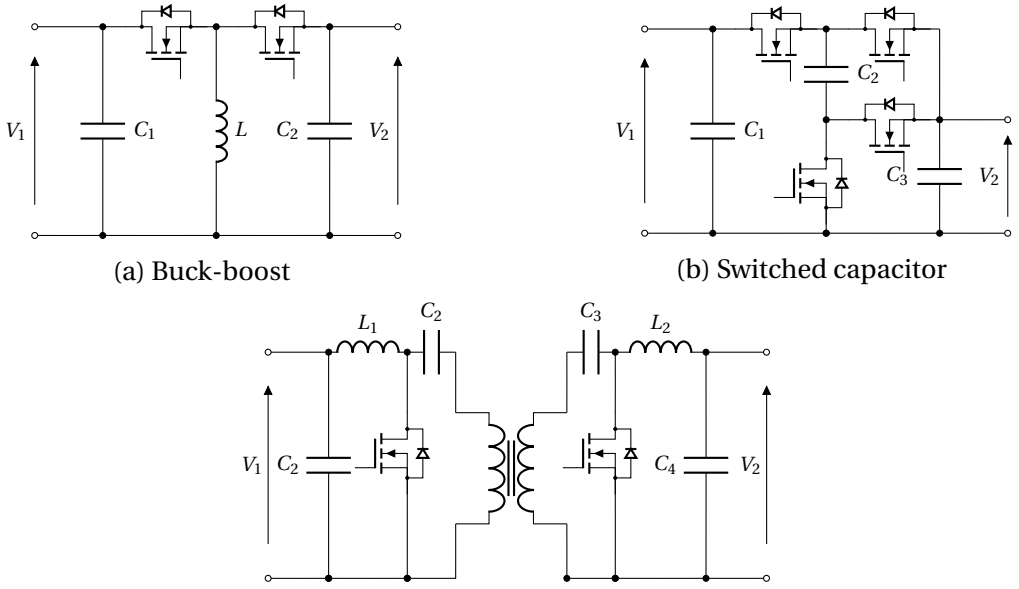
A common DC-DC converter for applications that do not require galvanic isolation is the buck-boost. It is derived from the unidirectional converters buck and boost, and combined into one using a bidirectional switch, shown in fig. 2.3a. This results in a basic bidirectional converter with the ability to buck or boost the voltage. Due to the bidirectional capability, the converter can provide this for both directions of power flow with a negative output [17].

2.4.2 Switched-capacitor

Another typical un-isolated DC-DC converter is the switched-capacitor topology. The purpose of the switched-capacitor in the converter is to enhance its voltage-boosting capability further. This topology does not include an inductor, which most converters do (fig. 2.3b). This makes the converter lighter due to the inductor's extra weight and avoids magnetic utilization. Also, since there is no inductor, it can be applied a continuous current. The continuous current is realized by adding multiple switched capacitor converters together. By combining switches and a capacitor into a cell, multiple cells can be combined into a string, done in [42]. Two similar strings in parallel can be operated in the anti-phase to achieve continuous current. One can simply add more cells to further extend the continuous current operating area [17], [43], [44].

2.4.3 Cuk

The isolated bidirectional cuk is based on the un-isolated cuk and derived from it. Inductors on the input and output of the converter ensure that current ripples can be eliminated. This is recommended for many applications with varying supply current, such as intermittent energy production. It includes a continuous input and output current based on the voltage gain of the transformer (fig. 2.3c) [17], [45].



(a) Buck-boost

(b) Switched capacitor

(c) Isolated cuk

Figure 2.3: Bidirectional DC-DC converter topologies

2.4.4 Dual Active Bridge

The DAB is a widely used topology and consists of two back-to-back full-bridge converters, one on each side of a high-frequency transformer. This makes the converter suitable for applications that require bidirectional power flow. In total, there are eight active power switches, shown in fig. 2.4 [18], [22]. The many power switches make the converter capable of transferring large amounts of power, since its power transferring capabilities increase with the number of power switches [17]. The inductor is placed on the high voltage side bridge. It is a flexible topology that consists of half-or full-bridges and is either current or voltage fed. Leakage inductance is directly affected by inductance in the transformer and inductor, which is crucial to achieving the correct power transfer [19], [22]. Capacitors on both sides of the DAB should be designed to limit a voltage ripple within a certain percentage, dependent on the use [46].

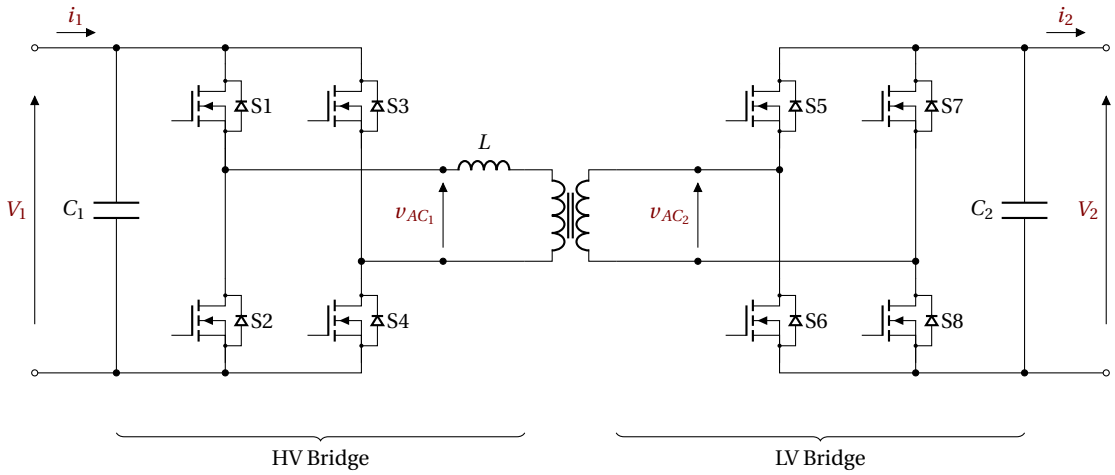


Figure 2.4: General dual active bridge topology

2.4.5 Electrical Isolation

The two bridges in the DAB is separated by a high frequency transformer which makes it a IBDC [47]. The galvanic isolation is great for protecting large energy storage systems consisting of batteries or SC connected to a grid [20] and essential in applications for electric vehicles [21] and marine vessels [41].

2.5 Control Method

There are multiple control methods suitable for IBDC. Different control strategies can be utilized on the same system simultaneously. This way, it is possible to overcome the drawbacks of a single strategy and draw out multiple benefits.

2.5.1 PID-controller

The Proportional, Integral and Derivative (PID) controller is a well-documented control scheme. It is used in many applications and might be combined with other schemes. The controller utilizes three different parts: Proportional, integral and derivative [17]. The proportional part gives a change to the input signal equal to the control error. The integral part of the controller applies a change to the input equal to the integrated error. Its main purpose is to eliminate offset in the output response. As for the derivative part, the input is changed according to the derivative error. This part is less commonly used than the proportional and the integral part and is usually used to stabilize the system or speed up a response [48]. One version of expressing the PID's control action is described in

$$K_P + K_I\,\alpha(z) + K_D \frac{N}{1 + N\,\alpha(z)}, \tag{2.7}$$

where K_P, K_I, and K_D denote the proportional gain, integral gain, and derivative gain respectively, N expresses the filter coefficient, and $\alpha(z)$ indicates the discrete-time integrator of the plant [49].

2.6 Switching Strategy

There are multiple strategies when it comes to switching patterns of semiconductor devices. In the journal article [18], an isolated DAB is investigated for the different switching strategies: Single-Phase-Shift (SPS), extended-phase-shift, dual-phase-shift and triple-phase-shift. The method SPS is widely used and well documented because of its easy implementation and simple philosophy [18], [50], [51]. While SPS only focus on shifting the signals from one bridge with respect to the other, extended-phase-shift extends the control to the two switch-pairs in the same bridge also. This is referred to as an "inner" phase-shift. Hence, enabling a third voltage level and reducing the converter losses. Double-phase-shift again takes the control further, extending the extended-phase-shift principle to both full-bridges. This "inner" phase-shift is the same for both bridges. With triple-phase-shift, however, the "inner" phase-shift need not be the same for both bridges and is regulated separately, introducing a third phase-shift signal. The different methods increase the level of efficiency in the converter and may extend the level of Zero-Voltage Switching (ZVS). This is discussed further in section 2.6.1.

The switching patterns, voltages and current of SPS is visualized in fig. 2.5. all of the switches are operated with a 50% duty-cycle ($D = 1/2$) which gives currents and voltages half-cycle symmetry. This means that the AC voltages v_{AC_1} and v_{AC_2} of each respective bridge will switch between positive and negative, as described in

$$\begin{aligned} v_{AC_1}(t + T_s/2) &= -v_{AC_1}(t), \\ v_{AC_2}(t + T_s/2) &= -v_{AC_2}(t), \end{aligned} \tag{2.8}$$

where t expresses the time and T_s indicates one period [18], [52].

S1 and S4 are operated by the same gate signal which respectively is the opposite of S2 and S3. By shifting the gate signals of the two bridges with respect to one another the energy flowing through the DAB will change. Energy flows from the leading to the lagging bridge. This can be realized by simply delaying the gate signals. Fig. 2.5 shows the principle behind SPS and the phase-shift angle φ between the two bridges [46].

Maximum power transfer will occur when $\varphi = \pi/2 = 0.5\,\pi$ rad. This is equivalent to 90°

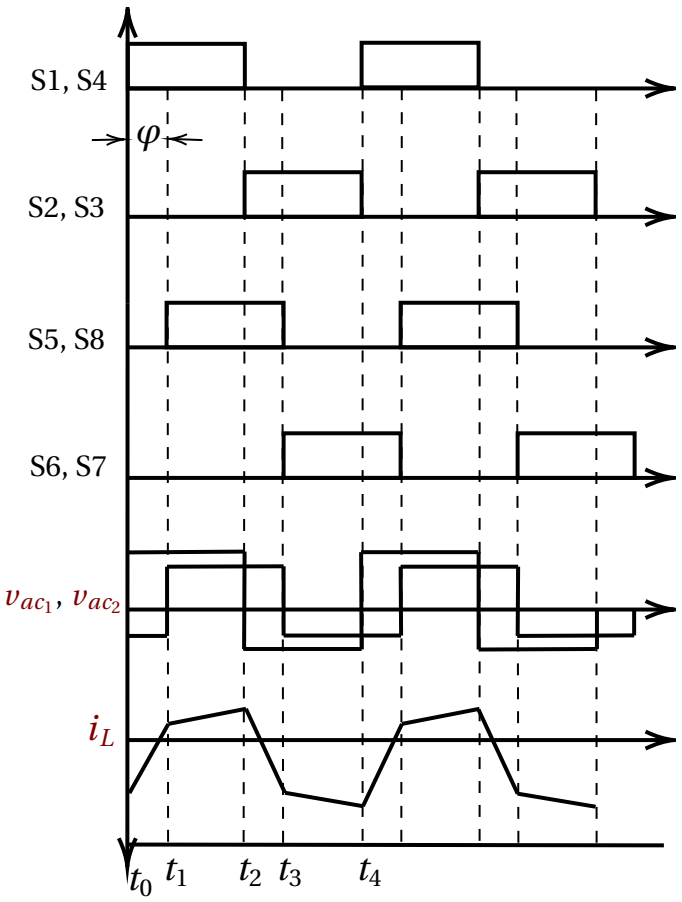


Figure 2.5: Operating principle of single phase-shift modulation as a switching strategy

phase-shift and will be referred to as the theoretical maximum. The times t_0 - t_4 represents one period of SPS. The following analysis requires a lossless model and the statement $P_{in} = P_{out}$ is correct [46], [52], [53]. Hence, the inductor voltage, V_L, is expressed as

$$V_L = V_1 - nV_2, \tag{2.9}$$

where V_1 and V_2 denote the input and output voltages, respectively, and n indicates the turn-ratio between the input and output. By performing the following integral, a general relationship for the inductor current, i_L, is expressed by

$$i_L = I_{L,t_0} + \frac{1}{L_k}\int_{t_0}^{t_1} V_L \, dt, \tag{2.10}$$

where I_{L,t_0} denotes the instantaneous inductor current at time t_0 and L_k express the total leakage inductance. The current, I_{L,t_0}, is calculated by

$$I_{L,t_0} = \frac{\pi(nV_2 - V_1) - 2\varphi nV_2}{4\pi f_s L_k}, \tag{2.11}$$

where f_s indicates the converters switching frequency and φ denotes the required phase-shift. The inductor current, i_L, can then be described from t_0 to t_2 using the same principle from eqs. (2.10) and (2.11), representing the first half of the period, expressed as

$$\begin{aligned} i_L(t) &= (I_{L,t_0} + (V_1 + nV_2)\,t/L_k \qquad \forall \quad t_0 < t < t_1, \\ i_L(t) &= (I_{L,t_1} + (V_1 - nV_2)(t - t_1)/L_k \quad \forall \quad t_1 < t < t_2, \end{aligned} \tag{2.12}$$

where I_{L,t_1} denotes the instantaneous inductor current at time t_1. Hence, it is possible to describe the negative half of the period, as the positive and negative are opposites. The equation for transferred power can then be derived. Positive and negative power will be P_1 and P_2 respectively, described as

$$P = P_1 = P_2 = \frac{nV_1V_2\varphi\left(\pi - |\varphi|\right)}{2\pi^2 f_s L_k} \quad \forall \quad -\pi < \varphi < \pi. \tag{2.13}$$

By rearranging eq. (2.13) it is possible to derive an equation for the required leakage inductance, expressed as

$$L_k = \frac{nV_1V_2\varphi\left(1 - |\frac{\varphi}{\pi}|\right)}{2\pi^2 f_s P_{out}} \quad \forall \quad -\pi < \varphi < \pi. \tag{2.14}$$

As mentioned, the maximum power transfer occurs when the phase-shift is $\pm\pi/2$ [52]. The maximum power, P_{max}, is derived as

$$|P_{max}| = \frac{nV_1V_2}{8f_sL_k} \quad for \quad \varphi = \pm\frac{\pi}{2}, \tag{2.15}$$

and gives an indicator for the converter's required leakage inductance. The required phase shift can also be derived for a given power transfer by rearranging eq. (2.13), expressed as

$$\varphi = \frac{\pi}{2}\left[1 - \sqrt{1 - \frac{8f_sL_k|P|}{nV_1V_2}}\right] \quad \forall \quad P < |P_{max}|, \tag{2.16}$$

where P denotes the average power.

2.6.1 Soft Switching

A significant advantage of both DAB and SPS is that soft-switching can be realized. ZVS is possible for most of the switching instances and depends on the amount of energy stored in the inductor and the converter's voltage transfer ratio, d, expressed as [46], [51], [54]

$$d = \frac{V_1}{nV_2}. \tag{2.17}$$

The ZVS phenomenon occurs right before the switches in a bridge go from off-state to on-state. The energy stored in the inductor will discharge the MOSFETs capacitance during a small dead-time between the two states. As a result, the voltage across the MOSFET remains close to zero. This is dependent on E_L which indicate the amount of energy stored in the inductor, expressed as

$$E_L = \frac{1}{2} L \, {I_L}^2, \tag{2.18}$$

where L indicates the inductance and I_L denotes the inductor current. Now, E_L has to be sufficient to charge and discharge the MOSFETs output capacitance, E_C, to achieve ZVS for as many switches as possible, expressed by

$$E_C = \frac{1}{2} C \, {V_{DS}}^2, \tag{2.19}$$

where C denotes the MOSFET capacitance and V_{DS} indicates the drain-source voltage. When the capacitor is fully discharged, the MOSFET's parallel diode will conduct a small current, keeping the voltage close to zero as the switch closes [46].

2.7 Losses Related to Dual Active Bridge

All losses relating to the DAB are presented in this section. Firstly, switching and conduction losses in the power switches[53], followed by transformer and inductor [46]. The temperature of the components is an essential aspect of loss and efficiency. For the following equations to be valid, the semiconductor device has to be adequately cooled, with heat-sinks if necessary, and kept within its temperature operating limit set by the manufacturer. When the temperature becomes too high, the efficiency tends to plummet.

Switching losses

The switching losses in a MOSFET is calculated by

$$P_{sw} = \frac{1}{2} V_{DS} I_{DS} t_{on} f_s, \tag{2.20}$$

where V_{DS} and I_{DS} denote the voltage and current with reference drain to source. t_{on} and t_{off} indicate the transition times between on- and off-switching. A switching instance of turn-on will start with the drain-source voltage decreasing and the current increasing. The two currents calculated in eq. (2.12) can be solved for t_0 and t_1 and rearranged as

$$I_o = -\frac{(V_1 + V_2)\varphi + (V_1 - V_2)(\pi - \varphi)}{4\pi f_s L_k}, \tag{2.21}$$

and

$$I_\varphi = \frac{(V_1 + V_2)\varphi - (V_1 - V_2)(\pi - \varphi)}{4\pi f_s L_k}, \tag{2.22}$$

where I_o and I_φ denote the instantaneous switching currents at t_0 t_1, respectively. Eq. (2.20) can then be solved by setting $V_{DS} = V_1$ and $I_{DS} = I_o$.

Conduction losses

Conduction losses are divided into two parts. The first for P_{DC}, which denote the MOSFET conduction loss, derived as

$$P_{MC} = R_{DS,on}\ {I_{M,RMS}}^2, \tag{2.23}$$

and the second for P_{DC}, indicating the diode conduction loss, derived as

$$P_{DC} = V_D \; I_{D,RMS}, \tag{2.24}$$

where $R_{DS,on}$ identifies the on-resistance for the MOSFET and V_D is the diodes forward voltage drop. $I_{D,RMS}$ and $I_{M,RMS}$ are the Root Mean Square (RMS) currents through each respective component, expressed as

$$I_{D,RMS} = \sqrt{\frac{D_1}{3}({I_o}^2 + I_o I_1 + {I_1}^2)}, \tag{2.25}$$

and

$$I_{M,RMS} = \sqrt{\frac{D_2}{3}{I_1}^2 + \frac{D_3}{3}{I_\varphi}^2 + \frac{D_4}{3}({I_o}^2 + I_o I_\varphi + {I_\varphi}^2)}, \tag{2.26}$$

where the dead time is D_1, denoting the diodes conduction duration. I_1 is the current at the end of the dead time and depend on the duration of D_1 and choice of MOSFET driver. The durations $D_2 - D_4$ are all times when the MOSFET is conducting.

Transformer losses

This part is inspired by [46], due to the example of an actual planar transformer from Payton Planar Magnetics. Losses related to the transformer are divided into three parts: Core, copper, and skin effect. Core loss in the transformer is found by multiplying P_v, denoting core loss per unit volume, with A_e, the volume of the core, expressed in

$$P_{core} = P_v A_e. \tag{2.27}$$

These values will be listed in the core's datasheet. Copper losses, P_{copper}, are calculated by

$$P_{copper} = {i_{AC_1}}^2 + R_{DC_1} + {i_{AC_2}}^2 R_{DC_1}, \tag{2.28}$$

where R_{DC_1} and R_{DC_1} denote the DC resistance in the respective primary and secondary winding. This resistance is listed in the manufacturer's datasheet. i_{AC_1} and i_{AC_2} indicates the primary and secondary AC currents, respectively, and are in this section used as RMS value. Skin effect is increasing with the switching frequency [55]. As a result, higher switching frequencies give a higher AC resistance and loss. Losses in the transformer related to AC can be calculated by

$$P_{AC} = {i_{AC_1}}^2 R_{AC_1} + {i_{AC_2}}^2 R_{AC_2}, \tag{2.29}$$

where R_{AC_1} and R_{AC_2} denote the transformers primary and secondary AC resistance.

Inductor losses

Losses related to the inductor are from both DC and AC resistance in the coil. With a high switching frequency, the coils AC resistance will be the most relevant component, considering increased skin effect and eddy current formation [46].

2.8 Microcontroller - LaunchPad F28379D

Texas Instruments manufacture a number of different control boards, or MCUs, for all kinds off applications. The C2000 Delfino F28379D LaunchPad is such a board, with two TMS320C28x 32-bit Central Processing Unit (CPU)s. The CPUs run a frequency of 200 MHz which enables high precision. Features, such as 16-bit and 12-bit Analog-to-Digital Converter (ADC)s, Pulse-Width Modulation (PWM) outputs, and a large number of General-Purpose Input/Output (GPIO)s make it a good choice for fast switching applications [56].

The ADCs used in the Launchpad are successive approximation (SAR) ADCs and have a sampling speed of 40 MHz. Single ended 12-bit or differential 16-bit mode can be selected. The ADC inputs on the controlcard can handle an input voltage between V_{REFLO} and V_{REFHI}, which is set by the card's supply voltage V_{DDA} and V_{SSA}, and is between $0-3.3$V [56]–[58]. The GPIOs use the same supply and reference as the ADCs.

2.9 Software Tools

In this section, the relevant software tools will be introduced. The software is downloaded and used on a desktop computer with a Windows 10 Pro version 20H2, 64-bit operating system.

2.9.1 Mathworks Matlab® version R2020B and Simulink® v10.2

Matlab® is a software tool designed for a large number of uses. With a unique programming language, Matlab® is used to solve advanced equations and problems. Simulink® is a platform within Matlab® that enables implementation of physical simulation and directly transferring a concept to code [59]. Essential add-ons during the course of thesis:

- Simulink v10.2

- Simulink Control Design v5.6
- Simscape v5.0
- Simscape Electrical v7.4
- Embedded Coder Support Package for Texas Instruments C2000 Processors v20.2.0
- System Identification Toolbox v9.13
- Stateflow v10.3
- Simulink Coder v9.4
- Embedded Coder v7.5
- MATLAB Compiler v8.1
- Matlab Coder v5.1

2.9.2 Code Composer Studio V10.1.1

Code Composer Studio (CCS) is an integrated Development Environment Specially designed to support Texas Instruments' microcontrollers. It is used to develop and debug embedded applications as well as run example programs. Features like source code editor, debugger, project build environment, and optimizing C/C++ compiler are all features found in CCS.

2.9.3 KiCad V5.1.7 and KiCad Libraries V1.4

KiCad is a cross-platform and open-source electronics design automation suite used to develop Printed Circuit Board (PCB)s. Components are placed in a schematic view to connect the different ports properly. The 3D viewer enables the user to see the PCB visually before manufacturing. Component libraries can be included with the tool KiCad Libraries.

3 Method

This chapter describes the methods used during testing and development of the three main parts of the thesis. Firstly, the methods used for the IBDC model in Matlab® / Simulink® together with a SC (section 3.1), is described. Secondly, the SC is investigated further as a crucial element to the IBDC. A SC design for a 30 V module with integrated cell balancing (section 3.2) is developed in Matlab® / Simulink®. Third, a physical prototype of the SC module is developed with several features of an integrated system (section 3.3). The Simulink® diagrams, component parameters, source code, and the prototype system design in this chapter are displayed in appendices C to F. The Matlab® / Simulink® models and code are made available in the *IBDC_DAB_SC_Matlab-Simulink* Github repository [60]. The schematics and layout for the integrated SC system design are included in the *Integrated_SC_system_Kicad* Github repository [61]. Both repositories are open-access and available to the public.

The SC used together with the DAB has a voltage level of 180 V. This is achieved by connecting six 30 V modules in series. It is divided into respective sections, which in detail describe the methods used for each part. For the Matlab® /Simulink® implementations, standard component from the Simscape library (section 2.9.1) is utilized and show satisfactory results.

3.1 DC-DC Converter Model in Matlab®/Simulink®

The DAB is implemented in Matlab® / Simulink®. This section dives into the details regarding the simulated DAB and aims to prepare the physical development of a IBDC. All Simulink® diagrams are included in appendix C.1 with the required workspace variables from appendix E.1. The primary bridge is connected to the SC, while the DC-bus is connected to the secondary bridge, displayed in appendix C.1.1. Therefore, the inductor is placed on the high voltage side, which differs from fig. 2.4. The simulation model used in this section is shown in fig. 3.1. The system specification for this simulation is found in table 3.1, with bridge 1 being the primary and bridge 2 being the secondary.

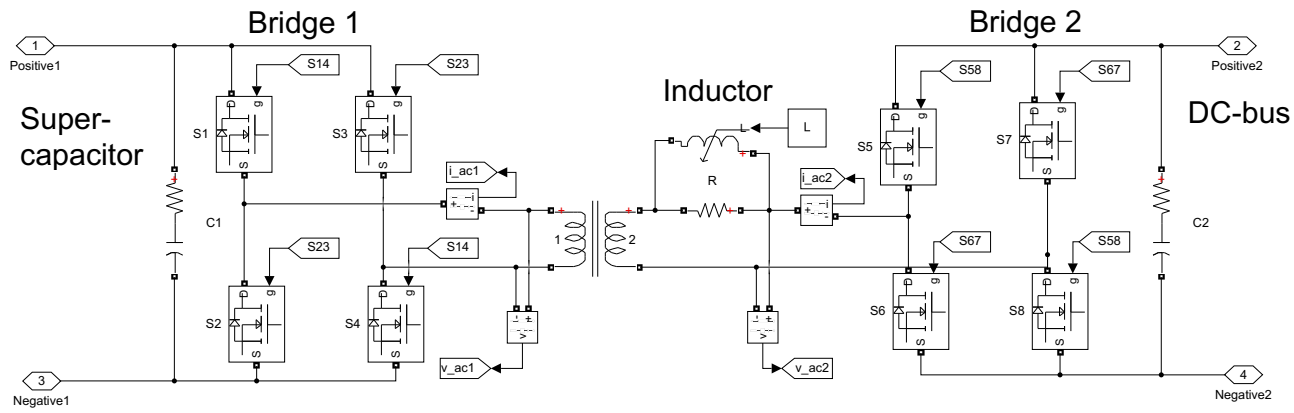


Figure 3.1: Dual active bridge model in Matlab® /Simulink®

3.1.1 Operation Principles

Operation principles in this section are directly linked to the theory described in section 2.6. The MOSFET gates are operated with two signals for each full-bridge. This is displayed in appendix C.1.2. The small dead-time needed for ZVS is ensured by operating the gate signals with a 49% duty-cycle, instead of 50% (theory in section 2.6.1). The STOP signal is also displayed, which is operated by four switches and sets the gate signals to zero when initiated. This is to simulate an emergency stop. Appropriate blocks are selected from the Simscape library (section 2.9.1).

Table 3.1: System specifications for dual active bridge model

Name	**Value**
Primary Voltage V_p Max/Min	180/90 V
Secondary Voltage V_s	340 V
Nominal Power P_{nom}	1000 W
Primary Current I_p Max/Min	11.4/5.7 A
Secondary current I_s	3 A
Frequency f_s	250 kHz
Phase-shift φ	$\left[-\frac{\pi}{2}, \frac{\pi}{2}\right]$
Turn Ratio n	9:17

3.1.2 Operation Modes

The model is operated under two main modes: Stabilize and charge. Before the model can be used, a pre-charge signal has to be activated. This will initiate a pre-charge sequence and charge the DC-bus capacitor. After the DC-bus capacitor is charged, the converter can be used and the desired mode is selected. Stabilize mode utilizes a voltage PI-regulator and aims to keep the DC-bus at a constant voltage of 340 V. Charge mode is selected to charge the SC by constant current. For simulation purposes, a voltage source is connected to the DC-bus when this mode is active to simulate a stable DC-bus.

3.1.3 Control

Control of the phase-shift is achieved by two PI-regulators, displayed in appendix C.1.3. The derivative part is not necessary to reach the desired result. The relevant theory regarding the PI-regulator is found in section 2.5.1. Averaging blocks are selected to filter the input signal, while switches are utilized to choose between the two operating modes. Both PI-regulators are tuned with the *Simulink Auto Tuner App*. The auto tuner is a built-in tool that allows for a good balance between robustness and performance by analyzing the plant model. Then, by interacting with sliders, the controls response time and transient behavior can be chosen. The gain values K_P and K_I of the respective controllers are shown in table 3.2.

Table 3.2: PI-regulator values for voltage and current control

Name	K_P	K_I
Voltage Control	-0.0035	-2.4900
Current Control	-0.01	-100

To choose the correct phase-shift signal to output, a Matlab® function is utilized to create a *pidSELECTOR* (appendix C.1.3). It is a simple if-else code that outputs a two when charging is selected, and otherwise a one. To correctly maneuver between the modes, a Stateflow-diagram [62] is designed (appendix C.1.4). This means that the model can only be in one state at a time, and certain conditions need to be met before entering or leaving a state.

Useful displays, a few parameter editor blocks and push-buttons are illustrated in appendix C.1.5, followed by signals and scopes used during loggingappendix C.1.6. Simulation scope is displayed in appendix C.1.7.

3.1.4 Parameters

Appendix D shows the relevant parameters for the SC (appendix D.1.1), the MOSFET (appendix D.1.2) and the transformer (appendix D.1.3). The SC block and selected parameters match the SC cell used in the integrated SC design in section 3.3.

3.1.5 Switching Frequency

As this thesis aims to utilize the SC's fast electric response, a high switching frequency is desired. The focus is on fast response and quickly neutralize a voltage drop on the DC-bus. The frequency of 250 kHz is chosen but might cause problems on the physical model from electromagnetic noise and switching losses (section 2.7). Other benefits with a high switching frequency are that the physical size of the inductor and capacitor can be reduced.

3.1.6 Sampling Time

With a switching frequency of 250 kHz on the DAB, each period is equal to 4 µs. Events in the simulation is decided to happen based on discrete-time. According to Nyquist-Shannon [63] theorem, the sampling time of the simulation must be at least twice as fast as the frequency of the system. Because the model's phase-shift ratio is adjusted with small steps between $\pm\frac{T_s}{4} = 1$ µs, it is important that the sampling is many times faster than this value. Through simulation, it is decided that the sampling rate has to be 0.01 µs, which gives the phase-shift an accuracy of 100 steps in both positive and negative direction. This is a sampling frequency of 100 MHz which will be discussed further in section 5.1.

3.1.7 Leakage Inductance

Total leakage inductance is directly linked to the amount of power transferred. It is decided that the converter will be able to deliver 1 kW continuously while the SC is discharging all the way to 90 V. This is considered in the following calculation. The required leakage inductance is calculated from eq. (2.14) and is equal 28.9 µH. Hence, the converter will have a maximum power of 2 kW when the SC is fully charged.

3.1.8 Sizing of Components

The total leakage inductance of the DAB comes from total inductance in transformer and inductor (section 2.4.4). The transformer used is a linear transformer block, and its parameters are found in appendix D.1.3. For the inductor on the DABs output, its inductance has to compensate for the missing leakage inductance from the transformer. This correct in-

ductance is therefore acquired by subtracting the transformer inductance from the leakage inductance. The inductor is calculated to be 19.5 µH. Capacitors are sized to limit the voltage ripples within 5% of nominal values. It is sized to 500 µF on the SC side and 54.3 µF on the DC-bus side.

3.2 Supercapacitor Model Matlab®/Simulink®

A model of the simulated SC module is developed in Matlab® / Simulink®utilizing the relevant SC theory from section 2.1. The SC is simulated by the block from Simscape Electrical (section 2.9.1). This simulation aims to build a better understanding of the balancing circuit (section 2.1.6) and prepare for the physical SC development. It has a discrete sampling rate of 0.01 s.

Matlab®/Simulink® diagrams relevant to this section is found in appendix C.2. A total of 12 SC blocks (appendix C.2.1) are selected to simulate each individual cell in the physical SC module. Cell number one is displayed in fig. 3.2. Each of the 12 cells has the same parameters as the physical SC cell (appendix D.2). Adjustments in capacitance is done to simulate imperfect cells and for the sake of simulations, as shown in table 3.3. Maximum variations in capacitance is listed to be +20% by Maxwell (appendix D.2), which is demonstrated with cell 12.

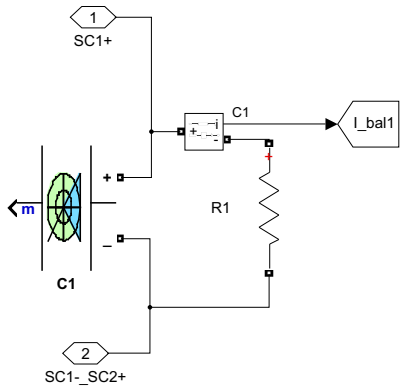


Figure 3.2: Cell one of 12 in the simulated supercapacitor model with balancing circuit

3.2.1 Measurement

Voltage measurements are included for each cell, as well as the whole pack (appendix C.2.2). Current measurements are included for each balancing circuit and total charging current.

Table 3.3: Variation in capacitance for each supercapacitor cell

Cell Number	Value
1	360 F
2	365 F
3	370 F
4	375 F
5	380 F
6	385 F
7	390 F
8	395 F
9	400 F
10	410 F
11	420 F
12	432 F

3.2.2 Supercapacitor Balancing

Balancing is simulated with a passive resistor of 360 Ω in parallel to each cell (appendix C.2.1), from the theory in section 2.1.6 with the passive method without a switch. The balancing resistor is discussed further in section 3.3.2 and matches the physical implementation of the circuit.

3.2.3 Pre-charge, Charge and Discharge Circuits

Circuits used in this section are shown in appendix C.2.3. Pre-charge limits the charging current before the total voltage reaches $V_{tot} \times 0.9$. The pre-charge resistor is set to 30 Ω, which gives a maximum charging current of 1 A for 30 V. This is a small charging current but sufficient for simulation purposes. It is necessary to reduce in-rush current, in regards to the SC's small ESR (section 2.1.1). The charging is switched to the charge circuit when the SC voltage reaches $V_{tot} \times 0.9$, equal to 27 V. The voltage drop over the resistor is fairly small, and the charging current is limited. Discharging of the SC is also realized by a 30 Ω resistor to make the charging and discharging results comparable.

3.3 Physical Supercapacitor Module Implementation

An integrated SC system is designed based on the simulated SC from section 3.2. The PCB development tool KiCAD (section 2.9.3) is utilized for the design. The goal is to construct a SC module with integrated design of 30 V to be a building block in a bigger 180 V SC system. It is essential that this is concluded before continuing the physical development of the IBDC.

When building a SC module, one important component is the actual SC cell. Companies like Maxwell, SPSCAP, LICAP, EATON, and SECH manufacture single cells and complete modules of various sizes. The chosen approach is to order single cells and assemble them at the bottom of a PCB. This way, the complete module design is described and included in appendix F). The physical prototype is shown in fig. 3.3.

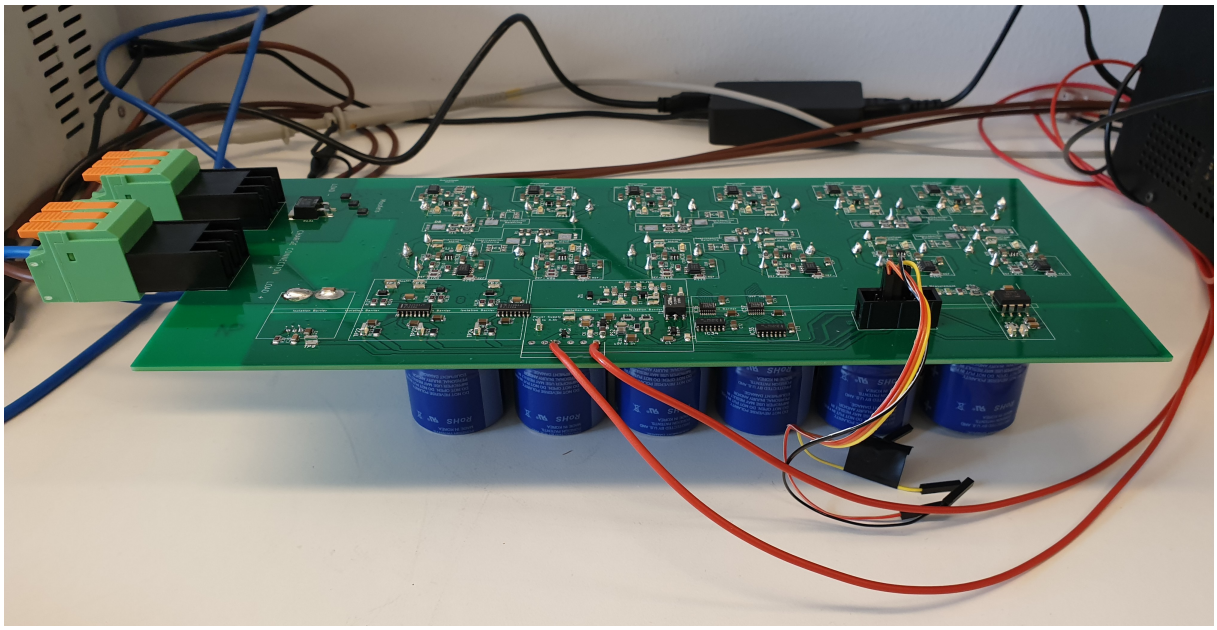


Figure 3.3: Physical Supercapacitor module

3.3.1 Supercapacitor cell

The sizing of the SC is done using the theory from section 2.1.2. The energy required by the complete SC storage (180 V) is set to 1 kW for at least 60 s. It is also going to deliver 1 kW until 50% SOC. For the module, it is used a SC cell of 360 F, 2.7 V cylindrical SC from Maxwell. With a maximum stored energy of 0.36 Wh, a module of 12 cells is sufficient to meet the requirement. Since one module of 30 V is only 1/6 of the final SC system, the module only requires 1/6 of the required energy. One 30 V module will have a theoretical maximum energy of 3.75 Wh, which makes it able to supply 225 W for 60 s. The cell is displayed in fig. 3.4 and its parameters are found in appendix D.2 together with its datasheet.

Figure 3.4: Supercapacitor cell from Maxwell (appendix D.2)

3.3.2 Cell Balancing

The chosen method for cell balancing is passive and consists of two parts. The first is a resistor placed in parallel to every SC cell. With only this type of balancing, the resistor must be large enough to bypass ten times the maximum leakage current of the SC. For a 360 F capacitor with a leakage current of 750 µA, the resistor is 360 Ω (360 Ω = 2.7 V/(10 × 750 µA) for each cell.

The second part is a balancing Integrated Circuit (IC) which will bypass more current as the voltage increases [64]. This component will bypass 3 mA at 2.2 V and 10 mA at 2.7 V. Optimally, the IC would bypass less current, but due to low stock of the component a replacement had to be made. The IC contributes to a lower power loss overall. The passive resistor, in combination with the IC, can therefore carry less of the balancing current. It is sufficient that the resistor carry 3.375 mA at 2.7 V and is sized to 800 Ω for each SC cell instead of the 360 Ω.

3.3.3 PCB Layout and Design

The PCB consists of a four copper layer design. The whole schematic for the development is shown in appendix F.1. In appendix F.2 the PCB layout is displayed without any of the copper layers. This is to visualize the placement of each SMD. The top (appendix F.3) and bottom (appendix F.6) copper layer are mainly used for copper tracks connecting the components. The middle top (appendix F.4) and middle bottom (appendix F.3) layers are used for ground and supply voltages. The SC cells are mounted on the bottom of the PCB and used as a base for the whole module. Most of the SMDs are located on top of the PCB.

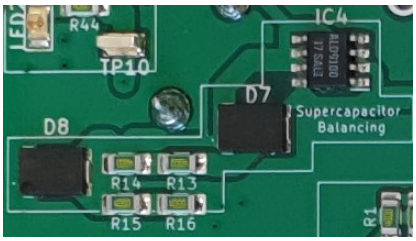


Figure 3.5: Supercapacitor balancing on the printed circuit board

A large part of the components used on the PCB are in the SC balancing. Each circuit balances two cells, hence, a total of six circuits are required (appendix F.1 p:2-7). One circuit is displayed in fig. 3.5.

Another large part of the components are used in the modules Over-Voltage Protection (OVP) circuits. It is based on a voltage detection IC which output a signal when the voltage over each cell reaches 2.7 V. A differential amplifier IC is utilized to measure the voltage across each cell correctly. A total of 12 circuits are needed for the module (appendix F.1 p:11-23). One circuit is shown in fig. 3.6.

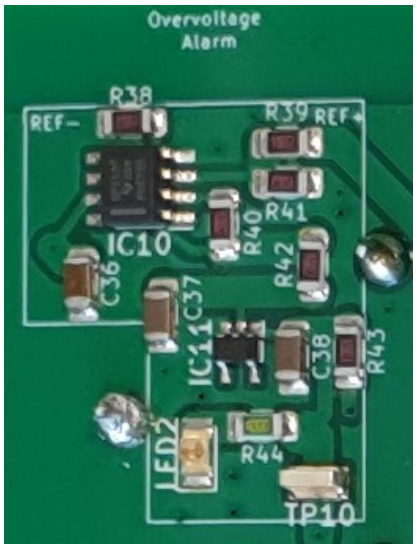


Figure 3.6: Over-voltage protection circuit for the Supercapacitor on the printed circuit board

This IC does not contain electrical isolation. Therefore, an isolation IC is needed before the signals are gathered in a logic OR-gate with Schmitt trigger. The circuits is displayed in fig. 3.7.

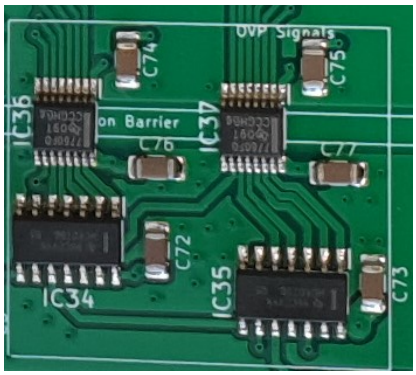
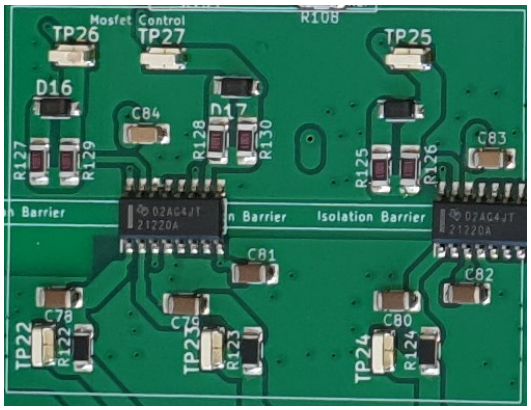


Figure 3.7: Isolation component for the over-voltage protection signals and OR-gate

The module's main power is connected to two power MOSFETs to act as power switches: One for pre-charge, one for charge, and a third to control the load connection. This is only necessary for discharging results for testing, since charge and discharge will be on the same connection when integrated with the DAB. The MOSFETs are displayed in fig. 3.8a. The MOSFETs are controlled with gate-drivers connected to the MCU, displayed in fig. 3.8b.

(a) MOSFETs which control the charging, discharging, and load of the supercapacitor



(b) MOSFET drivers which give correct output to the gates

Figure 3.8: MOSFETs and MOSFET drivers on the printed circuit board

Several voltage levels are created from an external 15 V supply. An isolation barrier ensures electrical isolation for the supplies. Two supplies of 5 V and 3.3 V are created from the 15 V. The 5 V is used to create an isolated supply of 6 V to supply the gate-drivers, which is then bucked to a 5 V isolated supply. The un-isolated supplies are separated from the isolated through the isolation barrier. The circuitry is displayed in fig. 3.9.

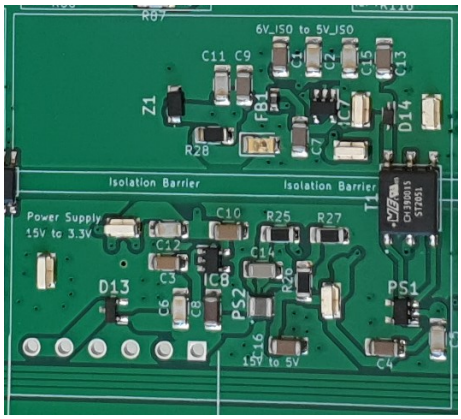


Figure 3.9: Voltage levels created on the printed circuit board

Pictures of the design from Kicad's 3D-view are found in appendix F.7. The top of the PCB is on the left and the bottom on the right. The system specifications for the module are displayed in table 3.4.

Table 3.4: Integrated supercapacitor module specifications

Type	**Value**
Cells in series	12
Capacitance	30 F
Nominal Voltage	30 V
Maximum Current	20 A
Maximum Power	600 W
DC ESR	38.4 mΩ
Maximum Stored Energy	3.75 Wh
Usable Specific Power	3282.56 W/kg
Total SC Weight	0.8568 kg

3.3.4 Construction

The SMD components are soldered to the PCB by utilizing a stencil. Solder paste is applied on top of the stencil while it rests on top of the board. This allows correct placement of the solder paste, and the components are placed in their marked positions. When all components are properly placed, the board is heated in an industrial oven.

3.3.5 Equipment

During testing of the SC module, the equipment in table 3.5 are utilized. The equipment are displayed in fig. 3.10. An oscilloscope from Keysight is used for current and voltage sensing to achieve more detailed result plots than with the designed current and voltage measurement. The current and voltage probe utilized with the oscilloscope are not included in fig. 3.10. Both probes are calibrated pre-testing and have an accuracy of 3% and 2%, respectively. A multimeter from Hioki is utilized to measure the cell voltage to ensure each balancing circuit is working properly. The power supply from Elektro-Automatik is used for the charging of the SC. The Mascot power supply ensures a stable 15 V for the entire PCB. During discharging of the SC, the programmable DC-load from Elektro-Automatik is used. The Delfino microcontroller is displayed in fig. 3.10.

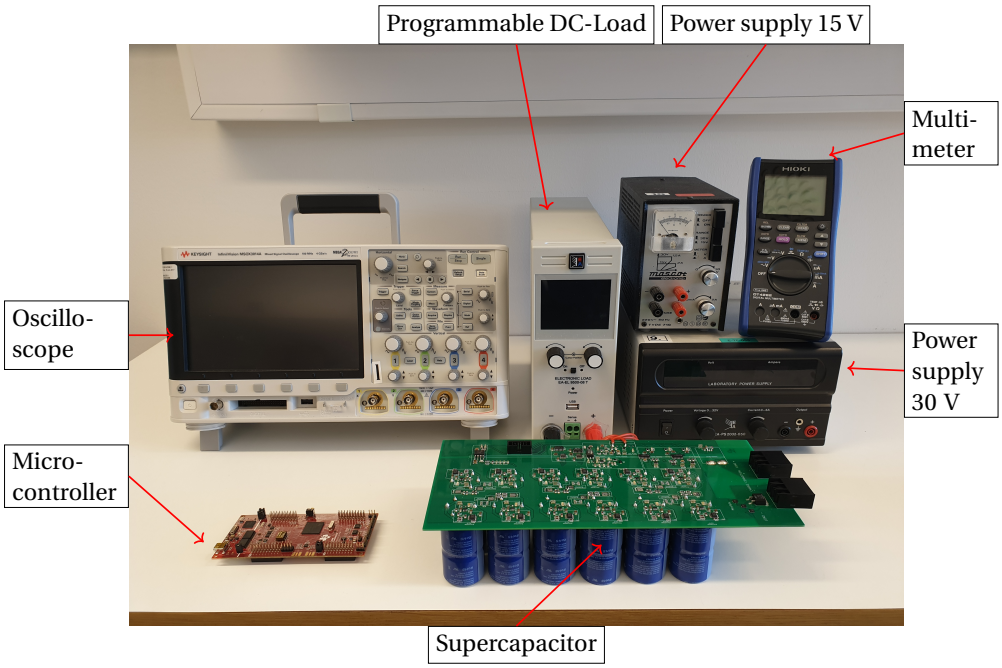


Figure 3.10: Laboratory test equipment

Table 3.5: Laboratory test equipment

Type	**Manufacturer**	**Type**
Programmable Load	Elektro-Automatik	9500-08 T
Oscilloscope	Keysight	MSOX3014A
Diff. Probe	Micsig	DP10013
Current Probe	Micsig	CP2100A
Multimeter	Hioki	DT4282
Power Supply	Elektro-Automatik	EA-PS 2032-050
Power Supply	Mascot	719
Supercapacitor	Maxwell Technologies	BCAP0360 P270 S18
Delfino Launchpad	Texas Instrument	TMS320F28379D

3.3.6 Current and Voltage Sensing

Current sensing on the PCB is realized with a *hall-effect current sensor*. This device utilize the magnetic field created to detect either current or voltage in a circuit. The component ensures safe sensing of large currents since the output is electrically isolated from the input.

A *voltage operational amplifier* is a device that amplifies a signal. It is designed to measures the SC module voltage by utilizing its inverting and non-inverting inputs. This is realized with a differential voltage op-amp which outputs the voltage differential of two input pins.

3.3.7 TMS320F28379D LaunchPad

This Delfino LaunchPad is used to handle digital and analog signals from the SC module. There are four digital signals needed on the board: Three control signals for the power MOSFETs, and one for the OVP alarm signal. A Matlab® /Simulink® diagram is utilized to communicate with the MCU, displayed in appendix C.3. Analog signals are used to receive voltage and current measurements. Details about the Launchpad is found in section 2.4.5.

4 Results

This chapter presents the results from the simulated and physical models presented in this thesis. It starts with the simulated DAB in section 4.1, followed by the simulated SC model (section 4.2) and the integrated SC design (section 4.3). This is achieved by first presenting the DAB's functionality, integrated with the simulated SC, before going into the details regarding the physical SC prototype. The results are later discussed in the discussion chapter and follow the findings chronologically.

4.1 DC-DC Converter Model in Matlab®/Simulink®

Simulations of the DAB IBDC is carried out in Matlab®/Simulink®. Methods used in this section for development of the model is explained in section 3.1. Circuits related to the model is found in appendix C.1.

Firstly, the charge characteristics for the SC block with 72 cells in series used together with the DAB, is shown in fig. 4.1. This provides a good indication of the SC's capacity. The parameters for this block is shown in appendix D.

Secondly, during operation, the SC voltage will start to decrease from the loss of charge, resulting in lower a power output. The phase-shift will increase as the voltage decrease to maintain the same level of power transfer. This is illustrated in fig. 4.2. The curves are plotted utilizing eq. (2.13). The phase-shift is given in radians, where $\pm\pi/2$ rad indicates the maximum power in positive or negative direction. Source code for fig. 4.2 is shown in E.2.1.

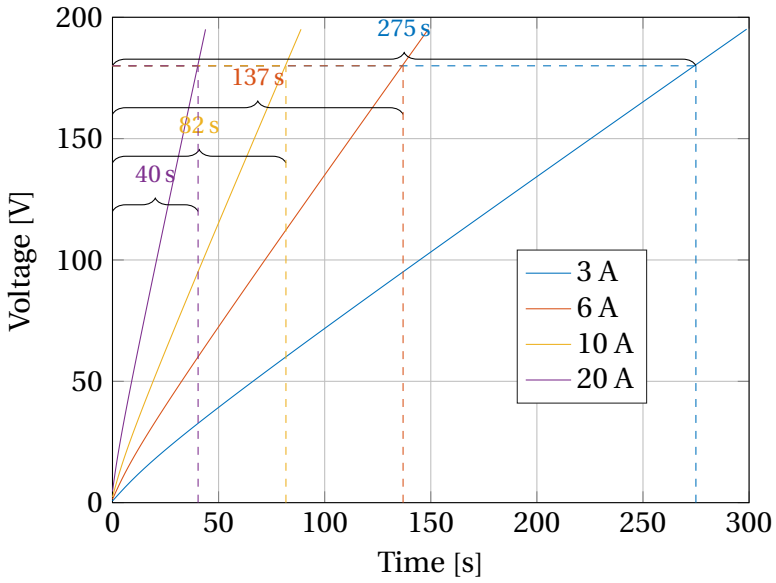


Figure 4.1: Charge characteristic of the simulated supercapacitor used with the dual active bridge

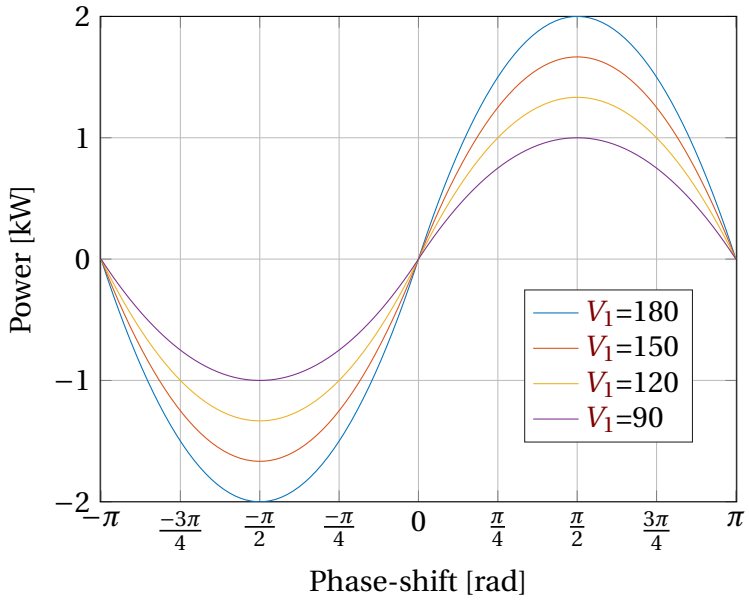
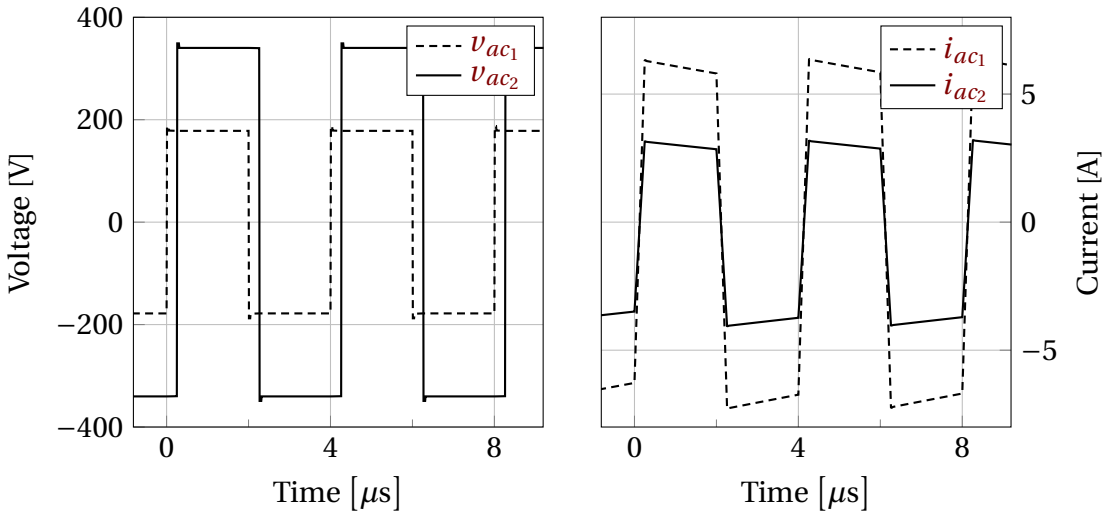


Figure 4.2: Theoretical output power of the dual active bridge as a function of phase-shift. Plotted for different supercapacitor voltage

4.1.1 Primary and Secondary AC Components

Simulations start by showing the primary and secondary AC components (voltage and current) of the DAB. This is measured on the input and output of the transformer. The following scenario utilize a fully charged SC bank delivering 1000 W to the load. The converter has settled in steady-state and display two full periods (8 µs).



(a) AC voltages

(b) AC currents

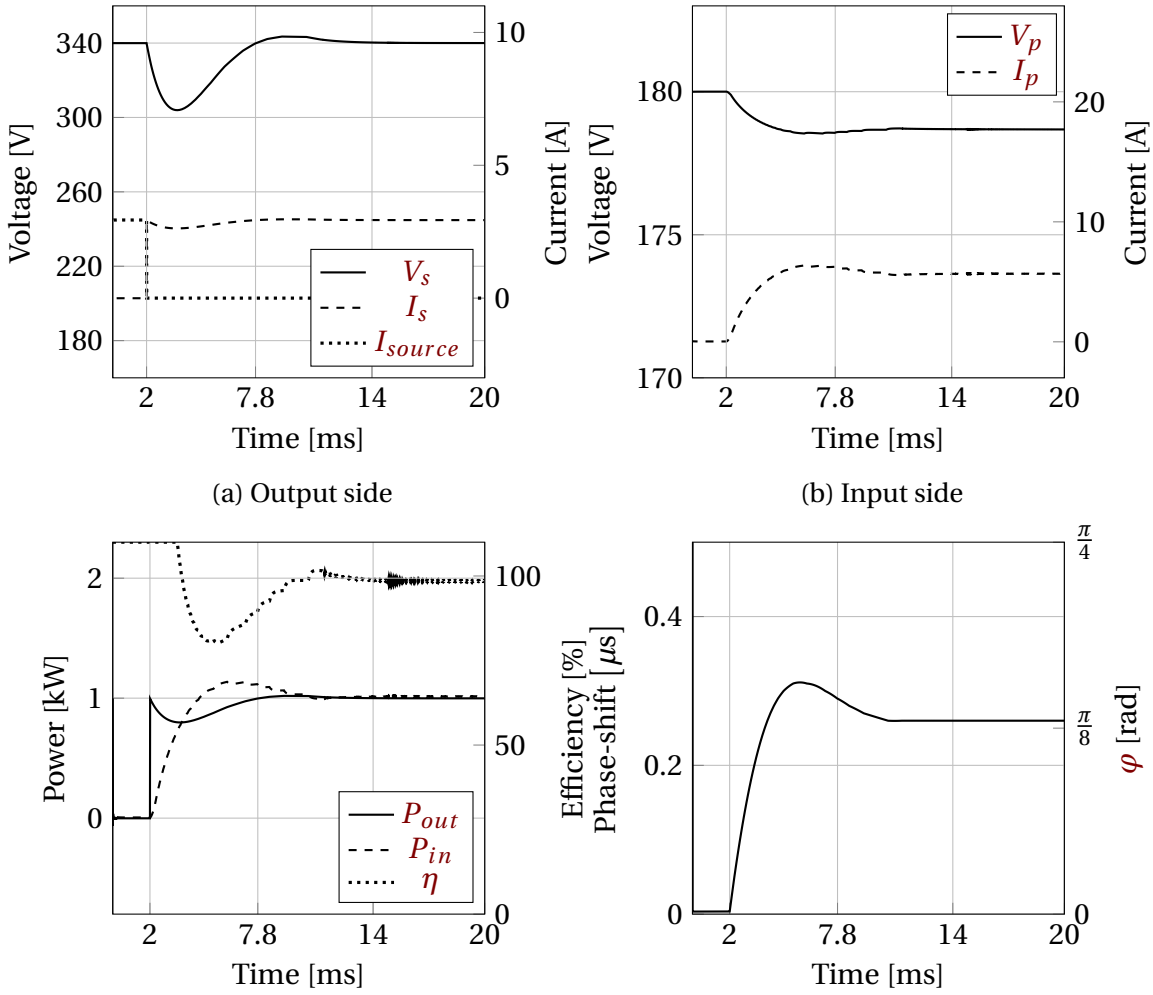
Figure 4.3: Primary and secondary AC components (voltage and current). The plot in (a) shows the primary and secondary voltages varying between ±180 V and ±340 V. The plot in (b) shows the primary and secondary currents, varying between ±6.2 A and ±3 A. The currents stretch a bit further on the negative than the positive

4.1.2 Supercapacitor SoC Scenarios with Stabilization Mode

The SC is able to supply the DC-bus while it contains between 100% to 50% SOC. Below 50% the primary AC current becomes too large and efficiency too low. The tests are divided into four, where the SC is charged to the different voltage levels: 180 V, 150 V, 120 V, 90 V. All scenarios start with the DC-bus supported by an external source. This source is disconnected at time 2 ms, making the voltage drop. The current supplying the DC-bus is also included in the plot. The source current drops to zero when the source is removed. The converter responds by supplying the load, maintaining the DC-bus voltage. The efficiency (η) of the converter is calculated by dividing the input power, P_{in}, by the output power, P_{out}. Each scenario is displayed by four smaller plots to display the results.

Stabilization with 180V SC

The first stabilization scenario display the fully charged SC responding to the dropping DC-bus at time 2 ms. At 7.8 ms, the voltage drop is neutralized and reach the stable voltage at time 14 ms. The simulation results are shown in fig. 4.4.



(a) Output side

(b) Input side

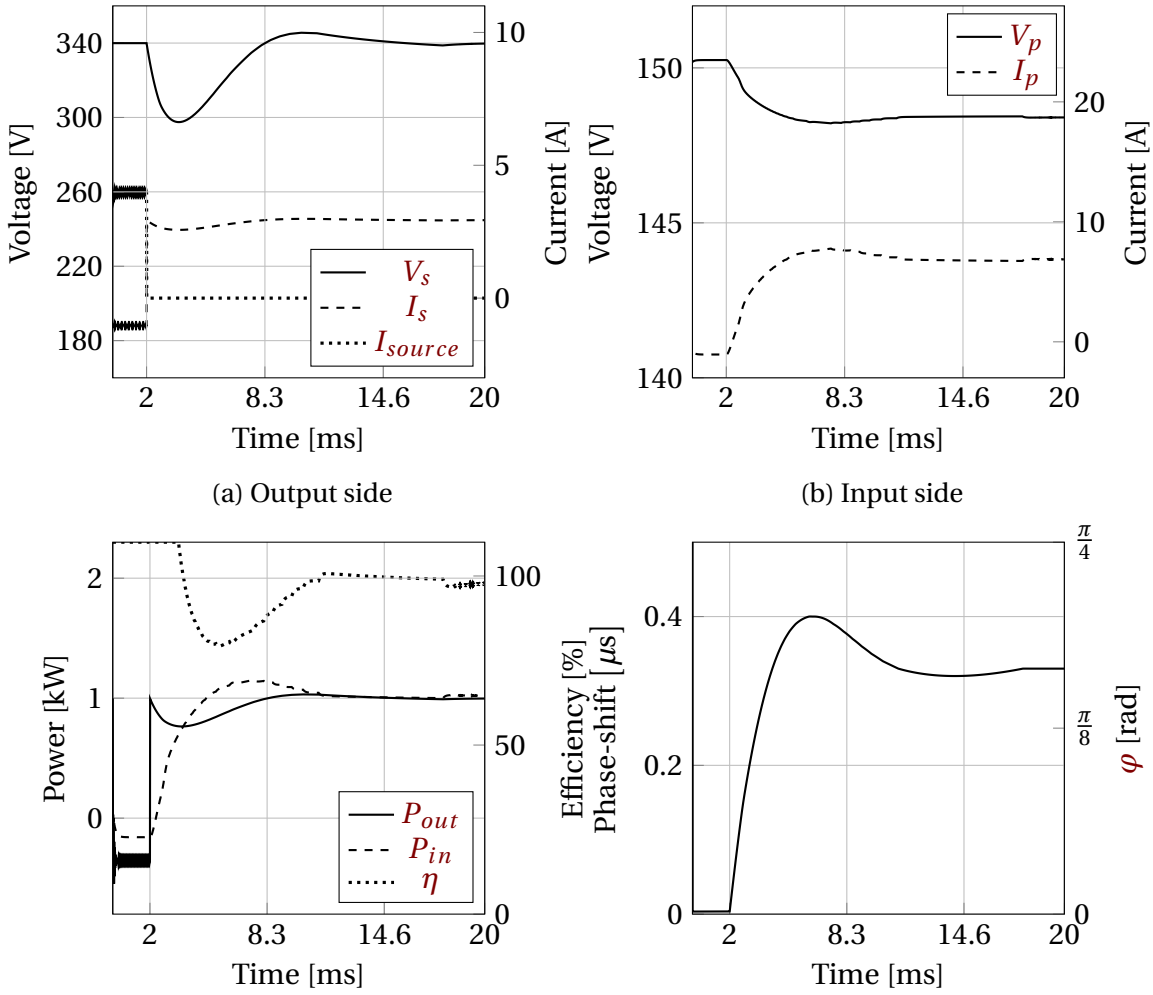
(c) Input and output Power

(d) Required phase-shift

Figure 4.4: The first plot, (a), naturally displays the DC-bus voltage at 340 V and dropping to about 305V before reaching 340 V again after 7.8 ms. A slight overshoot is shown and adjusted after 14.0 ms. The primary/SC current and voltage is displayed in (b). As a response to the DC-bus, the SC voltage drops and the current increases. The power calculated from (a) and (b) is monitored, and the converter's efficiency is calculated and displayed in (c). Efficiency is not completely displayed before 4 ms. Lastly, the required phase-shift for this scenario is displayed in (d)

Stabilization with 150V SC

In the second stabilization scenario, the SC is charged to 150 V, responding to the dropping DC-bus at time 2 ms. At 8.3 ms the voltage drop is neutralized and reaches a stable voltage at time 14.6 ms. The simulation results are shown in fig. 4.5.



(a) Output side

(b) Input side

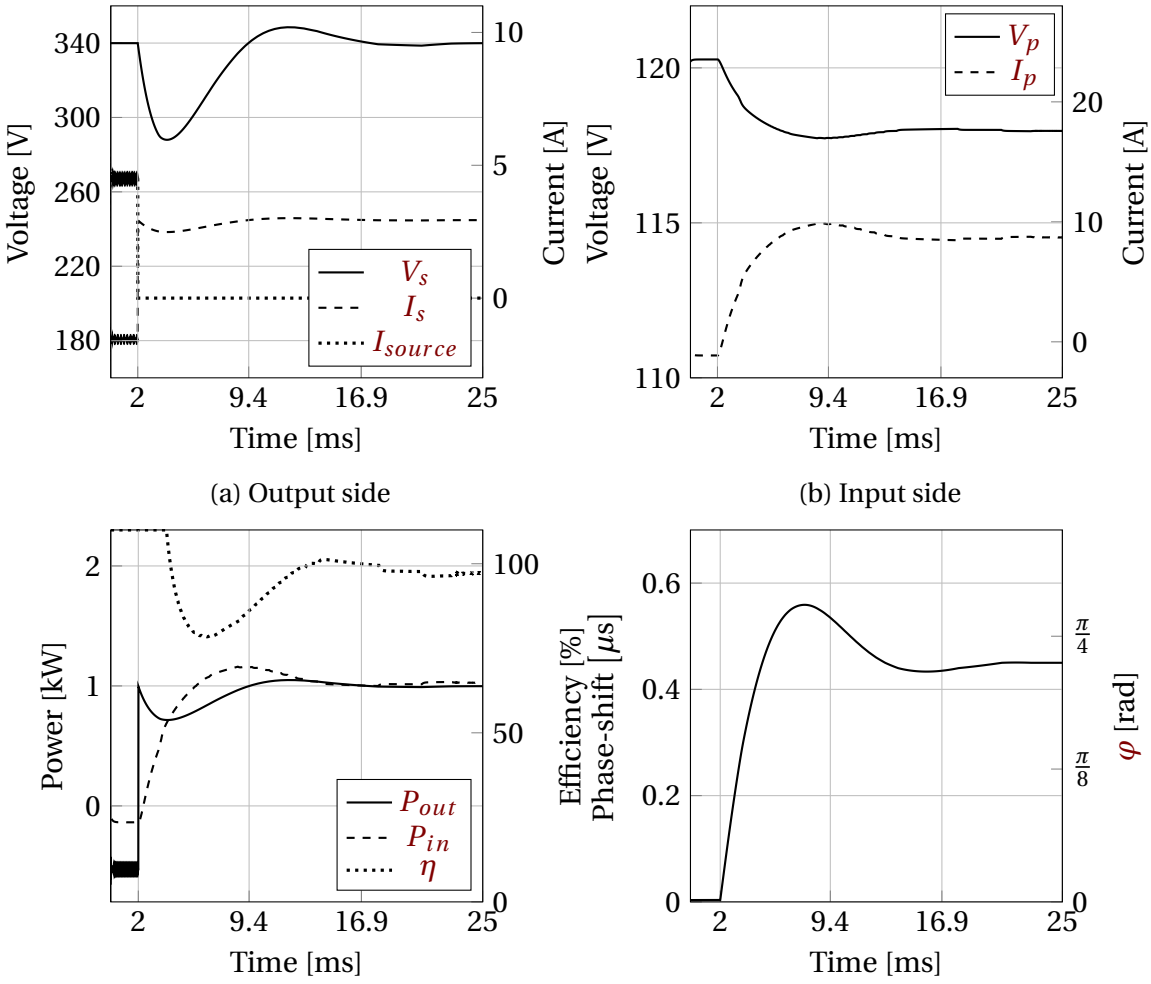
(c) Input and output power

(d) Required phase-shift

Figure 4.5: The first plot, (a), naturally displays the DC-bus voltage at 340 V and dropping to just below 300 V before reaching 340 V again after 8.3 ms. A slight overshoot is shown and adjusted after 14.6 ms. The primary/SC current and voltage is displayed in (b). As a response to the DC-bus, the SC voltage drops and the current increases. The power calculated from (a) and (b) is monitored, and the converter's efficiency is calculated and displayed in (c). Efficiency is not fully displayed before 4 ms. A negative current and power is displayed before the trigger. Lastly, the required phase-shift for this scenario is given in (d)

Stabilization with 120V SC

In the third stabilization scenario, the SC is charged to 120 V, responding to the dropping DC-bus at time 2 ms. At 9.4 ms, the voltage drop is neutralized and reaches a stable voltage at time 16.9 ms. The simulation results are shown in fig. 4.6.



(a) Output side

(b) Input side

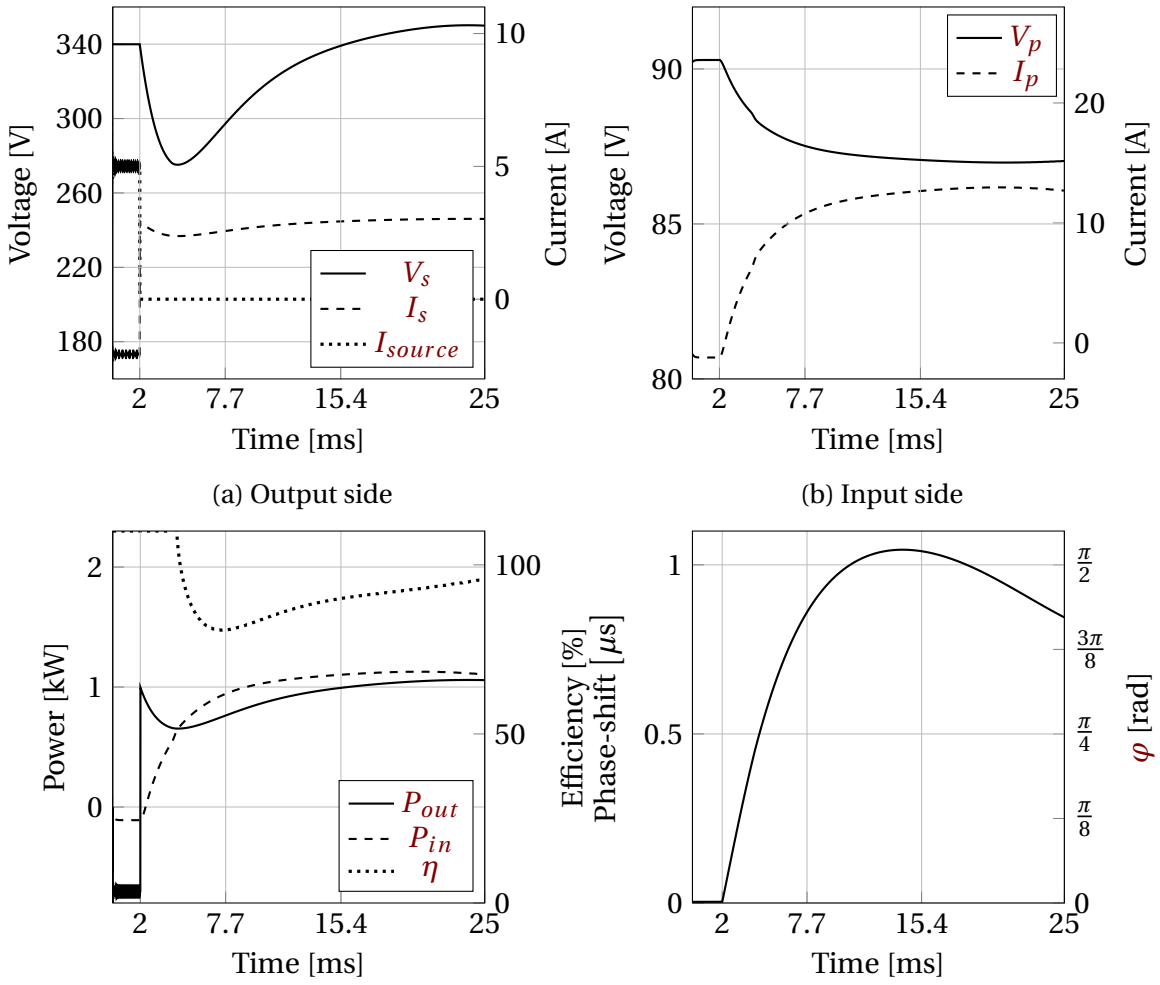
(c) Input and output power

(d) Required phase-shift

Figure 4.6: The first plot, (a), naturally displays the DC-bus voltage at 340 V and dropping to about 288 V before reaching 340 V again after 9.4 ms. An overshoot of 8 V is shown and adjusted after 16.9 ms. The primary/SC current and voltage is displayed in (b). As a response to the DC-bus, the SC voltage drops and the current increases. The power calculated from (a) and (b) is monitored, and the converter's efficiency is calculated and displayed in (c). Efficiency is not fully displayed before 4 ms. A negative current and power is displayed before the trigger. Lastly, the required phase-shift for this scenario is given in (d)

Stabilization with 90V SC

In the fourth stabilization scenario, the SC is charged to 90 V, responding to the dropping DC-bus at time 2 ms. At 15.4 ms, the voltage drop is neutralized. The simulation time of 25 ms is not enough time for the converter to stabilize the voltage. The simulation results are shown in fig. 4.6.



(a) Output side

(b) Input side

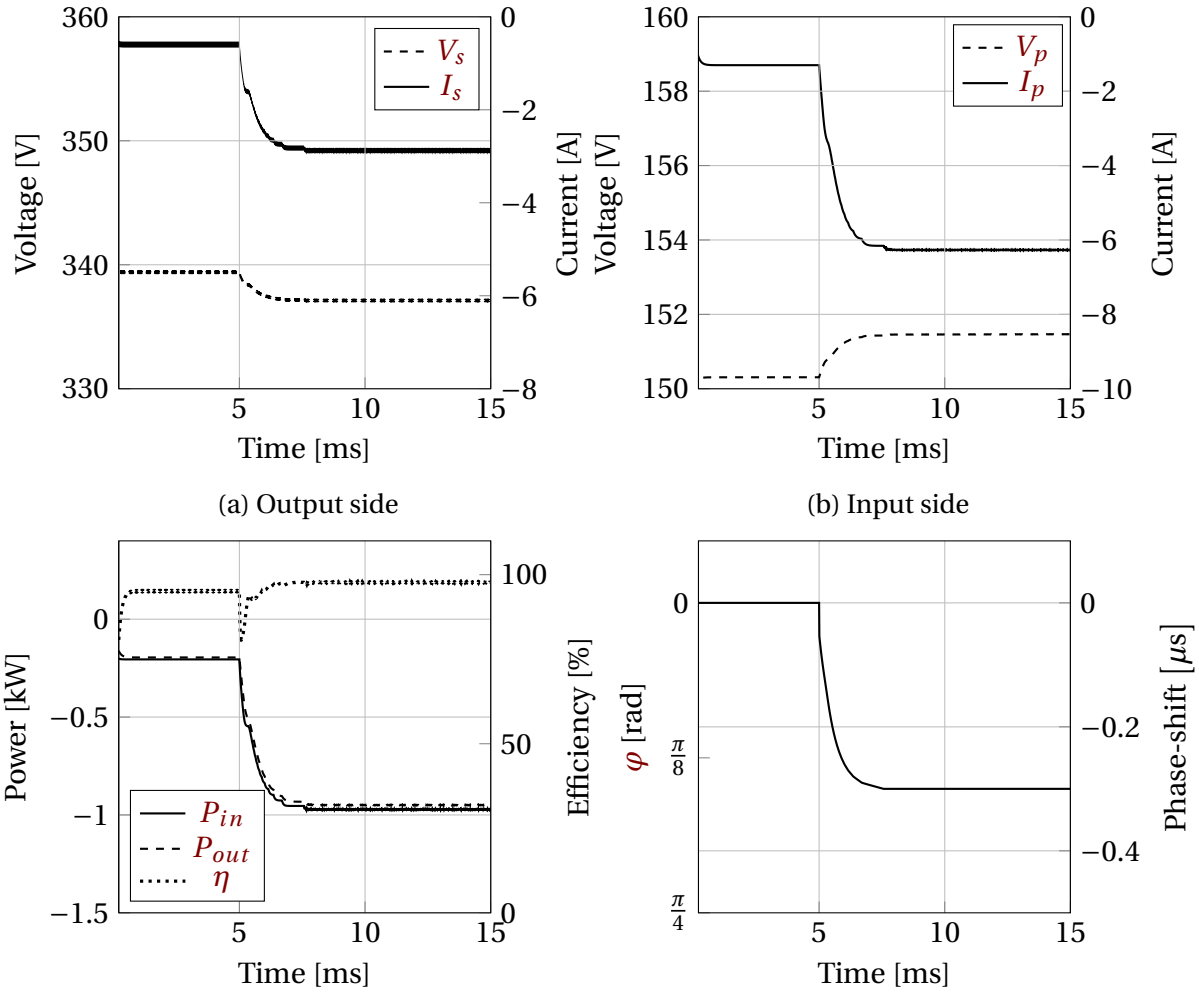
(c) Input and output power

(d) Required phase-shift

Figure 4.7: The first plot, (a), naturally displays the DC-bus voltage at 340 V and dropping to about 278 V before reaching 340 V again after 15.4 ms. An overshoot of 10 V is shown and starts to decrease. The primary/SC current and voltage is displayed in (b). As a response to the DC-bus, the SC voltage drops and the current increases. The power calculated from (a) and (b) is monitored, and the converter's efficiency is calculated and displayed in (c). Efficiency is not displayed before 4 ms. A negative current and power is displayed before the trigger. Lastly, the required phase-shift for this scenario is given in (d)

4.1.3 Supercapacitor charging scenario

The SC's charging mode is covered in this scenario. It aims to showcase the modes functionality during a charging scenario after a stabilization scenario. The SC is charged to 150 V, which is a typical voltage when the SC can charge, when the command for charging is initiated time 5 ms. At 8.3 ms, the voltage drop is neutralized and reaches a stable voltage at time 14.6 ms. The simulation results are found in fig. 4.5.



(a) Output side

(b) Input side

(c) Input and output power

(d) Required phase-shift

Figure 4.8: The first plot, (a), naturally displays the DC-bus voltage at 340 V. At time 5 ms, a small voltage drop is exerted as the charge is initiated. The secondary charging current is about −3 A. The primary/SC current and voltage is displayed in (b). The power calculated from (a) and (b) is monitored, and the converter's efficiency is calculated and displayed in (c). Efficiency is not fully displayed before 4 ms. Lastly, the required phase-shift for this scenario is given in (d)

4.2 Supercapacitor Model Matlab®/Simulink®

This model is developed using Matlab® /Simulink®. Methods used in this section to develop and test the model are explained in section 3.2. The purpose of the following results is first to understand the charging (section 4.2.1) and discharging (section 4.2.2) characteristics of the SC module before developing the integrated SC design. Second, it is desirable to investigate the importance of a balancing circuit during charging and discharging when multiple cells' capacitance in series differs between the manufacturer's minimum and maximum values. In section 4.2.3, the simulated SC is connected to different loads to show its transient response.

4.2.1 Charging from 0-30V

Charging the discharged SC through a pre-charge resistor of 30 Ω before switching to the charging circuit at time 2156 s. All plots share the same time axis and are simulated over 3000 s. The charge current is chosen to start at 1 A.

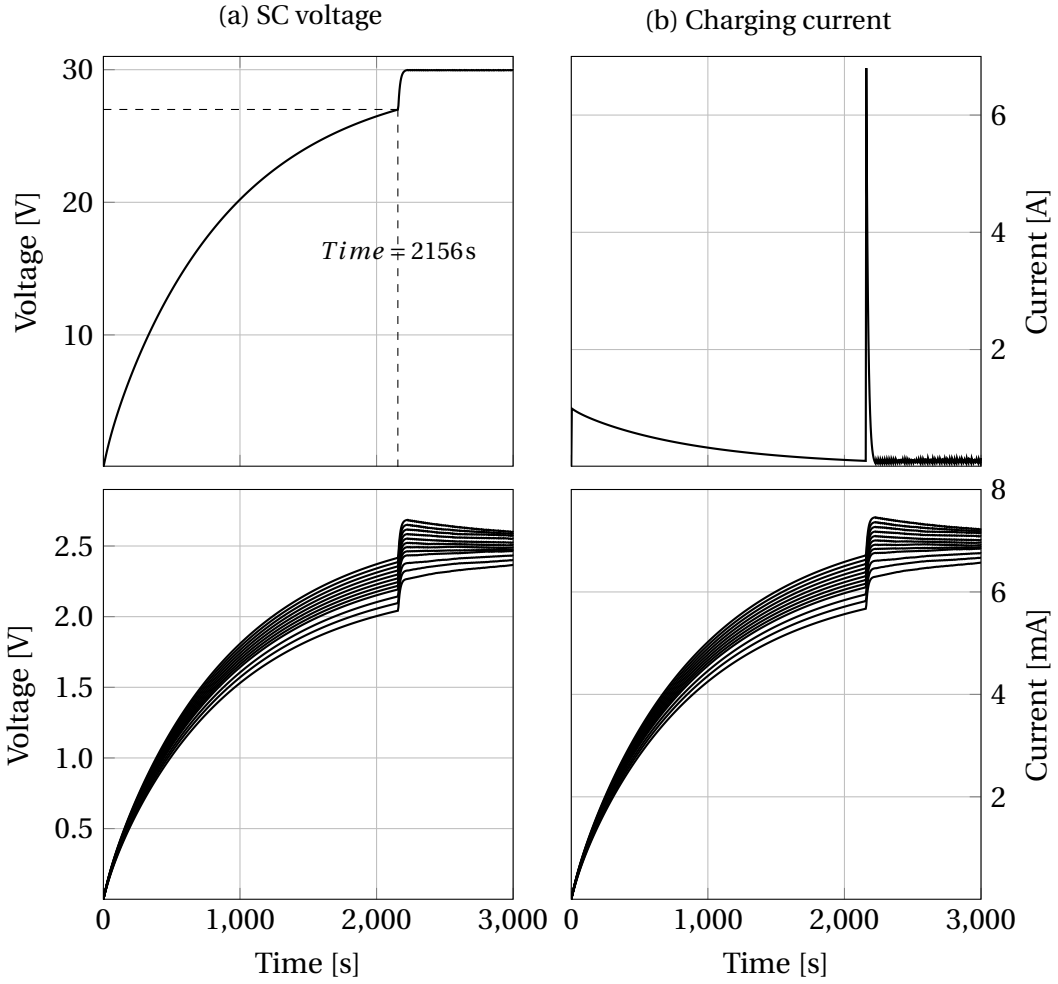


Figure 4.9: Charging the supercapacitor module from 0 to 30V. (a) and (b) show the modules voltage and charging current. The charging current is defined as positive and starts at 1 A. (c) shows the individual voltage of cell $1-12$, which are all discharged at time zero. When the pre-charge is disconnected at time 2156 s the respective cell voltages are between 2 V and 2.5 V. The charge circuit then ensures the balancing of the cells, causing them to become more evenly charged. (d) displays the current through each respective balancing circuit. With the designed balancing resistance of 360 Ω, the balancing current starts at zero and ends up at about 7 mA as the cell voltage increases. Every figure is simulated over 3000 seconds

4.2.2 Discharging from 30-0V

Discharging the fully charged SC through a 30 Ω resistor. All cells are completely discharged after 2776 s, while the cell with the lowest capacitance (cell 1 in table 3.3) is already discharged after 2056 s.

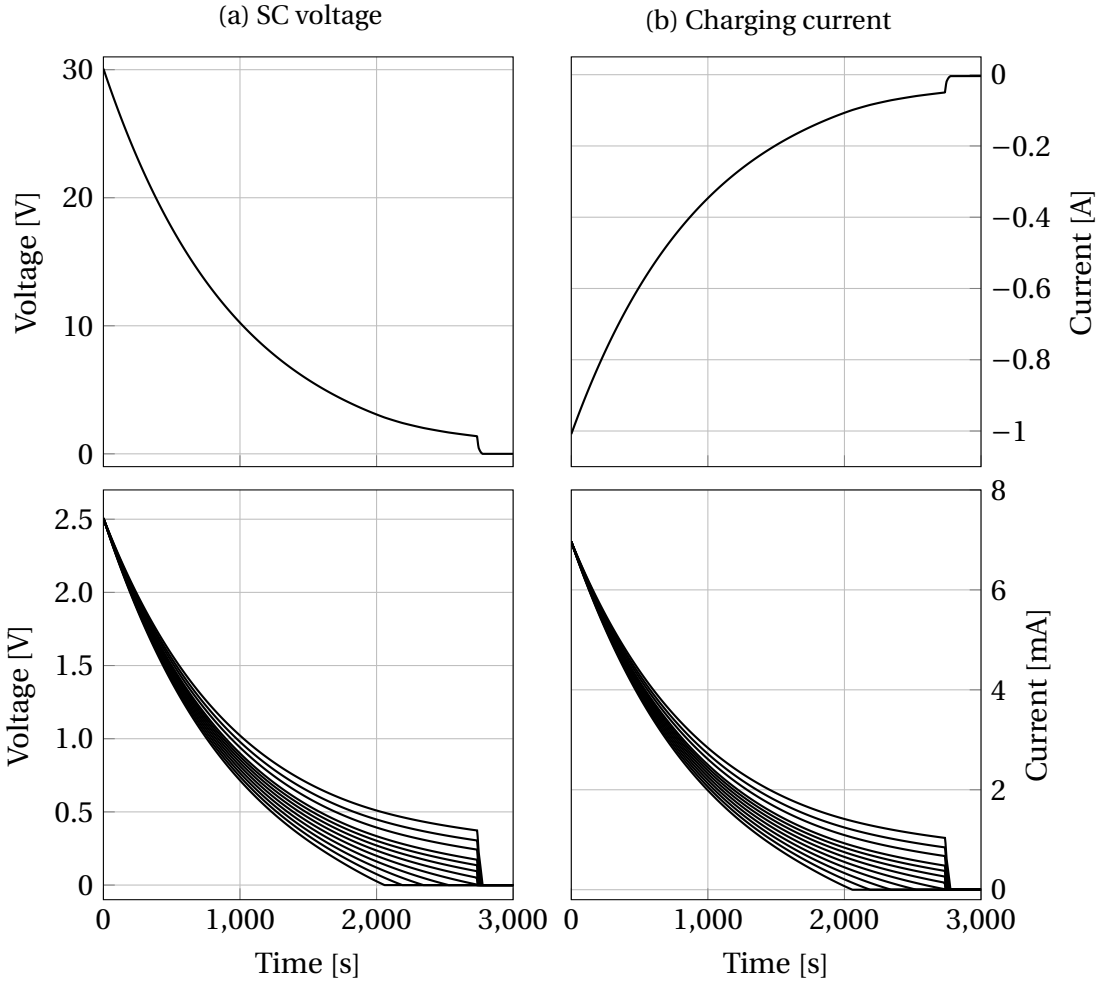
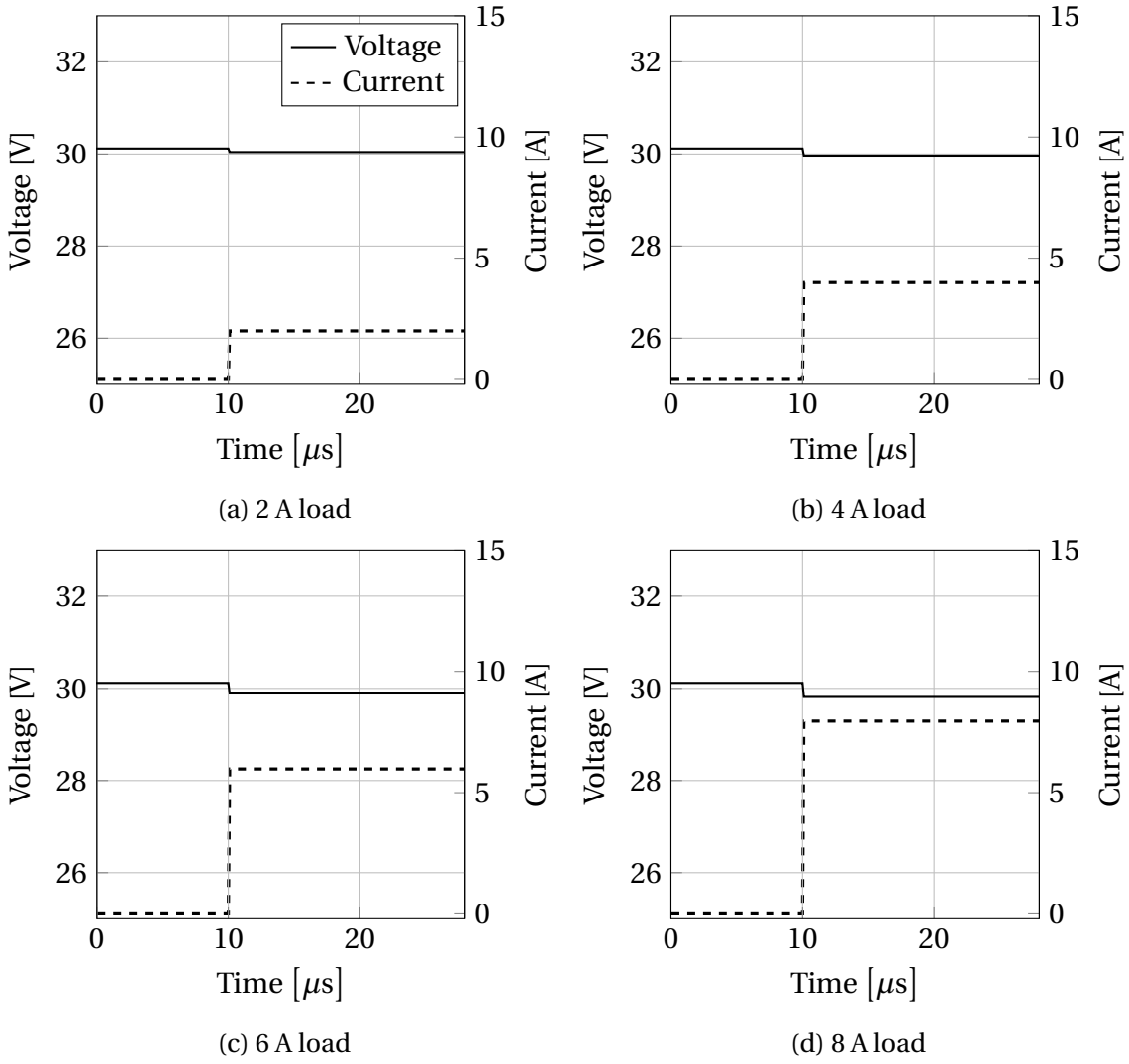


Figure 4.10: Discharging the fully charged SC through a 30Ω resistor. (a) and (b) show the modules decreasing voltage and discharge current. The discharging current is defined as negative and starts at −1 A. (c) shows the individual voltage of cell 1 − 12, which are all charged with 2.5 V. The cells discharge un-even and the first cell is completely discharged after 2056 s and the last after 2776 s. (d) displays the current through each respective balancing circuit. With the designed balancing resistance of 360 Ω the balancing current starts at about 7 mA and decreases as the cell voltage decreases. Each plot is simulated over 3000 s

4.2.3 Transient response to a load

The SC block utilized in this result is the same block used in the DAB simulations (section 4.1). It is desirable to test the SC block's transient response to a resistive load without the IBDC. This result is later compared to the integrated SC design results in section 4.3.1. There (sections 5.3.3 and 5.3.4), an analysis on how the DAB is affected by a physical SC module is carried out. The following plot has a trigger at time zero. Both the voltage and current transients are practically instant.



(a) 2 A load

(b) 4 A load

(c) 6 A load

(d) 8 A load

Figure 4.11: Voltage and current of the SC responding to different loads. All plots have a trigger at time 10 µs. The first plot, (a), shows the fully charged SC's response to a 2 A load. The current and voltage transient response is instant. The transient voltage drop is about 77 mV when the load is connected. The second plot, (b), shows 4 A load. The transient voltage drop is about 153 mV when the load is connected. The third plot, (c), shows 6 A load. The transient voltage drop is about 230 mV when the load is connected. The last plot, (d), shows 8 A load. The transient voltage drop is about 307 mV when the load is connected. All four plots share the same legend displayed in (a)

4.3 Physical Supercapacitor Module Implementation

Results regarding the integrated SC design are presented in this section. Methods used to develop and test the module are explained in section 3.3. Testing of the module is carried out with the programmable DC-load listed in table 3.5. Both the voltage and current transients in fig. 4.12 have a trigger at time zero and show the current and voltage responses over a time period of 28 µs. The rise time (T_R) for each respective plot is represented.

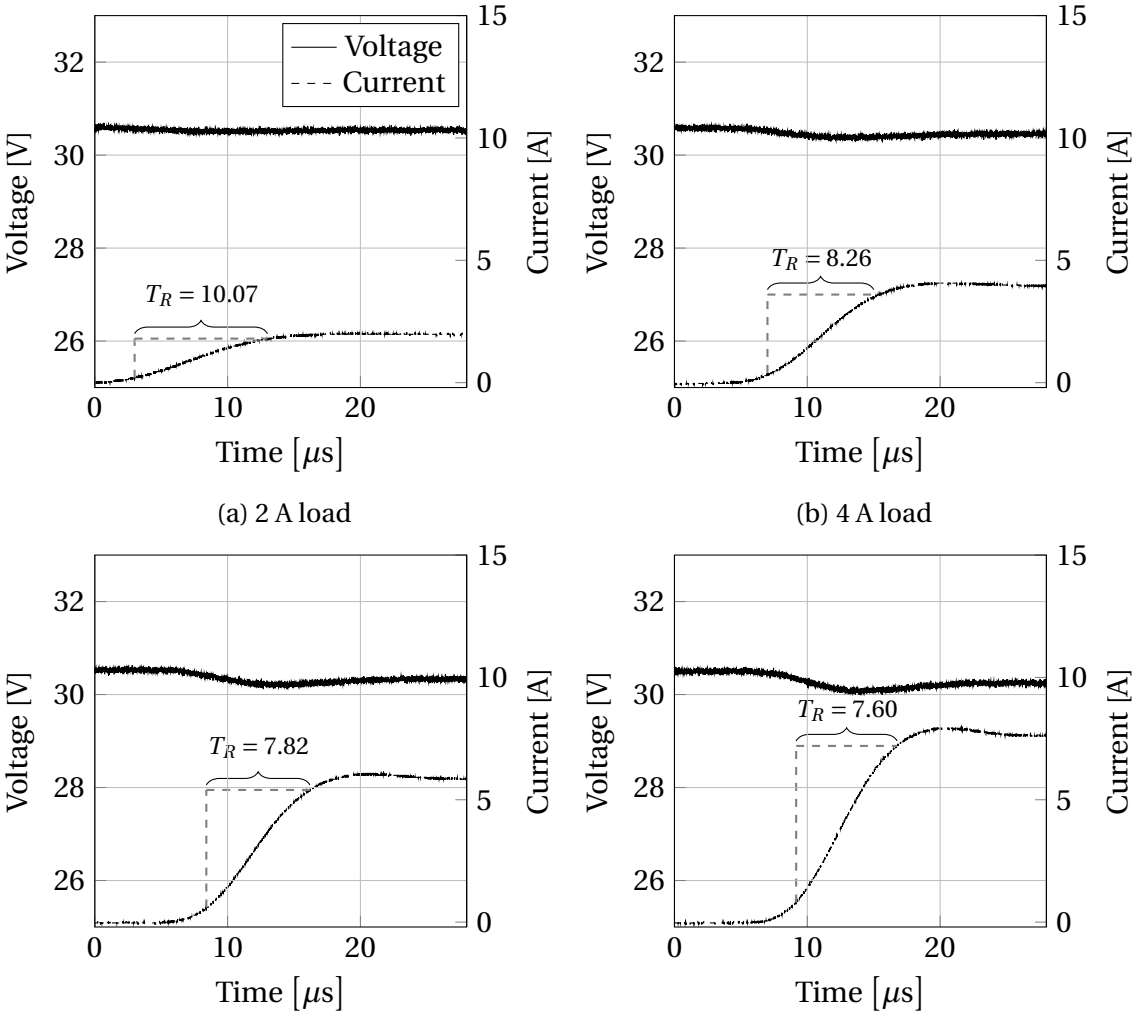
The rise times of the SC load currents are displayed in table 4.1. It is acquired when the response rises between 10% to 90% of the steady-state value. It is noted that this is not the time it takes the SC to rise from the load is initially connected. That would be from time zero. The settling time (T_S) is the time it takes the response to reach a value within 2% of the steady-state value. The overshoot (OS) represents a maximum percentage the response touches compared to the steady-state value.

Table 4.1: Plot info for the supercapacitor current's transient response in fig. 4.12

Type	**2 A**	**4 A**	**6 A**	**8 A**
T_R (µs)	10.086	8.2610	7.8208	7.6040
T_S (µs)	52.172	14.547	33.007	24.746
OS (%)	4.0666	4.0535	1.3407	0.7588

4.3.1 Transient response to a load

The result in fig. 4.12 display the physical SC's transient response when connected to a programmable DC-load. The load is programmed to trigger a set of four load currents: 2 A, 4 A, 6 A, and 8 A. All plots are made comparable to the simulation results in fig. 4.11.



(a) 2 A load

(b) 4 A load

(c) 6 A load

(d) 8 A load

Figure 4.12: Voltage and current of the SC responding to different loads. The first plot, (a), shows the fully charged SC's response to a 2 A load. The voltage drop is about 0.1 V, gradually decreasing over 10 µs as the current increases. The second plot, (b), shows 4 A load. The voltage transient indicate a voltage-drop of about 0.2 V. The third plot, (c), shows 6 A load. The voltage transient indicate a voltage-drop of about 0.3 V. The last plot, (d), shows 8 A load, with a final voltage-drop of about 0.4 V. All four plots share the same legend displayed in (a)

5 Discussion

The chapter is divided into three main sections and follow the findings from chapter 4. Firstly, results regarding the DAB simulation in section 4.1, is discussed. The purpose is to analyze the working principle of the DAB and show its functionality when integrated with the SC. The SC's charging characteristic is also investigated further. Secondly, the simulated SC results (section 4.2) is explained to achieve a deeper understanding of the module as a whole. Lastly, a comparison of the integrated SC design (section 4.3) and the simulated SC module (section 4.2) is carried out, and its different transient responses are analyzed.

5.1 DC-DC Converter Model in Matlab®/Simulink®

This section discuss the most important aspects of the results in section 4.1. The discrete sampling time of this simulation is decided to be 0.01 µs. With a switching frequency of 250 kHz, only 100 MHz sampling is sufficient to achieve the correct efficiency of the converter. This sampling rate may prove too high for a physical implementation and need to be considered in future work.

5.1.1 Charging Characteristic of the Supercapacitor

The charging mode of the DAB has a current reference of 6.25 A. From the charging characteristic (fig. 4.1) of the SC used with the DAB, the charging time can be calculated. The charging times are also displayed in fig. 4.1. For the 6 A charging current the charging time is approximately 137 second. This gives a voltage increase of 180 V/137 s = 1.3139 V/s. A good estimate of the 6.25 A can be made by

$$\frac{V_1}{T_{C_1}\, I_1} = \frac{V_2}{T_{C_2}\, I_2}, \tag{5.1}$$

where $V_1 = V_2 = 180\,\text{V}$, the charging time $T_{C_1} = 137\,\text{s}$, $I_1 = 6\,\text{A}$ and $I_2 = 6.25\,\text{A}$. By solving for T_{C_2} gives a charging time of 131.5 s with a constant current of 6.25 A. The actual charging time will be slightly slower, since the voltage increase per second will be somewhat larger.

5.1.2 Theoretical Power Transfer of the Dual Active Bridge

Figure 4.2 displays the output power as a function of phase-shift. The graph is plotted for different levels of SC charge to display its effect on the power. The phase-shift extends from $\pm\pi$, but the maximum power transfer is achieved at $\pm\frac{\pi}{2}$. The absolute maximum power is set at 2 kW which is clearly displayed in fig. 4.2. At the lowest operation voltage of 90 V the power transfer has a maximum of 1 kW. This is verified in the simulation done in section 4.1.2. When the charging mode is initiated, the negative power spectrum is utilized. Moreover, the positive is utilized when the stabilizing mode is initiated.

5.1.3 Primary and Secondary AC Components

This section discuss the plot in fig. 4.3. The difference in primary and secondary AC current (i_{AC_1} and i_{AC_2}) is defined by the turn-ratio of the high-frequency transformer. The AC voltages v_{AC_1} and v_{AC_2} also differ in magnitude based on the transformers turn-ratio. The secondary side is shifted with respect to the primary, making the power flow from bridge one to bridge two. Each period can be divided into four stages: The primary voltage is low and the secondary high. The primary is high, and the secondary low. The shorter scenarios being when both voltages are high and both low. This decides if the inductor current is increasing or decreasing during that stage. When the phase-shift increases, the ac-currents have longer time to ”grow”, resulting in a larger current. This results in a larger power transfer, as explained in section 2.6. When steady-state is reached and the phase-shift settles, it will make small adjustments to keep the voltage as steady as possible. This results in the ac-currents fluctuation in the positive and negative direction.

5.1.4 Super Capacitor SoC Scenarios with stabilization mode

The SC is going to supply the DC-bus from 100% to 50% SOC. Hence, the goal of the results in section 4.1.2 is to visualize that this is achieved. Another topic to be discussed from the results is how the response time of the DAB is affected by a decreasing SC voltage.

The simulation starts off with the DC-bus stable at 340 V. At 2 ms the supply breaker opens, leaving the SC to supply the load. The recovery time for each scenario is different, because of the required phase-shift for different voltages. It should be noted that the first two scenarios (figs. 4.4 and 4.5) only shows a time period of 20 ms while the last two (figs. 4.6 and 4.7) shows 25 ms. This is explained by the high SOC SC reach steady state quicker than the low SOC SC. Hence, a longer simulation time is required.

From the plots in figs. 4.4a, 4.5a, 4.6a and 4.7a the time-axis displays the different stabilization times for each respective scenario. The fully charged SC is the fastest to bring the

DC-bus voltage back to 340 V with the smallest overshoot. This shows that a fully charged SC will in fact have a faster response, and gradually slow down for lower SOC, when integrated with the DAB. This is as expected since a larger phase-shift is required. This difference in phase-shift is displayed in fig. 4.4d-4.7d. The plots also show a larger overshoot to maintain the low response time as the SOC decrease.

Output power (P_{out}) in all scenarios (figs. 4.4c, 4.5c, 4.6c and 4.7c) immediately jumps to 1 kW when the circuit breaker opens since the simulation treats the DC-bus as the output. This is because the DC-bus is already charged by the external source before time 2 ms and is displayed through the input power (P_{in}) which is zero/negative before this time. Calculated efficiency for the different scenarios is also displayed in these plots. Before the breaker opens at time 2 ms and until 4 ms, this value is misleading. The output power (P_{out}) is also not correct, since it is the external source sustaining the DC-bus and not the DAB. Hence, the efficiency is displayed as outside of the plot before 4 ms.

In all scenarios, except with the fully charged SC (fig. 4.4), a reverse charging current of varying magnitude can be seen before the 2 ms mark in figs. 4.5c, 4.6c and 4.7c. This is because of the low SC voltage and constant switching of the DAB. There is practically no phase shift since the control is only designed to keep the DC-bus at 340 V. The voltage transfer ratio (eq. (2.17)) is closer to 0.5, which makes the DAB move some power into the SC without a negative phase-shift.

Lastly, the phase-shift plot (figs. 4.4d, 4.5d, 4.6d and 4.7d) is displayed for all scenarios. A larger phase-shift is required to stabilize the DC-bus as the SC voltage decreases.

In the last scenario (fig. 4.7) the SC is charged to 90 V, which is set as the limit for the converter to supply the DC-bus. During normal operation, the control system is designed to stop the converter when the SC voltage reaches this voltage. Hence, the limit is disabled to display the results when the converter is supplied with this voltage. It is clearly displayed in fig. 4.7d that the converter is on the brink of collapsing. The maximum phase-shift of the converter is the 1 µs/$\frac{\pi}{2}$ mark, which is exceeded in this scenario.

5.1.5 Supercapacitor charging scenario

This section discuss the charging mode of the SC (section 4.1.3) and how the DAB is suited for this task. The scenario has a trigger at 5 ms when the charging mode is selected. This is clearly displayed in fig. 4.8d when the phase-shift decreases quickly to about 0.25 µs/25% and delays bridge one with respect to bridge two by this amount. Compared with the stabilization scenarios (section 5.1.4) this is quicker, since it is easier for the DAB to transfer power in the direction of the lower voltage. This is explained by the voltage-transfer ratio in eq. (2.17) which is 0.83 in this case. This is also visualized with the small charging current in

fig. 4.8a and power in fig. 4.8c.

At the trigger point, the input power (P_{in}) and output power (P_{out}) have switched places due to the opposite power direction. The input is the first to react in fig. 4.8c, causing a slight drop in efficiency. This is quickly neutralized when the output catches up to the input. The efficiency in this mode settles nicely around 97.7%. Before the trigger, when the phase-shift is zero, the efficiency is stable at 95%. A more realistic transformer can be included to improve the model. The transformer used is ideal, which gives high efficiency.

5.1.6 Response time

The time it takes from the DC-bus voltage decreases to the SC can bring it back to 340 V is increasing as the SC voltage decreases. The DC-bus/secondary voltage from all stabilization scenarios (figs. 4.4a, 4.5a, 4.6a and 4.7a) is plotted in fig. 5.1. This is to further display the response of the DAB and showcase how the voltage curve is stretched as the SC voltage decreases. The overshoot is also displayed more clearly.

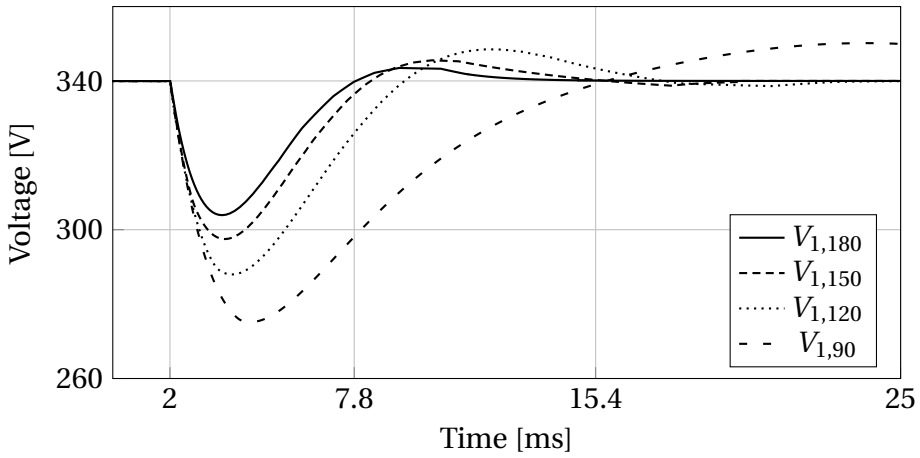


Figure 5.1: DC-bus voltages for all physical supercapacitor load scenarios

Figure 5.1 clearly displays the importance of keeping the SC charged and charge it when it is not needed. The IBDC has the fastest stabilization time of 7.8 ms and the slowest of 15.4 ms. A good tool like the stateflow chart in Matlab®/Simulink® is crucial to optimize the SC usage together with the DAB, and charge it when it is not needed. This needs consideration when developing the overall energy management system and can easily be implemented by a MCU or Programmable Logic Controller (PLC) to initiate the different modes. In the developed stateflow chart (appendix C.1.4), the stabilize mode can be triggered by a dropping DC-bus voltage and charging mode after the DC-bus voltage has been stable for a certain amount of time. The charging control can also be tuned for a slower response to increasing the charging current slowly. This will not significantly load the DC-bus, preventing a large voltage drop and triggering the stabilize mode again.

The response time of the DAB discussed in this section only considers how it is affected by changes in the SC voltage. Section 5.3 will take this a step further and look at the SC's transient response without the DAB to clarify how it is affecting the response time of the DAB.

5.2 Supercapacitor Model in Matlab®/Simulink®

This section discuss the results gathered from the SC simulation (section 4.2) in Matlab®/ Simulink®. Firstly, the charging results of the SC from section 4.2 are discussed with a focus on the cell balancing and un-even charging. Secondly, the discharging of the SC is covered briefly and discuss the un-even discharging of the different capacitance cells. The result from section 4.2.3 is discussed in section 5.3 and directly compared to the integrated SC design results.

5.2.1 Charging

The SC is charged by utilizing a pre-charge circuit consisting of a resistor of 30 Ω and voltage source of 30 V. This way, a high in-rush current is prevented and limited to 1 A. As the voltage increases, the charging current drops off gradually because of the smaller voltage-drop over the resistor. At 30V × 0.9 the pre-charge switches off and connects the charging circuit. This circuit only has a resistance of 0.4 Ω and is estimated from the physical circuit. This value is lower for the physical module because of the low ESR in each SC cell. The charging current increases to about 7 A for a short duration when the pre-charge is disconnected until the SC is fully charged. This completes the charging of the SC by pre-charge and charge circuit. The whole charging scenario is complete after approximately 2200 s.

The SC cells differ in capacitance from 360 F to 432 F, which is a +20% increase in capacitance. This is done to visualize the worst case in capacitance. This makes the cells charge un-even and can be seen in fig 4.9c. Fig. 4.9d shows how the balancing current is higher for the cell with the highest cell voltage. Cell with the smallest capacitance receives the highest charge because it can contain less energy. Still, the voltage comes close to the rated voltage of 2.7 V, but not quite. This means the balancing is sufficient, and the charge mode is balancing out the cells after the total voltage reaches 30 V. The cell voltage must not exceed the absolute maximum cell voltage rating, as it will damage the SC. There is room for improvement in the balancing circuit, since the voltage comes close to the absolute maximum rating.

5.2.2 Discharging

Similar to the charging scenario and fig. 4.10 it is clear that the cells also discharge un-even when their capacitance is not equal. The SC is discharged through a load of 30 Ω, same as the pre-charge resistance. The difference in balancing current of each cell in fig. 4.10d is only explainable from the difference in cell voltage. The cell with the lowest capacitance will discharge first because it can hold the least energy. This is the same for charging, which means the weakest cell is the one first to receive over-voltage in the case of over-charging.

5.3 Supercapacitor Transient Response

In this section, the response of the simulated SC (section 4.2.3) is compared with the integrated SC design's transient voltage and current response (section 4.3.1).

5.3.1 Simulated Supercapacitor

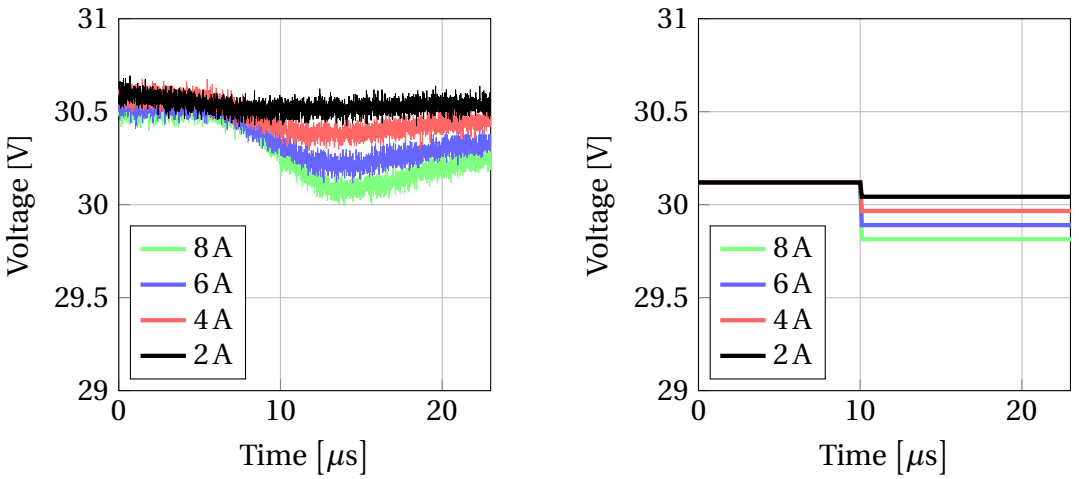
The simulated SC in fig. 4.11 has an instantaneous transient response for all load scenarios. The transient voltage drop is increasing with about 77 mV for each increase in load. The instant response in voltage and current indicates that its rise time is practically zero for all loads with no visual overshoot.

5.3.2 Physical Supercapacitor

The integrated SC design's voltage transient from fig. 4.12 show a distinct behavior with an overshoot. This characteristic becomes more visual as the load increase. The current in fig. 4.12 is increasing over the plotted period from zero to the listed load. Curve data from the plot is displayed in table 4.1 and suggests a slower rise time for smaller current. This is because of the rise times definition described in section 4.3 and is the time when the curve rises between 10% and 90%. It introduces some uncertainties since the low load will increase faster than the large load compared to the trigger point at time zero. Therefore, the rise time is somewhat misleading and is not a good representation of the overall response time. However, the time it takes for the current to start rising will be shorter for the low load. The programmable DC-load may explain the source of error. Moreover, the settling time is not a very good indicator because of the minor voltage irregularities in the physical measurement. The settling time is defined when the value reaches 2% of steady-state. For the 2 A load, this is 1.98 A, and the irregularity in the measurement indicates a source of error. The same is valid for the overshoot (*OS*). Moreover, the voltage drop is not significant and is only about 0.4 V for the most significant 8 A load.

5.3.3 Comparison

For simplicity, the voltages from figs. 4.11 and 4.12 are plotted in fig. 5.2. This way, the difference between the two plots will be more clear. From the start, the two plots display a slight voltage difference. The simulated SC in fig. 4.11 starts with a voltage of 30.1 V, while the physical in fig. 4.12 is closer to 30.5 V.



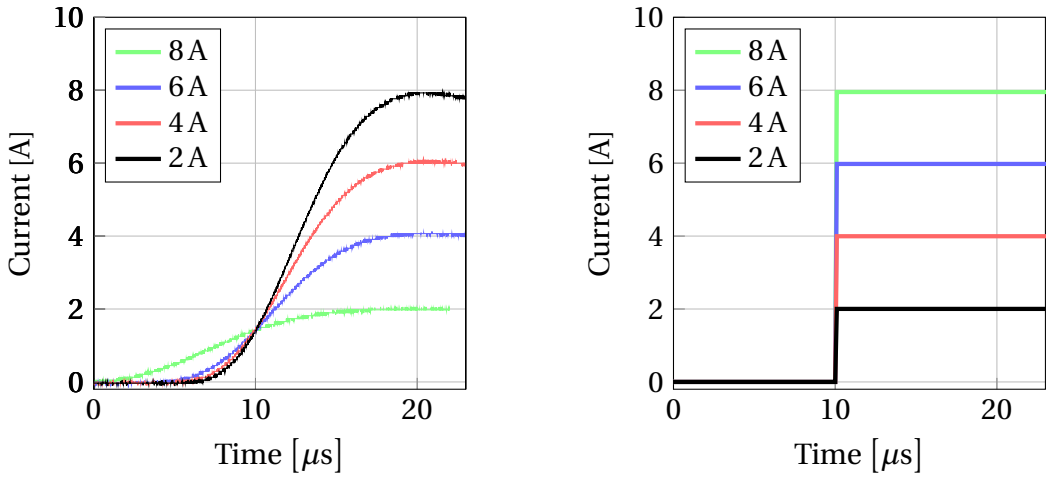
(a) Physical SC voltage transient response

(b) Simulated SC voltage transient response

Figure 5.2: Voltage transient response of the physical and simulated supercapacitor

When comparing the two SCs, the transient response is completely different, with the largest difference being the rise time. The rise time of the simulated SC is practically zero, while for the real module, it is significantly larger. However, the size of the voltage drop is more comparable. For the physical SC in fig. 5.2a the voltage drop is about 0.4 V and 0.3 V for the simulated. This is a 25% difference that might prove to be significant for a larger load.

The same is done for the currents in figs. 4.11 and 4.12 to display the difference in transient response in fig. 5.3. All currents in the simulated scenario rise from zero to the respective current value instantly. The physical current starts to increase first for the low load current. This is consistent through all loads. On the other hand, for the larger load, the current's rise time is shorter when it first has started to rise. This characteristic is not anticipated, and the programmable DC-load may be the source of error. Moreover, it is safe to say that the physical SC has a much slower transient response than the simulated.



(a) Physical SC current transient response (b) Simulated SC current transient response

Figure 5.3: Current transient response of the physical and simulated supercapacitor

5.3.4 Considerations

Since the DAB (section 4.1) is simulated with the same SC block as in fig. 4.11, it is not affected by the integrated SC design's slow response, compared to the simulated. This needs consideration when developing the physical DAB DC-DC converter. With a frequency of 250 kHz and a period of 4 µs the overall response of the DAB will be somewhat slower than the simulated results. It is still hard to predict exactly how this difference in response time will affect the converter. Implementing a more robust control method than a regular PI-controller will also help the response of the converter. A good alternative here is the model predictive control, which also predicts the future response. Also, introducing a more advanced switching strategy like double-phase-shift will increase the power transfer capability and extend the soft switching range of the physical DAB. The difference between the physical and simulated SC is also one major topic in the conference paper in appendix A.

Testing of the integrated SC design is limited to a load of 8 A because of the programmable DC-load listed in table 3.5. It is desirable to test the module against a more significant load with a larger current to investigate the larger voltage and current transient. This will also help test the settling time of the current further and give a correct value. The programmable DC-load also introduced some exciting sources of error in regards to the rise and settling times. To test the SC against a different load is desirable to validate if the load causes the characteristic or not.

6 Conclusion

6.1 Conclusion

In this thesis, an IBDC is implemented with the renowned DAB topology and integrated with a SC to strengthen the stability of DC-microgrids. The DC-DC converter is simulated in Matlab® / Simulink® with a high switching frequency to fully utilize the SC's strengths. A control system is integrated with SPS modulation and different control modes to direct the SC's power flow. As a stepping stone towards a physical IBDC development, the crucial energy storage is investigated further. A SC model with integrated cell balancing is first simulated, followed by a integrated SC system prototype. A comparison of the simulated SC and the physical SC design is carried out and presented.

Simulation results indicate that the combination of the DAB and a SC is promising to quickly stabilize a DC-bus. The SC's SOC will greatly affect the response time of the IBDC and is considered when developing the control system. As expected, the SC results show large variations between the simulated SC model and the physical integrated SC design. The simulated SC results show an instant transient response compared to the physical SC's more realistic response. However, the SC should be able to handle a DAB with fast switching frequency, but an overall slower response time from the IBDC is expected with a physical design.

6.2 Future work

The following prioritization of events are considered for achieving a physical IBDC development in the future.

- test the SC prototype with a different DC-load and compare the transient responses for larger loads with the original results.
- improvements to the SC module's integrated design and assemble multiple modules in series for higher voltage level.
- implement a more robust control method, such as model-predictive control, and more

advanced switching strategy, such as dual-phase-shift. Investigate the possibility of a lower sampling rate with a different control strategy.

- develop the physical DAB model prototype and execute tests with the already tested SC design and DC-bus.

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A ICECCME 2021 Conference Paper - Submitted for Review

Comparison of Supercapacitor and Battery Transient Response for DC-bus

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***Abstract*—A comparison of different transient responses by a supercapacitor and battery reacting to a load is presented in this paper. The main focus is improving energy storage systems designed to support a DC-microgrid. This is done by introducing the two storage devices to act as stabilization elements. Through simulations in Matlab®/Simulink®and physical models, a comparison is achieved. Transient characteristics from the simulations tend to give a faster response than the physical. Verification on the error between ideal and physical are analyzed based on the results.**

***Index Terms*—Renewables, DC-bus, DC-microgrid, energy storage, battery, supercapacitor, isolated bidirectional DC/DC converter(IBDC),**

I. Introduction

This paper presents a comparison between the transient response of a battery and a supercapacitor connected to various loads. Energy storage and renewable energy production [1] connected with a DC-microgrid prove necessary for many applications [2]–[4], due to the unpredictability of renewables, as they often are dependent on irregular energy sources. In addition, the transient response in a DC system is more critical than in a comparable AC system.

The growing trend with wind- [5], [6] and solar-energy [7] is increasing the demand for energy storage with a low response time [8]. Combining energy storages with varying response times may respond faster to DC-microgrid energy demand. Storage devices as supercapacitors are assumed to react more rapidly to change in demand than devices like batteries. Thereby, combining the supercapacitor and the battery in a system, a faster response time can be achieved when required.

The use of batteries and supercapacitors in combination has been studied and researched; a paper on energy management of fuel cell, battery, and supercapacitor is described in [9], where the systems response time measurements are included. Similarly, [10] presents batteries and supercapacitors for use in electric/hybrid vehicles. Each storage device can deliver power to the DC-bus in a typical energy storage system through an isolated bidirectional DC/DC converter. A potential model configuration is shown in Fig. 1 which exhibits a simplified configuration. With a slightly faster storage device, the overall response time of the storage system can be significantly decreased.

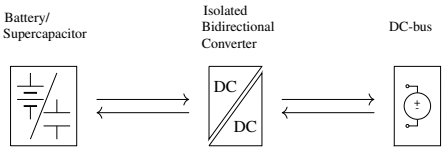


Figure 1: Model configuration for energy system

One of the principal differences between a battery and supercapacitor is power density versus energy density [11]–[13]. While a supercapacitor can release large amounts of energy in a short period, a battery can store significantly greater amounts of energy [14]. Therefore the supercapacitor possesses high power density while a battery has a high energy density compared to each other. Combining and compromising the sources provides a high-performance system with fast transient response.

The battery stores energy as an electrochemical reaction as opposed to the supercapacitor, which utilizes static charge [15], [16]. This difference in energy storage is the primary cause of the unique response times. This paper will showcase the difference in energy ability and response of the two sources while responding to a programmable load.

The paper is organized as follows: Section II presents the model description and laboratory test setup and the design of the batter and supercapacitor system. Section III presents the test cases with results. Section IV presents the conclusions.

II. Model Description

When comparing the transient response of the storage devices, they must have a common factor. In this paper, a requirement of a nominal voltage of close to 30 V is applied. However, the battery and supercapacitor capacity will vary, as this was not feasible to match.

Each supercapacitor cell has a maximum voltage of 2.7 V, thereby 12 single cells must be connected in series to reach a maximum voltage of 32.4 V and a nominal voltage of 30 V. The supercapacitor parameters are displayed in table I [18], while the maximum stored energy and usable specific power is calculated in (1) and (2), respectively. Compared to the supercapacitor, the battery has a higher cell voltage of 4.2 V,

Table I: Supercapacitor Module Specifications

Type	Value
Cells in Series	12
Capacitance	30 F
Nominal Voltage	30 V
Maximum Current	20 A
Maximum Power	600 W
DC ESR	38.4 mΩ
Maximum Stored Energy	3.75 W h
Usable Specific Power	3282.56 W/kg
Total SC Weight	0.8568 kg

Table II: Li-ion Battery Specifications

Type	Value
Cells in Series	8
Cells in Parallel	2
Nominal Voltage	29.6 V
Maximum Current	10.4 A
Maximum Power	305.76 W
DC ESR	38.4 mΩ
Maximum Stored Energy	159.92 W h
Usable Specific Power	409.36 W/kg
Total Battery Weight	0.752 kg

with a nominal voltage of 3.7 V; therefore, only eight cells connected in series are required. The battery parameters are collected from the datasheet [19] and presented in table II.

The supercapacitor and battery parameters showcase the difference between the storage devices. The maximum stored energy is significantly higher in the battery, while the usable specific power in the supercapacitor considerably exceeds the battery; this corresponds with the assumptions made in the introduction.

As the voltage requirement is set to 30 V, the supercapacitor is designed with 12 cells in series. These cells are soldered directly to a PCB, with built-in balancing and measurement [20]. The passive balancing system is designed with a constantly discharging current. As a cell charges to a higher voltage level than the rest, the discharging current increases, causing the pack to balance. Included in the PCB design is both current and voltage measurement over the supercapacitor bank.

The supercapacitor is charged up to the required 30 V with an EA-PS 2032-050 30V laboratory power supply. A passive cell balancing circuit is designed, to prevent un-even cell charging. This system balances the cells so that the cells with higher voltage discharge faster than the other. The PCB requires a 15 V DC supply to power the circuitry. For this supply, the mascot 719 DC power supply is utilized.

The battery is design as two 4S2P packs connected in series, equaling an 8S2P pack. The eight cells in series produce a nominal voltage of 29.6 V, while the parallel cells increase the capacity from 2.6 A h to 5.2 A h. Contrary to the supercapacitor, each cell pair of the battery pack is connected to a sensor PCB connected to a central controller PCB. These cards are based on an open-source project designed by Stuart Pittaway [20]. The sensor cards interact through standard UART serial communication with a single control card. The external sensor cards have implemented passive balancing. Instead of constantly discharging the cells, they are only discharged when the voltage level is too high. This action is achieved by redirecting the current through a MOSFET when required.

$$E_{max} = \frac{0.5 \cdot C \cdot {V_R}^2}{3600} \tag{1}$$

$$P_{usable} = \frac{0.12 \cdot {V_R}^2}{ESR_{DC} \cdot Weight} \tag{2}$$

The measured cell voltage is presented to the controller PCB and can be displayed on a local network. This system requires a 5 V DC supply via a USB charger to power the wifi controller. However, the balancing circuit will work without this supply. Due to the unique charging characteristic of the lithium-ion battery, a constant-current constant-voltage charger is obliged to charge the battery. For this purpose, a SkyRc E680 smart charger is applied to charge the voltage to 30 V.

Equipment used during testing is found in table III. The setup displayed in Fig. 2 consists of a programmable load, the sources, and an oscilloscope. The load is an EL 9500-08 T electronic DC load. With a maximum input voltage of 500 V and a maximum input current of 8 A, it is thereby not limited by the battery or supercapacitor at 30 V. The load features a touchscreen and simple control settings, allowing for fast and easy tests and use. The current mode is set to rectangular function for the tests, which produces a square wave signal for the input current.

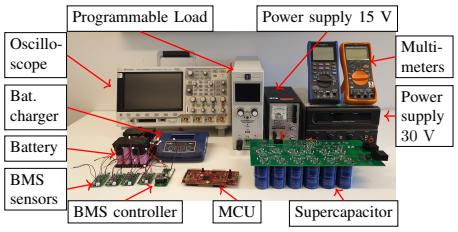


Figure 2: Laboratory test equipment

Table III: Laboratory test equipment

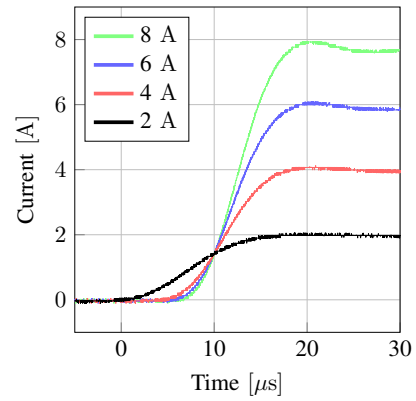
Type	Manufacturer	Type
Programmable Load	Elektro-Automatik	9500-08 T
Oscilloscope	Keysight	MSOX3014A
Diff. Probe	Micsig	DP10013
Current Probe	Micsig	CP2100A
Power Supply	Elektro-Automatik	EA-PS 2032-050
Power Supply	Mascot	719
Battery Charger	SkyRc	E680
Supercapacitor	Maxwell Technologies	BCAP0360 P270 S18
Battery	Samsung	18650

The controller can adjust the amplitude to reach the required

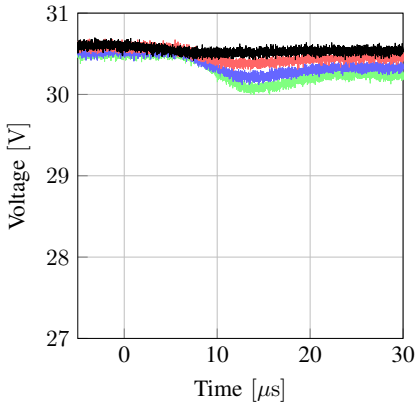
current level and change the upper and lower pulse width. For the test performed, both pulse width is 1 ms, and the current amplitude increases to 2 A, 4 A, 6 A, and 8 A between each test. The frequency of the pulse will therefore be 500 Hz, with a duty cycle of 50%. This square wave signal is measured with a CP2100A current probe connected to an MSOX3014A oscilloscope from Keysight. For the voltage measurement, a DP10013 differential probe is utilized. These probes have an accuracy of 3% and 2%, respectively.

III. Results

The current and voltage response by the supercapacitor from the laboratory tests are plotted in Fig. 3. From Fig. 3a, the current rises steadily from zero to each load current reference of 2 A, 4 A, 6 A, and 8 A. The plot characteristic from the currents are displayed in table IV, and are obtained from Matlab®by utilizing the "stepinfo" command. The rise time is the period between 10% and 90% of the steady-state value and shows the rate of current increase.



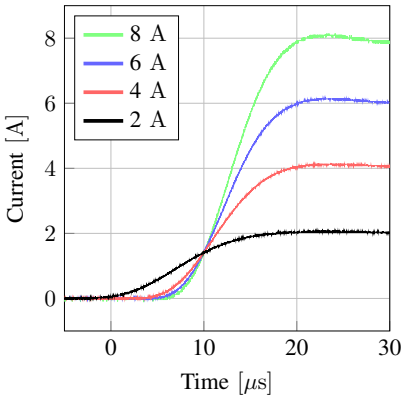
(a) Currents



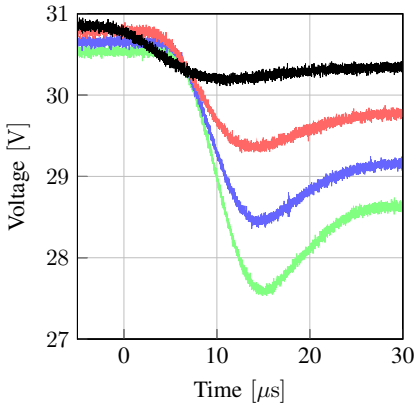
(b) Voltage transients

Figure 3: Supercapacitor current and voltage during load scenarios from physical model

However, it is essential to note the complete response from time zero when the load is initially connected. The settling time is the period between the initial step response and a value within 2% of the steady-state value. The overshoot represent the maximum percentage the response touches compared to the steady-state value. The response of the supercapacitor voltage presented in Fig. 3b shows the decreasing voltage in response to the current increase. The voltage-drop has a magnitude of 0.06 V, 0.16 V, 0.2 V, 0.26 V in response to the load currents. The results from the battery test are plotted in Fig. 4. The currents are stepped up from zero to 2 A, 4 A, 6 A, and 8 A, similar to the supercapacitor test. The current transient response is shown in Fig. 4a, while the voltage transient is shown in Fig. 4b. The plot characteristics for the current response is listed in table. V. The voltage-drop is 0.5 V, 1 V, 1.5 V, and 1.93 V, respectively to the load currents. A comparison between the physical setup and the modeled simulation in Matlab®/Simulink® is made. The simulated battery and supercapacitor models utilized are part of the Simscape electrical library.



(a) Currents



(b) Voltage transients

Figure 4: Battery current and voltage during load scenarios from physical model

Table IV: Plotinfo for supercapacitor current Fig. 3a

Type	**2 A**	**4 A**	**6 A**	**8 A**
RiseTime (µs)	10.086	8.2610	7.8208	7.6040
SettlingTime (µs)	52.172	14.547	33.007	24.746
Overshoot (%)	4.0666	4.0535	1.3407	0.7588

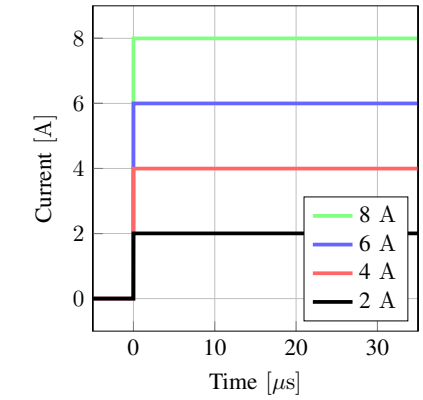
Table V: Plotinfo for battery current Fig. 4a

Type	**2 A**	**4 A**	**6 A**	**8 A**
RiseTime (µs)	11.313	9.5400	8.8175	8.4550
SettlingTime (µs)	21.345	17.980	17.820	24.640
Overshoot (%)	4.0330	4.0164	3.3649	1.7572

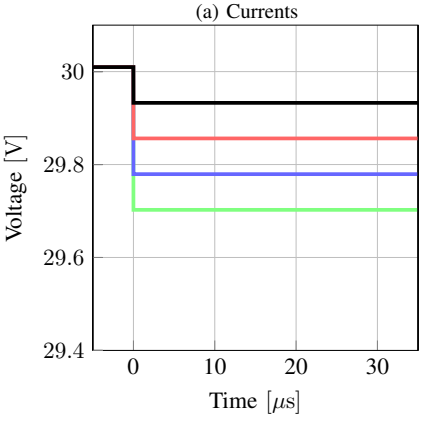
The simulated test models are designed to replicate the physical laboratory tests. The current and voltage responses from the simulated supercapacitor model are shown in Fig. 5a, and from the physical battery model are visualized in Fig. 6a. The supercapacitor and battery simulations in Figs. 5 and 6 show an almost instant current response. The voltage response shows an instant voltage-drop for the supercapacitor in Fig. 5b and decreases with 0.08 V, 0.16 V, 0.23 V and 0.31 V, respective to the load currents. The battery voltages indicate a steady decreasing curve when the current increases, visualized in Fig. 5b. The battery voltages decrease with 0.13 V, 0.26 V, 0.39 V and 0.53 V respective to the increasing load currents. The load step is initiated at time zero for every test and simulation.

IV. Discussion

The physical supercapacitor and battery currents are fairly similar at first glance, displayed in Fig. 3a and 4a. The battery currents start to rise slightly before the supercapacitor currents with an inconsiderably less steep curve. This results in a faster rise time for the supercapacitor, visualized in table IV and V. The supercapacitor 8 A load current show a sag after reaching the reference value at 20 µs. This dip is neutralized shortly outside the included time plot and indicates increasing times for larger load. The same behavior is visualized for the battery current with a slower response. This results in a small overshoot and a smaller sag. The characteristic of both the current and voltage response displays an anomaly for the 2 A.

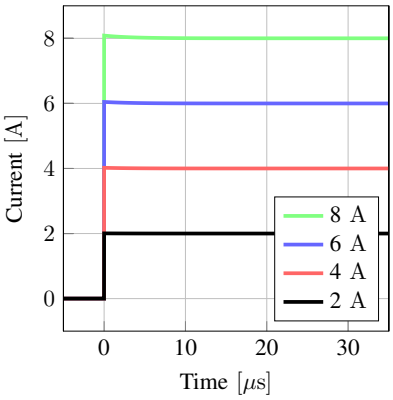


(a) Currents

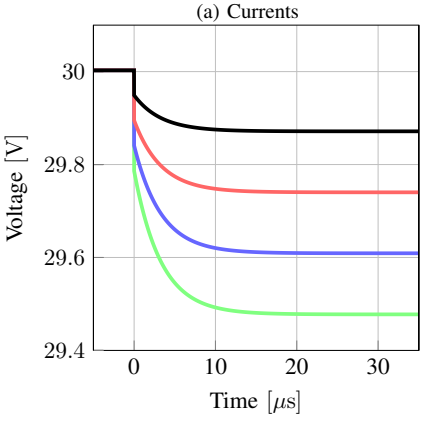


(b) Voltage transients

Figure 5: Supercapacitor current and voltage during load scenarios from simulation model



(a) Currents



(b) Voltage transient

Figure 6: Battery current and voltage during load scenarios from simulation model

As the load connects, the current rises almost immediately from the initial pulse at time zero. This characteristic visualizes a delayed response for larger currents. This delay is explained by the load not responding fast enough. Contrary to the currents, the difference in voltage response of the battery and the supercapacitor is more visually noticeable when comparing Fig. 3b and 4b. The large difference in voltage-drop explains this visual difference. For the 8 A load, the supercapacitor stabilize at $300\ \mathrm{mV}$ lower and the battery closer to 1.8 V. This is a significant contrast and originates from the large power density difference. It will also depend on the strength of the storage device. Moreover, the supercapacitor is built with physically larger cells, and another improvement to this experiment is to make the battery pack larger, with more cells in parallel, thereby increasing the capacity. This improvement will make the battery pack more robust and able to withstand the load better. Both display the same transient voltage-drop curve with an under-shoot and stabilize when the current reaches the reference value. The shape of the curve seemingly originates from the programmable DC-load.

Both physical storage devices are compared with simulated results of matching parameters. The supercapacitor displays the largest difference with the simulated supercapacitor's instant transient response during the same time window. This will have a significant impact when taking a simulation into a physical design. The voltage-drop is surprisingly similar with $300\ \mathrm{mV}$. The simulated battery, however, indicates a less ideal transient voltage response. Compared to the physical battery, the voltage transients show no under-shoot and a significantly smaller voltage-drop of $520\ \mathrm{mV}$ for the 8 A load. This indicates a limitation of the simulated battery because of the large contrast compared to the physical.

V. Conclusion

This paper compares the transient responses of both physical and simulated supercapacitor and battery storage devices. The contrasts are displayed through physical tests with a programmable DC-load, and simulations in Matlab®/Simulink®.

The results indicate a slightly faster electric response for the physical supercapacitor compared to the battery. The physical battery shows a significant voltage-drop compared to the supercapacitor, originating from the supercapacitor's bigger power density. A significant difference in voltage transient is visualized between both physical storage devices and their respective simulations. The simulated storage devices show a more consistent voltage-drop curve for all loads. Considerations need to be made when taking simulations into physical prototypes designed for DC-microgrids.

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B SEST 2021 Conference Paper - Approved Abstract

Due to the covid-19 lockdown of the campus, the physical model development was postponed, which resulted in not making the conference deadline.

Comparison of Supercapacitor and Battery Transient Response for DC-bus

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***Abstract*—A comparison of the different transient responses of a supercapacitor and a battery supporting a DC-bus is presented in this paper. The main focus is to improve energy storage systems designed to support DC-bus in a microgrid. This is done by introducing a battery or a supercapacitor to act as a stabilization element. The two elements will be compared through simulations in Matlab/Simulink and physical components. Transient characteristics from the simulations tends to give a faster response then the physical components. A verification on the error between ideal and physical are analysed based on both simulations and measurements. The results will be presented in the full text paper.**

***Index Terms*—Renewables, DC-bus, DC-microgrid, energy storage, battery, supercapacitor, isolated bidirectional DC/DC converter(IBDC),**

I. Relevant Conference Scope

This paper fits well into the conference scopes of SEST2021 and the authors agree that the scope prioritization for this paper is:

1) Energy Storage Systems and Technologies
2) Microgrids, Virtual Power Plants, and Aggregators
3) Renewable Energy and Distributed Generation

II. Introduction

This paper presents a comparison between battery and supercapacitor transient response when supporting a DC-bus. Energy storage together with renewable energy [1] production and DC-microgrid is proving to be a necessity for many applications [2]. A growing trend with wind [3] and solar [4] is increasing the demand for energy storage with a low response time [5] [6]. By combining different storage devices the system will be able to respond faster to the DC-microgrids demand. The faster storage can initially react before the main storage responds. A paper on energy management of fuel-cell, battery and supercapacitor is described in [7], where measurements of the systems response time is included. Both of the energy storage devices will deliver power to the DC-bus through a isolated bidirectional DC/DC converter(IBDC). The model configuration is shown in Fig. 1 and shows how the two sources are connected. The main difference between a battery and a supercapacitor is power density versus energy density [8]. While a supercapacitor can release large amounts of energy in a short period of time, a battery can store larger amounts of energy [8]. This is why a supercapacitor has high power density while a battery has high energy density compared to each other. This paper will showcase the difference in energy ability of the two sources through the response of a dropping DC-bus by supporting the transient period [8] [9].

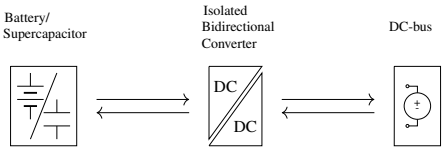


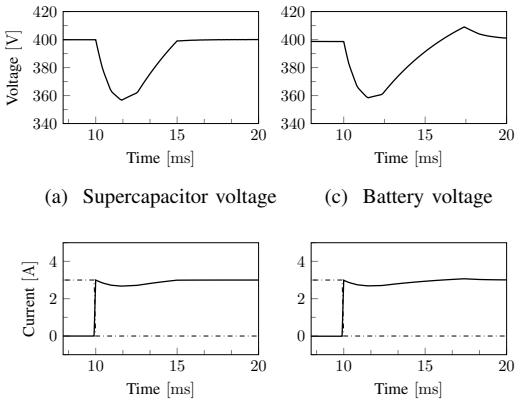
Figure 1: Model configuration for energy system

III. Results

Simulation results for both the supercapacitor and the battery can be seen in Fig. 2. Both the voltage and current response is shown. The voltage level on the DC-bus is set to $400\,\mathrm{V}$ and the current load is $1.2\,\mathrm{kW}$. The voltage drops as a load increase is forced on the DC-bus. When it reaches roughly $360\,\mathrm{V}$ the energy system responds. The load current decreases as the external energy storage takes time to respond. Simulink simulation shows a small difference in the transient response from a battery compared to supercapacitor. A voltage overshoot can also be seen from the battery simulation. As these are ideal components, a slightly different behavior from physical components is expected. These will be analysed and simulated in full paper. From the simulation it is expected that the supercapacitor will have a faster response than the battery with physical components [7]. A method based on the cost benefit for optimal sizing is presented in [10]. The size of a storage device is dependent on the required power and amount of time the DC-bus has to be supported [10].

IV. Conclusion

With the responses from the Matlab/Simulink simulations, the supercapacitor and battery shows signs of a different transient response then the physical measurements. The error between the physical and simulated model is shown through this paper. More results from simulations and physical model will be included in full paper.



(a) Supercapacitor voltage (c) Battery voltage

(b) Supercapacitor current (d) Battery current

Figure 2: Transient response of battery and supercapacitor

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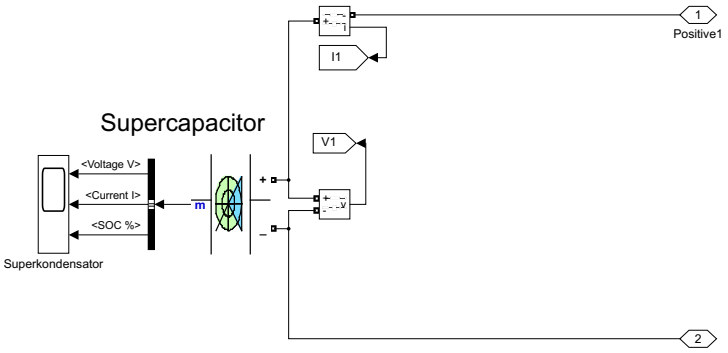
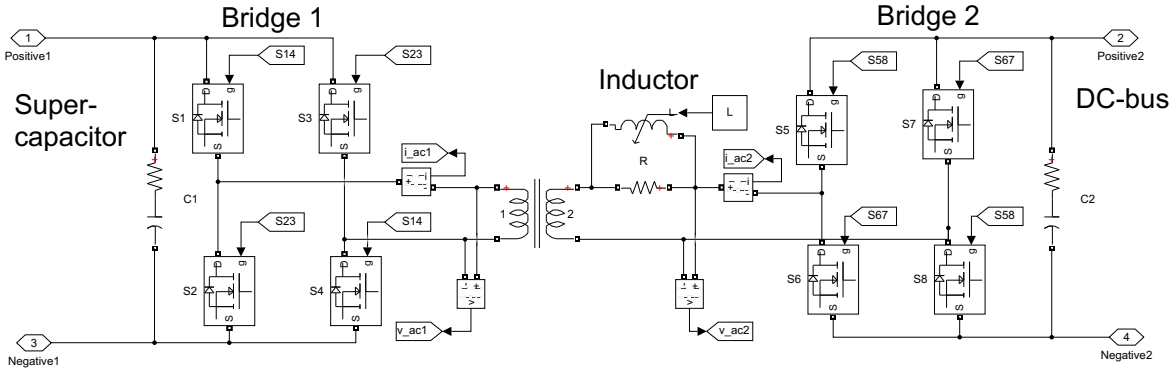
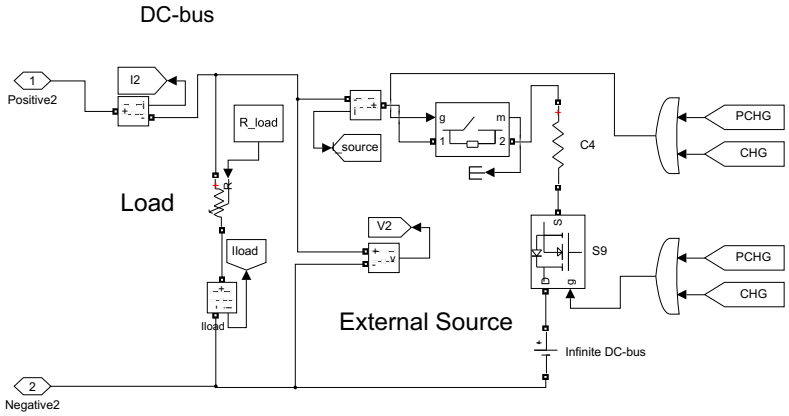
C Matlab®/Simulink® Diagrams

C.1 Dual Active Bridge Model with Supercapacitor and DC-bus

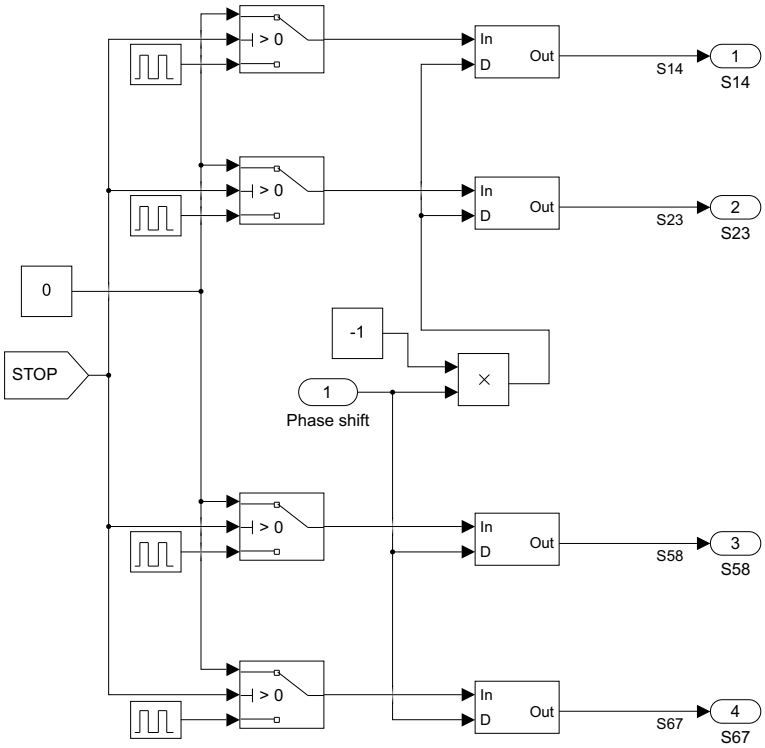
C.1.1 Setup with Supercapacitor, DAB and DC-bus



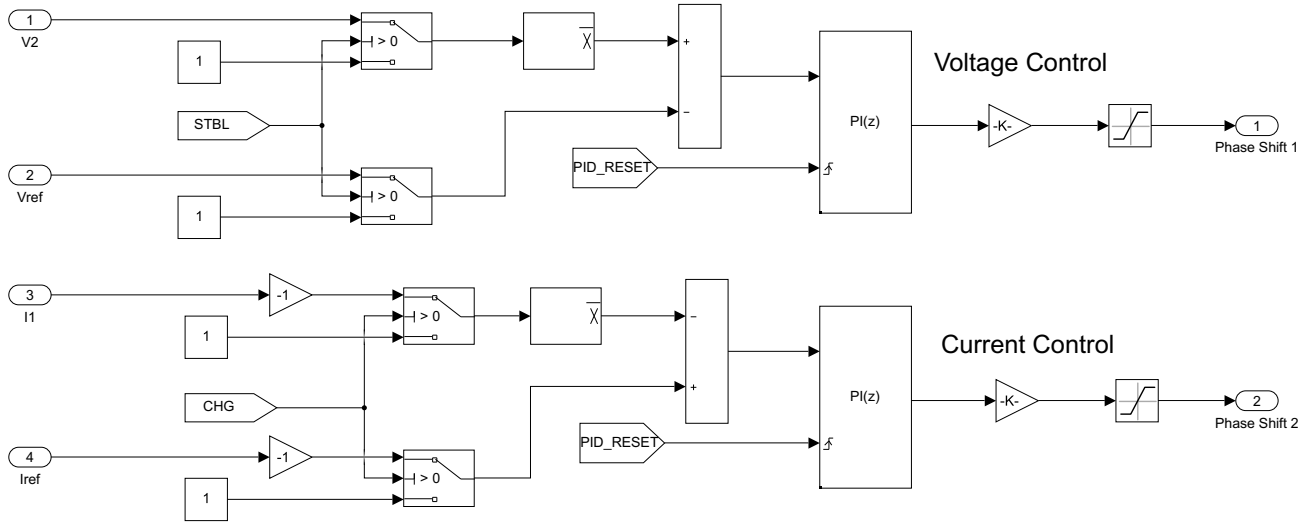


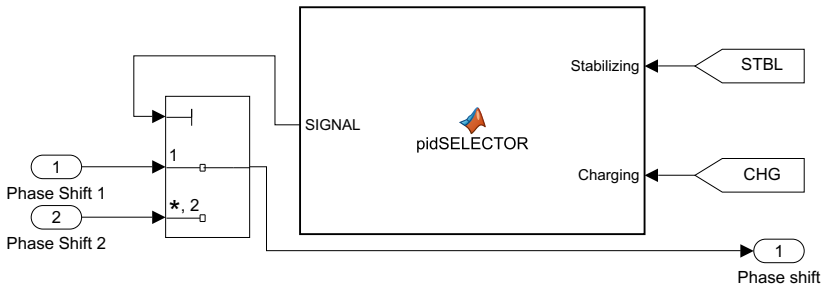


C.1.2 MOSFET Gate Signals

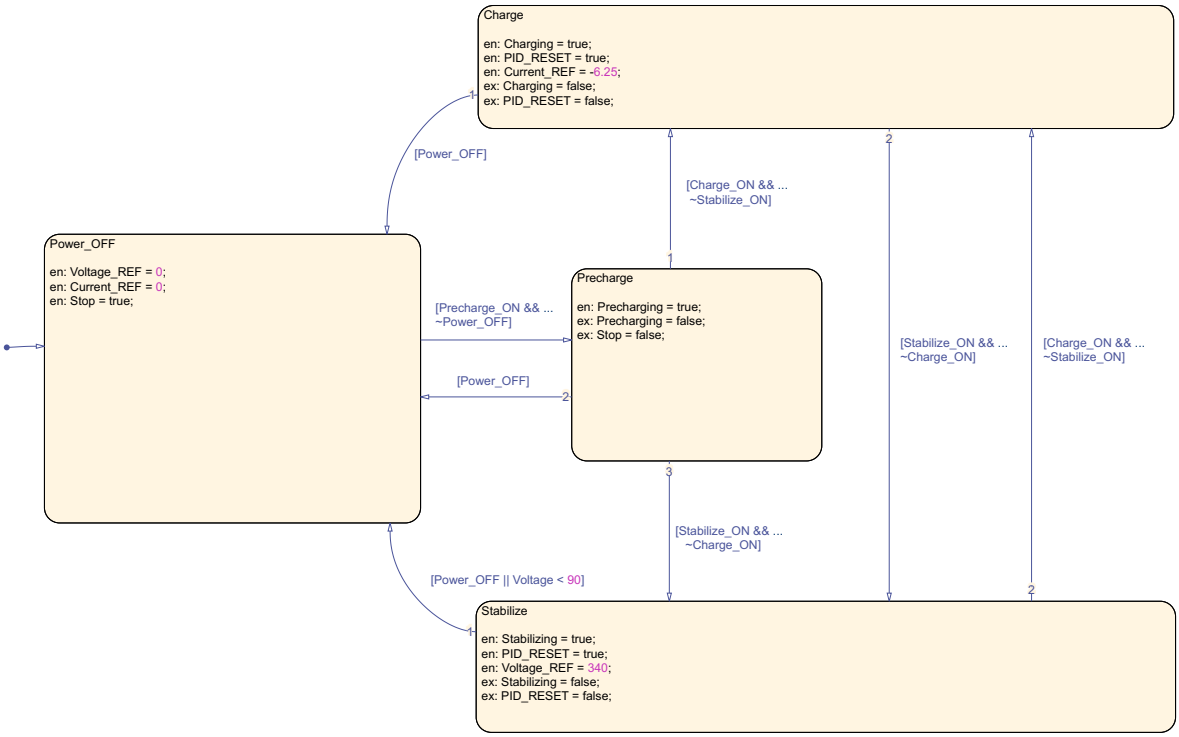


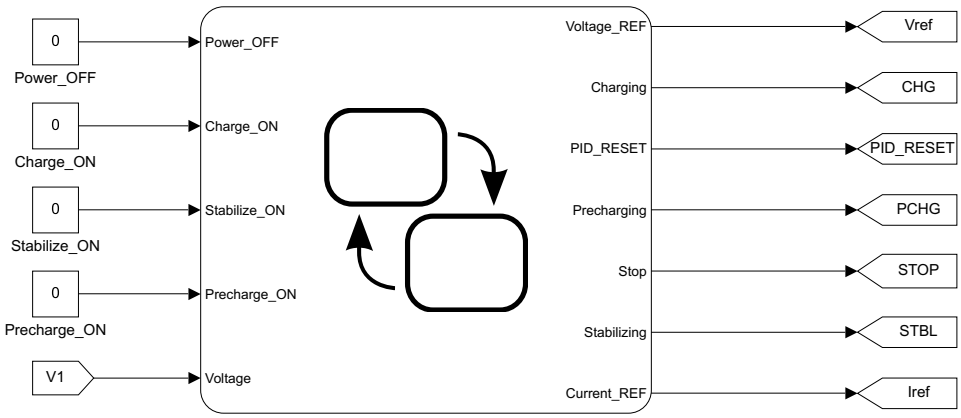
C.1.3 PI-Regulators for Phase-Shift



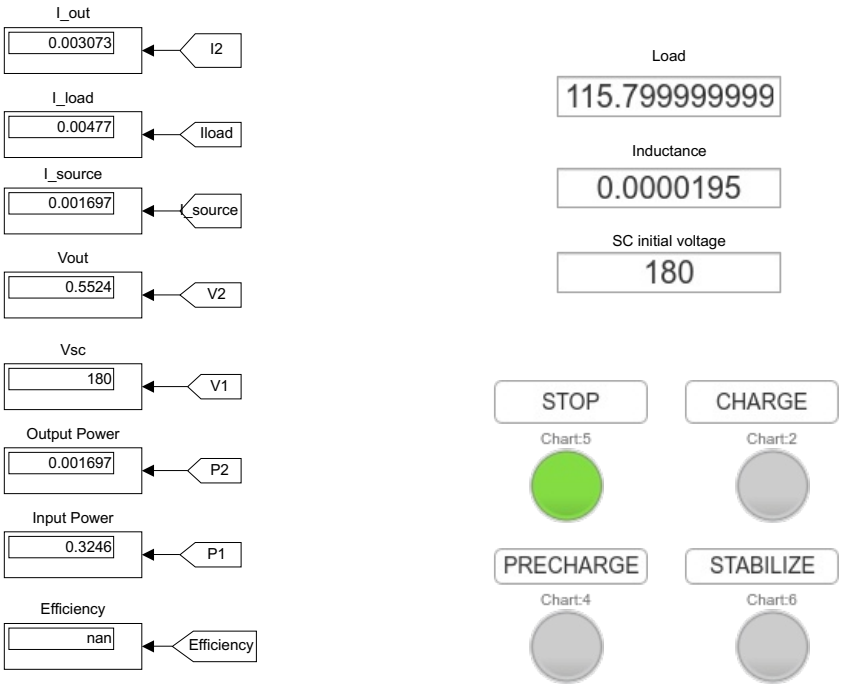


C.1.4 Stateflow Diagram to Control the Simulation

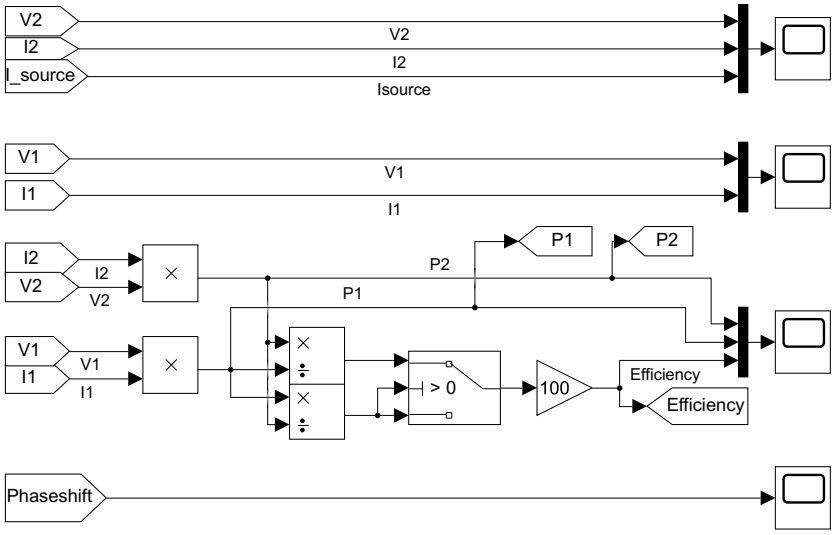




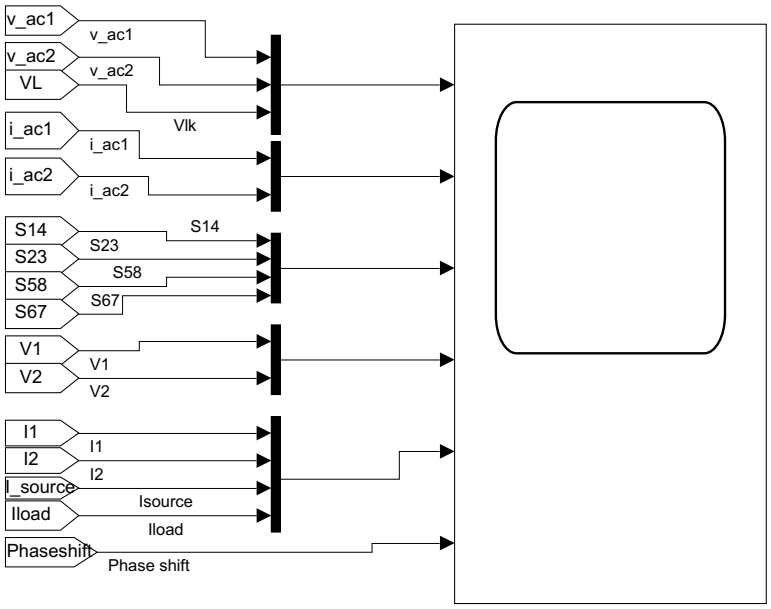
C.1.5 Displays and Control



C.1.6 Scopes Used for plotting

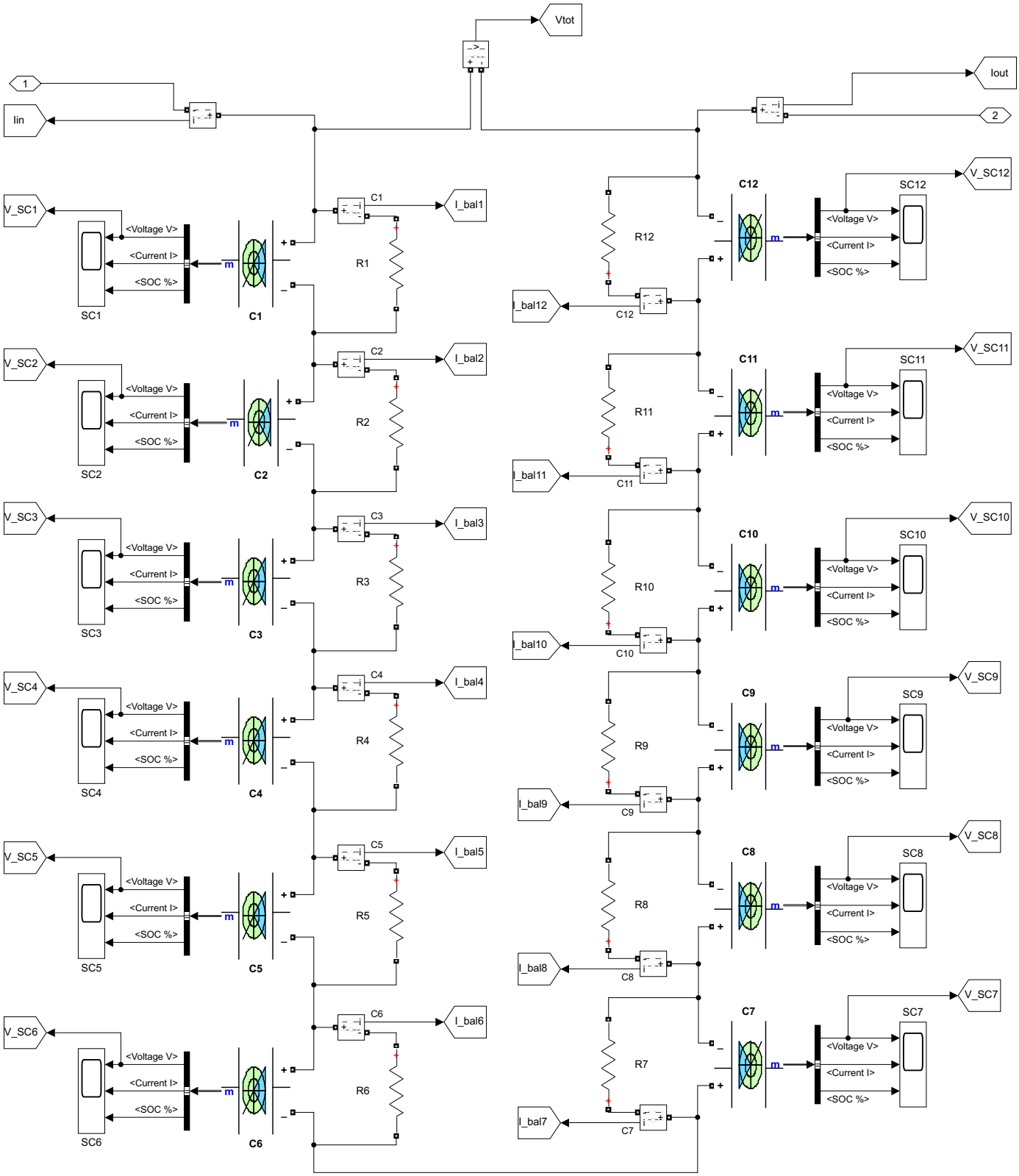


C.1.7 Scope Used During Simulation

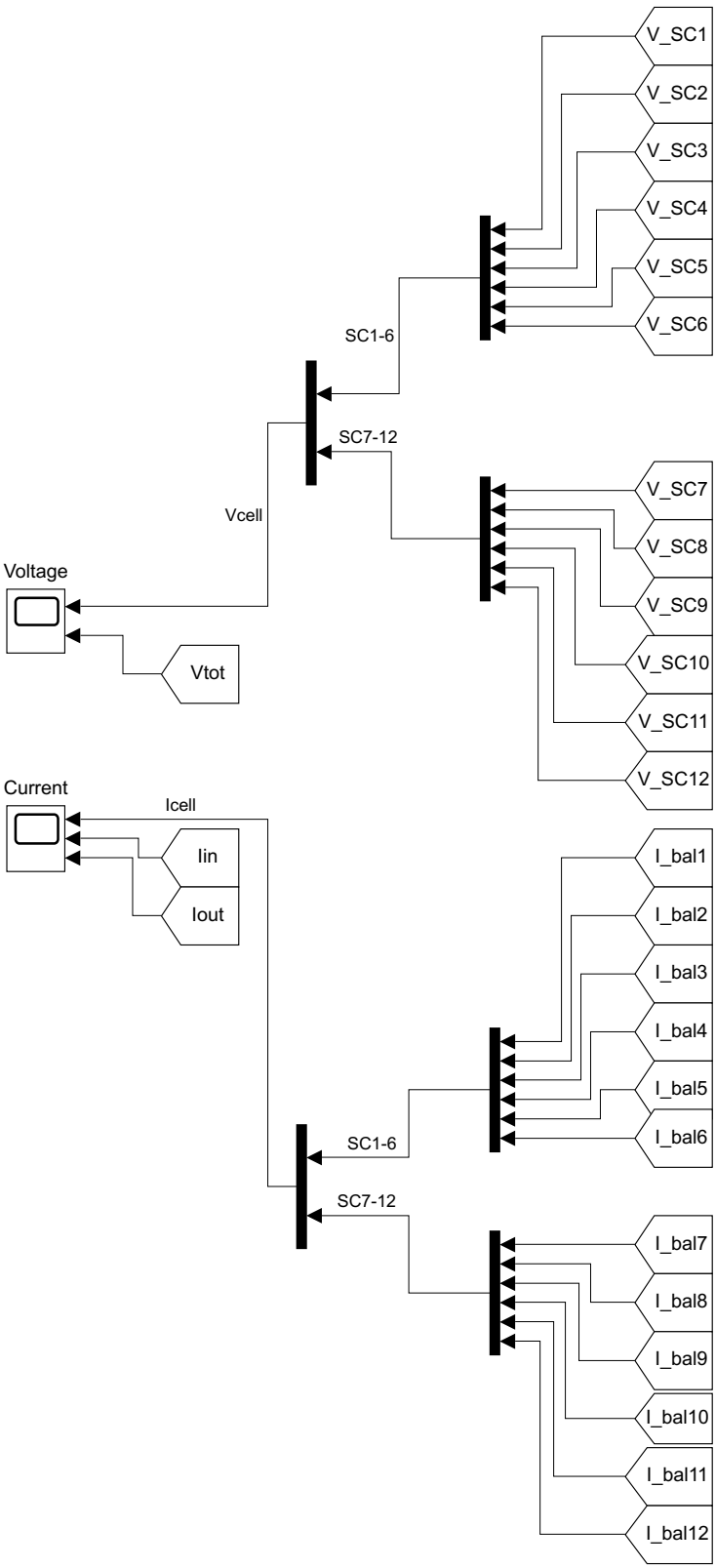


C.2 Supercapacitor Model with Passive Cell Balancing

C.2.1 SC Cells Arrangement in Series, with Balancing, Current and Voltage Measurement

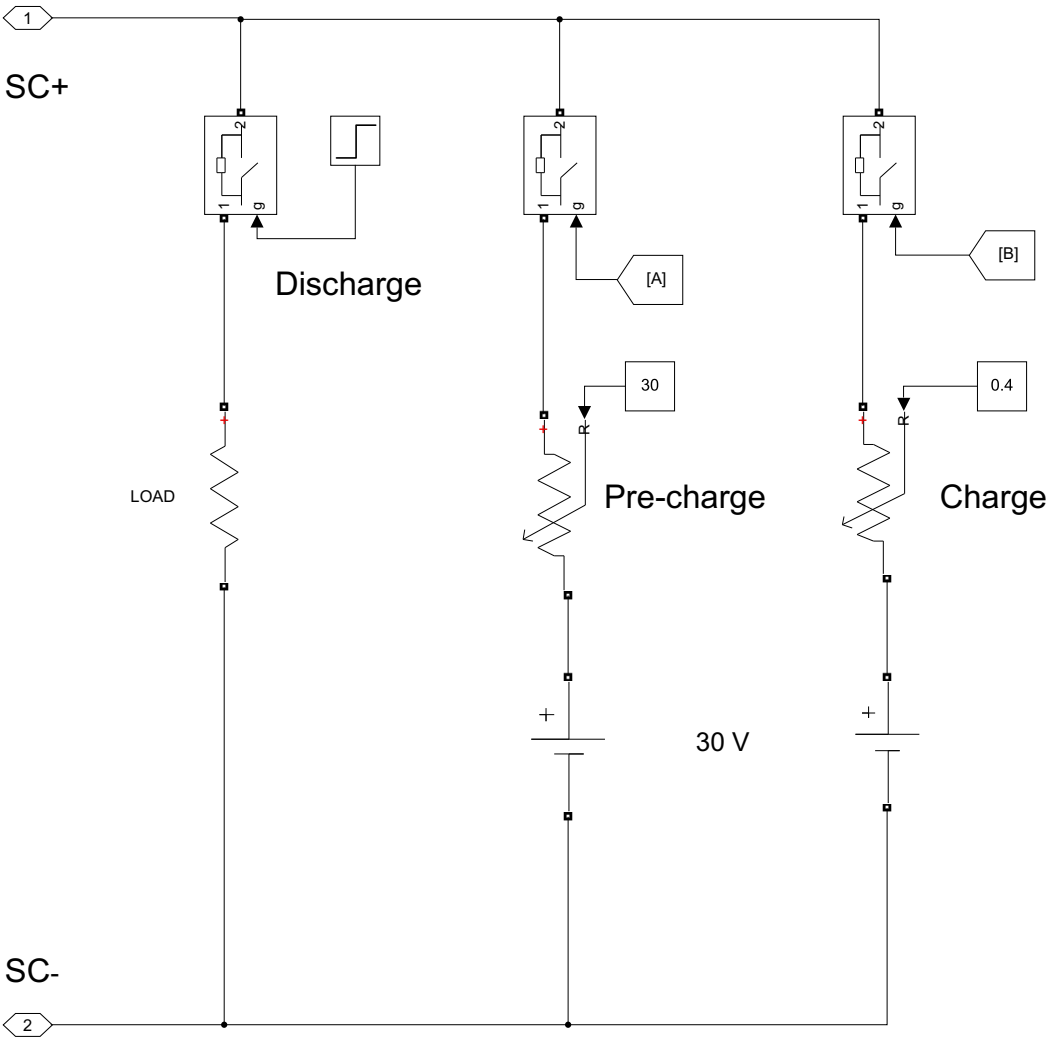


C.2.2 Scopes for Voltage (Total and Cells) and Current (Input, Output and Cells)

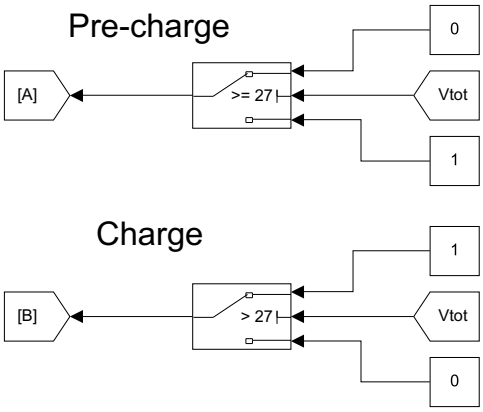


C.2.3 Control of Discharge, Pre-charge and Charge for the Supercapacitor

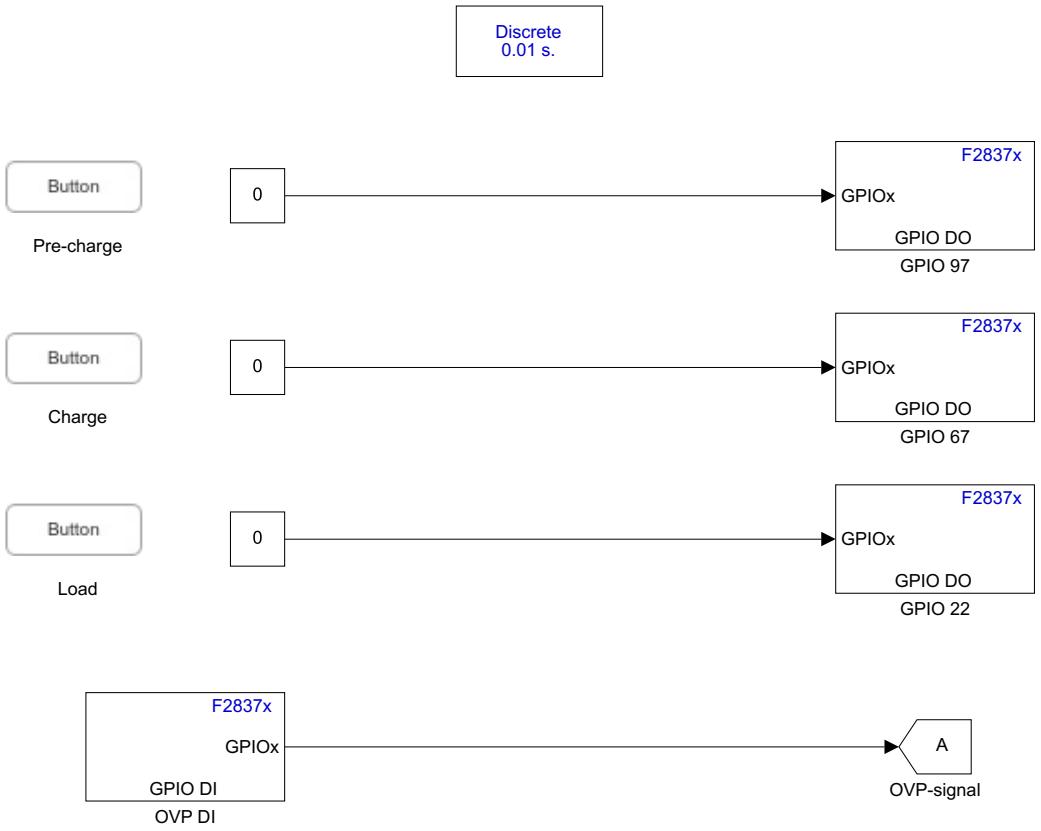
Discharge and Charge/Precharge is to be operated only one at a time. The other one should be commented out.



Control of the Charge and Pre-charge circuit.



C.3 Physical Supercapacitor Module GPIO Control for the TMS320F28379D LaunchPad



D Parameters

D.1 Dual Active Bridge

D.1.1 Supercapacitor Block Parameters

Supercapacitor Block	
Name	**Value**
Rated Capacitance	5 F
ESR DC	230.3 mΩ
Rated Voltage	180 V
Series Capacitors	72
Parallel Capacitors	1
Operation Temperature	25 °C

Simscape Library Path: Simscape / Electrical / Specialized Power Systems / Electric Drives / Extra Sources

D.1.2 MOSFET Block Parameters [65]

MOSFET Block	
Name	**Value**
FET resistance Ron	0.027 Ω
Internal diode inductance Lon	0 H
Internal diode resistance Rd	0.005 Ω
Internal diode forward voltage Vf	2 V
Snubber resistance Rs	10 kΩ
Snubber capacitance Cs	inf F

Simscape Library Path: Simscape / Electrical / Specialized Power Systems / Fundamental Blocks / Power Electronics

D.1.3 Linear Transformer Block Parameters

Linear Transformer Block	
Name	**Value**
Nominal Power Pn	2000 W
Frequency fn	250 kHz
Winding 1 Voltage V1	180 V
Winding 1 Resistance R1	0.0324 Ω
Winding 1 Inductance L1	0.825 µH
Winding 2 Voltage V2	340 V
Winding 2 Resistance R2	0.1156 Ω
Winding 2 Inductance L2	2.9438 µH
Magnetization Resistance Rm	8100 Ω
Magnetization Inductance Lm	0.0051565 H
Turn Ratio	9:17

Simscape Library Path: Simscape / Electrical / Specialized Power Systems / Fundamental Blocks / Elements

D.2 Supercapacitor

Maxwell Supercapacitor cell [31] **Ref: BCAP0360P270S18**	
Name	**Value**
Rated Capacitance	360 F
Capacitance Tolerance Min/Max	0 / 20%
ESR DC Average/Max	2.9/3.2 mΩ
Rated Voltage	2.7 V
Maximum Leakage Current	0.75 mA
Maximum Stored Energy	0.36 Wh
Usable Specific Power	3.8 kW/kg

E Matlab® Source Code

E.1 Dual Active Bridge

E.1.1 Initializing Code for Variables Related to the Simulation

```
%Standard***************
Vref = 340;
Iref = -6.25;
f = 250000;
P = 1/f;
D = 50;
Vsc=180;
Power=2000;
Sample=1e-8;

cycledelay = 2;
Ts = cycledelay/f;
K = 0.03;
R_load=115.8;
L=19.5e-6;

% MOSFET parameters**************
ron_mosfet_pri = 0.03;
ron_mosfet_sec = 0.03;
ron_body_diode_pri = 0.005;
ron_body_diode_sec = 0.005;
vf_body_diode_pri = 4.5;
vf_body_diode_sec = 4.5;
}
```

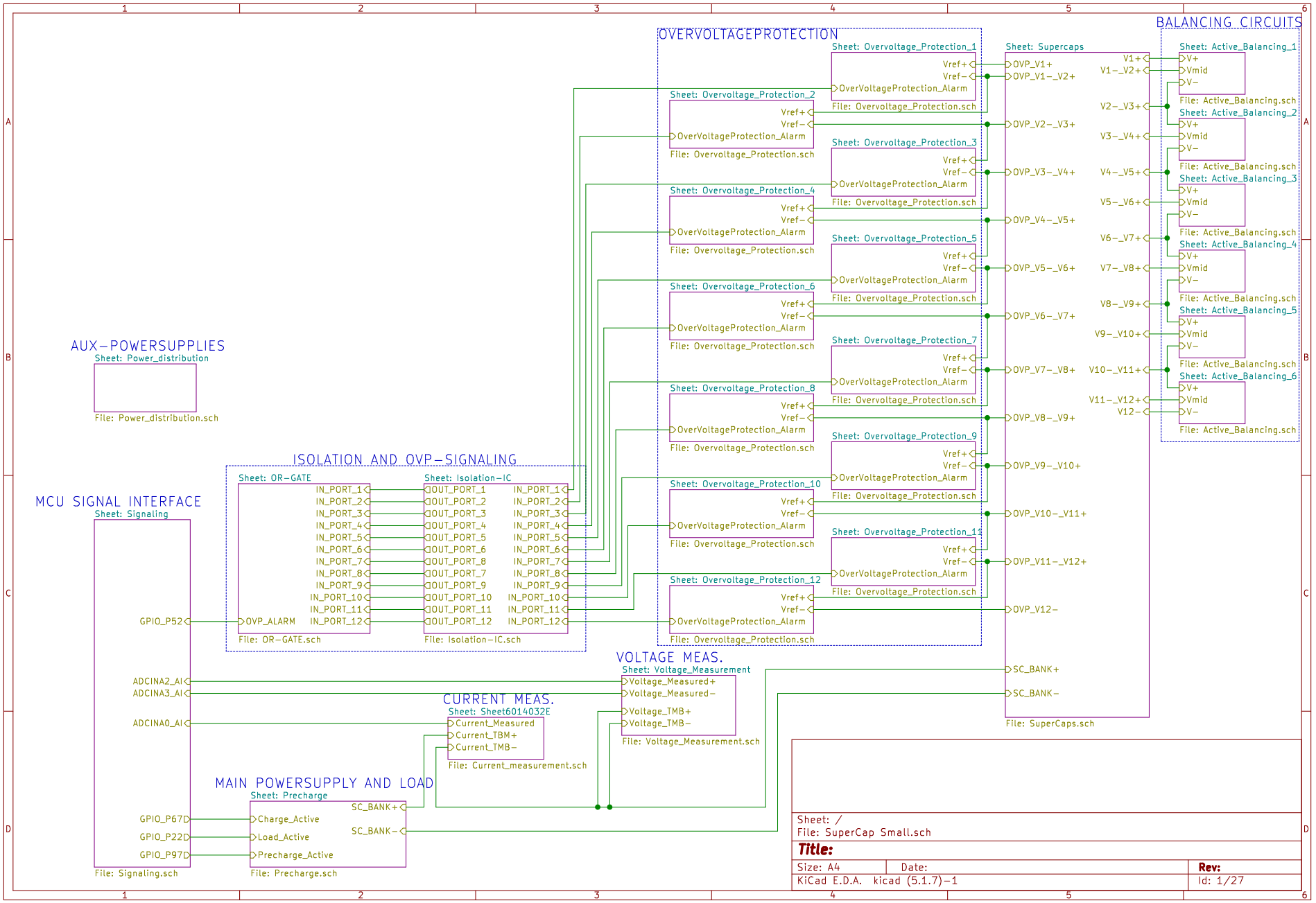
E.2 Supercapacitor

E.2.1 Code for the Power/Phase-shift Graph

```
clc
clear

%This code plots the voltage/power graph
syms L P n V1 V2 F PHI;

n = 340/180;
V1 = 180;
V2 = 340;

F = 250000;
L =28.9e-6;

PHI = linspace(-pi, pi, 110);

figure
hold on

V1 = 180 ;
P = (n/pi*V1*V2*PHI.*(pi-abs(PHI)))/(2*pi*F*L);
plot(PHI,P)

V1 = V1 -30 ;
P = (n/pi*V1*V2*PHI.*(pi-abs(PHI)))/(2*pi*F*L);
plot(PHI,P)

V1 = V1 -30 ;
P = (n/pi*V1*V2*PHI.*(pi-abs(PHI)))/(2*pi*F*L);
plot(PHI,P)

V1 = V1 -30 ;
P = (n/pi*V1*V2*PHI.*(pi-abs(PHI)))/(2*pi*F*L);
plot(PHI,P)

xlabel('Phase Shift')
ylabel('Power')
title('Phase shift')
legend('V1=180','V1=150','V1=120','V1=90', 'Location', 'best')
```

F Integrated Supercapacitor System Design

F.1 Supercapacitor Circuit Diagram


OVERVOLTAGEPROTECTION
BALANCING CIRCUITS
AUX−POWERSUPPLIES
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ISOLATION AND OVP−SIGNALING
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MCU SIGNAL INTERFACE
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CURRENT MEAS.
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MAIN POWERSUPPLY AND LOAD
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Sheet: Overvoltage_Protection_4
Sheet: Overvoltage_Protection_5
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Sheet: Overvoltage_Protection_9
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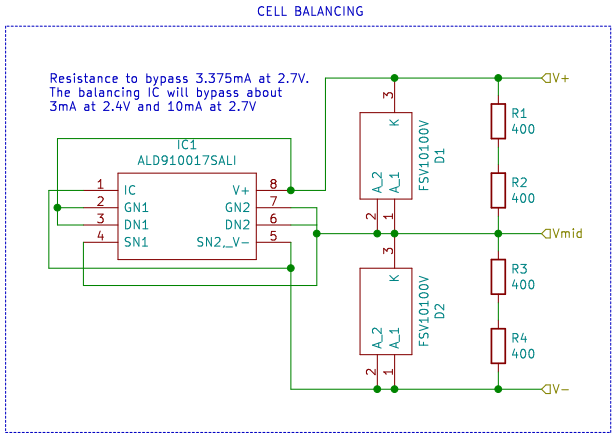
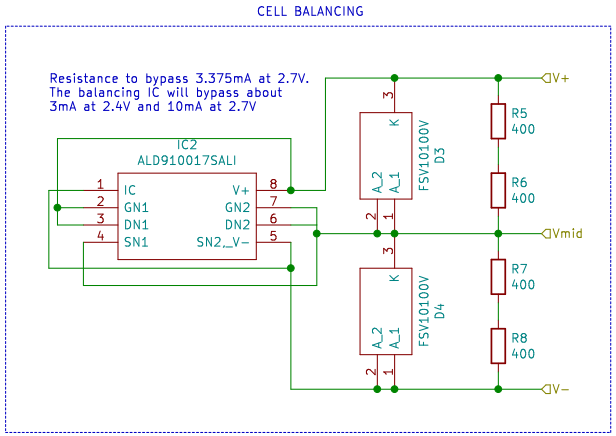
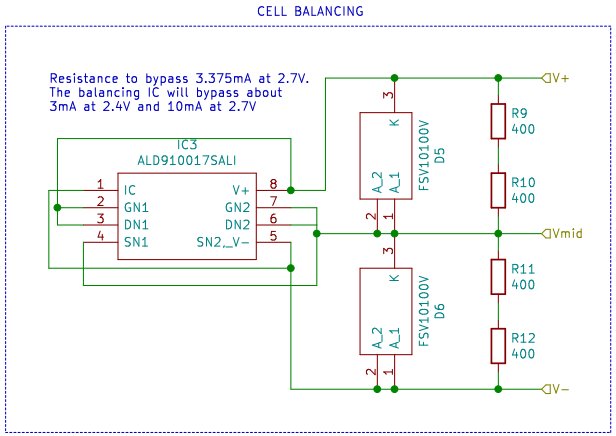
Sheet: Active_Balancing_2
Sheet: Active_Balancing_3
Sheet: Active_Balancing_4
Sheet: Active_Balancing_5
Sheet: Active_Balancing_6
File: Active_Balancing.sch
Sheet: /
File: SuperCap Small.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.7)−1
Id: 1/27



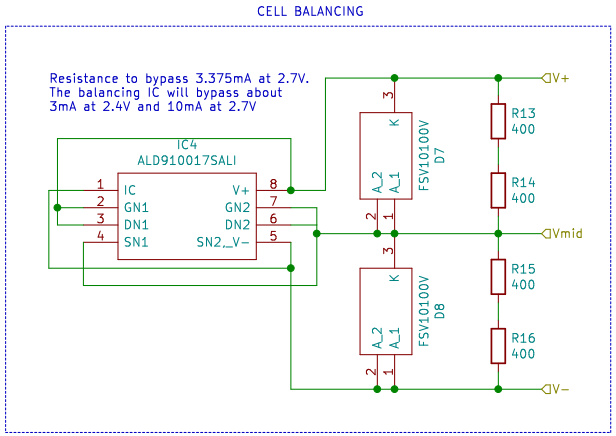
Sheet: /Active_Balancing_1/		
File: Active_Balancing.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)−1		Id: 2/27



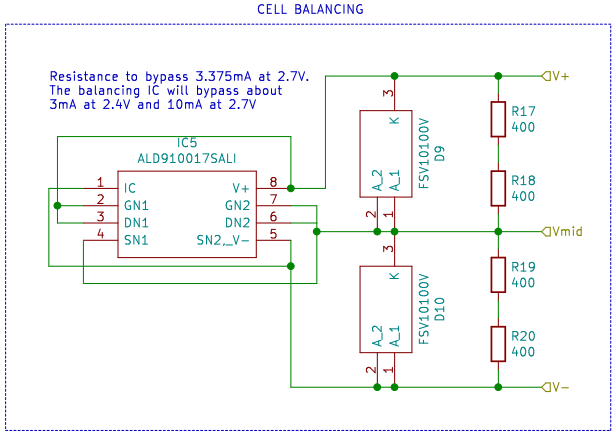
Sheet: /Active_Balancing_2/		
File: Active_Balancing.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)−1		Id: 3/27



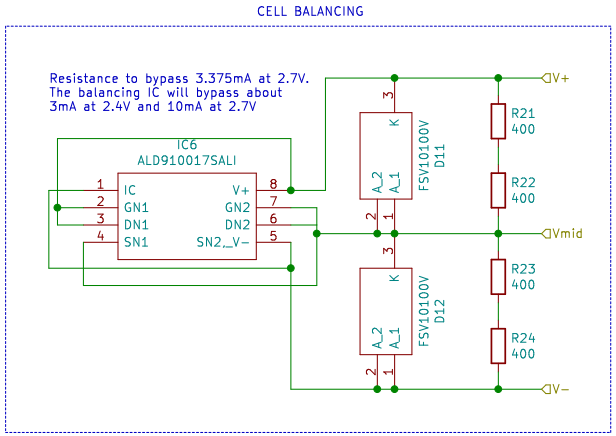
Sheet: /Active_Balancing_3/		
File: Active_Balancing.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 4/27



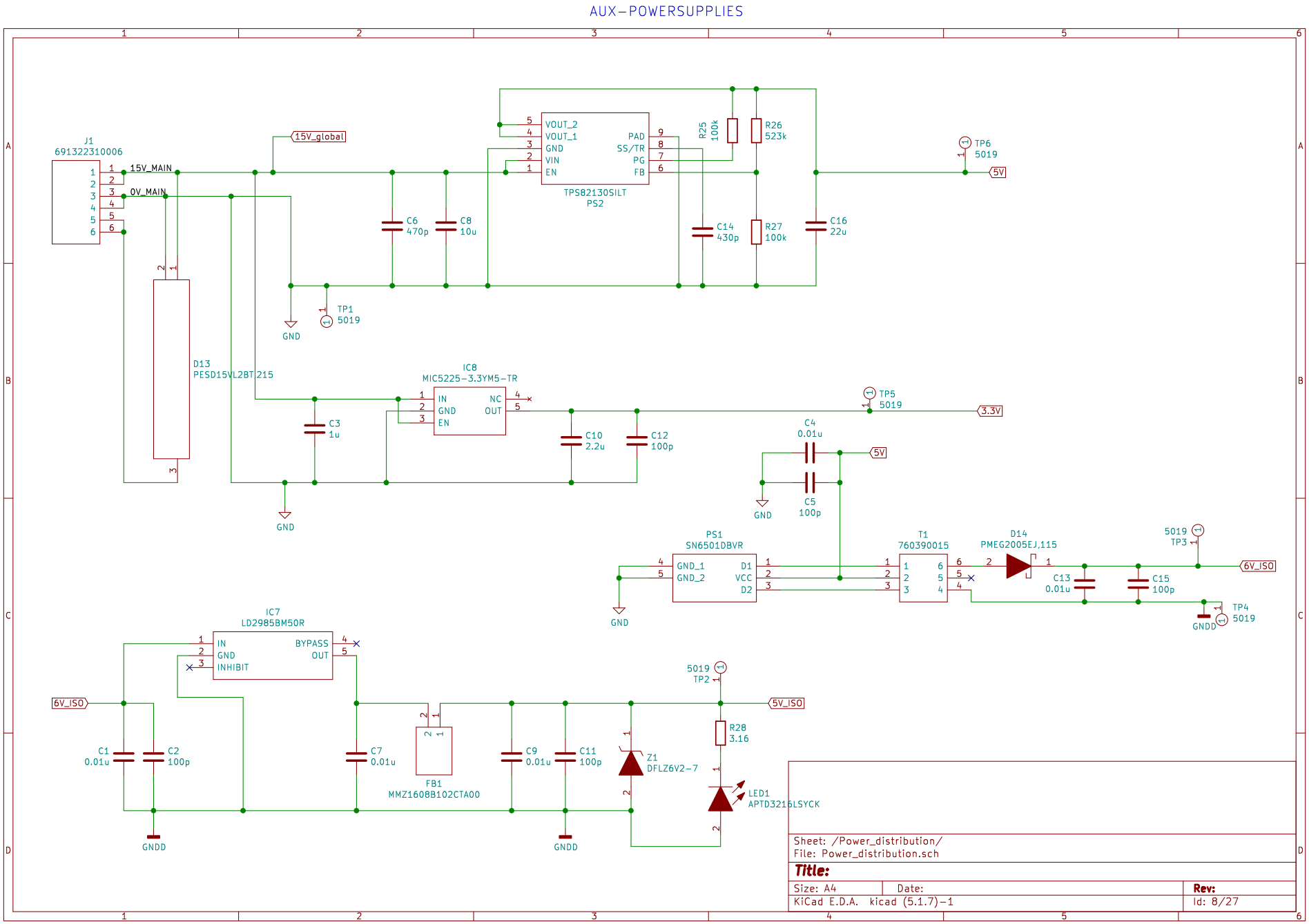
Sheet: /Active_Balancing_6/		
File: Active_Balancing.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)−1		Id: 5/27

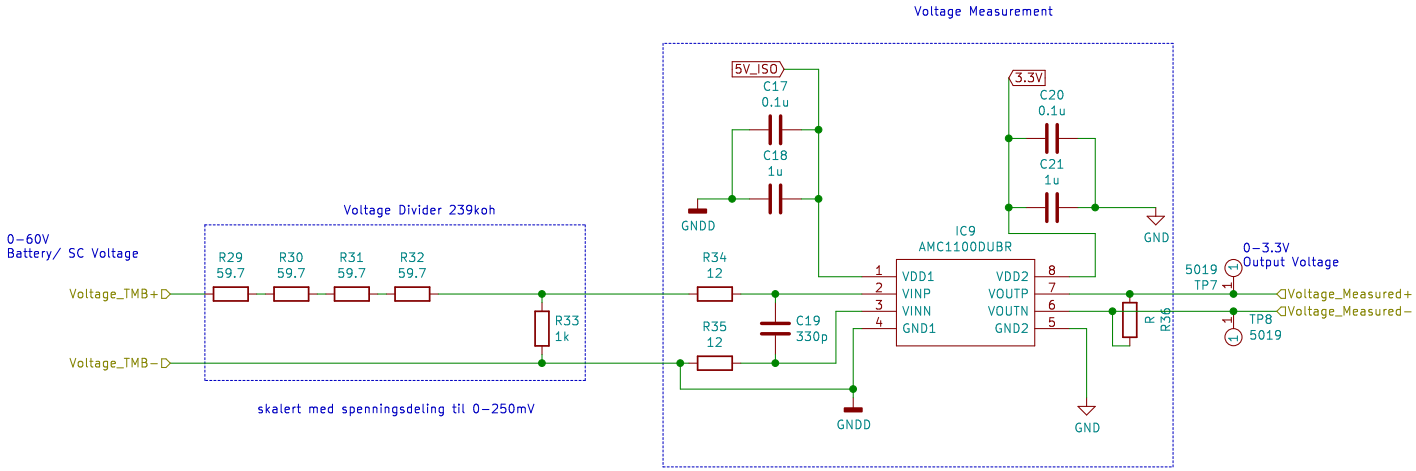


Sheet: /Active_Balancing_5/		
File: Active_Balancing.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 6/27

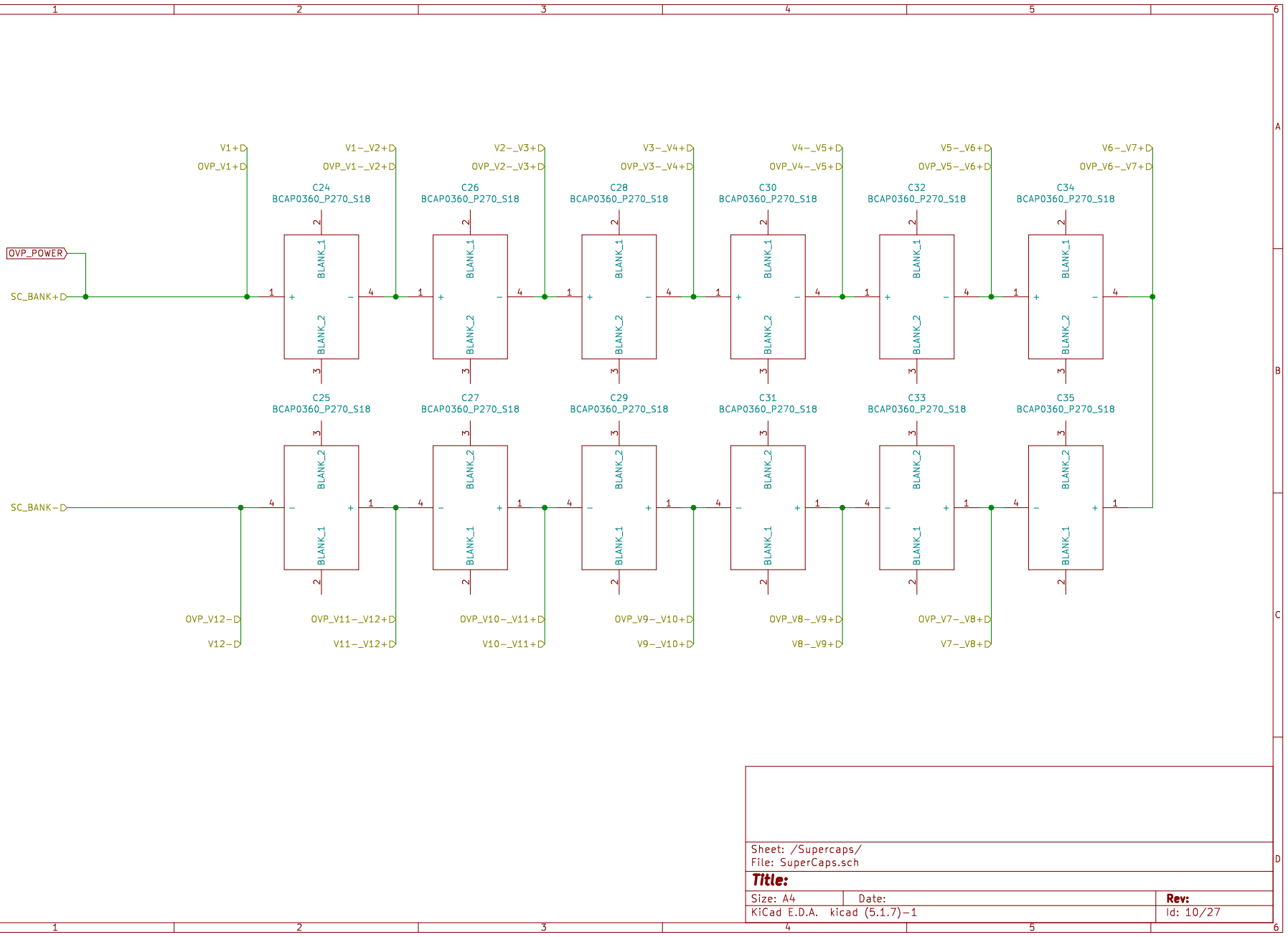


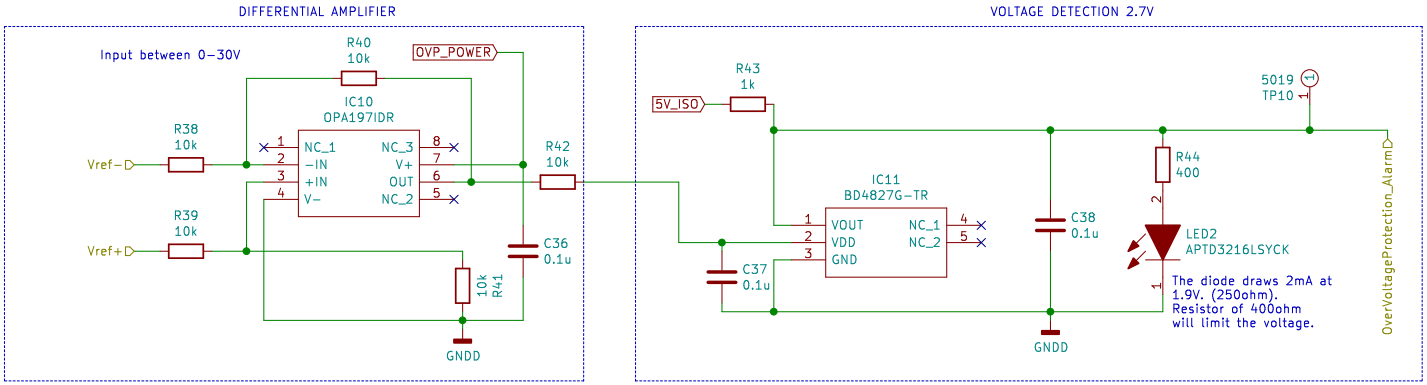
Sheet: /Active_Balancing_4/		
File: Active_Balancing.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)−1		Id: 7/27


AUX—POWERSUPPLIES
J1
691322310006
15V_MAIN
0V_MAIN
15V_global
TPS82130SILT
PS2
VOUT_2
VOUT_1
GND
VIN
EN
PAD
SS/TR
PG
FB
R25
100k
R26
523k
R27
100k
C6
470p
C8
10u
C14
430p
C16
22u
TP6
5019
5V
TP1
5019
GND
D13
PESD15VL2BT,215
IC8
MIC5225—3.3YM5—TR
IN
GND
EN
NC
OUT
C3
1u
C10
2.2u
C12
100p
TP5
5019
3.3V
C4
0.01u
C5
100p
5V
GND
PS1
SN6501DBVR
GND_1
GND_2
D1
VCC
D2
T1
760390015
D14
PMEG2005EJ,115
C13
0.01u
C15
100p
5019
TP3
6V_ISO
TP4
5019
GNDD
IC7
LD2985BM50R
IN
GND
INHIBIT
BYPASS
OUT
6V_ISO
C1
0.01u
C2
100p
C7
0.01u
FB1
MMZ1608B102CTA00
C9
0.01u
C11
100p
Z1
DFLZ6V2—7
5019
TP2
5V_ISO
R28
3.16
LED1
APTD3216LSYCK
GNDD
Sheet: /Power_distribution/
File: Power_distribution.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.7)—1
Id: 8/27



Sheet: /Voltage_Measurement/		
File: Voltage_Measurement.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)–1		Id: 9/27


V1+
OVP_V1+
V1-_V2+
OVP_V1-_V2+
V2-_V3+
OVP_V2-_V3+
V3-_V4+
OVP_V3-_V4+
V4-_V5+
OVP_V4-_V5+
V5-_V6+
OVP_V5-_V6+
V6-_V7+
OVP_V6-_V7+
C24
BCAP0360_P270_S18
C26
BCAP0360_P270_S18
C28
BCAP0360_P270_S18
C30
BCAP0360_P270_S18
C32
BCAP0360_P270_S18
C34
BCAP0360_P270_S18
OVP_POWER
SC_BANK+
BLANK_1
BLANK_2
C25
BCAP0360_P270_S18
C27
BCAP0360_P270_S18
C29
BCAP0360_P270_S18
C31
BCAP0360_P270_S18
C33
BCAP0360_P270_S18
C35
BCAP0360_P270_S18
SC_BANK-
OVP_V12-
V12-
OVP_V11-_V12+
V11-_V12+
OVP_V10-_V11+
V10-_V11+
OVP_V9-_V10+
V9-_V10+
OVP_V8-_V9+
V8-_V9+
OVP_V7-_V8+
V7-_V8+
Sheet: /Supercaps/
File: SuperCaps.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.7)-1
Id: 10/27

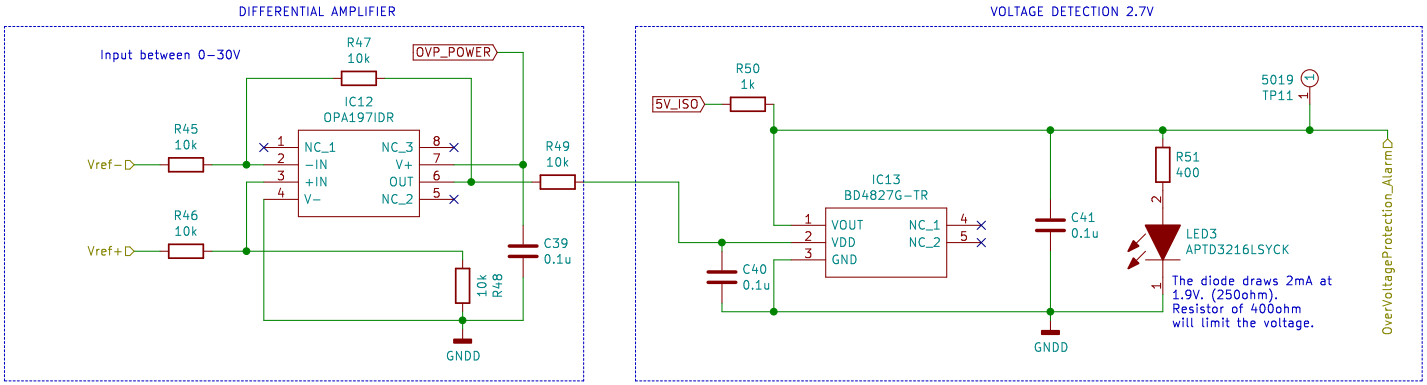


Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_12/
File: Overvoltage_Protection.sch

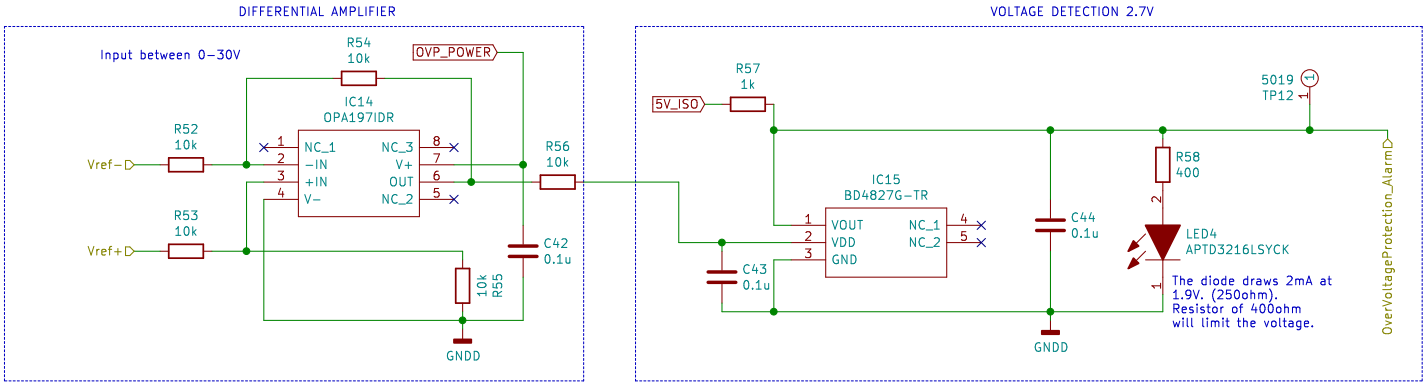
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 11/27



Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_11/		
File: Overvoltage_Protection.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 12/27

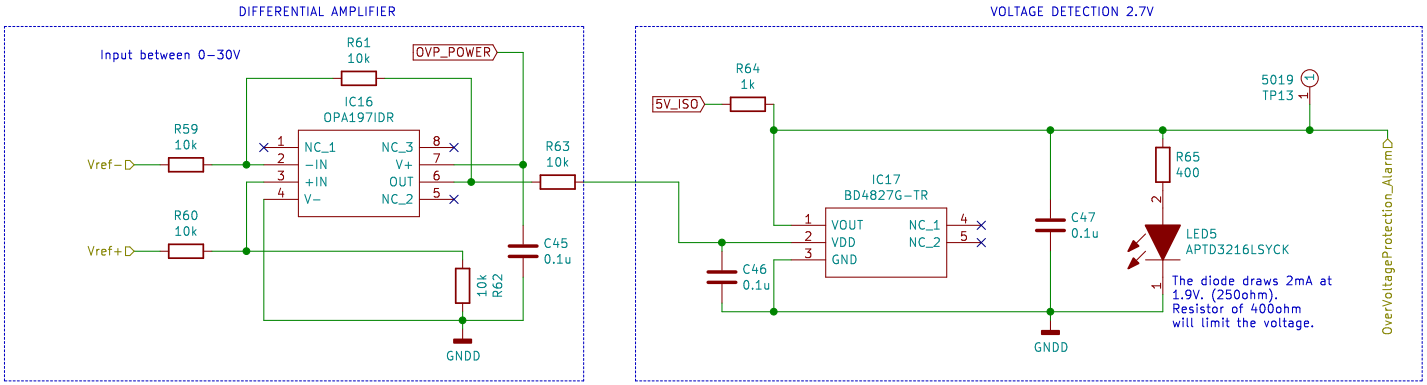


Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_10/
File: Overvoltage_Protection.sch

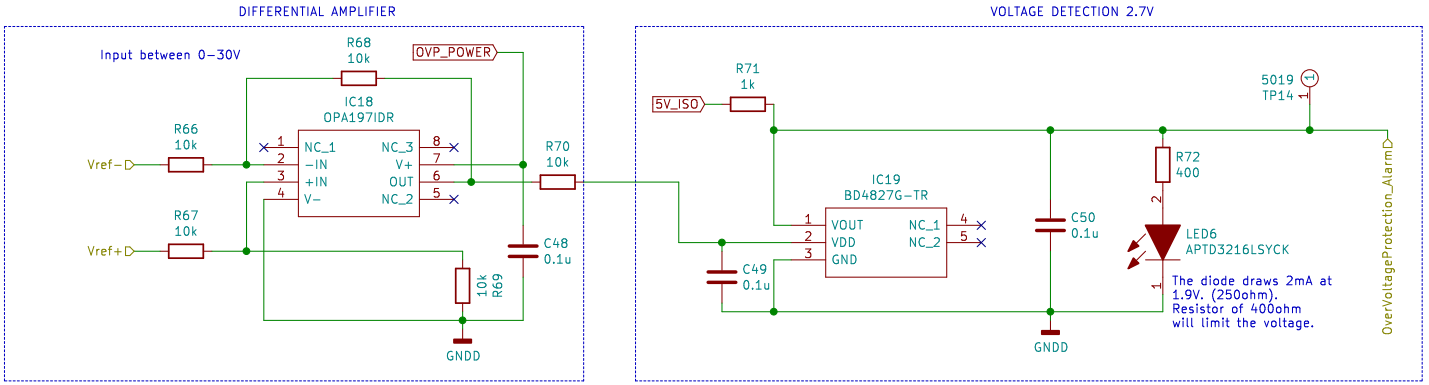
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 13/27



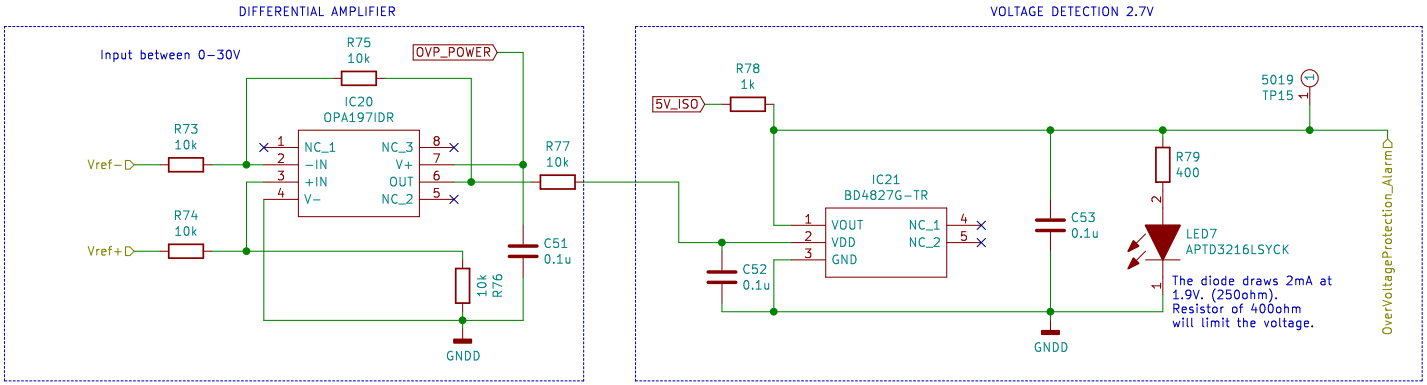
Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_9/		
File: Overvoltage_Protection.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 14/27



Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_8/		
File: Overvoltage_Protection.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 15/27

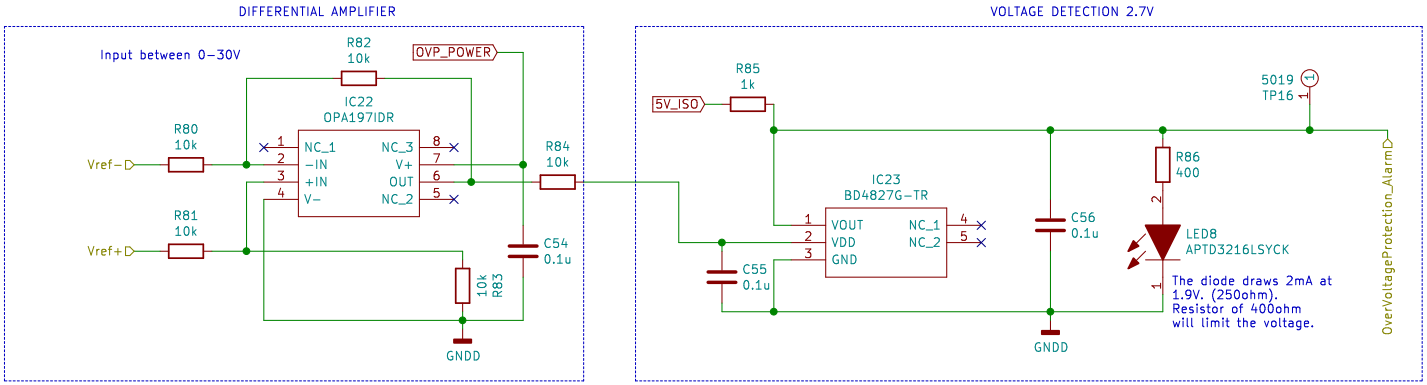


Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_6/
File: Overvoltage_Protection.sch

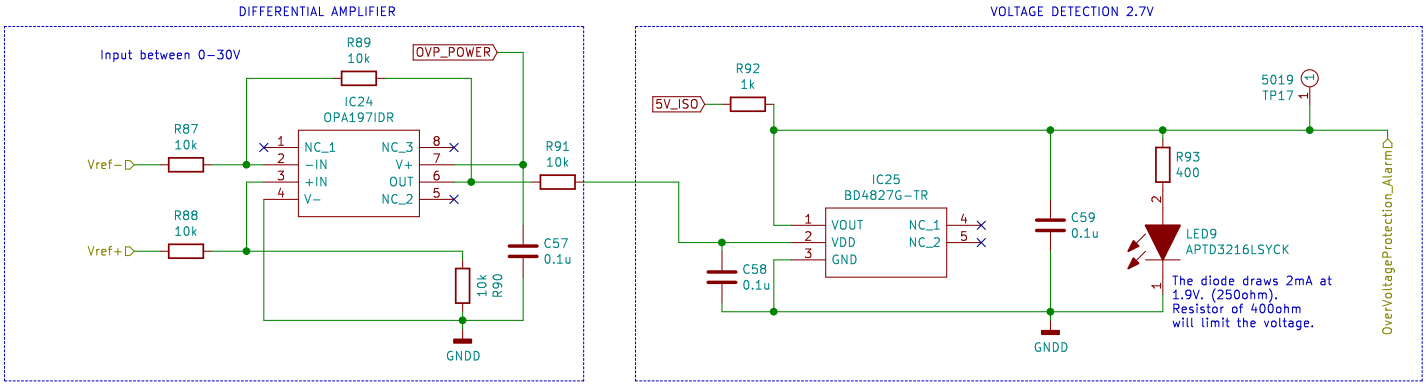
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 16/27



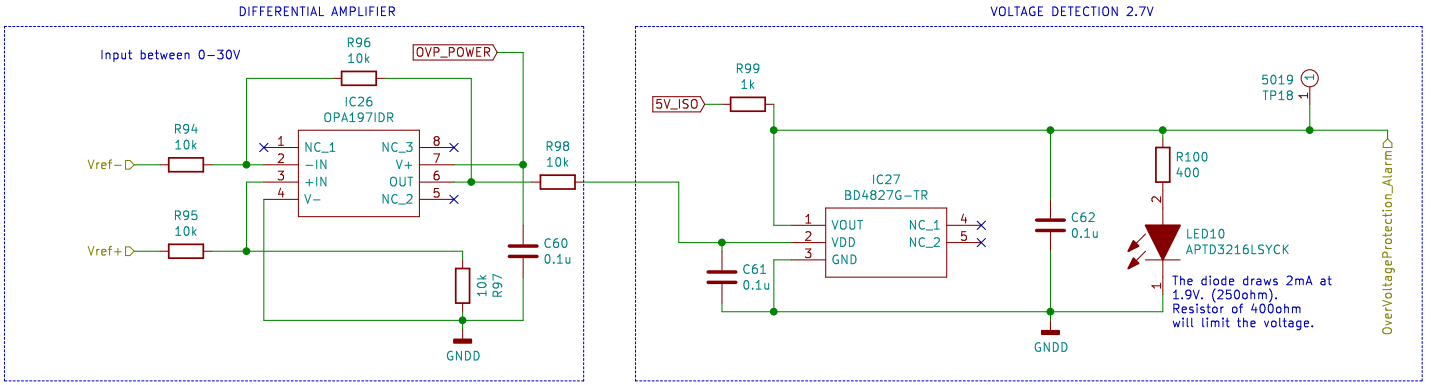
Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_4/		
File: Overvoltage_Protection.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 17/27



Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_2/		
File: Overvoltage_Protection.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 18/27

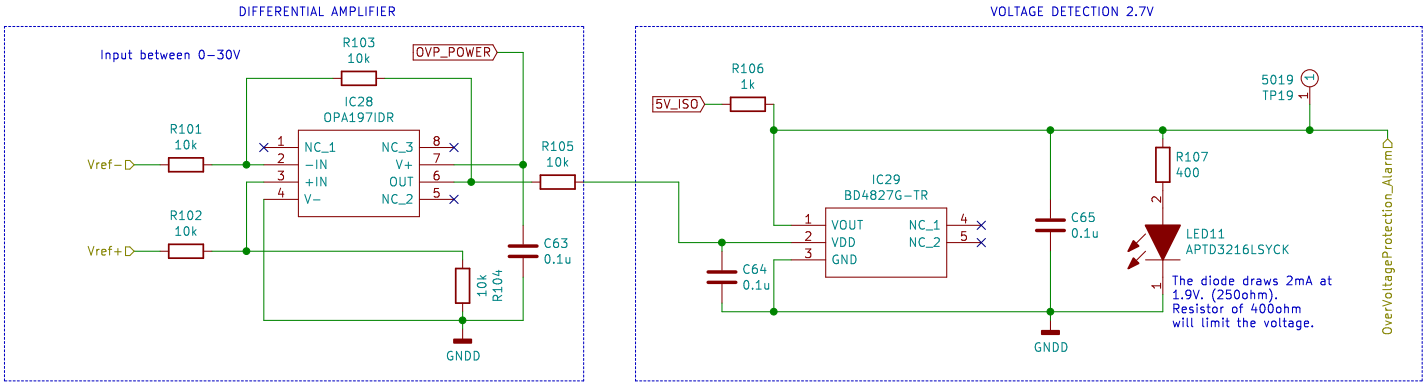


Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_7/
File: Overvoltage_Protection.sch

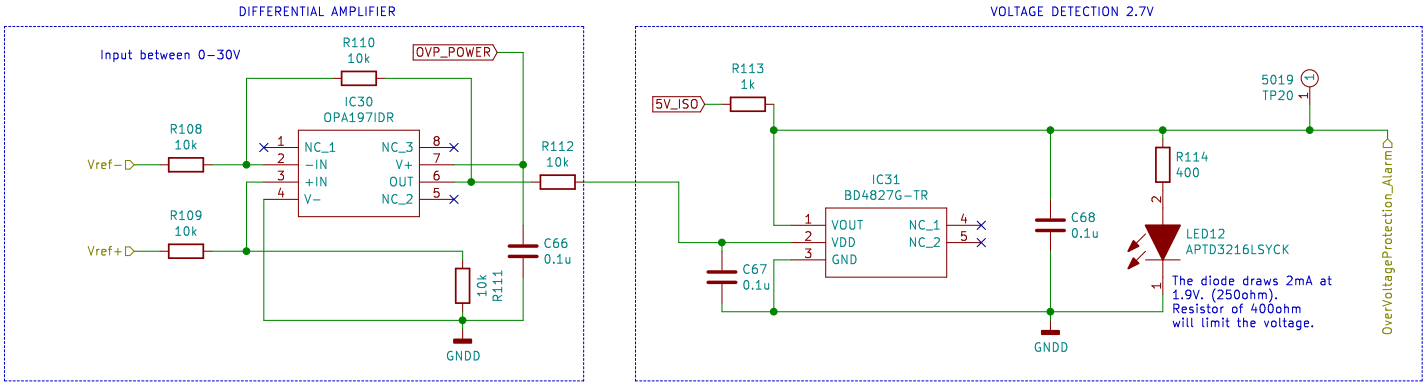
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 19/27



Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_5/		
File: Overvoltage_Protection.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 20/27

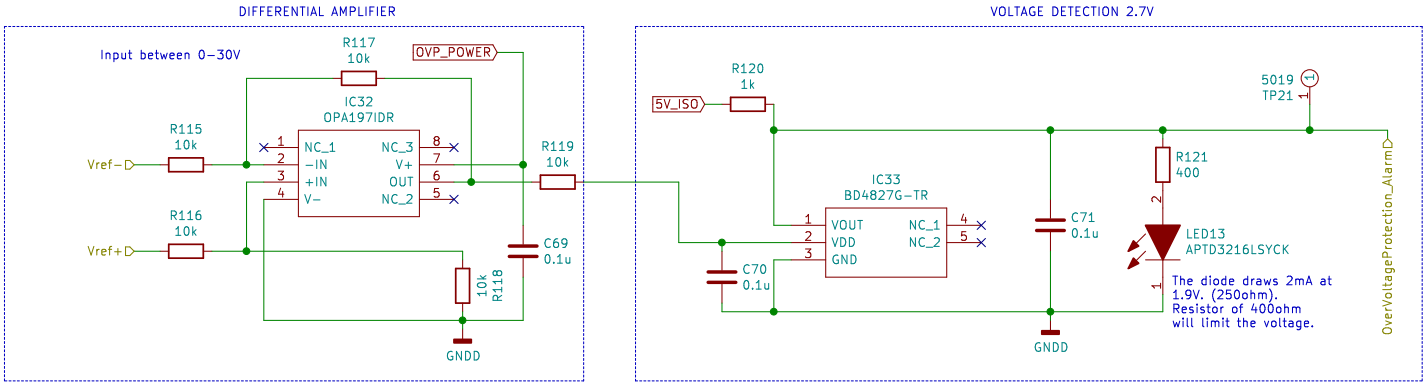


Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

Sheet: /Overvoltage_Protection_1/
File: Overvoltage_Protection.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 21/27

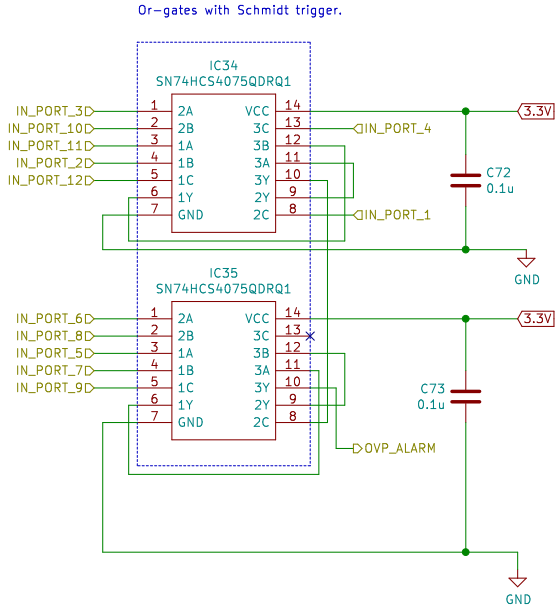


Rev 1.1: Pull-up resistor changed to 47kohm.
Removed schotky diode.
Removed diode circuit.

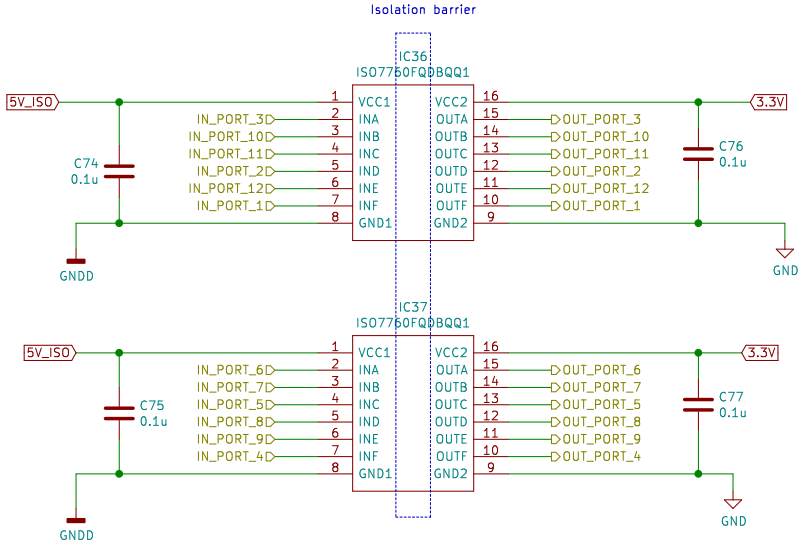
Sheet: /Overvoltage_Protection_3/
File: Overvoltage_Protection.sch

Title:

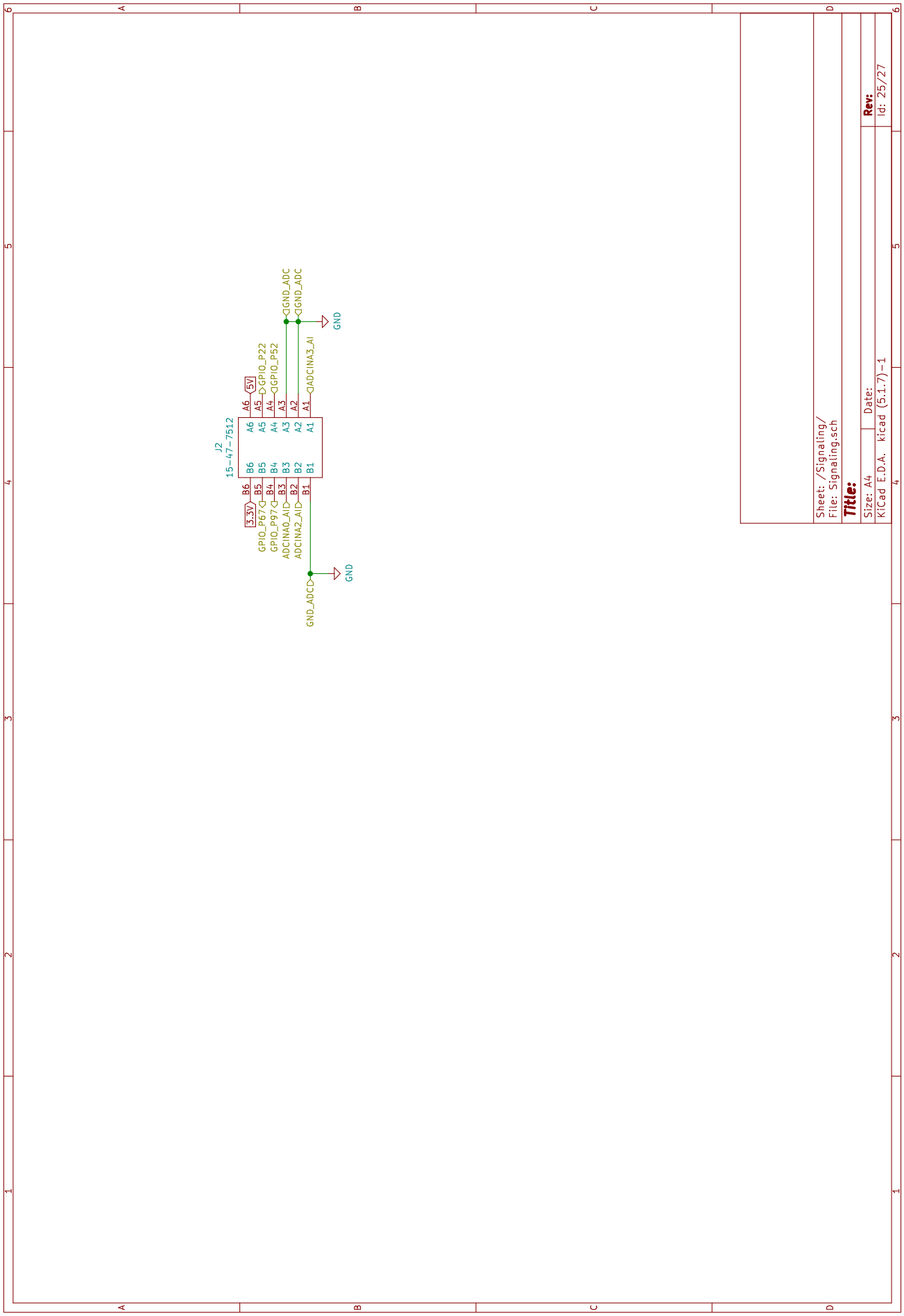
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 22/27

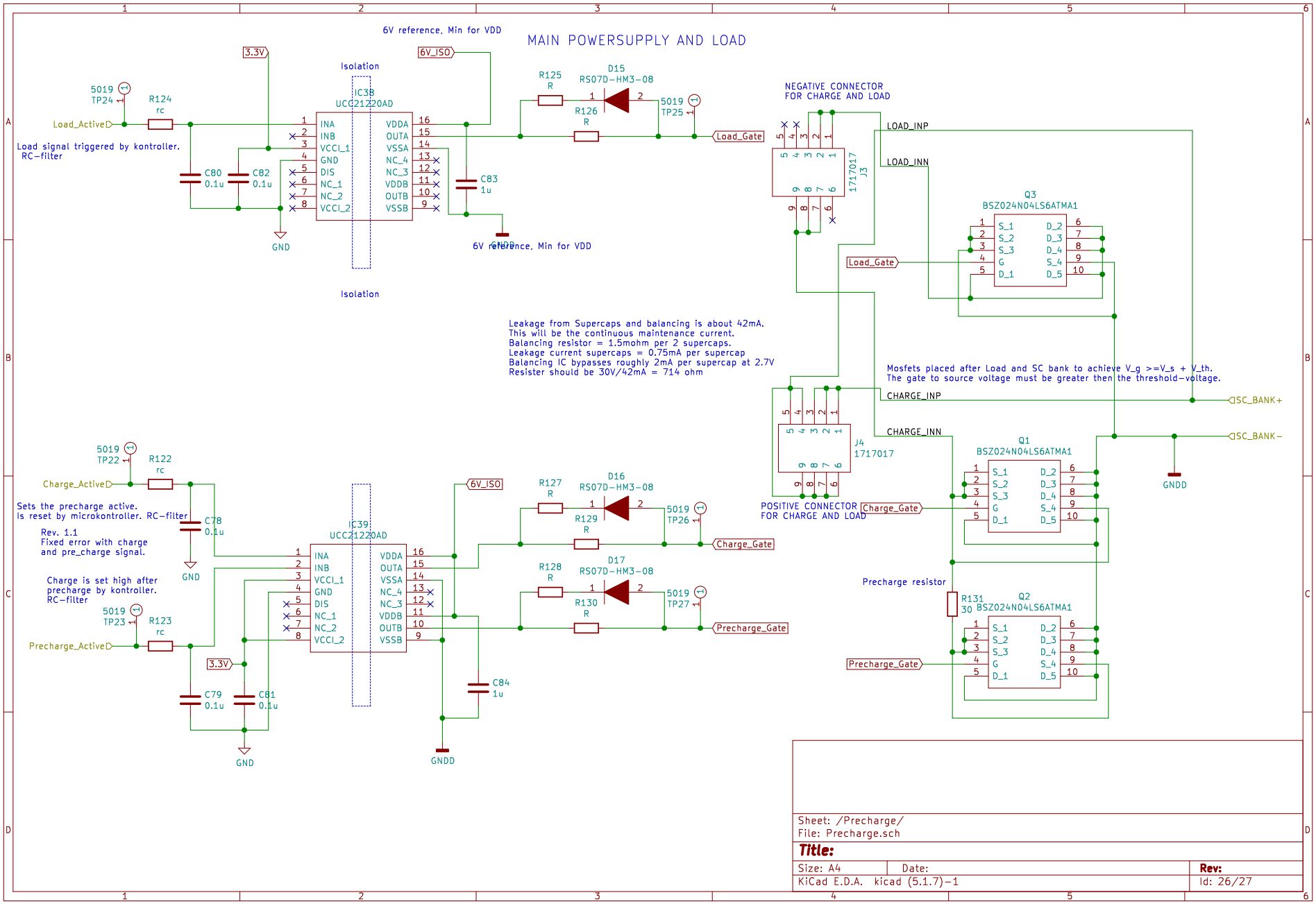


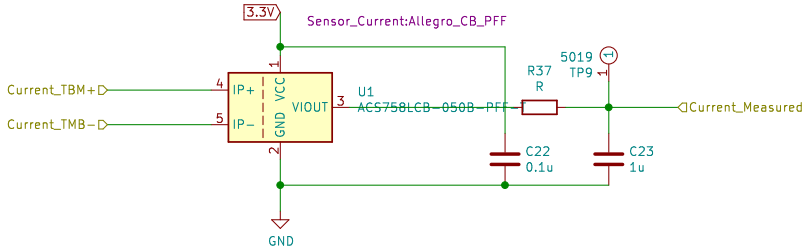
Sheet: /OR-GATE/		
File: OR-GATE.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 23/27



Sheet: /Isolation-IC/		
File: Isolation-IC.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 24/27


J2
15-47-7512
A6
A5
A4
A3
A2
A1
B6
B5
B4
B3
B2
B1
5V
GPIO_P22
GPIO_P52
ADCINA3_AI
GND_ADC
GND
3.3V
GPIO_P67
GPIO_P97
ADCINA0_AI
ADCINA2_AI
GND_ADCD
Sheet: /Signaling/
File: Signaling.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.7)-1
Id: 25/27

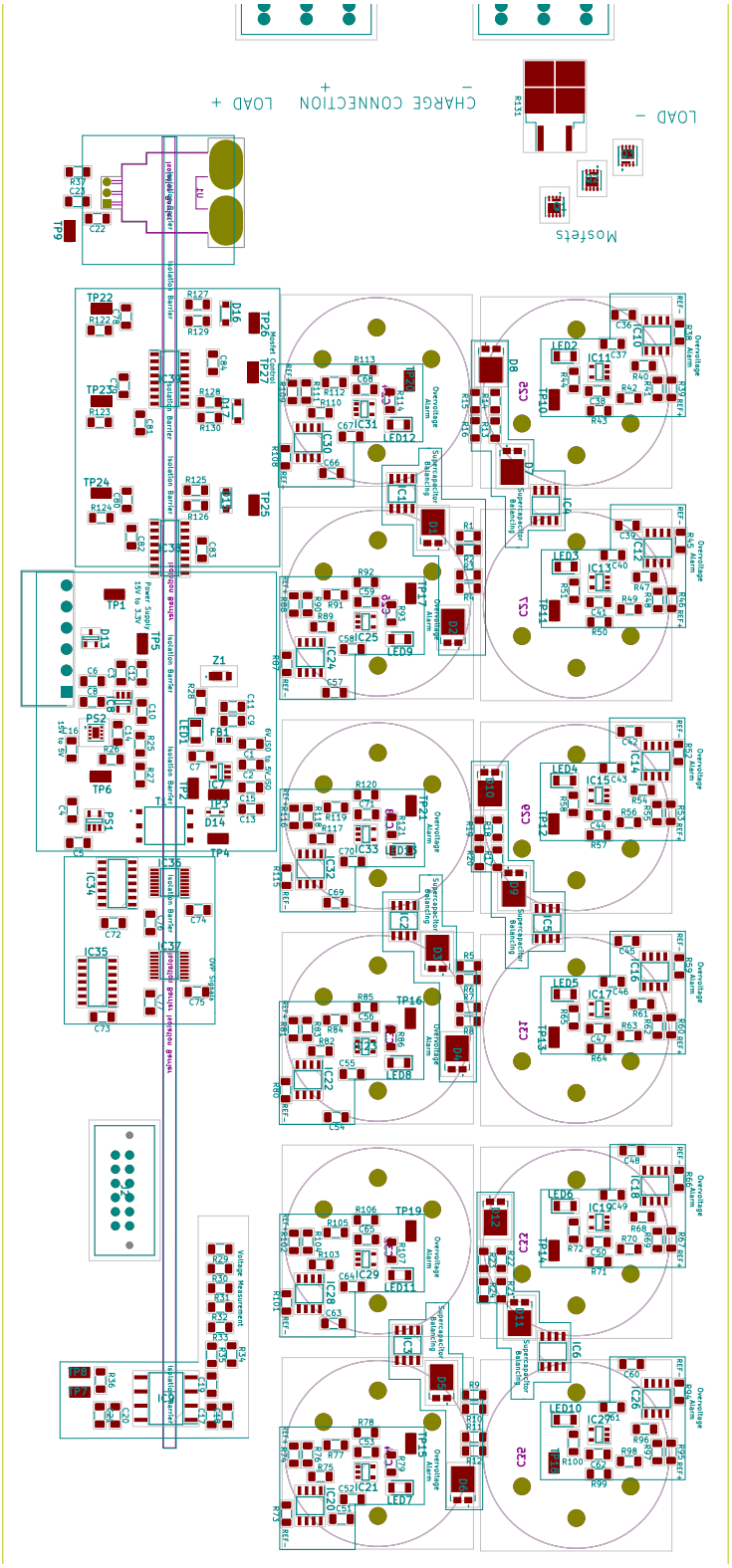

MAIN POWERSUPPLY AND LOAD
6V reference, Min for VDD
3.3V
6V_ISO
Isolation
IC38
UCC21220AD
INA
INB
VCCI_1
GND
DIS
NC_1
NC_2
VCCI_2
VDDA
OUTA
VSSA
NC_4
NC_3
VDDB
OUTB
VSSB
5019
TP24
R124
rc
Load_Active
Load signal triggered by kontroller.
RC-filter
C80
0.1u
C82
0.1u
C83
1u
GND
GNDD
R125
R
D15
RS07D-HM3-08
R126
R
5019
TP25
Load_Gate
NEGATIVE CONNECTOR
FOR CHARGE AND LOAD
1717017
J3
LOAD_INP
LOAD_INN
Q3
BSZ024N04LS6ATMA1
S_1
S_2
S_3
G
D_1
D_2
D_3
D_4
S_4
D_5
Leakage from Supercaps and balancing is about 42mA.
This will be the continuous maintenance current.
Balancing resistor = 1.5mohm per 2 supercaps.
Leakage current supercaps = 0.75mA per supercap
Balancing IC bypasses roughly 2mA per supercap at 2.7V
Resister should be 30V/42mA = 714 ohm
Mosfets placed after Load and SC bank to achieve V_g >=V_s + V_th.
The gate to source voltage must be greater then the threshold-voltage.
CHARGE_INP
CHARGE_INN
SC_BANK+
SC_BANK-
J4
1717017
Q1
BSZ024N04LS6ATMA1
POSITIVE CONNECTOR
FOR CHARGE AND LOAD
Charge_Gate
Precharge resistor
R131
30
Q2
BSZ024N04LS6ATMA1
Precharge_Gate
5019
TP22
R122
rc
Charge_Active
Sets the precharge active.
Is reset by microkontroller. RC-filter
Rev. 1.1
Fixed error with charge
and pre_charge signal.
C78
0.1u
IC39
UCC21220AD
R127
R
D16
RS07D-HM3-08
R129
R
5019
TP26
R128
R
D17
RS07D-HM3-08
R130
R
5019
TP27
Charge is set high after
precharge by kontroller.
RC-filter
5019
TP23
R123
rc
Precharge_Active
C79
0.1u
C81
0.1u
C84
1u
Sheet: /Precharge/
File: Precharge.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.7)-1
Id: 26/27



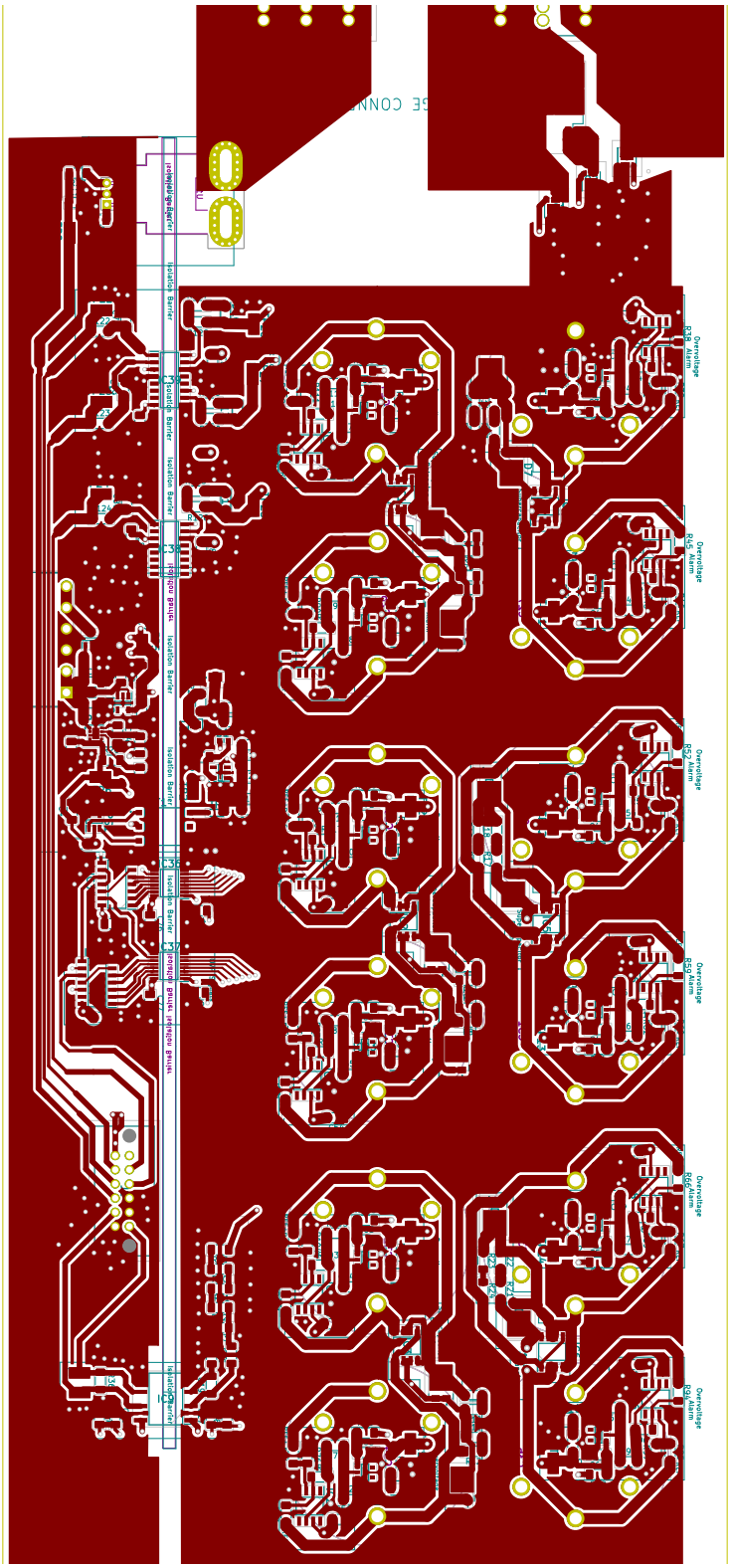
Sheet: /Sheet6014032E/		
File: Current_measurement.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.7)-1		Id: 27/27

F.2 Component Layout

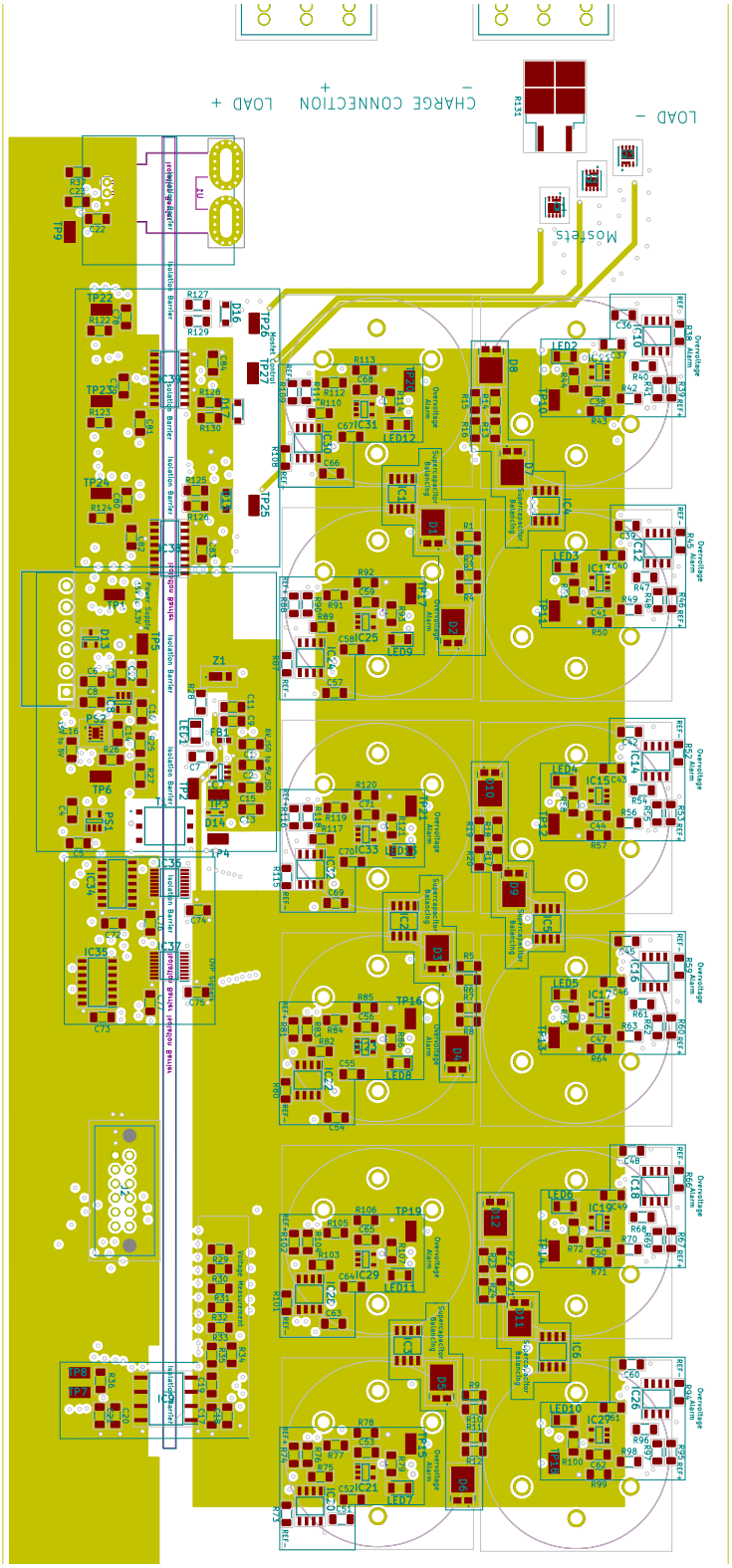
;



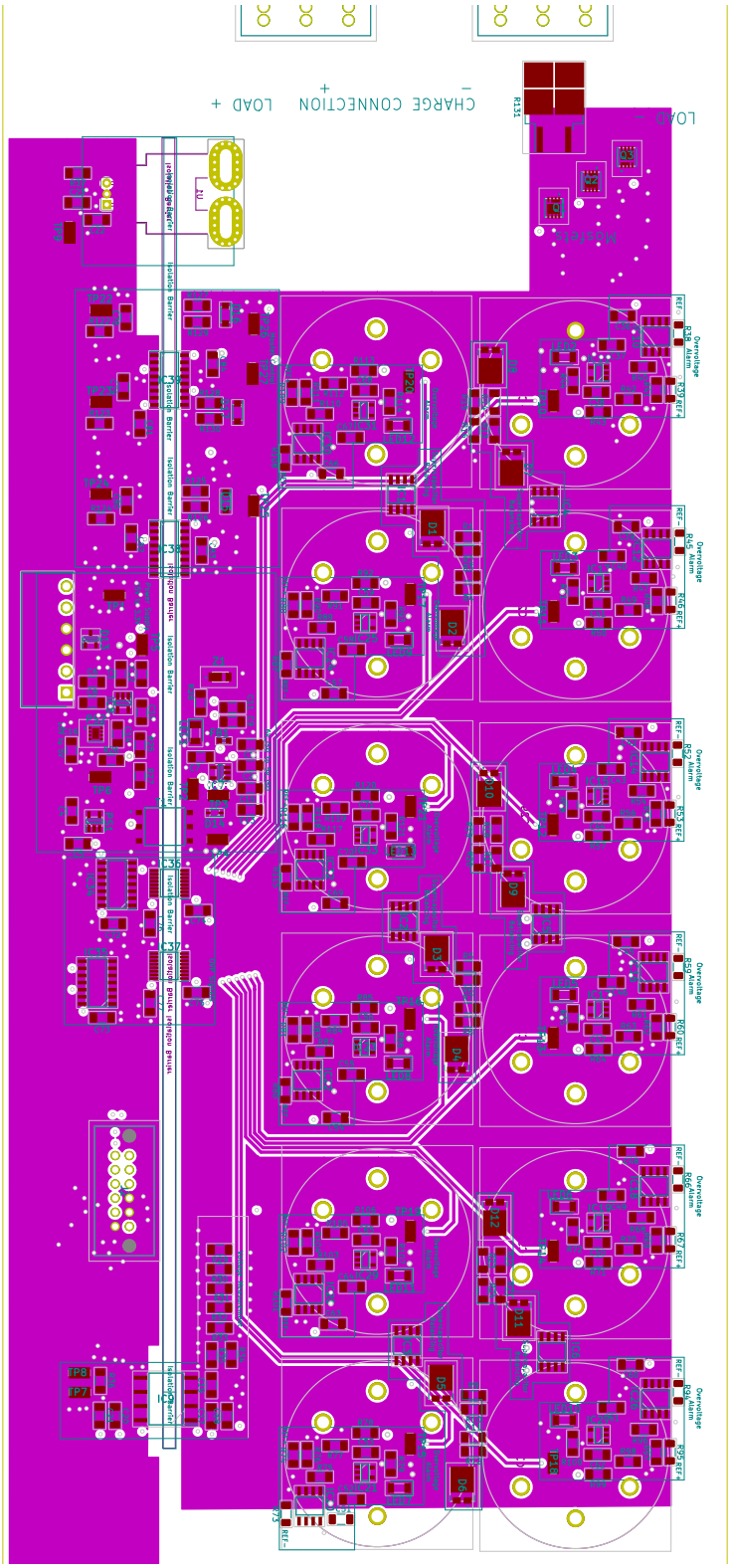
F.3 Top Copper Layer



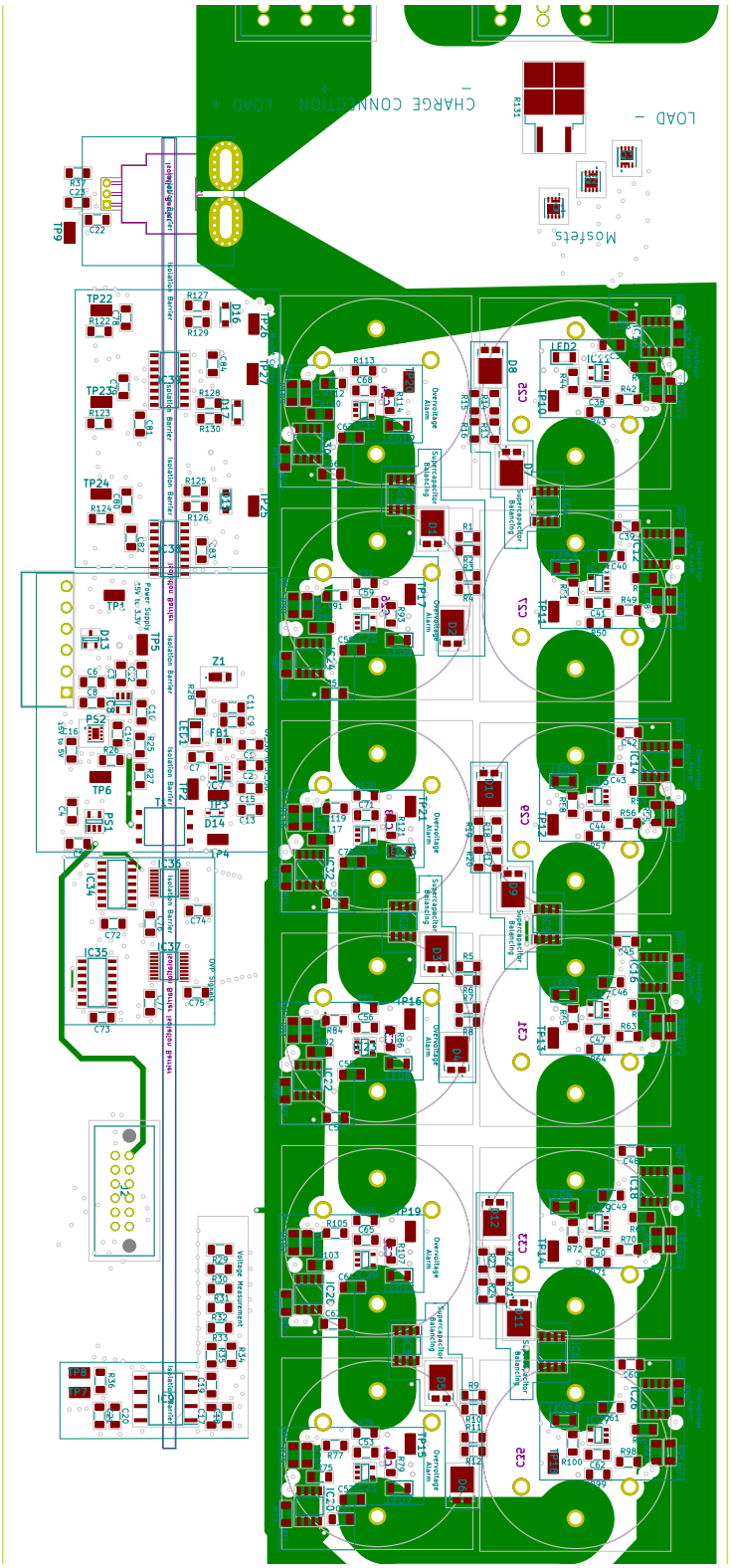
F.4 Top Middle Copper Layer



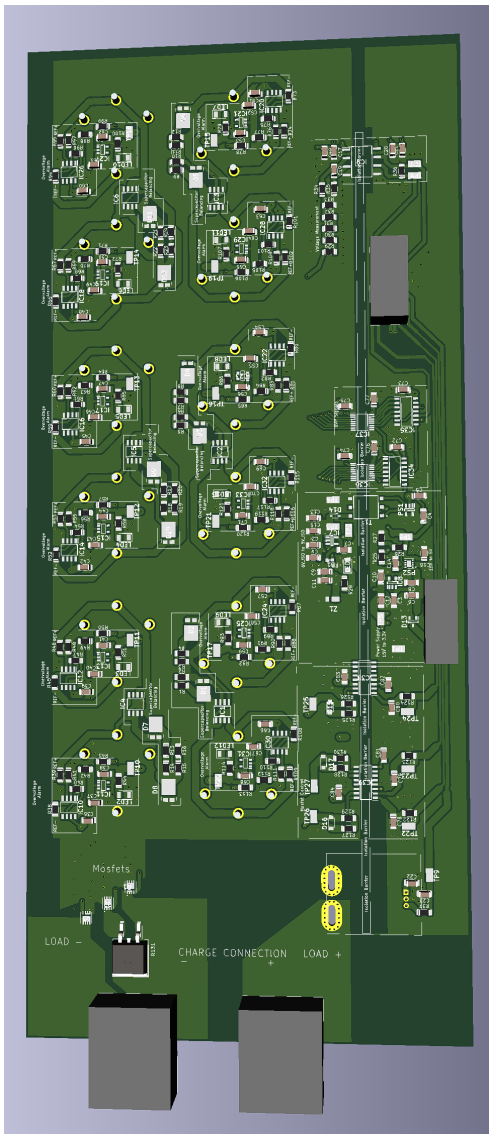
F.5 Bottom Middle Copper Layer

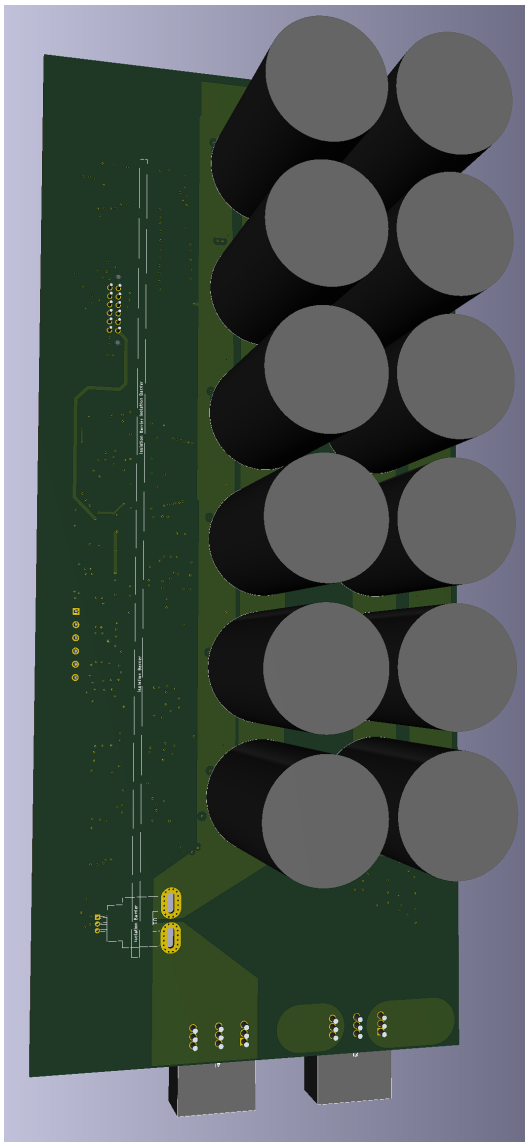


F.6 Bottom Copper Layer



F.7 3D Diagram





G Supercapacitor Module Component List (Mouser)

SUPERCAP MODULE PROJECT

Mouser No	Mfr. No	Manufacturer
621-DFLZ6V2-7	DFLZ6V2-7	Diodes Incorporated
710-760390015	760390015	Wurth Elektronik
71-RCS120651R0FKEA	RCS120651R0FKEA	Vishay
660-RN73H2TD1001B10	RN73H2BTTD1001B10	KOA Speer
667-ERA-8AEB5233V	ERA-8AEB5233V	Panasonic
660-RN73R2BTD1003B25	RN73R2BTTD1003B25	KOA Speer
660-RN73H2BTD1002B10	RN73H2BTTD1002B10	KOA Speer
660-RN732BTTD4000B25	RN732BTTD4000B25	KOA Speer
660-RN732BTTD5972B50	RN732BTTD5972B50	KOA Speer
284-AP75025RF	AP750 25R F	Ohmite
603-RT1206BRD0712RL	RT1206BRD0712RL	Yageo
71-CRCW12063R16FKEA	CRCW12063R16FKEA	Vishay
726-BSZ024N04LS6ATMA	BSZ024N04LS6ATMA1	Infineon
595-SN6501DBVR	SN6501DBVR	Texas Instruments
604-APTD3216LSYCK	APTD3216LSYCK	Kingbright
710-691322310006	691322310006	Wurth Elektronik
651-1717017	1717017	Phoenix Contact
538-15-47-7512	15-47-7512	Molex
595-UCC21220AD	UCC21220AD	Texas Instruments
595-SN74HCS4075QDRQ1	SN74HCS4075QDRQ1	Texas Instruments
595-OPA197IDR	OPA197IDR	Texas Instruments
998-MIC5225-3.3YM5TR	MIC5225-3.3YM5-TR	Microchip
511-LD2985BM50	LD2985BM50R	STMicroelectronics
595-ISO7760FQDBQQ1	ISO7760FQDBQQ1	Texas Instruments
755-BD4827G-TR	BD4827G-TR	ROHM Semiconductor
595-AMC1100DUBR	AMC1100DUBR	Texas Instruments
585-ALD910017SALI	ALD910017SALI	Advanced Linear Devices
810-MMZ1608B102CTA00	MMZ1608B102CTA00	TDK
78-RS07D-HM3-08	RS07D-HM3-08	Vishay
771-PMEG2005EJ115	PMEG2005EJ,115	Nexperia
771-PESD15VL2BT-T/R	PESD15VL2BT,215	Nexperia
512-FSV10100V	FSV10100V	ON Semiconductor
723-BCAP0360P270S18	BCAP0360 P270 S18	Maxwell Technologies
80-C1206C226K8R7210	C1206C226K8RAC7210	KEMET
80-C1206C106J3RAUTO	C1206C106J3RACAUTO	KEMET
80-C1206C225J4RECLR	C1206C225J4REC7210	KEMET
80-C1206C105J3R	C1206C105J3RACTU	KEMET

80-C1206C104F5JACTU	C1206C104F5JAC7800	KEMET
80-C1206C103F3GECAUT	C1206C103F3GECAUTO	KEMET
80-C1206C471F5G	C1206C471F5GACTU	KEMET
77-VJ12A100V431J	VJ1206A431JXBAT	Vishay
80-C1206C331F3HACTU	C1206C331F3HACTU	KEMET
581-12063A101FAT2A	12063A101FAT2A	AVX
651-1716922	1716922	Phoenix Contact
910-TS391AX250	TS391AX250	Chip Quik
517-3365/08100	3365/08100	3M
517-3365/12	3365/12-100	3M
517-3365/16-100	3365/16-100	3M

Description

Zener Diodes 1.0W 6.2V
Power Transformers MID-SN6501 TI Driver Toroid .475mH 3.3VDC
Thick Film Resistors - SMD 0.5watt 51ohms 1% 100ppm
Thin Film Resistors - SMD 1K OHM .1% 10PPM
Thin Film Resistors - SMD 1206 523Kohm 25ppm 0.1% AEC-Q200
Thin Film Resistors - SMD 100K ohm 0.1% 25 ppm
Thin Film Resistors - SMD 10K OHM .1% 10PPM 1/4W
Thin Film Resistors - SMD 400Ohm,1206,0.1%,25p pm,125mW,150V
Thin Film Resistors - SMD 1206 59K7 Ohms 0.1% 50PPM
Thick Film Resistors - SMD 25 ohm 1% 50W Power Resistor
Thin Film Resistors - SMD 1/4W 12 ohm .1% 25ppm
Thick Film Resistors - SMD 1/4watt 3.16ohms 1%
MOSFET TRENCH <= 40V
Power Management Specialised - PMIC Transformer Driver for Iso Power Supply
Standard LEDs - SMD 1206 Dome Lens LED Yellow- 590nm
Pluggable Terminal Blocks WR-TBL Terminal block - PCB Header - THT
Pluggable Terminal Blocks PC 6/ 3-G1-7,62 BK
Headers & Wire Housings CGrid VT Shrd Hdr w/Pg TIN 12Ckt
Gate Drivers 4-A/6-A, 3.0-kVRMS dual-channel isolated gate driver with 5-V UVLO 16-SOIC -40 to 125
Logic Gates Automotive 3-ch, 3-input, 2-V to 6-V low power OR gates with Schmitt-Trigger inputs 14-SOIC -40 to 125
Precision Amplifiers 36-V, Precision Rail-to-Rail
LDO Voltage Regulators High Vin, Low Iq Regulator
LDO Voltage Regulators 5.0V 150mA Positive
Digital Isolators Automotive, robust EMC, six-channel, 6/0, reinforced digital isolator 16-SSOP -40 to 125
Supervisory Circuits CMOS DETEC VOLT 2.7V
Isolation Amplifiers 4.25kV PEAK Iso Amp
MOSFET Dual SAB MOSFET ARRAY VT=1.70V
Ferrite Beads 1000 OHM 25%
Rectifiers 1.4A 200V
Schottky Diodes & Rectifiers SCHOTTKY 20V 0.5AF
ESD Suppressors / TVS Diodes 15V BIDIRECTION ESD DUAL
Schottky Diodes & Rectifiers 10 Amp 100V Schottky Rectifier
Supercapacitors / Ultracapacitors 2.7V, 360F, snap-in
Multilayer Ceramic Capacitors MLCC - SMD/SMT 10V 22uF X7R 1206 10%
Multilayer Ceramic Capacitors MLCC - SMD/SMT 25V 10uF X7R 1206 5% AEC-Q200
Multilayer Ceramic Capacitors MLCC - SMD/SMT 16V 2.2uF X7R 1206 5%
Multilayer Ceramic Capacitors MLCC - SMD/SMT 25V 1uF X7R 1206 5%

Multilayer Ceramic Capacitors MLCC - SMD/SMT 50V 0.1uF U2J 1206 1%

Multilayer Ceramic Capacitors MLCC - SMD/SMT 25V 0.01uF C0G 1206 1% AEC-Q200
Multilayer Ceramic Capacitors MLCC - SMD/SMT 50V 470pF C0G 1206 1%
Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 430pF 100volts C0G 5%
Multilayer Ceramic Capacitors MLCC - SMD/SMT 25V 330pF X8R 1206 1%
Multilayer Ceramic Capacitors MLCC - SMD/SMT 25V 100pF C0G 1206 1%
Pluggable Terminal Blocks LPC 6/ 3-ST-7,62
Solder Paste No-Clean 250g Sn63/Pb37 T4
Flat Cables .050 8C RND 28AWG 100 FT
Flat Cables 12/CAB/RC/TYP1/ 28AWG/STR/.050"/100'
Flat Cables .050" 16C ROUND 28AWG STD GRAY

RoHS	Lifecycle	Order Qty.	Price (NOK)	Ext.: (NOK)
RoHS Compliant		1	kr 4,27	kr 4,27
RoHS Compliant		1	kr 17,20	kr 17,20
RoHS Compliant By Exemption		3	kr 2,88	kr 8,64
RoHS Compliant	New Product	21	kr 10,20	kr 214,20
RoHS Compliant By Exemption		1	kr 5,76	kr 5,76
RoHS Compliant		2	kr 6,74	kr 13,48
RoHS Compliant	New Product	60	kr 8,83	kr 529,80
RoHS Compliant		36	kr 5,88	kr 211,68
RoHS Compliant		4	kr 6,12	kr 24,48
RoHS Compliant By Exemption		1	kr 38,52	kr 38,52
RoHS Compliant By Exemption		2	kr 4,97	kr 9,94
RoHS Compliant By Exemption		1	kr 0,876	kr 0,88
RoHS Compliant		3	kr 14,52	kr 43,56
RoHS Compliant		1	kr 17,92	kr 17,92
RoHS Compliant		13	kr 2,29	kr 29,77
RoHS Compliant		1	kr 14,11	kr 14,11
RoHS Compliant		2	kr 20,70	kr 41,40
RoHS Compliant		1	kr 29,66	kr 29,66
RoHS Compliant		2	kr 30,90	kr 61,80
RoHS Compliant	New Product	2	kr 4,37	kr 8,74
RoHS Compliant		12	kr 12,98	kr 155,76
RoHS Compliant		1	kr 3,84	kr 3,84
RoHS Compliant		1	kr 5,76	kr 5,76
RoHS Compliant	New Product	2	kr 45,32	kr 90,64
RoHS Compliant		12	kr 3,74	kr 44,88
RoHS Compliant		1	kr 40,89	kr 40,89
RoHS Compliant		6	kr 48,62	kr 291,72
RoHS Compliant		1	kr 0,876	kr 0,88
RoHS Compliant	New Product	3	kr 3,49	kr 10,47
RoHS Compliant		1	kr 4,10	kr 4,10
RoHS Compliant		1	kr 3,92	kr 3,92
RoHS Compliant		12	kr 5,19	kr 62,28
RoHS Compliant		12	kr 101,35	kr 1 216,20
RoHS Compliant		1	kr 21,32	kr 21,32
RoHS Compliant		1	kr 7,59	kr 7,59
RoHS Compliant		1	kr 2,88	kr 2,88
RoHS Compliant		6	kr 11,12	kr 66,72

RoHS Compliant	50	kr 16,07	kr 803,50
RoHS Compliant	5	kr 19,06	kr 95,30
RoHS Compliant	1	kr 16,38	kr 16,38
RoHS Compliant By Exemption	1	kr 2,88	kr 2,88
RoHS Compliant	1	kr 3,75	kr 3,75
RoHS Compliant	5	kr 5,84	kr 29,20
RoHS Compliant	2	kr 59,64	kr 119,28
	1	kr 479,36	kr 479,36
RoHS Compliant	1	kr 273,57	kr 273,57
RoHS Compliant	1	kr 347,52	kr 347,52
RoHS Compliant	1	kr 396,55	kr 396,55

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