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Faculty of Mathematics and Natural Sciences

Masters Thesis

Design of a Rectifier for Electric Vehicle Chargers

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Preface

This thesis was submitted in partial fulfilment for the degree of Master of Science in the field of electrical power engineering at the University of Bergen. The work was carried out for the duration of two semesters, from fall 2020 to spring 2021. The necessary resources and facilities were provided by the Western University of Applied Sciences.

The process of writing this thesis has been quite a fruitful endeavour. It has introduced me to many fascinating concepts and also allowed me to immerse myself in a field that I find highly interesting. However, it has not been a bed of roses all through. There have been many challenges along the way, and the completion of this thesis could not have been possible without the help and encouragement from the people involved in both my personal and academic life.

I would like to acknowledge the help and counsel received from my supervisor, Associate Professor Shujun Zhang, who also gave me the idea for this research project. Many thanks to my co-supervisor, Associate Professor Mostafa Paskyabi, for his invaluable feedback. I would also like to thank Senior Engineer Lars Manger Ekroll for providing me with the necessary laboratory equipment. Finally, I would like to extend my deepest gratitude to my friends and family, whose kind words and support have spurred me along to complete this work.

Abstract

Bidirectional Electric Vehicle (EV) chargers are becoming a more popular research topic in regard to overcoming the predicted increase in electricity demand from the decarbonization of the transportation sector. With a bidirectional charger, the energy stored in an EV battery can be transferred back to the grid in a grid-to-vehicle configuration, or power the home in a vehicle-to-home configuration. Conventional EV chargers are predominantly unidirectional and lack the necessary technology for bidirectional flow. This thesis investigates several rectifiers and control schemes with the aim of proposing an appropriate topology capable of being implemented in a bidirectional EV charger. The derived topology consists of a voltage-oriented controlled active front-end rectifier. Several topics related to the design are presented. Among these are the phase-locked loop, space vector modulation, voltage-oriented control, and filter design for mitigating harmonics.

The system is simulated in MATLAB Simulink during various load conditions to investigate the design and test the DC-link response of the controller. The results show that the system is capable of transitioning from rectification during a resistive load, to inversion during a regenerative load. The results also suggest that the system is capable of withstanding an increasing load, well over the intended application. This demonstrates the flexibility of the controller during off-nominal operation. A fast Fourier transformation analysis is conducted for all the load tests to verify the performance of the LCL filter. During nominal conditions, the results from the analysis show that the filter is able to attenuate the harmonics to an acceptable level in accordance with the IEEE standards.

An experimental prototype is designed for the purpose of investigating the simulated results. The design methodology and working principle behind all the components in the prototype are presented. This includes the process of programming the microcontroller unit, which is used to implement all the control algorithms. Tests are conducted to verify the performance of the hardware components and software algorithms. Results from tests suggest that more work needs to be done in order for the prototype system to work as designed.

Glossary

bandgap energy difference between the valence band and conduction band in insulators and semiconductors. 6

commutation transfer of current between semiconductor devices in a converter. 7

fundamental frequency lowest or base frequency of a complex waveform. 33

Hall effect named after Edwin Hall, who discovered that a magnetic field induces a transverse voltage in a conductor. 71

microprocessor peforms arithemtic and log operation. 60

Nyquist frequency named after Harry Nyquist, who discovered that a signal must be sampled at atleast twice its frequency to avoid alaising. 51

transducer converts one form of energy to another. 71

Nomenclature

Components

C_d, C_{dc} Output capacitor

L_r Rectifier inductor

L_s Gridside inductor

L_a, L_b, L_c Line inductors

R Arbitrary resistor

R_m Measurement resistor

R_p Input resistor

R_{load} Load resistor

Electrical

$\boldsymbol{i_r}$ Rectifier current vector

$\boldsymbol{i_s}$ Grid current vector

$\boldsymbol{i}$ Current vector

$\boldsymbol{i}_c^{dq}$ Filter capacitor current vector in dq frame

$\boldsymbol{i}_r^{dq}$ Rectifier current vector in dq frame

$\boldsymbol{i}_s^{dq}$ Grid current vector in dq frame

$\boldsymbol{i}_s$ Grid current vector

$\boldsymbol{v_c}$ Filter capacitor voltage vector

$\boldsymbol{v_r}$ Rectifier voltage vector

$\boldsymbol{v_s}$ Grid voltage vector

$\boldsymbol{v}$ Voltage vector

$\boldsymbol{v}^*$ Reference vector

$\boldsymbol{v}_c^{dq}$ Filter capacitor voltage vector in dq frame

$\boldsymbol{v}_r^{dq}$ Rectifier voltage vector in dq frame

$\boldsymbol{v}_s^{dq}$ Grid voltage vector in dq frame

$\boldsymbol{v}_k$ Switching vector w.r.t SVM state k

$\boldsymbol{v}_r$ Rectifier voltage vector

$\boldsymbol{v}_s$ Grid voltage vector

$\boldsymbol{x_{abc}}$ Arbitrary vector in abc domain

Δi_{max} Max ripple current

$\Delta V_{dc}, v_{rip}$ Ripple DC voltage

$\Delta v_d, \Delta v_q$ Voltage regulator outputs

i_d^*, i_q^* Reference currents

i_{rd}^*, i_{rq}^* Reference currents in dq frame

I_d DC current

I_s RMS line current

I_α, I_β Currents in $\alpha\beta$ frame

i_α, i_β Currents in $\alpha\beta$ frame

I_{sat} Inductor saturation current

I_a, I_b, I_c RMS phase currents

i_a, i_b, i_c Phase currents

i_{ca}, i_{cb}, i_{cc} Filter capacitor currents

i_{dcc} Capacitor current

i_{dc} Rectifier output current

I_d, I_q Currents in dq frame

i_d, i_q Currents in dq frame

i_{load} Load current

I_{PN} Nominal primary current

i_{ra}, i_{rb}, i_{rc} Rectifier phase currents

i_{rd}, i_{rq} Rectifier currents in dq frame

I_{rm} Maximum rectifier current

i_{sa}, i_{sb}, i_{sc} Gridside phase currents

I_{sm} Grid current amplitude

p^* Active power reference

q^* Reactive power reference

v^* Reference voltage

v_{dc}^*, v_{dc}^* DC reference voltage

v_{dq}^* Control signal vector

v_d^*, v_q^* Control signals

$V_d, V_{d\alpha}$ Average DC output

V_m Mesurement voltage

V_P Primary voltage

V_α, V_β Voltages in $\alpha\beta$ frame

v_α, v_β Currents in $\alpha\beta$ frame

v_{ab}, v_{bc}, v_{ac} Line-to-line voltages

V_{ADC} Analog voltage

v_a, v_b, v_c Phase voltages

v_{ca}, v_{cb}, v_{cc} Filter capacitor voltages

$V_{dc\min}$ Minimum DC voltage

V_{dc}, v_{dc} DC voltage

V_d, V_q Voltages in dq frame

v_d, v_q Voltages in dq frame

V_{IN} Input voltage

V_{LL} Line-to-line voltage

V_{offset} Offset voltage

V_{PN} Nominal primary voltage

V_{PWM} Voltage of PWM signal

v_{ra}, v_{rb}, v_{rc} Rectifier phase voltages

v_{rd}, v_{rq} Rectifier voltages in dq frame

v_{sa}, v_{sb}, v_{sc} Gridside phase voltages

v_{sd}, v_{sq} Grid voltages in dq frame

V_{sm} Grid voltage amplitude

v_{us} Undershoot voltage

x_a, x_b, x_c Signals in abc domain

x_d, x_q Arbitrary dq components

General

α Firing anlge

$\mathbf{T}$ Transformation matrix

$\mathbf{T}_c$ Clarke transformation

$\mathbf{T}_p$ Park transformation

$\boldsymbol{S}_r$ Rectifier switching state

$\boldsymbol{t_k}$ Duration of switching state k

$\boldsymbol{v}_1, .., \boldsymbol{v}_6$ Active SVM switching vectors

δ Attenuation constant

ω	Angular frequency
ω_n	Natural frequency
ω_{res}	Angular resonance frequency
$\theta, \omega t$	Instantenious phase-angle
θ^*	Angle of reference vector
θ_k	Angle of SVM sector k
θ_n	Angle of sector in DPC
ζ	Damping ratio
$a, a_{\max}$	Constants used for filter calulation
A	Area
a_0, a_h, b_h	Fourier coefficients
a_1, a_2, a_3	Constants used for filter calulation
A_α	Commutation delay area
b_2, b_3	Constants used for filter calulation
C	Capacitor
$C_{d\min}$	Min DC capacitance
$C_{f\max}$	Max filter capacitance
$C_{f\min}$	Min filter capacitance
dv	Voltage drop
f_g	Grid frequency
f_h	Frequency of harmonic order
f_{res}	Resonance frequency
F_{RMS}	Fourier transformation
f_{sw}	Switching frequency
Hp, Hq	Hysteresis bands
k_i	Intergral gain
k_p	Proportional gain
L	Arbitrary inductor
L_t	Total filter inductance
$L_{r\min}$	Min rectifier inductance
$L_{s\max}$	Max grid inductance
$L_{s\min}$	Min grid inductance
$L_{t\max}$	Max filter inductance
m_a, m_f	Modulation ratios
P, p	Active power
P_L	Load power
Q, q	Reactive power
S_1, S_2, S_3	Switching state
Sp, Sq	Hysteresis controller outputs
t	Time
T_s	Sampling time
t_0, t_7	Duration of SVM zero states
$t_1, .., t_6$	Duration of active SVM states
T_{sim}	Simulation time
T_{sw}	Switching time
v_{cr}	Carrier signal

Acronyms

ADC Analog to Digital Conversion. 62, 64, 72, 76, 77, 82–84, 88, 89

AFE Active Front End. 12–17, 20, 27, 28, 30, 32, 37, 54, 56, 57, 59, 100

BJT Bipolar Junction Transistor. 5, 13

CBPWM Carrier Based Pulse Width Modulation. 20, 22

DPC Direct Power Control. vi, 17, 30, 32, 37, 100

ePWM Enchanced Pulse Width Modulation. 64, 74, 75, 82, 83, 87

EV Electric Vehicle. 1–3, 76

FFT Fast Fourier Transform. 51

GaN Gallium Nitride. 6

GPIO General Purpose Input/Output. 64, 70, 81

GTO Gate Turn of Thyristor. 4

HVL Western Norway University of Applied Sciences (Høgskulen på Vestlandet). 62

IC Integrated Circuit. 75, 80, 88

IEEE Institute of Electrical and Electronics Engineers. 46, 51

IGBT Insulated Gate Bipolar Transistor. 5, 13, 60–62, 65, 66, 68, 74–76, 83, 87, 88, 101, 116

KVL Kirchhhoff's Voltage Law. 13, 39

LED Light Emitting Diode. 68–70

MCU Microcontroller Unit. 45, 60–64, 66, 68–71, 73–75, 80–83, 88, 101

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor. 5, 13, 66

PCB Printed Circuit Board. 61–63, 68–72, 101

PF Power Factor. 2, 17, 51, 86

PFC Power Factor Correction. 2, 3

PLL Phase Locked Loop. 27, 28, 43, 44, 49, 50, 81, 82, 84, 85, 89, 100, 101

PWM Pulse Width Modulation. v, 12, 13, 17, 20–22, 27, 37, 50, 60, 62, 64, 66, 68–70, 74, 75, 83, 100, 101

RMS Root Mean Square. iv, 8, 33, 35, 78, 79, 88

SiC Silicon Carbide. 6

SVM Space Vector Modulation. iv–vi, 22, 26, 37, 44, 45, 49, 50, 83, 101

TF Transfer Function. 44

THD Total Harmonic Distortion. 3, 33, 35, 37, 43, 46, 51–53, 55, 86, 87

UPF Unity Power Factor. 29, 31, 40, 46, 51, 52, 86

V2G Vehicle-to-Grid. 1, 2

V2H Vehicle-to-Home. 1, 2

VBC Voltage Based Control. 17

VFBC Virtual Flux Based Control. 17

VOC Voltage Oritented Control. 17, 18, 20, 22, 27, 28, 37, 76, 100

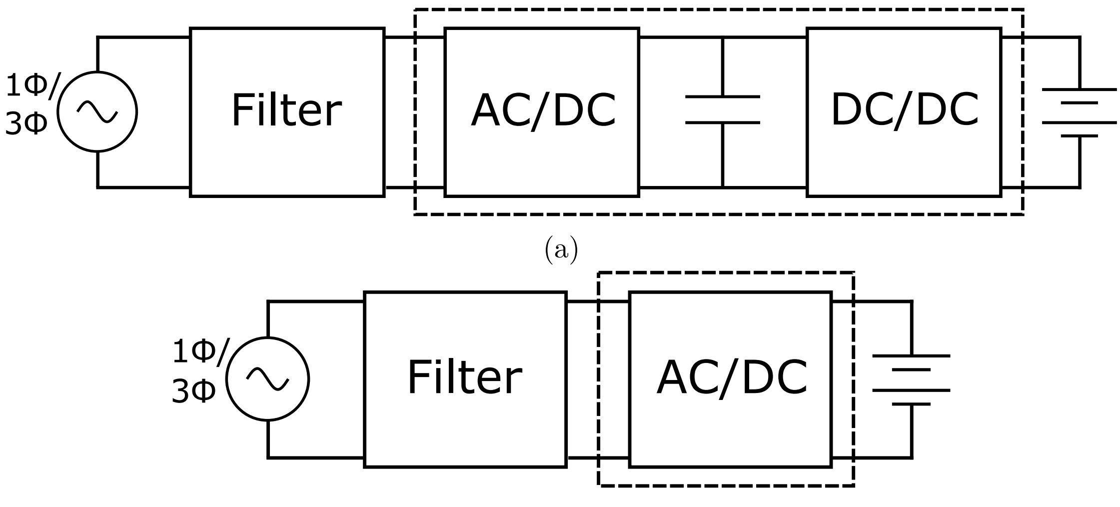
Contents

1 Introduction

1.1 Background

The reality concerning climate change and environmental degradation from carbon emissions has strengthened the global response in favour of using alternative energy in otherwise fossil dependent sectors. In particular, the transportation sector is highly dependent on fossil fuels, as almost all of the energy (95%) is derived from petroleum [1, 2]. Transportation is also responsible for 24% of direct CO2 emissions from fuel combustion [3]. As an effort to cut pollution, several nations have established a timeline for phasing out combustion engine vehicles [4]. This has caused a rise in development and sales of Electric Vehicles (EV), which has already been on an increasing trend globally and is expected to increase further [5]. The electricity demand is also expected to increase in parallel to the decarbonisation of the transportation sector. Furthermore, new infrastructure is being built to accommodate for the energy needs required by the increasing amount of EVs. However, with the current available technology, it can be difficult for the grid utility to meet the increasing energy demand. More specifically, as more charging stations are being installed in both private and public settings (e.g., filling stations and parking lots), balancing the electricity demand and supply will become an increasing challenge. This is partly due to EVs being a mobile and unpredictable load. Another reason is that the majority of EV chargers are uncontrolled, that is, unable to regulate the power consumption with respect to the capacity of the connected grid [6]. Furthermore, given that the majority of EVs are connected to the grid while idle [7] makes them an unnecessary load when fully charged. There has been several researches on the topic to overcome these challenges, and some emerging concepts are Vehicle-to-Grid (V2G), Vehicle-to-Home (V2H) and smart charger technology [8–12].

Smart charging implies that an algorithm is used to control and coordinate the charging of the EV, as opposed to uncontrolled charging, which, as mentioned earlier, means that charging of the EV occurs the instant it is connected to the utility. With smart charging, the total grid load during times of maximum energy consumption (peak load hours) can be reduced significantly. With an appropriate algorithm, an EV charger can be programmed to charge with respect to the electricity price. This also creates an economic incentive for EV owners to adopt smart charger technology. Furthermore, there is also an economic incentive in adopting V2G technology. With V2G, the energy stored in the EV battery can be transferred back to the grid. In combination with smart charging, this allows EV owners to charge when the electricity is cheap and sell power back to the utility at a higher price during peak load hours (also called energy arbitrage). For EV owners living in self-sufficient smart homes, V2G can be especially profitable. In this case, surplus energy generated from intermittent energy sources (e.g., rooftop solar panels or small-scale wind turbines) can be sold to the utility. Aside for monetary gain, another advantage is that transferring power back to the grid can help compensate for larger intermittent energy sources, which can adversely affect the stability of the grid in terms of frequency, voltage, and Power Factor (PF). Otherwise, with a V2H configuration, the energy stored in the EV battery can be used to power the home. During a power outage, V2H can be quite useful as the EV battery can act as an backup supply. There are clearly many benefits with V2G and V2H technologies. However, for any of these to be possible, an appropriate EV charger is needed.



(a)

(b)

Figure 1.1: General architecture of a two-stage charger (a) and single-stage charger (b). The supply can be either single-phase (1ϕ) or three-phase (3ϕ).

In general, EV chargers have a single or two stage architecture [13, 14], as shown in Figure 1.1. In a two-stage architecture, an active front-end rectifier provides Power Factor Correction (PFC) and steady DC voltage to a DC/DC converter. The DC/DC converter can be used to provide a galvanic isolation, but has the main function of regulating the power flow. Most EV chargers use a two-stage configuration for higher efficiency and step-up capabilities. A single-stage configuration (no DC/DC converter) is often preferred for a cheaper and less bulky design. Either way, for V2G and V2H to be possible, it is essential that the converter(s) have bidirectional capabilities. Furthermore, a control algorithm is needed for maintaining the desired DC voltage and conducting PFC. With an appropriate design, a high efficiency can be achieved with a low Total Harmonic Distortion (THD). Moreover, the filter design is important for mitigating harmonics, which, if neglected, can cause overheating and have a degrading effect on the system [15].

1.2 Objectives

The aim of this thesis is to design and implement a 20 kW three-phase bidirectional AC/DC rectifier system. More specifically, the objectives are:

- Propose a topology and describe its operating principle.
- Construct a simulation model and produce results verifying its bidirectional capabilities.
- Construct a prototype and measure its output for verifying the simulation results.

1.3 Outline

In the following chapter, the theory behind various concepts, which are prerequisite for designing an appropriate rectifier are presented. In chapter three follows a complete presentation of the proposed rectifier, including results from simulations conducted for various load conditions. The process of building the experimental prototype system, and results from real-time tests are presented in chapter four. A discussion concerning the performance of the designed system, based on both simulation and physical results, is presented in chapter five. Finally, a conclusion is formulated in chapter six.

2 Theoretical Framework

This chapter serves to give an overview of the fundamental knowledge related to the design of a front end rectifier system capable of bidirectional flow. Various topics concerning power electronics and control are presented, with an emphasis on rectifier topologies used for three phase AC/DC converters.

2.1 Power Semiconductor Devices

In all converters, the power flows through semiconductor devices that are either in the off-state (reverse biased) or on-state (conducting). Ideally, these devices should not conduct current in the off-state. In reality, there will be a small leakage current during reverse bias until the device reaches its breakdown voltage. These characteristics are determined by the semiconductor material. Silicon (Si), Germanium (Ge) and Gallium Arsenide (GaAs) are traditionally used for manufacturing such devices [16].

It is possible to classify all semiconductor devices in three main categories according to their degree of controllability, namely diodes, thyristors and controllable switches. Below is a figure showing the generic symbols for each category. There are of course many different variations of these devices, with their own characteristic symbols. However, they are all based on at least one of the working principles which defines the three categories.

In a diode, the on and off states are controlled by the power circuit. Depending on its predefined characteristics, it will ideally start conducting when forward voltage across the device is at rated value. For a thyristor, the on state can be triggered by applying a pulse of current at the gate terminal during its forward-blocking state. Once the device starts conducting, it cannot be turned off by the gate, and behaves like a diode until the anode current changes polarity. Afterwards the gate regains control with the possibility of triggering the device into its on state during its initial blocking condition. This latch-like behaviour differs from a controllable switch, which can be turned both on and off by the gate [17].

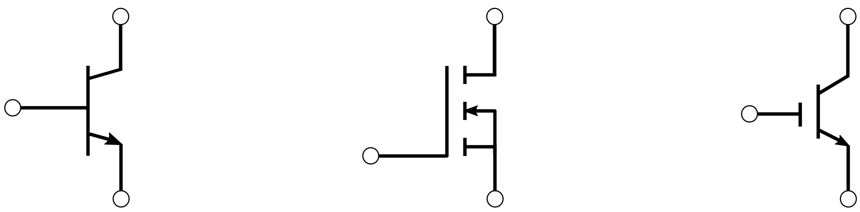
The Gate Turn of Thyristor (GTO) and various other transistors can be categorized as controllable switches. The GTO is similar to the thyristor in Figure 2.1b,

(a) (b) (c)

Figure 2.1: Generic symbol for a diode (a), thyristor (b) and controllable switch (c).

but can be turned off by applying a negative gate-cathode voltage, and is therefore classified as a controllable switch. Transistors have the same controllability, and due to major advances during recent years, there have been developed many different variations [18].

The most popular transistors are the Bipolar Junction Transistor (BJT), Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and the Insulated Gate Bipolar Transistor (IGBT). Respective symbols representing each transistor is shown in Figure2.2.



(a) (b) (c)

Figure 2.2: Symbols representing the BJT (a), MOSFET (b) and IGBT (c).

2.1.1 Comparison of Controllable Switches

Due to structural differences and junction composition, all controllable switches have a nominal range of operation. This range can be defined by power capability and switching speed, as illustrated in Figure 2.3. This comparison is useful for selecting a device that meets the requirements of an arbitrary converter. However, other factors such as price and switching losses should also be considered.

Due to minor switching losses and high switching frequencies, the MOSFET is preferred in low- and medium-power applications (<500 kW). Furthermore, the IGBT is appropriate for high power applications (>500 kW) [18]. The nominal power rating is often limited by the semiconductor material used to manufacture the switch.

Figure 2.3 only compares Si devices. However, due to limitations on semiconductor properties (e.g power density and temperature), there have been developed two new alternatives which have attracted considerable attention in the last decade, namely Silicon Carbide (SiC) and Gallium Nitride (GaN). Their superiority stems from having a wide bandgap, which enables them to operate at temperatures above 600°, in addition to other properties as low leakage current and high breakdown strength [19–22].

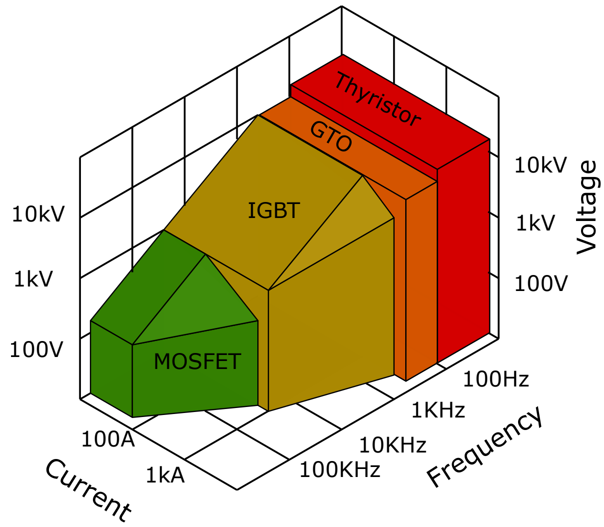


Figure 2.3: Comparison of Si devices with respect to voltage, current and frequency. Adapted from [18].

2.2 Three Phase Rectifiers

Rectifiers are used for AC to DC conversion. They have a wide range of applications and are often found in DC power supplies. Other applications include: high voltage power transmission, electrochemical processes, motor drives, and traction equipments [19]. Depending on the power rating and application, rectifiers can have a three or single phase topology. Both utilize semiconductor devices (presented in section 2.1) for the conversion process.

In rectifiers, semiconductor devices form a bridge that connects the AC part of the topology to a DC bus, storage element or load. Capacitors are normally used to store the DC voltage. Conversion quality and other capabilities are determined by various factors, including capacitor size, controllability and characteristics of the devices used in the bridge. In reference to the three main categories of semiconductors from Figure 2.1, a rectifier can be classified as a diode, thyristor or a fully controlled rectifier.[1] In high power applications, these types of rectifiers usually adopt three phase topologies.

In this section, the working principle of three different three-phase rectifiers are presented and compared [17]. For simplicity, only idealized circuits without grid side inductance, with constant DC voltage, and without load are analysed in section 2.2.1 and 2.2.2. In reality, grid side inductance affects the commutation process, causing a phase shift in the rectified current, which consequently forces more than one diode to conduct simultaneously with a continuously flowing current [17].

2.2.1 Diode Rectifier

A circuit of a three-phase diode bridge rectifier is illustrated in Figure 2.4. The rectifier provides a DC current i_d and voltage v_d at the output, which is connected to a capacitor C_d. The instantaneous currents are denoted as i_a, i_b and i_c. These currents flow through the diodes in a sequential order. More specifically, the diodes conduct in pairs and are numbered according to their respective sequence: D1-D2, D3-D2, D3-D4, D5-D4, D5-D6 and D1-D6. Each sequence lasts for 60°, where each diode conducts for 120°.[2] This configuration gives a DC output with six ripple pulses over the course of one period (360°), and is therefore often called a six-pulse bridge rectifier.

The conduction sequence depends on the difference in voltage between common anode and cathode for the top and bottom diodes, respectively. In other words, the diode with highest anode voltage among D1, D3 and D5, and lowest cathode voltage among D2, D4 and D6 will conduct simultaneously as a pair. This conduction scheme can be seen in Figure 2.5. The phase (i.e line-to-neutral) voltages are denoted as v_{an}, v_{bn} and v_{cn}. The instantaneous DC side voltage is denoted as v_d.

The average value of the output DC voltage can be derived from one ripple pulse (60°). For this purpose, the time origin $t = 0$ in Figure 2.5 is set at a point where the line-to-line voltage v_{ab} is at its maximum. The instantaneous waveform of v_d can therefore be expressed as:

$$v_d = v_{ab} = \sqrt{2}V_{LL}\cos\omega t \qquad -\pi/6 < \omega t < \pi/6 \tag{2.1}$$

[1] A fully controlled rectifier is also called an active or synchronous rectifier.
[2] For this to work, one diode must conduct for 60° in the start.

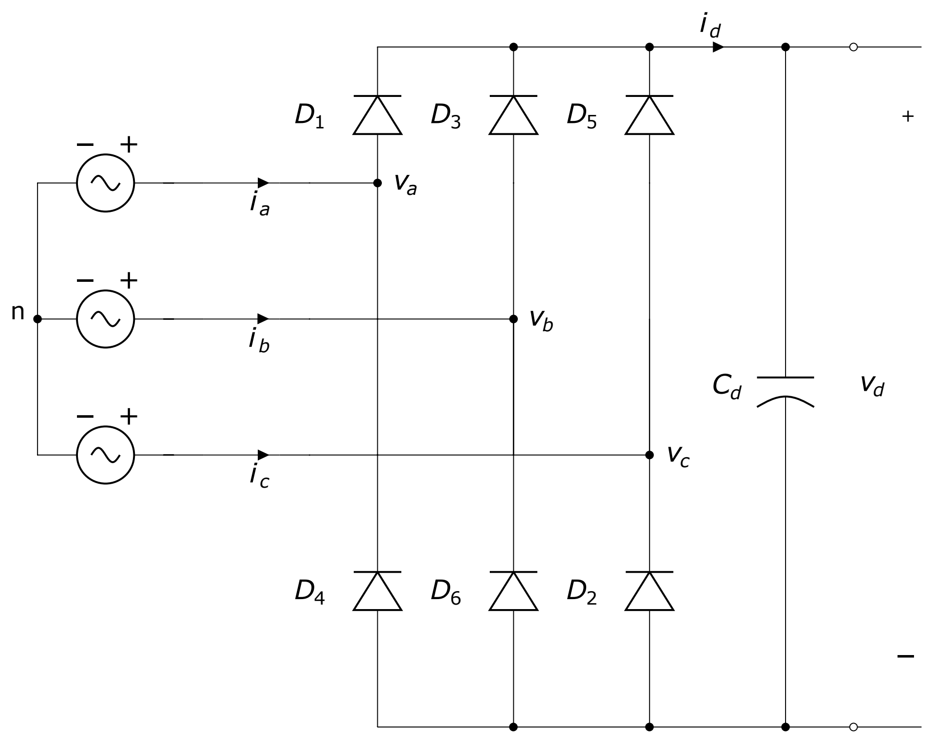


Figure 2.4: Three-phase diode rectifier.

where V_{LL} is the RMS line-to-line voltage. Integrating this expression with respect to the sequence duration, gives the corresponding volt-second area:

$$A = \int_{-\pi/6}^{\pi/6} \sqrt{2} V_{LL} \cos \omega t \, d(\omega t) = \sqrt{2} V_{LL} \tag{2.2}$$

A simplified expression for the average DC output can now be derived by dividing A over the interval $\frac{\pi}{3}$:

$$V_d = \frac{1}{\pi/3} \int_{-\pi/6}^{\pi/6} \sqrt{2} V_{LL} \cos \omega t \, d(\omega t) = \frac{3}{\pi} \sqrt{2} V_{LL} = 1.35 V_{LL} \tag{2.3}$$

In this idealized case, the RMS value of the line current I_s can easily be derived with respect to the DC current I_d:

$$I_s = \sqrt{\frac{1}{\pi} \int_{\frac{\pi}{3}}^{\pi} I_d^2 d(\omega t)} = \sqrt{\frac{2}{3}} I_d = 0.816 I_d \qquad s \in \{a, b, c\} \tag{2.4}$$

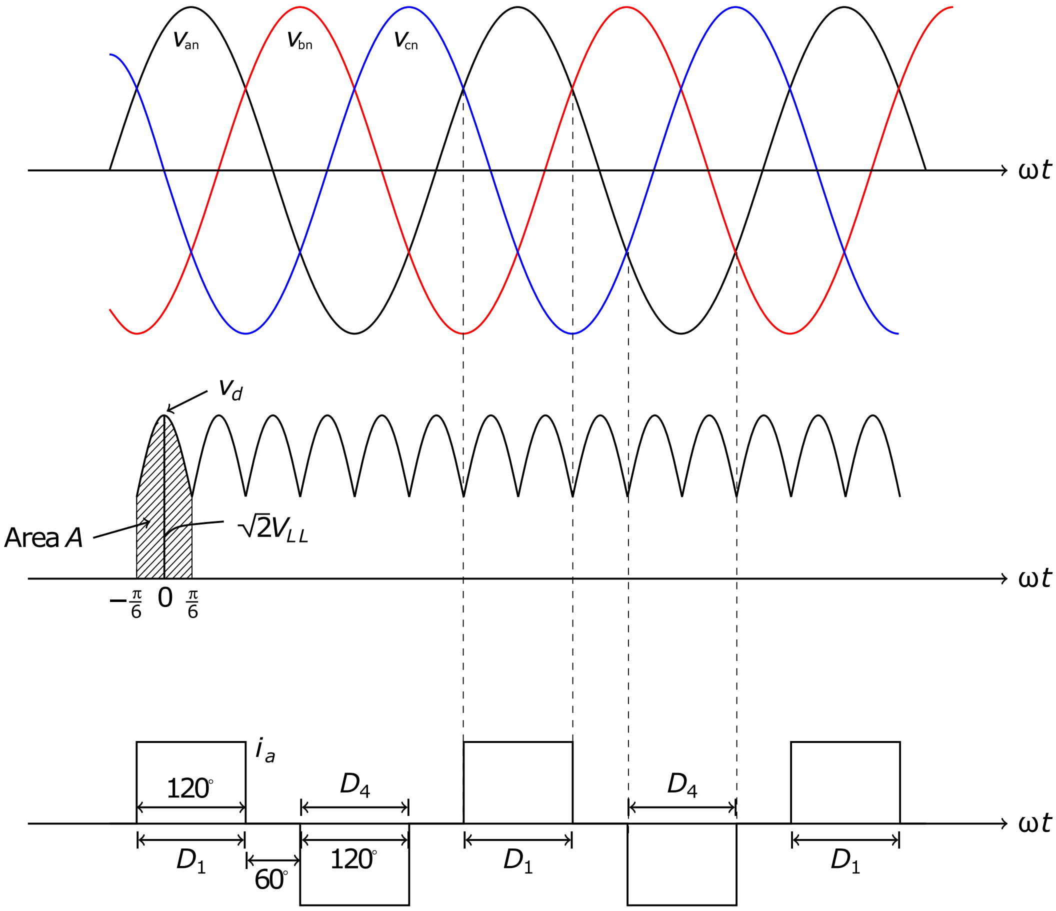


Figure 2.5: Conduction scheme for the circuit in Figure 2.4 [23]

2.2.2 Thyristor Rectifier

If the diodes (D1-D6) in Figure 2.4 are replaced by thyristors (T1-T6), the circuit will look like the one given below in Figure 2.7. The difference between using diodes or thyristors in a three phase rectifier topology lies in the controllability. As briefly discussed in section 2.1, thyristors can be turned on by an external gate pulse during forward bias. Using thyristors therefore gives the advantage of being able to control the output DC voltage. This is done by timing the gate pulse firing angle α, relative to the AC voltage phase angle ωt. This means that the rectified output voltage can be derived as a function of the thyristor firing angle.

Being able to control the average DC output includes extended capabilities that surpasses traditional rectifier operation. In addition to outputting a positive DC voltage, the thyristors can also be controlled in a manner of inverting an arbitrary voltage DC source. Ideally, this transition is continuous, with the capability of changing the output from a positive maximum to a negative minimum. Although,

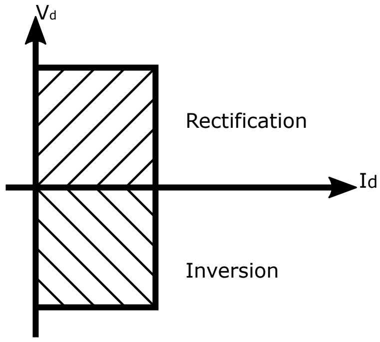


Figure 2.6: Active quadrants, adapted from [17].

during such a transition when the DC voltage changes its polarity, the DC current will maintain its direction. This means that the converter only operates in two of the four quadrants spanning the $V_d - I_d$ plane, as illustrated in Figure 2.6. The DC limits are determined by the circuit configurations and input voltage, while the current is limited by the components' rating. However, for deriving a relationship between the average DC output and firing angle, an analysis of the converter in rectifier operation will suffice.

If gate pulses are continuously provided to the thyristors in Figure 2.7 without delay ($\alpha = 0°$), the output voltage will be the same as for the rectifier discussed in section 2.2.1. The respective formula has been derived in (2.3). By itself, this relation is not valid with a delayed firing angle ($\alpha > 0°$). In this case, a new equation can be derived from the waveforms illustrated in Figure 2.8.

When the gate pulse is sent, a pair of thyristors will start conducting until the sequence is done. Because this is a six pulse topology with a 120° conduction scheme similar to the diode rectifier, a new sequence will start every 60° from the first gate pulse at $\omega t = \alpha + 60°$. In Figure 2.8, the thyristor firing angle is set at $\alpha = 30°$, from $\omega t = 0$. This delay is marked on the voltage waveform as the area A_α. The difference between the phase current and voltage can be given as $\phi_1 = \alpha$. From the waveform, it is also clear that the average DC output will be lower with a higher firing angle. The average DC output can therefore be expressed as:

$$V_{d\alpha} = V_d - \frac{A_\alpha}{\pi/3} \tag{2.5}$$

The volt-second area A_α can be obtained through the integral of $v_{an} - v_{cn}$ (=v_{ac}),

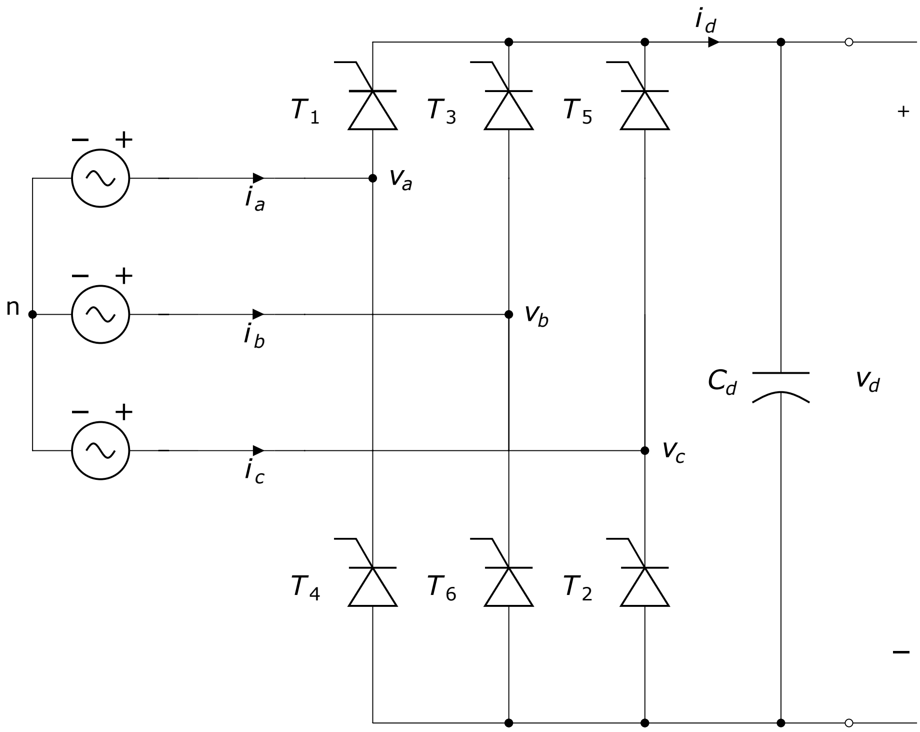


Figure 2.7: Three phase thyristor rectifier.

which is given as:

$$v_{ac} = \sqrt{2}V_{LL}\sin\omega t \tag{2.6}$$

Furthermore, the area can be found as:

$$A_\alpha = \int_0^\alpha \sqrt{2}V_{LL}\sin\omega t\, d(\omega t) = \sqrt{2}V_{LL}(1-\cos\alpha) \tag{2.7}$$

By substituting v_d and A_α in (2.5) with the expressions from (2.3) and (2.7), it is possible to derive a simplified statement for the average DC voltage:[3]

$$V_{d\alpha} = \frac{3\sqrt{2}}{\pi}V_{LL}\cos\alpha = 1.35V_{LL}\cos\alpha \tag{2.8}$$

The line current is the same as for the diode rectifier:

$$I_s = \sqrt{\frac{2}{3}}I_d \tag{2.9}$$

[3]If the firing angle is $\alpha > 90°$, the converter will act as an inverter.

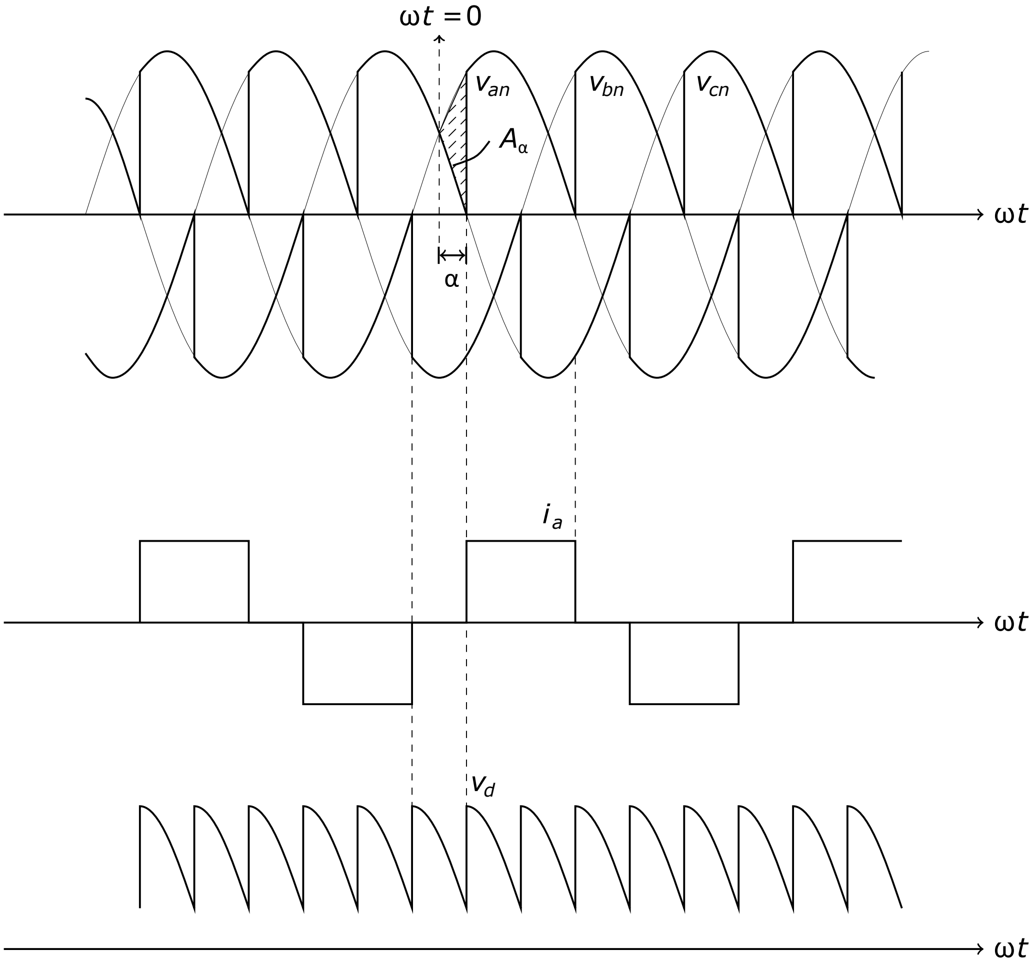


Figure 2.8: Waveforms for the circuit in Figure 2.7 [23].

2.2.3 Active Front End Rectifier

An Active Front End (AFE) converter utilizes controllable switches (usually transistors [24]) for converting voltage. Similar to the thyristor converter, both rectification and inversion is possible. However, as mentioned in section 2.1, controllable switches can be switched on and off whenever required. This allows for forced commutation independent of the line voltage, which depending on the device rating, can occur several hundreds of times during one period. With this increased control, it is possible to modulate the drawn current by means of timing the gating pulses relative to a reference signal. This method is called Pulse Width Modulation (PWM), and makes it possible for the converter to transfer power bidirectionally. PWM will be discussed more later in section 2.3.2.

In general, an AFE converter can operate in all four quadrants of the aforementioned $V_d - I_d$ plane, as illustrated in Figure 2.9. However, the figure clearly shows that there are two quadrants for rectification. This means that there are two scenarios where the AFE converter will operate as a rectifier: by DC voltage reversal with positive i_d, or the inverse – DC current reversal with positive v_d. Either way, the DC side can be built with a current-source (inductor) or voltage-source (capacitor). The latter is by far the most widely used topology [19], and will therefore be in focus for the following analysis. A circuit of the voltage-source rectifier can be seen in Figure 2.10. For the sake of example, the bridge consists of six IGBTs. However, other transistors like the BJT and MOSFET are also commonly used in AFE rectifiers. By combining these devices with a proper control scheme, it is possible to achieve the desired DC output.

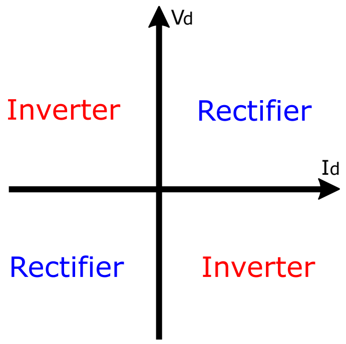


Figure 2.9: Operational quadrants for the AFE converter.

The goal of a voltage-source rectifier is to keep the DC output voltage at a constant level. Depending on the specifications, the DC voltage can also be controlled to match a predefined reference value. This is done by combining the rectifier with a control circuit, forming a feedback loop. In such a configuration, V_d is compared with the reference value, generating an error signal. This difference is fed to a control block, which uses PWM to generate the appropriate gating signals, supplying the required DC current. There are of course various elements involved in such a control circuit, and due to the complexity it will be discussed separately in section 2.3. For now, a basic analysis of the voltage-source rectifier without a control circuit will be conducted.

In Figure 2.10, the inductors L_a, L_b and L_c represent the line inductances. By assuming $L_a = L_b = L_c = L_s$, and using Kirchhhoff's Voltage Law (KVL), the voltage equations can be expressed as:

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = L_s \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.10}$$

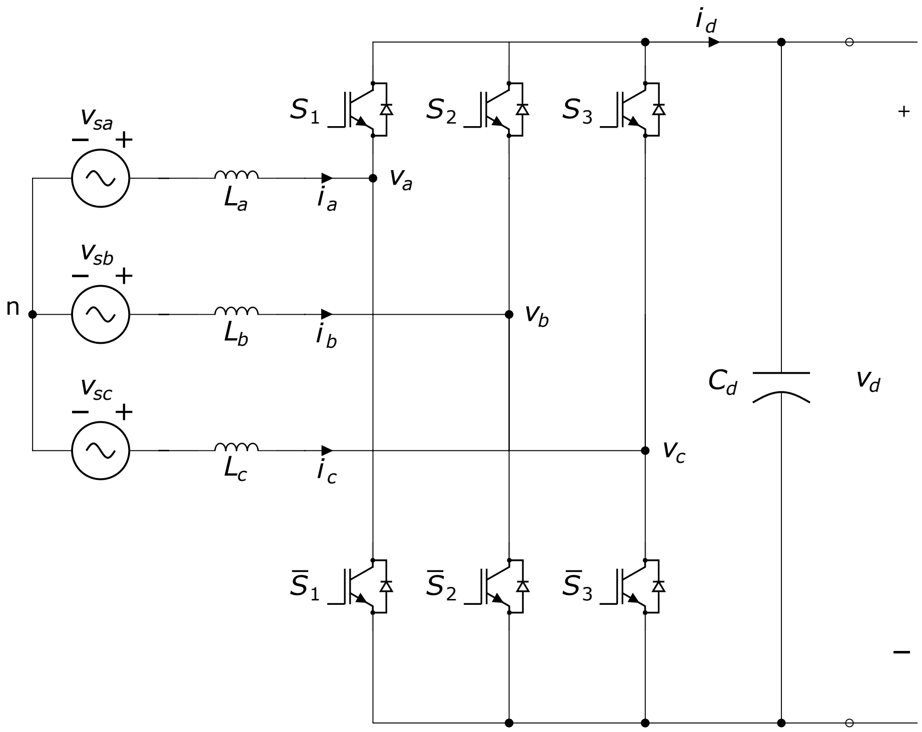


Figure 2.10: Circuit of a voltage-source AFE rectifier.

Furthermore, the AC side voltages can be simplified into a space vector [25]:

$$\boldsymbol{v}_s = \frac{2}{3}(v_{sa} + \mathbf{a}v_{sb} + \mathbf{a}^2 v_{sc}) \tag{2.11}$$

where $\mathbf{a} = e^{j2\pi/3}$. A vector equation for the grid dynamics can now be obtained by substituting (2.10) into (2.11):

$$\boldsymbol{v}_s = L_s \frac{d}{dt}(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)) + \frac{2}{3}(v_a + \mathbf{a}v_b + \mathbf{a}^2 v_c) \tag{2.12}$$

The equation above can be further simplified by the following definitions:

$$\boldsymbol{i}_s = \frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c) \tag{2.13}$$

$$\boldsymbol{v}_r = \frac{2}{3}(v_a + \mathbf{a}v_b + \mathbf{a}^2 v_c) \tag{2.14}$$

where $\boldsymbol{v}_r$ is determined by the switching state of the converter ($\boldsymbol{S}_r$) and DC voltage.

This relationship can be expressed as:

$$\boldsymbol{v}_r = \boldsymbol{S}_r V_d \tag{2.15}$$

The switching states for each of the converter's legs can be defined as S_1, S_2 and S_3. Considering that the switches can be either on or off, each state can be defined with a binary value (1 or 0). $\boldsymbol{S}$ can then be defined in a vector space as follows:

$$\boldsymbol{S} = \frac{2}{3}(S_1 + \mathbf{a}S_2 + \mathbf{a}^2 S_3) \tag{2.16}$$

It is now possible to simplify (2.12) to:

$$L_s \frac{di_s}{dt} = \boldsymbol{v}_s - \boldsymbol{v}_r \tag{2.17}$$

2.2.4 Comparison

The working principle of the diode, thyristor, and AFE rectifier has been explained in the previous sections. By comparing the three, it is clear that the diode rectifier has the simplest and cheapest topology. However, it also has a major disadvantage when it comes to control. Being a line-commutating rectifier and therefore entirely dependent on the line voltage, there is virtually no possibility for controlling the DC output. Using thyristors solves this issue by changing the firing angle to manipulate the flow of power. Although this makes the thyristor rectifier bidirectional, the controllability is still limited by the line voltage. Apparently, full controllability is achieved by forced-commutation, as implemented in the AFE rectifier. This allows for bidirectional flow and gives the opportunity for controlling the DC voltage according to a predefined reference value. However, aside from a more complicated control, its main disadvantage is the higher cost in comparison to the diode and thyristor rectifier [25].

The AC inputs and DC output for each rectifier is presented in Figure 2.11. From observation, a connection between stability and current drawn from the grid can be made. Figure 2.11c represents the characteristics of an AFE rectifier, and has the most stable output. This is due to the gate turn-off capability of controllable switches that makes them able to switch on and off several times during one cycle, and therefore draw a current resembling a sinusoid. In reality, the current is never perfectly sinusoidal due to distortion. They are, however, lower in an AFE rectifier compared to a diode and thyristor rectifier.

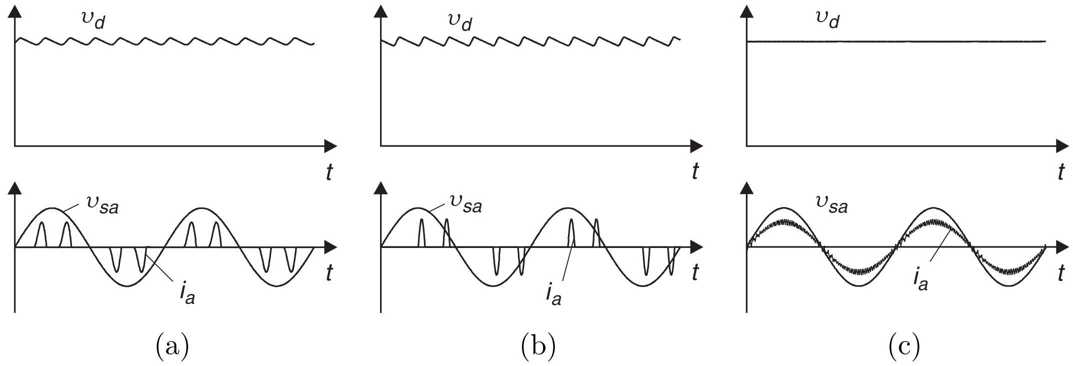


Figure 2.11: AC inputs and DC output for the diode (a), thyristor (b) and AFE rectifier (c) [25].

Distortion and efficiency are other important factors to consider when comparing the three topologies. Distorted current is often drawn from the grid, but is also affected by the process of power conversion in the converter (i.e. commutation and switching). The efficiency is also greatly affected by the ability to draw a perfectly sinusoidal current. These aspect have not been discussed previously, but from analysis conducted in the previous subsections, it follows that there is a relationship between the current distortion, and control of the converter. Therefore, it also follows that the diode rectifier will give the highest distortion and lowest efficiency, while an AFE rectifier has the potential of operating at a higher efficiency with the lowest distortion. This, of course, is a generalisation which in reality largely depends on the system in question. With this in mind, a general table comparing the different aspects discussed until now can be made, as presented in Table 2.1.

Rectifier	**Distortion**	**Control**	**Efficiency**
Diode	Highest	None	Lowest
Thyristor	High	Semi	Low
AFE	Low	Full	High

Table 2.1: General comparison of different rectifiers.

2.3 Control Strategies

In rectifiers, the term control is often used to describe the ability to somehow affect the conversion of power. In this section, the focus will be on different types of control circuits and the elements involved in manipulating the conversion process of three phase rectifiers. In view of the fact that controllability of the diode and thyristor rectifier is limited, there is no point in discussing this aspect for these particular topologies. The AFE rectifier, however, is of more interest due to its controllable switches.

The concept of applying a control scheme to an AFE voltage-source rectifier for maintaining a constant DC output voltage has been introduced in the previous section. This type of control can generally be classified as Voltage Based Control (VBC) and is being used in many different applications,[4] e.g., motor drives, wind power systems, and micro-grids [26–29]. There are many variations of VBC, and aside from keeping the DC output constant, they also aim to deliver a clean sinusoidal waveform with high Power Factor (PF). There are, however, principle differences in how they operate to achieve these goals.

The two main types of VBC are Voltage Oritented Control (VOC) and Direct Power Control (DPC). Both control strategies have the same inputs in terms of DC reference voltage and line measurements. The difference lies in the fundamental principles which are used to build the control circuits. In the case of VOC, the AC measurements are transformed into a rotating reference frame by the use of coordinate transformation. This way, the AC measurements can be treated as DC quantities, and easily regulated inside an inner current loop to generate the necessary reference signals for controlling the PWM (coordinate transformation will be discussed in detail later). This makes it possible for the AFE converter to operate as a rectifier by drawing a sinusoidal current in phase with the grid voltage, while maintaining a constant DC output. The key elements in VOC can therefore be defined as the current loop and PWM module. For DPC the strategy is quite different.

As opposed to VOC, DPC has no inner current control loop or PWM module. Instead, switching states are selected from a table based on the instantaneous errors between the commanded and estimated values of active and reactive power. The fundamental principle behind DPC is therefore efficient calculation of line power for determining the correct switching states. This makes the implementation of VOC far more complicated in comparison. Although VOC demands a current loop and PWM, it is still the most popular strategy [26]. This is in part because VOC has the ability to operate with a fixed switching frequency, and possibility of utilizing more advanced PWM techniques. However, for this to be possible, a

[4]The term: Virtual Flux Based Control (VFBC) is often used instead of VBC as an analogy to motor control

coordinate transformation and decoupling between active and reactive components is required.

2.3.1 Clarke and Park Transformation

In VOC, coordinate transformation is used for simplifying three phase AC measurements into more manageable quantities which can be regulated inside control loops. After regulation, these quantities can be inverse transformed into AC values. There are specifically two types of transformations that can be implemented, Clarke and Park transformation. Clarke transformation is used to represent three phase values as two components in an orthogonal stationary frame, which is also called the $\alpha\beta$ coordinate system [30, 31]. This transformation is illustrated in Figure 2.12b.

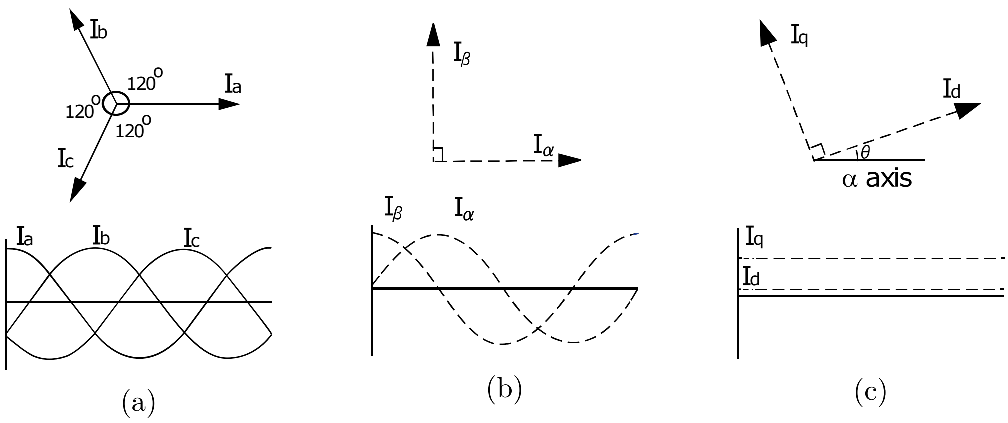


Figure 2.12: Three different reference frames, showing the abc (a), $\alpha\beta$ (b) and dq (c) coordinate system with output signals [32].

By assuming a generic set of symmetrical and balanced three phase AC currents I_a, I_b and I_c (120° displacement), the orthogonal components I_α and I_β can be expressed as:

$$\boldsymbol{I}_{\alpha\beta0} = \mathbf{T}_c \boldsymbol{I}_{abc} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.18}$$

where the zero component is 0, due to balanced AC values. However, for calculating active and reactive power in the $\alpha\beta$ domain, another variation of the Clarke transformation must be used instead. This is due to the transformation matrix $\mathbf{T}_c$ not being unitary. For the preservation of power, $\mathbf{T}_c$ must therefore be replaced with another matrix that fulfils the general criteria: $\mathbf{T}^*\mathbf{T} = \mathbf{T}\mathbf{T}^*$. As derived in [33], the power invariant Clarke transformation can be expressed as:

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.19}$$

The inverse Clarke transformation can then be given as:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \\ 0 \end{bmatrix} \tag{2.20}$$

The orthogonal $\alpha\beta$ components represent two AC signals that rotate with a fixed frequency. By using Park transformation, these AC signals can be simplified to appear as DC quantities instead (Figure 2.12c). This is done by transforming the stationary $\alpha\beta$ frame into a rotating reference frame, which is also called the *dq* coordinate system. By assuming that I_d and I_q are rotating with an arbitrary frequency, this transformation can be derived as:

$$\begin{bmatrix} I_d \\ I_q \\ 0 \end{bmatrix} = \mathbf{T}_p \boldsymbol{I}_{\alpha\beta} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \\ 0 \end{bmatrix} \tag{2.21}$$

where the position is determined by θ. Similarly to Clarke transformation, (2.21) has a zero component under the assumption of a balanced set of AC values. Clarke and Park transformation are often combined [34], so that a coordinate transformation from the *abc* time domain to the *dq* domain can be done in one step. This is possible by multiplying the transformation matrix in (2.20), with the one in (2.21). The resulting matrix $\mathbf{T}_{cp}$, can then be derived as:

$$\mathbf{T}_{cp} = \mathbf{T}_p\mathbf{T}_c = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.22}$$

The inverse transformation is:

$$\mathbf{T}_{cp}^{-1} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{\sqrt{2}} \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.23}$$

For a coordinate transformation from the *abc* time domain to the *dq* domain, $\mathbf{T}_{CP}$ from (2.22) can be used as:

$$\boldsymbol{I}_{dq0} = \mathbf{T}_{cp}\boldsymbol{I}_{abc} \tag{2.24}$$

In the case of VOC, (2.24) can be used directly to control AC signals as DC quantities in a *dq* synchronous reference frame. Afterwards, the transformation matrix in (2.23), is used to revert back to the AC domain. The goal of this entire process is to generate the desired AC signals to use as inputs in a PWM scheme.

2.3.2 Pulse Width Modulation

Previously, PWM has been described as a method of controlling the switching in an AFE rectifier. It has also been mentioned that the purpose of this is to ensure rectifier operation, by modulating the current drawn from the three phase AC source, in such a way that it stays in phase with the drawn voltage (Figure 2.11c). In VOC, this entire process is done inside a closed current control loop. Furthermore, the control loop utilizes Clarke and Park transformation to produce the necessary AC reference signals for the PWM module. Inside this module, the switching states are determined by comparing the input reference signals to triangular carrier signals. Due to the switching, the converter output current will have the shape of a pulsed waveform, with a fundamental component proportional to the reference signals. This type of PWM scheme is called Carrier Based Pulse Width Modulation (CBPWM) or sub-oscillation method [26, 35].

For simplicity, the characteristics of CBPWM can be analysed in a one phase inverter with an open loop topology. This allows for an easy presentation of the concept, by observing how PWM shapes a sinusoidal output from a DC voltage source. By picturing an arbitrary inverter with only two switches S_1 and $\overline{S}_1$, the waveforms can then be illustrated as in Figure 2.13. In this case, a sinusoidal reference signal v^* is compared to a triangular carrier signal v_{cr}. The output is

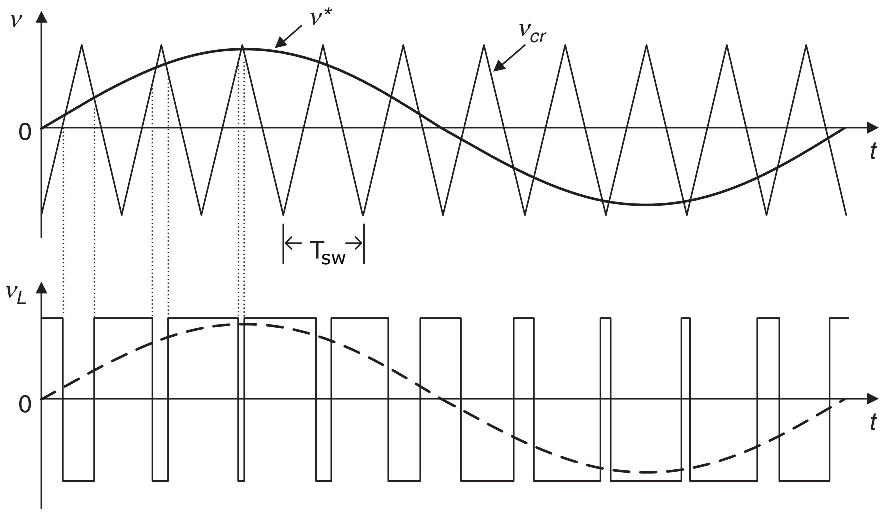


Figure 2.13: Waveforms of carrier based PWM, showing the comparison of reference signal v^* and control signal v_{cr}, with resulting output (v_L) over an arbitrary RLC load [25].

a result of this comparison, where the complimentary switches are turned on or off (never simultaneously) based on the instantaneous values of the signals. From observing the waveforms, the on/off conditions can therefore be expressed as:

$$v^* > v_{cr}, \qquad S_1 \text{ is on}$$

or

$$v^* < v_{cr}, \qquad \overline{S}_1 \text{ is on}$$

Due to the sinusoidal nature of the reference signal, the switching duty-cycle varies with the time period. This causes the pulsed output to have a varying thickness, effectively modulating a sinusoidal waveform. The smoothness of this sinusoid is dependent on the switching frequency, which is controlled by the triangular carrier signal. For a smoother sinusoidal output, the carrier frequency (f_{sw}) must therefore be increased. In practice, this increases the density of the pulsed outputs, which shapes a sinusoid resembling signal. However, the actual output can never be a perfect sinusoid, and will always contain harmonic components of the fundamental frequency f_1 [17].

The fundamental frequency of the sinusoidal output is the same as for the reference signal, i.e. f_1 is determined by v^*. The ratio between the switching frequency and

f_1 is called the frequency modulation ratio m_f, and can be expressed as [17]:

$$m_f = \frac{f_{sw}}{f_1} \tag{2.25}$$

This ratio is used to describe the harmonic output components of f_1. In the frequency domain, they appear as side-bands centred around multiples of m_f. The amplitudes of these harmonics are connected to another important term used when describing PWM, namely the amplitude modulation ratio m_a. This is the ratio between the amplitude of v^* and v_{cr}, and can be expressed as:

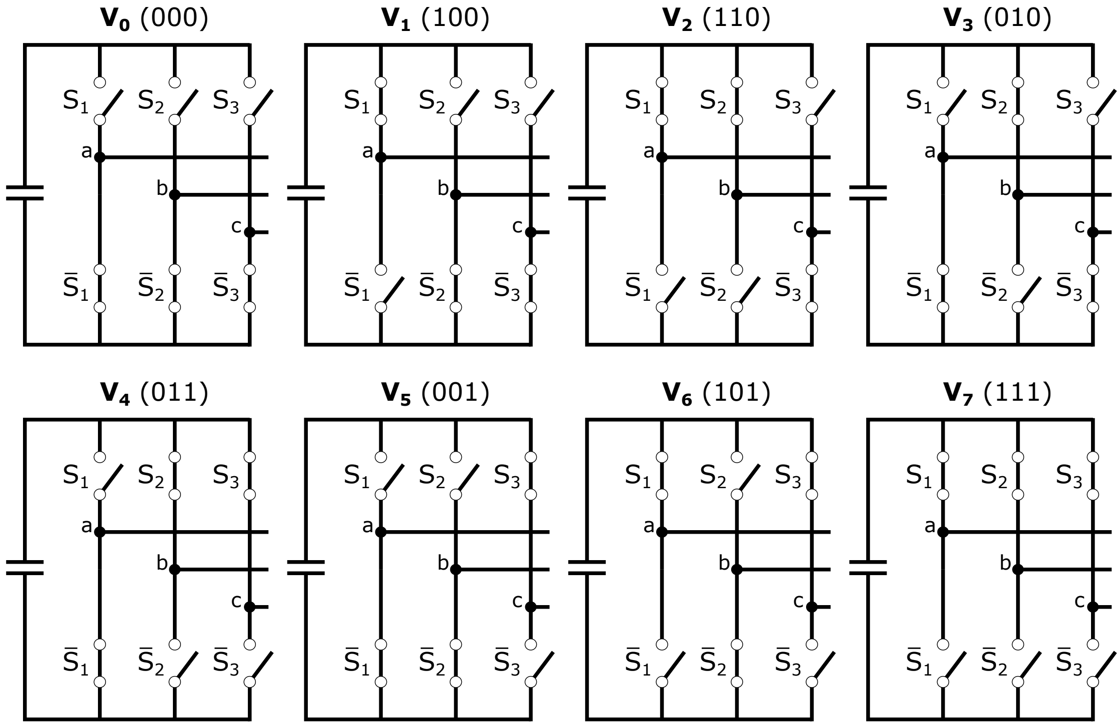
$$m_a = \frac{\hat{v}^*}{\hat{v}_{cr}} \tag{2.26}$$

By observing the waveform, it is clear that this ratio should stay $m_a \leq 1$. Otherwise, due to the reference signal having a larger amplitude than the carrier, some switching cycles will be skipped. During $m_a > 1$, the PWM is operating in the overmodulation region. This region is characterized by the non-linear relationship between the fundamental-frequency and m_a. During overmodulation, the PWM will produce more output harmonics, and if m_a is high enough, the output will degenerate to a square wave [17].

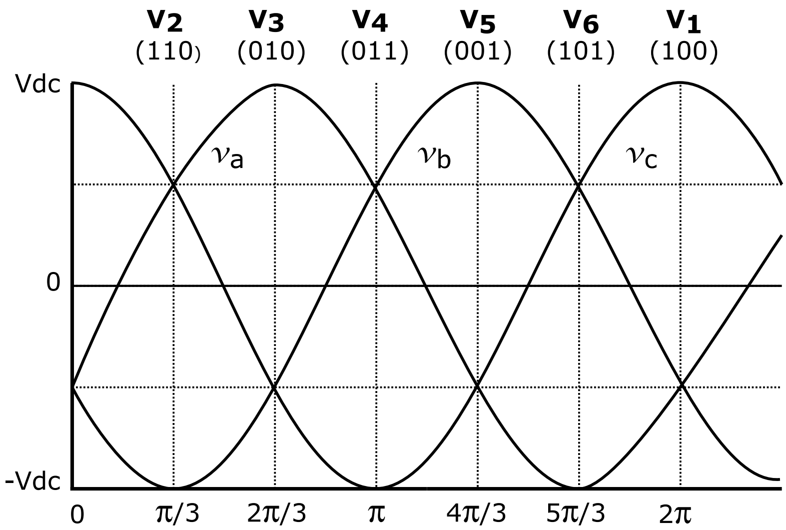
For a three phase topology, the basic principles for CBPWM remain the same. However, a more sophisticated PWM scheme is often utilized instead: Space Vector Modulation (SVM). This is due to its higher efficiency and ability to produce lower harmonics in comparison to CBPWM [36–39]. SVM is also a popular scheme to employ in VOC [40–42]. Given its superiority and wide application, it seems only natural to describe this method in more detail.

Space Vector Modulation

In SVM, the fundamental principle is based on representing each switching state in a converter as stationary space vectors, placed inside a $\alpha\beta$ reference frame. For a three phase, two level converter, there are a limited amount of switching combinations. Considering that each half bridge (also called leg) must have one switch that is on while the other is off (complementary switches), the number of possible switching combinations are: $2^3 = 8$ different combinations or specific converter states. For simplicity, an inverter is used to illustrate these states in Figure 2.14a. Every combination can be described with a three digit number, where every digit represents the on/off state of the upper switch on each arm (1 or 0). Notice that there are two combinations where the bridge won't conduct any current, (000) and (111). These two are called zero states, while the remaining six are called active states. In Figure 2.14b, the angular position of each active state can be seen in reference to a three phase cycle.



(a) The eight switching states of an three phase, two level inverter.



(b) The switching states in relative posistion to the three phase voltages $v_a(t)$, $v_b(t)$ and $v_c(t)$.

Figure 2.14: Switching states in reference to the circuit (a), and angular position (b) [43].

By knowing the angular position of each switching state, the voltages $v_a(t)$, $v_b(t)$ and $v_c(t)$ at each instant can be represented as stationary vectors by using Clarke transformation. The equation for this transformation was presented in the previous section. Equation (2.18) can in this case be applied as [25]:

$$\boldsymbol{v} = \frac{2}{3}(v_a(t) + v_b(t)e^{j2\pi/3} + v_c(t)e^{-j2\pi/3}) \tag{2.27}$$

The resulting vectors are illustrated in Figure 2.15. The zero vectors $\boldsymbol{v}_0$ and $\boldsymbol{v}_7$ are located in the origin, while the active vectors $\boldsymbol{v}_1$-$\boldsymbol{v}_6$ point outwards with an angle of 60° between them. Two adjacent vectors form a sector, giving a total of six sectors. By connecting the tip of each active vector, the resulting shape forms a hexagon. This is due to the vectors being evenly spaced, with the same maximum amplitude of $2v_{dc}/3$ [44].

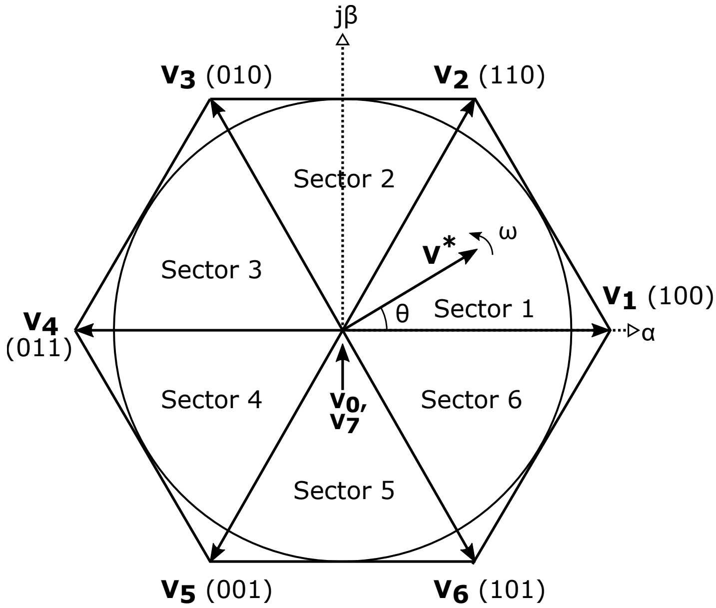


Figure 2.15: Switching states represented as stationary vectors, and $\boldsymbol{v}^*$ formed by adjecent vectors.

To rotate through one 360° cycle during a time period, each sector must be activated in sequence. This can be done by alternating between two active vectors spanning the same sector, increasing the duty cycle of the vector neighbouring the next sector, while decreasing the other. This transition can be tracked with a reference voltage $\boldsymbol{v}^*$, which rotates counter clockwise with the angular speed ω. This means that any reference vector can be synthesized using the adjacent vectors $\boldsymbol{v}_k$ and $\boldsymbol{v}_{k+1}$, of the respective sector k.[5] In practice, this is done by sampling $\boldsymbol{v}^*$ with a fixed clock frequency $2f_{sw} = 1/T_s$, where T_s is the sampling period. During sampling, the adjecent vectors are applied for a time t_k and t_{k+1}. However,

[5]For sector six the adjacent vectors will be $\boldsymbol{v}_6$ and $\boldsymbol{v}_1$

the allowable length of the reference vector is $\boldsymbol{v}^*/\sqrt{3}$ [26]. Therefore, to control the modulation index, zero vectors must be applied for a time $t_{0,7}$ during the sampling. Furthermore, the respective duty cycle for each vector is: t_k/T_s, t_{k+1}/T_s and $t_{0,7}/T_s$. To summarize, $\boldsymbol{v}^*$ and T_s can be expressed with the following equations [25]:

$$\boldsymbol{v}^* = \frac{\boldsymbol{v}_k t_k + \boldsymbol{v}_{k+1} t_{k+1} + \boldsymbol{v}_{0,7} t_{0,7}}{T_s} \tag{2.28}$$

$$T_s = t_k + t_{k+1} + t_0 \tag{2.29}$$

By defining the angle of $\boldsymbol{v}^*$ as θ^*, and θ_k as the angle of $\boldsymbol{v}_k$, application times can be expressed through trigonometric relations:

$$t_k = \frac{3T|\boldsymbol{v}^*|}{2v_{dc}}(\cos(\theta^* - \theta_k) - \frac{\sin(\theta^* - \theta_k)}{\sqrt{3}}) \tag{2.30}$$

$$t_{k+1} = \frac{3T|\boldsymbol{v}^*|}{v_{dc}} \frac{\sin(\theta^* - \theta_k)}{\sqrt{3}} \tag{2.31}$$

$$t_{0,7} = T_s - t_k - t_{k+1} = t_0 + t_7 \tag{2.32}$$

There are many variants of SVM, but (2.30), (2.31) and (2.32) are valid for all. The only difference between the various SVM techniques, is placement and duration of the zero vectors. However, the total duration of $\boldsymbol{v}_0$ and $\boldsymbol{v}_7$ must fulfil (2.32). The most common way to implement SVM, is with symmetrical zero states [26]. This implies that the remaining sampling time after one switching cycle, is distributed equally among the zero state durations. In this case, the relationship between t_0 and t_7 can be expressed as:

$$t_0 = t_7 = \frac{T_s - t_k - t_{k+1}}{2} \tag{2.33}$$

An example of SVM with symmetrical zero states is illustrated in Figure 2.16. This figure shows the relationship between vector placement, duration, and generation of gating pulses for sector one.

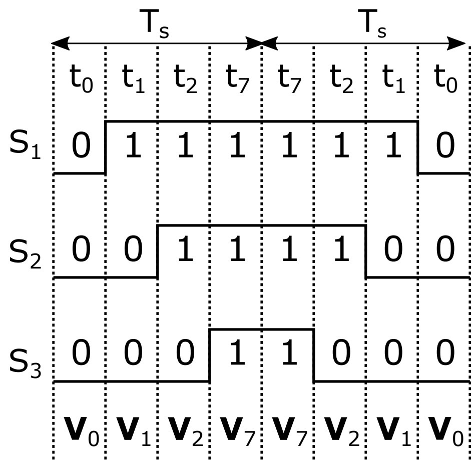


Figure 2.16: Conventional SVM with symmetrical zero states [26].

2.3.3 Voltage Oriented Control

A block diagram of VOC applied to an AFE rectifier is illustrated in Figure 2.17. The blocks labelled *abc/dq*, transform the line voltage and current measurements from the *abc* domain to the *dq* synchronous reference frame.[6] These *dq* values are then regulated by a controller with respect to the DC voltage measurement v_{dc} and reference v_{dc}^*. By utilizing feedback loops and PI regulators, the controller produces the desired control signals $\boldsymbol{v}_{dq}^* = [v_d^*, v_q^*]$. These are essentially templates for a PWM scheme. As explained in section 2.3.2, there are different PWM schemes. Therefore, depending on the scheme, $\boldsymbol{v}_{dq}^*$ must be transformed to either the $\alpha\beta$ or *abc* domain. For simplicity, the block containing a coordinate transformation and PWM module, is simply labelled "modulation". Six gating signals are produced from this block, one for each transistor. Given that current measurements are being taken continuously, the controller will adapt and produce the necessary control signals for maintaining rectification. This completes the control loop that makes up VOC. There are, however, more details concerning the controller, and the Phase Locked Loop (PLL) which has not been mentioned yet.

In Figure 2.17, a block labelled PLL can be seen connected to the voltage supply and various other blocks utilizing the Park transformation. As mentioned in the introduction, the grid measurements are to be controlled in the *dq* synchronous reference frame. For this transformation to be possible, an angle θ is needed for positioning the *dq* reference frame. However, considering that this coordinate system is continuously rotating with a fixed frequency, θ will also be constantly changing. It is therefore convenient to refer to the instantaneous angle in terms

[6]see section 2.3.1 for coordinate transformation

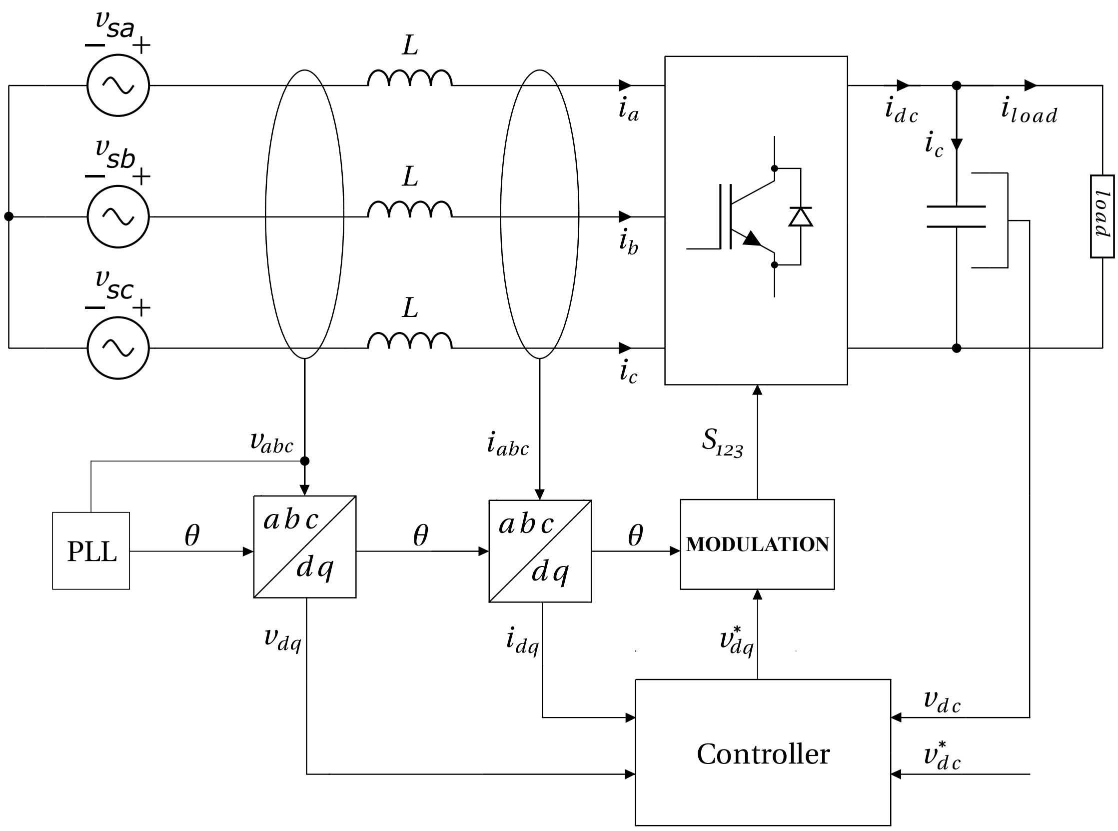


Figure 2.17: General block diagram of VOC applied to an AFE rectifier.

of angular frequency and time, so that $\omega t = \theta$. Furthermore, the PLL is used to extract this angle from the grid. More specifically, the PLL is a feedback circuit that generates a phase angle with the same angular frequency as the input signals. There are many variations of this type of circuit, but they all contain the three main components: a phase detector, loop filter, and voltage controlled oscillator [45–47]. A block diagram of a generic PLL can be seen in Figure 2.18. Due to the focus of this section, the process of each component will not be explained in detail.

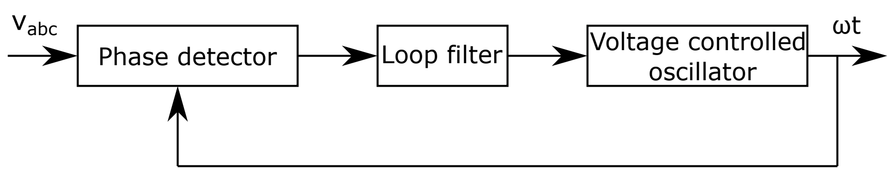


Figure 2.18: Block diagram of a generic PLL.

By using a PLL to extract the phase angle from the three phase voltage source, ωt can be used to transform the AC measurements to DC quantities. For this transformation, the previously given (2.24) can be written as:

$$\begin{bmatrix} x_d \\ x_q \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin\omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.34}$$

where $\boldsymbol{x}_{abc}$ is voltage or current. By applying the transformation to both three phase measurements, the resulting dq components can be controlled independently as $\boldsymbol{i} = [i_d, i_q]$ and $\boldsymbol{v} = [v_d, v_q]$. Both vectors are drawn inside an vector diagram in Figure 2.19. The $\alpha\beta$ coordinate system is included in the diagram as a rotational reference for the dq coordinates. Considering that the phase angle ωt is obtained from voltage measurements, the d-axis can be aligned with the voltage vector $\boldsymbol{v}$. This makes it easier to decouple the vector. The equations for v_d and v_q can then be given as in [26]:

$$v_d = L\frac{di_d}{dt} + v_d^* - \omega L i_q \tag{2.35}$$

$$v_q = L\frac{di_q}{dt} + v_q^* + \omega L i_d \tag{2.36}$$

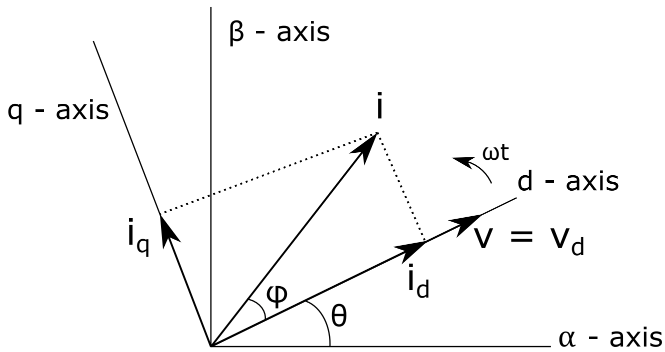


Figure 2.19: Transformed voltage and current measurements, with respective vectors $\boldsymbol{v}$ and $\boldsymbol{i}$.

To align the voltage vector with the d-axis, v_q must be set to zero so that $\boldsymbol{v} = v_d$. Furthermore, to ensure rectification with Unity Power Factor (UPF), the current vector i must be aligned with the voltage vector and d-axis. This is because of the relationship between the power and current dq components, which can be interpreted as i_d controlling the active power, and i_q determining the reactive power. It is therefore evident that i_q must be equal to 0. In reference to Figure

2.17, all these operations are done in the controller, i.e. (2.35) and (2.36) are manipulated inside a decoupled current controller. Assuming the q-axis current is regulated to zero, and voltage vector is aligned with both $\boldsymbol{i}$ and $\boldsymbol{v}$, equation (2.35) and (2.36) can be reduced to:

$$v_d = L\frac{di_d}{dt} + v_d^* \tag{2.37}$$

$$0 = v_q^* - \omega L i_q \tag{2.38}$$

A block diagram of the controller can be seen in Figure 2.20. PI regulators are used to minimize the error signals over time by adjustment of the control variables [48]. For Δv_d and Δv_q, this relationship can be expressed as:

$$\Delta v_d = k_p(i_d^* - i_d) + k_i \int (i_d^* - i_d)\, dt \tag{2.39}$$

$$\Delta v_q = k_p(i_q^* - i_q) + k_i \int (i_q^* - i_q)\, dt \tag{2.40}$$

where k_p is the proportional gain and k_i is the integral gain. The resulting control signals from the current controller can be expressed as:

$$v_d^* = v_d + \omega L i_q - \Delta v_d \tag{2.41}$$

$$v_q^* = v_q - \omega L i_d - \Delta v_q \tag{2.42}$$

2.3.4 Direct Power Control

The main principle behind DPC is to directly control the instantaneous active p and reactive q power flowing through the converter. This control scheme can be applied to an AFE rectifier as seen in Figure 2.21 [49, 50]. The switching states of the converter are selected from a table, which is, in essence, determined by the angular position of the terminal voltage vector and instantaneous power errors. To obtain these values, the power source voltages must first be calculated. However, considering that the system is without voltage sensors, an estimation technique

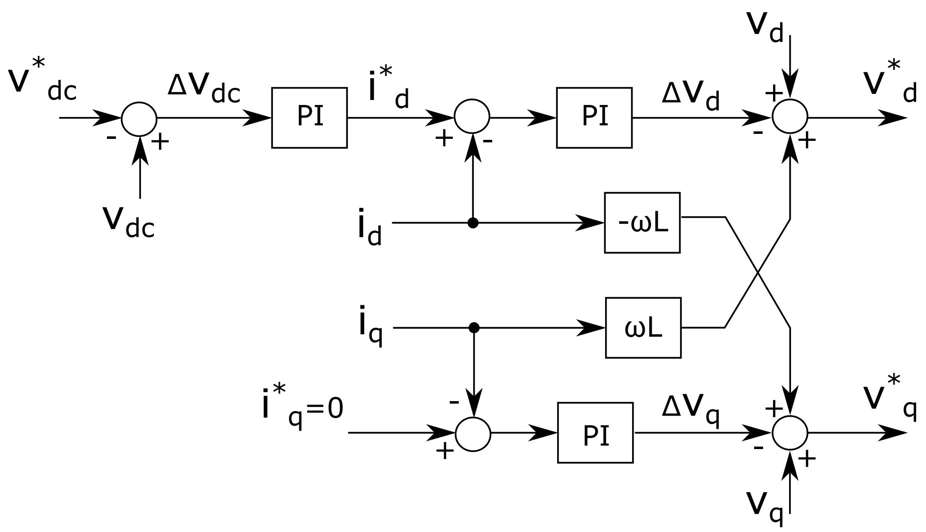


Figure 2.20: Block diagram of the current controller [26].

can be used to obtain the instantaneous power and then subsequently the line voltage in the $\alpha\beta$ domain.

The line voltages can then be given as [49]:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{1}{i_\alpha^2 + i_\beta^2} \begin{bmatrix} i_\alpha & -i_\beta \\ i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{2.43}$$

where the instantaneous active and reactive powers are given as [26]:

$$p = L(\frac{di_a}{dt} i_a + \frac{di_b}{dt} i_b + \frac{di_c}{dt} i_c) + v_{dc}(S_1 ia + S_2 i_b + S_3 i_c) \tag{2.44}$$

$$q = \frac{1}{\sqrt{3}}\{3L(\frac{di_a}{dt} i_c - \frac{di_c}{dt} i_a) - v_{dc}[S_1(i_b - i_c) + S_2(i_c - i_a) + S_3(i_a - i_b)]\} \tag{2.45}$$

The calculated power from the equations above are compared with the instantaneous reference values to produce errors. The active power reference p^* is obtained from the outer DC voltage loop while the reactive power command q^* is provided by an external signal. Furthermore, to obtain UPF, q^* is therefore set as $q^* = 0$. The error values from the comparison are quantised by hysteresis controllers as binary outputs defined as S_p and S_q. The controllers try to match the instantaneous power with the reference by limiting the error within hysteresis bands, defined as H_p and H_q. This means that the controller will give 1 as an output if the power

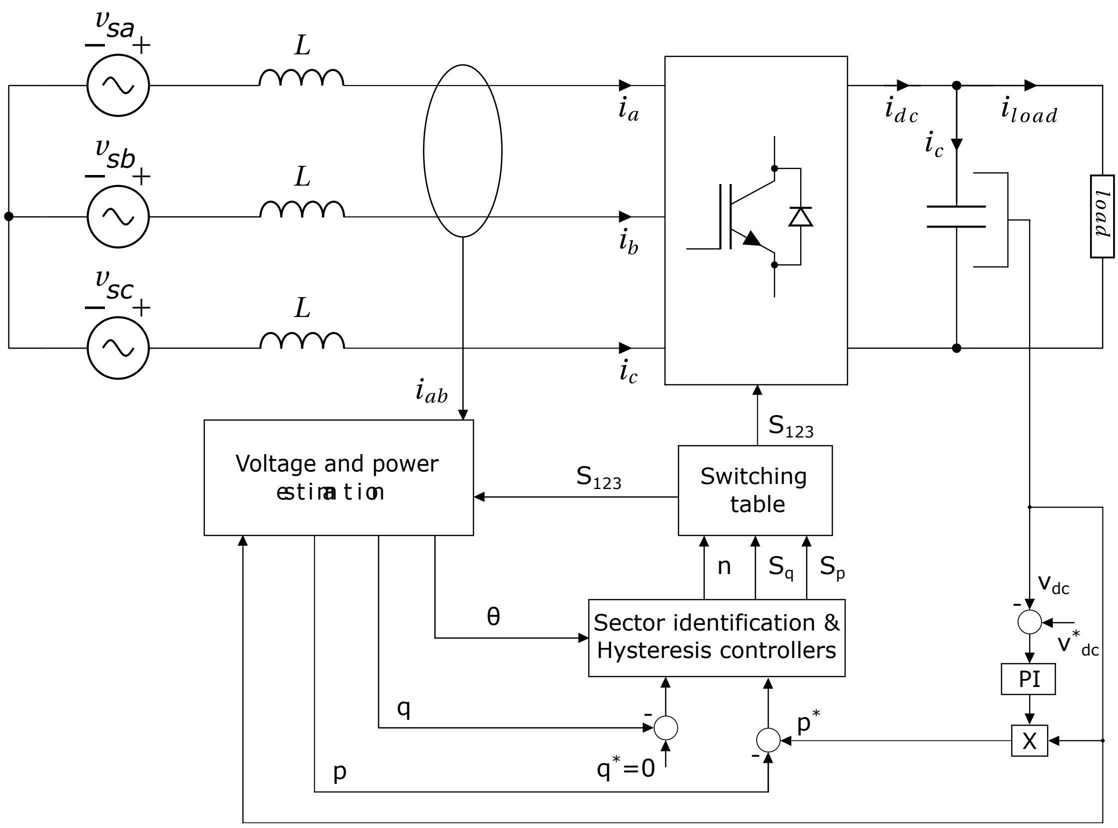


Figure 2.21: Block diagram of DPC applied to an AFE rectifier

goes beyond the lower band, or 0 if the power goes above the higher band. In the case of the active hysteresis controller, this can be expressed as:

$$S_q = \begin{cases} 1, & q < q^* - H_q \\ 0, & q > q^* + H_q \end{cases} \tag{2.46}$$

For the reactive hysteresis controller the binary states can similarly be given as:

$$S_p = \begin{cases} 1, & p < p^* - H_p \\ 0, & p > p^* + H_p \end{cases} \tag{2.47}$$

The hysteresis controller outputs are combined with the angle $\theta = \arctan(u_\alpha/u_\beta)$, of the terminal voltage vector to determine the switching state. More specifically, the region of the voltage vector is divided into twelve sectors, and θ is used to identify which sector the vector is positioned in. The respective angular region for each sector can be expressed as:

$$(n-2)\frac{\pi}{6} \leq \theta_n < (n-1)\frac{\pi}{6}, \qquad n = [1, 12] \tag{2.48}$$

2.4 Harmonic Distortion

In power systems, disturbances are generally caused by loads without linear voltage/current characteristics (non-linear loads). Some examples of non-linear loads are transformers, rotating electric machines and all equipments with built in switching devices [51]. The reason such loads cause disturbances, is because they draw a deformed sinusoidal current (non-sinusoidal). This current is essentially a composite of harmonic waveforms, which are multiples of the fundamental frequency f_1. In other words, harmonics are higher frequency waveforms superimposed on f_1, and can therefore be expressed as:

$$f_h = f_1 \cdot h, \qquad h \in \mathbb{R}^+ \tag{2.49}$$

where h denotes the harmonic order. In a non-sinusoidal current, the summation of different harmonic components constitutes the distortion. Depending on the order, these harmonics can have a varying detrimental effect on electrical equipment and power systems [52–54]. Some categories of harmonics are: triplen harmonics, inter-harmonics, and sub-harmonics. The order of triplen harmonics are odd multiples of the third harmonic ($h = 3, 9, 15, ...$) and can cause overloading of the neutral wire in grounded-wye systems. If the harmonic order is not an integer multiple of the fundamental frequency, it is called an inter-harmonic. This type of harmonic can cause flicker, temperature rise, and malfunctioning of protective relays [55]. The rarest form of harmonics found in power systems are sub-harmonics. These can have a frequency which is below the fundamental frequency and can cause voltage modulation with visual flicker [56]. A current or voltage waveform can, to some degree, contain all these categories (and others) of harmonics.

A non-sinusoidal waveform can contain a whole spectre of different harmonics. It is therefore practical to use the common term Total Harmonic Distortion (THD), for describing the harmonic content of a distorted waveform. More specifically, THD is a percentage measure of the ratio between the RMS amplitude of a set of higher harmonic frequencies to the RMS amplitude of the fundamental frequency [57, 58]. An equation for this relationship can be derived by using Fourier analysis.

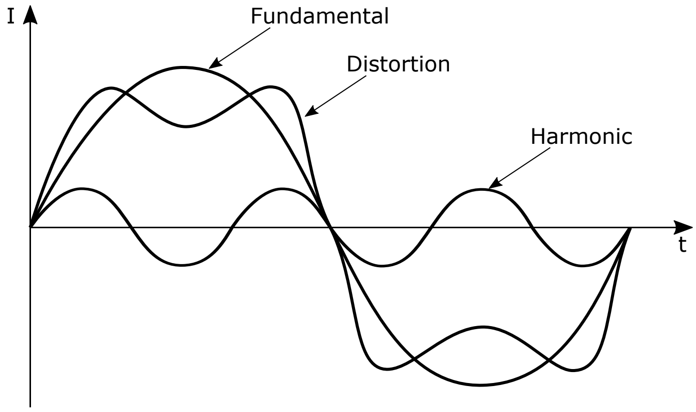


Figure 2.22: The effect of harmonic distortion.

Furthermore, any repeating waveform $f(t)$ that satisfies the Dirichlet conditions can be expressed with the following Fourier expansion [59]:[7]

$$f(t) = a_0 + \sum_{h=1}^{\infty} [a_h \cos(h\omega t) + b_h \sin(h\omega t)] \tag{2.50}$$

where ω is the angular frequency. The average value a_0, and Fourier coefficients a_h and b_h can be given as:

$$a_0 = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\, dt$$

$$a_h = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \cos(h\omega t)\, dt \tag{2.51}$$

$$b_h = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \sin(h\omega t)\, dt$$

By using a known trigonometric identity,[8] (2.50) can be expressed as:

$$f(t) = a_0 + \sum_{h=1}^{\infty} \sqrt{a_h^2 + b_h^2} \sin(h\omega t + \arctan(\frac{a_h}{b_h})) \tag{2.52}$$

[7]Dirichlet conditions must be met for a repeating function to be equal to the sum of its Fourier series at each point where it is continuous

[8]Sum of sines: $a \times \sin(\omega t) + b \times \cos(\omega t) = \sqrt{a^2 + b^2} \sin(\omega t + \arctan(\frac{b}{a}))$

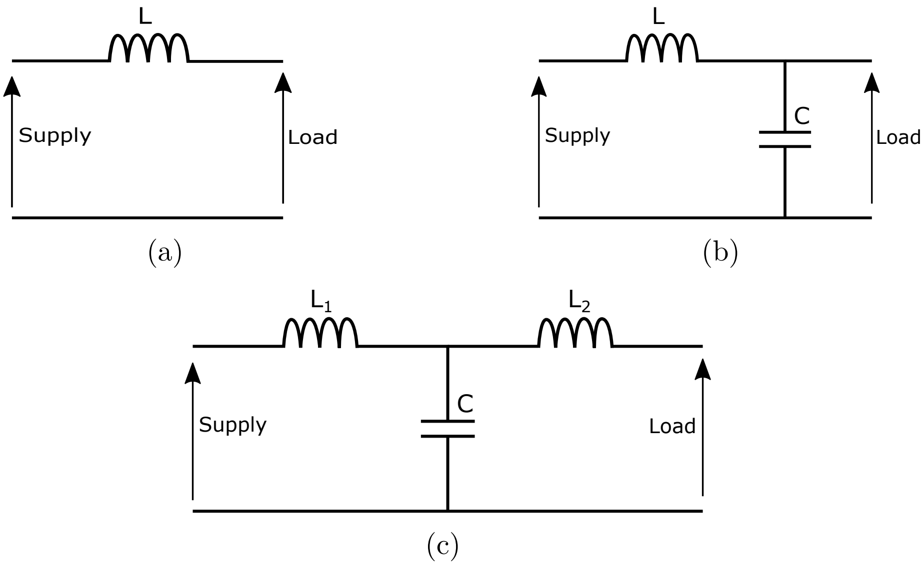


Figure 2.23: Three topologies of a passive filter: L (a), LC (b) and LCL (c).

The RMS value of an arbitrary waveform can then be calculated as:

$$F_{RMS} = \sqrt{a_0^2 + \sum_{h=1}^{\infty} \frac{a_h^2 + b_h^2}{2}} \tag{2.53}$$

By using the equation above, an expression for THD can now be formulated as:

$$\text{THD} = \sqrt{\frac{F_{RMS}^2 - F_{1,RMS}^2}{F_{1,RMS}^2}} \tag{2.54}$$

where $F_{1,RMS}$ is the RMS value of the fundamental signal. It is also worth noting that the DC component (a_0) is usually zero when calculating THD [59].

Due to the detrimental effects of harmonic distortion, a filter is usually connected between the grid and non-linear load to attenuate harmonics. Depending on the application and format of the signal, one can choose from many different filters [60]. The most simple and cheapest configuration consists of only passive elements, such as resistors, inductors, and capacitors. This makes the passive filter a preferred choice for use in power converters [61]. There are mainly three topologies for passive filters: L, LC, and LCL, as seen in Figure 2.23. It is also possible to include a resistor in the topology for damping purposes, e.g, reducing the peak resonance frequency [62]. However, adding a resistor will naturally lead to higher power loss.

The topology determines the size and cost of the filter. For a LCL filter the required inductance and capacitance is lower compared to the other topologies. This makes it the least bulkiest and expensive choice, which also makes it the preferred topology for passive filters [63]. The only drawback is resonance peaks, which can be mitigated by connecting a resistor in series or parallel with the capacitor.

3 Design and Simulation

Based on the theory presented in the previous chapter, this chapter serves to give the design methodology for the proposed rectifier and also presents results from simulations conducted under various load conditions.

3.1 Proposed Topology

From the comparison presented in section 2.2.4, it is evident that an AFE rectifier is needed for bidirectional flow. This also means that controllable switches are needed in combination with an appropriate control scheme for PWM. As described in section 2.3, the most popular control schemes are VOC and DPC. The latter seems to be the least complicated control scheme due to fewer algorithms, such as no coordinate transformation and current control loops. However, according to various research [64–68], VOC offers lower THD and requires a lower sampling frequency, which makes it cheaper to implement. The research also states that DPC is prone to high estimation errors. This makes VOC not only cheaper, but also more reliable. For these reasons, VOC is the preferred control scheme for this thesis, and can be seen implemented in the proposed topology below.

The proposed topology in Figure 3.1 shows a VOC configured AFE rectifier. This topology is more detailed but somewhat similar to the one presented previously in Figure 2.17. There are, however, some major differences in filter structure and PWM. In the proposed topology, a LCL filter is used to mitigate harmonics, and SVM is used as the PWM scheme. This will ensure smaller inductors, lower THD, higher efficiency and better utilization of the DC bus voltage. The only disadvantage is the complexity of the resulting control scheme and possible instability due to filter resonance. To reduce the risk of instability, resonance can be damped by placing a resistance in series with the capacitor, also called passive damping. Another method is to use active damping techniques, which uses feedback-loops to control the oscillations [69]. Nevertheless, it is still possible to obtain stability without passive or active damping [70, 71]. Considering the losses associated with damping resistors and the complexity of active damping algorithms, it can also be advantageous to design the filter without any damping. With this in mind, the LCL filter used in the proposed topology is therefore without damping.

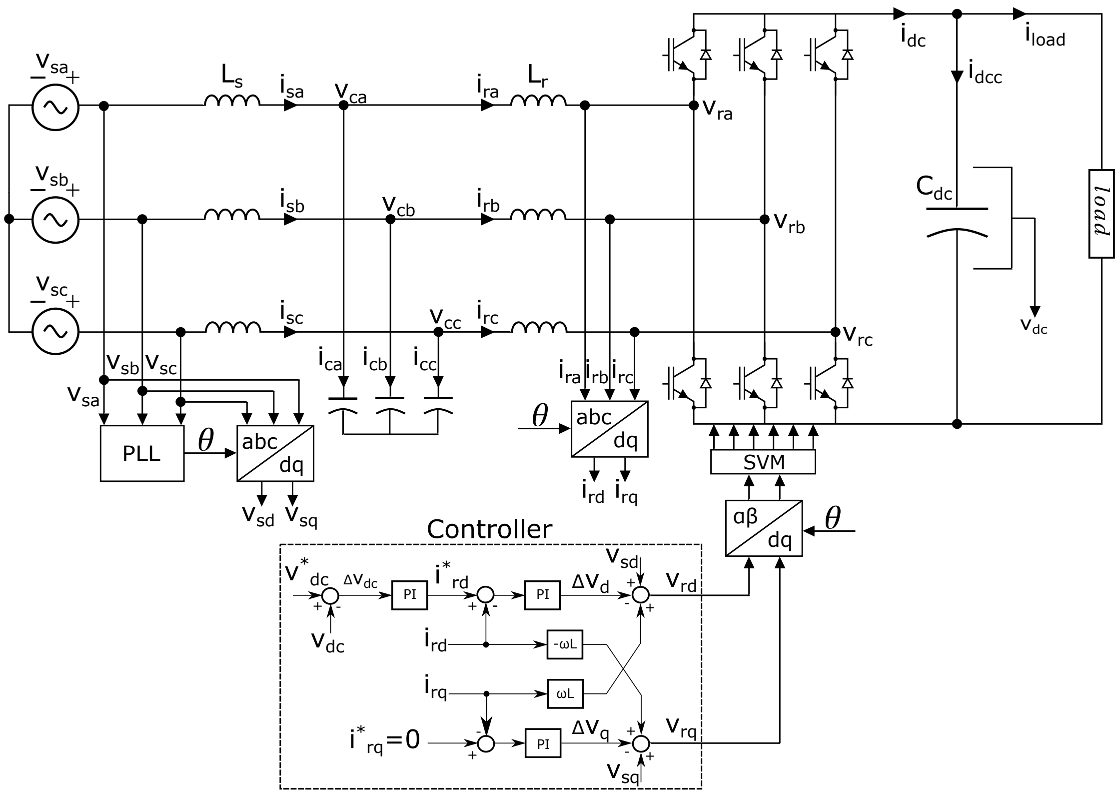


Figure 3.1: Proposed topology of the rectifier.

3.1.1 Mathematical Model

By assuming an ideal and balanced three phase system, where $i_{sa} + i_{sb} + i_{sc} = 0$, the grid voltages and currents can be defined as:

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = V_{sm} \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t - \frac{2\pi}{3}) \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = I_{sm} \begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t + \frac{2\pi}{3} + \phi) \\ \cos(\omega t - \frac{2\pi}{3} + \phi) \end{bmatrix} \tag{3.2}$$

where V_{sm} and I_{sm} are amplitude values, and $\omega = 2\pi f_g$ is the angular frequency of the grid. The frequency of the grid is defined as f_g.

A single phase equivalent circuit of the rectifier can be seen in Figure 3.2, where the grid voltage is defined as $\boldsymbol{v}_s = [v_{sa}, v_{sb}, v_{sc}]$ and current defined as $\boldsymbol{i}_s = [i_{sa}, i_{sb}, i_{sc}]$. The converter side voltage and current are similarly defined as $\boldsymbol{v}_r = [v_{ra}, v_{rb}, v_{rc}]$

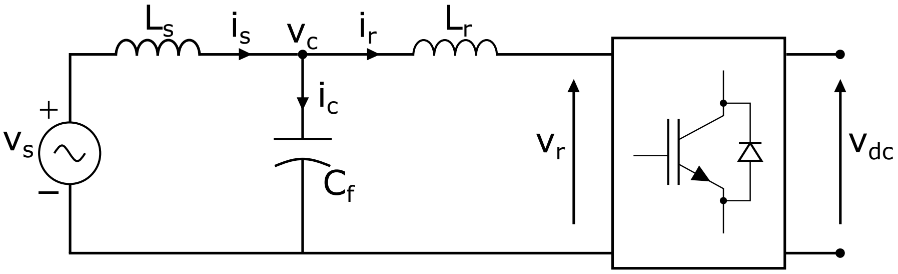


Figure 3.2: Single phase equivalent circuit.

and $\boldsymbol{i}_r = [v_{ra}, v_{rb}, v_{rc}]$, respectively. Finally, by also defining the filter capacitor voltage as $\boldsymbol{v}_c = [v_{ca}, v_{cb}, v_{cc}]$, general voltage equations for the rectifier can then be derived with KVL:

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = L_s \frac{d}{dt} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} + L_r \frac{d}{dt} \begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} + \begin{bmatrix} v_{ra} \\ v_{rb} \\ v_{rc} \end{bmatrix} \tag{3.3}$$

$$\boldsymbol{v}_s = \frac{d\boldsymbol{i}_s}{dt} L_s + \frac{d\boldsymbol{i}_r}{dt} L_r + \boldsymbol{v}_r \tag{3.4}$$

Furthermore, the currents can be expressed as:

$$C_f \frac{d\boldsymbol{v}_c}{dt} = \boldsymbol{i}_s - \boldsymbol{i}_r \tag{3.5}$$

$$C_{dc} \frac{dv_{dc}}{dt} = S_1 i_{ra} + S_2 i_{rb} + S_3 i_{rc} - i_{load} \tag{3.6}$$

Clarke and Parke transformation – as presented in section 2.3.1 – is used to transform three phase grid voltages and currents into the rotating dq reference frame. Coupled equations can then be derived with respect to the filter [72]:

$$L_s \frac{d\boldsymbol{i}_s^{dq}}{dt} = \boldsymbol{v}_s^{dq} - \boldsymbol{v}_c^{dq} \pm \omega L_s i_s^{dq} \tag{3.7}$$

$$C_f \frac{d\boldsymbol{v}_c^{dq}}{dt} = \boldsymbol{i}_s^{dq} - \boldsymbol{i}_c^{dq} \pm \omega C_f \boldsymbol{v}_c^{dq} \tag{3.8}$$

$$L_r \frac{d\boldsymbol{i}_r^{dq}}{dt} = \boldsymbol{v}_c^{dq} - \boldsymbol{v}_r^{dq} \pm \omega L_r \boldsymbol{i}_r^{dq} \tag{3.9}$$

For designing the decoupled current controller, a L approximation of the LCL filter is used [73, 74]. This makes it easier to decouple the dq components and manipulate them inside the controller. Therefore, by neglecting the filter capacitor and defining the total inductance as $L_t = L_s + L_r$, simplified voltage equations for v_{sd} and v_{sq} can be written as:

$$v_{sd} = L_t \frac{di_{rd}}{dt} - \omega L_t i_{rq} + v_{rd} \tag{3.10}$$

$$v_{sq} = L_t \frac{di_{rq}}{dt} + \omega L_t i_{rd} + v_{rq} \tag{3.11}$$

The relationship between the voltage and current vectors is described in section 2.3.3 and can be seen placed inside a diagram in Fig 2.19. The dq reference frame is rotating synchronously with the grid phase angle ω and has its d-axis aligned with the line voltage vector so that $\boldsymbol{v}_s = v_{sd}$. Simplified equations for the injected or absorbed grid power can therefore be derived as:

$$P = \frac{3}{2} v_{sd} \cdot i_{rd} \tag{3.12}$$

$$Q = \frac{3}{2} v_{sd} \cdot i_{rq} \tag{3.13}$$

From the equations above, it is apparent that the control of active and reactive power is reduced to controlling the d and q components of the current $\boldsymbol{i}_r^{dq}$. For this purpose, PI controllers are used to control the DC voltage error and also drive the q-axis converter current to zero, so that $\boldsymbol{i}_r^{dq}$ is aligned with $\boldsymbol{v}_s^{dq}$ and UPF is achieved. With regard to the L approximation, the decoupled control equations are in essence identical to (2.41)-(2.42), and can be rewritten as:

$$v_{rd} = v_{sd} - \Delta v_d + \omega L_t i_{rq} \tag{3.14}$$

$$v_{rq} = v_{sq} - \Delta v_q - \omega L_t i_{rd} \tag{3.15}$$

Similarly, equations for the PI output signals for the current controllers, as given previously in (2.39)-(2.40), can be rewritten as:

$$\Delta v_d = k_p(i_{rd}^* - i_{rd}) + k_i \int (i_{rd}^* - i_{rd})\, dt \tag{3.16}$$

$$\Delta v_q = k_p(i_{rq}^* - i_{rq}) + k_i \int (i_{rq}^* - i_{rq})\, dt \tag{3.17}$$

The PI gains K_p and K_i are tuned by trail and error. There also exist other tuning methods: *modulus optimum* and *symmetrical optimum* [75]. However, these are only valid when modelling the controller in the frequency domain and only give broad indicators for gains that might be stable given ideal conditions. These methods are therefore not be implemented nor presented. Although no concrete tuning method is used, the current loop is tuned to achieve a faster response than the outer voltage loop, as is common practice for cascade control.

3.1.2 Filter Design

The filter design methodology is mainly based on [71], and aims to achieve stable operation without damping for a PI-based current controlled converter. It also takes into account variations in grid inductance, accuracy of capacitor standard values and inductor saturation. Resonance problems are avoided by tuning the filter parameters to a stable frequency region, where no damping is required. However, considering that variations in grid inductance are taken into account, there will be a range of possible resonance frequencies which vary as a function of the grid inductance and filter capacitance. This range is constrained by the frequency of the grid f_g and switching f_{sw}. An expression for the resonance frequency f_{res} can be given as:

$$f_{res} = \frac{\sqrt{\omega_{res}}}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{L_s + L_r}{L_s L_r C_f}} \tag{3.18}$$

Furthermore, as derived in [71], the stable region is given by:

$$10 f_g < \frac{f_{sw}}{6} < \frac{1}{2\pi}\sqrt{\frac{L_r + L_{s\max}}{L_{s\max} L_r C_{f\max}}} \leq f_{res}(L_s, C_f) \leq \frac{1}{2\pi}\sqrt{\frac{L_r + L_{s\min}}{L_{s\min} L_r C_{f\min}}} < \frac{f_{sw}}{2} \tag{3.19}$$

For the best possible dynamics, the total inductance should be as small as possible.

Therefore, the total inductance is limited to 0.1 pu of the base impedance. The maximum filter inductance can then be expressed as:

$$L_{t\max} = 10\% \frac{V_{LL}^2}{2\pi f_g P} \tag{3.20}$$

where V_{LL} is the line to line RMS grid voltage, and P is the rated active power of the system. Generally, no more than five precent of P should be consumed by the filter capacitor as reactive power. This constraint can be used to calculate the maximum filter capacitance:

$$C_{f\max} = 5\% \frac{P}{2\pi f_g V_{LL}^2} \tag{3.21}$$

For tuning the filter capacitor, it is recommended to start with a value of $0.5C_{f\max}$ and then gradually increase the filter capacitance to $C_{f\max}$. For tuning the converter side inductor, the inductance must be large enough to attenuate the maximum switching ripple current Δi_{max}, and also avoid saturation. The relationship between $\Delta i_{\max}$ and minimum converter side inductance $L_{r\min}$ can be given as:

$$L_{r\min} = \frac{V_{dc}}{6 f_{sw} \Delta i_{\max}} \tag{3.22}$$

To avoid saturation problems, the converter side current must not exceed the rated inductor saturation current I_{sat}. This relationship can be expressed as:

$$\left| I_{rm} + \frac{\Delta i_{\max}}{2} \right| < I_{\text{sat}} \tag{3.23}$$

where, during high frequencies, the maximum converter side current I_{rm} can be given as:

$$I_{rm} = I_{sm} = \sqrt{\frac{2}{3}} \frac{P}{V_{LL}} \tag{3.24}$$

The minimum converter side inductance can then be expressed with respect to the saturation current and maximum converter side current:

$$L_{r\min} > \frac{V_{dc}}{12 f_{sw}(I_{\text{sat}} - I_{rm})} \tag{3.25}$$

For tuning the grid side filter inductance, an attenuation constant δ must be selected first. This constant represents the relationship between the converter and grid current at the switching frequency, and can be given as:

$$\delta = \left|\frac{i_s}{i_r}\right|_{sw} = \frac{1}{|1 + a(1 - L_r C_f \omega_s^2)|} \tag{3.26}$$

$$a = \frac{1+\delta}{\delta a_1} \tag{3.27}$$

where $a_1 = L_r C_f \omega^2 - 1$. The attenuation ratio is proportional to THD, which means that current harmonics can be substantially reduced with a low δ. However, to avoid resonance problems, δ should meet the following conditions:

$$\delta < \frac{36L_r - (2\pi f_{sw} L_r)^2 C_{f\max}}{a_3(2\pi f_{sw})^2 - 36a_2} \tag{3.28}$$

$$\delta < \frac{36L_r - (2\pi f_{sw} L_r)^2 C_{f\max}}{a_3(2\pi f_{sw})^2 - 36a_2} \tag{3.29}$$

$$\delta > \frac{1}{|1 + a_{\max} a_1|} \tag{3.30}$$

where $a_2 = L_r + a_1 L_{s\max} + a_1 L_r$, $a_3 = (L_r + a_1 L_{s\max}) L_r C_{f\max}$, $b_2 = L_r + a_1 L_{s\min} + a_1 L_r$, $b_3 = (L_r + a_1 L_{s\min}) L_r C_{f\min}$ and $a_{\max} = \frac{L_{t\max}}{L_r} - 1$. If the selected attenuation rate fulfils all the conditions, the grid side inductor can be calculated with the equation:

$$L_s = aL_r = \frac{L_r(1+\delta)}{\delta a_1} \tag{3.31}$$

3.1.3 Phase Locked Loop

A synchronous reference frame PLL is used to extract the phase angle from the grid. The PLL employs a conventional control algorithm which is based on driving the q component of the transformed voltage to zero [76–78]. v_{sq} is in this case therefore an error value. A PI controller is used to reduce the error inside a feedback loop. The control signal $\Delta\omega$ is summed with the angular centre frequency ω_c in radians per second, and then integrated to produce the instantaneous angle. To avoid a continuously increasing ramp, cosine is used to wrap the angle at 2π, subsequently producing a sawtooth signal instead. A block diagram of the specified PLL can be seen in Figure 3.3.

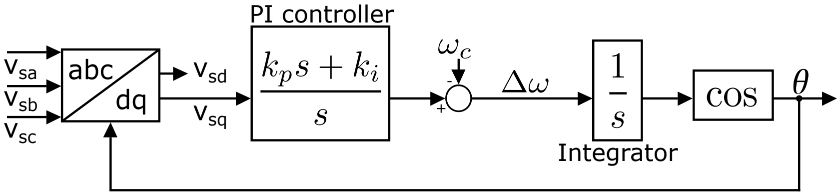


Figure 3.3: Topology of the synchronous reference PLL.

The TF of the PI controller can be given as:

$$G_c(s) = \frac{k_p s + k_i}{s} \tag{3.32}$$

A closed loop TF can be derived from the open loop expression as:

$$G_{OL}(s) = \frac{V_{sm}(k_p s + k_i)}{s^2} \tag{3.33}$$

$$G_{CL}(s) = \frac{V_{sm}(k_p s + k_i)}{s^2 + V_{sm}k_p s + V_s k_i} \tag{3.34}$$

To design the controller, an expression for the gains k_p and k_i can be derived from comparing the closed loop TF to the standard form expression of the following second order system:

$$G_{CL}(s) = \frac{V_{sm}(k_p s + k_i)}{s^2 + V_{sm}k_p s + V_s k_i} = \frac{k\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.35}$$

$$\implies \quad k_i = \frac{\omega_n^2}{V_{sm}} \quad \wedge \quad k_p = \frac{2\zeta\sqrt{V_{sm}k_i}}{V_{sm}} \tag{3.36}$$

where ω_n^2 is the natural frequency, and ζ is the damping ratio.

3.1.4 DC Bus

The rated DC capacitor voltage must be large enough to store the rectified voltage, and also large enough to be utilized by the SVM scheme. To calculate the maximum rectified voltage, an L approximation of the LCL filter can be used for fundamental signals. The filter capacitor is designed to have an impedance for fundamental signals. Therefore, neglecting the filter capacitor, and approximating the total inductance to L_t, the maximum rectifier side voltage can be given as [71]:

$$V_{rm} = \sqrt{V_{sm}^2 + (L_t \omega I_{sm})^2} \tag{3.37}$$

With respect to SVM, the minimum DC voltage can be calculated as:

$$V_{dc\mathrm{min}} = \sqrt{3} V_{rm} \tag{3.38}$$

Aside from system parameters, such as line voltage and rated power, the capacitance is mainly determined by the acceptable ripple voltage ΔV_{dc} and desired switching frequency. Therefore, if ΔV_{dc} and f_{sw} are known, the minimum capacitance can be defined as [79]:

$$C_{dc\mathrm{min}} = \frac{P(\sqrt{2}V_{dc} + \sqrt{3}V_{LL})}{2\sqrt{3}V_{LL}V_{dc}\Delta V_{dc} f_{sw}} \tag{3.39}$$

3.2 Simulation Model

The MATLAB® based application Simulink® is used to construct the complete rectifier system in a block diagram environment. In this environment, simulations can be conducted in the continuous or discrete domain. A sample time of 1 μs is chosen to solve the differential equations for the electrical circuit. This sample time is only set inside the powergui block. For the simulation solver, as found in the configuration parameter settings, a variable step solver is chosen to shorten the time required to simulate the model and take into account any continuous states. The sample time inside all the discrete blocks is set to -1, which indicates that the sample time is *inherited* and Simulink determines the best sample time for each block. This ensures faster execution of the algorithms and lowers the risk of instability. Although the controller must be fully discretized – preferably with a more modest sample rate – for real-time implementation with a Microcontroller Unit (MCU), this method of analysis is acceptable for the purpose of presenting the control characteristics under ideal conditions. All algorithms are implemented either textually with MATLAB functions or graphically with prebuilt Simulink blocks from the software library. An overview of the simulation model can be found in Figure 3.4.

The model is designed to provide a steady DC voltage to the load with UPF in closed loop operation, regulating for any load side variations. Simulations are therefore conducted to observer the controllers' response and overall performance during sudden load changes. Considering that the controller is depended on many different algorithms for its performance, the build-up and output of all the main subsystems are therefore also presented during steady state. These are, however, presented before the varying load simulations, separated from the section containing the main results (next section). The parameters for the simulation can be seen in Table 3.1.

Calculations for LCL filter values are conducted with an attenuation ratio of $\delta = 0.07$, and takes into account variations in grid inductance ranging from stiff grid conditions (0 mH), to weak grid conditions (13 mH). All the conditions for δ are met as according to (3.28)-(3.30). The filter is designed to limit the grid current THD percentage well below 5%, which is recommended according to IEEE standards [80]. A MATLAB script, which can be seen attached in Appendix A.1, is used to conduct the calculations and gives a warning if any of the conditions are not met. Only the LCL filter and DC bus voltage values are deduced through calculations. Other parameters, such as the DC capacitance, have been selected for more practical reasons.

Parameter	**Symbol**	**Value**	**Unit**
Rated power	P	20	kW
Grid voltage	V_{LL}	400	V
DC reference	V_{dc}^*	600	V
Grid frequency	f_g	50	Hz
Switching frequency	f_{sw}	5	kHz
Sampling rate	f_s	1	MHz
Gridside inductor	L_s	1.7	mH
Rectifier inductor	L_r	1	mH
Filter capacitor	C_f	10	μF
DC capacitor	C_{dc}	1525	μF
DC load	R_{load}	18	Ω

Table 3.1: Simulation parameters

The DC capacitance has been chosen to maintain consistency with respect to the laboratory setup presented in the next chapter. According to (3.39), the voltage ripple should be $\Delta V_{dc} = 4.86$ V. However, this does not take into account the controller and is therefore only a conservative estimate. The controller has great influence over the load-side stability and has given appropriate tuning of the voltage and current regulators, the voltage ripple will most certainly be lower during nominal conditions.

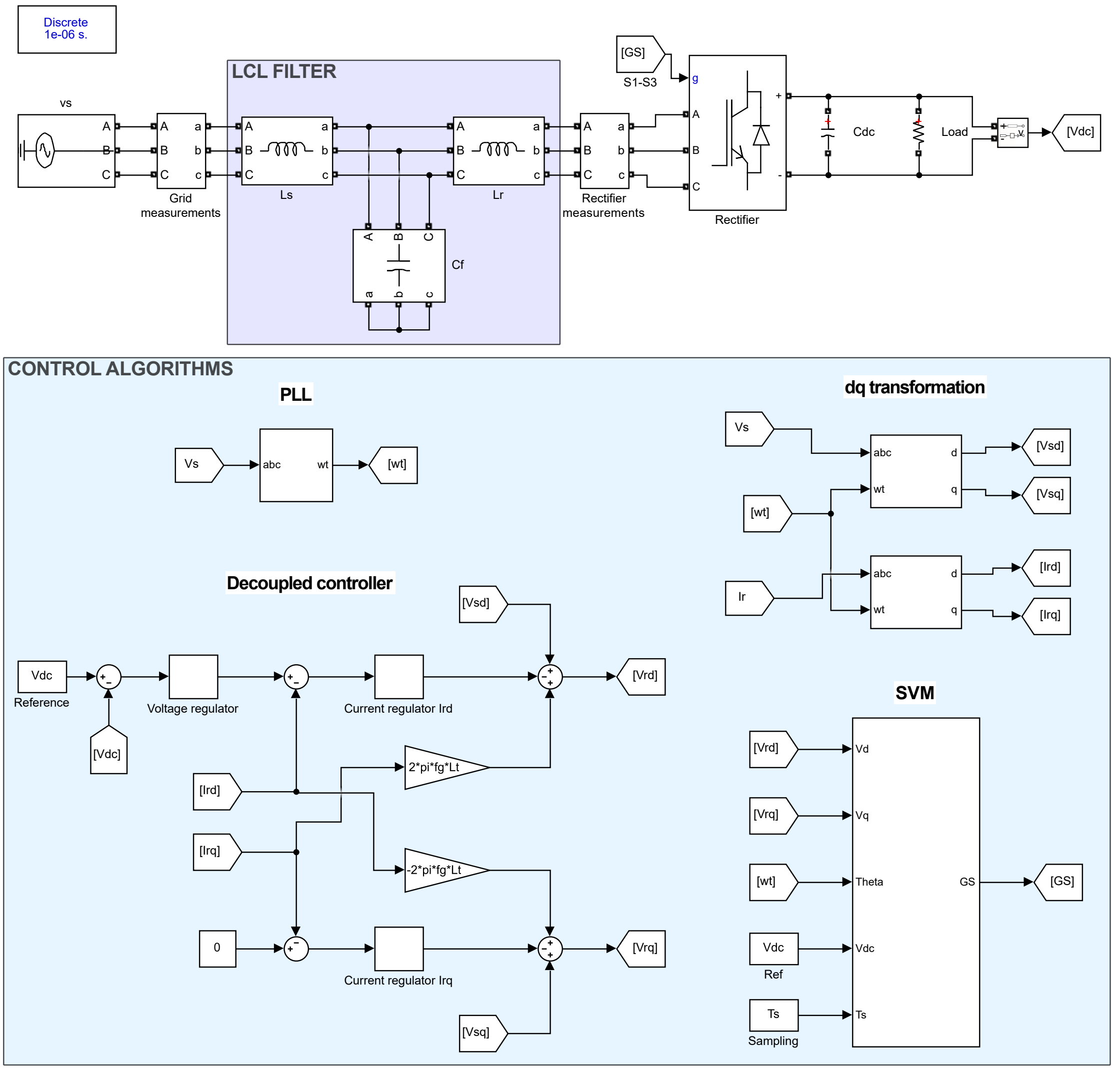
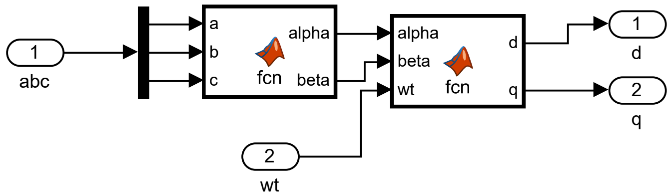


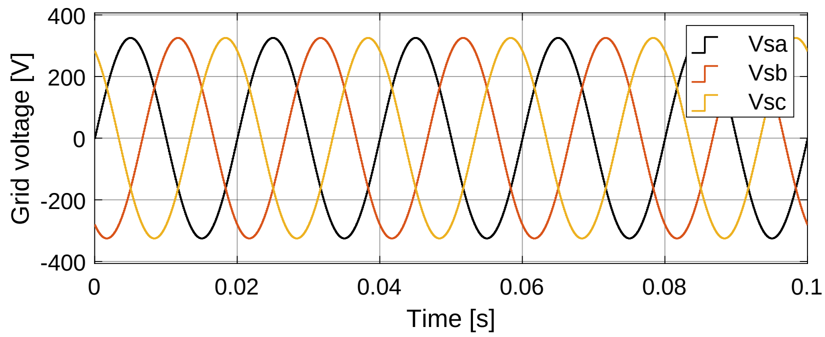
Figure 3.4: Overview of the simulation model.

3.2.1 Clarke and Parke Transformation

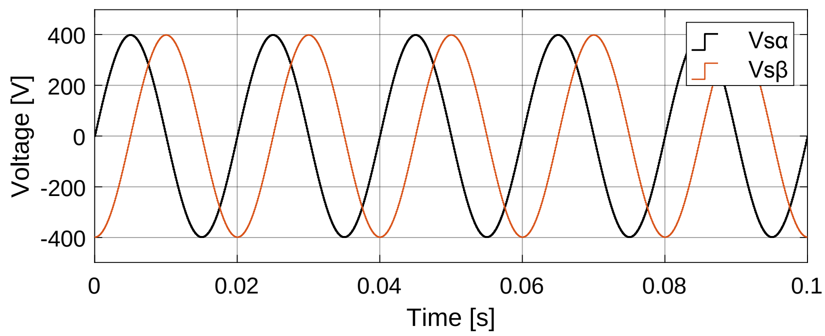
Clarke and Parke transformation is implemented with two separate MATLAB functions, one for transforming the *abc* values to the $\alpha\beta$ domain and one for further transforming the $\alpha\beta$ values to the *dq* domain. The block diagram of the system and its output during voltage transformation can be seen in Figure 3.5. The output looks similar for the current transformation. The MATLAB code is attached in Appendix A.3.



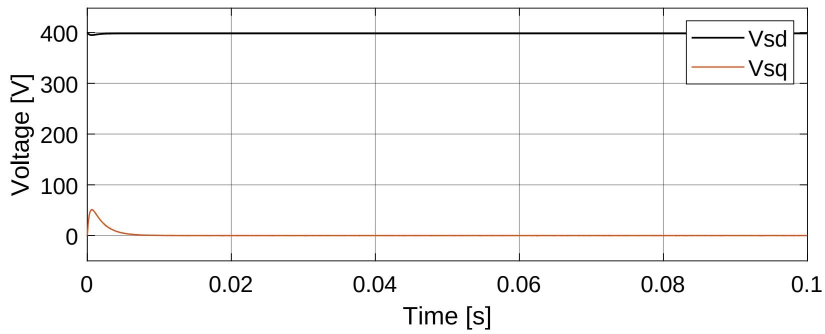
(a) Subsystem.



(b) Grid voltage in the *abc* domain.



(c) Grid voltage in stationary reference frame.

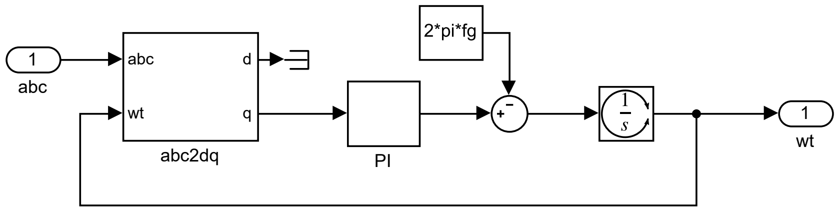


(d) DC values, as seen from a rotating reference frame.

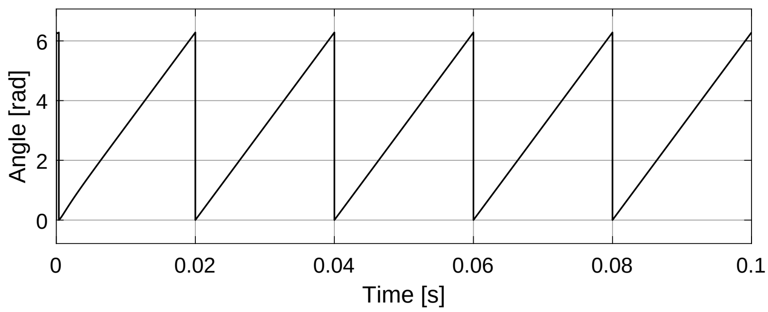
Figure 3.5: Block diagram of the system (a) responsible for coordinate transformations (b)-(d).

3.2.2 Phase Locked Loop

The phase locked loop consists of continuous states blocks and the whole subsystem can be seen modelled in Figure 3.6a. The integrator block has the function of wrapping θ around 2π. A seperate cosine block is therefore not needed. The output can be seen in Figure 3.6b, which shows a sawtooth shaped signal representing the grid phase angle varying from 0 to 2π with a frequency of 50 Hz.



(a)



(b)

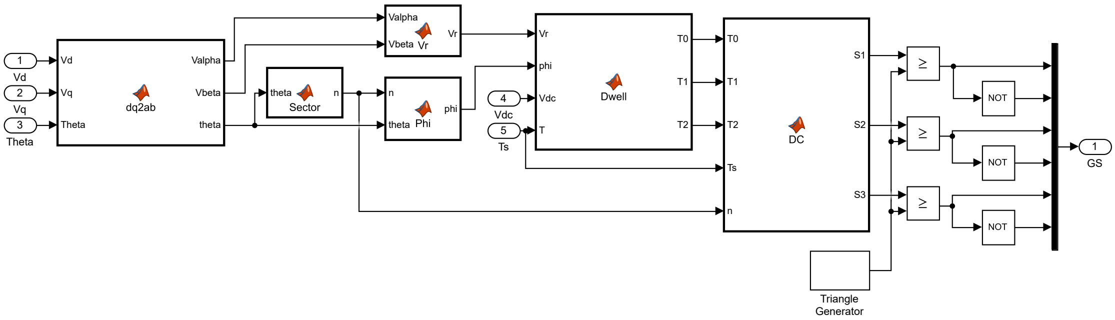
Figure 3.6: The PLL subsystem (a), and *wt* sawtooth output (b)

3.2.3 Space Vector Modulation

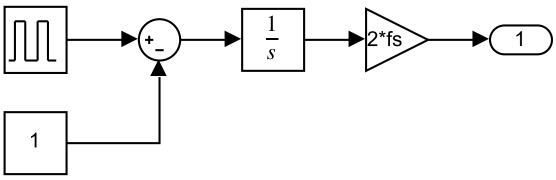
The algorithm used to execute SVM is separated into several MATLAB functions, as seen in Figure 3.7a. A short description of each function is provided to clarify the process from the *dq* inputs to the gating logic:

- dq2ab: Converts the *dq* reference voltages into the $\alpha\beta$ domain, and calculates the angle of the resulting vector sum $V_{\alpha\beta}$.
- Vr: Calculates the magnitude of $V_{\alpha\beta}$.
- Sector: Identifies the current sector in which $V_{\alpha\beta}$ lies.
- Phi: Calculates the angle between $V_{\alpha\beta}$ and its adjacent switching vector.
- Dwell: Calculates the time duration of active and zero states.
- DC: Calculates the duty cycle of each switch with respect to the sector.

The MATLAB code for each function is attached in Appendix A.2. After the duty cycles are generated, they are compared to a triangle waveform to generate the gating pulses with the desired switching frequency. To generate the triangle waveform, a pulse signal is integrated and is then scaled to give an amplitude of 1. The internal block diagram of the triangle generator can be seen in Figure 3.7b. A more in depth description on the theory behind SVM, as a general PWM scheme for inverters, was given in section 2.3.2.



(a)



(b)

Figure 3.7: Inside look at the SVM subsystem (a), and triangle generator (b).

3.2.4 Proportional Integral Control

A PI regulator is used in both the PLL and decoupled controller for reducing the error signals and producing the desired control response. The PI design used is quite simple and can be seen in Figure 3.8. In the decoupled controller, there are in total three such regulators, one in the outer voltage loop labelled: "voltage regulator", and two in the inner current loop, each labelled: "current regulator". All the proportional and integral gain values have been deduced by trail and error, as listed in Table 3.2.

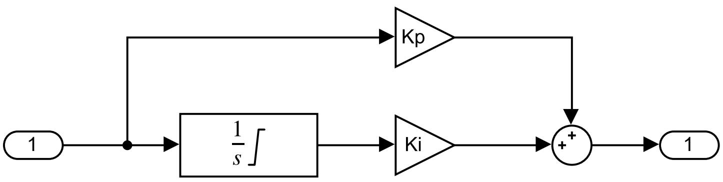


Figure 3.8: Block diagram of the PI regulator.

Regulator	**Kp**	**Ki**
Voltage	1	150
Current	1000	0
PLL	10	5000

Table 3.2: PI gains.

3.3 Simulation Tests and Results

Various tests are conducted to observe the capabilities and performance of the control system. As presented in Table 3.1, the controller is designed to maintain a steady DC voltage of 600 V, over a purely resistive load of 18 Ω. However, the controller should also be able to demonstrate some flexibility with respect to off-nominal load conditions. Some of the the tests are therefore also designed to push the system well beyond its rated power, as to observe its behaviour when transitioning from stable to unstable operation. Furthermore, the grid side voltage and current are monitored to observe the PF of the system and its bidirectional capabilities. The rectifier should be able to maintain rectification with UPF during load changes and operate as an inverter when connected to a regenerative load with higher voltage than the setpoint. There are also other interesting aspects to be observed, such as the transient response of the system during load changes and the THD_i of the grid current.

A THD_i analysis of the grid side current is included to determine the performance of the LCL filter during the different loads. Although the filter is designed to take into account some variations in grid impedance, it does not, however, take into account load side variations which can cause instability in the system and thereby increase the THD_i. The quality of the filter design is determined by its ability to filter out the switching harmonics, and under nominal conditions it is expected that the THD_i is well below the IEEE limit of 5%.

The THD_i is calculated for two cycles during each load scenario, but only when the DC voltage has reached a steady state around its setpoint. Simulink is used to conduct the THD_i analysis, which is based on a FFT algorithm that identifies all the harmonics relative to the fundamental frequency. The max frequency for THD_i computations is set to the Nyquist frequency. Only the THD_i percentage is presented in the following results. The complete FFT analysis for all the load conditions is attached in Appendix B.

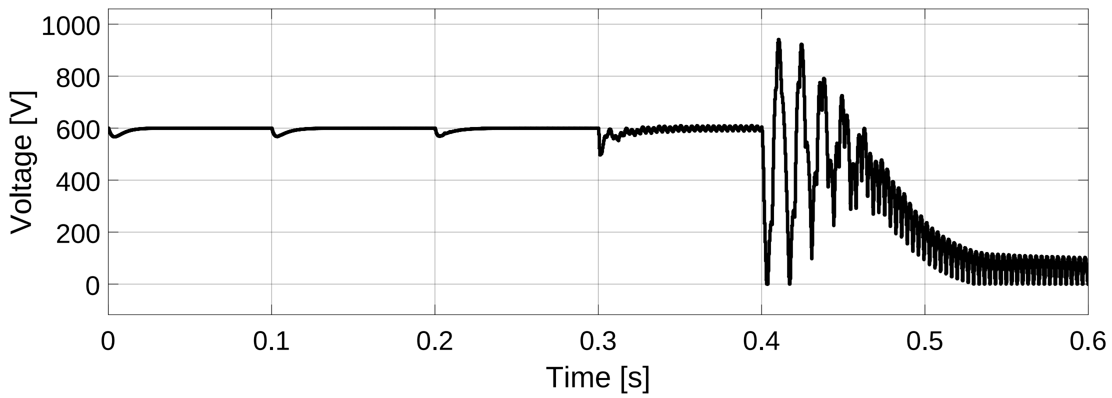
3.3.1 Rectifier Operation

In the following test, a step load is applied to the DC side of the rectifier every tenth of a second for a duration of 0.4 sec. In other words, the load is increased (from nominal) in total four times over the course of the simulation run-time, which lasts 0.6 sec. In the simulation environment, the load consists of one ideal resistor and four ideal switches, all connected in parallel. This setup can be seen in Figure 3.10. Each switch has an internal resistance, subsequently acting as a resistor when closed. The snubber resistance is in the order of megaohms and can therefore be neglected when the switch is open. The initial state of all the switches are open, making the total resistance 18 Ω at the start of the simulation. The total load applied to the rectifier with respect to time can be seen in Table 3.3. The table also gives information about the transient and steady state response of the system. These parameters are: the settling time T_{sim}, voltage drop dv, peak-to-peak DC ripple voltage v_{rip} and the THD_i of the grid current.

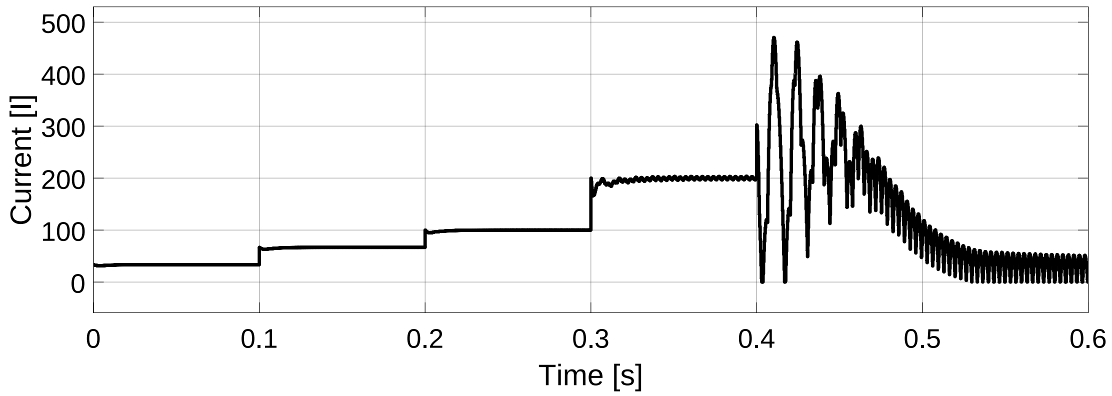
		Transient		Steady State	
$\mathbf{T_{sim}}$ [s]	$\mathbf{P_L}$ [kW]	$\mathbf{T_s}$ [ms]	**dv** [V]	$\mathbf{v_{rip}}$ [mV]	$\mathbf{THD_i}$ [%]
<0.1	20	39	33	61	0.29
<0.2	40	46	32	150	0.17
<0.3	60	49	31	362	0.13
<0.4	120	60	103	20e3	4.52

Table 3.3: Transient and steady state response during rectification.

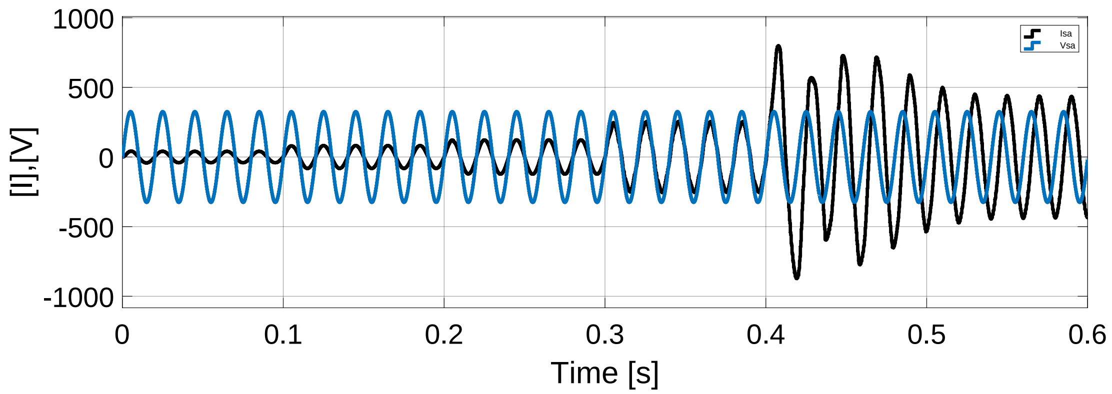
The DC output voltage and current measurements for the whole duration of the simulation can be seen in Figure 3.9a. Considering that the DC capacitor is precharged to 600 V and a load is applied at the start of the simulation, there is an initial voltage drop which the controller is able to compensate for in a matter of milliseconds. This process repeats every time the load increases until the last step load is applied at 0.4 sec. In this instance, the system becomes unstable and is unable to maintain rectification. When operating as a rectifier, the system can be defined as stable for loads not exceeding 120 kW, which corresponds to a total load current of 200 A. The transition from stable to unstable operation can also be observed in Figure 3.9c, which shows a graph depicting the relationship between the grid phase voltage (blue line) and current (black line). From this figure, it is clear that the rectifier is able to maintain rectification with UPF until the load becomes too large for the controller to handle.



(a) DC voltage.



(b) DC current.



(c) Phase voltage (blue) and respective current (black).

Figure 3.9: DC (a, b) and AC (c) measurements during rectification with an increasing step load.

In the time period spanning from the start of the simulation to 0.4 sec, the system is able to achieve a steady state without overshoot after every applied load. However, from Table 3.3 it is apparent that the transient and steady state response are worst when the load increases to 120 kW. From 20-60 kW the THD_i is well below 5% and the transient response of the system does not change substantially. Although the change is small, it is worth noting that the THD_i actually seems to decrease with increasing load up to 60 kW, as opposed to the ripple voltage, which increases substantially.

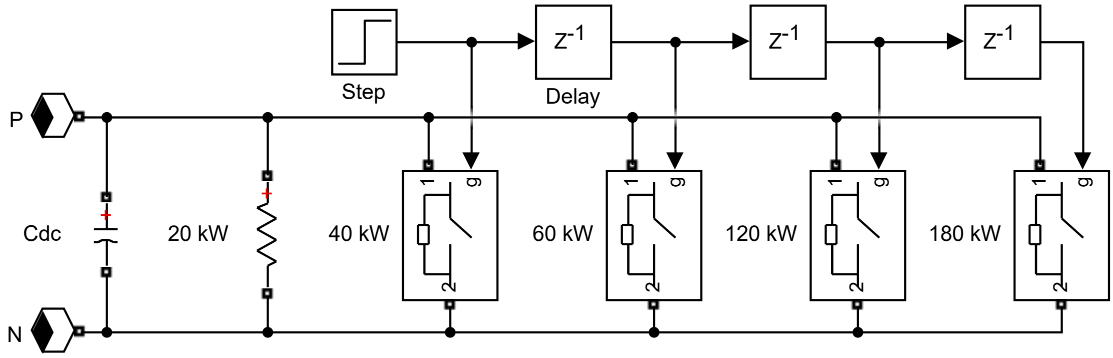


Figure 3.10: Increasing step load setup during rectification.

3.3.2 Inverter Operation

In this test, the AFE rectifier is connected to an increasing regenerative load to test its inverting capabilities and limits. The load side setup can be seen in Figure 3.11. This setup consists of a resistor connected to several ideal DC voltage sources in series, separated by switches. Similarly to the previous test setup, ideal switches are used in combination with timed step signals to increase the load every tenth of a second. Instead of a resistor, an ideal switch (labelled R) with an internal resistance of 18 Ω is used in its place. The snubber resistance and internal resistance of all other switches are negligible. The first step load is applied at the start of the simulation, connecting a 1200 V DC voltage source to the rectifier. The initial load is 20 kW, on account of the capacitor being precharged to 600 V. Staring from the initial load, the total load is increased five times, over a time period of 0.4 sec. The whole duration of the simulation is 0.5 sec. A table including parameters of interest, describing the transient and steady state response of the system with respect to time, can be seen below. The table is structured almost identical to the one presented in the previous test. It does not, however, include the parameter dv, as to describe the voltage rise after each applied load. This is because the voltage rise is the same (33 V) for every load applied before 0.4 sec. Graphs showing DC and AC measurements can be seen in Figure 3.12.

According to Table 3.4, which excludes the response of the system after 0.4 sec, the ripple voltage increases with every step load. The other parameters, however, do not seem to change substantially until the load is increased to 80 kW. During this event, the system is able to enter into a steady state at a faster rate due to there not being any undershoot. The THD also increases, but is still well below the IEEE limit of 5%. The PF of the system can be observed in Fig 3.12c, where it is also clear that the system is able to maintain inversion in the time period <0.4. This can be deduced from studying the phase difference between the grid voltage and current. The current is clearly shifted 90° from the voltage, which gives a PF of -1, subsequently feeding power back to the grid. When the load exceeds 80 kW the system becomes unstable and is unable to maintain inversion.

At 0.4 sec, when the load is increased to 100 kW, the current becomes too large for the system to handle and the controller is therefore unable to compensate for the error and keep the DC voltage at the setpoint. Figure 3.12a only shows the DC voltage up until 0.5 sec. If the simulation was to be extended, the measurements would show the voltage increase to around 3.6 kV, which is the sum of all the voltage sources.

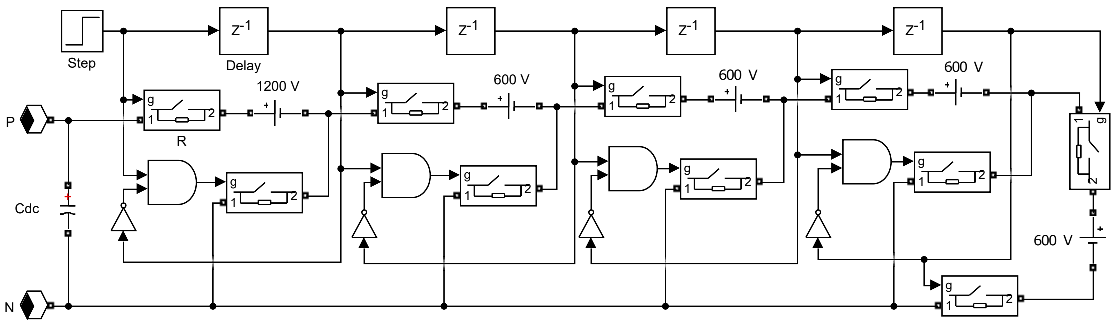
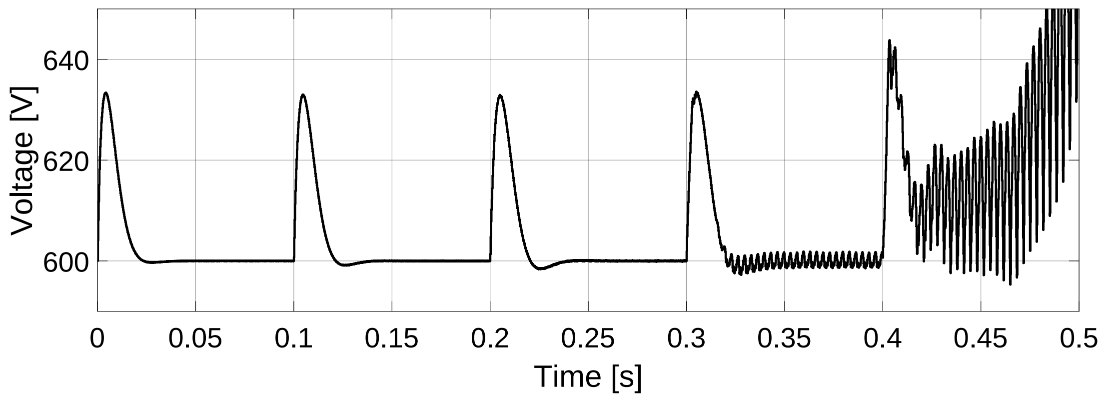


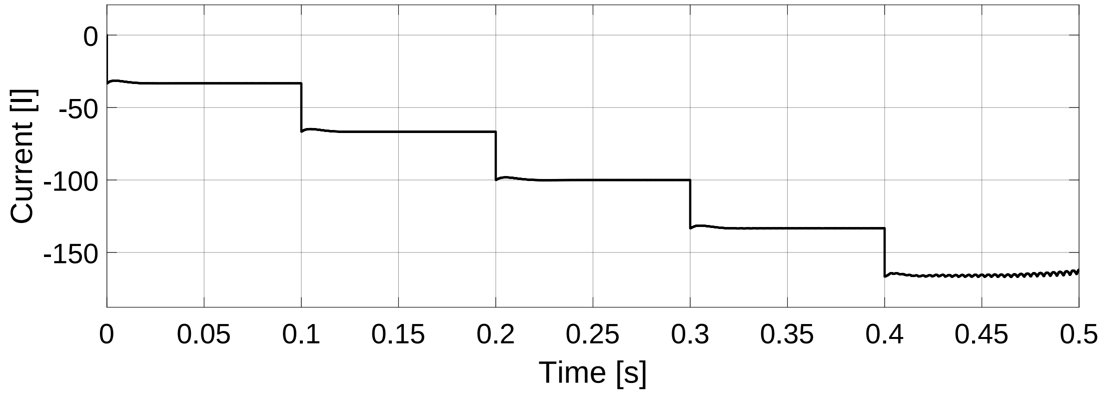
Figure 3.11: Increasing step load setup during Inversion.

		Transient		Steady State	
$\mathbf{T_{sim}}$ [s]	(-)$\mathbf{P_L}$ [kW]	$\mathbf{T_s}$ [ms]	$\mathbf{v_{us}}$ [V]	$\mathbf{v_{rip}}$ [mV]	$\mathbf{THD_i}$ [%]
<0.1	20	38	0.3	69	0.21
<0.2	40	40	0.8	152	0.25
<0.3	60	40	1.5	232	0.18
<0.4	80	21	0	3e3	1.11

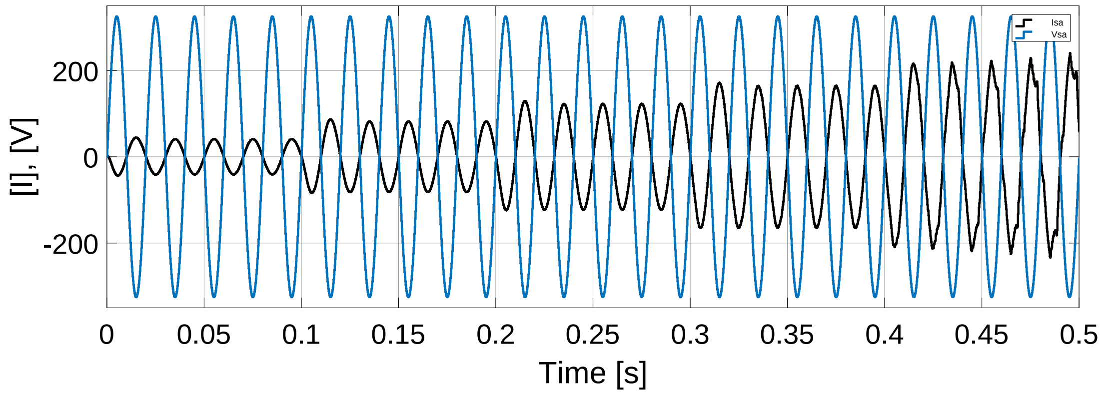
Table 3.4: Transient and steady state responses during inversion.



(a) DC voltage.



(b) DC current.



(c) Phase voltage (blue) and respective current (black).

Figure 3.12: DC (a, b) and AC (c) measurements during inversion with an increasing step load.

3.3.3 Bidirectional Operation

In the following test, the bidirectional capabilities of the AFE rectifier is tested to observe if it can transition from rectification to inversion and vice versa, while maintaining stability during an increasing step load. The structure of the load, as used in the simulation environment, can be seen in Figure 3.13. As observed in the figure, the load is essentially a combination of the ones used in the two previous tests. It consists of two resistors in parallel, which are in parallel to one resistor in series with two DC voltage sources. Starting from 20 kW, a step load is applied every tenth of a second for a duration of 0.3 sec. In other words, they are in total 4 loads. However, the total load is only increased once, from ±20 kW to ±40 kW. The applied load and operation of the rectifier, for the whole duration of the simulation (0.4 sec), can be seen in Table 3.5. The transient and steady state responses of the system have already been documented in the previous tests and are therefore not included in the table. The DC and AC measurements can be seen in Figure 3.14.

As seen in Figure 3.14a the controller is able to compensate for all the voltage drops and voltage rises caused by the step loads. The rises are larger than their preceding drops. This is most likely due to the sudden change in the direction of the DC current, as seen in Figure 3.14b. However, the AFE rectifier is still able to transition smoothly from rectification to inversion, and vice versa, in a matter of milliseconds without causing any significant instability in the system. This can be seen in Figure 3.14c, where it is clear that the current is in phase with the voltage during the time periods of [0, 0.1] and [0.2, 0.3], and shifted 90° relative to each other during the time periods of [0.1, 0.2] and [0.3, 0.4].

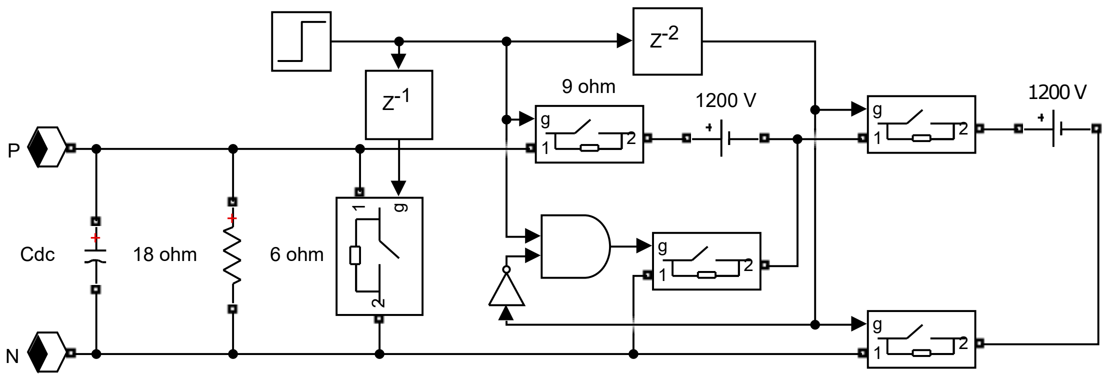
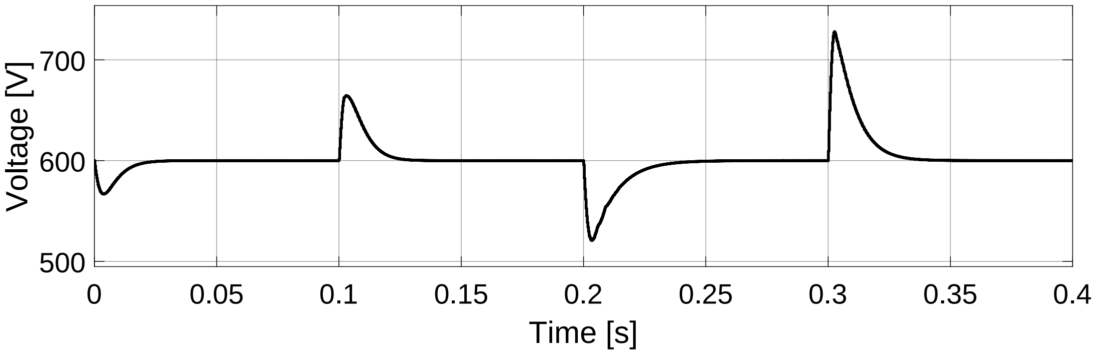


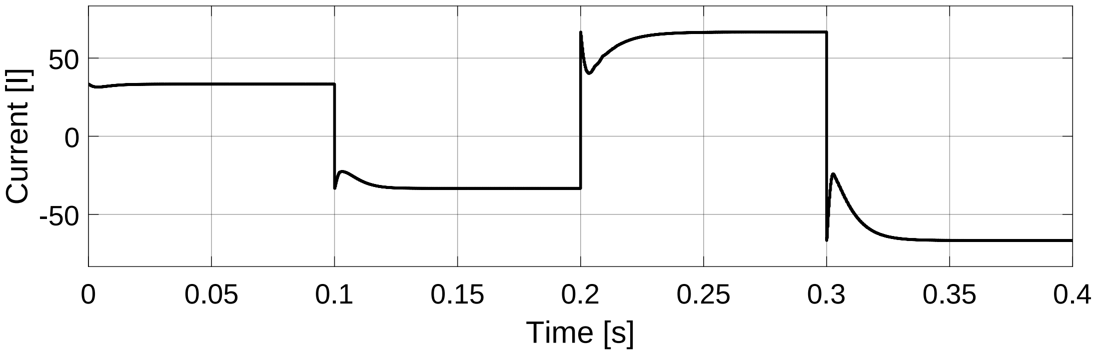
Figure 3.13: Step load setup for bidirectional operation.

T_{sim} [s]	P_L [kW]	Mode
<0.1	+20	Rectifier
<0.2	-20	Inverter
<0.3	+40	Rectifier
<0.4	-40	Inverter

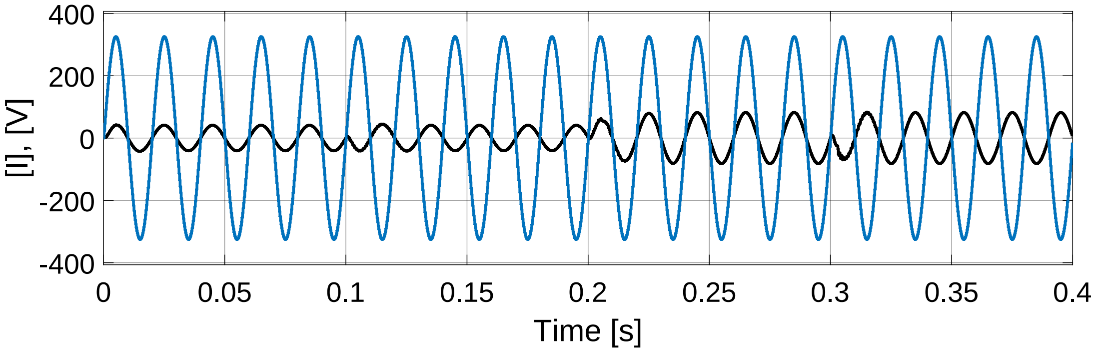
Table 3.5: Applied load and operation for the duration of the simulation.



(a) DC voltage.



(b) DC current.



(c) Phase voltage (blue) and respective current (black).

Figure 3.14: DC (a, b) and AC (c) measurements during bidirectional operation.

4 Experimental Prototype

This chapter presents a physical model of an AFE rectifier system. The physical model is constructed in reference to the theoretical design that is presented in the previous chapter. All the hardware components that are used in the physical model are described in the first section of this chapter. Afterwards, in section 4.2, follows a presentation of various tests conducted to investigate the performance of the hardware components. In section 4.3, the software used to implement the algorithms is described, and results from real-time software tests are also presented. The remaining introduction gives a general description of the system setup and topology.

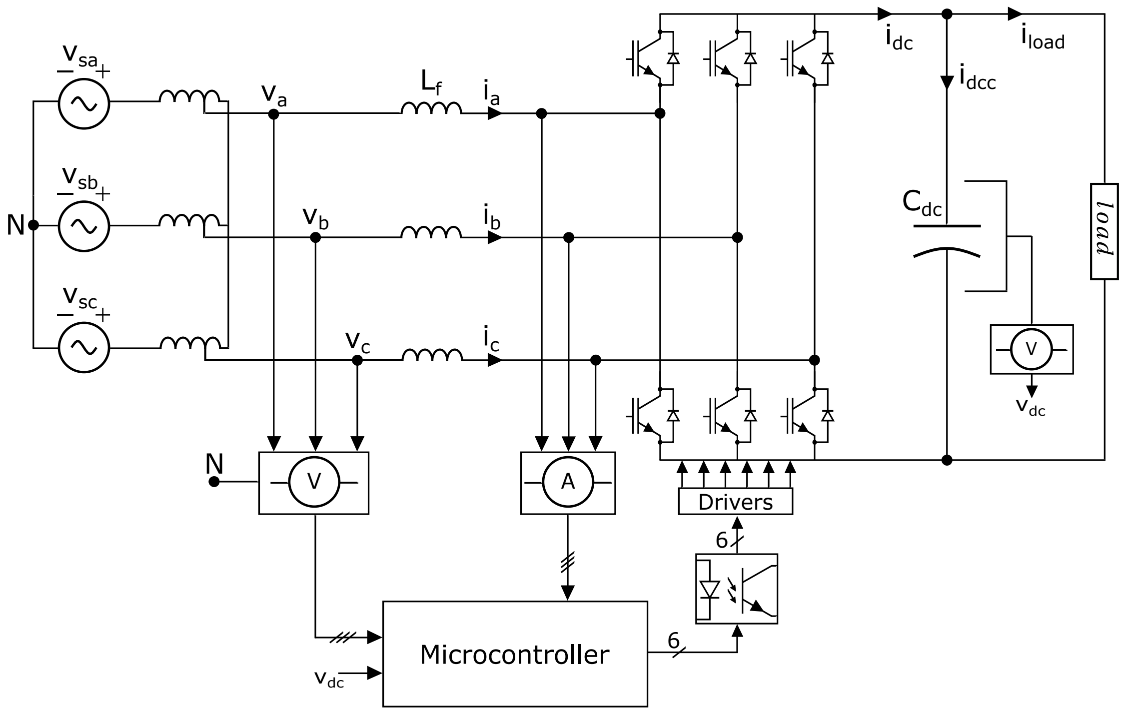


Figure 4.1: Topology of the physical model.

A topology of the physical model can be seen in Figure 4.1. The model topology is based on the design presented previously in chapter 3. However, only the resources available at hand have been used to build the system, and its topology is therefore not entirely identical to the original design. Some fundamental changes have been made to the filter topology and power rating. A L filter has been used instead of a LCL filter, and due to the limited power capacity of the laboratory supply and equipment, the power rating of the system has been scaled down to 3 kW. The largest factor restricting the power rating is the DC load, which is also equipped with a 5 A fuse. Otherwise, the grid is able to deliver much more power.

The three-phase power sockets in the laboratory, which are connected to a TN-S grid, have the capacity to deliver 6.4 kW and are protected by 16 A circuit breakers. Also, as a safety measure, a Y-N configured autotransformer is connected to the grid. This permits the user to safely scale the voltage from zero to the rated grid voltage. Although no galvanic separation is provided, the autotransformer is equipped with internal fuses and circuit breakers. This concludes the grid side of the topology. The rest of the system topology, excluding the DC capacitor and load, can be considered as the prototype.

As seen in Figure 4.1, the prototype consists of: three measurement modules, a Microcontroller Unit (MCU), an optocoupler circuit, driver circuits and IGBT transistors. Every phase voltage is measured in reference to the neutral (from autotransformer). All the AC and DC measurements are fed to the MCU. This is a microprocessor circuit that is programmed to execute all the necessary control algorithms for conducting PWM. The MCU outputs six gating pulses, which are amplified by the connected optocoupler circuit. This is due to the required input threshold voltage of the driver circuits. The optocoupler circuit also provides some safety by physically separating the MCU from the driver circuits. The drivers are directly connected to the IGBTs and provide the required turn-on and turn-off voltage level. They also provide safety during switching. The rated switching frequency and other system parameters can be seen in Table 4.1.

Parameter	**Symbol**	**Value**	**Unit**
Rated power	P	3	kW
Grid voltage	V_{LL}	400	V
DC reference	V_{DC}^{*}	600	V
Grid frequency	f_g	50	Hz
Switching frequency	f_{sw}	5	kHz
Sampling rate	f_s	1	MHz
Filter inductor	L_f	10	mH
Coil resistance	R_L	0.19	Ω
DC capacitor	C_{DC}	1525	μF

Table 4.1: System parameters.

4.1 Technical Aspects

A picture of the prototype, with all its components labelled, can be seen in Figure 4.2. The prototype has been disconnected from the AC and DC powersupply for the purpose of clarity. For an even better overview of the system, it can be advantageous to compare the figure to the topology in Figure 4.1. Otherwise, a complete connection digram is attached in Appendix C, and all available datasheets are attached in Appendix D.

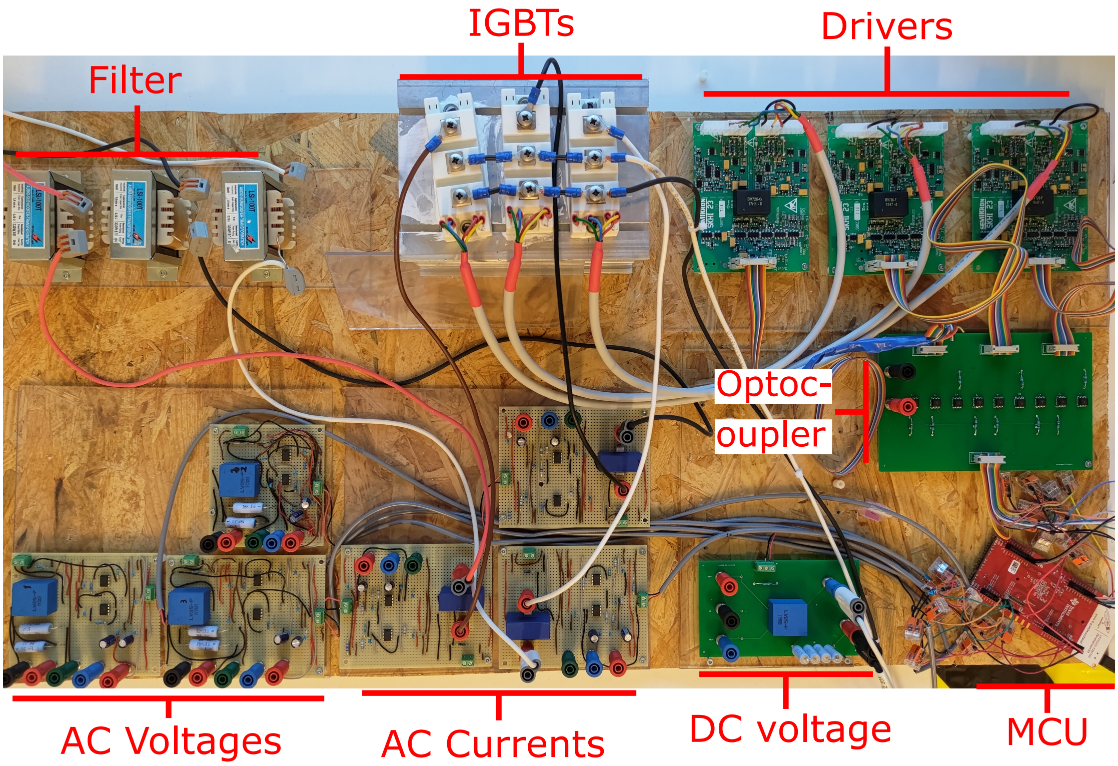


Figure 4.2: Picture of the prototype with its components labelled.

By observing the picture of the prototype, it is clear that the measurement modules consist of individual measurement cards. There are in total seven such cards; six for conducting grid measurements, and one for the load-side DC voltage. It is also worth noting how the measurement cards were built. The AC measurement circuits have been assembled by hand and soldiered on breadboards, while the DC measurement card is a Printed Circuit Board (PCB). Furthermore, all the measurement cards are connected to the MCU, which can be seen in the lower right corner of the picture. Above the controller lies a PCB, which is the same optocoupler module drawn in the system topology. The optocoupler PCB is connected to three driver cards, one for each IGBT half bridge.

Due to the heat loss associated with high frequency switching, the IGBTs are placed on a heath sink with a layer of thermal paste in-between. There is also some heat loss from the current flowing through the converter bridge. The current is supplied by an autotransformer, which is not included in Figure 4.2. The filter inductor, however, can be seen in the upper left corner of the picture depicting the prototype. Each inductor is essentially a repurposed audio subwoofer transformer and have an internal resistance of 0.19 Ω. The internal resistance of the filter, combined with the resistance of the conductors, will have a degrading effect on system efficiency. Also, although miniscule, there is heat and power loss through each component.

All of the components, which were used to build the prototype, have been provided by HVL. However, some of the components were designed by previous students. In particular, the optocoupler and measurement circuits were originally built to be used in previous projects. For use in this project, only minor adjustments have been made to change the nominal operating range of the optocoupler and DC measurement circuits. Otherwise, the fundamental PCB design remains the same. A more detailed description of the concepts, which were used to design all the circuits, will be given later. For now, only a brief description of the role and working principle behind every component will be given.

In short, every measurement card scales down the input, which is either voltage or current, to a much smaller voltage that ranges from 0 to 3 V. Furthermore, this analog voltage is sampled by the connected MCU, which assigns a binary number to the measured analog voltage level. In other words, the MCU produces a digital output that represents the analog input. This process is called Analog to Digital Conversion (ADC), and the quality of the ADC conversion depends on the resolution and sampling rate of the MCU. When a digital output is produced, it is further processed through software. This way, by programming the MCU, the digital signal is scaled back up to a value closer to the actual voltage or current measurement (digital measurement). All digital measurements are inputted to control algorithms. These algorithms are executed within every sampling period and are also responsible for calculating the PWM gating pulses. There are six PWM gating pulses that are outputted from the MCU.

The gating pulses that are generated by the MCU have a maximum voltage of 3.3 VDC (high). However, the required turn-on voltage level, which is inputted to the IGBT drivers, is 15 VDC. This means that the PWM pulses from the MCU must be amplified. As a solution, an optocoupler circuit is therefore connected in-between the MCU and drivers. The primary side is connected to the MCU while the secondary side is connected to the drivers. Although it is not visible in Figure 4.2, a 15 VDC supply is also connected to the secondary side to amplify the DC pulses.

A more detailed description of each component will be given in the following sections.

4.1.1 Microcontroller Unit

A close up picture of the MCU that is used in the prototype can be seen in Figure 4.3. More specifically, the MCU is the chip attached to the PCB. The whole card, as seen in the figure, is called a "MCU LaunchPad™development kit" and is developed by Texas Instruments for embedded development. There exist many different LaunchPad models on the market. However, the one used in the prototype and shown in the picture has the model name: LAUNCHXL-F28379D. The attached MCU chip is classified as: TMS320F28379D. There are many different components on the Launchpad that simplify programming of the chip and interactions with other devices.

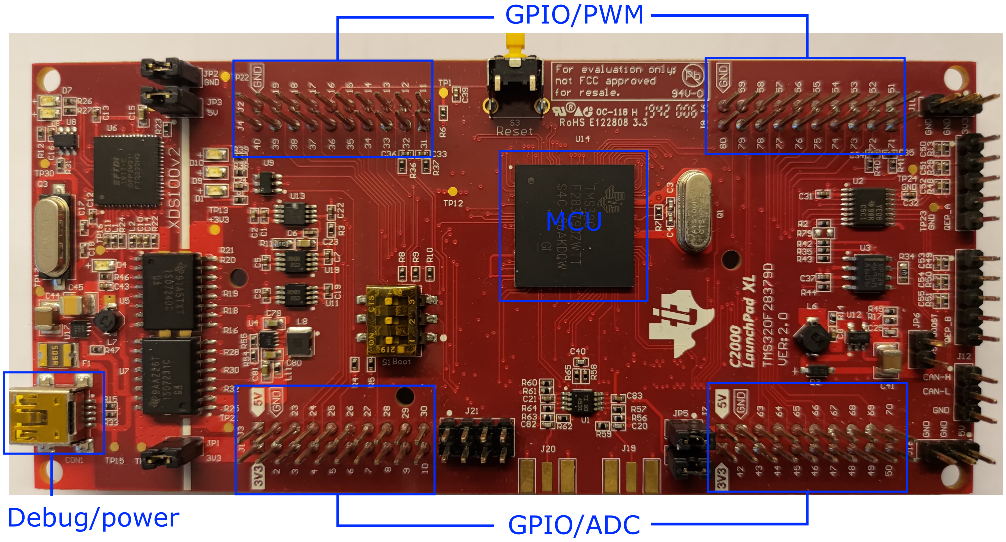


Figure 4.3: Picture of the TI LaunchPad: LAUNCHXL-F28379D.

The debug probe, which is labelled in Figure 4.3, enables programming of the MCU through USB. When connected to a computer, the USB also provides the required voltage to power all the on-board components. The USB connection provides 5 V, and a DC/DC converter is used to step down this voltage to 3.3 V, which is

Pin	Designation	Function	Comment
1	Output	3.3 V	Connected to optocoupler PCB
20	Input	GND	Connected to optocoupler PCB
22	Input	GND	Common for all measurement cards
24-25, 27	Input	ADC	AC voltage measurements
35-40	Output	ePWM	PWM outputs
41	Output	3.3 V	Connected to external switch
67	Input	ADC	DC voltage
64-66, 68	Input	ADC	AC currents
77	Input	GPIO	Input for external switch

Table 4.2: General overview of the pins used in the prototype.

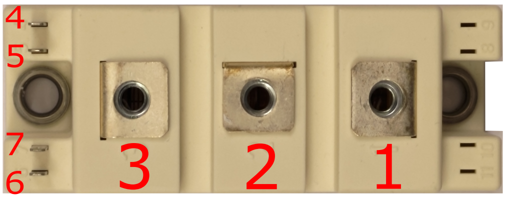
required by the MCU. On the LaunchPad, there are therefore two voltage levels available; 5 V and 3.3 V. There are also several General Purpose Input/Output (GPIO) pins (0-3.3V) that are connected to the MCU and its peripherals. Through software, the GPIO pins can be programmed to read an input voltage (high/low), or toggle an output voltage at a high frequency. However, these basic functions are not enough for high precision switching or reading analog voltages. There are therefore dedicated pins for ADC and PWM purposes.

For conducting ADC, the MCU has four internal converters with a scalable resolution; 16-bit or 12-bit. The MCU also has its own hardware modules for generating PWM pulses, which is called Enchanced Pulse Width Modulation (ePWM). Although the GPIO pins can be toggled through software, it is more efficient to use the ePWM modules. This is because the ePWM modules have their own counters that are separate from the software. This way, there will be less delay calculating the control algorithms, and the PWM frequency will not be limited by the software timer. Therefore, for use in the prototype, the ePWM modules are used to generate all the PWM gating pulses.

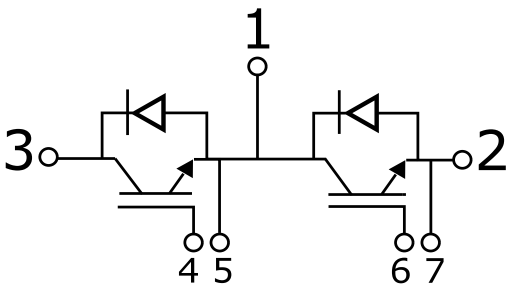
The position of the GPIO pins that are used for ADC and PWM are highlighted in Figure 4.3. However, not all are GPIO pins. Some of the pins have other functions; supplying DC voltage or connecting signals to a common potential (GND). Altough it is not clearly visible, on the LaunchPad, a number is printed next to every pin. The ones highlighted in the picture are numbered 1-80. Furthermore, a general overview of the pins that are utilized for use in the prototype can be seen in Table 4.2. The table also gives informations about each pin' input/output designation and function. More information on how the GPIO pins are configured through software is given in section 4.3.

4.1.2 Transistor Module

In the prototype, the converter bridge consist of three half-bridge IGBT modules. These modules are developed by Semikron, and the specific product type is classified as: SKM100GB12T4. For this type of module, the maximum rated switching frequency is 20 kHz. Also, according to the datasheet, the collector-to-emitter junction can support up to 1200V (V_{CES}), with a nominal collector current of 100 A (I_{Cnom}). By comparing these ratings with the system parameters in Table 4.1, it is apparent that the IGBT modules are more than capable for the required use. A close-up picture of a single module can be seen in Figure 4.4. The figure also shows the respective connection diagram.



(a)



(b)

Figure 4.4: Picture (a) and connection diagram (b) of the IGBT module.

A single module has three connections points for the half-bridge and two pins for each transistor. The grid phase voltage is connected to terminal 1, and the load is connected to terminal 3 and 2, with respect to polarity. To form a three-phase two-level bridge, three such modules are connected in parallel. This can be seen in Figure 4.2, which depicts the prototype with all the modules connected.[1] Furthermore, for safe and optimal switching, the gate-emitter pins on every module is connected to a driver, which is described in the following section.

[1]The load is not visible in the picture. The converter connections, however, are visible.

4.1.3 Transistor Driver

A gate driver is needed for high frequency switching of a high-power transistor, such as an IGBT or MOSFET. This is because of the high currents that flow through the transistor during a fast turn-on and turn-off sequences. Furthermore, to achieve high switching frequencies, the gate-capacitor must be charged and discharged with a large current. In other words, a higher gate current yields faster switching. For switching frequencies in the order of microseconds, a current in the order of several hundred milliampere or higher is often needed.[2] Only using a MCU is therefore not sufficient, as these typically only provide a few milliamperes. Without a gate driver, the high switching currents can damage the connected MCU. Gate drivers are therefore included in the prototype built for this thesis.

A close-up picture of one of the three IGBT gate drivers, which are used in the prototype, can be seen in Figure 4.5a. The driver is developed by Semikron and the product type is SKHI 12/23 (R). In fact, the driver actually consists of two independent, though interconnected, circuits. Due to its double circuit topology, which is described in the datasheet, a single driver card can control both transistors in one Semikron IGBT module. The supply voltage is 15 VDC and the threshold voltages for the PWM input signals are the same.[3] However, the required threshold voltage, including other parameters, can be configured by bridging specific connection points on the driver card. Other configurable parameters include: optimal switching frequency, switching deadtime, and soft turn-off time.[4] There are also many other configurable functions and parameters. However, these will not be discussed in detail. Nevertheless, the driver does have some safety features that are worth mentioning.

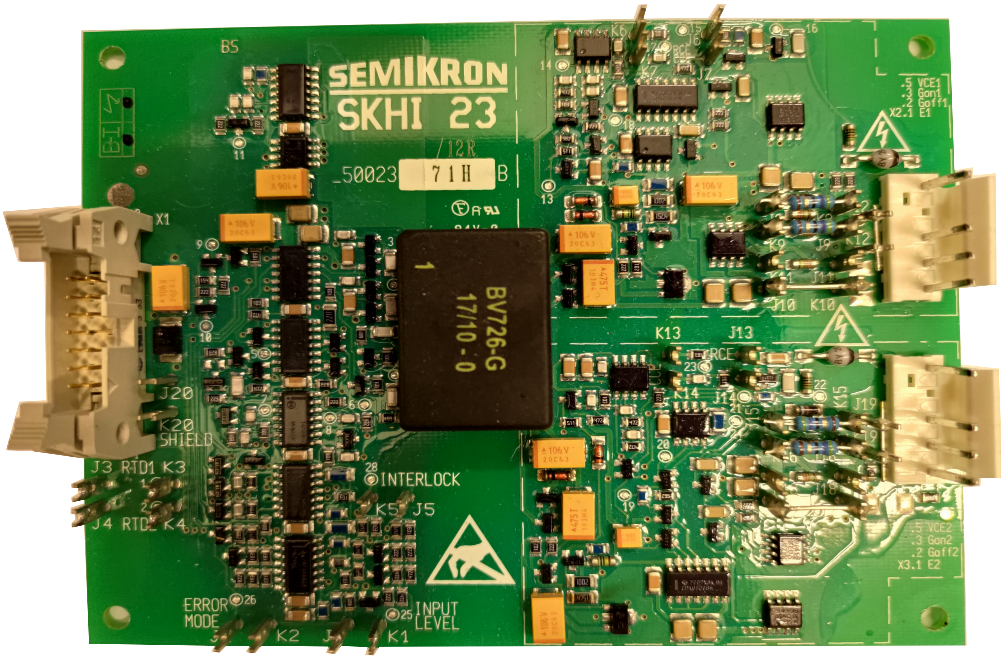
The driver has several safety features, such as: short circuit protection by V_{CE} monitoring, galvanic isolation and an interlock function that prevents both transistors from conducting simultaneously. Also, if there occurs an error (e.g., a short circuit), the driver will force the outputs to a logical low voltage (-8 VDC) and produce an output signal, which is factory set to logical high (15 VDC). During the error, the driver outputs will stay low until the driver is reset; both PWM inputs are low. However, this can be bypassed by shorting the output pins that are used for V_{CE} monitoring. Otherwise, as mentioned earlier, the driver can be

[2]The gate voltage typically lies in the range of 10 to 15 VDC (logical high)

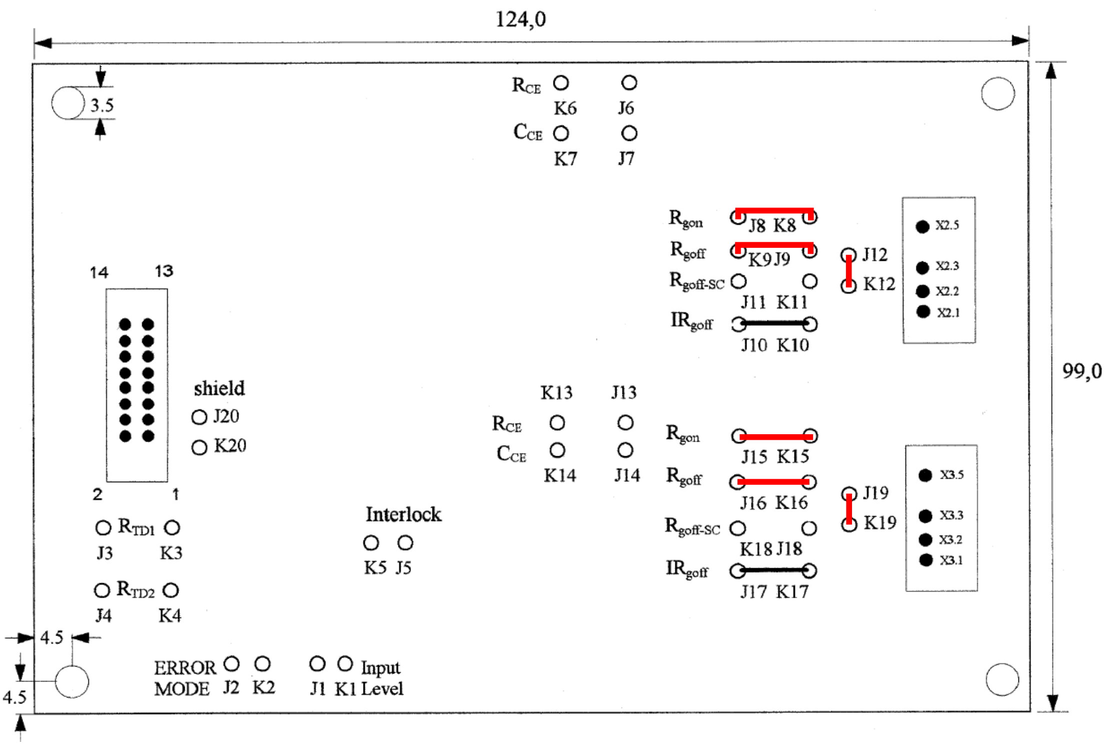
[3]The threshold voltage is the required voltage level for the PWM signal to be registered as logical high by the driver.

[4]In case of a short circuit, the IGBT turn-off time should be longer than usual (soft turn-off) to avoid high voltage spikes

configured by shorting certain connections on the driver card.



(a)



(b) Bridged connections are highlight in red, and lengths are given in mm.

Figure 4.5: Picture (a) and connection diagram (b) of the gate driver.

For use in the prototype, every adjustment made to the driver, which is done by bridging connection points on the card, can be seen in Figure 4.5b and are highlighted in red. The connection points J12-K12 and J19-K19 are bridged to reduce the amount of outputs for the gate signals. Otherwise, there would be in total four outputs, which would only be necessary for controlling several IGBT modules in parallel.[5] Furthermore, the connection points for R_{gon} and R_{goff} are also bridged. However, these are bridged with resistors, whose values are selected according to a table in the datasheet. More specifically, these connection points are bridged to adjust for the optimal switching speed, which is determined by the gate current during turn-on and turn-off. The factory adjusted resistance is 22 Ω. According to the specified datasheet, the recommended resistance is 15 Ω (for both R_{gon} and R_{goff}) when driving a SKM100GB12T4 IGBT module.[6] Therefore, to decrease the total resistance to 15 Ω, 47 Ω resistors are bridged in parallel.

4.1.4 Optocoupler Circuit

As previously mentioned, the IGBT drivers that are used in the prototype have an input threshold voltage of 15 VDC. It was also mentioned that the MCU can only output a maximum voltage of 3.3 VDC. Therefore, to increase the voltage level of the PWM signals from the MCU, an optocoupler circuit is included in the prototype. This is the PCB that is connected between the drivers and the MCU LaunchPad in Figure 4.2. A more detailed image of the PCB can be seen in Figure 4.6. The working principle behind the amplification is centred around the Integrated Circuit (IC) chips, which are attached on the PCB. As a matter of fact, every one of these chips is an optocoupler.

An optocoupler chip consists of an infrared Light Emitting Diode (LED) and light-sensitive transistor (phototransistor). Inside the chip, these components are separated, in essence forming two isolated circuits. However, although the circuits are physically separated, electrical signals can still be transferred through light. More specifically, when current flows through the LED, infrared light is emitted, which crosses the gap and activates the phototransistor, given that the current is strong enough to produce the required light intensity. The transistor turns off when the LED stops emitting light. In essence, the optocoupler behaves like a switch. This switch-like behaviour makes it possible for a PWM signal to be amplified by connecting the phototransistor to a DC voltage supply. In fact, this

[5]In theory, one driver might be able to control all the IGBT modules in the prototype. However, this option has not been explored.

[6]This information can be found listed in Table 4a in the datasheet, which, in this thesis, is attached in Appendix D

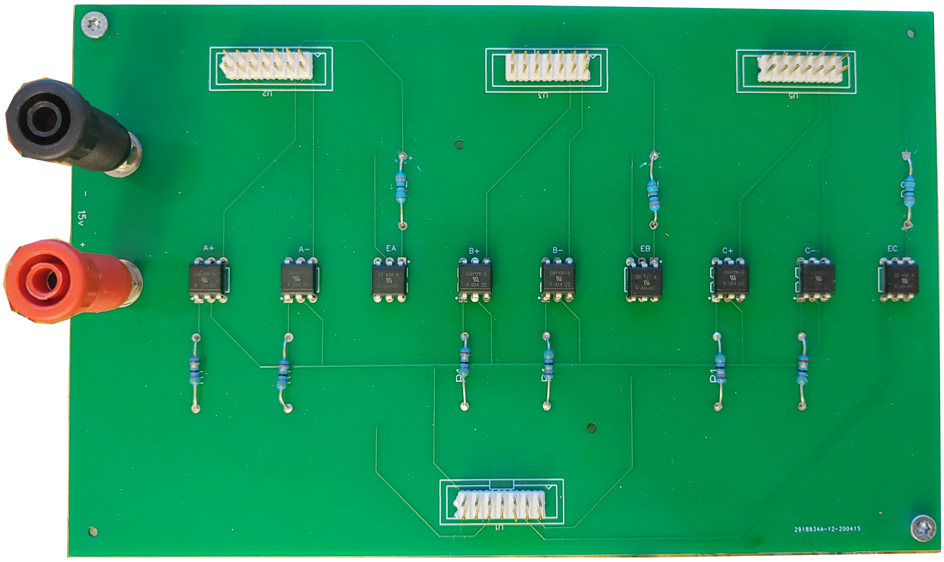


Figure 4.6: Optocoupler PCB.

is the working principle behind the PCB in Figure 4.6.

On the PCB, there are six optocoupler circuits for amplifying the PWM signals from the MCU. Each circuit has the exact same structure, and a simplified diagram of one of these optocoupler circuits can be seen in Figure 4.7. Furthermore, this circuit consists of one CNY17-F optocoupler chip from Vishay Semiconductors and a 47 Ω current limiting resistor. The gating pulses are inputted at the connection point labelled as V_{PWM}, and a 15 VDC supply is connected to the collector of the phototransistor, labelled V_{dc}. During nominal operation, whenever $V_{PWM} = 3.3V$, the phototransistor will activate and subsequently connect the DC supply to the driver (SKHI 23).

When V_{PWM} is at a logical high voltage level, the maximum current through the LED can be calculated as: $3.3\,\mathrm{V}/47\,\Omega = 70$ mA. This current will be lower due to PCB resistance. Also, although the LaunchPad is rated to supply 3.3 V, it will most likely be a bit lower in practice. The current through the LED will therefore be within the rated limit, which, according to the optocoupler datasheet, is 60 mA. Furthermore, the maximum collector-emitter current for the phototransistor is given as 80 mA. This is well above the maximum supply current for the driver, which is 0.32 A. This concludes the presentation of the circuit presented in Figure 4.7. However, the PCB also contains another set of optocoupler circuits with a different purpose than amplifying PWM signals.

There are in total nine optocouplers chips attached to the PCB in Figure 4.6. As explained above, six of these are used for amplifying PWM signals. The remaining

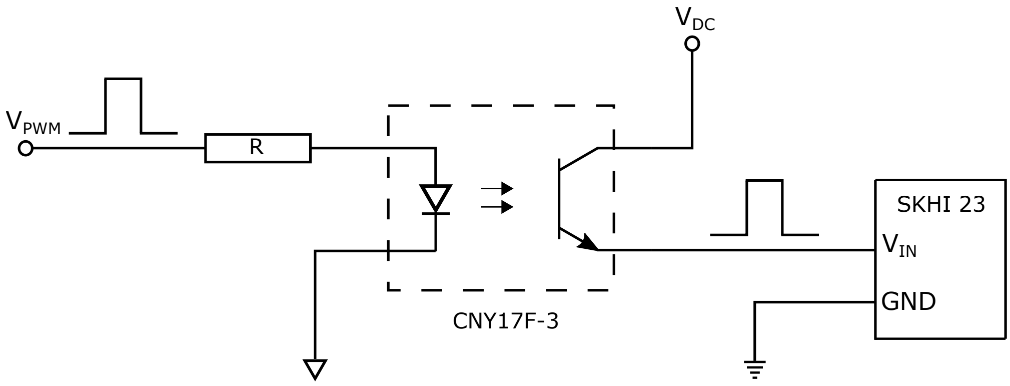


Figure 4.7: Optocoupler circuit used for amplifying the PWM signals.

three optocouplers, however, are used for reducing the error voltages, which are outputted from the drivers. The structure of these circuits are similar to the one in Figure 4.7. The only fundamental difference is that the LED side circuit of the optocoupler is connected to the driver while the phototransistor is connected to a 3.3 DC voltage (from LaunchPad). Otherwise, due to the high error voltage (15 V) from the driver, the current limiting resistor is 2.7 kΩ. Furthermore, by decreasing the error voltage from 15 V to 3.3 V, the signal can be identified by the MCU through the GPIO pins.

Pin	**Input**	**Output (x3)**	**Pin**	**Input**	**Output (x3)**
1	C-	NC	8	EA	15 V
2	3.3 V	A-	9	A-	15 V
3	C+	EA	10	NC	GND
4	EB	A+	11	A+	GND
5	B-	NC	12	NC	NC
6	EC	NC	13	SGND	NC
7	B+	NC	14	SGND	NC

Table 4.3: Description of the input and output connector pins.

14-pin connectors are used to connect the optocoupler PCB to the GPIO pins and gate drivers. The connector standard is DIN 41651, and a pin-map of the input and output connectors can be seen in Table 4.3. In the table, the letters A, B, and C represent the three drivers. Furthermore, the positive (+) and negative (-) signs denote the complementary gating signals. The pins for the error signals are denoted by EA, EB and EC. Another thing worth mentioning is that the three output connectors have the same structure. The table therefore only describes the pins for one output connector. Lastly, the pins that are not connected to anything are denoted as NC.

4.1.5 DC Measurement Circuit

A close-up picture of the DC measurement PCB, which is used in the prototype, can be seen in Figure 4.8. Its nominal measurement range is 0-600 V. The analog output from the PCB is in the range 0-3.3 V (compatible with MCU). In essence, the measurement card scales down a larger DC voltage to a smaller one. This conversion is achieved through the PCB circuit, which consists of one voltage transducer (LV 25-P) and two resistors. A simple diagram of this circuit can be seen in Figure 4.9. The working principle behind the voltage conversion is centred around the transducer, which utilises a phenomena called the Hall effect.[7]

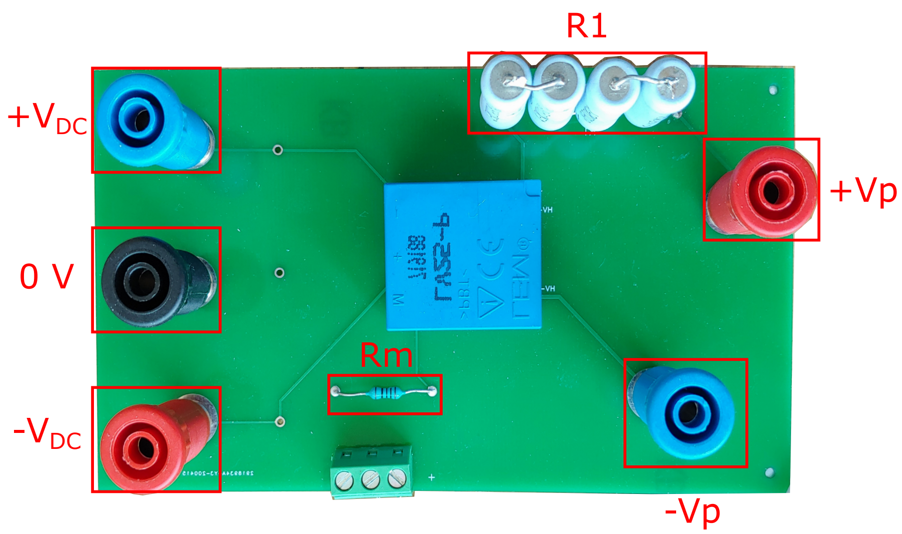


Figure 4.8: Simple digram of the transducer circuit used for VDC measurement.

The transducer consists of two physically separate circuits, primary and secondary, that are galvanically connected. A hall sensor is connected to the secondary circuit and is used to produce a voltage (Hall voltage) which is proportional to the magnetic field measured in-between the circuits. An amplifier is connected to the hall sensor and the transducer therefore requires a DC supply (V_{dc}).[8] The transducer can be supplied with either ±12 V or ±15 V. For use in the prototype, the PCB was designed with respect to the latter ($V_{dc} = \pm 15$ V). Moreover, the conversion ratio is rated at 25:10. In terms of current, the nominal input (I_{PN}) is 10 mA, and the nominal output is subsequently 25 mA. It is therefore apparent that appropriate resistor values must be selected to configure the measurement range of

[7]Named after Edwin Hall, who, in 1879, discovered that a magnetic field induces a transverse voltage in a conductor.

[8]The amplifier is presumably used to increase the Hall voltage or improve the sensitivity of the sensor.

the circuit. The external resistor is picked according to the nominal input voltage (V_{PN}) and current. In reference to the PCB in Figure 4.8, R_1 is calculated as:

$$R_1 = \frac{V_{PN}}{I_{PN}} = \frac{600\,\mathrm{V}}{10\,\mathrm{mA}} = 60\,\mathrm{k\Omega} \tag{4.1}$$

In case of an overvoltage, the measurement resistance R_m is calculated with respect to the maximum input measurement current I_{PM}, which according to the datasheet is 14 mA (840 VDC). Furthermore, for use in the PCB, the measurement resistor is calculated as:

$$R_m = \frac{V_m}{2.5 I_{PM}} = \frac{3.3\,\mathrm{V}}{35\,\mathrm{mA}} = 94.3\,\Omega \tag{4.2}$$

where V_m is the maximum voltage for ADC. Considering that the calculated R_m is not a standard value, a 100 Ω resistor is used instead. The datasheet also specifies 100 Ω as the lower limit for R_m.

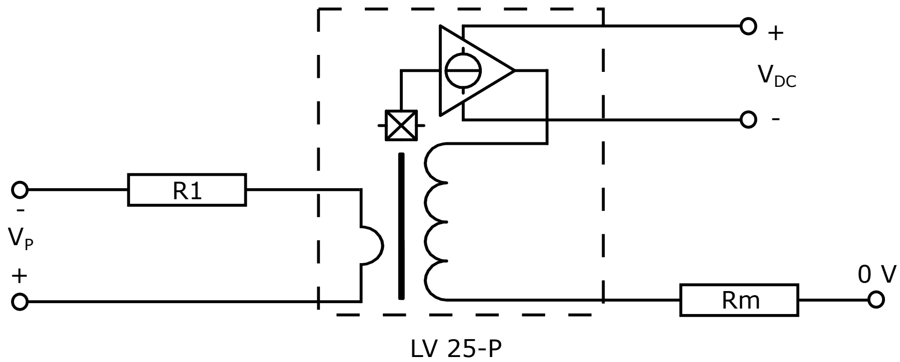


Figure 4.9: Simple digram of the transducer circuit used for DC measurement.

4.1.6 AC Measurement Circuits

There are in total six AC measurement cards in the prototype. As mentioned in the introduction to section 4.1, these cards were designed by someone else than the author of this thesis for use in another project [23]. Also, unlike the DC measurement card, which was presented in the previous section, the AC cards have not been altered. An in depth explanation of the design calculations will therefore not be given. However, a short presentation of the working principle behind the measurement circuits will be given instead.

In the prototype, three of the six AC measurement cards are designed for measuring voltages from 0 to ±360 V, whereas the remaining half is designed for measuring line currents from 0 to ±10.65 A. All the measurements are represented as an analog voltage output from 0 to 3 V. This conversion is achieved through several components, which are common for both the voltage and current measurement circuits. Each measurement circuit consists of a transducer, two operational amplifiers (op amps), resistors and capacitors for filtering out noise. Detailed diagrams of the circuits can be seen attached in Appendix C.1. For simplicity, the fundamental structure of the circuits can be represented with a single generic diagram, which can be seen in Figure 4.10. The transducer section of the circuit diagram is similar to the one presented in the previous section (Figure 4.9). However, there is a small difference between the transducer used for measuring voltage (LV 25-P) and the one used for measuring current (LA 100-TP). Their working principle is the same; utilizes the hall effect to output a current that is proportional to the input current. However, the current transducer is rated for a much larger input current and does therefore not need a current limiting resistor ($R_P = 0\,\Omega$). Otherwise, they have the same structure. Aside from the transducer, the op amps in Figure 4.10 play an important role in producing the correct analog output voltage.

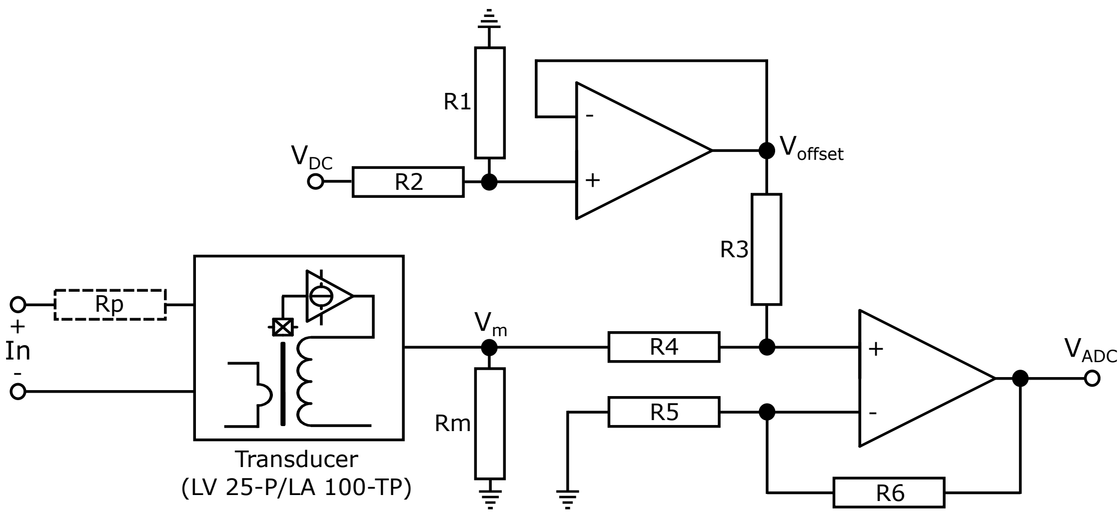


Figure 4.10: Simple diagram representing the fundamental structure of the AC measurement circuits.

In the AC measurement circuits, op-amps are used to scale and offset the transducer output. This is necessary due to the alternating polarity of the voltage drop over the measurement resistance R_m. Without the op amps, for instance, the output from voltage measurements would be within ±3 V, whereas the MCU only accepts an input from 0 to 3 V. Furthermore, the transducer output is therefore scaled down to ±1.5 V, and then offset by ±1.5 V so that the final output is in the acceptable range (0-3 V). The lower op-amp circuit does the scaling while the upper applies the offset. The same operations apply for the current measurement circuit, and by assuming that $R_4 = R_5$ and $R_3 = R_6$, a general expression for the output can be given as [23]:

$$V_{ADC} = \frac{V_m R_6 + V_{offset} R_5}{R_5} \tag{4.3}$$

4.2 Hardware Tests

In this section, tests are conducted to investigate the accuracy and response of hardware components used in the prototype.

4.2.1 Propagation of a Single Gating Pulse

The switching response of the IGBTs and quality of the received PWM signals are imperative for the performance of the rectifier. Too much delay or noise in the signals can cause the IGBTs to switch out of sync, malfunction, or damage the gate. The voltage used to drive the IGBTs can also have a significant effect on the switching time. Furthermore, if the applied voltage is too low compared to the threshold voltage, the IGBTs might not even turn on. On the other hand, if the applied voltage is too high, the IGBTs can be damaged. It is therefore important to investigate these aspects before running the prototype system. In the prototype, the gating pulses that are emitted from the MCU travel through several components. There can therefore exist many sources of errors and the PWM signals should therefore be investigated at every junction.

As explained in section 4.1, ePWM modules are used to emit the gating pulses, which are then amplified by an optocoupler circuit before entering a driver circuit that applies the IGBT gate voltages. In this test, the propagation of a single pulse signal is monitored for the full duration of its rise and fall sequence. A 5 kHz signal with a 50% duty cycle is used to conduct the test. The signal outputted from the MCU is labelled as V_{PWM} and can be seen in Figure 4.11. Furthermore, the output from the optocoupler is labelled as V_{OPTO}, and the driver output voltage, which is applied to the gate-emitter of an IGBT, is labelled as V_{DRIVE}.

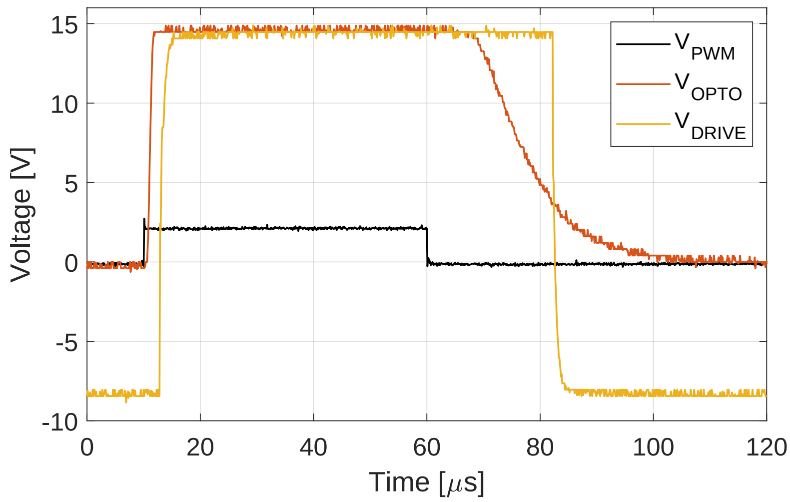


Figure 4.11: PWM signal in each junction from the MCU to an IGBT.

Upon initial inspection of Figure 4.11, it is clear that the optocoupler circuit is able to amplify the input signal to almost 15 V, as intended. It is also clear that the driver is able to register the amplified signal and subsequently produce the necessary gate-emitter voltages; 14 V during turn-on and -8 V during turn-off. Other noticeable details are the input-output turn-on and turn-off propagation times. In other words, the time it takes for the optocoupler and driver input-output signals to reach their on or off states with respect to the initial signal V_{PWM}. Furthermore, from the figure, there can be observed a substantial delay between the turn-off of V_{PWM} and the remaining signals. In comparison, the turn-on seems to be almost instant. These observations can be summarized in Table 4.4, where $t_{\mathrm{d(on)}}$ and $t_{\mathrm{d(off)}}$ denote the propagation delay, and v_{max} and v_{min} denote the maximum and minimum voltage levels.

From closer inspection of the data presented in Table 4.4, it is apparent that the ePWM module is only capable of emitting a maximum voltage of 2.1 V. This is 1.2 V lower than what is expected and rated for the MCU LaunchPad (3.3 V). In fact, this is a 36% reduction in regard to the nominal operating point for the optocoupler circuit (as designed in section 4.1.4). Furthermore, the reduced voltage also reduces the amount of current that flows though the primary side of the optocoupler (forward current). This can explain the prolonged turn-off time for the optocoupler output signal. According to the datasheet for the optocoupler IC CNY17F-3, the fall time increases with a decreasing forward current. The datasheet also states that the connected load (secondary circuit) can affect the turn-on time. Either way, the driver is still able to register V_{OPTO} and is able to apply the negative gate-emitter voltage almost instantly. The turn-off time of the connected IGBT is in the order of nanoseconds, and there is therefore no noticeable slope for V_{DRIVE} during its transition into the off-state.

Parameter	Signals			**Unit**
	$V_{\mathbf{PWM}}$	$V_{\mathbf{OPTO}}$	$V_{\mathbf{DRIVE}}$	
$t_{\mathrm{d(on)}}$	0	2.7	5.1	μs
$t_{\mathrm{d(off)}}$	0	30	22.5	μs
v_{min}	0	0	-8	V
v_{max}	2.1	14.5	14	V

Table 4.4: Table showing various signal parameters interest. The input-output propagation times are calculated with respect to V_{PWM}.

4.2.2 DC Voltage Measurement

In VOC, which is the control scheme for the designed rectifier, accurate measurements of the DC voltage is important for outputting the correct control signals from the voltage controller. In other words, inaccurate DC measurements will result in a wrong voltage to be delivered to the DC bus. This can have a significant impact on efficiency, or, if the error is large enough, cause substantial damage to the connected load. For example, if the measurements show a lower voltage than what is available at the DC bus, the controller will still try to deliver the necessary current as an effort to increase the voltage in accordance with the measured error. In this case, the excess power will most likely have an detrimental effect any load that might be connected to the DC bus (e.g, an EV battery). On the other hand, if the measurements are too high, the connected load will operate with a reduced efficiency. In the case of an EV, an undercharged battery will reduce the range of which the EV can travel on a single charge. To avoid such problems, it is therefore important to investigate the accuracy of the DC measurement modules that are utilized in the feedback loops of the control system.

In the experimental prototype, the DC measurement circuit is designed to scale down the measured DC voltage to a much smaller quantity that is within the maximum voltage limit for ADC. The complete design procedure and working principle behind the circuit is presented in section 4.1.5. Moreover, a test has been conducted to investigate the accuracy of the design. In this test, the circuit card was tested during nominal conditions, that is, a DC voltage of 600 V was applied at the input.[9]

The measurement result from the test can be seen in Figure 4.12. From observing the graph, it is clear the analog voltage output (labelled V_m) is aligned with the DC input (labelled V_{DC}). This indicates that the measurement card is capable of providing accurate measurements. However, there is also some substantial noise present at the output signal. Noise is highly unfavourable, as it can lead to instability in the controller (from unstable feedback) and thereby cause the system to malfunction. A simple frequency filter can be used to minimise the noise, e.g, a fist order low-pass filter consisting of passive components. This can be implemented as a physical circuit consisting of a capacitor and resistor. Another option is to implement the filter digitally. Either way, the goal is to attenuate the frequency of the noise.

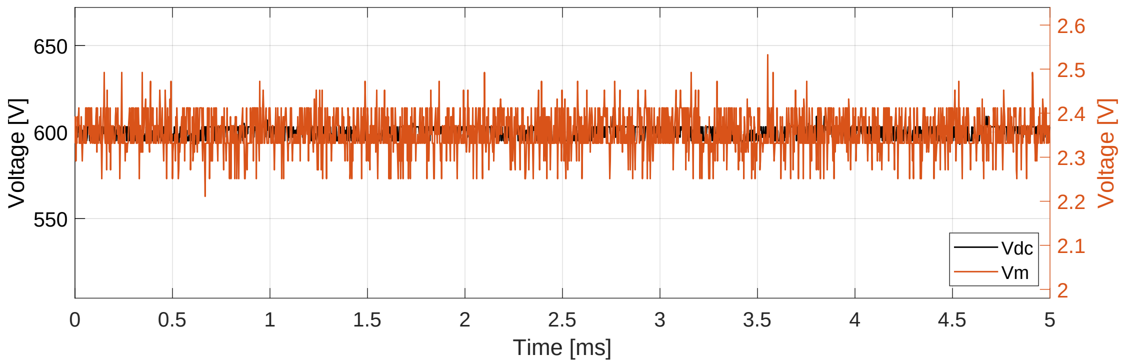


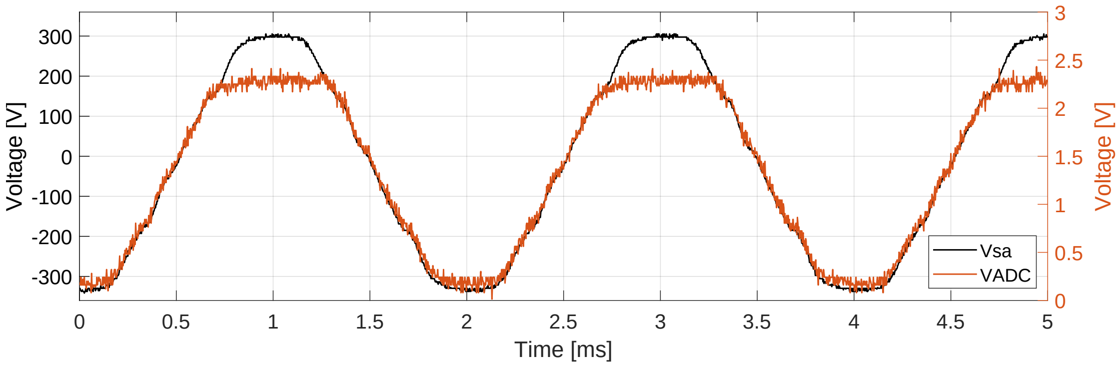
Figure 4.12: Result from test conducted to demonstrate the accuracy of the DC measurement card, where the DC voltage input V_{DC} is compared to the analog output V_m.

4.2.3 AC Voltage Measurements

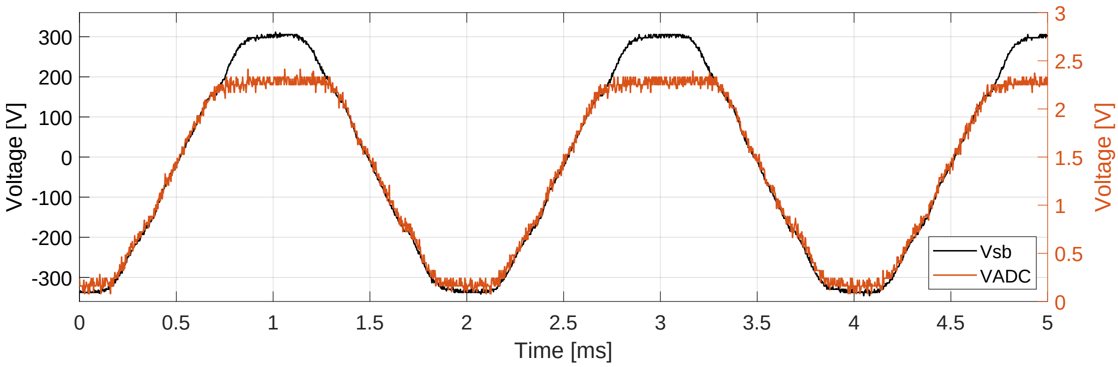
Accurate measurements of the three-phase grid voltages are important for orienting the space vectors in the stationary and synchronous rotating reference frames (Clarke and Park transformation). This is done through software algorithms, after the measurements have been sampled by the ADC modules. The resulting dq components from the Park transformation of the AC voltage measurements are used as feedback in the controller. These play an important role for calculating the transistor duty cycles. Any inaccuracy can therefore affect the switching sequence of the rectifier. Correct AC voltage measurements are especially important for extracting the phase angle from the grid, which are used for grid synchronization. Any phase

[9]The voltage was supplied by an external supply.

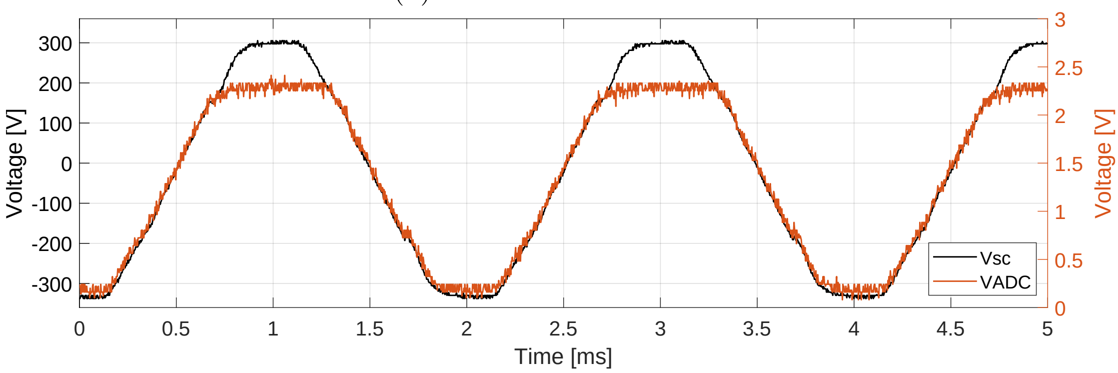
delay from the measurements will cause the switching sequence to be wrong, even if the measured magnitude is correct. The accuracy of the measurement circuits should therefore be investigated with these aspects in mind.



(a) Measurement card U1.



(b) Measurement card U2.



(c) Measurement card U3.

Figure 4.13: Test of the AC voltage measurement cards.

The results from the AC voltage measurement test can be seen in Figure 4.13. In this test, every measurement card is applied with a 230 V RMS voltage supplied by the grid. The input voltage is chosen with respect to the system parameters, which are given in Table 4.1. The caption beneath every result includes the letter U accompanied by a number from one to three. This is done to differentiate the measurement with respect to the card. The measurement cards are labelled in the same manner as in the wiring diagram attached in Appendix C. Although it is not shown clearly in Figure 4.2, the measurement cards are also physically labelled in the same number sequence (1-3).

By comparing the input voltages with their respective measurement outputs, it is clear that there is an substantial error of around 25% between the input and output amplitudes. There is also some error between the negative peak amplitudes. Otherwise, the outputs from the measurement cards seem to be in phase with the grid voltages, in addition to having minimal noise. However, the measurement errors are still substantial and need to be corrected.

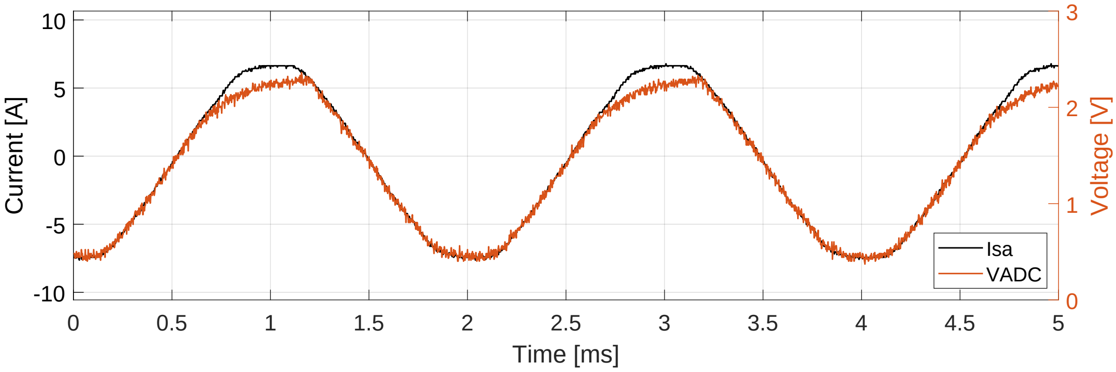
It is not expected for the grid voltages to change much during nominal operation of the experimental prototype. The measurement errors are therefore also likely to stay the same. Given the constant nature of the voltage measurements, the errors can be corrected quite easily through software. Exactly how this is done will be explained later in section 4.3.

4.2.4 AC Current Measurements

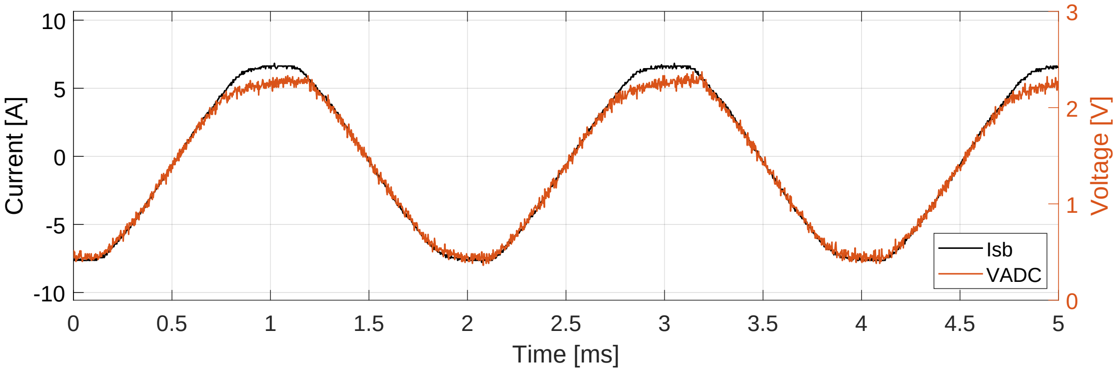
Similarly to the AC voltage measurements, the accuracy of the current measurements are important for producing the correct control signals. Another similarity is that the current measurements undergo the same coordinate transformation to the synchronous reference frame. The resulting dq quantities are also used as feedback in the decoupled current controller. However, the current measurements are especially important for controlling the active and reactive power flow through the rectifier. As opposed to the AC voltage, the current is expected to change continuously with the duty cycles of the transistors. It is therefore important to assure correct measurements of the AC currents.

This test investigates the accuracy of the three AC current measurement cards that are used in the prototype. To differentiate between the results, the cards are labelled in the same manner as drawn in the wiring diagram, which is attached in Appendix C. The results from the test can be seen in Figure 4.14. A RMS current of 5 A is applied to the two measurement cards U1 and U2, while a higher current (around 6.3 A RMS) is applied to the remaining card, U3.

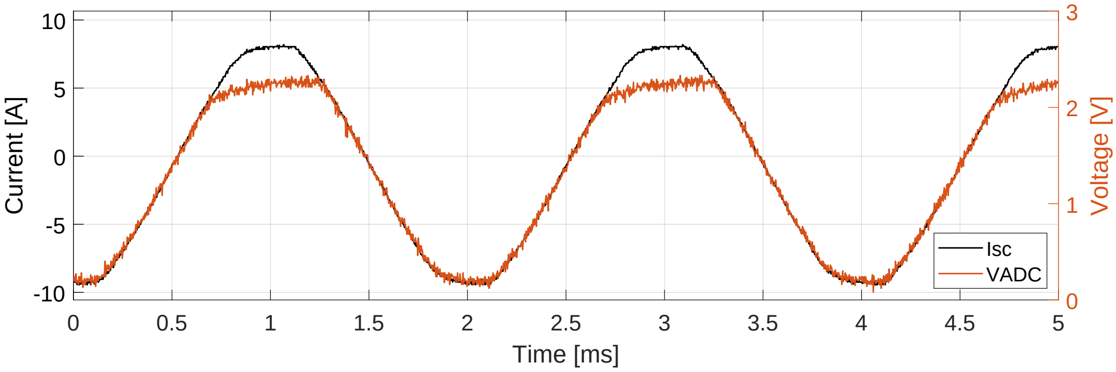
The results show that the measurement cards are incapable of measuring currents above 5 A. Below 5 A, however, the measurements seem to be quite accurate. This might indicate that one or more the main circuit components (voltage transducer or op-amp ICs) are damaged. The error could also arise from a faulty design or insufficient DC supply.



(a) Measurement card U1.



(b) Measurement card U2.



(c) Measurement card U3.

Figure 4.14: Test of the AC current measurement cards.

4.3 Software Implementation and Tests

This section starts off by giving a description of the software used to program the MCU. Afterwards follows a presentation of results from tests conducted to investigate the performance of the implemented algorithms.

4.3.1 Implementation

The MCU is programmed with Simulink and Code Composer Studio (CSS). CSS is an integrated development environment (IDE) and is used to compile and execute C code on the MCU. Simulink is used to auto-generate all the C code with the help of several MATLAB software packages,[10]. This is a much simpler alternative to personally writing the code in CSS. Another advantage of using Simulink is that the model can be run in external mode, which allows for real-time tuning of parameters and signal logging. The model can be seen in Figure 4.15. Relevant MCU peripherals and GPIO pins are configured through Simulink blocks, and the control algorithms are also programmed either textually or graphically in a block diagram environment. The control algorithms are almost identical to the ones implemented in the simulation model (3.4), which was presented in the previous chapter. The only difference is the PLL algorithm.

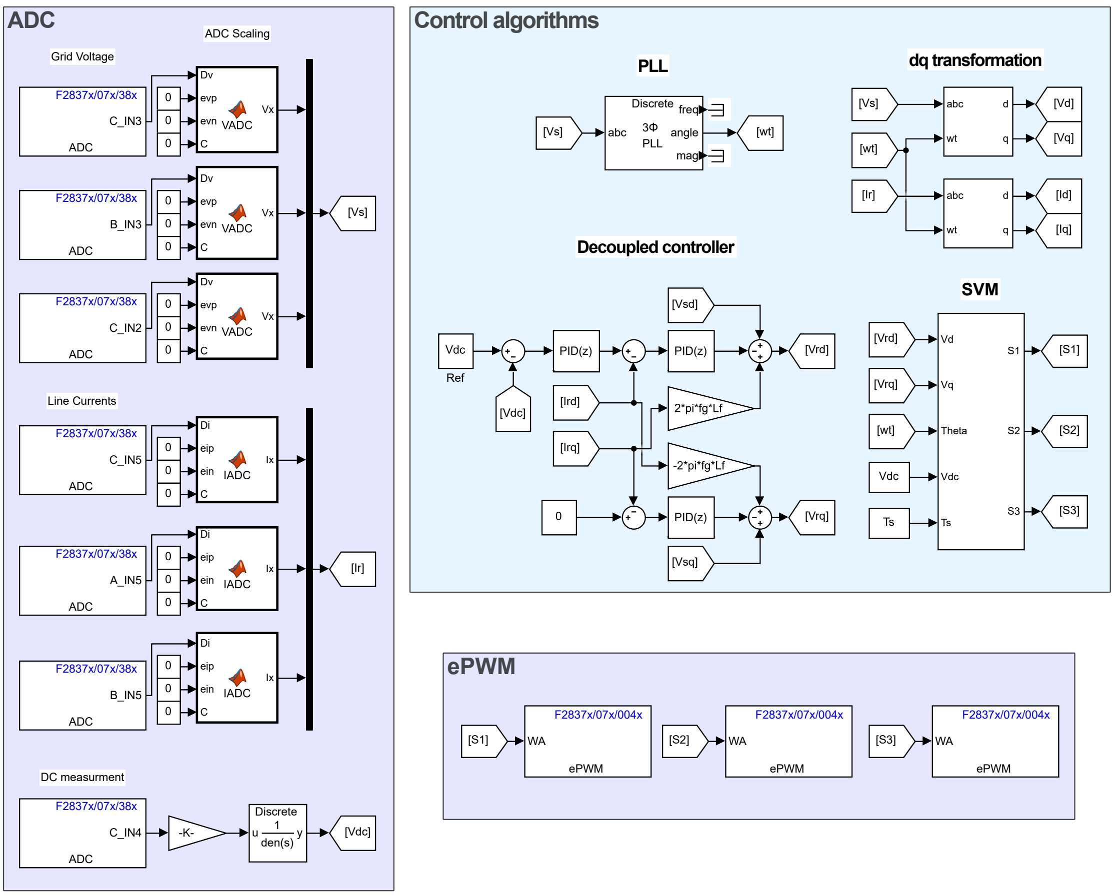


Figure 4.15: Simulink model for code generation.

[10]The software packages: MATLAB Coder™ Simulink Coder™ and Embedded Coder® are needed.

The original PLL algorithm, which was designed for the simulation model, is not included in the MCU model for code generation. This is due to difficulties with discretization and tuning of the internal PI controller during real-time operation. A more reliable algorithm from the Simulink library is therefore used instead. Otherwise, the algorithms used in the MCU model are the same as the ones in the simulation model. In addition to the control algorithms, the MCU model also contains blocks for interacting with the ADC and ePWM peripherals.

The ADC modules are configured to sample the voltage present at the MCU analog input pins. In Simulink, the ADC blocks output a constant stream of digital data. The range of the output is determined by the conversion resolution, which is set at 12-bit. It is possible to increase the resolution to 16-bit. However, with this resolution, the voltage must be sampled through a pair of analog input pins (differential inputs). Therefore, a 12-bit resolution, which allows for a single ended input, is used instead. A single-ended input implies that only one pin is needed for sampling a single analog input. Furthermore, a 12-bit resolution means that the measurements are divided into $2^{12} = 4096$ different values. In other words, the ADC Simulink blocks are configured to output a digital value ranging from 0 to 4096. For each ADC block, this range represents a specific measurement. A mathematical operation is done to every digital output to scale it to its actual respective measurement value.

The ADC outputs for the AC measurements are scaled with MATLAB functions. The function used to scale the AC voltages is slightly different to the one used to scale the currents. The MATLAB code for both scaling functions can be seen attached in Appendix A.4. In addition to scaling the ADC outputs, the MATLAB functions are also used to compensate for any measurement errors that may arise from, e.g., an unstable DC supply or inaccurate circuit design. Each function therefore has three extra inputs; two for adjusting the extremal points and one for adding an offset. A different method is used to process the DC voltage measurement. The DC voltage is always positive and is therefore much easier to scale. A simple gain block is therefore sufficient for this purpose. A digital low pass filter is also connected at the DC output to attenuate high frequency noise. Noise in the DC voltage measurement can cause an error in the process of calculating the correct duty cycles for the ePWM modules.

As mentioned previously in section 4.1.1, the ePWM modules are used for generating and outputting the gating pulses. In Simulink, three such modules are configured through interactive blocks. Each block/module is configured to generate two complementary gating signals according to a duty cycle ranging from 0 to 100 percent. The previously presented SVM algorithm is used to calculate and provide three duty cycles, one for each ePWM block. During normal operations, the modules are programmed to continuously output PWM pulses. However, they are also programmed to force all outputs to a logical low in response to an external *trip zone* event. More specifically, this event occurs when a logical high is inputted at a specified GPIO input; GPIO09. A switch is used to form a circuit between GPIO09 and a 3.3 VDC supply, which is provided by the Launchpad. This allows the user of the system to stop the PWM, even if the Microcontroller Unit (MCU) is running separated form external mode.[11]

This concludes the description of the software. A demonstration of the implemented algorithms are given in the following sections. The tests are conducted in external mode and a Simulink scope is used to log the digital signals.

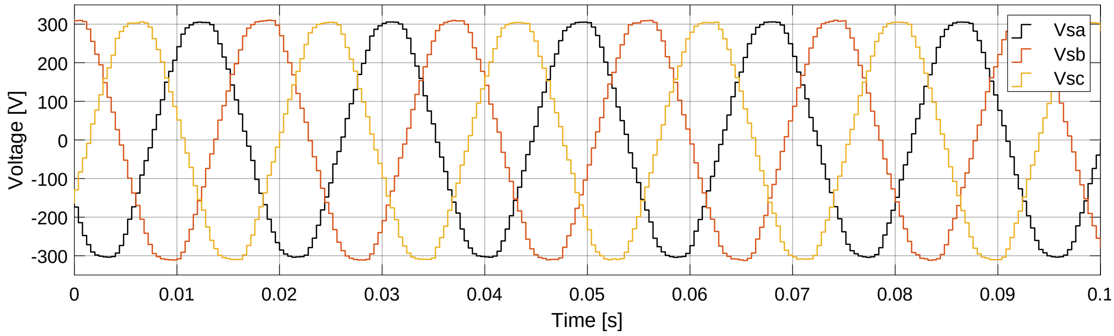
4.3.2 Sampling and Scaling of Measurements

This test demonstrated the performance of the ADC process. The analog input pins are connected to the AC voltage and current measurement cards. The AC voltage measurement cards are applied with a three-phase 230 V voltage supplied by the grid. Similarly, the current measurement cards are supplied with a three-phase current around 7 A. The digital output signals are measured after being processed by the scaling functions. Moreover, this test also demonstrates the performance of the scaling functions used to correct the measurement errors. The measurement errors for the AC voltages was presented previously in section 4.2.3, and the error present in the current measurement was presented in section 4.2.4 Furthermore, to correct these error through software, the measurements are tuned by changing the input parameters for the scaling functions. These parameters are tuned real-time during external mode.

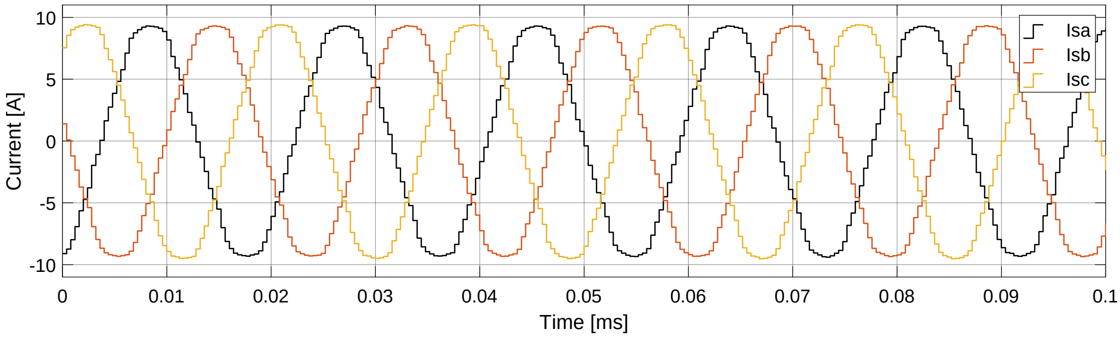
The measurement results from the test can be seen in Figure 4.16. By observing the graphs presented in this figure, it is clear that these errors are gone. More specifically, from observing the digital voltage measurements in Figure 4.16a, it can be deduced that the the MATLAB scaling functions are able to correct the initial amplitude errors. The same applies to the three-phase currents in Figure 4.16b. All the results show that the waveforms are balanced and symmetrical when

[11] If the switch is activated during normal operation, all the IGBT will turn of, which forces the current to flow through the freewheeling diodes and subsequently makes the system operate as an three-phase diode rectifier.

comparing the positive and negative peak amplitudes.



(a)



(b)

Figure 4.16: Three-phase grid voltages (a) and currents (b) as sampled by a Simulink scope during external mode.

4.3.3 Grid Phase Angle Extraction

As explained earlier in section 4.3.1, the implemented PLL algorithm has been imported from the Simulink library. This test demonstrates the performance of this algorithm, to see how well it is able to extract the phase angle from the grid voltages. The PLL is tested during nominal conditions. This means that the algorithm is run in real time during external mode. During external mode, the phase angle is extracted from the digital AC voltage measurements, which are sampled by the ADC modules. The quality of the PLL output therefore also depends on the quality of the ADC process. The performance of the ADC sampling was demonstrated in the previous test.

The result from the PLL test can be seen in Figure 4.17. The graph depicts a sawtooth shaped waveform, which represents the instantaneous angle of the grid. The waveform increases from 0 to 2π with a frequency of around 50 Hz. This indicates that the algorithm is capable of synchronizing its output to the frequency of the grid.

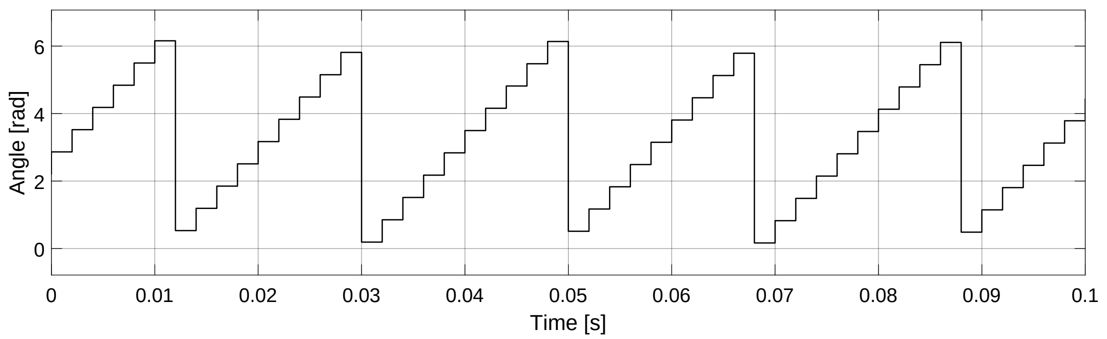
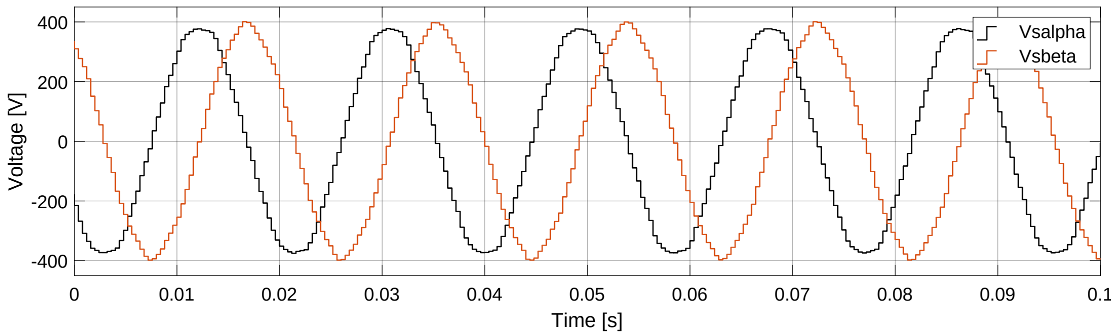


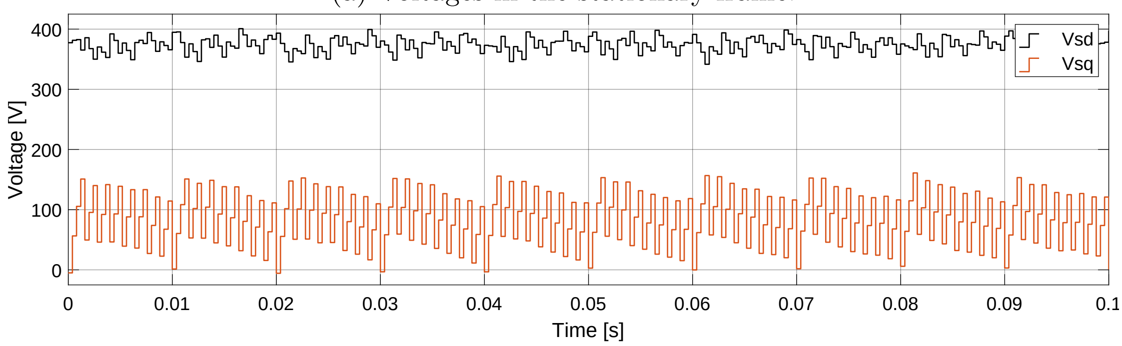
Figure 4.17: PLL output.

4.3.4 Coordinate Transformation

In this test, the digital AC measurements are transformed to the stationary and synchronous reference frames. Figure 4.18 shows the resulting signals from the Clarke and Park algorithms. In Figure 4.18a, the three-phase grid voltages are represented as two sinusoidal waveforms labelled $V_{s\alpha}$ and $V_{s\beta}$. In Figure 4.18b, these voltages can be seen in the synchronous reference frame as two DC quantities labelled V_{sd} and V_{sq}.



(a) Voltages in the stationary frame.



(b) Voltages in the synchronous frame.

Figure 4.18: Clarke and Park transformation of digital voltage measurements.

5 Discussion

This chapter discusses the main results from simulations and experimental tests.

5.1 Simulation

The proposed rectifier was modelled in Simulink and simulated during various load conditions in section 3.3. The simulation tests were conducted for the purpose of demonstrating the performance of the control system with respect to its bidirectional capabilities. In total three simulation were conducted. The system was tested during rectification, inversion, and bidirectional operation. Starting from nominal load conditions (20 kW), an increasing step load was applied during each simulation, and several observations were made in regard to the DC-link voltage response (transient and steady state), the PF, and the THD of the grid current (THD_i). The system was also pushed well beyond its limit to observe its behaviour when transitioning into instability.

Overall, the results show that the system is capable of bidirectional flow with UPF during rectification and leading PF during inversion. The results show that the system is able to seamlessly transition from rectification to inversion and vice versa. The results also show that the system is capable of delivering a steady DC voltage to the load during off-nominal load conditions. In fact, the results suggests that the system is capable of withstanding a load up to 300% over the nominal load before becoming unstable. This is most likely unrealistic from a practical standpoint, but, as the results substantiate, it is still theoretically possible given ideal conditions. Furthermore, the controller was designed for optimal stability around the operating point of the controller (600 VDC). This can be verified with respect to the transient and steady state response of the system. According to the results, the best response occurs during nominal load conditions. In other words, the system is able to recover quickly and provide the most stable output when a 20 kW load is connected. However, considering the PI regulators were tuned by hand, the rectifier system might still not be fully optimized in terms of control. In addition, a relatively large capacitance was chosen for the output capacitor. This might explain why the system has such a large region of stability. Moreover, the results indicate that the stability affects the THD_i.

A notable observation is that the THD_i stays below 5%, which is recommended by IEEE standards, throughout the entire duration of every load test. The largest THD_i (4.52%) and harmonic current component (4.2%) occurs when the system is unstable during a resistive load of 120 kW. During stable operations, the largest THD_i (0.29%) occurs during a resistive load of 20 kW, which is also the nominal load. These results indicate that the LCL filter design is more than sufficient for mitigating the switching harmonics, even during unstable operations. However, considering that the THD_i is larger during nominal load conditions compared to stable off-nominal load conditions, the results also indicate that the filter design is not optimally designed for the intended power rating.

5.2 Experimental Prototype

5.2.1 Propagation of a Gating Signal

In section 4.2.1, the propagation of a signal gating signal was monitored from its initial source to the gate-emitter terminals of an IGBT for the duration of its on-state and off-state. A 5 kHz pulse signal with a 50% duty cycle was used to conduct the test. The results indicate three things. First, the ePWM is capable of emitting the required gating pulse. Second, the optocoupler circuit is capable of amplifying the gating pulse. Third, the driver is capable of applying the required gate-emitter voltage during both the on-state and off-state. However, the results also show that the there is a substantial turn-off delay between the ePWM and optocoupler output. The fall-time is also quite large compared to the turn-on.

A large delay and fall-time in the propagation of the gating signals can have a substantial effect on the response of the system. The delay can cause instability in the controller and cause switching errors. For example, if the duty cycles are high enough, the IGBTs might never completely turn off before transitioning to the on-state. This is a likely scenario considering that the turn-on is much faster than the turn-off, which the test results substantiate. Furthermore, the test results also show that the ePWM module is able to output a maximum voltage of only 2.1 V, which is 36% lower than what the optocoupler circuit is expected to handle. This might explain the prolonged fall-time. Nevertheless, the results show that the optocoupler circuit is able to register the 1.2 V input, and output a voltage of 14.5 V to the connected driver.

The threshold input voltage for the connected driver is 15 V. However, the minimum threshold voltage is 12.5 V. The driver is therefore still able to register the 14.5 V input during turn-on. The voltage difference of 0.5 V might indicate that the external DC supply, which supplies both the optocoupler circuit and driver cards, is adjusted too low or unable to deliver the required power. Still, the driver is able to register the input and output 14 V to the IGBT gate-emitter. During turn-off, the driver applies a voltage of −8 V at the gate-emitter. The driver is therefore able to apply the correct voltage and is working as expected.

5.2.2 Measurement Circuits and Digital Sampling

All the measurement circuits in the prototype system were tested to determine their performance and accuracy. The measurement results from the DC measurement circuit can be seen in section 4.1.5, where a DC voltage of 600 V was applied to the circuit and compared to its equivalent down-scaled analog output voltage. Similarly, the AC voltage measurement circuits were tested in section 4.2.3, where a 230 V RMS voltage was applied to every circuit. In section 4.2.4, a 5 A RMS current was used to test two of the current measurement circuits, while the remaining circuit was tested with a higher current around 6.3 A.

The results from the DC voltage measurements indicate that the circuit is able to provide accurate measurements. However, this is not the case for the AC measurement circuits. According to the results, both the AC voltage and current measurement circuits are unable to accurately measure the positive halves of the inputted waveforms. More specifically, the voltage circuits are unable to measure above 200 V, while the current measurements saturate at around 5 A. Considering that the error is common in all the circuits and that all the AC circuits are designed in a similar manner, the design methodology might be faulty. Another reason might be an insufficient DC supply. The measurement circuits contain transducers and op-amp ICs that require an external DC supply. If these components receive an insufficient voltage or current, it may affect the accuracy of the measurements. Either way, the error can to some extent be corrected through software algorithms. Results from software tests substantiate this claim.

To test the performance of the ADC process, the outputs from the AC measurements circuits were sampled at the analog input pins of the MCU and processed in software (digitally sampled). It was also attempted to correct the measurement errors through MATLAB scaling functions. Simulink was used to program and log the digital signals in real time. The software model was presented in section 4.3.1, and the digital measurement results was presented in section 4.3.2.

The results show that the ADC modules are able to successfully sample the input AC voltages and currents. The results also indicate that any initial measurement error from the physical measurement circuits can be corrected with MATLAB scaling function. However, it is not safe to assume that the scaling functions are sufficient for correcting saturation errors. It might be sufficient in the case of correcting the voltage error, but not necessarily the current error. This is because the voltages are expected to stay constant for the duration of the operation, while the currents might change during start-up of the system or changes in load.

5.2.3 PLL and Coordinate Transformation

The PLL algorithm was tested in section 4.3.3, and the results indicate that the algorithm was able to successfully extract the phase angle from the digitally sampled voltage measurements. The PLL output is important for synchronizing the rectifier to the grid. Furthermore, the phase angle is used in the Clarke and Park coordinate transformation.

The software algorithms for the Clarke and Park transformation were tested in section 4.3.4. The results show that the algorithms are able to transform the three-phase voltages to the stationary and synchronous reference frames. However, the results also show that there are some substantial oscillations in the dq signals. In theory, the dq components are supposed to represent DC quantities. Oscillations are therefore quite unfavourable, as they can cause instability in the control system.

6 Conclusion

This thesis aimed to design a 20 kW bidirectional three-phase rectifier for EV charger applications. A complete topology was proposed by comparing several conventional rectifiers and control schemes. The proposed topology consists of an AFE rectifier, and the control scheme is based on VOC. A PLL algorithm is used to extract the phase angle from the grid voltages and synchronize the switching of the rectifier. The rectifier bridge consists of six IGBTs, and SVM is used as the switching scheme. The rectifier topology includes a LCL filter for filtering out the switching harmonics. A mathematical model of the rectifier was presented, and the complete system was modelled in Simulink. Several simulations were conducted to investigate the performance and bidirectional capabilities of the system. The system was tested with an increasing step load during rectification and inversion. The transient and steady state response of the controller was investigated during the increasing step loads. Furthermore, a FFT analysis was conducted for each load scenario to investigate the performance of the LCL filter.

The simulation results indicate that the system is capable of bidirectional flow. More specifically, measurements show that the system is able to reach UPF during rectification and transition into inversion with a leading PF. The controller is able to maintain a DC voltage of 600 V during nominal load conditions. Furthermore, the controller is also able to adjust to an increasing step load, well above its intended operating point. According to the results, the transient and steady state response of the controller deteriorates during off-nominal load conditions, i.e., larger settling time, ripple voltage, and $\mathrm{THD_i}$. The results also show that the LCL filter is able to attenuate the current harmonics to a acceptable level in accordance with the IEEE standards.

An experimental prototype was built for the purpose of investigating the simulated results. The working principle behind all the hardware components and software was described in detail. Tests were conducted to investigate the performance of the hardware and software algorithms. The test results indicate that further research is needed in order to conclude that the system is appropriate for practical implementation.

Suggestions for Further Work

As discussed in chapter 5, some noticeable observations were made during testing of the hardware components and software algorithms. For instance, there was some substantial turn-off delay between the gating signal emitted from the ePWM module and optocoupler circuit. It could be interesting to investigate the source of this delay and attempt to minimise it if possible. However, the test results also showed that the ePWM voltage was lower than expected. It is possible that this is the source of the error and it is therefore recommended to investigate if there is a connection between the voltage level applied to the optocoupler input and fall-time of the output signal. A more obvious reason for the delay might be an insufficient DC supply.

The AC measurement circuits should be further investigated. These exhibited some inaccuracy in measuring the positive peak amplitudes of the input waveforms. The error seems to be common for both the voltage and current measurements. Considering that the circuits have a similar design, this might indicate that the design is faulty. Another reason might be insufficient supply. These aspects should be taken into account when investigating the source of the error.

Results from the real-time software tests showed that the algorithm used for coordinate transformation of the AC voltage measurements were unable to output stable DC values in the synchronous reference frame. The digital sampling process of the ADC inputs should therefore be investigated further. However, the fault might actually lie in the PLL algorithm. There might be a steady-state phase error present, even though the PLL output was able to synchronize to the grid frequency. This should therefore also be investigated.

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A Matlab Code

A.1 Filter Calculations

```
%% SYSTEM
Vs = 230;
P = 20e3;
fg = 50;
fsw = 5e3;
Lg = 13e-3; % estimation in weak grid conditions

Vll = Vs*sqrt(3);
w = 2*pi*fg;
w_sw = 2*pi*fsw;

%% max inductor value
% Should be 0.1 pu of base value
Ltmax = 0.1*Vll^(2)/(2*pi*fg*P);

%% minimum DC-link voltage
Ismax = P/Vll; % safer with 20% reduction (sqrt(2/3))
Vrmax = sqrt((Vs*sqrt(2))^(2)+(Ltmax*w*Ismax)^(2));
Vdc = sqrt(3)*Vrmax; % for SVM
Vdc = roundn(Vdc,2); % Round up dc voltage (conditional)

%% max filter capacitance
Cfmax = 0.05*P/(w*Vll^(2));
Cf = Cfmax *0.5; % recomended

%% Converter side inductor
Iimax = Ismax; % for high frequencies
Isat = Iimax + 10; % (conditional)
i_rip = (Isat-Iimax)*2;
RF = i_rip/Iimax; % Converter side ripple factor
Lrmin = Vdc/(6*fsw*i_rip);
Lr = 0.4 * Ltmax;

if(Lr <= Lrmin)
```

```
    error('Inverter side inductor too small, try increasing ...
        ripple current or total inductance')
end

%% CALCULATIONS FOR GRID SIDE INDUCTOR
Lsmax = Lg; %weak grid
Lgmin = 0; %stiff grid
% capacitor accuracy range (5%)%
Cfmax = Cf*1.05;
Cfmin = Cf*0.95;
%constants
a_max = (Ltmax/Lr) - 1;
a1 = Lr*Cf*w_sw^(2)-1;
a2 = Lr+a1*Lsmax+a1*Lr;
a3 = (Lr+a1*Lsmax)*Lr*Cfmax;
b2 = Lr+a1*Lgmin+a1*Lr;
b3 = (Lr+a1*Lgmin)*Lr*Cfmin;
%attenuation conditions derived from freq range
delta_1 = ...
    (36*Lr-(2*pi*fsw*Lr)^(2)*Cfmax)/(a3*(2*pi*fsw)^(2)-36*a2);
delta_2 = (4*Lr-(2*pi*fsw*Lr)^(2)*Cfmin)/(b3*(2*pi*fsw)^(2)-4*b2);
delta_min = 1/abs(1+a_max*a1);
if(delta_1 > delta_2)
    delta_max = delta_1;
else
    delta_max = delta_2;
end

%% Filter value
delta = 0.07; %lower delta gives lower THD
Ls = Lr*(1+delta)/(delta*a1);

%% Freauency range and filter verification
f_res = (1/(2*pi)) * sqrt((Ls+Lr)/((Ls)*Lr*Cf));
f_res_min = (1/(2*pi)) * ...
    sqrt((Ls+Lsmax+Lr)/((Ls+Lsmax)*Lr*Cfmax));
f_res_max = (1/(2*pi)) * ...
    sqrt((Ls+Lgmin+Lr)/((Ls+Lgmin)*Lr*Cfmin));
fc_min = fsw/6;
fc_max = fsw/2;

if (10*fg >= fc_min || fc_min > f_res || f_res > f_res_max || ...
    f_res_max > fc_max)
    error('Frequency range condition not met')
```

```
end

if (delta > delta_max || delta < delta_min)
    error('Attenutaion constant outside valid range')
end

if ( 1/(w*Cf) < w*Ls*10)
    error('Filter capacitor impedance too small')
end
if (10/(w_sw*Cf) > w_sw*Ls)
    error('Grid side inductor impedance too small')
end
```

A.2 Space Vector Modulation

A.2.1 dq2αβ

```
function [Valpha, Vbeta, theta] = ...
    dq2ab(Vd, Vq, Theta)
Valpha = Vd*sin(Theta) + Vq*cos(Theta);
Vbeta =  -Vd*cos(Theta) + Vq*sin(Theta);
theta = atan2(Vbeta, Valpha);
```

A.2.2 Vr

```
function Vr = Vr(Valpha, Vbeta)
Vr = sqrt(Valpha^2+Vbeta^2);
```

A.2.3 Sector

```
function n = Sector(theta)
n=0;
if(theta>0)&(theta<pi/3)
n=1;
end
if(theta>pi/3)&(theta<=2*pi/3)
n=2;
```

```
end
if(theta>2*pi/3)&(theta<=pi)
n=3;
end
if(theta<=0)&(theta>=-pi/3)
n=6;
end
if(theta<=-pi/3)&(theta>=-2*pi/3)
n=5;
end
if(theta<=-2*pi/3)&(theta>-pi)
n=4;
end
```

A.2.4 Phi

```
function phi = Phi(n, theta)
phi=0;
if(n==1)
phi = theta;
end
if(n==2)
phi = theta-pi/3;
end
if(n==3)
phi = theta-2*pi/3;
end
if(n==6)
phi = pi/3+theta;
end
if(n==5)
phi = 2*pi/3+theta;
end
if(n==4)
phi = pi+theta;
end
```

A.2.5 Dwell

```
function [T0, T1, T2] = Dwell(Vr, phi, ... Vdc, T)
a = Vr/Vdc;
T1 = T*a*sin(pi/3-phi)/sin(pi/3);
T2 = T*a*sin(phi)/sin(pi/3);
T0 = T-T1-T2;
```

A.2.6 DC

```
function [S1,S2,S3]  = DC(T0,T1,T2,Ts,n)
S1=0;
S2=0;
S3=0;
if(n==1)
S1=(T1+T2+T0/2)/Ts;
S2=(T2+T0/2)/Ts;
S3=(T0/2)/Ts;
end
if(n==2)
S1=(T1+T0/2)/Ts;
S2=(T1+T2+T0/2)/Ts;
S3=(T0/2)/Ts;
end
if(n==3)
S1=(T0/2)/Ts;
S2=(T1+T2+T0/2)/Ts;
S3=(T2+T0/2)/Ts;
end
if(n==4)
S1=(T0/2)/Ts;
S2=(T1+T0/2)/Ts;
S3=(T1+T2+T0/2)/Ts;
end
if(n==5)
S1=(T2+T0/2)/Ts;
S2=(T0/2)/Ts;
S3=(T1+T2+T0/2)/Ts;
end
if(n==6)
S1=(T1+T2+T0/2)/Ts;
S2=(T0/2)/Ts;
S3=(T1+T0/2)/Ts;
```

```
end
```

A.3 Clarke and Park

A.3.1 abc2αβ

```
function [alpha, beta] = fcn(a, b, c)
alpha = (2*a-b-c) * 1/sqrt(6);
beta = (b-c)*1/sqrt(2);
```

A.3.2 αβ2dq

```
function [d, q] = fcn(alpha, beta, wt)
d = alpha*sin(wt) - beta*cos(wt);
q = alpha*cos(wt) + beta*sin(wt);
```

A.4 Measurement Scaling

A.4.1 AC Voltage

```
function Vx = VADC(Dv,evp,evn,C)

if Dv*3/4095 >= 1.5
e = evp;
else
e = evn;
end

Vx = ((Dv*3/4095 - 1.5) * (360+e)/1.5) + C;
```

A.4.2 AC Current

```
function Ix = IADC(Di,eip,ein,C)

```

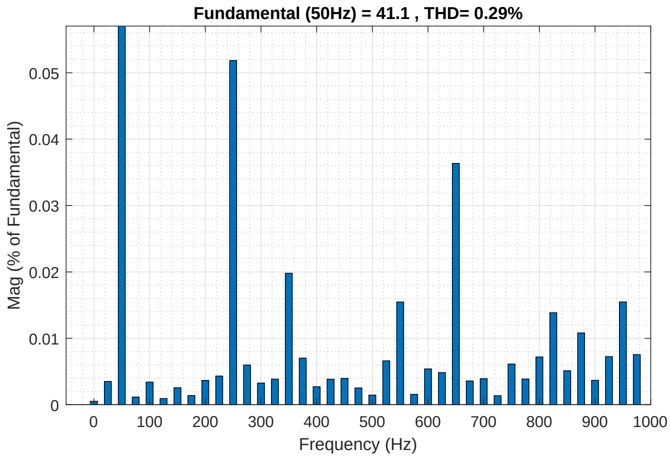
```
        if Di*3/4095 >= 1.5
        e = eip;
        else
        e = ein;
        end

        Ix = ((Di*3/4095 - 1.5) * (10.65+e)/1.5) + C;
```

B Fast Fourier Transform Analyses

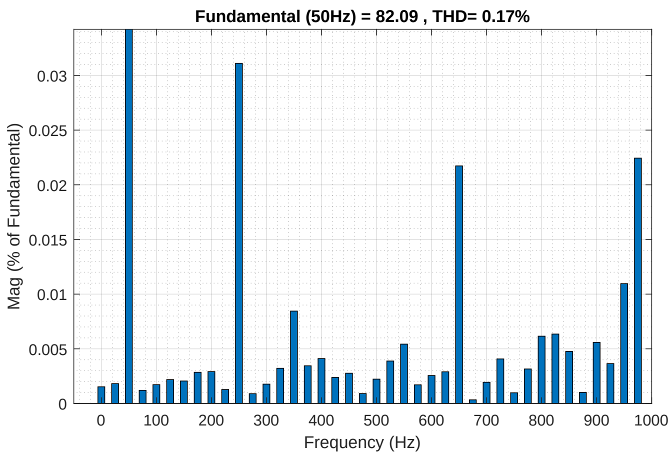
These are all the FFT analyses conducted for the various load conditions in section 3.3.

B.1 Rectification

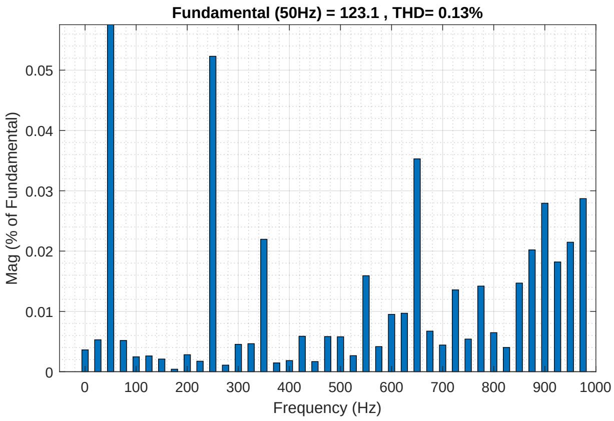
B.1.1 20 kW



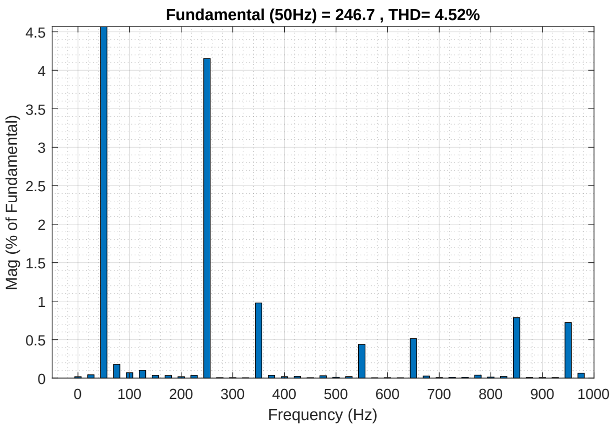
B.1.2 40 kW



B.1.3 60 kW

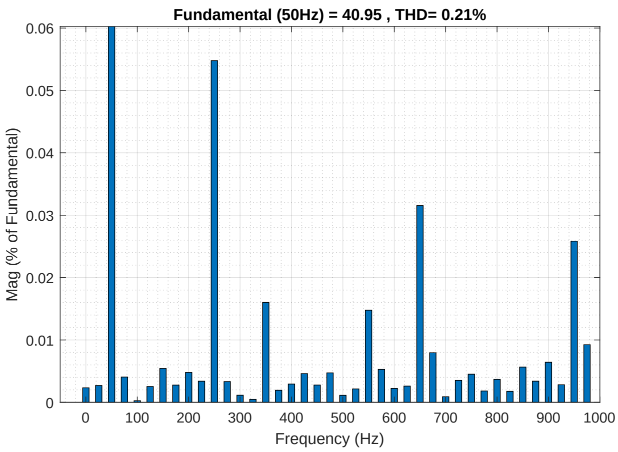


B.1.4 120 kW

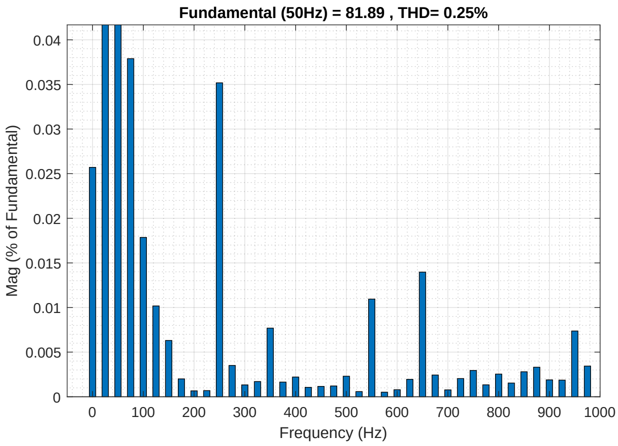


B.2 Inversion

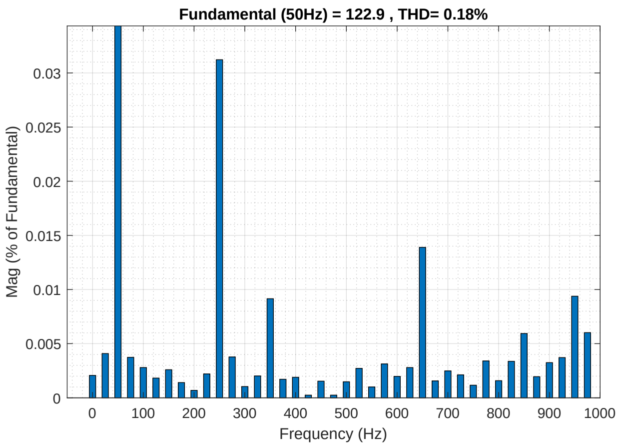
B.2.1 20 kW



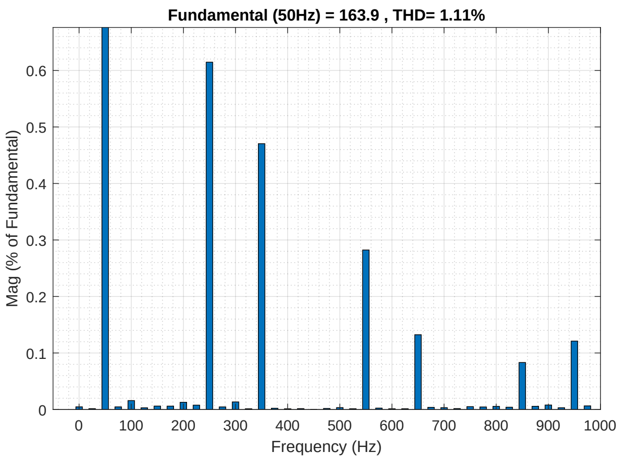
B.2.2 40 kW



B.2.3 60 kW

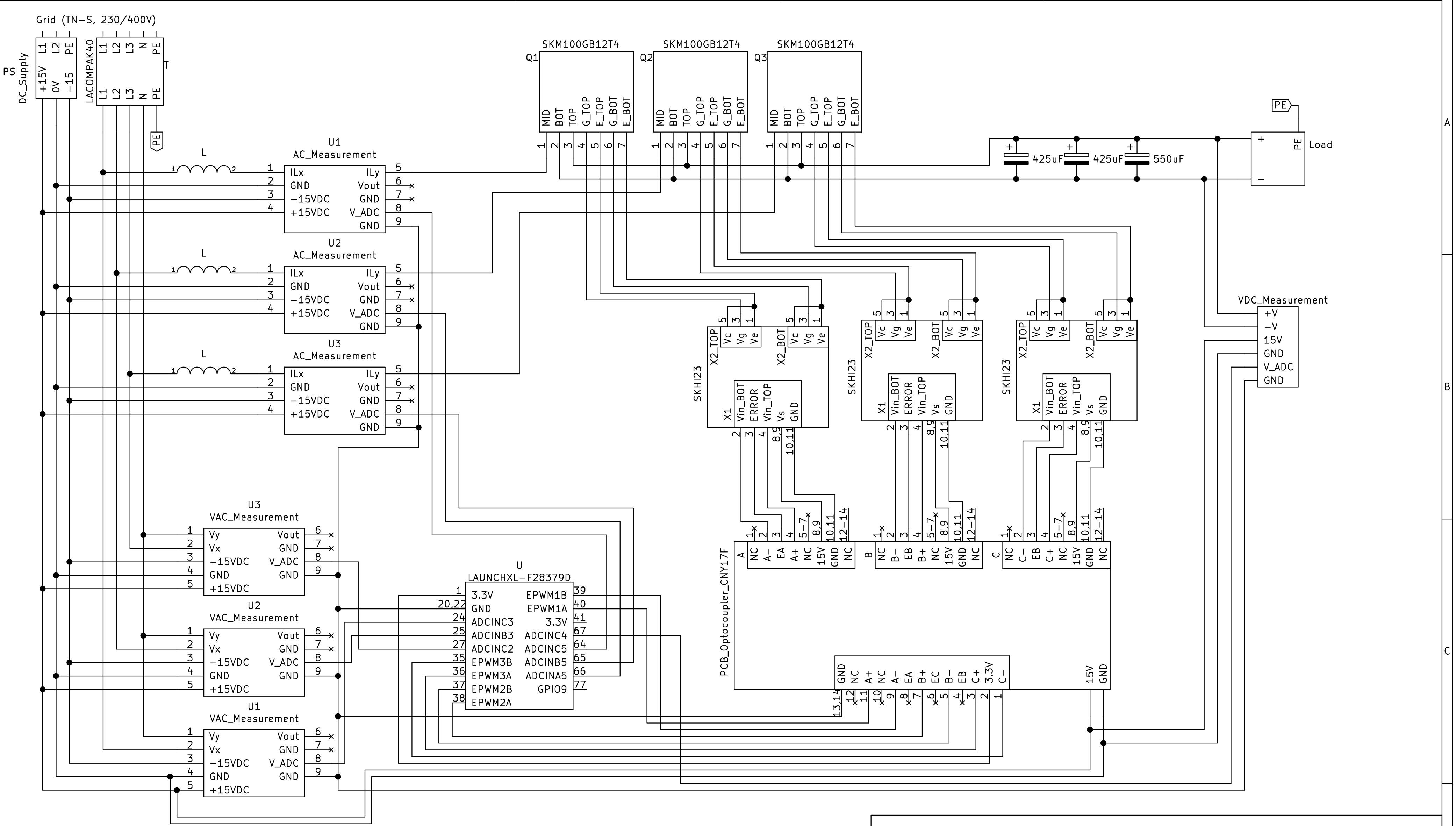


B.2.4 80 kW



C

Wiring Diagram



Sheet: /
File: Prototype.sch

Title: Prototype System

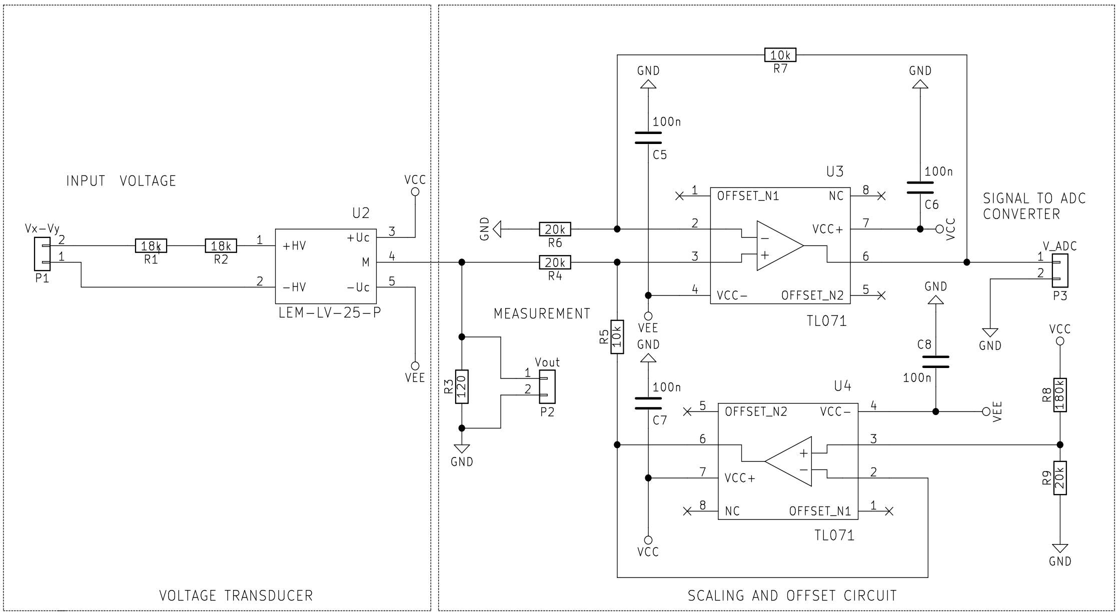
Size: A4 Date: Rev:

KiCad E.D.A. kicad (5.1.7)-1 Id: 1/1

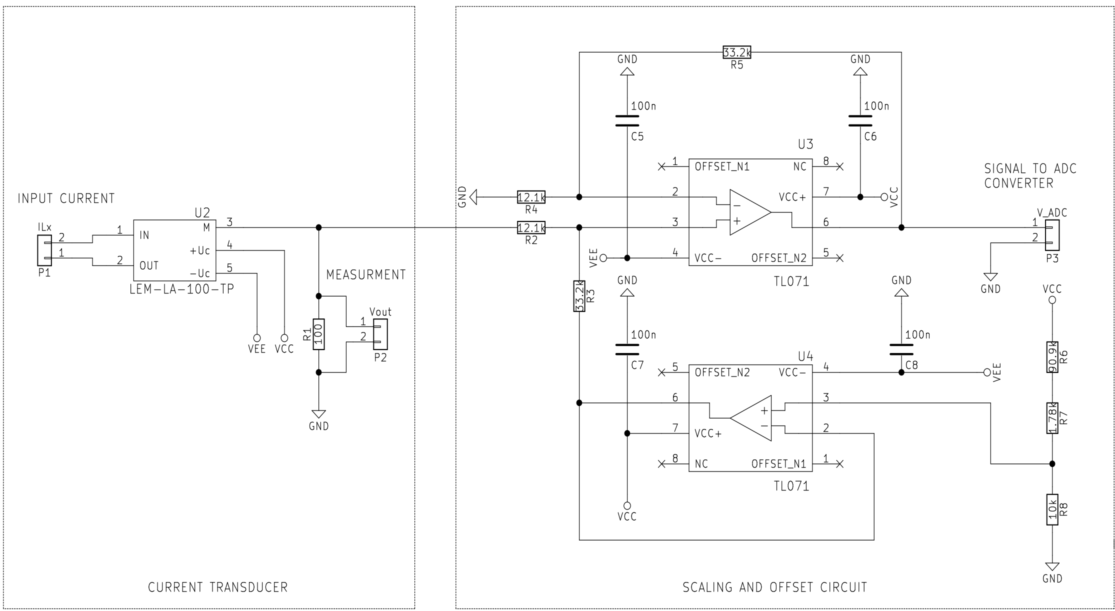
C.1 AC Measurement Circuits

The AC measurement circuits have been designed and drawn by Andreas Sagedal [23].

C.1.1 Voltage Measurement



C.1.2 Current Measurement



D Datasheet

The available datasheets are listed below. Click the respective paper-clip icon to open the PDF.

- IGBT driver-card SKHI23
- IGBT module SKM100GB12T4
- Optocoupler CNY17F
- Voltage transducer LV 25-P
- Current transducer LA 100-TP