Setup and Integration of the Readout Electronics for the Pixel Layers of the New ALICE FoCal Detector

Thomas Arnesen Økland

Master's Thesis of Physics
Department of Physics and Technology
University of Bergen

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Abstract

The Forward Calorimeter (FoCal) sub-detector is a planned upgrade to the A Large Ion Collider Experiment (ALICE) at CERN. It is currently in a initial design phase, where, amongst others, simulations and irradiation tests provide data for performance analysis. These results are crucial for the Technical Design Report (TDR), which needs a final approval from the LHC Experiment Committee (LHCC).

The FoCal detector will provide ALICE with the capability of detecting subatomic particles in a completely new direction from the particle collisions. Whenever two particles collide, without exactly symmetrical momentum, the resulting elementary particles will not be captured by any currently existing detector. The FoCal detector will fulfill this need and this feature could lead to a new, deeper understanding of our physical world.

This thesis will reflect upon the work done in advance of a beam test. The test will measure the performance of an early prototype of the final FoCal sub-detector in a radiation environment. The prototype needs to incorporate new pixel layers, using the ALICE Pixel Detector (ALPIDE) chips from the Inner Tracking System 2 (ITS2) upgrade. These chips are arranged into a new topology, which requires the use of a special card to reroute the data stream. Together with these chips, the electronic readout system from ITS2 will provide the necessary infrastructure to support the data-taking processes. Therefore, this work revolves around obtaining knowledge of how the readout system of ITS functions and applying this knowledge in order to gather valuable data in a beam test. The beam test took place at the Super Proton Synchrotron located at CERN in September - October 2021.

The beam test turned out to be mostly successful. Some of the chips for the pixel layers turned out to be non-working with insufficient time to fix them. The remaining working chips still provided results important in assessing the chip performances. After returning to Bergen, investigation into the problematic chips provided understanding into why they were not working.

Acknowledgements

First, I would like to thank my supervisor *Professor Johan Alme* for always having the patience to discuss whatever I do not fully understand. I would also like to thank my two co-supervisors *Professor Kjetil Ullaland* and *Associate Professor Constantin Loizides* for providing valuable input to my thesis.

With this project, I got the opportunity to participate and play an essential role in a beam test at CERN in Switzerland. Being there for three weeks working with the detector setup was incredibly fun and an experience I will not forget. With this, I want to thank all the incredible people I got to meet from all over the world. A special thanks to *Viljar Nilsen Eikeland* for being a great companion and friend every single day of those three weeks. A huge thanks to *Dr. Ola Slettevoll Grøttvik* for all the help surrounding the setup. Thanks to *Tea Bodova* and *Bendik Husa* for reading my thesis and not holding back on comments.

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Thomas Arnesen Økland
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Contents

1 Introduction

CERN is the European organization for nuclear research and hosts the Large Hadron Collider (LHC), the largest particle accelerator globally. This accelerator lies inside an underground tunnel with a circumference of 27 kilometers and contains four detector experiments. One, in particular, is the A Large Ion Collider Experiment (ALICE) detector.

ALICE studies the Quark-Gluon Plasma (QGP), which dominated our universe the first few microseconds after the Big Bang [1]. At that moment, the temperatures were so extreme that quarks and gluons could not combine to form the hadrons that make up the universe we know today. ALICE attempts to recreate this state by colliding heavy nuclei, ^{208}Pb, at ultra-relativistic energies and using an array of different detectors to track and analyze the resulting sub-atomic particles and their evolution. Figure 1.1 displays a schematic view of the detectors.

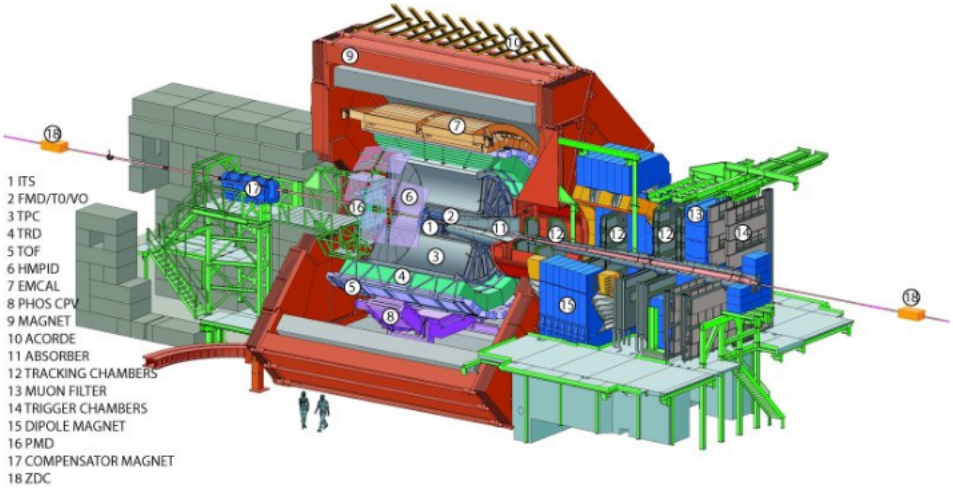


Figure 1.1: Schematic of the ALICE detector in its Run 1 and 2 configuration [2].

Data-taking is divided into runs with Run 3 of the LHC starts in 2022 after Long Shutdown 2 (LS2). During LS2, ALICE received several upgrades to its detectors. Figure 1.2 shows the current plan for the future of operation for the LHC. Regardless, the development for new upgrades for Run 4 has already begun, and one of the upgrades is the FoCal sub-detector.

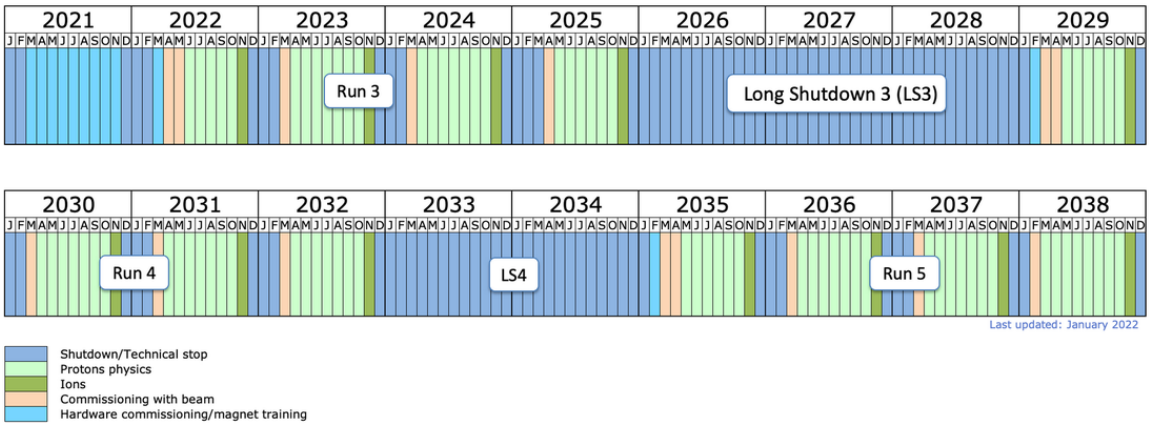


Figure 1.2: Current plan of Runs and Shutdowns [3].

The Forward Calorimeter (FoCal) sub-detector is one of ALICE's planned upgrades. The design will measure particles flying from the impact point of a collision at a sharp angle from the beam pipe. The FoCal sub-detector separates into three parts. The first part consists of several low spatial resolution sensor layers, the second part consists of two high spatial resolution sensor layers, and the last part is a hadronic calorimeter. The first two parts will be referred to as FoCal-E in this thesis, as these are part of an electromagnetic calorimeter that measures the energy levels of incoming electromagnetic radiation. The last part will be referred to as FoCal-H, as this is a hadronic calorimeter that measures the energy levels of incoming hadronic particles. The pixel layers will refer to the high-resolution layers, and the pad layers will refer to the low-resolution layers throughout this thesis.

The two high-resolution sensor layers will utilize the ALICE Pixel Detector (ALPIDE) chips to track incoming particles. These chips are designed for the LS2 upgrade of the Inner Tracking System (ITS), located at the center of ALICE. The readout electronics required to extract all data produced by the ALPIDE chips need a fast readout scheme to accommodate a high impact rate. In September - October 2021, at the SPS at CERN, an early prototype of the FoCal underwent testing in a radiation environment. For this test, the exact readout electronics in use by the ITS provided the necessary infrastructure for the two high-resolution custom sensor layers.

1.1 Detector Design Process

A new (sub)detector at LHC often originates from a physics problem someone desires to solve or, at the very least, investigate. These inspirations may spur from the shortcomings of current detectors, or they may come from a theoretical standpoint. Regardless of how the idea came into being, the goal is to uncover a new field, region, area, or part of physics. For FoCal, the new idea introduced is placing the detector at a forward position to explore new particle collision regions.

The first step is to produce a technically detailed idea of how to make this new detector. It is paramount to understand the current technological equipment available and what may be available in the foreseeable future. This new detector will push the technical requirements to their limits. Computer simulations can provide some initial information

about the requirements needed. Physical testing along the way of development is also critical to confirm that everything works together. If any fundamental design flaws appear, they are easier to solve early in the development when there is time to alter the design.

For the new detector to be approved and then to secure the proper funding necessary to produce it, a Letter of Intent is produced by the project team. This document describes everything about the new detector. What type of physics the detector aims to study, and why this is important or relevant. Results from early simulations map out the status of equipment available to date or estimate how much improvement is needed. Simulations provide a basis for a proposal of what equipment to use and if any research and development is necessary, including an estimate of the cost required to develop, test, and build the entire detector. These estimates are in terms of money, time commitment, and other resources, i.e., computing power and data storage. The LHC Experiment Committee (LHCC) will review the letter, and if the project is approved, the work carries on with getting funding and creating a Technical Design Report (TDR).

Funding is always a challenge, as it is usually a limiting factor for most projects. For ALICE upgrade projects, funding is determined by counting how many participating members are involved from each country and dividing it by the total. This method outputs a fraction, representing the fraction of a country's cost to the project. Representatives from each country then have to write an application for funding to their research council and ask for the amount needed. Depending on the strength of the application, then the necessary funds are granted.

In parallel with gathering the required funds, producing a TDR is initiated. The TDR will encapsulate all aspects of the final design, including early prototyping and exposing them to beam tests to measure their performance in radiation. The prototype starts as a miniature version of the final detector and progressively iterates to reassemble the final detector more and more for each step. Simulations are run in all configurations to generate the best picture of the detector behavior and possibly find problems to fix early on in the development. The TDR will also include a general timeline for the project. The FoCal detector is currently at this step of the process.

After finishing the TDR, the report is reviewed by the LHCC. If accepted and the necessary funding is secured, the project can mass produce all the required components. The installation of the detector in the beam hall can start after producing and assembling all the components. This installation will occur during one of the Long Shutdowns of LHC. When everything is in place, commissioning of the new detector can commence. This step tests all systems of the detector to ensure everything works properly.

The new detector is ready for data taking once the commissioning step is complete. Hopefully, the data produced will lead to new exciting physics that allows a deeper understanding of the universe we inhabit.

1.2 Objective of This Thesis

The FoCal project is in its early stages of producing the required TDR before the LHCC accepts the project entirely as part of ALICE. With this report, a beam test of an early prototype took place at CERN in the autumn of 2021. The team from the University of Bergen has the primary responsibility for the pixel layer of this early FoCal prototype. The beam test goal for the pixel layers was to expose the ALPIDE chips to electromagnetic showers to see how they perform in such an environment. This environment is substantially different from the environment of ITS as the electromagnetic showers create a lot of second-hand particles from scattering. Therefore, the occupancy effects on the ALPIDE chips are a vital metric to simulate and test. A higher hit rate will mean more data to read out, which will effectively limit the trigger rate in order to avoid occupancy effects.

The pixel layers of FoCal are planning on using the same ALPIDE chip as designed for the newly upgraded ITS2 at ALICE. With the upgrade comes a new electronic readout system. FoCal will use this system for the beam test as it fully supports the readout process of the ALPIDE chips. Eventually, this system will provide a baseline for developing a more specific readout scheme that fits the FoCal detector better. Regardless, an understanding of how the ITS system works is crucial for the operation of the early prototypes in the beam tests. The ITS system constitutes several different components that each has its dedicated role and is necessary to function. By understanding how the whole system works, the chip, and the components supporting the readout process, the problems that might occur will be easier to understand.

The work done for this thesis includes learning how the ITS readout system works and introducing a triggering system and more readout cards in the UiB lab setup for the first time. Also, making essential modifications to the software used to control the system to accommodate the newly introduced components. The work done testing the ALPIDE chips, provided the opportunity of finding fixable issues prior to the beam test. In hindsight, time constraints delayed the testing until after the beam test. Finally, the general knowledge of the system helped resolve any issues that appeared prior, during, and after the beam test.

1.3 Outline

Chapter 2 - Long Shutdown 2 Upgrades will describe the newly upgraded ITS2 readout system. This chapter includes a short description of components used during the beam test for FoCal and a thorough description of how the operation of the ALPIDE chip works.

Chapter 3 - Long Shutdown 3 Upgrades will describe a picture of how the fully developed FoCal plans to function and operate. It will also discuss some challenges that need solving before finalizing the complete design.

Chapter 4 - SPS Beam Test will shed some more detail on why beam tests are essential in the development of a new detector. The chapter will include a description of the FoCal setup for this beam test. This chapter will also discuss much of the preparation done regarding getting the pixel layers ready for data taking in the beam test.

Chapter 5 - Beam Test Results will present the performance results of the chips at the beam test. This chapter will include the beam energies exposed onto the chips, problems that occurred during the runs, and the state of the chips in the beam test aftermath.

Chapter 6 - Conclusion, and Outlook will give a conclusion and an outlook for the next beam test and possibly the final detector.

2 Long Shutdown 2 Upgrades

In the period of 2019-2021, the LHC had its Long Shutdown 2. During this time, several of the ALICE sub-detectors underwent substantial upgrades. Most notably is the upgrade of Time Projection Chamber (TPC) and the upgrade to ITS2. This chapter focuses on the ITS2 upgrade.

2.1 ALICE ITS2

As mentioned in the introduction, ALICE is an experiment designed to study the QGP [4]. The experiment comprises several different sub-detectors with their functionality and purpose. One of these detectors, in particular, is the ITS.

The ITS is the detector located closest to the Interaction Point (IP)[1] of all the detectors at ALICE [6]. The ITS provides four essential functions for ALICE:

- Pin-pointing the primary vertex with a resolution of 100 μm, or better.
- Reconstructing secondary vertices required for charm and hyperon decay reconstruction.
- Tracking and identifying low-momentum particles.
- Improving the momentum and angle tracking of particles reconstructed by the TPC.

In 2021, the ITS completed several upgrades. A Monolithic Active Pixel Sensor (MAPS)[2] chip, known as the ALPIDE chip, now acts as the core of the detector. The design distributes a total of 24,120 individual chips across seven different layers [8]. Figure 2.1 shows the structure of ITS around the beam pipe.

[1]The Interaction Point is the location where particles collide in a particle accelerator experiment. Additionally, the primary and secondary vertices are the reconstructed locations of individual particle collisions. [5]

[2]Monolithic Active Pixel Sensor is a technology which incorporates the sensor into the CMOS technology. This has several advantages over the previous Passive Pixel Sensor technology. Some of these advantages are lower power consumption, smaller pixel sizes and radiation hardness. [7]

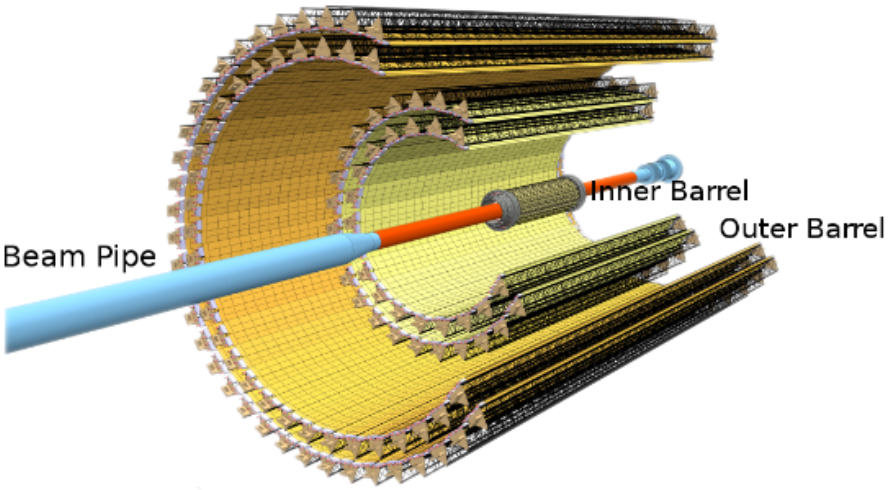


Figure 2.1: The Inner Tracking System in use at ALICE [2].

2.2 ITS Readout System

The electronic readout system, responsible for transmitting data from the front-end electronic sensors to the data storage facilities at CERN, is made up of several different components [9]. These components handle everything from distributing timing information across ALICE, streamlining data to central nodes, and organizing data from different sensors into coherent packets. Figure 2.2 shows a schematic overview of the ITS readout system for an Inner Barrel module. ITS uses Power Units (PU) and Power Supply Units (PSU) to supply two staves per PU with power.

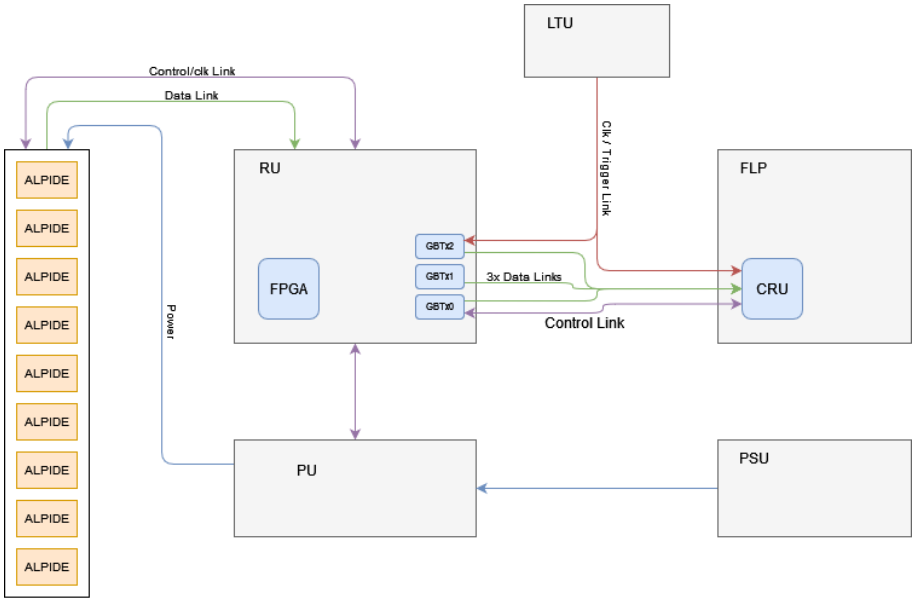


Figure 2.2: A schematic overview over the ITS readout system.

2.2.1 ALPIDE

The core component of ITS is the front-end ALPIDE chip. These chips are placed in the seven layers making up the ITS, see Figure 2.1. Two outer layers, two middle layers, and

three inner layers make up the seven ITS layers. MAPS technology forms the basis of the chips, which incorporates the analog pixel sensor technology into the digital CMOS technology [8]. Each chip has a pixel matrix of 512 x 1024 individual pixels distributed over an area of 1.5 x 3 cm^2, resulting in a pixel size of approximately 28 x 28 μm^2. Each pixel has an analog front-end capable of collecting charge generated by an ionizing particle striking the substrate. When enough charge is collected, a digital hit can be registered. Whenever the ALPIDE chip receives a trigger from an external source, it asserts a strobe signal. The chip will only register the hits it collects if a trigger asserts a strobe signal simultaneously. All pixels on the chip receive the strobe signal simultaneously. The duration of the strobe signal is configurable. When the strobe signal is de-asserted, the chip will read out all hits with their corresponding coordinates and transmit the data upstream in the readout chain. Section 2.3 discusses further details of the functions of the ALPIDE. Figure 2.3 shows an image of nine ALPIDE chips.

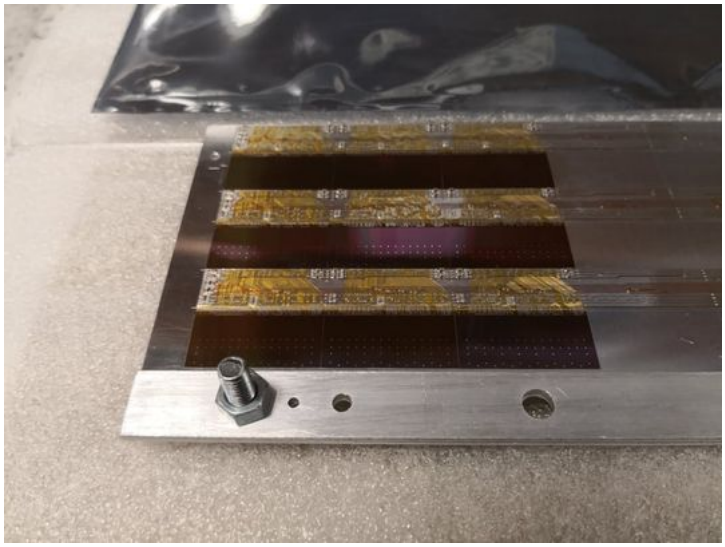


Figure 2.3: Image of nine ALPIDE chips in a three by three matrix.

2.2.2 RU - Readout Unit

Upstream in the readout chain from the ALPIDE chips sits a Readout Unit (RU). This card is responsible for direct communication in the forms of control, trigger, and data handling with several chips [10]. In total, the ITS upgrade uses 192 RUs to accommodate all the chips. The RUs handle either nine chips, in Inner Barrel (IB) mode, shown in Figure 2.2, or 196 chips, in Outer Barrel (OB) mode, each, depending upon the location of the chips. The 196 chips are distributed over 28 data links. Chips close to the IP expect a higher hit rate and generate more data than chips located further away from the IP. The location of the chips dictates the readout mode of the RU. Each RU has three GigaBit Transceiver (GBTx) ASIC modules that transmit data upstream at a payload rate of 3.2 Gbps, for a total of 9.6 Gbps. The GBTx is an optical transceiver chip designed by CERN to be radiation hardened and capable of high data transmission rates. In total, there are three optical links for data transmission, one for trigger information and one for control. The RUs also control Power Units in the system. These Power Units control the voltage levels of the ALPIDE chips. At the center of the RU lies an FPGA. The FPGA acts as the central processing component of the board.

The RU is also responsible for receiving and handling triggers from the Local Triggering Unit (LTU). These triggers contain general timing information and indicators, which dictate whether the RU will trigger the ALPIDEs. After the RU sends a trigger to the ALPIDEs, it waits a configurable period for a packet from the chips containing their data. When this data arrives, the RU adds important timing information and forwards the packet upstream to a Common Readout Unit (CRU). The timing information is essential for synchronizing the hit data from across ALICE. Figure 2.4 displays an image of an RU.

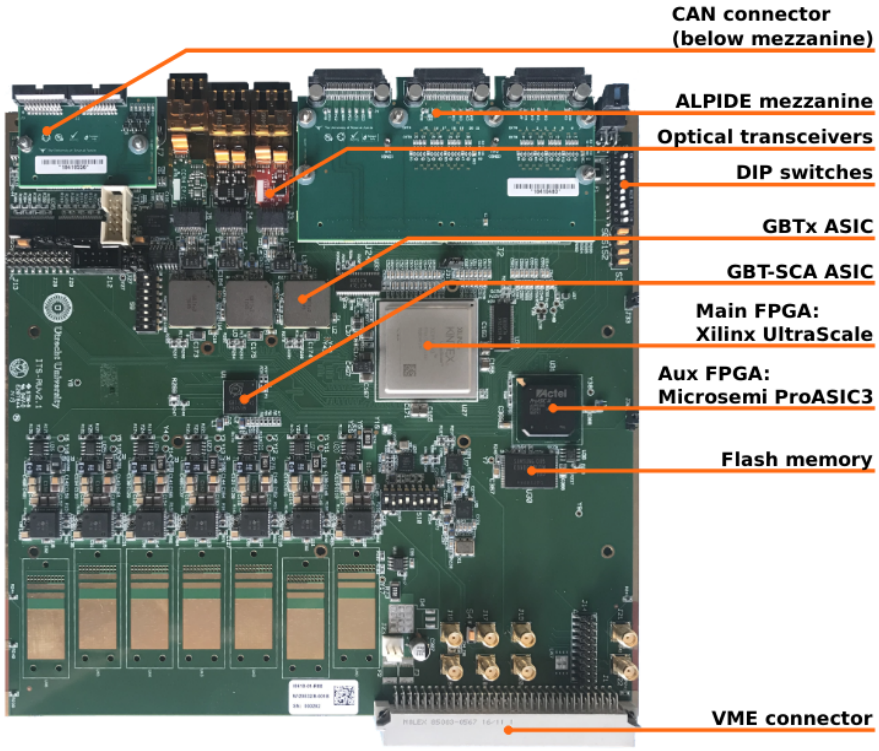


Figure 2.4: An image of a Readout Unit v2.1 board [11].

2.2.3 LTU - Local Trigger Unit

The LTU distributes triggers, clocks, and general timing information from a higher level trigger distribution system, the Central Trigger Processor (CTP) [12]. This system encompasses several detectors at ALICE. Each CRU connects to one LTU via a Passive Optical Network link, and each RU connects via a fiber optic GBTx link. These links distribute the trigger and timing information. The LTU encapsulates the information into so-called HeartBeat frames (HBf). The rate of HBf matches the LHC orbit rate at a frequency of 40.08 MHz.

The HBfs builds data sets from ALICE, where 128 HBf make up one Time Frame (TF) [13]. The number of HBf needed to make a TF is configurable, but 128 is the default value. At the beginning of each HBf, the CTP sends out an HB signal with a HeartBeat reject (HBr) flag. The CRU will then either accept or reject the HB packet based on the value of the HBr. In return, the CRU responds with a HeartBeat acknowledgment message whenever a packet successfully transfers to the First Level Processor (FLP).

The triggering system for ITS has two different triggering modes [12]. Either the system is run in continuous mode or triggered mode. In continuous mode, the packets stream in a continuous flow of successive TFs. Each packet contains timing information and flags indicating any errors. According to a Bunch Crossing (BC)[3] rate, the RUs will issue trigger signals to the ALPIDE chips. In this mode, the ALPIDEs have a strobe window length configuration forcing a minimal gap between two strobes.

In triggered mode, packets will only be created and sent whenever the LTU sends a Physics Trigger. A Physics Trigger is generated by other detectors in ALICE when a collision has been detected. The packet will still contain a header with the current timing information. The LTU can either respond by sending a trigger when receiving an external triggering source, i.e., a scintillator, or sending triggers at a fixed rate. The RUs will be configured only to issue a trigger signal to the ALPIDEs when it receives a Physics Trigger from the LTU. In this mode, the ALPIDEs have a short strobe window length because they will receive triggers only when the system knows there is an incoming particle. Therefore, the ALPIDEs only need to take a quick snapshot of their current pixel matrix state. Figure 2.5 shows the packet stream from the LTU in both continuous and triggered mode.

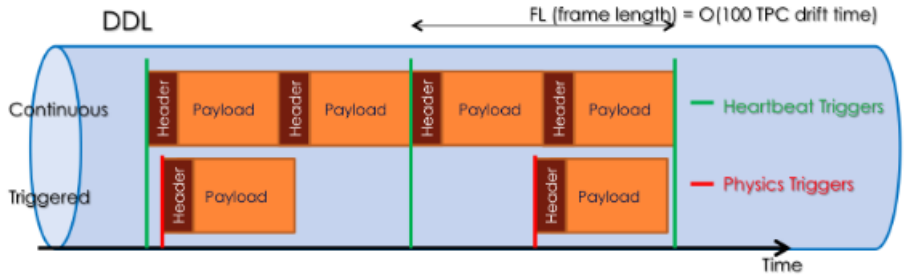


Figure 2.5: HeartBeat and Physics Triggers in continuous and triggered readout mode on a Detector Data Link (DDL) [9].

2.2.4 CRU - Common Readout Unit

The CRU funnels the data stream from multiple RUs to the FLP and ensures consistent timing information. It facilitates communication and data flow with up to eight different RUs. It too receives timing information from the LTU and, in addition, a clock, which it distributes down to the RUs, also. The clock distribution makes the entire system run on a shared clock, which is crucial when receiving data and information from multiple optical fibers. The GBTx fiber optic link functions as the data and control link between the CRU and its RUs.

2.2.5 FLP - First Level Processor

The FLP is a desktop computer that hosts up to two CRU cards [14]. It is responsible for transferring the data from the detector to the computer memory. The FLP incorporates a new Online-Offline (O2) system for data management from the CRUs. It also

[3]Bunch Crossing refers to when two groups of particles crosses path. Each crossing is associated with a BC ID.

functions as an interface for the user to read registers, configure the setup, and check the sub-components' status. The functions necessary to communicate with the components are a part of the Detector Control System (DCS).

2.2.6 CRU_ITS - GIT Repository

A Git repository provides a software package with the tools necessary to operate and communicate with all the setup components in a lab setting. The CRU_ITS GIT repository is for testing a simple setup of the ITS. It contains scripts for initializing the setup, changing configurable settings, and starting a Data Acquisition (DAQ) script. Most of the software is written in Python. A description of the functions used the most during the beam test can be found in Appendix C.

2.3 ALPIDE

This section will discuss how the ALPIDE chip works. Therefore, most of the statements made in this section are based upon its operations manual [15]. If any other sources are used, they are explicitly stated.

2.3.1 Operation Modes

The ALPIDE chip has three different modes of operation. These modes are IB mode, OB Master mode and OB Slave mode. The decision of which mode each chip should be configured to is based on the expected interaction rate, and by extension, the amount of data that is estimated to be generated. The expected interaction rate is heavily dependent on how close to the IP the chip is located. The RUs will also be configured to match its chips. This means that an RU is either configured in IB or OB mode, and therefore, cannot have both IB and OB chips connected to it.

The chips are integrated in sets on staves. An IB module consists of nine chips and an OB stave consists of two OB Master chips with six OB Slaves each. Figure 2.6 shows the layout for both configurations. Each chip has a dedicated 7-bit CHIPID port, which dictates the operation mode of the chip and where on the module the chip is located. The three MSBs of the chip id is used for determining IB or OB mode, with all zeros indicating IB mode. In IB mode, the four LSBs indicate the position of each chip, while in OB mode only the three LSBs tell the position. Bit 3 in OB describes if a particular chip is in the top or bottom row of the stave. All zero for bit 2:0 is the OB Master chip. The mode of the chip is determined in the process of mounting each chip on a stave, physically. Each individual port of CHIPID should either be tied to DVDD, digital supply, representing a digital 1. Otherwise, leave them unconnected, which is equivalent to shorting them to ground, setting the bit to a digital 0. The pads of the ports have internal pull-down resistors.

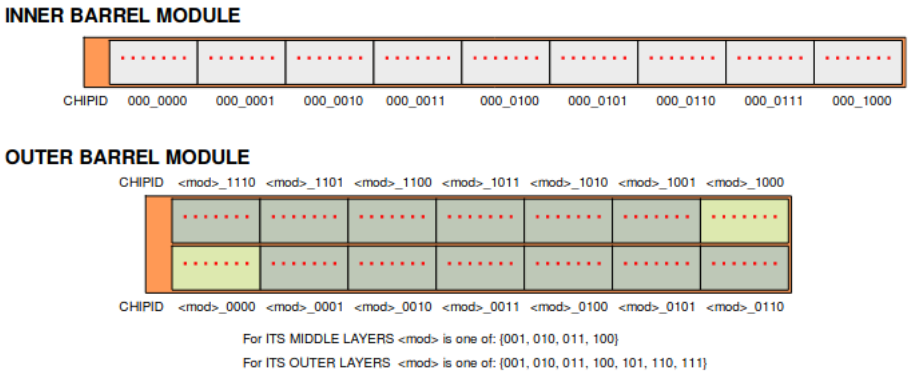


Figure 2.6: Layout of an Inner Barrel module and two Outer Barrel module [15].

For FoCal, different regions of the detector is expected to receive different amounts of events. Therefore, the detector will, as envisioned today, utilize all three operation modes. Section 3 discusses the details concerning FoCal.

2.3.2 Control Interface

The ALPIDE chip has two ports dedicated for slow control transactions, one differential signaling DCTRL port and one single-ended CTRL port. Which port is in use on each chip depends on the configuration of the operation mode on each chip. Figure 2.7 shows a topological view of the differences between IB and OB mode.

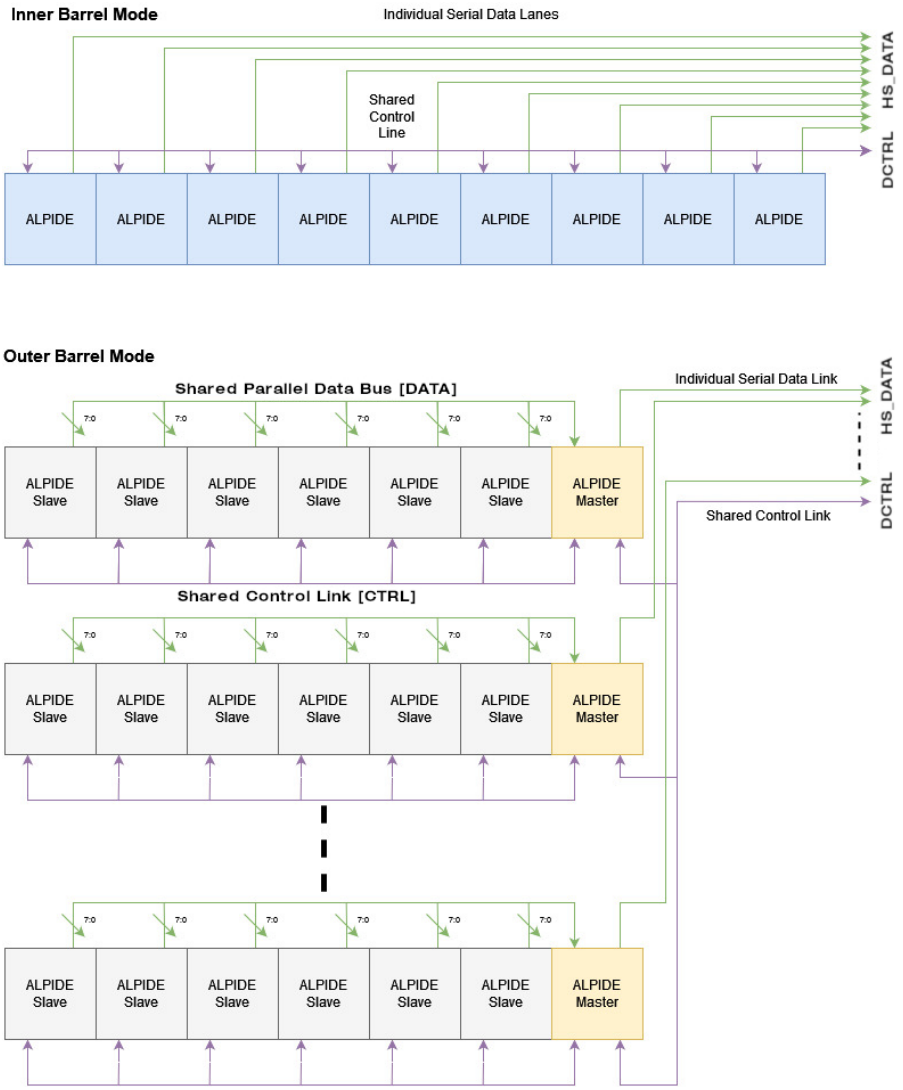


Figure 2.7: A topological view of data and control system for IB and OB mode.

For IB mode, all nine chips share the control line connected to the DCTRL port. A control bus based upon differential signaling is implemented with a multi-point topology. Therefore, the CHIPID has an important function for determining which chip is receiving a command, and possibly, is allowed to respond.

For OB mode chips, the control bus uses a hierarchical topology where each Master chip sharing a control line connected to the DCTRL with a multi-point topology. These Master chips then function as a slow control hub for all its subsequent Slave chips. The six Slaves beneath one Master share the single-ended multi-point line through the CTRL port. As viewed from off-detector hardware, the IB and OB modules appear equivalent and the communication is bi-directional and half-duplex.

The slow control system clock has a hierarchical structure and is synchronous with the LHC clock, running at nominal value of 40.08 MHz. All transactions are started from off-detector hardware. The chip continuously look for special OPCODE characters in the continuous data stream and will only respond when it has found one of the five available OPCODES. These OPCODES are pre-defined, and any two of them has a Hamming distance of 4. This prevents the chips from internally executing a transaction in the case of bit errors in the data stream. Figure 2.8 presents the format of each valid OPCODE.

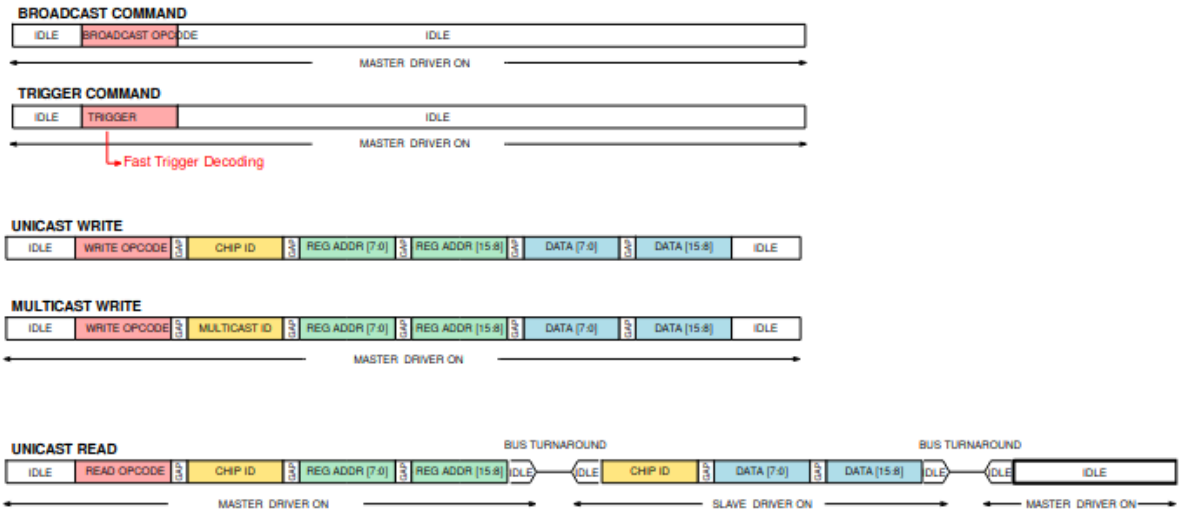


Figure 2.8: Format of each valid OPCODE [15].

Most of the OPCODES represent standard transactions. The BROADCAST COMMAND sends a single 10-bit character message to all chips, e.g. Global Reset (GRST) and UNICAST READ targets a specific chip and a specific address before waiting for a response from the chip. Then there is the TRIGGER COMMAND, which is not standard. This command is internally executed at the deserializing stage to reduce the trigger delay to a minimum. The chips then assert their STROBE signal, enabling them to write hits to their pixel memories. All chips receives the TRIGGER COMMAND simultaneously.

2.3.3 Data Interface

The ALPIDE chip has two sets of ports for data transmission. The first is a serial high-speed differential port, HSDATA_P and HSDATA_N, and the second is a parallel data port, DATA[7:0]. Both of these sets of ports use the same data formatting. The serial link is used by the IB mode chips and the OB Master chips for off-chip data transmissions. The parallel link is used by the OB Slave chips to transmit their data to their corresponding Master, where the Master then serializes the data and transmits it off-chip via the serial link. The data transmitted on the serial port is encoded by 8b/10b encoding, and K28.5 is used as a COMMA word when there is no data to transmit. The transmission of the COMMA word can be used for clock recovery and synchronization with the data stream. All data is transmitted in sets of bytes, and must be a valid data word. The valid data words are listed in Table 1.

Data Word	Length in Bits	Binary Value
IDLE	8	1111_1111
CHIP HEADER	16	1010<chip id[3:0]><BUNCH COUNTER FOR FRAME[10:3]>
CHIP TRAILER	8	1011<readout flags[3:0]>
CHIP EMPTY FRAME	16	1110<chip id[3:0]><BUNCH COUNTER FOR FRAME[10:3]>
REGION HEADER	8	110<region id[4:0]>
DATA SHORT	16	01<encoder id[3:0]><addr[9:0]>
DATA LONG	24	00<encoder id[3:0]><addr[9:0]>0<hit map[6:0]>
BUSY ON	8	1111_0001
BUSY OFF	8	1111_0000

Table 1: List of all valid data words [15].

A description of every data word can be found in the ALPIDE operations manual [15] in Section 3.4.1.

2.3.4 Front-End

As mentioned in Section 2.2.1, each ALPIDE chip has a pixel matrix with 512 x 1024 pixels. Each pixel has a width of 29.24 µm and a height of 26.80 µm. This area is split between a analog sensing circuit, capable of detecting ionizing radiation over a certain threshold, and a digital section which can store up to three different hits.

When the charge from the radiation is collected in the sensing node, a signal is sent through an amplifier. The amplifier shapes the signal into a more "slow" signal, which saves power [16]. Then a comparator compares the shaped signal to a configurable threshold level. Only when the signal is larger than the threshold will the comparator output a logical one. The hit can then be registered in the pixel memory if the STROBE signal is asserted a the same time. The pixel memory is referred to as a Multi-Event Buffer (MEB) and is able to store up to three hits. Depending on the readout configuration of the chip, a BUSY signal will be asserted when either two or three of the spots are filled up. Figure 2.9 shows a simplified front-end circuit and a timing diagram of the signal propagation.

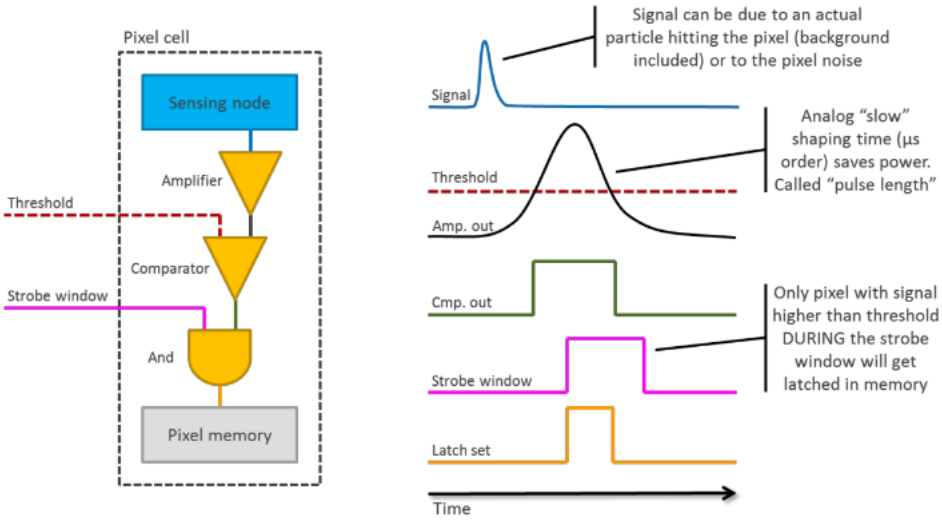


Figure 2.9: Diagram of signal shaping in the ALPIDE front-end [16].

It is important to note that noise in the substrate of the chip is also able to deliver enough charge to a node for the pixel to register it as a hit. Therefore, the length of the strobe window has to be adjusted to the mitigate as many fake-hits as possible. Each pixel has therefore the ability to be masked, meaning the hit information it stores will be ignored by the readout process of the chip. More details of the masking process will be discussed in Section 4.3.3.

Another note is that the threshold level given to the comparator is common for the entire chip. However, due to process variation, some pixels will register hits more easily than others.

2.3.5 Readout Structure

The pixel matrix of the ALPIDE chip is divided into 32 different regions, which each contains 16 double columns. Each double column is read out asynchronously by a priority encoder. This method creates a hit-driven readout scheme that is both fast and power efficient [8]. The readout speed for reading out any pixel is 50 ns, or two clock cycles. Figure 2.10 shows the layout of the regions and double columns.

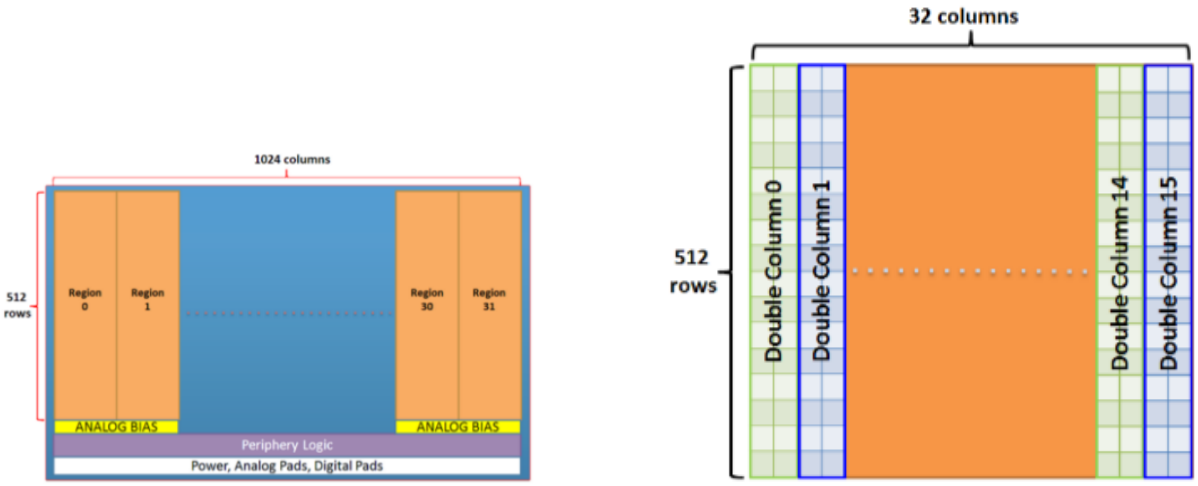


Figure 2.10: Diagram of regions and double column in the pixel matrix [15].

2.3.6 Triggering and Framing

The essential functionality of the ALPIDE chip is to take a snapshot or frame of the state of the front-end analogue pixel memory at a particular time. Whenever the chip receives a TRIGGER signal, a frame will be generated and transmitted upstream. As mentioned in Section 2.3.4, each pixel has a MEB capable of storing up to three complete frames before suffering any data loss. Data loss only happens if a complete readout of the pixel matrix is too slow, compared to the rate of which frames are generated. To prevent data loss, a special Framing and Management Unit (FROMU) is implemented into the chip.

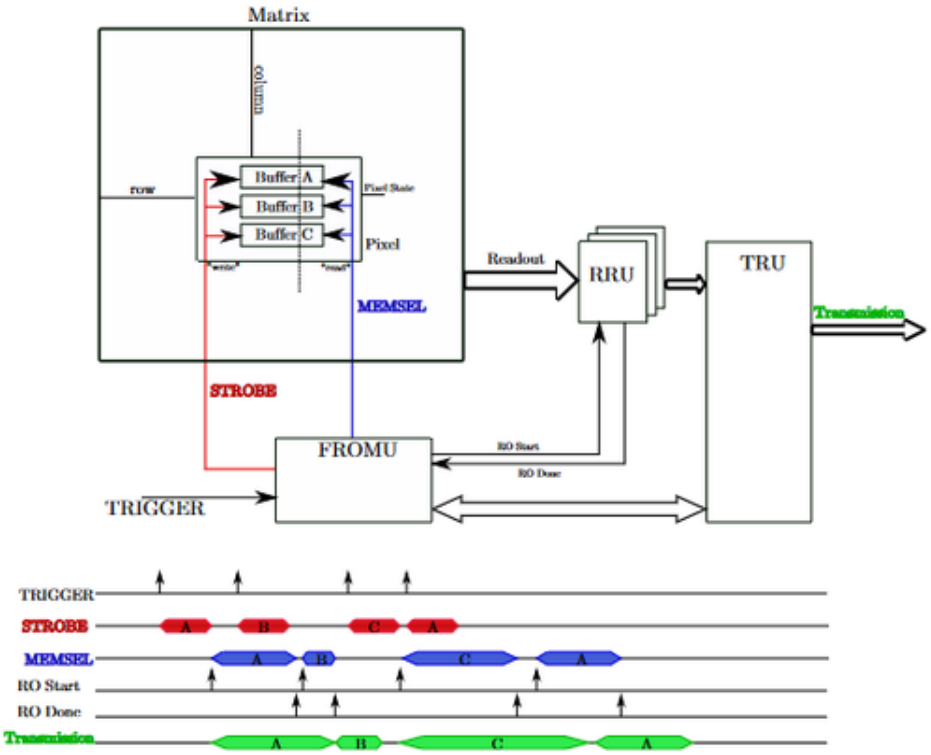


Figure 2.11: MEB management scheme of the chip MEB [15].

When the chip receives a TRIGGER signal, a chip-wide STROBE signal is asserted. The duration of which this strobe is asserted is referred to as the framing window. When the framing window is closed, the output of each pixel is latched into one of the three buffers in the pixel memory. The FROMU is responsible for only enabling one of the three latches to latch the output, and select from which memory buffer the readout process should read out from. Figure 2.11 shows a diagram of how the FROMU communicates with the different components. Each of the 32 readout regions has a Region Readout Unit (RRU) associated with it, and they all readout the pixel buffer concurrently. Each RRU then stores the data until the Top Readout Unit (TRU) fetches their data and transmit it off-chip.

If a chip receives a second TRIGGER signal while the STROBE from the previous TRIGGER is still asserted, it extends the framing window. When the windows is extended, it refreshes the duration of the STROBE. The length of the entire windows will therefore be whatever time between the two TRIGGERs plus the configured duration of a STROBE. If this event occurs, then the data packet will be marked with a STROBE EXTENDED trailer flag.

The ALPIDE has two ways of managing the MEB, which are called readout modes. First, the triggered mode is designed to sample the status of the pixel matrix over a relatively short interval. The duration of the strobe signal is expected to be of the order of a couple hundreds of nanoseconds. This mode is intended to start its framing window by receiving a trigger signal from an external triggering source. The readout scheme prioritizes the completion of reading out an old frame over new incoming triggers. When the FROMU asserts the STROBE to the last available MEB, a BUSY signal will also be asserted. If any new trigger signals is received while BUSY is active, the FROMU will then

refuse to generate a new framing window. The trigger signal will still be acknowledged in the data, by sending an empty packet with the data trailer flag indicating a BUSY VIOLATION. Section 2.3.8 expresses the implications of the BUSY VIOLATION flag.

The second readout mode is the continuous mode, where the sampling is intended to occur periodically with a gap between two framing windows as small as possible. The framing window will therefore be longer than for the triggered mode, on the order of a couple of microseconds. This mode will prioritize the arrival of new triggers over the data that is already stored in the pixel memory. To accomplish this, the chip will always make sure that the next memory buffer is available by deleting any hit information stored there. This can interrupt a potential readout process, but the data packet will be sent, containing all data up until the interruption and marked with a data trailer flag FLUSHED INCOMPLETE.

2.3.7 Internal Sequencer

The FROMU is equipped with the ability to generate triggers internally in the chip. This is enabled by configuring two registers in the FROMU which controls the strobe length and the period between two strobes. When using this functionality, the chip will assert the STROBE for the set amount, and then wait with re-asserting the STROBE for the set gap duration. The sequencer is initiated by setting an enable bit and then sending an external trigger to the chip. Any subsequent triggers will re-time the STROBE signal. The internal sequencer is terminated by resetting the enable bit.

2.3.8 Busy State

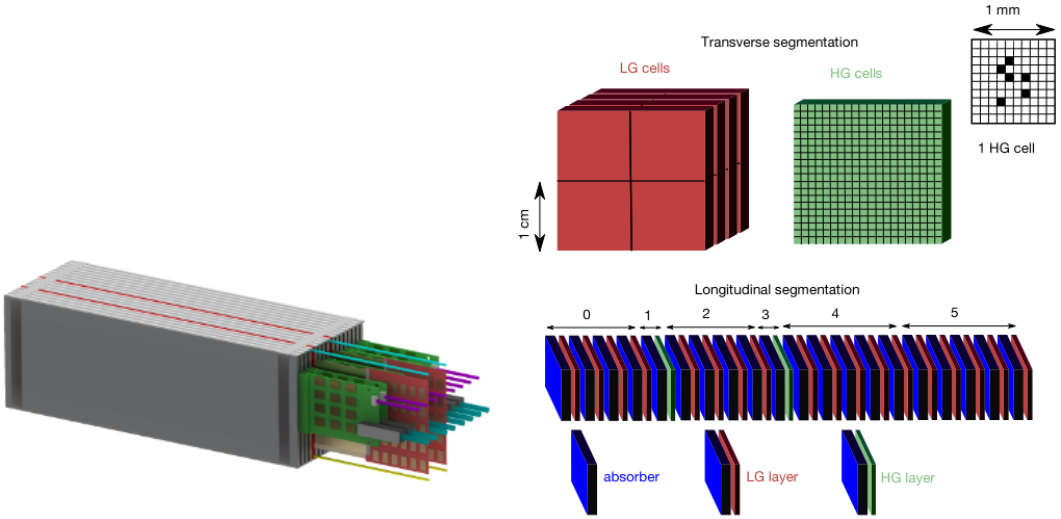
The ALPIDE is able to monitor its own internal circuitry. If the chip is ever close to saturating its own data processing capabilities, it will assert the BUSY signal. In IB mode, a BUSY word will be transmitted from each separate chip whenever they are in a BUSY state. In OB mode, if one of the slaves reach a BUSY state, it will transmit the BUSY word to the master. The master will then re-transmit the word on the serial link. The master and its slaves all share a connection on the BUSY pins, meaning that if one chip asserts the BUSY line, every chips BUSY will be interpreted as being busy.

3 Long Shutdown 3 Upgrades

The Long Shutdown 3 of LHC will, for the most part, revolve around the ITS3 upgrade, minor fixes, and tuning of the existing sub-detectors of ALICE. In addition to the introduction of a completely new sub-detector, FoCal. This chapter discusses several points of the FoCal design.

3.1 FoCal - Forward Calorimeter

FoCal is a sub-new detector planned for ALICE Run 4. This new sub-detector of ALICE will be installed during LHC LS3 and be ready for data-taking in Run 4, assuming the project is approved [17]. It will significantly enhance the scope of ALICE by covering pseudorapidities[4] of $3.4 < \eta < 5.8$. This forward direction allows for new physics to be detected, as currently, there are no detectors located in such high pseudorapidity. As of ALICE 2022, the only detectable collisions are when two particles with approximately the same energy collide. When the energy of two particles does not match, their parallel momentum, relative to the beam pipe, remains, and the collision is not detectable. The FoCal sub-detector can investigate these types of collisions.



(a) (b)

Figure 3.1: Mechanical (a) and conceptual (b) model of a full FoCal-E module [17].

Figure 3.1 shows how a whole module of FoCal is designed, with a view of how the different layers are distributed between the 20 total layers. Figure 3.2 shows a schematic view of the future detector location in the ALICE beam hall.

[4]Pseudorapidity refers to the angle of a particle relative to the beam pipe [18]. A line orthogonal to the beam pipe has a pseudorapidity value of 0, while a line parallel to the beam pipe has a pseudorapidity of infinite. An angle of 1° corresponds to a pseudorapidity of $\eta = 4.74$.

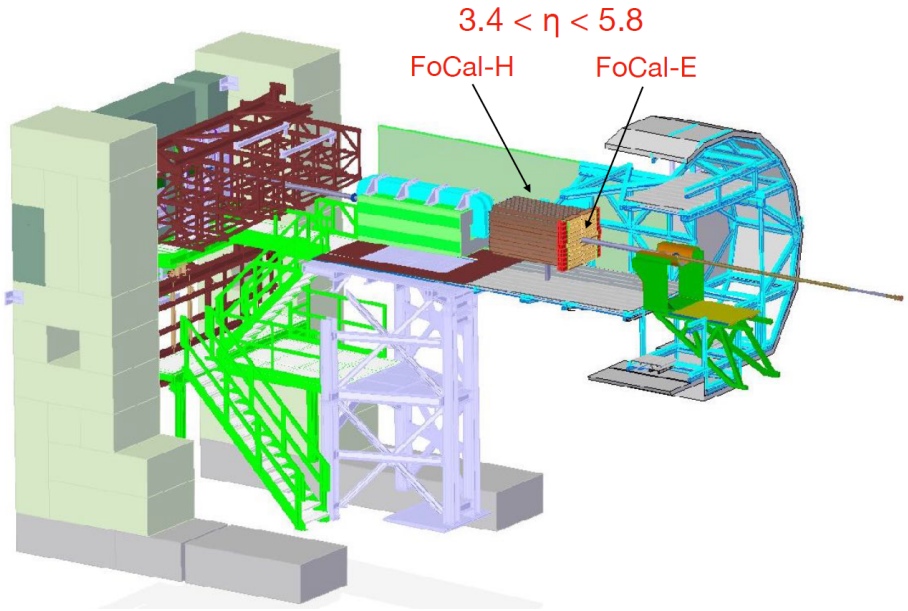


Figure 3.2: Schematic displaying the location and the relative size of FoCal in the ALICE beam hall [19].

In total, there are 11 modules on each side of the beam pipe, making up 22 modules for the entire sub-detector.

3.2 H-Cal - Hadronic Calorimeter

In particle physics, a calorimeter is a device used to measure the energy of an incoming particle [20]. The particle of interest starts a particle shower, which deposits all, or most, of its energy in the device. A hadronic calorimeter is a calorimeter specifically designed to allow incoming hadrons to start showering.

FoCal will have a hadronic calorimeter in complement to its electronic calorimeter [17]. This calorimeter helps the isolation of photons and the measurements of jets. FoCal-H will be located behind FoCal-E and cover the same pseudorapidities as FoCal-E. H-Cal will use copper tubes filled with scintillating optical fibers assembled into modules. Several of these modules will then make up the full sub-detector.

3.3 E-Cal - Electronic Calorimeter

The electromagnetic calorimeter part of FoCal will be built up of silicon + tungsten layers [17]. In total, there will be 20 layers of sensors with tungsten stacked between each layer. The fifth and tenth layers will use high-resolution sensors, and the remaining layers will use low-resolution sensors. The pixel layers will refer to the two layers with high-resolution sensors built up of ALPIDE chips. The pad layers will refer to the other layers using silicon pad sensors. Figure 3.1a shows a schematic of a full 20 layer module. The figure shows that readout, power supply, and cooling are placed on the same side of a module. This arrangement allows modules to be stacked next to and on top of each other, increasing the total sensitive area. This module's sensitive area is approximately 27 x 8

cm^2.

Tungsten was chosen as an absorber between each layer. Due to tungsten's small Molière radius[5] and radiation length of R_M = 9mm and X_0 = 3.5mm, respectively, the occupancy effects are minimized, and the separations of photon showers are optimized [17]. The Molière radius often dictates the cell sizes of the sensors, but simulations show that finer granularity is still helpful for π^0 identifications. Higher granularity also provides better resolution in multi-hit events, but this comes at the cost of handling vast amounts of data [17]. The compromise is, therefore, to have most of the layers use the pad sensor, with cell sizes of ∼1 cm^2 and two layers with a finer granularity of ∼30 μm^2.

3.3.1 Pad Layers

The pad sensors can measure the energy of the incoming particle by collecting charge in each of its cells. Therefore, a crucial feature is the dynamic range of the sensors, which determines how much or little charge the cell can collect. Ideally, the sensor is capable of detecting showers with energies of up to 2 TeV and is also able to detect Minimal Ionizing Particles (MIPs) for calibration [17].

The readout electronics for the pad layers has several requirements to fulfill. It needs an amplifier-shaper to allow for clean sampling of the signals from the cells, an ADC to convert the analog data to a digital format, and digital circuitry for transmission of the data. The HGCROC is a chip developed by CMS[6], which meets these requirements [17]. It has a dual-range ADC, allowing calibration and time-over-threshold measurements for up to 100 MIPs. It samples the signal with the LHC frequency of 40 MHz and sends out signals above a threshold. This frequency results in accurate time information from the pad layers on the order of 25 ns. Figure 3.3 shows two pictures of the pad sensors.

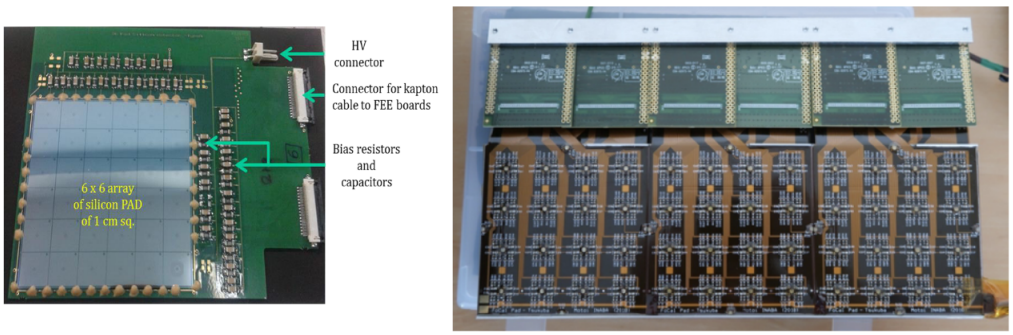


Figure 3.3: (Left) 6 x 6 array of silicon pad sensors. (Right) Three pad sensor modules stacked next to each other. [17]

3.3.2 Pixel Layers

The two pixel layers will use the ALPIDE chip, developed for the ITS2 upgrade. The chip is designed for a low occupancy tracking environment. However, beam test results

[5]The Molière radius is defined to be a transverse size, which can be thought of the transverse distance that a particle at the critical energy goes in traversing the last radiation length before it dies off [21].

[6]The Compact Muon Solenoid experiment, one of the other large experiments located at LHC at CERN.

and simulations show that the chips can handle a higher occupancy environment with a busy rate of below three percent [17]. The primary purpose of these layers is to track and separate showers. The positions of the layers are a compromise between catching a shower early, which makes it easier to separate two showers, and catching the shower late, which is better for energy resolution and efficiency [17]. The integration time of the ALPIDEs are around 5 µs with a peaking time of around 2 µs, which is slow enough in Pb-Pb collisions, but too slow for Pb-p or p-p collisions [22]. Therefore, some event pile-up will happen in the Pb-p and p-p of collisions.

Since the ALPIDE chip has two modes of operation, deciding which mode to use is essential. IB mode provides faster readout but uses more RUs, requires more cabling to the detector, and produces more data to store and transmit. On the other hand, OB mode may not read out data fast enough and generate busy signals.

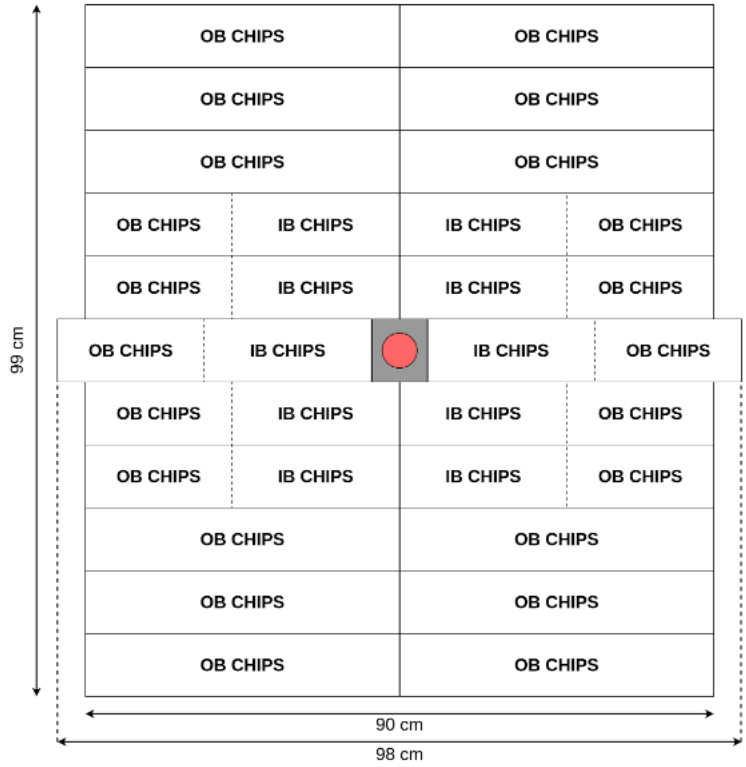


Figure 3.4: Proposed layout of the ALPIDE chip in the pixel layers [2]. The red circle in the center represents the beam pipe going through the plane (not to scale).

Figure 3.4 shows a proposed solution where the ten most central FoCal modules have a combination of both IB and OB mode chips. Each rectangle in the figure has 15x6 ALPIDE chips on it. This totals to 3960 ALPIDE chips distributed over the two pixel layers of FoCal. A decision for exactly how many IB mode chips there should be on these modules has not been made yet. As with most research projects, budgets are tight, and including too many IB chips are just a waste of resources. At the same time, data loss is never a good thing, so the decision is how much mitigating the risk of data loss is worth. More IB chips also require more infrastructure around the detector in terms of RUs, CRUs, FLPs, and more cables. All these things can be challenging to achieve, so the IB chips come with a high cost.

Because of the different topology between ITS and FoCal, it must be foreseen that the RU needs to support both IB and OB mode chips simultaneously. The current hardware solution of the ITS RUs can support this duality. Therefore, it is entirely dependent on the FPGA firmware and should be feasible to accomplish.

Simulations of the readout efficiency[7] for a layer with eight IB chips and seven OB chips in a central modules has been carried out. Figure 3.5 shows the results from these simulations.

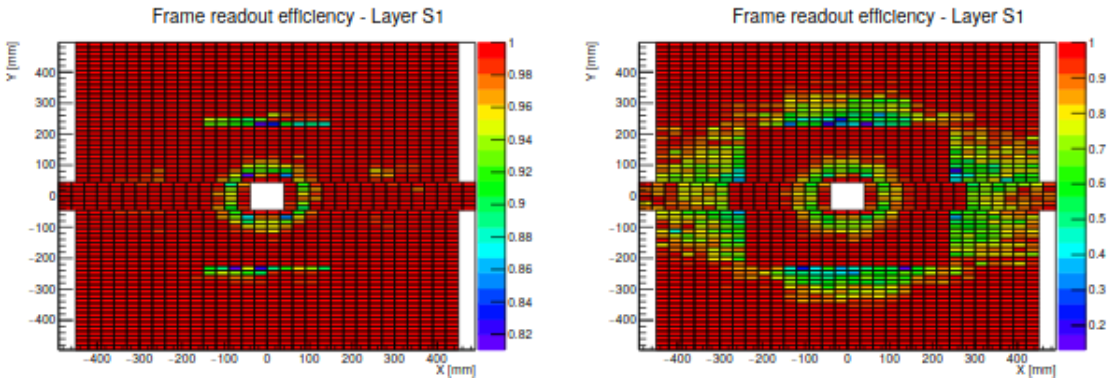


Figure 3.5: Map of frame readout efficiency for Pb-Pb simulations of FoCal [2]. The left plot shows the efficiency with an event rate of 50 kHz, and the right plot has an event rate of 100 kHz.

Figure 3.5 shows that the transition from IB to OB chips is crucial for readout efficiency. Most of the central OB chips cannot maintain high efficiency, and therefore, there is a discussion surrounding whether it is worth having more IB chips. Some of these OB chips are located on OB-only modules, which means they would have to be changed.

The amount of power dissipated by the chips makes it so that the modules will require active cooling [17]. For the complete FoCal, the ALPIDEs will be mounted directly on the tungsten, with aluminum covers. For the beam test the chips were mounted on aluminum plates. The chips were connected to the plate using aluminum-on-Kapton cables in parallel forming "strings". These strings stretch to the end of the plate. There they are connected to a transition card, see Section 4.2.3, via ZIF-connectors. Two of these plates were mounted together in a face-to-face fashion so that the chips cover the area of one layer/plate. Figure 3.6 and figure 3.7 illustrates the mounting scheme used in the SPS beam test.

[7]Readout efficiency is a term reflecting what fraction of frames generated got successfully read out[2]. This fraction is then the number of frames fully read out divided by the number of frames generated, including those lost to busy violations or those who were flushed.

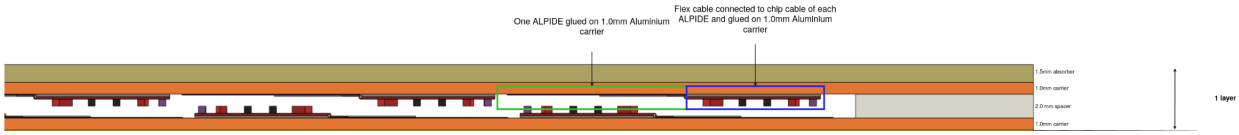


Figure 3.6: Side view of two plates with ALPIDEs mounted on top each other face-to-face [23].

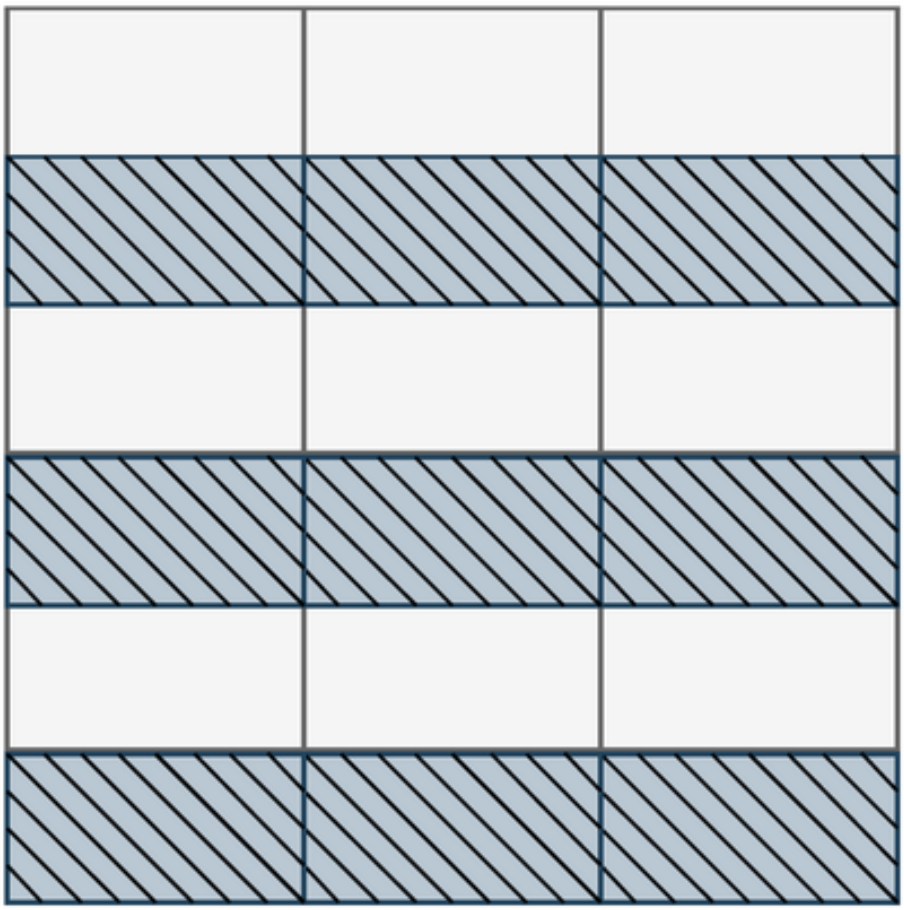


Figure 3.7: An illustration of how the ALPIDE chips are distributed on two layers to give maximum sensor area. The light areas represents ALPIDEs facing up, while the shaded areas represents ALPIDEs facing down.

3.3.3 Triggering and Readout

ITS plans on using continuous triggering with strobe duration almost as long as the interval between two triggers. For FoCal, the ALPIDE chips exist in a showering digital calorimeter, which means a lot more pixels are hit simultaneously for a given chip in each event. Therefore, keeping the same triggering scheme as ITS may be troubling because more data needs to be read out between the triggers. Each time the ALPIDE receives a trigger, the pointer in the MEBs moves one spot, and a value of one or zero is stored. A chip with zero hits still produces a data packet that needs to be read out. These seemingly empty packets are not a problem. However, the ALPIDE chips sends either DATA LONG or DATA SHORT data word when transmitting pixel hits, see Section 2.3.3. Whether any particles generate signals in the pixel matrix or not, a chip can register noise in the

substrate when triggered. These fake hits produce a lot of single-pixel hits instead of clusters. The single-pixel hit information is transmitted in DATA SHORT words, which means that if a chip experiences a lot of these hits, it can generate a lot of DATA SHORT words. Clusters are sent in DATA LONG packets, which includes several hits in the one, slightly larger, packet. Therefore, the total data amount can surpass the data amount of chips with real hits. Every ALPIDE chip receiving a trigger generates a strobe and stores any signal in the pixel matrix. Masking the noisiest pixels can reduce the number of packets with fake hits in the data stream. Section 4.3.3 presents more details on noise masking. Another workaround, using the fast hit information from the pad sensors, may help alleviate this problem.

The pad sensors provide a signal from its front-end electronics every BC, thanks to its fast shaper with a peak time of around 20 ns [17]. Compared to the shaping time of the ALPIDE of around 5 µs, the information from the pads can be used to produce a trigger signal that only triggers the ALPIDEs that actually are in the shower region. In practice, this would mean that when a particle starts a shower on the top right side of the detector, the chips on the opposite side will not receive a trigger. Therefore, the left side chips will not transmit any data and will be standing by for a trigger for their side. This method will reduce the event pile-up risk as the MEB pointer of the pixel matrix only moves if a shower hits the chips. Figure 3.8 illustrates how a shower may occur on only one side of the detector.

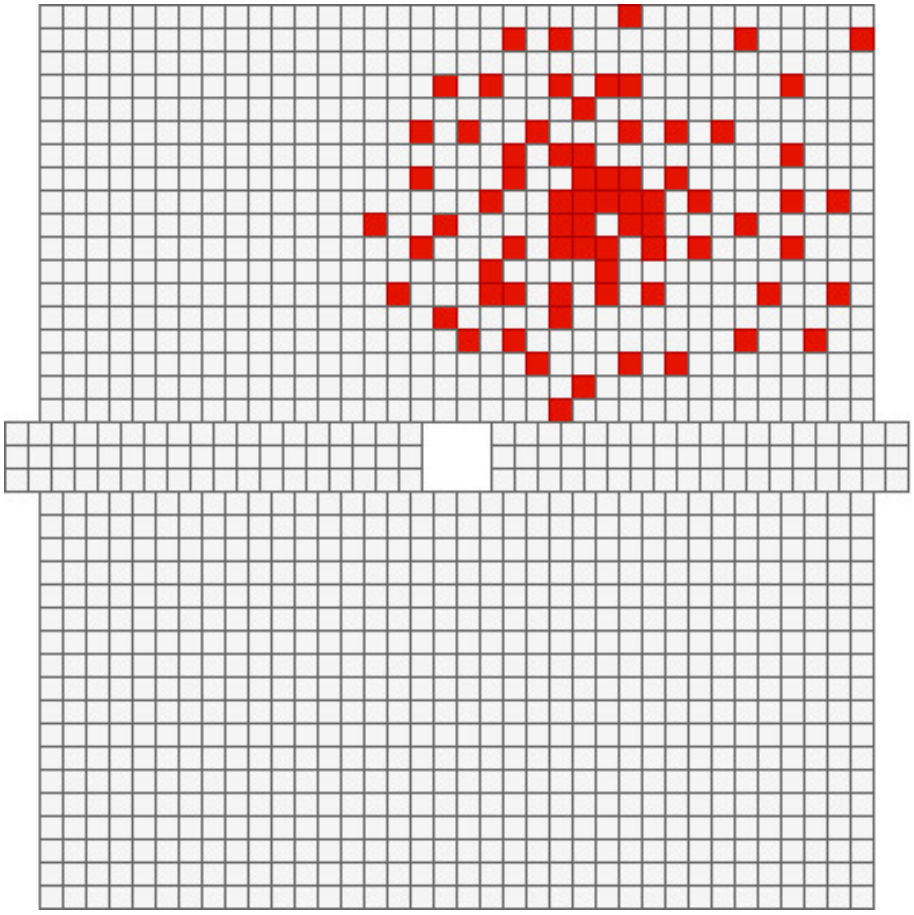


Figure 3.8: An artistic figure to illustrate that only some regions are hit (not to scale).

This solution requires a new concept called Trigger Sum. The Trigger Sum needs to be incorporated into the triggering system so that only relevant RUs generate a trigger signal or even only certain ALPIDEs on an RU. This new concept will require developing a new card that calculates which regions are of interest for each event. It also needs to fit into the detector architecture. The card would use the hit information from pad layers to calculate which regions are of interest. Using several pad layers may result in better decisions.

A decision on how to implement this concept in practice has not been made as of this date. One solution is to send the TS information to the CTP, including it into the HBs. This solution is the cleanest, as the triggering and readout scheme stays similar to the entire ALICE. However, the card needs to sample information from the pads, calculate which regions to trigger, and send this packet to the CTP. The information then has to flow down to the RUs, triggering the ALPIDEs. The time limit is the time interval from when the pads generate their signal to the ALPIDEs signal shaper outputs a signal above its threshold. This tight timing requirement needs to be consistent but may be challenging to achieve.

Alternatively, the Trigger Sum information can go directly to the RU, generating a trigger without the CTP's or LTU's involvement. This solution provides a faster response time but has drawbacks of its own. By using this method, the ALPIDEs will produce data packets out of sync with the CTP and the rest of ALICE. The RU would then have to store this information on board and wait for the appropriate time before sending it in the CRU packets. Finding space enough to potentially store all this information on the FPGA of the RU may be a challenge. In addition, storing bit information like this in a radiation environment risks corrupting the data due to Single Event Upsets [24]. Figure 3.9 shows a schematic including both alternatives.

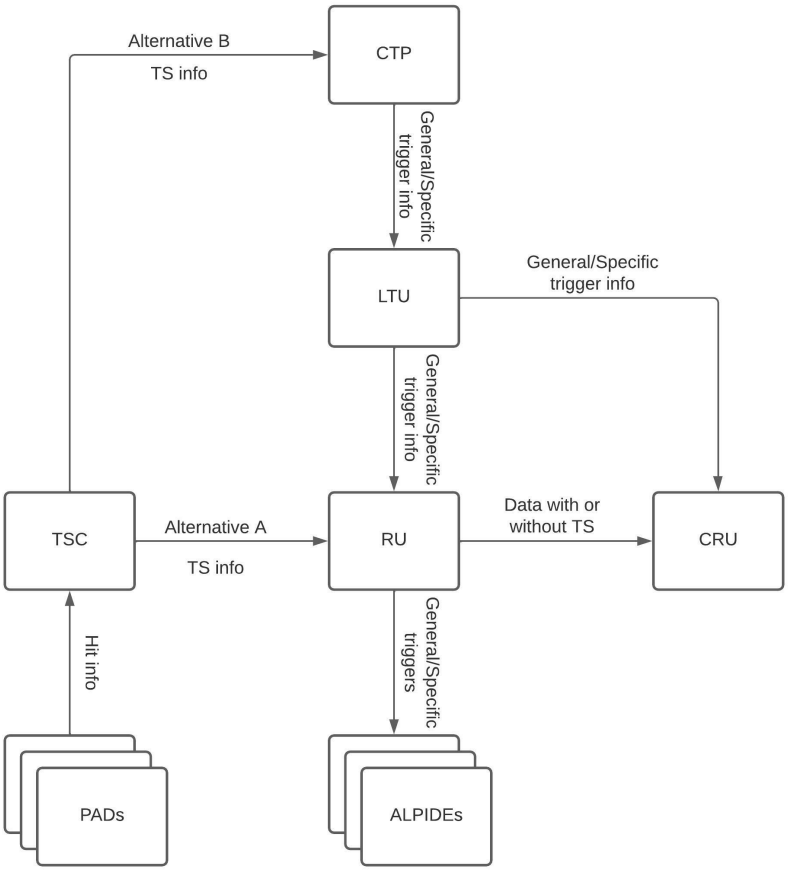


Figure 3.9: Schematic of a proposal of how a Trigger Sum Card (TSC) can fit into the FoCal readout system.

If the option of storing the ALPIDE data on the RUs is not feasible, then the data would have to be sent from the RU upon receiving it. This solution would result in FoCal triggering itself and generating data out of sync with the rest of ALICE. Matching events from all the different sub-detectors may then be problematic and consume unnecessary resources.

4 SPS Beam Test

This chapter discusses the setup for the 2021 beam test at SPS at CERN for FoCal. The focus is on the pixel layers, and the preparation steps completed in regards to getting the setup up and running for the beam test.

The Super Proton Synchrotron (SPS) is the second-largest accelerator located at CERN [25]. It has a circumference of almost seven kilometers. Its current job is primarily to receive particles from the Proton Synchrotron and accelerate them further before providing them to the LHC. The SPS was CERN's largest accelerator when it first turned on in 1976. Some of its achievements are probing the inner structure of protons, investigating nature's preference for matter over antimatter, searching for exotic forms of matter, and looking if matter was the first instance of the early universe.

4.1 Objective of the Irradiation Test

When conducting a beam test on a prototype, wherever it is in the process, the goal is to measure its performance in ionizing radiation. It is essential to ensure that the detector behaves as intended at every step during development. The best way to do that is by performing functional tests for every iteration made. The alternative is to develop the whole thing and then start testing. If something does not work, it will be near impossible to pinpoint where the error occurs and correct it, especially if there are multiple problems. Testing with regular intervals allows for testing new functionalities one by one as they get implemented into the design.

For the irradiation test performed in September - October 2021 for FoCal, the goal was to put all three of FoCal's parts together for the first time. Each part had its way of taking data and controlling its setup. Future beam tests include developing a system where the same interface controls all three parts.

4.2 Setup for September 2021 Beam Test

Figure 4.1 shows a photo taken of the beam test setup mount on a DESY table in the beam hall, while Figure 4.2 shows a schematic view of the same setup. There are two scintillators in the front capable of generating an electrical signal when a particle flies through them. The signal generated triggers both the pixel and pad layers, enabling them to collect data from the incoming particles. As the beam is shooting particles in a straight line, hitting the yellow squares in the image, the use of two scintillators allows the setup to filter out particles hitting the scintillators with an angle. If an incoming particle hits one of the scintillators but not the other, it will not hit the sensors either, and therefore they should not be triggered. This setup helps the setup trigger only when there is actual data to collect.

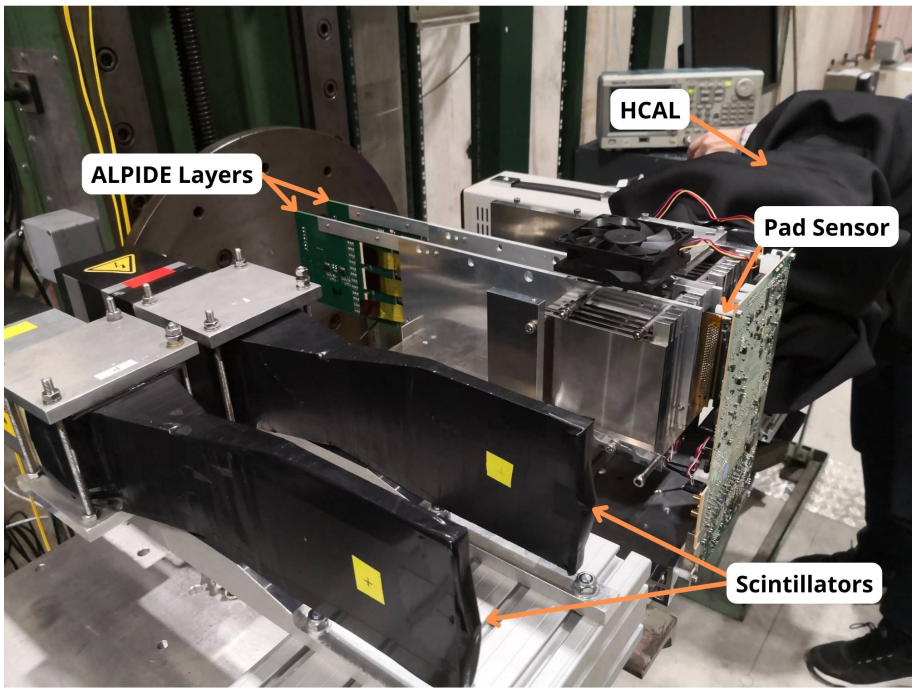


Figure 4.1: FoCal test setup for the SPS beam test.

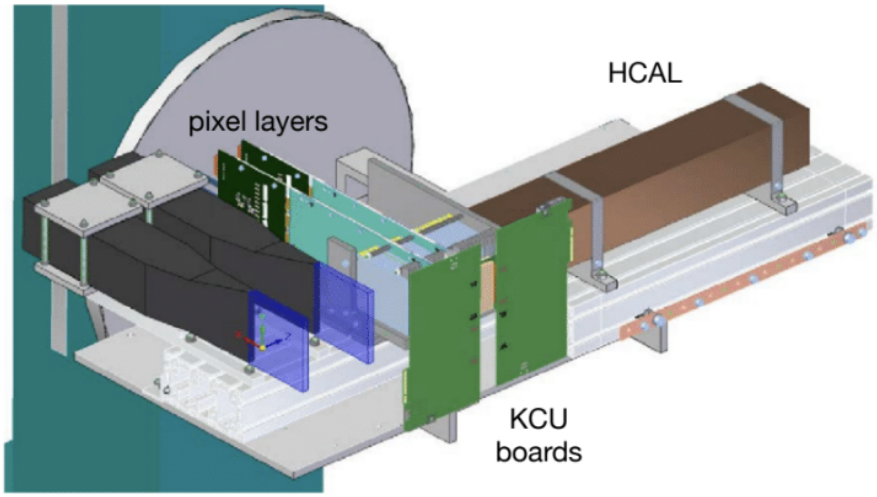


Figure 4.2: Schematic view of the beam test setup [19].

Behind the two scintillators is FoCal-E. The first five layers consist only of tungsten. As mentioned earlier, this helps create electromagnetic showers, which the pixel and pad sensors can detect. Layer five and layer ten are the pixel layers with a single pad layer placed in between the two pixel layers. The tungsten layers are between each sensor layer, and because the pads only have one of their eighteen layers, special spacers ensure the tungsten stays at their correct spots regardless of the missing pad layers. FoCal-H is located at the end, covered by a blanket made of opaque material. This blanket helps with reducing noise, as the detector is very sensitive to light. Figure 4.3 shows a schematic of the pixel layers of the test setup.

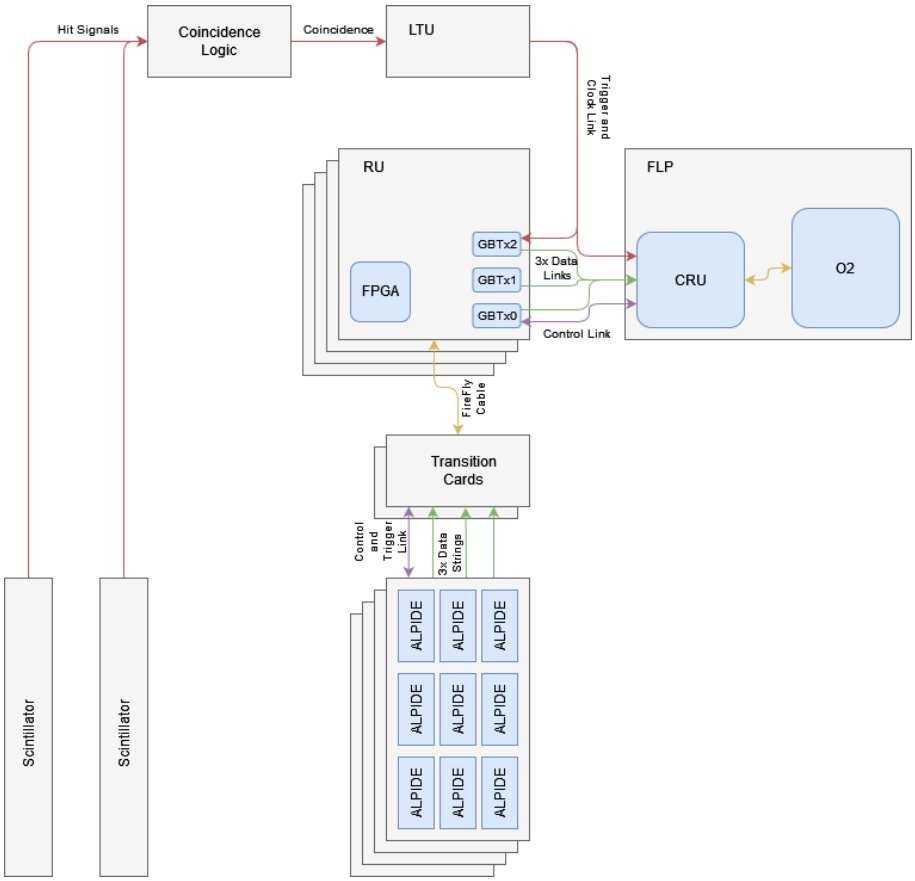
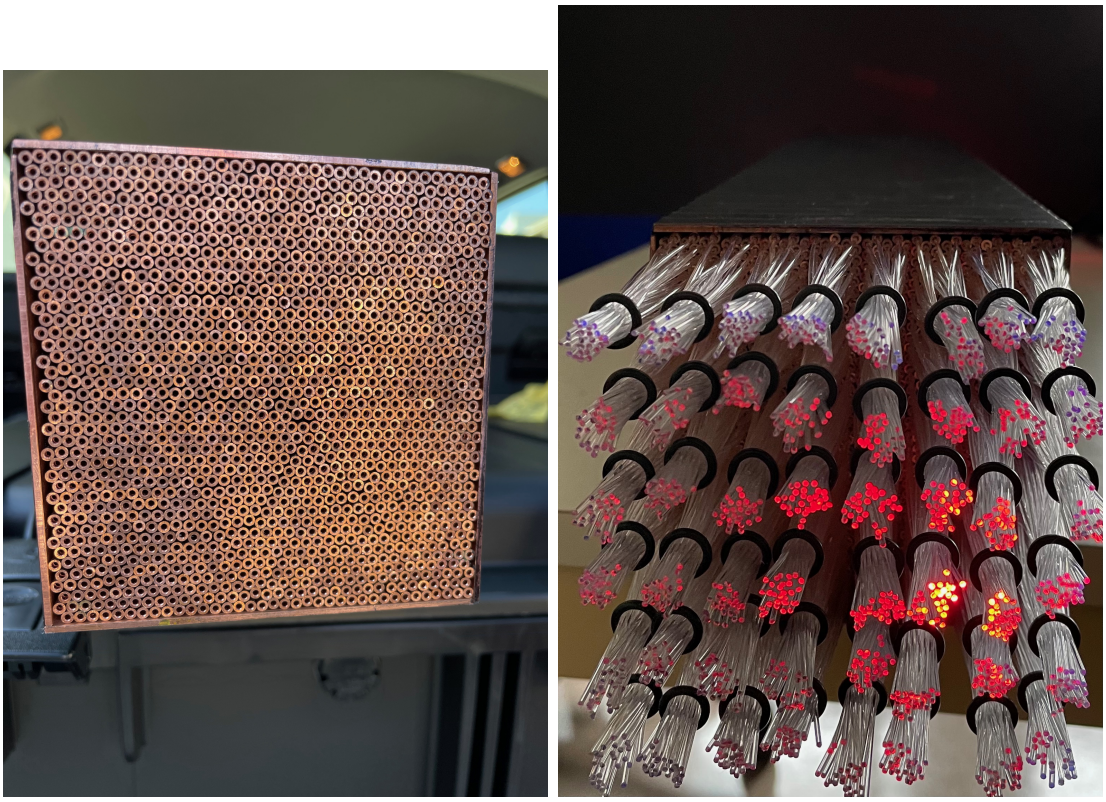


Figure 4.3: Schematic of the test setup for the pixel layers.

4.2.1 H-Cal

Figure 4.4 shows the FoCal-H module. When hadrons collide with the copper material of the tubes, they radiate light. The scintillating fiber captures this light and sends it to the end of the fiber. Sensors at the end detect the incoming signal and register it as data.



(a) (b)

Figure 4.4: Left (a) FoCal-H with all copper tubes without the scintillating fiber. Right (b) FoCal-H with the scintillating fiber threaded and grouped in sets of 30 fibers.

4.2.2 Pad Layers

The setup would initially have all 18 pad layers included in this test. Due to different reasons, the pad section only included one of these eighteen layers. Still, one layer is better than zero, and testing the readout system surrounding that one layer provides valuable information for future testing.

4.2.3 Pixel Layers

This beam test did not use the standard ITS layout of nine ALPIDE chips in a row on a single string. Instead, the chips were distributed into a three-by-three matrix, see figure 4.5. The figure displayed two of the four half-layers used in the beam test, one top layer, and one bottom layer. Two and two of these half-layers were mounted on top of each other, as displayed in figure 3.6. In total, the setup had 36 IB mode chips, which then required four RUs to handle all the data and control signals.

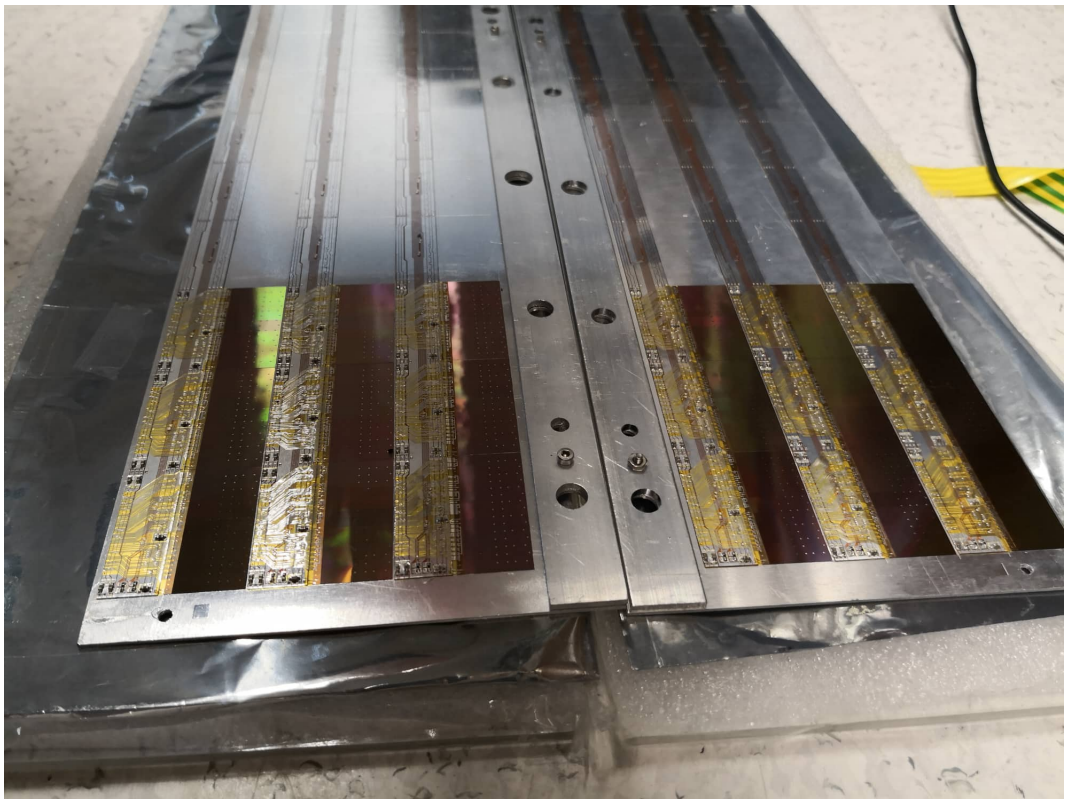


Figure 4.5: Image of two half-layers with nine ALPIDE chips each.

The chips are connected to a transition card via ZIF connectors at the end. Figure 4.6 shows three flex strings connected to the three ZIF connectors on one side of transition card. The transition card serves two purposes. First, it provides the necessary power and voltage levels to the chips on the string. Second, it reroutes the split nine chip string into one FireFly cable that connects to the RUs.

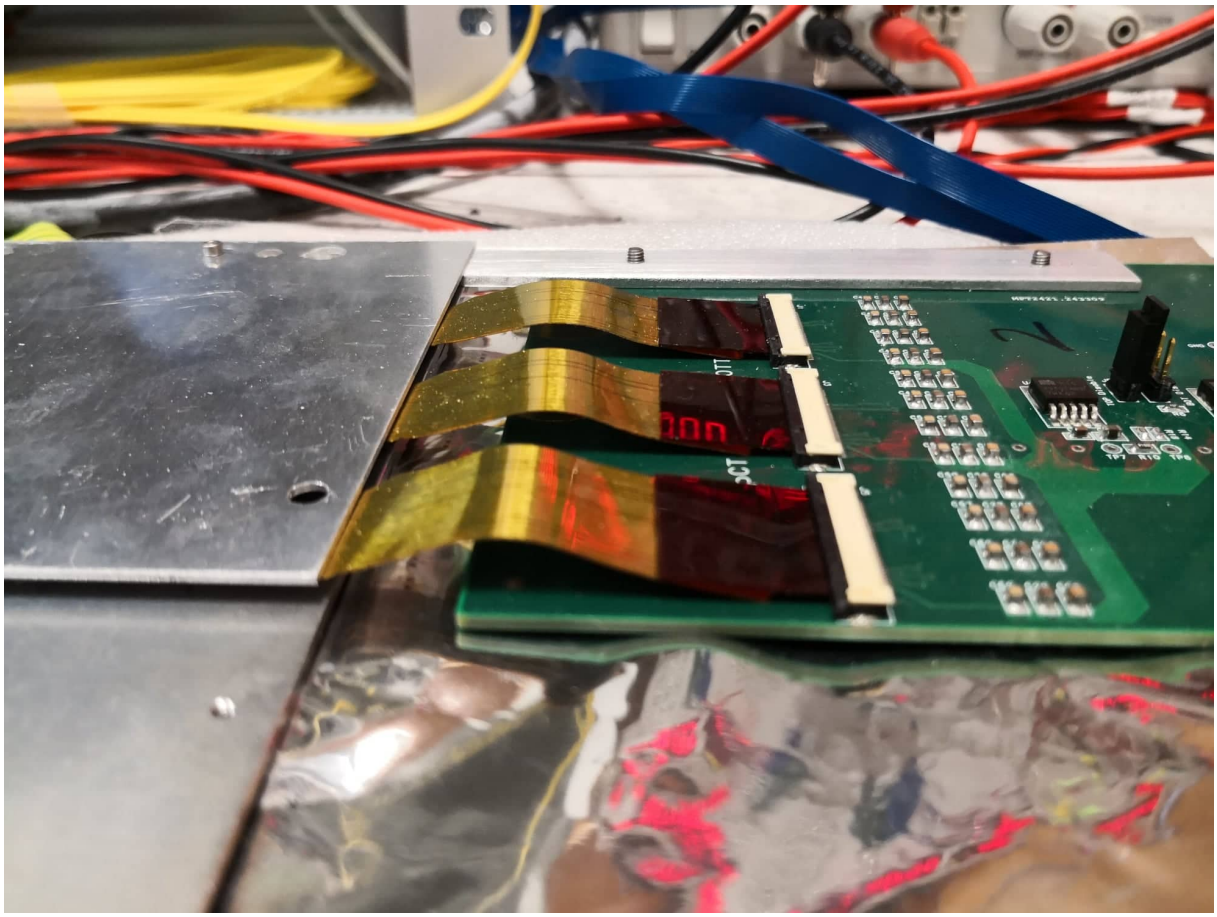


Figure 4.6: Three flex strings connected to three ZIF connectors.

The transition card connects to one top and one bottom half-layer and provides 1.9V to both the DVDD and the AVDD power supplies. It uses four regulators, one for DVDD and one for AVDD, for each layer to regulate the voltage down from 3 V. It can also apply a back-bias voltage to the layer. Figure 4.7 show an image of a transition card used in the beam test. These transition cards were designed and made specifically for this beam test[8].

[8]These transition cards were made and designed by Shiming Yang, based upon a similar transition card made for the Proton CT project by Tea Bodova

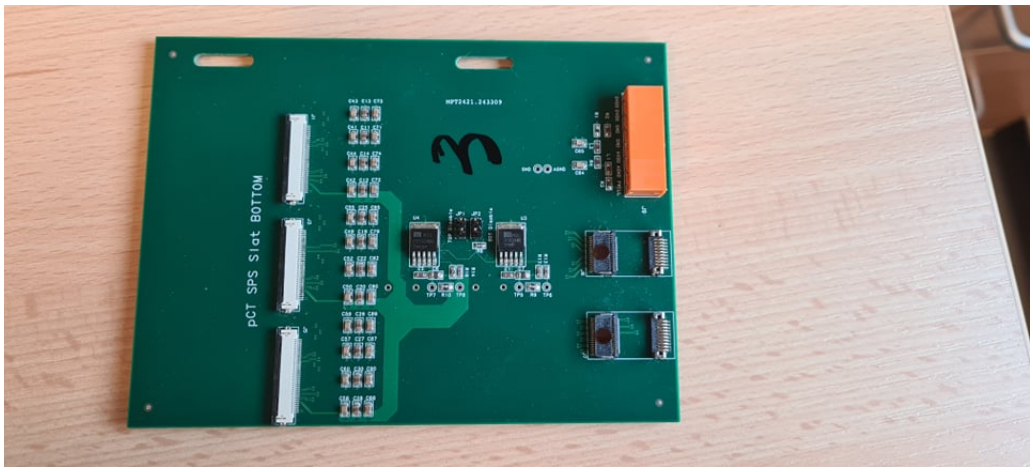


Figure 4.7: Transition card used for the SPS beam test.

4.2.4 Triggering

The LTU was used to generate trigger signals to the pixel layers for this beam test. The particle hit rate at the SPS is significantly lower than at the LHC. Even though the LTU design is for the LHC, it can also send triggers based on an external source. The LTU uses two different ports to generate triggers based upon incoming Low-Voltage Differential Signal (LVDS) or Emitter-Coupled Logic signals. The signals from the scintillators generated a Transistor-Transistor Logic (TTL) signal via a signal generator, which then was converted to LVDS using an LVDS-TTL converter module. The used LTU configuration produces trigger signals whenever it receives a pulse edge on the LVDS input.

This triggering method utilizes the triggered mode of the ITS readout system instead of the continuous mode. The main reason for using triggered in this beam test is the event rate expected at SPS. The beam at SPS follows a procedure of first loading the accelerator with particles and accelerating them. Then the particles are released as a beam to hit detectors before the accelerator loads up again with new particles. Each release is called a "spill", and the interval between each spill is approximately 20-30 seconds. By running the setup in continuous mode, any slightly noisy pixel would generate abundant data between these spills.

4.2.5 Readout

The setup used four RUs to read out data from the ALPIDE chips. Each RU connects to nine chips, and all four RUs connect to the same CRU and LTU. The lab setup in Bergen only had one RU prior to the beam test. The ITS team lent two RUs, and the University of Utrecht lent the last needed for the setup. All four RUs were updated to run with the same version of the FPGA firmware, and the CRU was set up to enable the data and control links for all four RUs.

4.2.6 CRU_ITS and DAQ_TEST

The CRU_ITS git lab repository was used as a user interface for the setup. Inside this repository is a script called `daq_test.py`. This script runs through a procedure of resetting, configuring, and starting the data-taking processes on the FLP, CRU, RU, and ALPIDE chips. A configuration file dictates the correct settings for a data-taking run. The script starts the data-taking process and stores the data received from the chips. It prints out the number of triggers received, packets created, and any errors in regular intervals. The script can be run at a set time or indefinitely. See Appendix C for further details.

4.3 Preparation for the Beam Test

In preparation for the beam test at SPS, several items needed to be completed beforehand:

- Verify readout system with confirmed working ITS stave.
- Four half-layers of nine ALPIDE chips must be tested upon arrival.
- Create a bitmap of the noisiest pixels for masking.
- Take cosmics data.
- Testing of Back-Bias.
- DAC test and Eye Scan.

4.3.1 Verify Readout System with Confirmed Working Stave

In Bergen, the lab setup had one ITS IB stave at disposition. This stave provided a reference to configure and verify that all the different parts of the readout system were working. These parts included the FLP, the CRU, an RU, and the LTU. The system was data taking random noise data successfully with the ITS chips. By doing this, the new FoCal staves can be isolated in testing to make sure they work.

4.3.2 Half-Layers with ALPIDEs Need to be Tested Upon Arrival

The chip layers got mounted and assembled in Ukraine before they got shipped to Bergen. They arrived at Bergen two days before the whole setup moved to CERN for the beam test. This late arrival meant that the chips could not be thoroughly tested. The only test conducted was a simple power-on test and attempting to read from some of the registers on the chips.

Before being shipped, each chip underwent testing in Ukraine and got a classification based on how much current it drew. There are four classifications a chip can have. These are listed in Table 2 together which each classification criteria. Appendix B lists the results and classification of each chip used for this beam test.

	Gold	Silver	Bronze	NOK
I_A[mA]	10.42 - 15.54	10.42 - 15.54	10.42 - 15.54	Otherwise
I_D[mA]	40.00 - 50.14	45.01 - 49.57	35.00 - 70.00	Otherwise

Table 2: Classification criteria for power test of the ALPIDE chip[26].

Some chips were determined to be NOK due to drawing slightly more current than is acceptable. However, it is the ITS upgrade project that sets these requirements, which means they could still be functional for this beam test. The worst set of three chips sits on WT2, with CHIPIDs 0-2. In total, these three chips should have a collective current consumption of around 250 mA on the digital circuit before applying a clock. When this set was powered on, it immediately hit the current limit of the power supply, forcing a voltage drop, and was powered off again quickly to avoid any permanent damage to the circuits. The power supply supplied 3 V to the analog and digital circuits and the current limiter was set to 1.5 A for the digital supply and 500 mA for the analog supply.

Unfortunately, several sets of three-chip strings hit the current limit and forced the power supply to drop the voltage. Due to the pressing time constraint, investigating what might cause this behavior could not be conducted before the beam test. Therefore, in fear of damaging the working chips, the chips with this voltage drop behavior were entirely excluded from the beam test. Since the transition cards deliver power to three chips per string, the whole string got excluded if just one of the three chips drew too much power. In total, four three-chip strings drew too much current, and these 12 chips got excluded. The remaining 24 chips showed relatively regular current consumption and got included in the beam test. The specific chips included and excluded are listed in Table 3. WT1 and WT2 refers to the two Working Top half-layers, and similarly, WB1 and WB2 refers to the two Working Bottom half-layers.

Half-Layer	Included	Excluded
WT1	0-5	6-8
WB1	3-8	0-2
WT2	3-5	0-2, 6-8
WB2	0-8	None

Table 3: List of CHIPIDs included and excluded in the beam test.

With the assembling of the half-layers, the digital current limit was increased to 2 A to account for more chips. The analog current limit stayed at 500 mA. Both limits stayed at those values for the entire beam test.

4.3.3 Create a Bitmap of the Noisiest Pixels for Masking

Each ALPIDE chip contains about 520 thousand pixels, each of them capable of registering a hit with sufficient charge in the collecting diode. The collected charge may come from an incoming particle, but it may also come from noise. Therefore, setting the pixel

threshold is a trade-off between detection efficiency and fake-hit rate.

Fake-hit rate is when pixels fire without any form of ionizing radiation. To test the fake-hit rate of a chip, N number of triggers are issued to the chip. Mask out the ten most fired pixels and Repeat this process one more time. The max fake-hit rate accepted by the specifications of ITS is 10^{-5} fake hits per event per pixel[27] (Table 1.5).

The setup for the SPS beam test was not able to use the masking method described above. The CRU_ITS software package does not support any functionality for masking individual chips. The masking procedure broadcasts to all chips on an RU, and the software does not allow for different masking patterns on different RUs. Ideally, the optimal masking solution uses one distinct pattern for each chip in the setup. Due to the convoluted CRU_ITS software, modifications to allow individual masking patterns are complicated to achieve. In addition, the lack of time meant that the development of an individual masking function had to be delayed until after the beam test. There is now a working individual chip masking function in the UiB_FoCal branch of the CRU_ITS repository.

Because of the lack of an individual masking function, a different method for masking was used. The method used issued 100k triggers to the chips, without exposure to ionizing radiation. The resulting hit data has to be from noisy pixels, and can then be used to create a masking pattern. All chips used the same masking pattern and Figure 4.8 displays the pattern used. The pattern masked about 4,500 pixels, amounting to less than 0.9% of all pixels per chip.

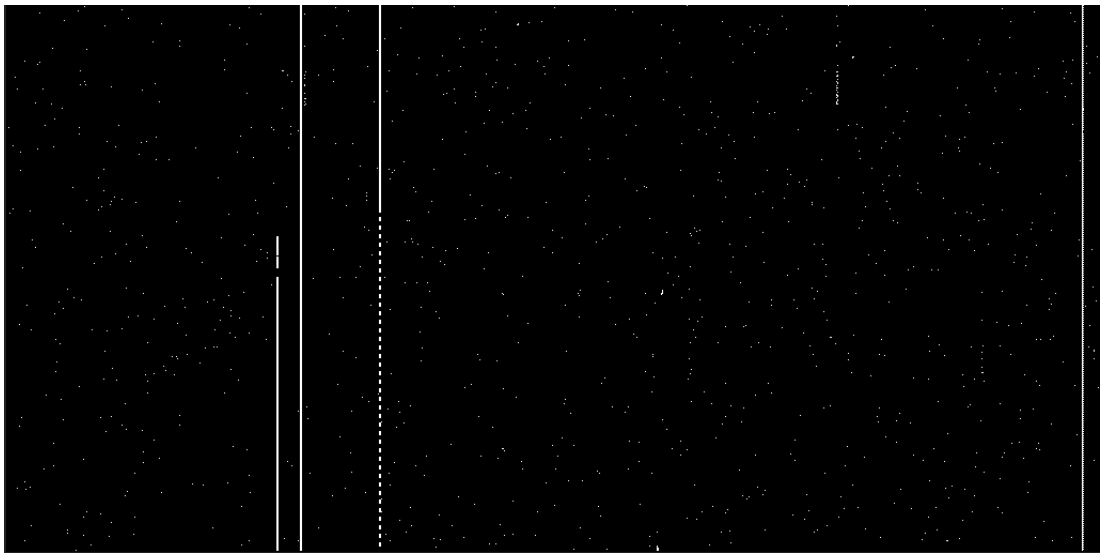
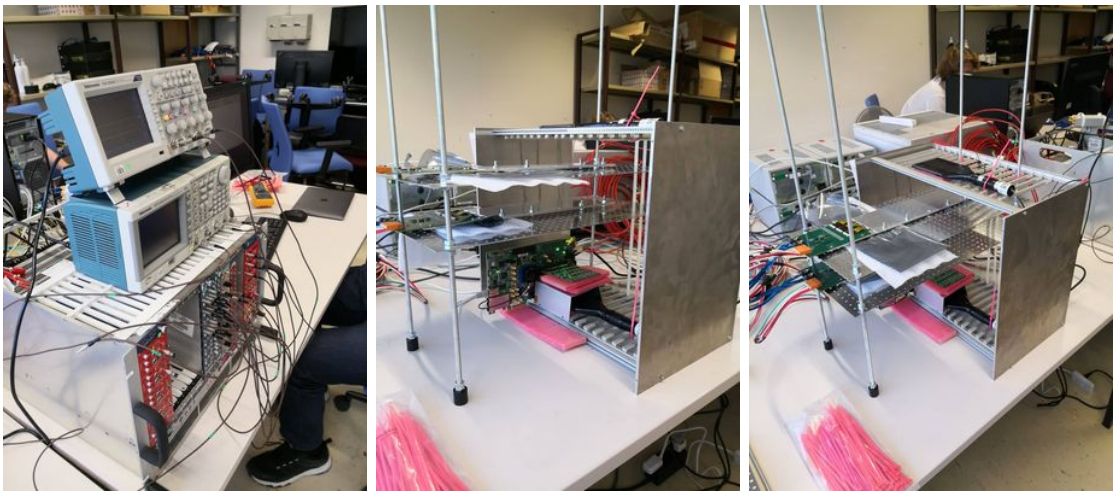


Figure 4.8: Image of masked pixel on all chips.

The figure shows that most of the masked pixels are randomly distributed all over the matrix. In addition, there are unfortunately some double columns that are broken, making all pixels in that column register hits regardless of the situation.

4.3.4 Cosmics Data

The pad and pixel sensors used the scintillators to trigger during the beam test. In the few days before moving the setups to the beam hall, the two setups took cosmics data together. Using two scintillators, multiple different modules to filter the signal, and a signal generator to produce a TTL signal triggered both setups by incoming cosmic MIPs. Figure 4.9 shows the arrangement of this setup.



(a) (b) (c)

Figure 4.9: Image of the setup used for collecting cosmics as a preliminary test of FoCal-E before putting the setup in the beam hall.

This setup allows for triggering based on incoming relativistic muons. Cosmic rays hitting particles in the atmosphere create secondary muons with relativistic speed. Due to special relativity, these muons can travel all the way to ground level and induce charge in the sensors. This setup then tests whether the pixel and the pad sensors receive the same trigger signals. This test ensures that the triggering system works for both modules.

4.3.5 Testing Back-Biasing

With the pixel layers arriving late in Bergen, severe time constraints got placed on the testing. Therefore, the back-bias tests got delayed until after returning to Bergen. Still, the back-biasing was attempted in the beam hall, but due to user error in a stressful environment, it had to be forfeited, see section 5.1.

The ALPIDE chips can apply a negative voltage to the PWELL, which internally connects to the substrate, creating a larger depletion region around the charge collecting diodes [15]. When applying the maximum voltage of 0 V, both the PWELL and substrate are connected to ground. The minimum voltage recommended is -6V. The primary purpose of applying a back-bias to the chips is to reduce the cluster size created by the incoming particle. The reduction in cluster sizes automatically translates to less data output, as fewer pixels register any hits.

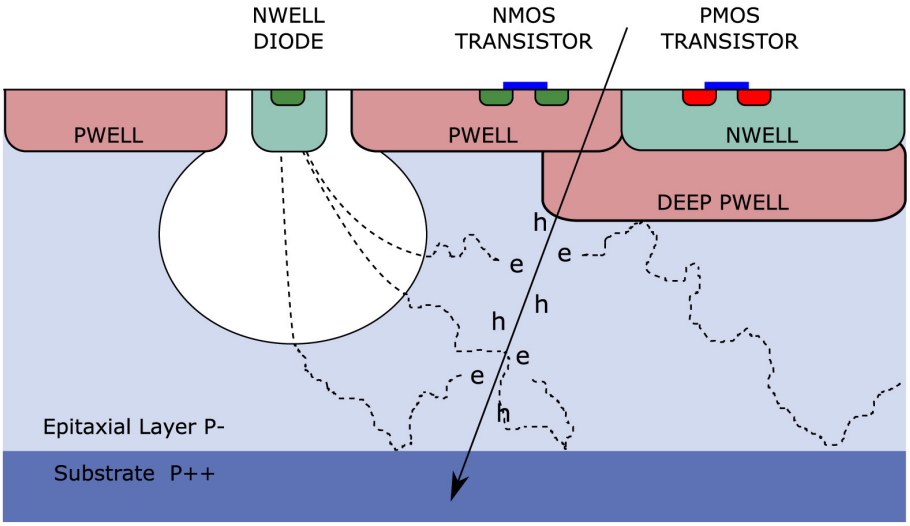


Figure 4.10: Side-view of a particle flying through the substrate of an ALPIDE pixel. [8]

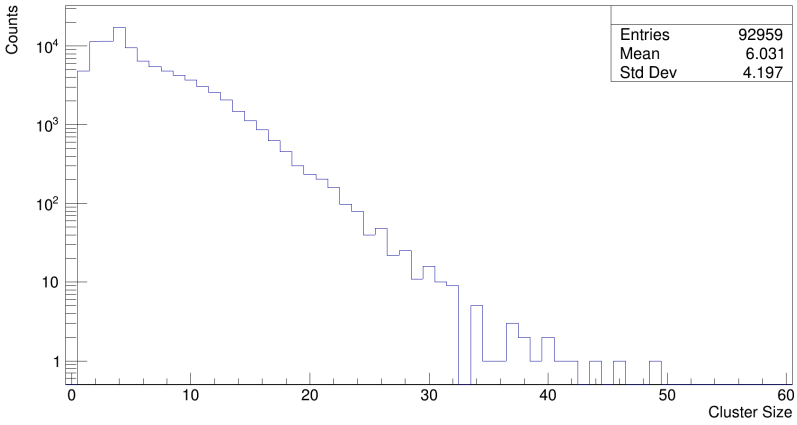
By applying a reverse bias to the substrate and PWELL, the depletion region surrounding the NWELL collection diode increases in size [28]. The white bubble in Figure 4.10 represents the depletion region. The depletion region size directly correlates with the difference in potential between the diode and the substrate.

When a particle penetrates the epitaxial layer, it excites electrons, creating electron-hole pairs. The electrons then slowly diffuse through the layer from the impinging point until they either, lose enough energy to recombine, or enter the depletion region. An electrical field pulls the electrons towards the collecting diode when the electrons enter the depletion region. After collecting enough charge, the pixel registers a hit in a digital latch.

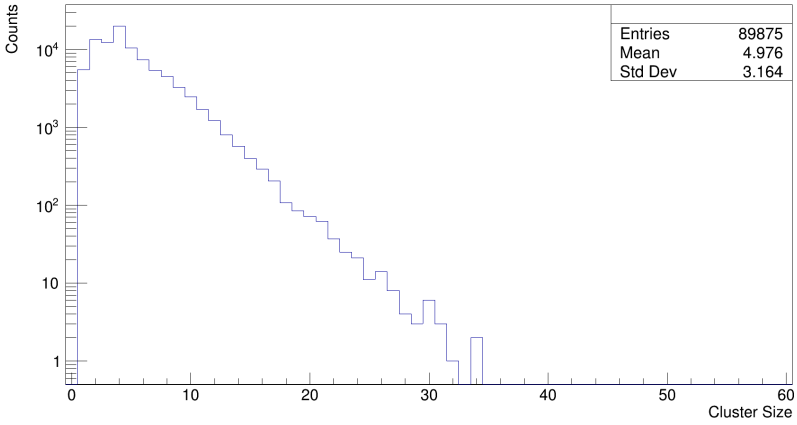
This fact can explain the reduction in cluster size. When the depletion regions increase in size, there is less opportunity for the electrons to diffuse from one pixel to a neighboring pixel and enter its collection diode instead. In other words, all the electrons excited by the incoming particle are collected by diodes closer to the impact point when the substrate has a reverse bias. This way, there are fewer pixels that register a hit, and with fewer pixel hits, the readout process is faster and generates less data [28].

The chip was tested using a beta source to compare cluster sizes with and without back-bias. The source used was a Na-22 with 2-3 MBq activity. Figure 4.11 shows the number of clusters at different sizes from 90k events. Based on these plots, the cluster size decreases by applying a back-bias. In these plots, the effect is more dramatic between 0 V and -3 V than between -3 V and -6 V. This might indicate some diminishing return of the effect, making it unnecessary to use a more negative back-bias voltage.

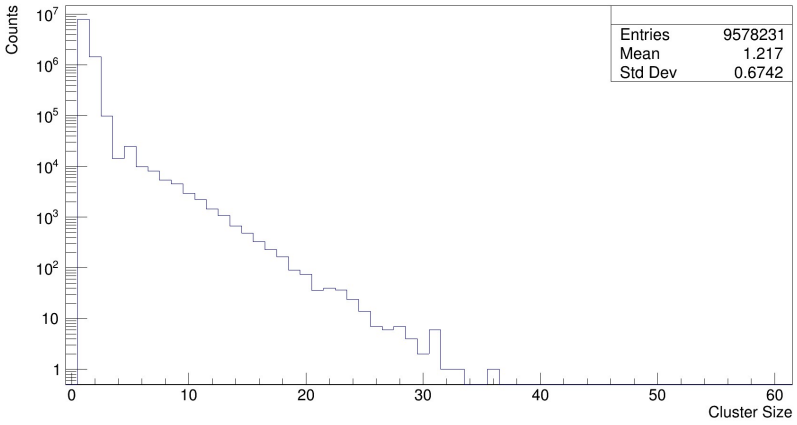
A significant difference to note is that the plot with -6 V has an order of magnitude more entries compared to the other two results, in addition to substantially more entries with cluster sizes of one or two pixels. This order difference may indicate that the chip was more sensible towards noise in the substrate and, therefore, able to register single-pixel hits easier. If the sensibility settings of the chips are adjusted to make the chip less sensible, fewer single-pixel hits should be registered. A test is necessary to confirm or deny this assumption.



(a) 0V back-bias.



(b) -3V back-bias.



(c) -6V back-bias.

Figure 4.11: Logarithmic scale of cluster sizes with different back-bias.

4.3.6 DAC Test and Eye Scan

Due to time constraints, the DAC test was performed after returning to Bergen. Instead, a good set of settings were found early and used for the entire duration of the beam test. There was enough time to perform the eye scan test at CERN before the beam test.

8b10b Encoding

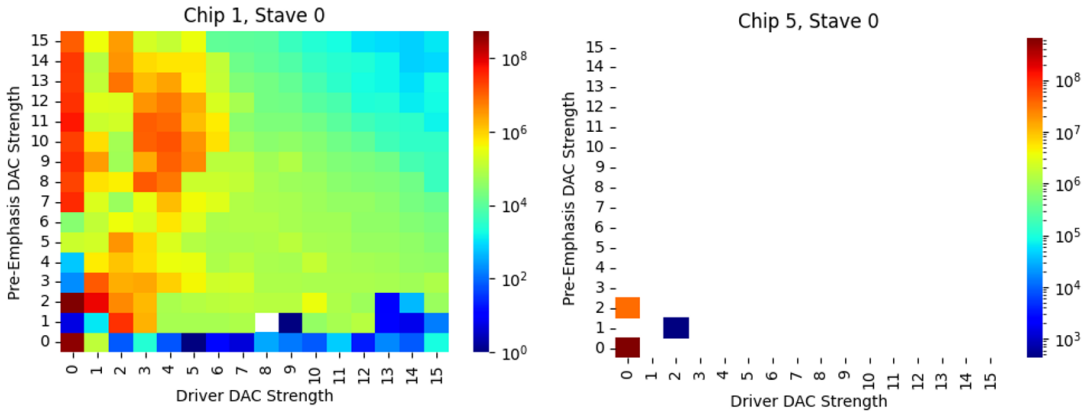
The ALPIDE chips and the RUs use an 8b10b encoding scheme for communication. This type of encoding takes an 8-bit word and turns it into a 10-bit word before sending it over the communication medium. The main purpose is to balance the number of ones and zeros transmitted to achieve a DC balance. The 8-bit word divides into two strings of 5 bits and 3 bits. They are each given an extra bit before being concatenated back together, with the Most Significant Bit (MSB) of the original word being the Least Significant Bit (LSB) in the new 10-bit word and vice versa. The original strings change according to a table describing the possible conversions for each input string. The new bits added are the LSB of each string, respectively. Two rules decide the value of each of the two bits added. First, the difference in how many ones and zeros have been transmitted in the last 20 bits should not be higher than two. Second, the maximum number of ones or zeros in a row should not be more than five.[29]

Generally, two types of errors can occur when decoding a 10-bit word. The receiving module reads a message with a disparity error, or the number of ones and zeros are not within plus/minus 2. Alternatively, the receiving module reads the 10-bit word but cannot convert it back to an 8-bit word because it does not exist in the table for conversion. This error is usually called an Out of Table (OoT) Error. These errors can occur due to an unclear signal on the transmission line.

Data Transmission Settings

The ALPIDEs use a high-speed differential serial line with pre-emphasis to transmit data to the RUs [15]. For IB Mode, the chips transmit data with a data rate of 1200 Mbps. The current delivered to the main line driver of the serial port can be configured in a Digital-to-Analog Converter (DAC) register to suit the characteristics of the line in use. The same DAC register can also configure the pre-emphasis driver in the same fashion. The value of these two drivers is essential to ensuring the RUs collect the data correctly. In this manner, a wrongly configured chip will cause the RU to decipher the receiving words incorrectly. Therefore, a scan testing all the different setting combinations will show which settings work and which do not.

Each DAC setting has 4 bits allocated, meaning they can hold a value between 0x0 and 0xF. In total, there are 256 different combinations of these settings. To characterize the performance of each setting, the RUs issued a set amount of triggers at a steady rate. The ALPIDEs generate a small amount of fake digital hits on each trigger to produce some fake data to transmit. The RUs then report how many 8b10b disparity errors they get from decoding the ALPIDE words. Figure 4.12a and Figure 4.12b show the result for a bad chip and a good chip, respectively.



(a) Poor chip performance (b) Good chip performance

Figure 4.12: Two examples from Data Transmission DAC test on a FoCal half-layer. White spaces indicate zero errors.

From Figure 4.12a it is clear to see that this chip does not perform well. All setting combinations result in more disparity errors than is tolerated, which is zero. One setting combination resulted in a white space, but this cannot be trusted because this result might be a fluke given the unstable nature of all the neighboring settings. For most settings, the difference between them seems gradient, meaning there is a slight difference in the number of errors between one square in the plot and the neighboring squares. This description is mostly accurate, except when either setting has a low value. Here the number of errors makes a jump of several magnitudes.

A possible explanation is that the signal does not correctly propagate through the entire signal line with the driver currents set too low. In support of this explanation, a similar test of DAC settings was performed on the ITS IB module available at Bergen. Figure 4.13 shows the results from this test.

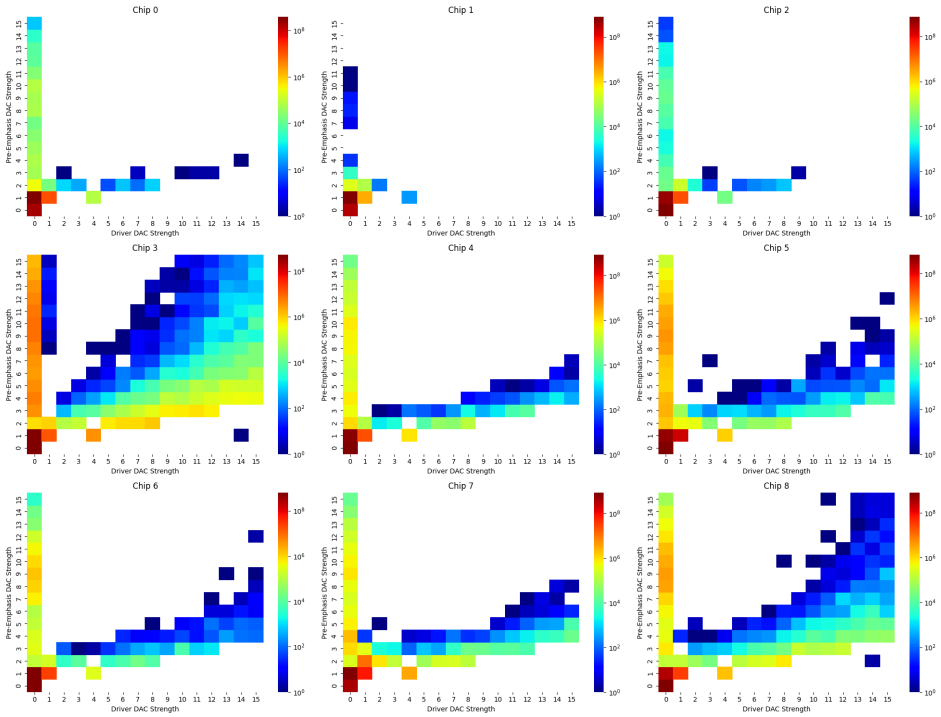


Figure 4.13: Results from ITS Data Transmission DAC scan.

In this figure, the number of errors increases similarly for all chips as the pre-emphasis driver current lowers. Then, suddenly, there are no more errors. This behavior is probably because the signal is too weak for the RU to even recognize an attempt at communication.

FoCal Data Transmission Settings

After returning from the beam test, the DAC scan was performed on as many chips as possible. Due to time constraints, the scan could not be performed prior to the beam test, though this would be preferable. Also, because of issues with broken traces (more details in Section 5.6) several chips were unavailable for the scan.

In total, 15 out of 36 could be characterized. Figure 4.14 shows the result from the chips that took part in the scan.

Most of the chips can operate correctly with most of the setting options. During the beam test, the setting was 0x8 for both the pre-emphasis and the main current driver. Chip 1 from stave 0 in Figure 4.14 got excluded in the beam test because of these decode errors.

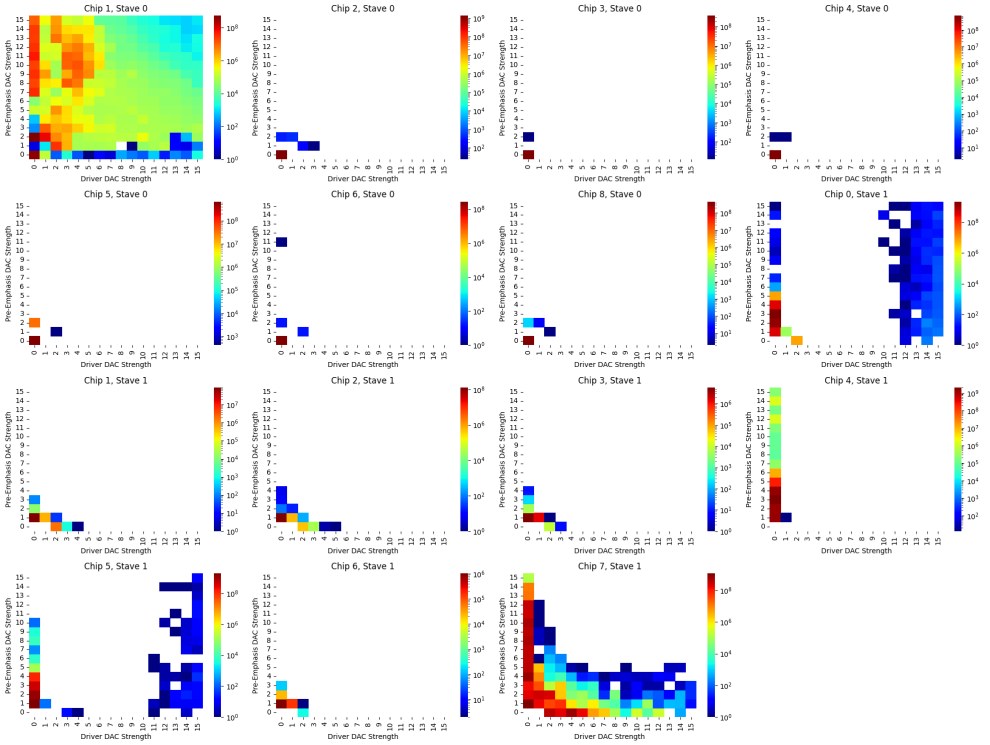
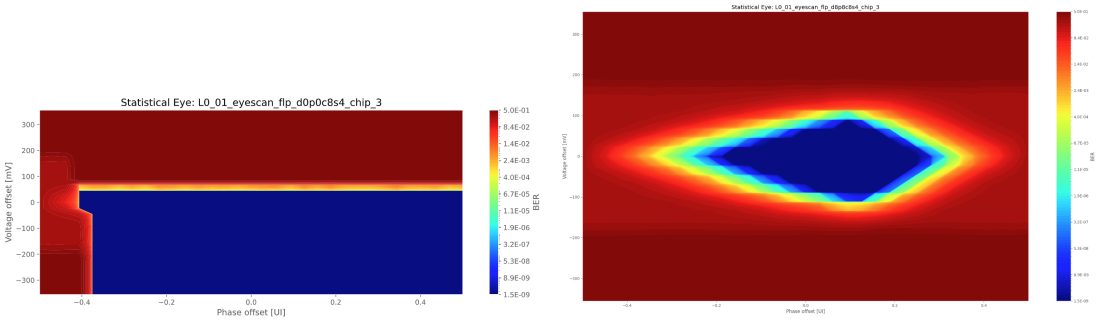


Figure 4.14: Result from scan of driver DACs

Eye Scan

The FPGA has built-in functionality for checking the eye diagram of each transceiver on the RU. The eye diagram provides information about the transition between high and low signals. An open eye means the transition is smooth, while a closed eye means a poor signal. Figure 4.15 below shows two examples. Each transceiver was tested via the built-in function and resulted in eye diagrams equivalent to the picture to the right. As a sanity check of the system, the FireFly cable was disconnected mid-scan to force a lousy eye diagram. This diagram is to the left of the figure, and clearly, it is not good. The eye scan was not performed on every working chip. Primarily because insufficient time, but also issues with the signal deemed it necessary.



(a) (b)

Figure 4.15: Left (a) eye scan where the FireFly was pulled out mid-scan. Right (b) eye scan with a good result.

4.3.7 CRU_ITS Modifications

Several functions in the `testbench.py` are not made for the use of multiple RUs. Modifications where loops did not properly loop through all the RUs were made to accommodate for the additional RUs. The testbench YML file also needed to be updated for the RUs, `CRU_ITS/software/config/testbench_uib.yml`. The link dict dictates how many RUs the testbench should account for, also which CRU links are in use for each RU. The end point configuration files for the CRU also needs to enable the links entered in the YML file. These end point file are located at
`CRU_ITS/software/config/roc_iftmikro0229602_sn0000_ep0.cfg` and `_ep1.cfg`.

5 Beam Test Results

This chapter presents the results achieved from the beam test at the SPS beam. It will also discuss issues that occurred during the beam test, and the action made to fix them. Lastly, this chapter presents a summary of the inspection of the pixel layers in the aftermath of the beam test.

5.1 Type of Runs

The pixel layers had several different types of runs planned for the beam test. These runs were:

- 5 runs with different electron energies (20 GeV, 40 GeV, 60 GeV, 80 GeV and 120 GeV) with 0 V back-bias and triggered via the scintillators.
- 1 run using the ALPIDE chips' internal sequencer with electron energy at 60 GeV.
- 1 run continuously triggering with a fixed rate of 100 kHz with electron energy at 60 GeV.
- 1 run with a -3 V back-bias applied to the ALPIDEs with electron energy at 60 GeV.
- 1 high rate test.

For each run, approximately 100k samples were collected to have statistically reliable results.

When the chips were first operable in the beam hall, three chips reported decode errors, making them unable to gather data reliably. These chips were excluded in the benefit of setting up the system and getting everything to work correctly. Figure 5.1 shows all the included chips for the entire duration of the beam test. The three chips that were excluded, in addition to those mentioned in Table 3, were Chip ID 0 and Chip ID 2 on WT1 and Chip ID 7 on WB2.

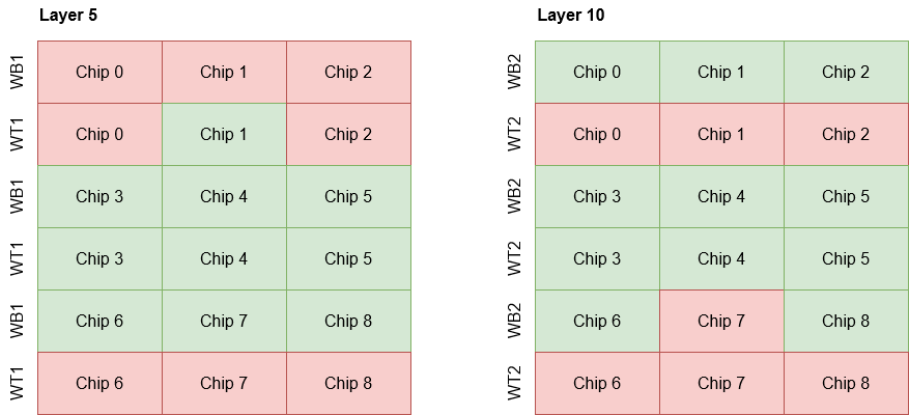


Figure 5.1: Figure of which chips at which position were included/excluded. The areas marked in green represent the chips that were included and the areas marked in red represent the chips that were excluded.

During early runs of the beam test, the system reported many detector timeout errors. The errors seemed to occur whenever the event rate per spill got too high. Attempts to adjust the high-voltage supply for the scintillators confirmed that the detectors timed out when the system received too many triggers at a too high rate. Initially, the strobe duration setting was set to 10 µs, the default value from CRU_ITS. When the rate is high enough, there is a good chance of a trigger being received by the chips while a strobe window is open and then extending it. The RU firmware is designed with continuous readout in mind, not triggered, so when it does not receive an expected data packet from the chip in time, it will flag this lane as timed out. A solution for this issue was to re-configure the strobe duration to last only 200 ns and configure the RUs to delay forwarding the trigger message to the ALPIDE. A trigger delay of 2.5 µs match the peak of the integration time for charge collection in the front-end circuits of the chips. After making these changes, the error of detector timeouts ceased to occur.

The run with back-bias applied to the ALPIDEs was never performed. Zero testing of this feature before the beam test meant that trying it for the first time in the beam hall was risky. The chips displayed some unexpected behaviors when attempting it in the beam hall, and the attempt was quickly terminated. This strange behavior turned out to be because of a user error connecting the power supply and the transition card. In hindsight, the error was correctable in the beam hall. Due to the stressful environment of a beam test, debugging was forfeited in favor of not losing precious beam time.

For the high rate test, the beam energy was configured to the maximum allowed for this beam, 120 GeVs. In addition, the collimator[9] was widened from 2 mm to 2.5 mm to 3 mm, which is the maximum width. The number of events per spill significantly increased with each increase in collimator width. Still, the chips only reported a few busy signals.

5.2 Electromagnetic Shower Event

Figure 5.2 shows one event recorded from the SPS beam test. In the figure, it is clear that the shower center expands between layers 5 and 10 due to the tungsten layers in between. Also, even though some of the chips were inoperable, the layers could still capture most of the shower events hitting the layers' center. Luckily, all of the chips in the middle row of the three by three matrix worked.

[9] A collimator is a device used to focus a beam better by making it more narrow and precise.

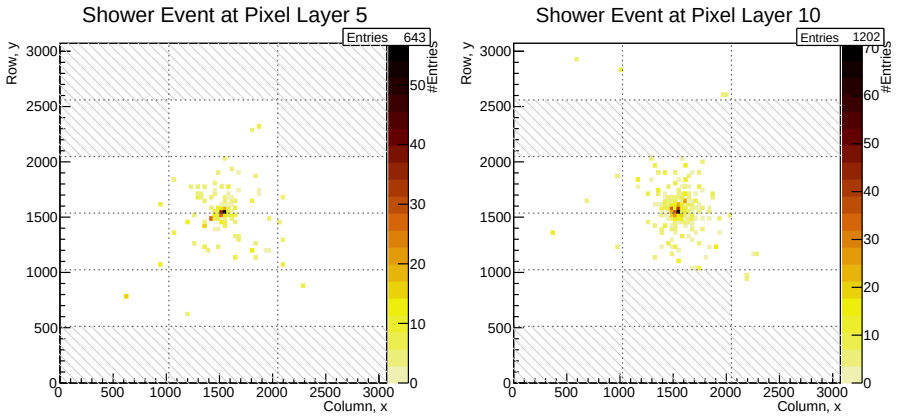


Figure 5.2: A shower event recorded in both Layer 5 and Layer 10[10]. The slashed areas mark the inoperable chips.

5.3 Busy Signals

Some busy signals appeared when running the setup using continuously triggering from the LTU with a frequency of 100 kHz. As mentioned in Section 2.3.5, the readout speed for any pixel is 50 ns. The regions are readout serially and contain about 16,000 pixels (16 double-columns). If 200 of these 16,000 pixels record a hit, it will take 200 x 50 ns = 10 µs to fully read out. A trigger rate of 100 kHz corresponds to 10 µs period between two triggers, which barely makes it possible to read out 199 hits. Therefore, the busy signal is heavily dependent on the evolution of the shower.

5.4 The ITS Readout Electronics

For this beam test, the FoCal test setup used the ITS readout systems. This included the use of an FLP, four RUs, a CRU and an LTU. For the duration of the beam test, no issues as a consequence of the environment were observed. The LTU was triggered by the scintillators, and the number of triggers reported matched the number of triggers from the other two readout systems.

5.5 Non-Working Chip Investigation

After completing the beam test, the setup returned to the Bergen lab, further investigation into why some of the chips were not working ensued. This investigation included checking the current consumption of each three-chip string, doing write and read back of some registers on-chip, looking for hot spots on any chip, and a general visual inspection. One whole half-layer, WB1, had all nine chips working during the beam test and was therefore exempted from these tests. They drew nominal current values, similar to the chip IDs 3-5 on WT1, shown in Table 4.

[10]This figure was made by Max Rauch and is from the data collected at the SPS beam test.

5.5.1 Current Consumption

The other two sets of chips had their flex string extracted from the ZIF connector to test how much current one three-chip string consumed. The power supply supplied the usual 3 V to the transition card. First, the current limiter had the usual limit of 1.5 A for the digital supply and 0.5 A for the analog supply. The goal was to look for the same behavior observed prior to the beam test, where the chips hit the current limit, and the power supply had to drop the voltage. After confirming this behavior, both current limiters were set to the maximum of 3 A before re-powering the string. Table 4 shows the current values recorded. All these tests were performed without providing any clock to the chips.

Layer	Chip ID	Analog [A]	Digital [A]
WT1	0-2	0.046	0.915
	3-5	0.046	0.050
	6-8	0.571	0.390
WT2	0-2	0.044	0.234
	3-5	0.046	0.084
	6-8	0.061	0.309
WB2	0-2	2.437	2.564
	3-5	0.046	0.050
	6-8	0.046	0.050

Table 4: Result from current consumption investigation on all the half-layers.

5.5.2 Communication Test

After testing the power, a simple communication test was performed. This test included writing to several registers on the chip and reading back the written value. Only one set of three chips was connected to the transition card at a time, and the transition card was connected to an RU. All chips were tested regardless of how much power they drew. Table 5 shows the results from this test.

Chip ID	WT1	WT2	WB2
0	Decode Errors	Decode Errors	Not Aligned
1	OK	OK	Not Aligned
2	Decode Errors	Decode Errors	Not Aligned
3	OK	OK	OK
4	OK	OK	OK
5	OK	OK	OK
6	Not Aligned	OK	OK
7	OK	Decode Errors	OK
8	OK	OK	OK

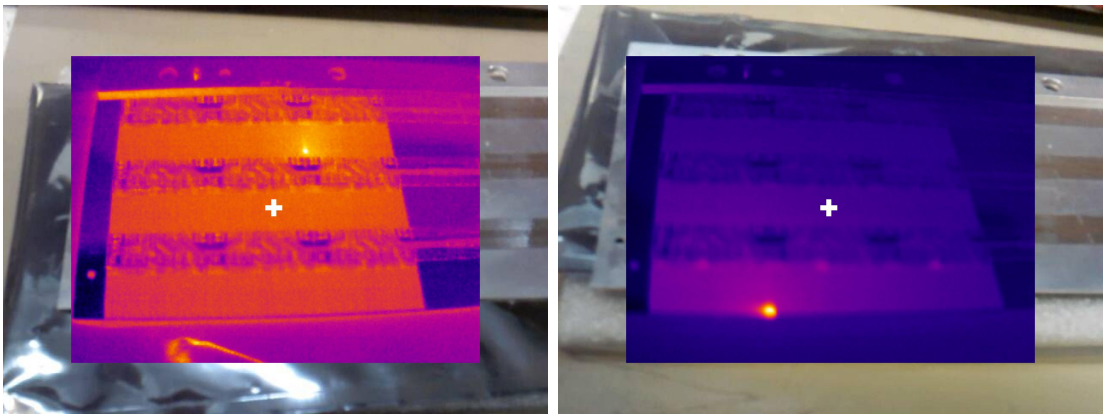
Table 5: Results from communication tests.

The decode error status indicates that the test reported decode errors when attempting to read back the data stream from the ALPIDEs. This points towards an error in the signal integrity of the data link transmitting data upstream. The not aligned status means the transceiver on the RU could not synchronize properly with the data stream, making it unable to sample the stream correctly. Some flex traces were observed broken prior to this test and might be the reason for the communication errors. Section 5.6 discusses the broken traces.

5.5.3 Hot Spots

The high current consumption observed in some of the three-chip strings raise suspicion towards possible short circuits within the chips themselves. A short circuit would create a concentrated area that dissipates a large amount of power. This area has an increased temperature compared to the neighboring region and should be detectable with an infrared camera. Therefore, the chips were powered on and investigated with an infrared camera to look for these hot spots. Figure 5.3, 5.4 and 5.5 shows the thermal image capture from the three half-layers.

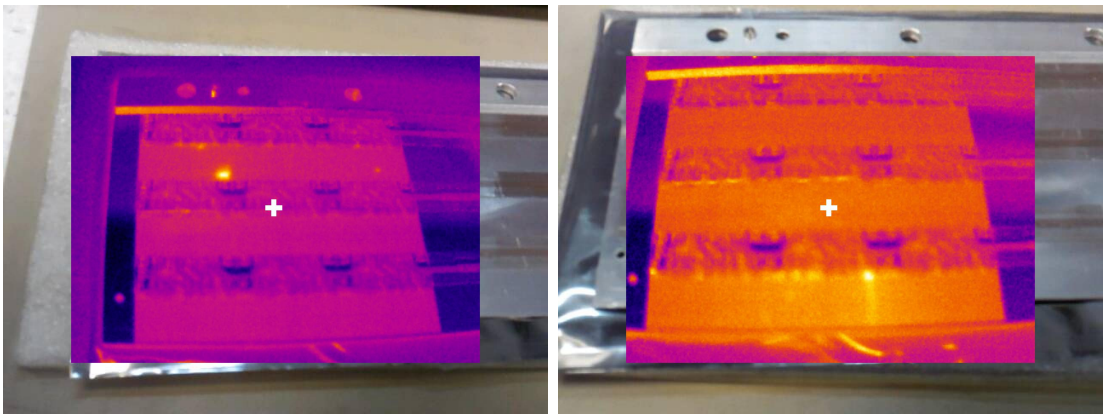
WT1



(a) (b)

Figure 5.3: Hot spots observed on WT1 half-layer. Right (a) Chip ID 0 with temperature measured at $\sim$ 33 °C. Left (b) Chip ID 8 with temperature measured at $\sim$ 63 °C.

WT2



(a) (b)

Figure 5.4: Hot spots observed on WT2 half-layer. Right (a) Chip ID 2 with temperature measured at $\sim$ 34 °C. Left (b) Chip ID 7 with temperature measured at $\sim$ 33 °C.

WB2

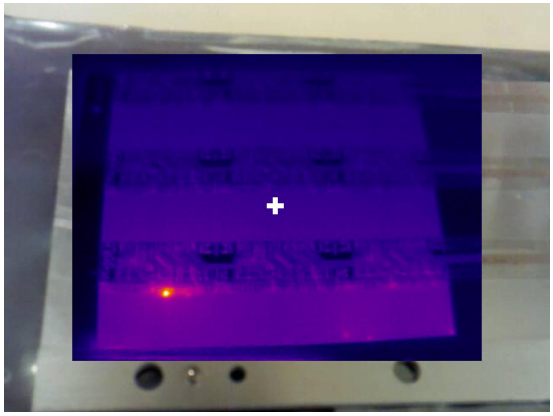


Figure 5.5: Hot spot observed on WB2 half-layer. Chip ID 2 with temperature measured at $\sim$ 56 °C.

5.5.4 Visual Inspection

A visual inspection looked for any physical flaws on either the flex string or the chips themselves. Figure 5.6 shows a visible crack in the pixel matrix of Chip ID 2 on WT2 half-layer. The location of this crack is the exact location of the hot spot observed on the same chip in Figure 5.4a.

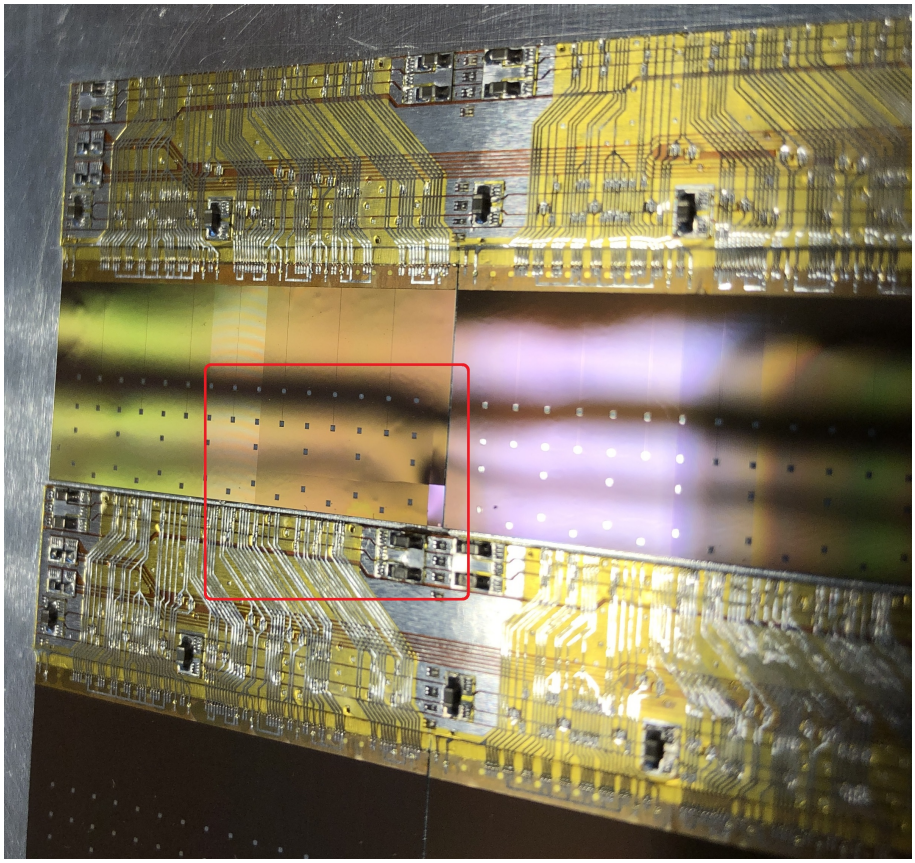
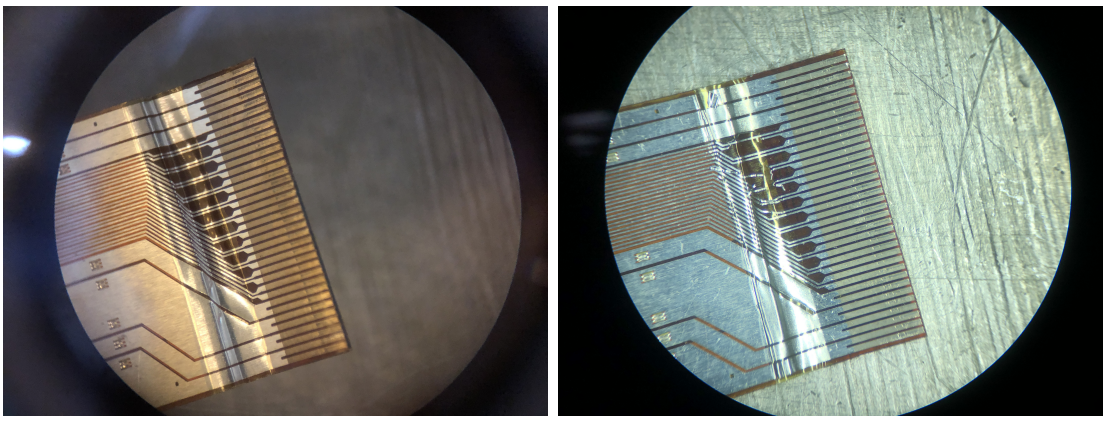


Figure 5.6: Visible crack in Chip ID 2 on the WT2 half-layer.

After using a microscope to investigate all chips, there were no other obvious flaws.

5.6 Broken Traces

During all the testing, assembling, and dissembling, the aluminum traces on the flex string wore down and eventually broke. As the aluminum is bent back and forth several times, the metal crystallizes, making it more brittle to the point where it snaps easily. The stresses applied from the unplugging and re-plugging force this crystallization. Figure 5.7 shows a flex string with no broken traces and a flex string with several broken traces. When the traces break, the connection to the chips is lost. For the most part, the data link traces broke (the thinnest strips), meaning the chips could not transmit their data. Appendix A includes several more pictures of the flex traces.



(a) (b)

Figure 5.7: Right (a) show a flex connector with no broken traces. Left (b) shows a flex connector with several broken traces. More pictures can be found in Appendix A.[11]

The current design of the flex strings has a thin part close to the end to allow for flexibility when inserting the string into the ZIF connector. As a consequence, it also breaks easily. The top design in figure 5.8 shows where this thin part is located. The idea was to allow for some bending to make it easier to insert the string, but this was unnecessary. The transition card can be loosened slightly to allow for easier insertion. With this in mind, two new solutions have been designed to reduce the probability of traces breaking from repeated insertions. Figure 5.8 shows these two solutions. Both designs remove the thinnest section of the string to make it stiffer, relying on the adjustment of the transition card for easy insertion. The current plan is to use design 1 in future layers.

[11] All pictures of traces are taken by Tea Bodova.

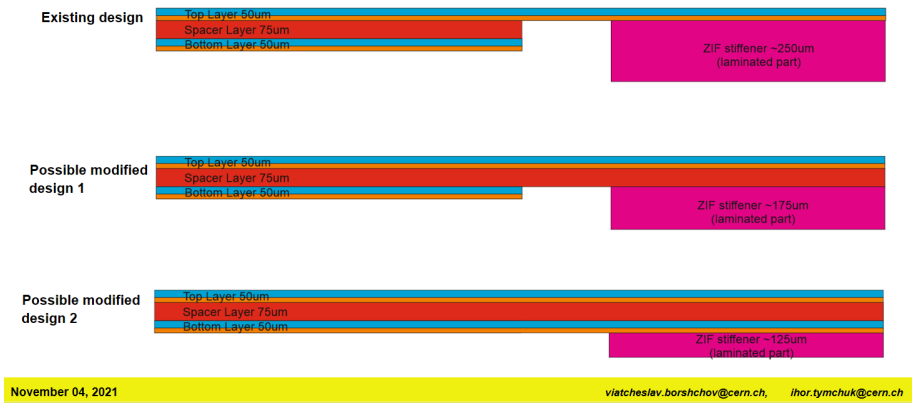


Figure 5.8: The current design of the flex string and two possible replacement designs. Designed by Ihor Tymchuk (Research and Production Enterprise LTU).

5.7 CRU_ITS Shortcomings

The CRU_ITS provided the necessary software tools required for the beam test. However, it had several difficulties to overcome. Firstly, multiple RUs are not sufficiently supported, and modification had to be made. Some of these modifications were easy to find and apply a fix, while others where difficult to understand. The software does not support disabling different CHIPIDs on different RUs at all, and a list of which chips to disable had to be hard coded into the functions. Therefore, a modification on the UiB_FoCal branch have now this functionality.

The data-taking script always configures everything every time the script is started. The configuration process takes several minutes to complete. During the beam test, restarts of the data-taking script happened often, wasting a lot of time with this configuration step without any changes applied to the setup. Attempts at making separate script for setup, run and tear-down of the setup were unsuccessful. The scripts are hard to pull apart, and a major refactoring is required to make this separation.

6 Conclusion and Outlook

In summary, this thesis has given an overview of the design and preparation for the first beam test for the FoCal detector. The beam test was performed at the SPS beam located at CERN. After the beam test, an investigation into the problematic chips to look for apparent faults causing them to be problematic took place.

6.1 Conclusion

The beam test was a largely successful beam test regarding the pixel layers. Late arriving chips made for a stressful situation with little time to get the setup working. However, by sacrificing fixing the broken chips, the setup got working in time for the start of the beam test and data was gathered successfully. The Bergen pixel setup included several new components for the beam test. These upgrades include incorporating the LTU into the system as a source of triggers. Additionally, the re-configuration of the CRU allowed for three more RU in the setup.

Except for a back-bias run, all the runs planned for the pixel layers took sufficient data amounts for analysis. The data analysis will provide crucial results helping FoCal receive the final needed acceptance from the LHCC. The back-bias run turned out to be due to a user error in a stressful environment and would have been avoided with an earlier arrival of the pixel layers in Bergen.

The FoCal project gained valuable experience running a detector in a beam test. This experience will improve the efficiency of future beam tests of this project.

Through the work of this thesis, a significant impact of have a fully functional lab setup in Bergen has been achieved. In addition, a manual explaining concisely how to operate the system has been written. This manual provides a good basic understanding of how to start data-taking runs, and which configuration file to edit.

6.2 Outlook

The beam tests provide valuable information about the performance of the chips in a high radiation environment. The ability to capture the entire electromagnetic shower without any blind spots is a vital feature to have working properly. Therefore, a goal for the next beam test is to have two complete pixel layers, with every single chip working correctly. There should also be a focus on making a new attempt to use the ALPIDE chips' back-bias feature. The pad layers should also have their full test setup ready for the next beam test, making it possible to compare the results better.

For the final version of FoCal, a common readout system for both the pixel and pad layers is preferable. This system will reduce the requirement of cabling and general infrastructure surrounding the detector, lower costs, and be simpler to maintain. The discussions necessary to achieve this have already begun. An important decision is whether to base the solution on the current readout system of ITS or base it on the solution used by the pad layers. The ITS system would require substantial modifications to accommodate

for this change, but it requires change regardless of whether it includes the pads or not.

The final detector cannot use the CRU and the RU from ITS. The reason is that these cards use components that may soon be out of production, meaning an order of the necessary components needs to happen soon. Therefore, the decision is to either redesign a new readout system similar to the ITS system, possibly including the pad layers, or incorporate the pixel layers into the current pad readout system. Regardless, the ITS readout system works as a good prototype until a specialized FoCal readout system is ready for testing.

ITS will eventually move on from ITS2 and upgrade to ITS3. With this upgrade, some early ideas of a new ALPIDE chip are interesting for FoCal. For ITS, an exciting feature of this new chip is the ability to bend it. Bending the chip makes it possible to place it close to the IP of ALICE. Other improvements, such as an increase in the transmission rates, smaller pixel sizes, and a substantially shorter integration time, are also attractive features for ITS and FoCal [30]. Especially is the possible reduction in the integration time of the front-end analog pixel matrix. A shorter integration time allows for a higher trigger rate because the probability of capturing two hits from the same incoming particle drastically reduces with a lower integration time.

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Appendix A Images of Broken Traces

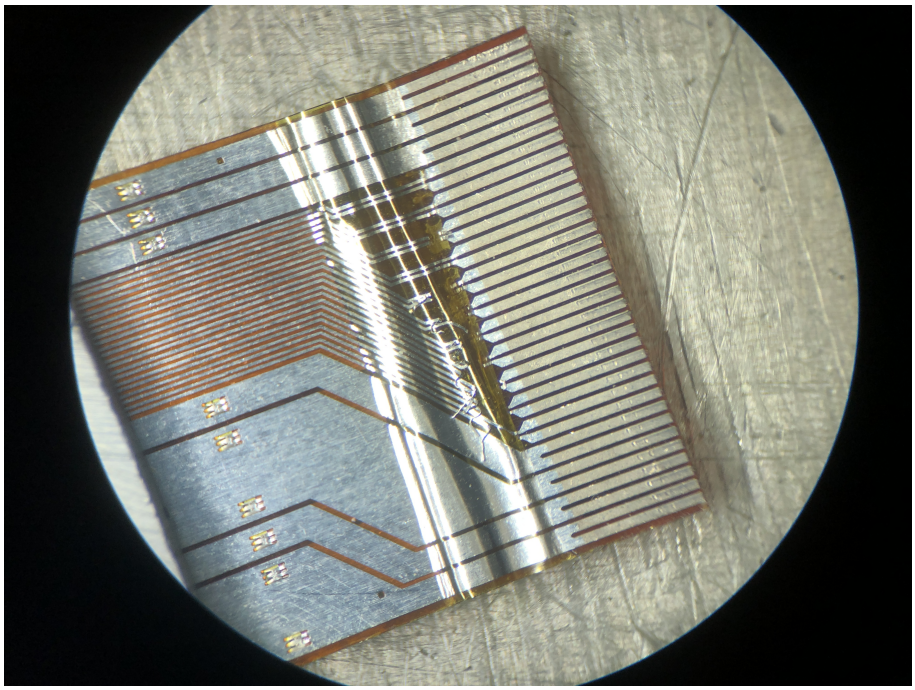


Figure A.1: Flex traces from layer WT1 Chip IDs 0, 1, 2.

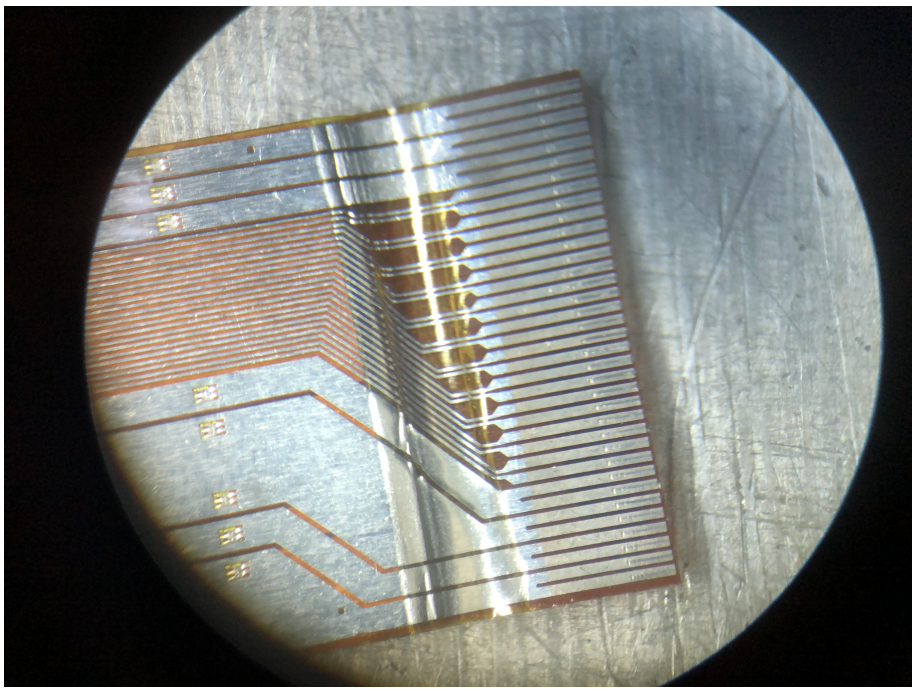


Figure A.2: Flex traces from layer WT1 Chip IDs 3, 4, 5.

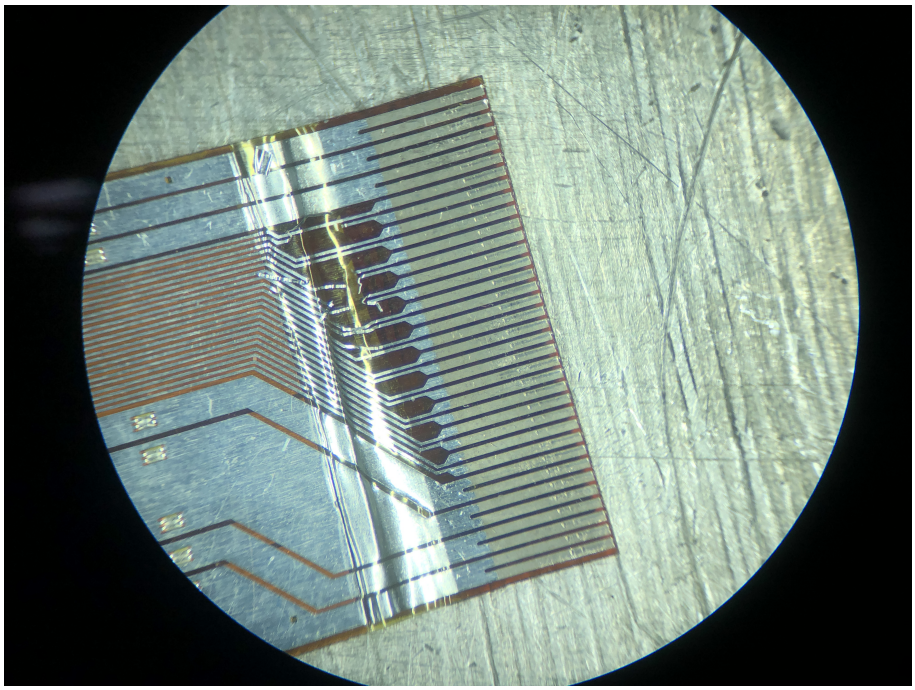


Figure A.3: Flex traces from layer WT1 Chip IDs 6, 7, 8.

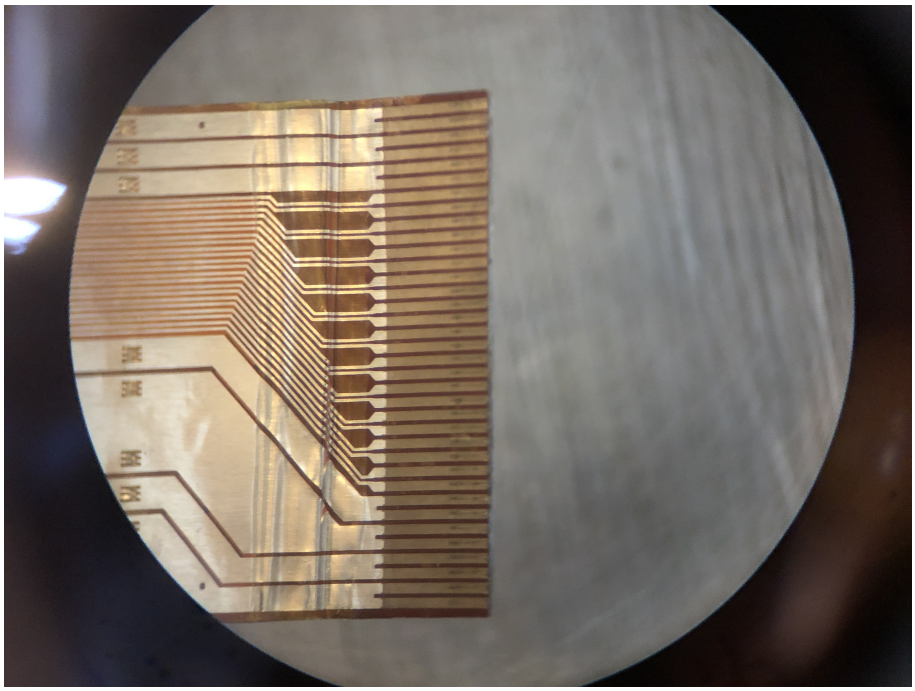


Figure A.4: Flex traces from layer WT2 Chip IDs 0, 1, 2.

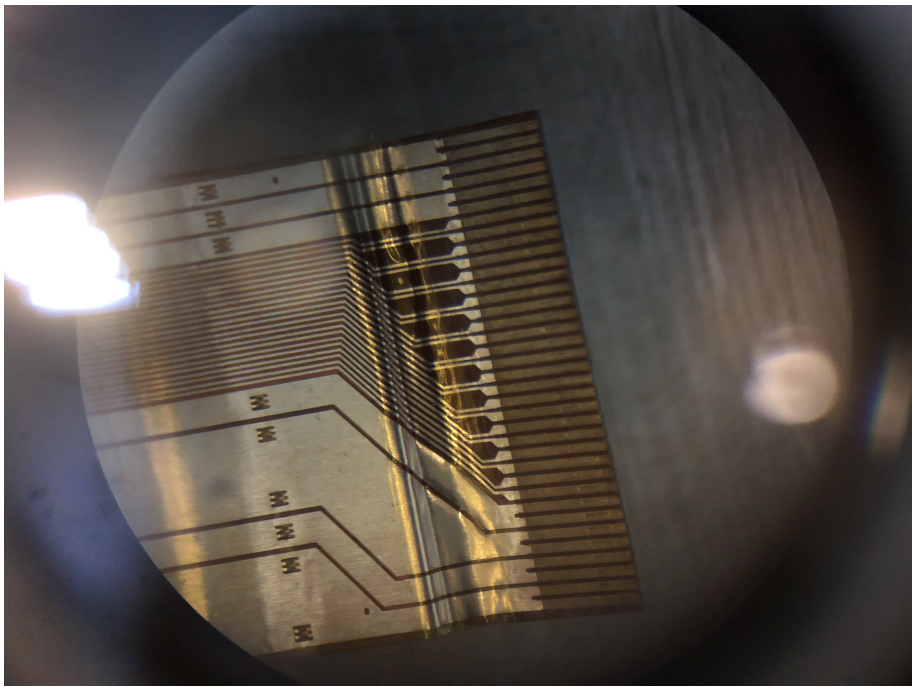


Figure A.5: Flex traces from layer WT2 Chip IDs 3, 4, 5.

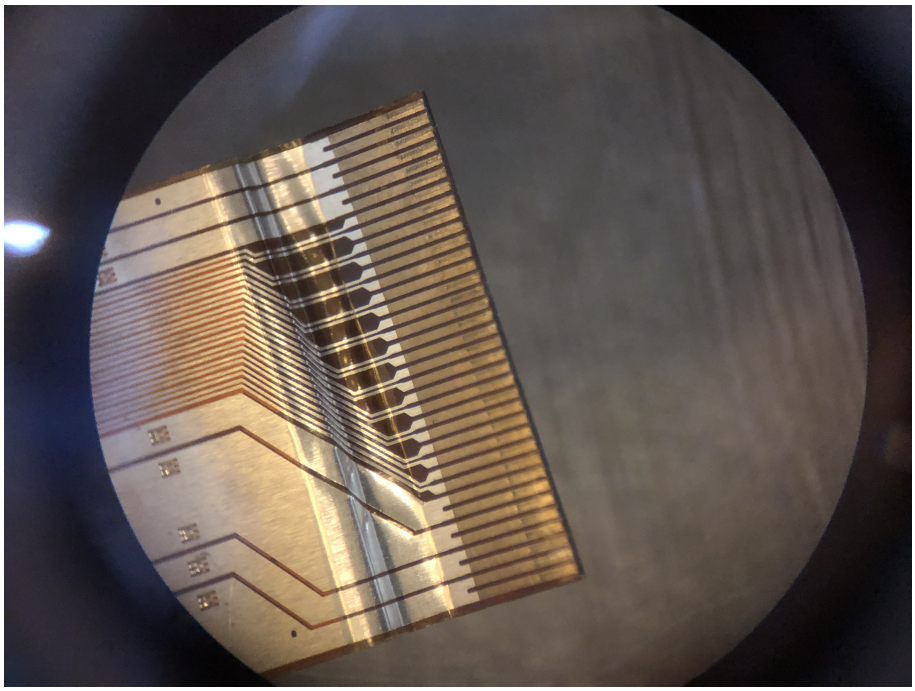


Figure A.6: Flex traces from layer WT2 Chip IDs 6, 7, 8.

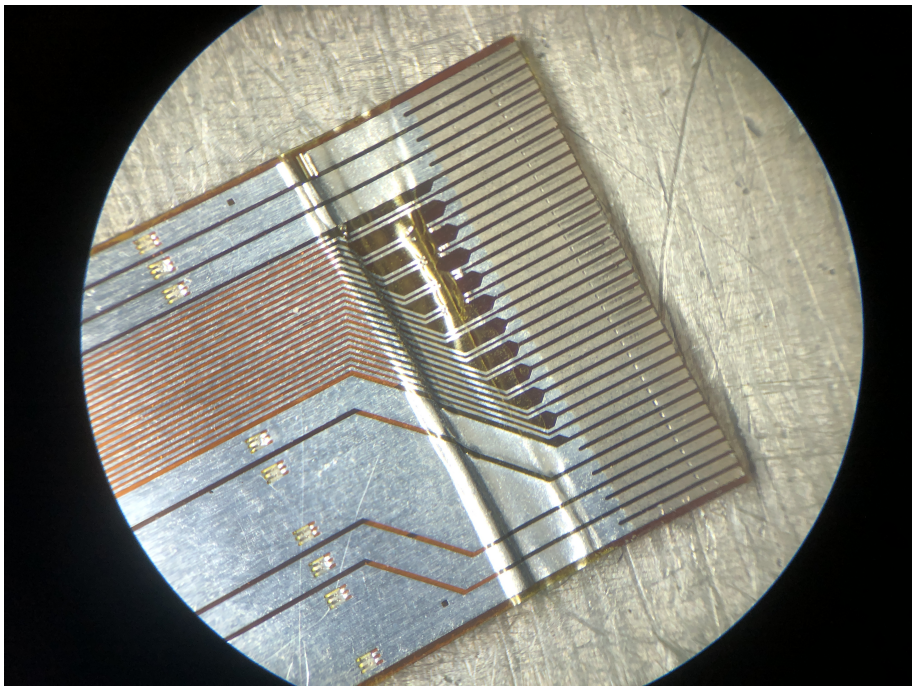


Figure A.7: Flex traces from layer WB2 Chip IDs 0, 1, 2.

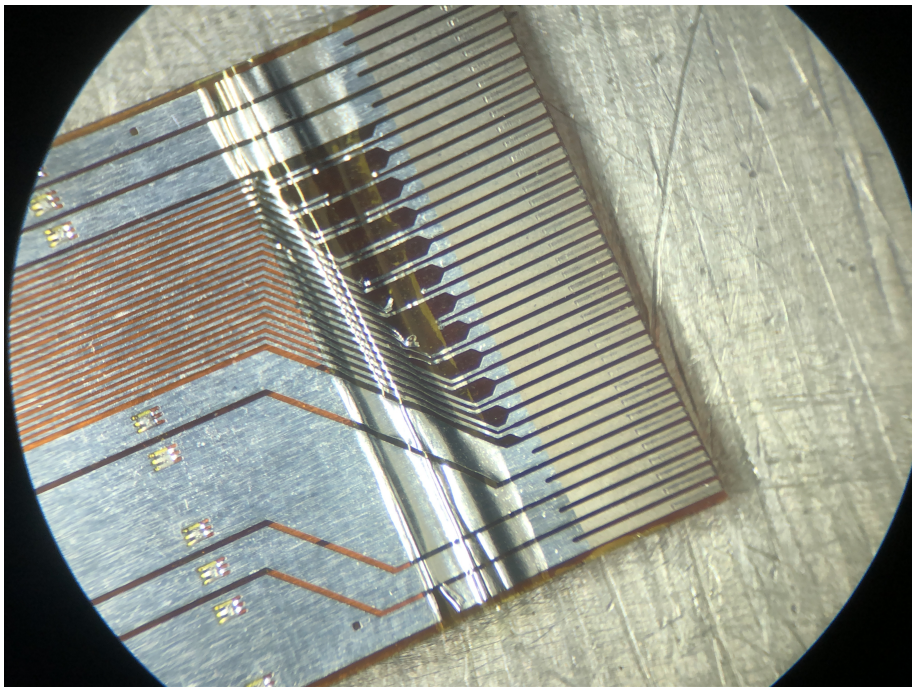


Figure A.8: Flex traces from layer WB2 Chip IDs 3, 4, 5.

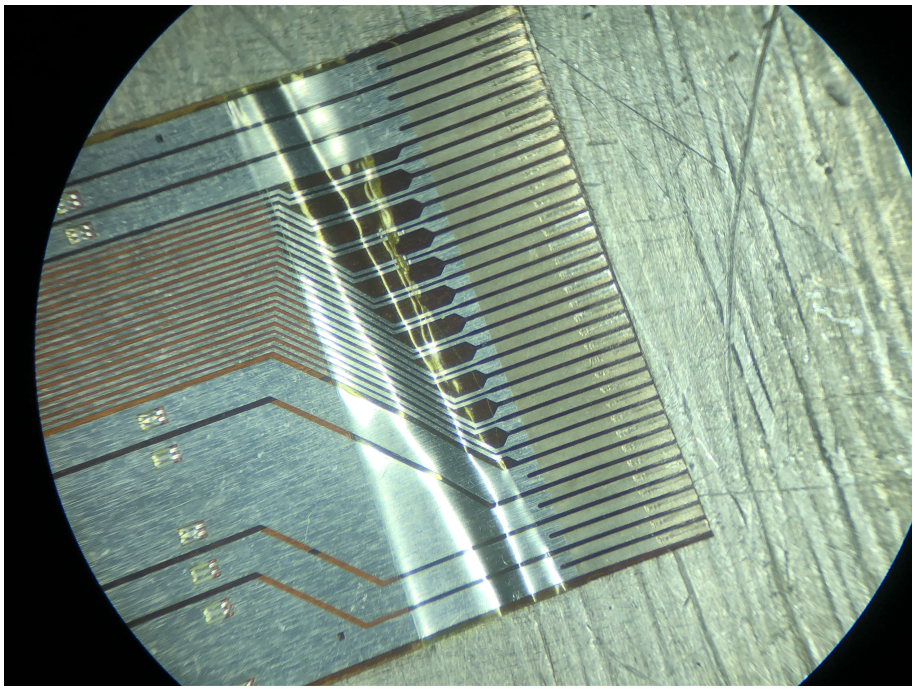
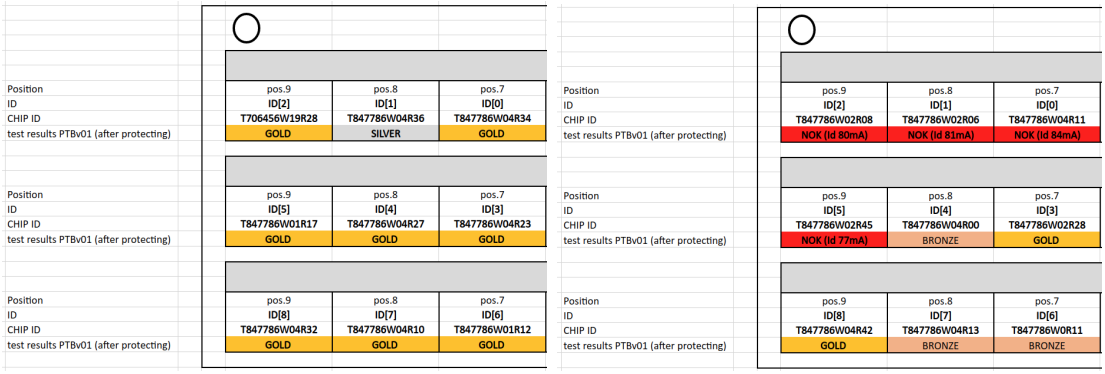


Figure A.9: Flex traces from layer WB2 Chip IDs 6, 7, 8.

This set does not include any pictures of the WB2 half-layer. The setup currently uses this half-layer and unplugging it risks breaking them further, rendering them useless for the setup. This is not worth it.

Appendix B Power Test Results



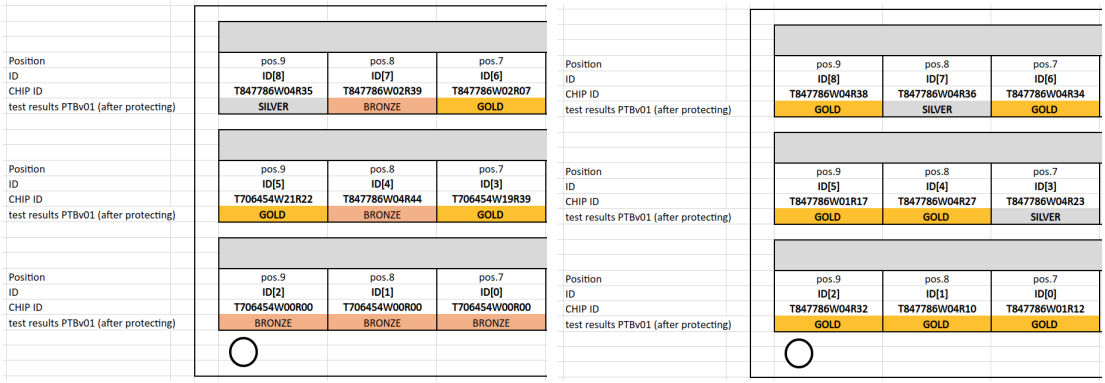
Position	pos.9	pos.8	pos.7
ID	ID[2]	ID[1]	ID[0]
CHIP ID	T706456W19R28	T847786W04R36	T847786W04R34
test results PTBv01 (after protecting)	GOLD	SILVER	GOLD
Position	pos.9	pos.8	pos.7
ID	ID[5]	ID[4]	ID[3]
CHIP ID	T847786W01R17	T847786W04R27	T847786W04R23
test results PTBv01 (after protecting)	GOLD	GOLD	GOLD
Position	pos.9	pos.8	pos.7
ID	ID[8]	ID[7]	ID[6]
CHIP ID	T847786W04R32	T847786W04R10	T847786W01R12
test results PTBv01 (after protecting)	GOLD	GOLD	GOLD

(a)

Position	pos.9	pos.8	pos.7
ID	ID[2]	ID[1]	ID[0]
CHIP ID	T847786W02R08	T847786W02R06	T847786W04R11
test results PTBv01 (after protecting)	NOK (Id 80mA)	NOK (Id 81mA)	NOK (Id 84mA)
Position	pos.9	pos.8	pos.7
ID	ID[5]	ID[4]	ID[3]
CHIP ID	T847786W02R45	T847786W04R00	T847786W02R28
test results PTBv01 (after protecting)	NOK (Id 77mA)	BRONZE	GOLD
Position	pos.9	pos.8	pos.7
ID	ID[8]	ID[7]	ID[6]
CHIP ID	T847786W04R42	T847786W04R13	T847786W0R11
test results PTBv01 (after protecting)	GOLD	BRONZE	BRONZE

(b)

Figure B.1: Results from a power test performed in Ukraine before shipment. Left (a) shows the results of WT1 half-layer. Right (b) shows the results of WT2 half-layer.



Position	pos.9	pos.8	pos.7
ID	ID[8]	ID[7]	ID[6]
CHIP ID	T847786W04R35	T847786W02R39	T847786W02R07
test results PTBv01 (after protecting)	SILVER	BRONZE	GOLD
Position	pos.9	pos.8	pos.7
ID	ID[5]	ID[4]	ID[3]
CHIP ID	T706454W21R22	T847786W04R44	T706454W19R39
test results PTBv01 (after protecting)	GOLD	BRONZE	GOLD
Position	pos.9	pos.8	pos.7
ID	ID[2]	ID[1]	ID[0]
CHIP ID	T706454W00R00	T706454W00R00	T706454W00R00
test results PTBv01 (after protecting)	BRONZE	BRONZE	BRONZE

(a)

Position	pos.9	pos.8	pos.7
ID	ID[8]	ID[7]	ID[6]
CHIP ID	T847786W04R38	T847786W04R36	T847786W04R34
test results PTBv01 (after protecting)	GOLD	SILVER	GOLD
Position	pos.9	pos.8	pos.7
ID	ID[5]	ID[4]	ID[3]
CHIP ID	T847786W01R17	T847786W04R27	T847786W04R23
test results PTBv01 (after protecting)	GOLD	GOLD	SILVER
Position	pos.9	pos.8	pos.7
ID	ID[2]	ID[1]	ID[0]
CHIP ID	T847786W04R32	T847786W04R10	T847786W01R12
test results PTBv01 (after protecting)	GOLD	GOLD	GOLD

(b)

Figure B.2: Results from a power test performed in Ukraine before shipment. Left (a) shows the results of WB1 half-layer. Right (b) shows the results of WB2 half-layer.

Appendix C Lab Setup Manual

This appendix explains how to use essential commands from the CRU_ITS git repository. Most of these commands assume that the current directory is
`git/CRU_ITS/software/py`
For other commands, the correct directory is stated in the text.

C.1 LTU Power Cycle

Step 1 - Check status

The LTU needs two system saervices running on the FLP for proper operation. Check the status of **rarpd** and **ltu_server.service** by using the following command wherever in the terminal:

```
systemctl status rarpd

systemctl status ltu_server.service
```

Figure C.1 shows the result of the `systemctl status rarpd` function. The function `systemctl status ltu_server.service` should yield a similar result if everything is in order.

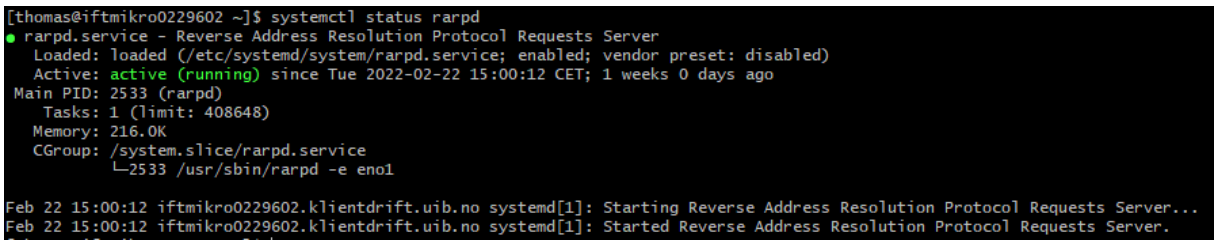


Figure C.1: RARPD status.

If either one of these two services does not display the green *active (running)* text, the first course of action should be to restart the problematic service. A restart command can be executed with sudo privileges using the following command:

```
sudo systemctl restart <insert service>
```

If this does not fix the problem, further investigation is required.

The following commands can check that the LTU correctly communicates with the CRU by returning a "True" value. The commands are:

```
./testbench_uib.py ltu is_ltu_on

./testbench_uib.py rdos 0 trigger_handler is_timebase_synced
```

These commands are independent of the services and can always be run to check the CRU - LTU communication.

Step 2 - Initialize

Before initializing the LTU, the services mentioned in step 1 need to be up and running. These commands need to be run every time either the LTU or the FLP have been turned off and on again. The commands for initializing the LTU are:

- `atb` - When the process is complete, information about the LTU connection is displayed.
- `atb 25` - When the process is complete, type q and press enter in the new shell to exit it.
- `atb 25 emuinit` - When the process is complete, type q and press enter in the new shell to exit it.
- `ttcpon focal_25.net init` - When this process is complete the LTU should be functional.

Step 3 - Running

The LTU has a GUI that can be used for controlling the triggers from the LTU. The GUI is accessed by using the following command wherever in the terminal:

```
qtltu
```

This opens a new window, where the correct IP address and address file need to be filled in. After those are correct, press the "Open" button, and after about 10 seconds, the "Standalone" radio checkmark should be filled in, see figure C.2.

Figure C.2: Screenshot of the qtltu GUI window.

By pressing the "CTP emulator" button, a new window will appear where it is possible to control the trigger configuration of the LTU, see figure C.3.

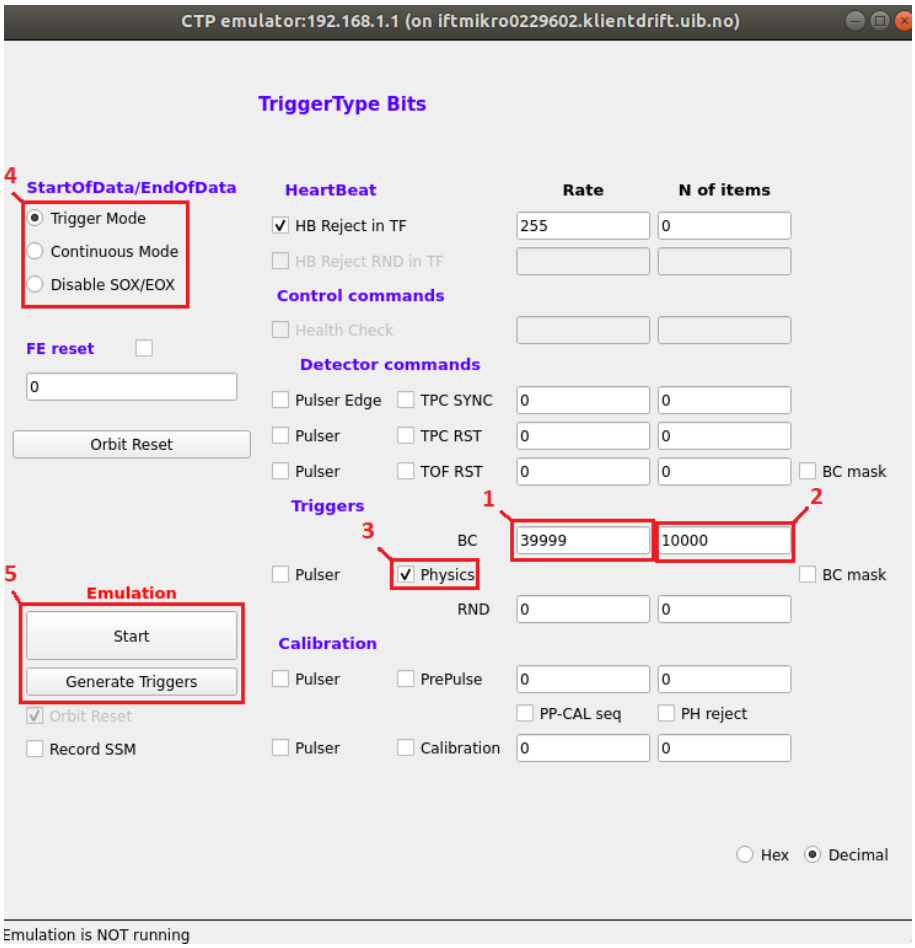


Figure C.3: Screenshot of the CTP emulator window

The value set in the red box marked with a "1" sets the rate of triggers that the LTU will send. A tooltip will appear by hovering the mouse over the box, displaying how to format the desired rate of triggers.

The value set in the red box marked with a "2" sets the number of triggers the LTU will send. A tooltip will appear by hovering the mouse over the box, displaying how to format the desired number of triggers. To make the LTU send infinite triggers, enter "inf" as a value in the box.

The checked marker in the red box marked with a "3" tells the LTU if it should send "Physics triggers" or not. This option needs to be checked off if the LTU is used in triggered mode.

The radio buttons in the red box marked with a "4" set the triggering mode for the system. This setting decides if the LTU sends a Start Of Triggered or Start Of Continuous packet at the beginning of the emulation and End Of Triggered or End Of Continuous at the end of the emulation. The last option of "Disable SOX/EOX" sends neither of these packets.

The "Start" button in the red box marked with a "5" starts emulating these trigger settings. The "Generate Triggers" button will generate a new set of triggers according to

the box marked with a "2". If the value was set to 10,000 triggers and the process was started, all 10,000 triggers were sent. Hitting the "Generate Triggers" button will send 10,000 new triggers without restarting the emulation with the "Start" button.

C.2 CRU Power Cycle

Step 1 - Initialize

After power cycling the CRU, it needs to be re-initialized. The following command will perform the re-initialization:

```
./testbench_uib.py cru initialize
```

Step 2 - Configure

The CRU needs to be correctly configured according to the number of RUs connected to it and if there is an LTU in the system. The configuration files are located at `git/CRU_ITS/software/config/roc_iftmikro0229602_sn0000_ep0.cfg` and the `ep1.cfg`. The following command will configure the CRU:

```
bash ../sh/clusterssh_tools/configure_all_crus.sh
```

C.3 RU Power Cycle

Step 1 - Configure GBTx0 (Special step)

One of the RUs currently connected to the Bergen setup requires a manual initialization of its GBTx0 module via a module. A separate program outside of CRU_ITS is needed to perform the manual initialization. The following command assumes the current directory is the folder where this program is located on the PC in use.

```
java -jar GBTx_config/programmerv2.20180725.jar
```

The GUI will often start with an error message which is irrelevant and can be ignored. After the error message is dealt with, a GUI similar to the window displayed in figure C.4.

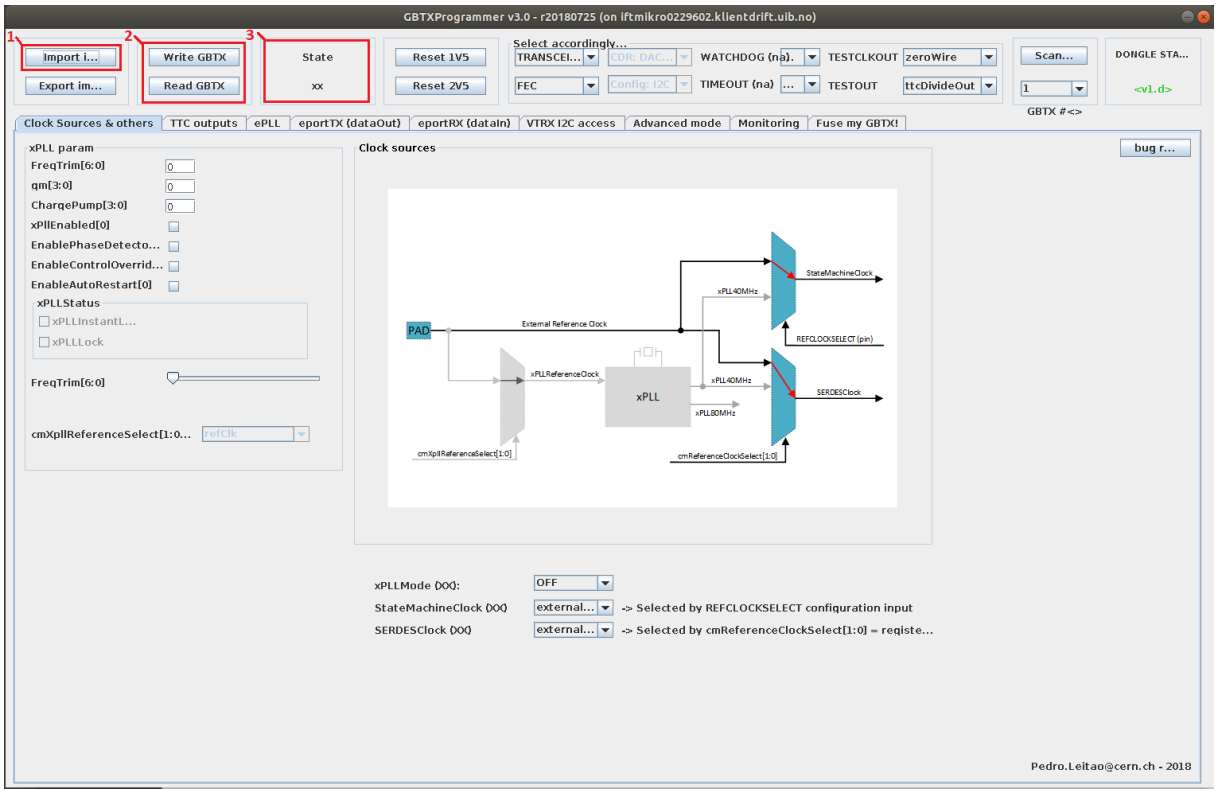


Figure C.4: Screenshot from the GBTx_programmer GUI.

First step is to click on the button in the red box marked with a "1". This will import an image to the GBTx0 module. The image is an XML file located in the `GBTx_config` folder.

The next step is to click "Write GBTX" in the red box marked with a "2", and after click "Read GBTX" in the same box. If everything is correct, the state of the GBTx0 is displayed in the red box marked with a "3" and should say "Idle".

Step 2 - Initialize

After this GBTx0 has been initialized, the rest of the RUs can also be initialized. The two following commands will initialize the RUs and their GBTx1 and GBTx2.

```
./testbench_uib.py initialize_all_rdos
```

```
./testbench_uib.py initialize_all_gbtx12
```

To check if general communication between the CRU and RUs is as it should, the following command can be used. This command will display the current firmware of the CRU and RUs.

```
./testbench_uib.py version
```

Step 3 - Running

The RUs need to provide a clock for the chips. In the UiB_FoCal branch of the CRU_ITS

git repository, a command for turning on all the chips clocks has been added. The following command will enable clock on all chips on all RUs:

```
./testbench_uib.py enable_all_dclk
```

After all the clocks have been turned on, the setup can start taking data using the DAQ script. The DAQ script will configure the chips and RUs according to settings set in a configuration file located at `git/CRU_ITS/config/daq_test_uib.py`. The following command will start the script with the correct configuration file:

```
./daq_test.py -c ../config/daq_test_uib.cfg
```

The script will continuously print out values from the RUs, indicating the current status of the setup. If any errors occur, they will appear in the scrolling text. Depending on the error, they can be ignored, or the DAQ script needs to be restarted. To stop the script, either set an appropriate run time in the configuration file or stop the run by pressing "Q" in the terminal. Using "CTRL + C" will also stop the run, **BUT THIS SHOULD NOT BE USED!** A tear-down process starts when the DAQ script is exited, and if the kill command is used, then the sub-processes will not be correctly stopped causing the next run not to function properly.

When the chips are no longer in use, the clock can be disabled by the following command:

```
./testbench_uib.py disable_all_dclk
```

Step 4 - Flashing New Firmware on the RUs

The firmware of the RUs is in active development, and newer versions are regularly being published. The setup in Bergen should follow these updates for as long as FoCal uses the ITS readout system. The new bit files news to be flashed onto the PA3 on the RU. These files can be found under "Releases" in the "RU_mainFPGA" git repository. A folder containing the bit files will be downloaded by clicking on the "Artifact: vivado" link. These files should be saved under `/home/shared/RU_mainFPGA/` on the FLP. The folder contains several bit files, and the correct file to use is the one ending with `_ecc.bit` and does not include `_bs`. After the bit file has been flashed, the FPGA needs to be reprogrammed. The two following commands will first flash the new firmware to the PA3 and then reprogram the FPGA. After the update, the third command can check the new version.

```
./testbench_.py flash_all_rdo_bitfiles /home/shared/RU_mainFPGA/
*version_folder*/XCKU_top**_ecc.bit
```

```
./testbench_uib.py program_all_xcku
```

```
./testbench_uib.py version
```