University of Bergen

Geophysical Institute

Master Thesis in Energy
Electrical Power Engineering

Control of Grid Connected Inverter

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08.08.2022

Preface

This master thesis concludes the effort of a five year long education for the degree of Master of Science in the field of electrical power engineering at the University of Bergen. The thesis has been submitted in partial fulfilment after having been worked on over the course of two semesters. I am grateful over the Western Norway University of Applied Sciences for providing an office space and a steady work environment from fall 2021 to spring 2022.

I would like to express my sincerest gratitude to my master thesis supervisor: Assistant Professor Eirik Haustveit, for his knowledge, patience and for providing necessary feedback throughout the final two semesters of my thesis. I would also like to express a special thanks to Assistant Professor Omes Jawaid Bajwa, for providing me with practical ideas and for his support.

Finally I wish to express my deepest gratitude to my fellow master students whom I have been working along side for the past two years, some of whom I have had the pleasure of knowing since the start of my five year education. Their presence has been a guiding light towards the completion of my studies, and I would like to thank them for sharing their knowledge and experiences.

Abstract

Power electronic converters and their control systems have played a significantly important role in the integration of renewable energy systems. The application of these converter systems have been rapidly growing as of late, and the subject of improving the systems by means of control is a key topic in research today. The Active Front End (AFE) converter, which allows for the bidirectional power-flow is one of such systems with the possibility of grid tied connection. This master thesis embarks on some of the methods which can be used to provide control over a Grid tied inverter (GTI), for the sake of charging and discharging a battery supply/load. The thesis has been separated into several chapters starting with the needed theoretical framework as an overview over the preliminary knowledge required for the rest of the thesis. The following chapters provide in detail all the required parts of the control and the design of the converter system. Once these chapters have been presented the simulation model is introduced with its results. The last chapters conclude the work by presenting the physical hardware components for a prototype, ending with the final chapter presenting the conclusions and suggestions for future work.

Acronyms

ADC Analog to digital conversion.. 103

AFE Active Front End. ii, 6–8, 101, 104

BESS Battery Energy Storage System. 12, 25–27, 81, 84, 104

CCL Current Control Loop. 32, 41, 42, 44, 54, 59, 67–70, 105, 106

CCM Continuous conduction mode. 13, 14, 104

DAB Dual Active Bridge. 101, 102

DCM discontinuous conduction mode. 13, 14, 52, 104

DERs Distributed Energy Resources. 1, 2

DG Distributed Generation. 1, 2

DPC Direct Power Control. 28, 30, 43, 44, 69, 70, 72, 74, 102, 105, 106, 116

ESS Energy Storage System. 52, 59

EV Electric vehicle. 2

FFT Fast Fourier Transform. 70, 72, 74, 76, 123

GTI Grid tied inverter. ii, 2, 3, 5, 6, 28, 38, 41, 45, 69, 70, 72, 83, 90, 98, 99, 101, 102, 105

IEC International Electrotechnical Commission. 6, 7

IEEE Institute of Electrical and Electronics Engineers. 6, 7, 46, 50, 74, 75, 79, 80, 102

IGBT Insulated Gate Bipolar Transistor. 6, 8, 9, 12, 51–54, 64, 65, 86, 98, 99, 103, 136

KCL Kirchhoff's Current Law. 10

KVL Kirchhoff's Voltage Law. 10

MCU Microcontroller. 83, 84, 86, 87, 93, 99, 100, 103

MO Modulus Optimum. 18, 20–22, 41, 55, 67, 68, 109

MOSFET Metal oxide semiconductor field effect transistor. 6, 8

P Proportional. 19

PCB Printed Circuit Board. 83, 84, 86–88, 90, 103, 107, 132

PF Power Factor. 8, 81

PI Proportional Integral. 17–21, 38, 41, 42, 44, 54, 55, 63, 67–69, 104, 106, 109

PLL Phase Locked Loop. 3, 38, 41, 59, 62, 63, 67, 71, 77, 105

PQ Power Quality. 8, 22

PWM Pulse Width Modulation. 8, 9, 14, 32–34, 36, 38, 45, 51, 63, 67, 104, 106

RMS Root Mean Squared. 22, 23, 46

SO Symmetrical Optimum. 20, 22

SPWM Sinusoidal Pulse Width Modulation. 33, 34, 37, 65, 66

SRF-PLL Synchronous reference frame PLL. 38

SVM Space Vector Modulation. 34, 36, 37, 51

SVPWM Space Vector Pulse Width Modulation. 25, 34, 63–67, 102, 105

TF Transfer function. 19–21, 38, 54–57, 105

THD Total Harmonic Distortion. 22, 23, 46, 50, 70, 71, 73–76, 78–80, 102, 109

THIPWM Third harmonic injection Pulse Width Modulation. 37, 105

UPF Unity Power Factor. 42, 43, 68, 69, 72, 75, 79, 80

UPS Uninterruptible Power Supply. 6

VCL Voltage Control Loop. 41, 42, 59, 67, 68, 70, 78, 105, 106

VOC Voltage Oriented Control. 28, 41, 42, 54, 68, 70, 74, 102, 105, 106

Contents

Chapter 1

Introduction

1.1 Background

The global electrical infrastructure in the latest years has been going through rapid changes, while motivated by the growing concerns over climate change and the environmental degradation. The systemic shift of the global energy structure has also been driven by the increased demand for electrical energy and the rapid technological advancements, particularly in the field of power electronics and the growing battery innovations. Such advancements are playing a key role to the transition towards clean energy and global sustainability.

Climate change and the environmental concerns have lead to policy changes and international treaties such as the "European Green Deal" with its goal to make Europe climate neutral in 2050. The currently proposed strategy to achieve this is by developing a systemic shift from the fossil fuel-based energy infrastructure towards the renewable energy sources and to develop greater improvements in energy efficiency [1]. Conventionally the traditional power generation stations have utilized large synchronous generators, built to operate with a fixed speed and frequency. The generated power is generally transmitted over the electric grid through large centralized facilities, such as fossil fuel based power plants. While the traditional methods have been advantageous they do not come without their own problems. Such as the loss of efficiency due to the large distance the generated energy is transported and should the grid go down, numerous people will be left without power. The development of smaller power systems which are located nearby their respective loads offers a solution, thereby the issues in the Distributed Generation (DG) can be avoided.

Distributed Energy Resources (DERs), are small-scale electrical resources or controllable

loads that are often interconnected with a nearby distribution system or the electrical grid. The DERs include a variety of energy generation systems such as PV solar panels, wind turbines, electrical energy storages and Electric vehicle (EV). Through the development and integration of such systems the future of the power system is going towards a smart grid, offering more control and communication between the producer and the consumer of the energy system. While also offering a viable solution towards the reduction of environmental pollution though the degradation of carbon based energy resources, while gradually developing systems which are better suited to be interconnected with renewable energy sources. This can be observed by the exponential growth of the PV power plants and the massive wind farms which are being constructed worldwide. However it must be stated that the increased development towards a smart grid has come with its own challenges, such as causing the grid structure to become far more complex. The reliability of the renewable energy sources come to question as the overall energy which can be collected can vary greatly due to numerous reasons, such as the meteorological conditions. Furthermore there can often be geographical limitations to these systems, in addition the grid-stability and power quality can be greatly effected by the volatile power generation of such system. While generally these issues have been previously solved through the use of conventional power plants containing large scaled synchronous generators and by the use of reliable and consistent fossil fuel based energy sources such as coal or natural gas. However with the external utility grid seeing an increase of connectivity with DG units, the issues pertaining to the use of renewable energy sources must be solved through the distribution [2].

These growing challenges which we are now faced with, can be prevailed through proper integration and control of the power electronic converters which are contained in their respective generation units. Fortunately the rise of technological advancements and the massive benefits related to the control of power electronic converters. Have lead to great interests being shown in the further research and development of such systems in the last few years. These developments include a copious amount of topologies such as the GTI, and the various control algorithms and methods of grid synchronization. Some of which will be presented in detail in the coming chapters of this thesis.

1.2 Objectives

The objective of this thesis is to design and implement a grid tied three phase bidirectional inverter connected to a battery. In addition to designing and utilizing a variation of control methods to be compared with each-other. The objectives of this thesis is intended to be completed in a set of steps which are as stated:

- Studying past research articles and methods which have been utilized, for the construction of a successful inverter and active front end converter systems.

- Selection of a three phase inverter and DC-DC topology with bidirectional power flow capabilities, while also displaying the characteristics.

- Selecting the different control and modulation structures which are to be used, and develop proper tuning methods for the controllers.

- Designing and calculating the proposed converter filter, while taking standards and requirements of grid connected converter systems into consideration.

- Designing the chosen converter topology and confirming its function using simulation software. choosing the necessary components and testing the bidirectional power flow capability, as well as the different control methods.

- Collecting all the necessary components and constructing a functioning prototype. Take measurements and compare with simulation test results to verify the control methods.

1.3 Outline

The master thesis rapport is divided between the theory and the engineering of the converter model. The theoretical framework as well as the control structure is introduced in chapter 2 and 3. This part of the thesis has more emphasis on the theory behind the required parts which are needed to build and control a grid tied inverter with bidirectional capabilities. Chapter 2 introduces the theoretical framework pertaining to the GTI which will be used further in this thesis. Furthermore DC-DC converter topologies which can be used with the battery supply/load are presented along with several key topics such as filtering, controllers and waveform distortions. While chapter 3 focuses on the control system structure and strategies which are used in the later simulated model. Such as the Park and Clarke coordinate transformations, Phase Locked Loop (PLL) structure, modulation strategies and so on.

Following these two chapters, comes the design and simulation of the converters system and its components which is split into chapters 4 and 5. Where chapter 4 presents the systems proposed topology including all parts such as the filter, inverter and the DC-DC converter with the battery supply/load. This chapter also explains how the different components are dimensioned and how the gain constants for the control are acquired.

Chapter 5 presents the simulation model using the simulation software known as Matlab Simulink and all its components, in addition to introducing and explaining alternative methods for both control and modulation. This chapter ends with the results from the simulation model showing different modes of operation.

Chapter 6 presents the physical hardware and components which are used or was intended to be used, as well as the design schematics of the intended PCB circuits. Due to a global chip shortage some alternative methods where necessary and have been presented as well.

Chapter 7 contains the final conclusions and discussion of the thesis. The approach which was taken in the completion of this thesis as well as the challenges are discussed in more detail during this chapter.

Chapter 2

Theoretical Framework

This chapter serves to give an overview of the fundamental knowledge as a prerequisite to the design of a grid connected inverter that is capable of bidirectional power flow. This chapter takes emphasis on converter topologies used for three phase DC-AC conversion, while also introducing DC-DC converter topologies that can be used in a two stage topology. Which can be necessary for the sake of bidirectional operation and a stable DC-link while using a battery supply/load. However the main topic of this thesis is the GTI which will be presented with far more detail throughout this thesis, while the DC-DC converters will only be introduced to present a necessary background for the selection and operation. Furthermore various topics concerning the control, power waveform distortions and grid filtering methods are presented.

2.1 Converter systems

The converter in a power electronic system is one of the main components and the focus of this thesis. In this section some of the required standards when designing a grid tied converter will be presented. Three phase inverter topology and DC-DC converter topologies which will be later used to connect the battery storage system will be presented with their operational principle during this section.

2.1.1 grid-tied standards

Three phase GTI are power converters which convert DC to AC and feed it into an existing electrical grid system. These types of converters are often used to convert the

DC which is produced by renewable energy sources such as PV plants, wind turbines and batteries which can be converted to AC and become connected to the power grid. GTIs cannot typically be used in stand-alone applications where the utility power is unavailable [3]. Standards are required when integrating such converters into the electrical grid and must follow a list of requirements which are relevant to the performance, operation, testing and safety of the applications. Therefore when one seeks to design a grid connected converter system, it becomes necessary to undergo research on the rules and regulations for the requirements to be met. These standards however can be subject to variations based on where the system is intended to be applied. However for the most part these standards tend to be quite similar and mostly based around two international standards being the Institute of Electrical and Electronics Engineers (IEEE) and International Electrotechnical Commission (IEC). Additionally as many of the grid tied converter system applications utilize renewable power sources and/or Uninterruptible Power Supply (UPS) systems it can also be important to research the standards built specifically for them. Some of the most relevant standards which provides the requirements for the interconnection of distributed generation resources into the grid, are as follows:

- 1547-2018 - IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces [4].
- 61850 - IEC Communication networks and system for power utility automation [5].

These standards which have been presented are not specifically targeted towards any particular application, and serve more as a general requirements. Should the need of more specific applications be considered such as renewable energy sources there are different standards that must be researched and complied for overall approval. This master thesis has an emphasis on the control of the GTI system. which is why further standards which specify the limitations of the distortions to the system must also considered. Such as: 519-2014 - IEEE standard for Harmonics [6].

2.1.2 Active Front End Converter overview

The AFE converter is a power electronic converter which generally uses controllable switches such as the Insulated Gate Bipolar Transistor (IGBT) or Metal oxide semiconductor field effect transistor (MOSFET) for power conversion. An AFE is generally connected to the grid through a passive filter, which consists of an inductor or the combination of inductors and capacitors, as will be explained in further detail in a later

section. The application of an AFE converter can be anywhere from power conversion for grid-tied electrical applications, motor drives and power conditioning. AFE converters are becoming more and more popular as the power ratings are increasing while the costs of the power electronic converters and device components are decreasing. With the use of renewable sources on the rise such as photovoltaic systems and wind power, the added benefits of utilizing the AFE converters as part of the drive system becomes important considering the necessary control and requirements that must be upheld following the standards, generally IEEE or IEC standards . Furthermore this becomes driven by the continuous advancement in technological development of power electronics, semiconductor devices and advanced control methods. Some of the advantages of an AFE converter are as follows[7][8]:

- **Reduced harmonic distortion in the grid**
  The AFE converter utilizes controllable switches which allow for better control over the power conversion. Such as the capability of using complex modulation strategies which reduce the harmonic distortion. This advantage is quite apparent when compared to the simple thyristor and diode based converters which are more limited in their control and harmonic levels.

- **Bidirectional power flow**
  Perhaps the most advantageous feature which we acquire from the AFE topology is the bidirectional power flow capability, which is attained from the converter being capable of operating in all four quadrants of the V-I plane, as shown in figure 2.1 As depicted in the illustration one can see that there are two quadrants of operation wherein the converter acts as a rectifier and vice versa as an inverter.

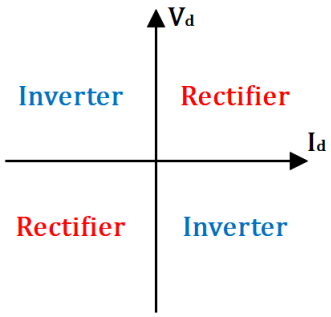

Figure 2.1: V-I plane with four quadrant operation of an AFE converter, adapted from [8].

- **Forced commutation**
  Due to the nature of controllable switches having the ability to switch on and off when it is required, we gain the advantage of utilizing forced Commutation independent of the line voltage. Forced Commutation is something which can

occur numerous times during a single period based on the operation, and allows for modulation of the drawn current by controlling the gate pulses relative to the reference signal. Furthermore by applying proper control strategies the dc voltage level of the converter can be controlled to be within a desirable boundary.

- **Reactive power control, Active power filter and enhanced grid stability** The reactive power flow of the converter is controllable and can be regulated to achieve and maintain desired Power Factor (PF) such as unity. As mentioned earlier in this section the AFE converter has the capability to regulate the grid current, which allows for the converter to be used for power conditioning purposes. This is achieved by harmonic cancellation with the use of active current injection into the non-fundamental frequency into the grid. By applying these capabilities we can contribute to an overall increased grid stability.

Generally the performance of a converter is determined by its means of efficiency, output Power Quality (PQ), harmonic distortion, the complexity of both the topology and control circuit in addition to the overall cost of implementation. AFE converters use controllable switches which allows for them to be switched on and off at any given time. With this advantage forced commutation becomes possible regardless of the line voltage, and the drawn current can be modulated based on the control of the gate pulses and reference signal. The quality of this output current will improve with the increase of commutations per cycle of the output voltage, but in turn will lead to energy loss due to the switching. Which is why selecting the proper type of controllable semiconductor switches is essential to reduce this loss, a simple rule of thumb is to use IGBTs when the switching frequency is less than 21 kHz and MOSFETs when its above if the application allows for it. This method of controlling the commutations (switching) to gain the desired current/voltage relative to a reference signal is known as Pulse Width Modulation (PWM), and is used in state of the art converters to enable the power transfer [9][10].

2.1.3 Three phase inverter

A three-phase two-level inverter topology is illustrated in figure 2.2, containing as the name implies three legs with two controllable switches on each leg. Power electronic converters schemes such as three phase inverters can produce a highly distorted current to the grid, this is considered undesirable and can cause numerous problems and reduce the efficiency of the overall system. To alleviate this issue filtering becomes necessary to reduce the distortions. Installing passive filters between the grid and the converter is a solution to filtering out harmonic distortions, this will be explained in further detail in a later section of this chapter. For the sake of simplicity line inductors have been added

to act as the filter in the illustration of the inverter. This simplicity comes with the disadvantage of being bulky and considerably costly, and may therefore not be considered suitable for some applications. Commonly inverters combine the passive filter with an active filtering technique such as PWM to acquire higher efficiency and less distortion.

It is important that any of the switches in the leg of the inverter is not switched on simultaneously, as this would lead to a short-circuit across the converter system. Which can cause irreparable damage to the converter itself. To avoid undefined states in the inverter and thereby the AC output line voltages, the switches of any leg must also not be switched off simultaneously. This could lead to voltages that depend upon the respective line current polarity. Commonly a preventative measure is taken by applying a blanking time which normally will occur during the switching operation of the converter [11]. Each of the legs in the inverter consists of two IGBTs that are connected in anti-parallel

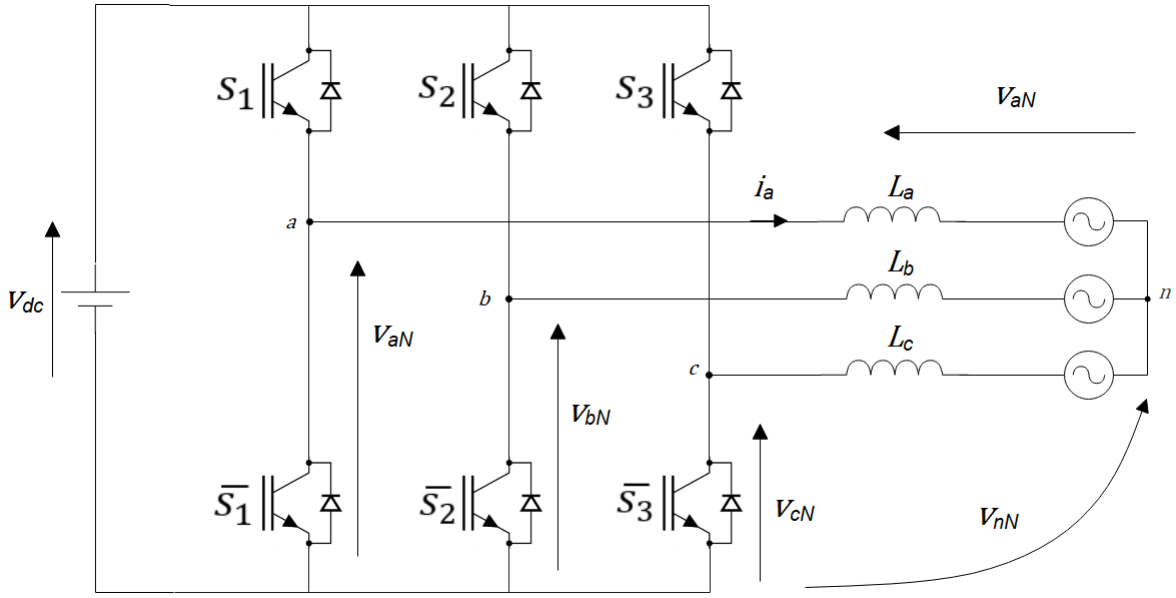

Figure 2.2: three phase voltage source inverter circuit [12].

with a flyback diode. For phase a the upper switch is named S_1 and the lower switch is named $\overline{S_1}$, and as illustrated the inverter consists of three legs where the rest of the switches has been named accordingly. The line inductors are represented as L_a, L_b and L_c, and for the sake of simplicity we can assume that they are all equal in size and may be used interchangeably with the term L in this section. A consideration can be made in the replacement of the IGBT switches to reduce losses if a considerably high switching frequency is used. For this thesis the switching frequencies will not exceed 20 kHz therefore the IGBTs can be considered to have good efficiency. The flyback diodes placed in the switches are installed to protect the IGBTs by providing the dc-link current a return path. Essentially solving the problem of high switching frequencies over an inductive load, which will produce voltage spikes due to the potential difference

between the switches and the inductor. This is further explained by the equation of the inductive load voltage $V_L = L\frac{di}{dt}$.

By applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) the voltage and current equations from the inverter illustration can be derived. As mentioned previously all the line inductors will be termed as L for the derived expressions shown.

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.1}$$

The switching state of the converters upper leg switches termed S_x (x=1,...,3) and their lower leg switches $\overline{S_x}$ (x=1,...,3) can be represented by the switching signals S_a, S_b and S_c are defined as followed:

$$S_a = \begin{cases} 1 & \text{if } S_1 \textbf{ on} \text{ and } \overline{S_1} \textbf{ off} \\ 0 & \text{if } S_1 \textbf{ off} \text{ and } \overline{S_1} \textbf{ on} \end{cases} \tag{2.2}$$

$$S_b = \begin{cases} 1 & \text{if } S_2 \textbf{ on} \text{ and } \overline{S_2} \textbf{ off} \\ 0 & \text{if } S_2 \textbf{ off} \text{ and } \overline{S_2} \textbf{ on} \end{cases} \tag{2.3}$$

$$S_c = \begin{cases} 1 & \text{if } S_3 \textbf{ on} \text{ and } \overline{S_3} \textbf{ off} \\ 0 & \text{if } S_3 \textbf{ off} \text{ and } \overline{S_3} \textbf{ on} \end{cases} \tag{2.4}$$

where the switching signals will define the output voltage value as shown in the following equation:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = V_{dc}\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{2.5}$$

where V_{dc} represent a DC voltage source. The phase-to-neutral voltages as shown in figure 2.2 are represented as v_{aN}, v_{bN}, v_{cN}. The three phase voltages can be defined using vectorial representation with a unitary vector expressed as $\mathbf{a} = e^{\frac{j2\pi}{3}} = \frac{1}{2} + j\frac{\sqrt{3}}{2}$. Where $\mathbf{a}$ represents the 120^o phase displacement between the phases. The instantaneous voltage space vector written in terms of inverter output voltages can be expressed as:

$$\mathbf{v} = \frac{2}{3}(v_{aN} + \mathbf{a}v_{bN} + \mathbf{a}^2 v_{cN}) \tag{2.6}$$

This way the switching state (S_a, S_b, S_c) = (0, 0, 0) will generate the voltage vector V_0

which can be expressed as:

$$\mathbf{V}_0 = \frac{2}{3}(0 + \mathbf{a}0 + \mathbf{a}^2 0) = 0 \tag{2.7}$$

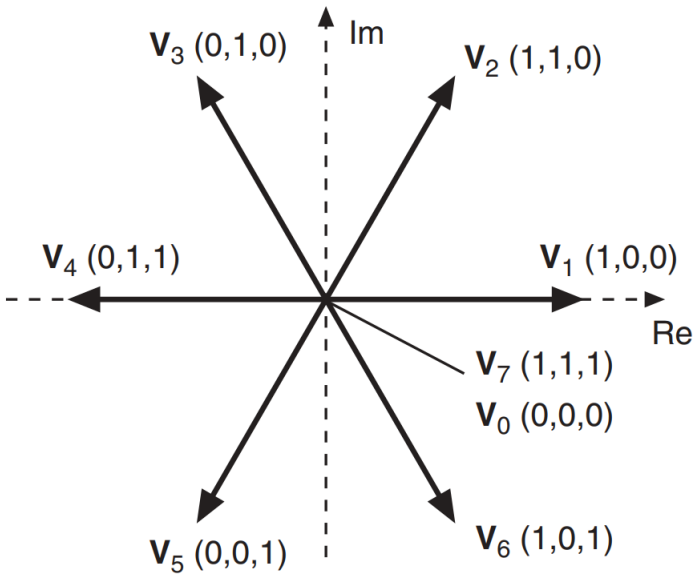

Figure 2.3: Voltage vectors in the complex plane [12]

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Based on the combinations of the gating signals (S_a, S_b, S_c) we can obtain a total of 8 switching states and their respective voltage vectors, as shown in Table 2.1. However considering that $\mathbf{V_0} = \mathbf{V_7}$ as shown in 2.3, only 7 different voltage vectors in the complex plane are obtained.

S_a	S_b	S_c	Voltage vector $\mathbf{V}$
0	0	0	$\mathbf{V}_0 = 0$
1	0	0	$\mathbf{V}_1 = \frac{2}{3}V_{dc}$
1	1	0	$\mathbf{V}_2 = \frac{1}{3}V_{dc} + j\frac{\sqrt{(3)}}{3}V_{dc}$
0	1	0	$\mathbf{V}_3 = -\frac{1}{3}V_{dc} + j\frac{\sqrt{(3)}}{3}V_{dc}$
0	1	1	$\mathbf{V}_4 = -\frac{2}{3}V_{dc}$
0	0	1	$\mathbf{V}_5 = -\frac{1}{3}V_{dc} - j\frac{\sqrt{(3)}}{3}V_{dc}$
1	0	1	$\mathbf{V}_6 = \frac{1}{3}V_{dc} - j\frac{\sqrt{(3)}}{3}V_{dc}$
1	1	1	$\mathbf{V}_7 = 0$

Table 2.1: Switching states (S_a, S_b, S_c) and voltage vectors

It should be noted that for the sake of simplicity a simple model has been used. A more complex model of the converter might for instance include dead time, IGBT saturation voltage, diode forward voltage drop. However the emphasis of this section is to explain the overall operation and overview of the inverter model with simplicity.

2.1.4 DC-DC converter topologies

A DC-DC converter can be a necessary converter to have between the battery system and the inverter to ensure a stable voltage and current is provided, which is a key requirement to be able to control the bidirectional inverter. Traditionally, it is not common practise to depend on battery cells in series to increase the voltage as this comes with several disadvantages such as: large economic cost and a large space is often needed. There are however many different DC-DC topologies which can be selected based on the application. The power conversion system is responsible for the power flow through the grid and Battery Energy Storage System (BESS). The manner in which the BESS and the grid is interconnected depends on the selected design, which is between a single stage topology or a two stage topology. Where are single stage topology will often contain a grid tied bidirectional DC-AC converter directly connected to the BESS. While a two stage topology contains a DC-DC converter between the BESS and the grid tied converter. The proposed method of this thesis will utilize a two stage topology. Thus a DC-DC converter becomes a necessity. The single and two stage topology will be explained with further detail in a later section of this chapter. in this section the Buck and Boost DC-DC converter topologies will be presented. The converters topologies will be introduced individually to explain their function and structure, and a combination of these two converters will be presented in a later chapter. The converter models that are introduced in this section will not be explained in great detail, as these converters are well established in literature such as in the following sources which have been used: [9; 13; 14; 15].

Buck converter

Buck converters often termed as step-down are simple and efficient converters, and as the name states it's primary use is to convert an input DC voltage to a lesser output voltage. One of the advantages of the buck converter is that it can provide a continuous output current. However a large capacitor is required in order to smoothen the discontinuous input current. A buck converter and its operation has been illustrated in figure 2.4. The converter contains a diode and a controllable switch where the gate signal has been

termed q, additionally the converter consists of passive components such as an inductor and a capacitor with its internal resistance. During the controllable switches off time the diode will allow the inductor current to freewheel across as depicted in figure 2.4 when the gate signal q is equal to zero. The converter has the ability to operate in both Continuous conduction mode (CCM) or in discontinuous conduction mode (DCM), which depends on the inductor waveform. A method of controlling the operation of the Buck converter and some simple calculations will be presented as follows:

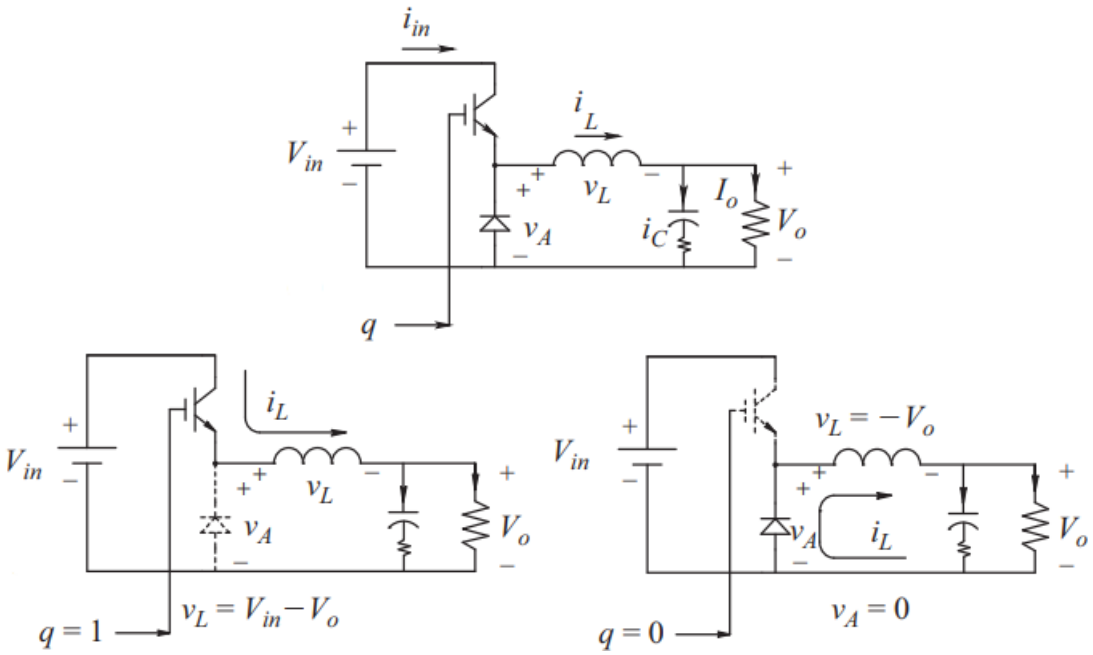


Figure 2.4: Buck converter topology, and switching state.[14]

- **Operation**

  When the controllable switch is on, the circuit will be able to provide the output load current and allow for the DC input to charge the inductor. Generally the converter can be controlled as shown in the waveform illustration where the inductor will be able to charge until the output voltage reaches the desired reference voltage. Once this is obtained the controller will turn off the switch allowing for the output voltage to remain close to the reference voltage. Furthermore due to the switch being turned off the circuit will no longer be charging the inductor, this will lead to the inductor changing its voltage polarity allowing for the current to flow in the same direction through the diode. The discharging of the inductor will continue until the output voltage reaches below the reference voltage, in which case the controller will turn on the switch to compensate for the output voltage drop and continue the operating cycle [16].

- **Duty cycle calculation**

The controllable switch is commonly controlled by using a PWM where its on and off state are determined by the switching frequency $f_{sw} = 1/T$ and the duty cycle D can be derived as:

$$D = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}} = \frac{V_o}{V_{in}} \tag{2.8}$$

where t_{on} is the time interval that the controllable switch is in its on-state, likewise the t_{off} represents the time interval that the switch is not conducting (off-state). The period is termed T and the switching frequency f_{sw}.

- **Buck converter Calculations**

The inductor current waveform at the boundary between the CCM and the CDM are illustrated in Figure 2.5. Where the inductor current waveform can be described by the following equation:

$$i_L = \frac{V_{in} - V_o}{L} t, \quad \text{for} \quad 0 < t \leq DT \tag{2.9}$$

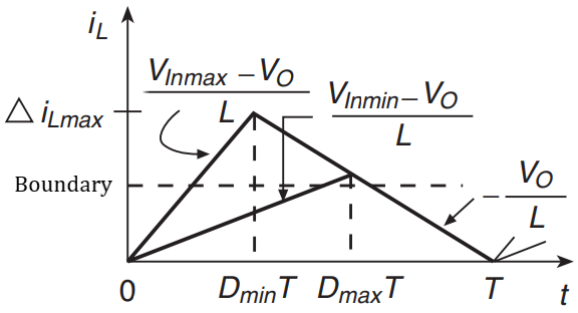


Figure 2.5: Inductor current at CCM/DCM boundary [15].

Furthermore we can derive the peak-peak inductor current often termed as ripple current $\Delta i_{L,p-p}$ as follows:

$$\Delta i_{L,p-p} = \frac{(V_{in} - V_0)DT}{L} = \frac{V_0(1-D)T}{L} \tag{2.10}$$

The size of the inductor component can be determined by calculating the minimum inductance required to maintain the CCM operation for the duty cycle range (D_{min} and D_{max}) as shown in the following equation:

$$L_{min} = \frac{V_0(1 - D_{min})}{\Delta i_{L,max} f_{sw}} \tag{2.11}$$

from equation 2.11 it can be observed that by increasing switching frequency f_{sw} we can reduce the minimum inductance required. For the sake of simplicity all

resistances are neglected and the minimum required capacitor size can be calculated by the following equation:

$$C_{min} = \frac{\Delta i_L}{8 f_{sw} \Delta v} = \frac{V_0(1 - D_{min})}{8 L f_{sw}^2 \Delta v} \tag{2.12}$$

where the voltage ripple is termed Δv, The calculation can be more complex if the resistances are included, which can be further detailed in the following source [17].

Boost converter

The boost converters often termed as step-up converters primary function is essentially the opposite of a buck converter, by providing an output voltage which is greater than the input voltage. Figure 2.6 provides an illustration of a Boost converter as well as its operation.

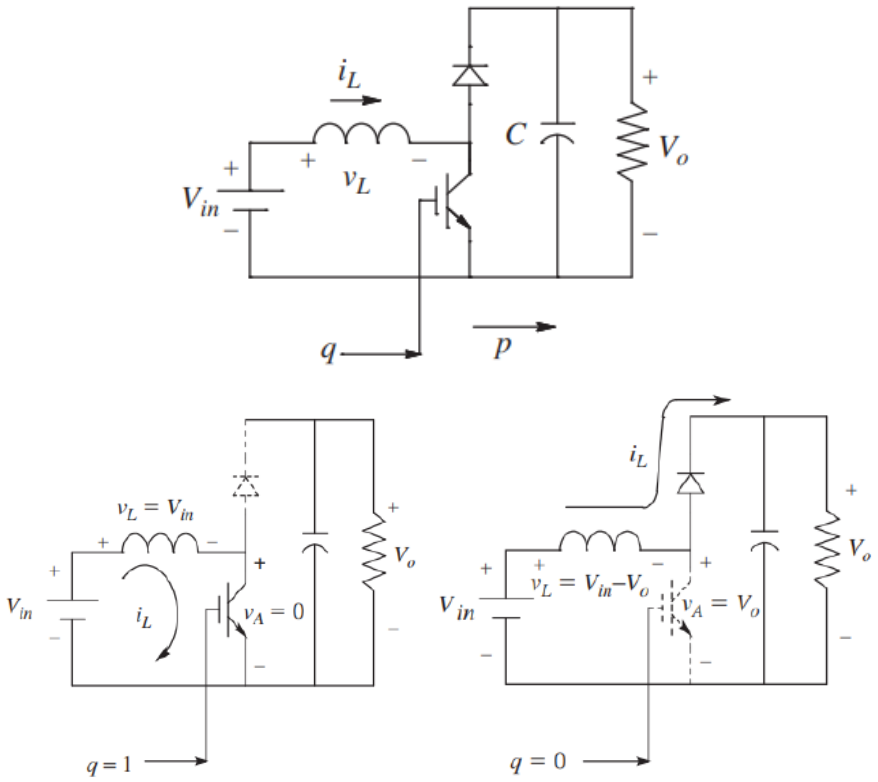


Figure 2.6: Boost converter topology and switching state [14].

The converter is supplied by a continuous input current and provides a discontinuous output current, with a better dynamic response. A disadvantage of the converter is the requirement of a high input side current, which means that it is not a suitable topology for all types of applications. Such as in the case of a PV system where the high input side current may not be possible to maintain at all times. Furthermore the converter requires

a larger inductance compared to that of a buck converter. The boost converter does however have the advantage of a cheaper implementation cost than a buck converter due to lower value input capacitor being required. Similar to the Buck converter topology the reverse current in the Boost converter is prevented by using a freewheeling diode, shown clearly in Figure 2.6.

- **Operation**

  By turning on the controllable switch ($q = 1$), the diode will be reverse biased and the inductor voltage V_L will be equal to the input voltage V_{in}, as is shown in figure 2.6. While also allowing the inductor current i_L to increase linearly at a rate of V_{in}/L, increasing the energy in the inductor. When the controllable switch is turned off ($q = 0$), the inductor current will be forced to flow through the forward biased diode. Hence leading to the stored energy of the inductor to be transferred to the filter capacitor C and the output load. At this time the inductor voltage will be equal to $V_L = V_{in} - V_0$ with the inductor current i_L decreasing at a rate of $(V_{in} - V_0)/L$. The operation of the Boost converter, while the switch is on and off has been illustrated in the previously mentioned figure 2.6.

- **Input/output voltage ratio**

  It is common for the controllable switch to be controlled using a PWM where its on and off state are determined by the switching frequency, similar to what has been presented previously with the buck converter. The relationship between the input and output voltage can be derived by using either the waveform of V_L or V_A as is sown in figure 2.7. By using the inductor voltage waveform in steady state we can obtain the following equation:

$$V_{in}(DT_s) = (V_0 - V_{in})(1 - D)T_s \tag{2.13}$$

  Which allows for the input/output voltage ratio to be expressed as:

$$\frac{V_0}{V_{in}} = \frac{1}{1 - D} \qquad (V_0 > V_{in}) \tag{2.14}$$

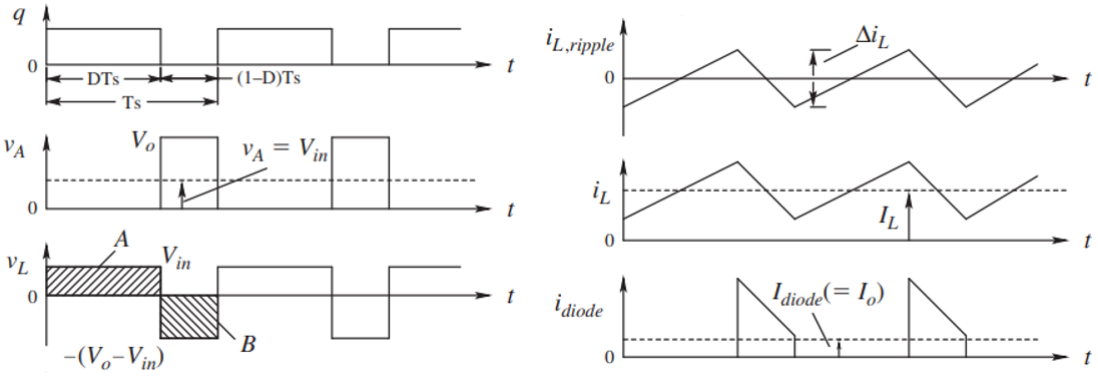


Figure 2.7: Boost converter waveforms [14].

- **Inductor size calculation**

  Traditionally the inductor size is determined through the inductor current ripple. By calculating the average inductor current I_L using equation 2.15, where I_o represents the output current. It is then suggested that the peak-peak ripple current termed $\Delta i_{L,p-p}$ should be around 20-40% of I_L [18].

$$I_L = \frac{V_0 I_0}{V_{in}} \tag{2.15}$$

  The inductor current waveform is built up by the average value, which is dependent on the output load and the ripple component:

$$i_L(t) = I_L + i_{L,ripple}(t) \tag{2.16}$$

  where the inductor ripple current termed $i_{L,ripple}$ is also dependent on the inductor voltage v_L. This is shown clearly in figure 2.7 where $i_{L,ripple}$ increases when v_L is positive and decreases when v_L is negative, finally resulting in an average of zero. we can then determine the inductor size by calculating the peak-peak ripple as shown in the following equation:

$$\Delta i_{L,p-p} = \frac{1}{L}\underbrace{V_{in}(DT)}_{AreaA} = \frac{1}{L}\underbrace{(V_0 - V_{in})(1-D)T_s}_{AreaB} \tag{2.17}$$

2.2 Controllers

There are various types of controllers which can be used for the purpose of controlling a converter or for the sake of grid angle extraction. However some of the most common types for the sake of converter control include the hysteresis controller and the Proportional Integral (PI) controller, which will be presented in this section along with

a method of tuning and optimizing a PI controller through Modulus Optimum (MO) criteria.

2.2.1 Hysteresis controller

The hysteresis controller theory has been sourced from [9]. Hysteresis control is often termed as tolerance band control and through out this thesis will be used interchangeably. This form of controller is commonly used as a current regulator. The tolerance band current control method is illustrated in figure 2.8 using one of the legs of an arbitrary inverter for a sinusoidal reference current i_A^*, where the real phase current i_A is compared to the tolerance band around the reference current to the phase. As shown in the figure V_d represents the DC voltage and the switches on the inverter leg are termed T_{A+} for the upper leg and T_{A-} for the lower leg.

Essentially the operational principle of the controller consists of an upper and lower tolerance band which dictate when the switches on the converter can be turned on and off. For instance when the real current value i_A increases above the upper level of the tolerance band, T_{A-} is turned on, conversely T_{A+} is turned off. Furthermore the same logic is implied for when the real current goes below the lower level of the tolerance band, with the opposite switching. The switching frequency is thereby determined by the speed of which the current changes from the the upper limit to the lower limit of the tolerance band and vice versa. However despite the simplicity of the hysteresis control method, a notable drawback of this controller is that the switching frequency changes as a function of the current waveform. For this specific reason, constant switching frequency controllers are often used as an alternative.

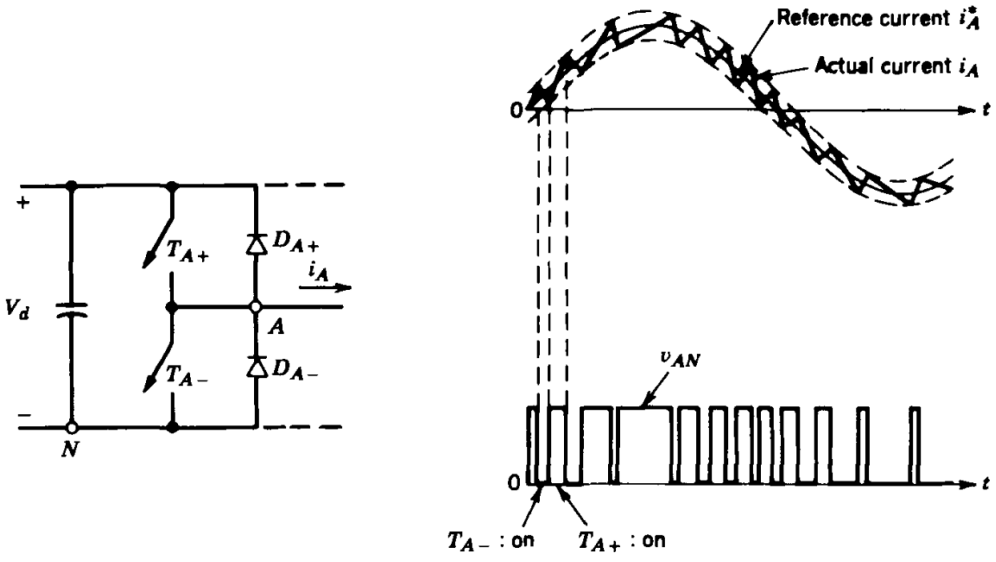


Figure 2.8: Hysteresis current control [9].

2.2.2 Proportional Integral Controller (PI)

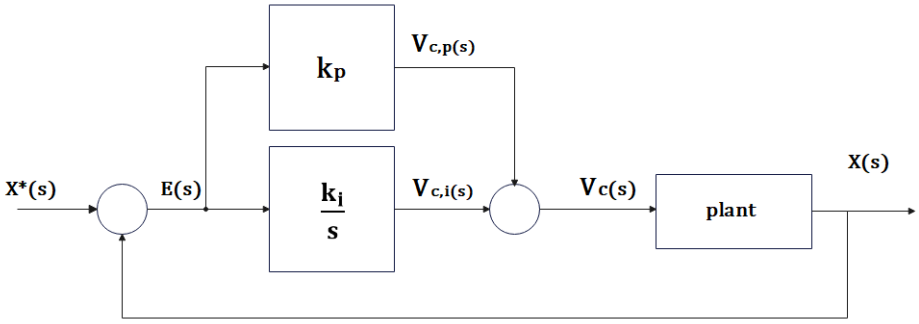


Figure 2.9: PI control loop in the frequency domain.

The Proportional Integral (PI) controller is a well established controller which is applied in a wide range of applications [19]. This type of controller is built up by two separate controller parts the proportional and the integral, as is illustrated in Figure 2.9. The Proportional (P) controller is the most basic type, which consists of a simple proportional gain, k_p. The proportional controller produces an output which can be expressed as:

$$V_{c,p}(s) = k_p E(s) \tag{2.18}$$

Where the difference between the reference input and the measured output is considered the input error of the controller E(s)=X*(s) - X(s). The integral part of the controller takes the error input signal and removes the steady state control offsets by ramping the output up or down depending on the amplitude and duration of the input error signal. However the integral constant which controls the ramp rate must be tuned properly or there becomes a risk of oscillations [20][21]. As illustrated in 2.9 the integral controllers output is proportional to the integral of the error E(s), and can be expressed in the Laplace domain as:

$$V_{c,i}(s) = \frac{k_i}{s} E(s) \tag{2.19}$$

where the integral controller gain is termed k_i. Such controllers have a slow response time due the actions being proportional to the time integral of the error. However the steady-state error will go towards zero for a step change in input because the integrator will continue until there is no error (ie, error equal to zero). The Transfer function (TF) of a PI controller can be expressed as:

$$PI(s) = \frac{V_c(s)}{E(s)} = k_p + \frac{k_i}{s} = \frac{k_p s + k_i}{s} = \frac{k_p \left(s + \frac{k_i}{k_p}\right)}{s} \tag{2.20}$$

Or alternatively the TF with the integral time constant $T_i = \frac{k_p}{k_i}$, can be expressed as:

$$PI(s) = k_p \left[\frac{1 + T_i s}{T_i s} \right] \tag{2.21}$$

2.2.3 Controller tuning and optimizations

There are various methods which can be used for optimizing PI controllers, in this section two popular tuning methods known as the MO and Symmetrical Optimum (SO) are introduced. These methods are based on a similar idea of finding a controller which makes the frequency response from set-point to the plant output as close to unity as possible [22]. Both optimization techniques have been proven to be successful in the tuning of PI controllers and have been widely implemented in grid tied converters. The parameter of PI controllers as has been previously explained consist of a proportional gain constant k_p and the integral time constant Ti.

Modulus optimum

MO, also known as absolute value optimum criterion as has been explained is a methodology of tuning a PI controller based on keeping the magnitude value of the systems closed loop TF $G_{CL}(s)$ equal to unity, while maintaining as wide of a frequency range as possible [22]. For instance if one has an arbitrary controller TF known as $G(s)$, we would then like to tune the controller in way which allows $G(0) = 1$ and for $\frac{d^n|G(j\omega)|}{d\omega^n} = 0$ at ω=0 for as long as possible [23].

For low order controlled plants without time delay, the MO is generally used in the conventional analog controller tuning. If the controlled system has one dominant time constant in addition to other minor time constants, the PI controller can be considered suitable for optimization by using the MO criteria. When the conditions are met, the standard form of the control systems TF for the MO is obtained by cancelling the largest time constant. This is done while keeping the closed loop gain larger than unity for as high frequencies as possible [24]. If we assume the TF of a plant system expressed as:

$$L(s) = \frac{1}{(1 + T_a s)(1 + \tau s)Rp} \tag{2.22}$$

where T_a represents a large time constant, while τ represents a small time constant or the sum of multiple smaller time constants, in addition to fulfilling the following condition $T_a >> \tau$. With reference to the PI-controllers TF shown in 2.21, we can derive the

system open loop and closed loop TF ($G_{OL}(s)$, $G_{CL}(s)$), as:

$$G_{OL}(s) = k_p \left[\frac{1 + T_i s}{T_i s}\right] \frac{1}{(1 + T_a s)(1 + \tau s) R_p} \tag{2.23}$$

$$G_{CL}(s) = \frac{k_p(1 + T_i s)}{k_p(1 + T_i s) + \frac{T_i}{R_p} s(1 + T_a s)(1 + \tau s)} \tag{2.24}$$

Zero pole cancellation can be applied for the dominating pole of the system , giving the PI gain parameters k_p and T_i by MO tuning criteria as follows:

$$T_i = \tau \tag{2.25}$$

$$k_p = \frac{R_p \tau}{2T_a} \tag{2.26}$$

with the tuning criteria given from the above equations (2.25, 2.26), the open loop and closed loop TFs of the systems control loop can be expressed as:

$$G_{c,OL}(s) = \frac{1}{2T_a} \cdot \frac{1}{s(1 + T_a s)} \tag{2.27}$$

$$G_{c,CL}(s) = \frac{1}{2T_a^2 s^2 + 2T_a s + 1} = \frac{\frac{1}{2T_a^2}}{s^2 + \frac{1}{Ta} s + \frac{1}{2T_a^2}} \tag{2.28}$$

The resulting closed loop TF from equation 2.28, resembles the form of a generic second order TF as expressed in 2.29. Given the similarity of these TFs we can determine the natural frequency and the damping factor of the closed loop system. Which has been expressed in equation 2.30 and 2.31.

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.29}$$

$$\omega_n = \frac{1}{\sqrt{2} T_a} \tag{2.30}$$

$$\zeta = \frac{1}{\sqrt{2}} \tag{2.31}$$

Due to the simplification of the system by using pole cancellation, and optimizing the absolute value to unity. The systems resulting response will always correspond to the given values of ζ and ω_n as shown in the above equations. However the crossover frequency can be tuned to obtain the desired value by regulating the proportional gain constant k_p. It is common to select the crossover frequency to be one or two orders smaller than the switching frequency of the system, thereby one can avoid the interference from the switching noise.

The MO criteria proves to be a suitable tuning technique, when the controlled system has one dominant time constant along with other minor time constants. However this is not the case when one of the poles is located near the origin or at the origin itself, due to the pole shift not causing any significant change. In which case an alternative controller tuning technique could be used such as the SO criterion which will not be used in this thesis [24].

2.3 Power Waveform Distortions

Power systems quality monitoring is considered to be common practice for utilities, as there has been an increased amount of requirements on the control and performance of such systems. The PQ refers to the amount of variation in voltage, current, harmonics, and frequency on the power system. The distortion in power distribution systems 50 Hz sinusoidal waveform, is referred to as the term "Waveform distortions". These waveform distortions can occur through various means, which can be separated into select groups such as: Harmonics, Noise and Impulsive transients [25].

Ideally we would like the converter systems current to be free from distortion and be completely sinusoidal, however this is not possible in a practical system due to the distortion in the converters output voltages occurring from the dead time and non-ideal characteristics of the power switches or due to the distorted grid voltage [26].

Harmonic current distortions in Power electronic systems in addition to the voltage waveform distortions it can lead to malfunctioning of components due to over-voltages due to resonance conditions. And has the capability of undesirable effects such as increased heating to the cables, loads and components of the circuits as well as additional problems to the power electronic system [9].

A distorted waveform will often contain a large amount of different harmonic distortions, and therefore when describing the harmonic content within the waveform it is common to use the term Total Harmonic Distortion (THD). A distorted waveform can be split into its fundamental component and its harmonic component, where the THD describes the percentage ratio of the Root Mean Squared (RMS) amplitude of the fundamental frequency compared to a set of harmonic frequencies. We are able to calculate these components by means of Fourier analysis [8].

A repeating waveform f(t) which satisfies the Dirichlet conditions is able to be expressed

with the use of Fourier expansion as shown.

$$f(t) = a_o + \sum_{h=1}^{\infty}(a_h \cdot cos(h\omega t) + b_h \cdot sin(h\omega t)) \tag{2.32}$$

In which case the coefficients a_o, a_h and b_h can be defined by the following expressions:

$$a_o = \frac{1}{T}\int_{-T/2}^{T/2} f(t)dt \tag{2.33}$$

$$a_h = \frac{2}{T}\int_{-T/2}^{T/2} f(t) \cdot cos(h\omega t)dt \tag{2.34}$$

$$b_h = \frac{2}{T}\int_{-T/2}^{T/2} f(t) \cdot sin(h\omega t)dt \tag{2.35}$$

each frequency component is represented in term of its RMS value, can be calculated as:

$$F_{RMS} = \sqrt{a_o^2 + \sum_{h=1}^{\infty}\frac{a_h^2 + b_h^2}{2}} \tag{2.36}$$

However it is important to note that the DC component a_o of f(t) is often zero, simplifying the equation to:

$$F_{RMS} = \sqrt{\sum_{h=1}^{\infty}\frac{a_h^2 + b_h^2}{2}} \tag{2.37}$$

using the above equation we can derive an expression for the THD, where $F_{1,RMS}$ represents the fundamental signal as:

$$THD = \sqrt{\frac{F_{RMS}^2 - F_{1,RMS}^2}{F_{1,RMS}^2}} \tag{2.38}$$

Furthermore the THD can be derived in terms of the current, where I_1 is the line frequency component of the drawn current from a load and I_h is the h harmonic current injected. this can be expressed as [9]:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{2.39}$$

2.4 Filter Methods

As previously mentioned the effects of harmonic distortion can be quite substantial, which is why it is common to develop a filter connected between the grid and the con-

verter too attenuate the harmonics. This method of acquiring a stable region of operation variates depending on the application, bandwidth and cost with several different methods of filtering to select from. One can generally divide the type of attenuation into two methods passive- and active damping. Both methods are capable of compensating the harmonic current precision and damp the switching ripples sufficiently. the passive and active damping methods which will be presented have been based on [27].

The state of the art methods of filtering today mainly contain three filter topology variations: L, LC, and LCL filter variations as is illustrated in 2.10. The size of the components are determined by the topology selection. Considering the LCL filter topology the filter size is determined by the inverter output current, switching frequency and the system bandwidth. The LCL filter design is considered to be the most preferred method for power conditioners when taking the advantages into consideration. Such as the lowered requirement of inductance and capacitance which reduces the bulkiness and cost. However with this topology the resonant peaks that are developed during the operation can be a challenge to attenuate, and may need passive or active damping depending on the operational requirements and chosen component values.

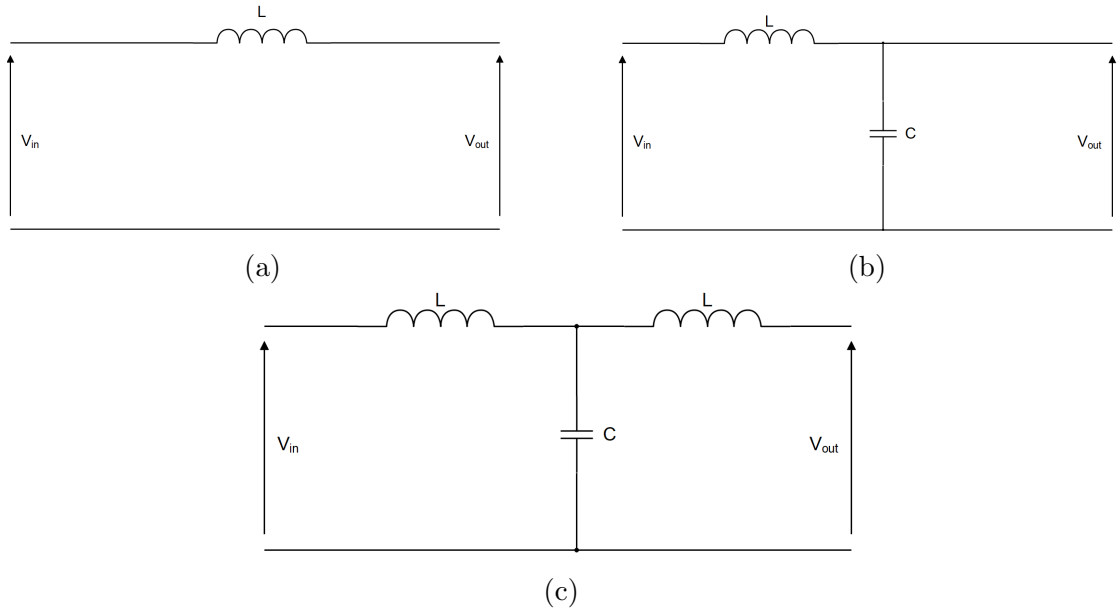


Figure 2.10: Three different types of passive filters, a) L filter, b) LC filter , c) LCL filter

The passive damping method consists of only passive elements such as resistors inductors and capacitors, which simplifies the complexity of design and can be more cost efficient when compared to the active damping counterpart. The advantages of having a simple control algorithm, cause the passive method of filtering to have a better bandwidth and dynamic performance. This advantage is one of the reasons that it can be the preferred choice given the right use of application. However the losses of the damping

resistance can be considerable to the point that is unacceptable when applied in a high-power system. This disadvantage can be mitigated given the right improvements of the filter topology, which can possibly reduce the power losses of the damping resistors to the point that it can be comparable with active methods. While simultaneously keep the advantages that is acquired by the passive methods.

The active damping method can be more expensive due to the requirement of more sensors and will cause an increase of the algorithm complexity in turn. While the passive methods have a large bandwidth, this is not the case for the active methods which have a smaller bandwidth and poor performance of dynamic response and noise immunity. Unlike the passive methods where it is common to use a physical resistor to damp the system, the active damping generally uses a control algorithm. These control methods come in many variations for instance with a LCL filter topology some of the commonly used control methods include complex modulation strategies such as Space Vector Pulse Width Modulation (SVPWM).

2.5 Battery Energy Storage Systems - BESS

In modern day BESS can have monitoring and control systems as well as power conversion systems. Batteries have the capability of storing energy chemically, with the advantages of having a dynamic response time, high energy efficiency and can generally be easily transported with out relying on any specific geographical restrictions. At least compared to other storage devices such as water storage, which can be limited by geographical restrictions, for instance water reservoirs.

BESS usually contain non-linear characteristics, thus leading to some challenges in its proper representation when one intends to perform tests by simulating. One model design method used to represent a battery storage system , consists of a circuit with an internal resistance in series with an ideal voltage source. Which is considered to be the simplest and the most commonly used model of a battery, this has been illustrated in figure 2.11.

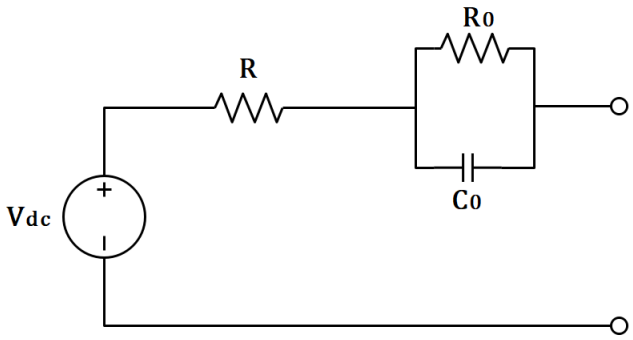


Figure 2.11: Simple Thevenin battery model [30].

However often there is a need for a more realistic model which takes the non-linear parameters into consideration. With such models the characteristics of the battery's internal resistance, self-discharge resistance, overcharge resistance and adding a separation between the charging and discharging processes. One of such models known as a third order battery model has been illustrated in figure 2.12. In the illustrated third order model the main branch which contains V_{dc}, R_1, C_1 and R_2 components is used to approximate the battery charge/discharge dynamics. While the parasitic branch which contains R_p and V_p represents the self-discharge, furthermore a resistor R_0 is placed in order to approximate the overcharge resistance. As is clearly displayed in the illustrated figure of the third order battery model the resistive elements are non-linear and current dependent. Both the simplistic model and the more realistic model are explained in further detail from their source [30].

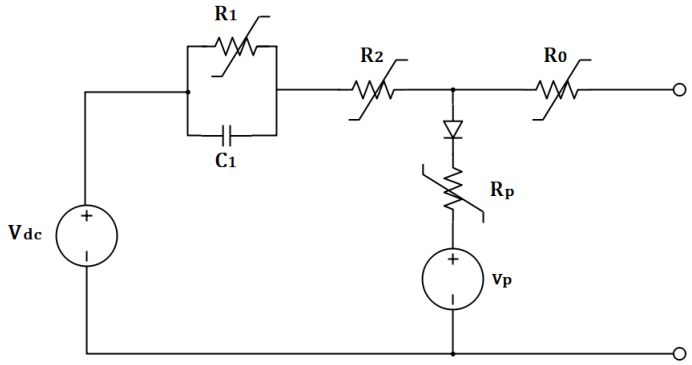


Figure 2.12: Third order battery model [30].

In order for the power to flow across the BESS and the grid, a power conversion system must be utilized. There are generally two variations of the topologies used for such systems, which are commonly known as single stage and two stage topologies as illustrated in figure 2.13a and 2.13b respectively. The single stage design topology connected to a BESS consists of a bidirectional DC-AC converter which interconnects the battery and the grid directly. While the two stage topology has an additional DC-DC converter

between the DC-AC converter and the battery supply/load. Using such power conversion systems a dc-link capacitor is often placed in order to stabilize the dc-link voltage. There are challenges which come depending on the selected topology. The single stage is considered a more simple design, however the two stage topology is considered to be superior in efficiency following the results of numerous studies such as [28]. The usual design topology of these systems have been illustrated and can be compared as mentioned in figure 2.13. As stated both of these topology variations have full bidirectional power flow capabilities, although each of the topologies come with their own advantages and disadvantages [29]. For this thesis the two stage topology will be used in the later chapters due to the overall advantages such as the capability of both boosting and bucking the voltage provided by the BESS.

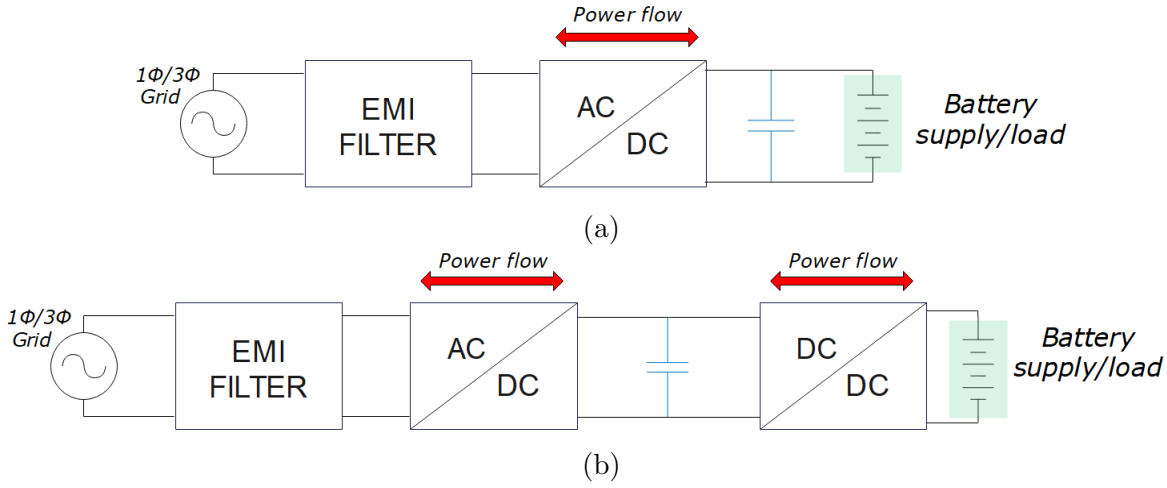


Figure 2.13: a)Single stage BESS topology. b)two stage BESS topology. [29].

Chapter 3

Control structure and strategies of grid tied converter

When converting DC to AC power and vice versa, it is essential that the three phase AC voltage and current is controlled. Where the main objective is to control the voltage and current components magnitude, frequency, phase angle and the direction of the power flow. Each of the respective voltage and current components, are the determining factors of the total amount of power delivered.

This chapter aims to present the control structures, components and strategies which are used in the GTI system. The chapter introduces coordinate transformations, modulation strategies, Phase Locked Loop control and the Voltage Oriented Control (VOC) strategy with an overview of the entire control structure. Furthermore an alternative control method by using the Direct Power Control (DPC) method will also be described. The following sections of this chapter will be using an inverter model with a LCL-filter when describing the method of control unless stated otherwise. This is the intended topology for simulation and prototyping of the system.

3.1 Clark and Park transform

In VOC and DPC, we use coordinate transformations to turn the measured AC values into quantities that can be more manageable and simpler to regulate by the converter control loops. Once these values have been transformed and regulated by the control loops we can then inverse transform these quantities into their corresponding AC-values. For this implementation we utilize two types of transformations to acquire our desired quantities the Clark and Park transform. An illustration has been provided to showcase

a graphical representation of the three phase reference frames, in figure 3.1. These transformations have their variations based on what invariance one would like, more specifically there is the magnitude invariant and the power invariant[8][31].

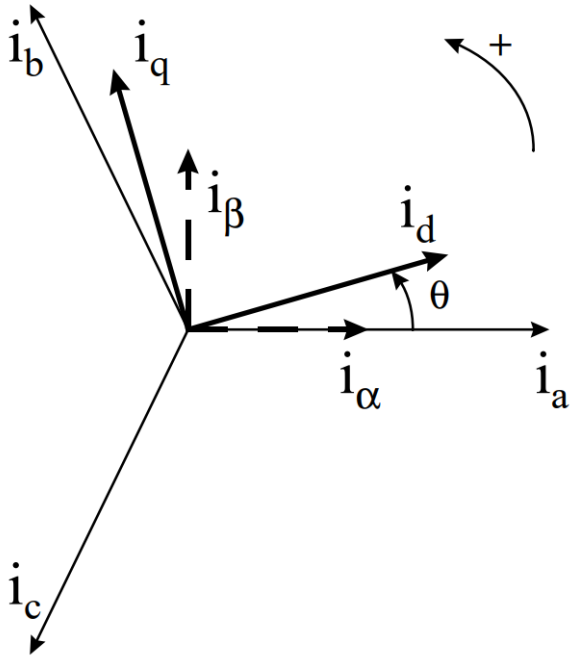


Figure 3.1: the stationary reference frame ($\alpha\beta$) and synchronous reference frame (dq) with its relation to the three phase (abc) reference frame [32].

3.1.1 Clark transformation

The Clarke transformation is used to transform the components in a three phase system (in abc frame) into two components in an orthogonal stationary frame ($\alpha\beta$) which is also referred to as the $\alpha\beta$ coordinate system [8][31]. By assuming symmetrical balanced three phase AC, the ideal voltage and current values termed as $\mathbf{V}_{abc}$ and $\mathbf{I}_{abc}$ (120°phase shift) are derived as:

$$\mathbf{V}_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V \cdot sin(wt) \\ V \cdot sin(wt - \frac{2 \cdot \pi}{3}) \\ V \cdot sin(wt + \frac{2 \cdot \pi}{3}) \end{bmatrix} \tag{3.1}$$

$$\mathbf{I}_{abc} = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} I \cdot sin(wt) \\ I \cdot sin(wt - \frac{2 \cdot \pi}{3}) \\ I \cdot sin(wt + \frac{2 \cdot \pi}{3}) \end{bmatrix} \tag{3.2}$$

For the transformation equations the current values will be selected to showcase the transformation. We use the Clark transformation to represent the corresponding orthog-

onal components I_α and I_β as shown:

$$\mathbf{I}_{\alpha\beta 0} = \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \mathbf{T}_c \mathbf{I}_{abc} = \frac{2}{3} \underbrace{\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}}_{T_c} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.3}$$

As shown we acquire three components by using this transformation matrix, however the zero components value will always remain 0 with the assumption of a symmetrical balanced sinusoidal three phase signal. Therefore we choose to neglect the zero component and focus more on the α and β components. This variant of the Clark transformation is known as the magnitude invariant, in which the magnitude of the three phase system vector is the same as the two phase system vector:

$$|I_a(t)| = |I_\alpha(t)| \tag{3.4}$$

This method can be a good choice for motor drive designers due to its intuitive nature of having the measured voltage magnitude be the same in both reference frames, which can be advantageous for control. Likewise the power invariant may be more suitable for DPC applications, as the power can be estimated using the $\alpha\beta$ coordinate. The magnitude invariant inverse Clark transformation can be expressed as:

$$\mathbf{I}_{abc} = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \mathbf{T}_{c,inv} \mathbf{I}_{\alpha\beta 0} = \underbrace{\begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}}_{T_{c,inv}} \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} \tag{3.5}$$

However in order to perform calculations on the active and reactive power whilst working in the $\alpha\beta$ domain one would need to utilize another form of the Clark transformation to accommodate for this. The currently shown Clarke transformation matrix does not contain the necessary criteria to allow for these calculations due to the matrix being non-unitary. Which implies that this variation of the Clark transformation does not fulfil the following criteria: $\mathbf{T}^*\mathbf{T}=\mathbf{T}\mathbf{T}^*$. The power invariant Clark transformation can be expressed as:

$$\mathbf{I}_{\alpha\beta 0} = \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \mathbf{T}_c \mathbf{I}_{abc} = \sqrt{\frac{2}{3}} \underbrace{\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{T_c} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.6}$$

As mentioned by using the power invariant equation we can calculate and determine an estimate of the instantaneous active power (P) and reactive power (Q) by using the voltage and current quantities in the $\alpha\beta$ coordinate as shown:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \tag{3.7}$$

The power invariant transformation shown in equation 3.6, can then be inverted by applying the inverse Clark transformation as shown:[33]

$$\mathbf{I}_{abc} = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \mathbf{T}_{c,inv}\mathbf{I}_{\alpha\beta 0} = \sqrt{\frac{2}{3}} \underbrace{\begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}}_{T_{c,inv}} \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} \tag{3.8}$$

3.1.2 Park transformation

The Park transformation is used to transform the two components which are represented in an orthogonal stationary frame ($\alpha\beta$) into a orthogonal rotating reference frame (dq) with also two components. Which in essence simplifies the two ac components which rotate with a fixed frequency that are represented by the orthogonal $\alpha\beta$ components, to appear as two DC quantities instead [8][31]. By using the $\alpha\beta$ quantities of the power invariant Clark transformation we can then transform them over to the dq coordinate by using the park transformation. Where the frame rotation speed is represented by ω and the position of the rotating reference frame is given by ωt. Assuming that the dq components are rotating at an arbitrarily given frequency in order to derive the dq components in the Park transformation which is expressed as:

$$\mathbf{I}_{dq0} = \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \mathbf{T}_P\mathbf{I}_{\alpha\beta 0} = \underbrace{\begin{bmatrix} cos(\omega t) & sin(\omega t) & 0 \\ -sin(\omega t) & cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{T_P} \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} \tag{3.9}$$

We can see that the Parks transformation does also contain the homopolar or zero-sequence component which should remain unchanged given the assumption that one is working with a balanced three phase signal. The inverse park transformation is given

by:

$$\mathbf{I}_{\alpha\beta 0} = \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \mathbf{T}_{P,inv}\mathbf{I}_{dq0} = \underbrace{\begin{bmatrix} cos(\omega t) & -sin(\omega t) & 0 \\ sin(\omega t) & cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{T_{P,inv}} \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} \tag{3.10}$$

By combining the Clark and Park transformation we obtain a method to transform the three phase abc components from the time domain over to the dq coordinate directly. We do this by simply combining the transformation matrices $\mathbf{T}_c$ and $\mathbf{T}_p$ with one another. the resulting matrix $\mathbf{T}_{cp}$ can then be shown as:

$$\mathbf{T}_{cp} = \mathbf{T}_c\mathbf{T}_p = \sqrt{\frac{2}{3}} \underbrace{\begin{bmatrix} cos(\omega t) & cos(\omega t - \frac{2\pi}{3}) & cos(\omega t + \frac{2\pi}{3}) \\ -sin(\omega t) & -sin(\omega t - \frac{2\pi}{3}) & -sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{T_{cp}} \tag{3.11}$$

With the inverse transformation begin derived as:

$$\mathbf{T}_{cp,inv} = \sqrt{\frac{2}{3}} \underbrace{\begin{bmatrix} cos(\omega t) & -sin(\omega t) & \sqrt{\frac{1}{2}} \\ cos(\omega t - \frac{2\pi}{3}) & -sin(\omega t - \frac{2\pi}{3}) & \sqrt{\frac{1}{2}} \\ cos(\omega t + \frac{2\pi}{3}) & -sin(\omega t + \frac{2\pi}{3}) & \sqrt{\frac{1}{2}} \end{bmatrix}}_{T_{cp,inv}} \tag{3.12}$$

Variations of the inverse transformation in equation 3.12 are possible depending on the desired alignment (ie. d- or q-axis alignment), and of the desired invariance. By multiplying the transformation matrix with $\sqrt{\frac{2}{3}}$ and altering the zero components of the matrix from 1 to $\sqrt{\frac{1}{2}}$ as is shown in 3.12, we acquire the power invariant transformation.

3.2 Pulse Width Modulation - PWM

In previous sections, PWM has been described as a modulation technique used to generate the gate signals for the purpose of controlling the switching of converters. While also ensuring both rectifying and inverting operation through the modulation of the drawn currents from the voltage source. Which is obtained by having the drawn current in phase with the drawn voltage. When applying the intended control methods for this thesis, the modulation process occurs within the Current Control Loop (CCL). This is achieved by using the coordinate transforms (Clarke and Park) to generate the needed control voltage reference signals for the PWM module.

3.2.1 Sinusodial Pulse Width Modulation - SPWM

To put it simply the Sinusoidal Pulse Width Modulation (SPWM) is achieved by comparing a carrier waveform (triangular waveform) V_{cr} with a sinusoidal reference voltage V^*. Thereby generating a pulsed waveform at the output of the converter. The fundamental component of this output voltage is proportional to the reference voltage. For the sake of simplicity the PWM technique applied in a single phase inverter has been illustrated in Figure 3.2.

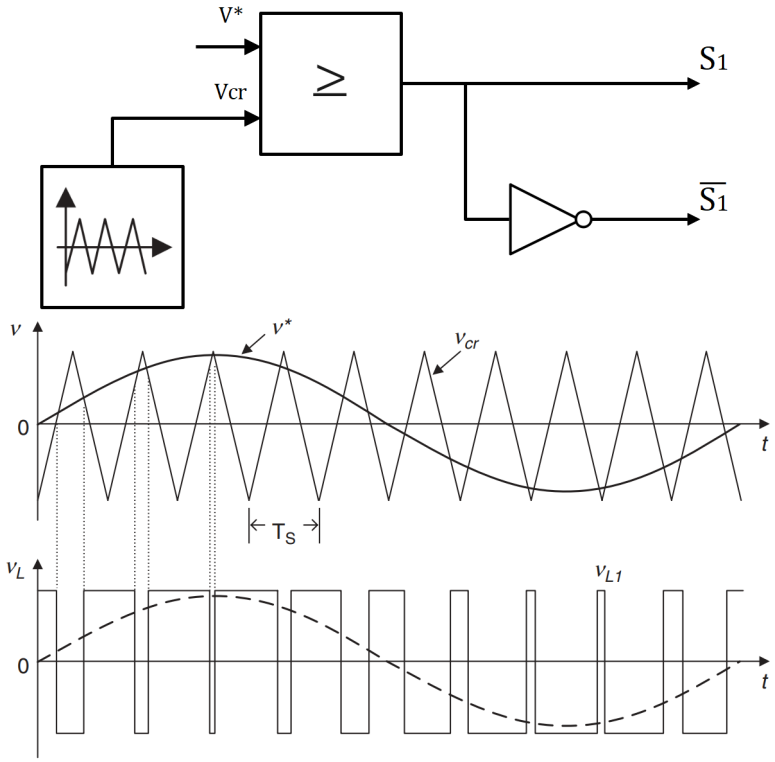


Figure 3.2: Sinusoidal PWM for a single phase [12].

By observing the waveforms in the figure one can see that the switches on and off time are determined by the following conditions:

$$\begin{cases} V* > V_{cr} & S_1 \text{ is } \textbf{on}, \ \overline{S_1} \text{ is } \textbf{off} \\ V* < V_{cr} & S_1 \text{ is } \textbf{off}, \ \overline{S_1} \text{ is } \textbf{on} \end{cases} \tag{3.13}$$

Similarly three phase output voltages are obtained by comparing the carrier waveform V_{cr} with three sinusoidal reference control voltages (V_a^*, V_b^*, V_c^*) with a 120^o displacement as shown in figure 3.3. Where the triangular waveform represents the carrier waveform V_{cr}.

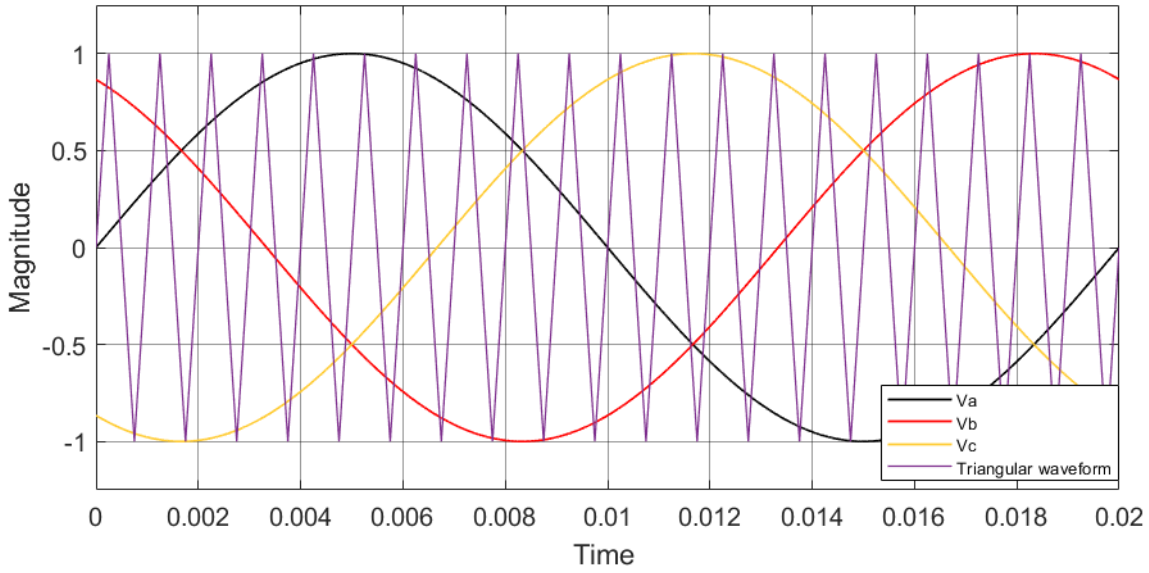


Figure 3.3: Sinusoidal PWM for three phase signal.

3.2.2 Space vector pulse width modulation - SVPWM

A variation of the PWM is termed Space Vector Modulation (SVM), which fully utilizes the available dc-bus voltage. Additionally resulting in an increased AC output of approximately 15% higher than that of SPWM control method which is limited to $V_{LL,max} = \frac{\sqrt{3}}{2}V_{dc}$. This is due to the SPWM method not taking advantage of the three phase properties and rather synthesizes the output voltages on a per-pole basis, where the power poles are $\overline{v}_{aN}$, $\overline{v}_{bN}$ and $\overline{v}_{cN}$. However by taking line-to-line voltages into consideration it is possible to get $V_{LL,max} \approx V_{dc}$ while using SVPWM [14].

The previously described three phase inverter from chapter 2, has been shown to only operate within eight distinct switching state topologies. Where six out of these eight switching states produce a non-zero output voltage which can be referred to as *active vectors* ($\mathbf{v}_1 \rightarrow \mathbf{v}_6$) while the remaining two switching states produce zero output voltage and are termed *zero vectors* ($\mathbf{v}_0, \mathbf{v}_7$). The six active vectors in the stationary reference frame form a hexagon and six separate sectors as shown in figure 3.4 [34]. The zero vectors ($\mathbf{v}_0, \mathbf{v}_7$) have not been included on the figure however they would be located in the origin. Additionally the angular position of the three phase voltages have been illustrated in figure 3.5.

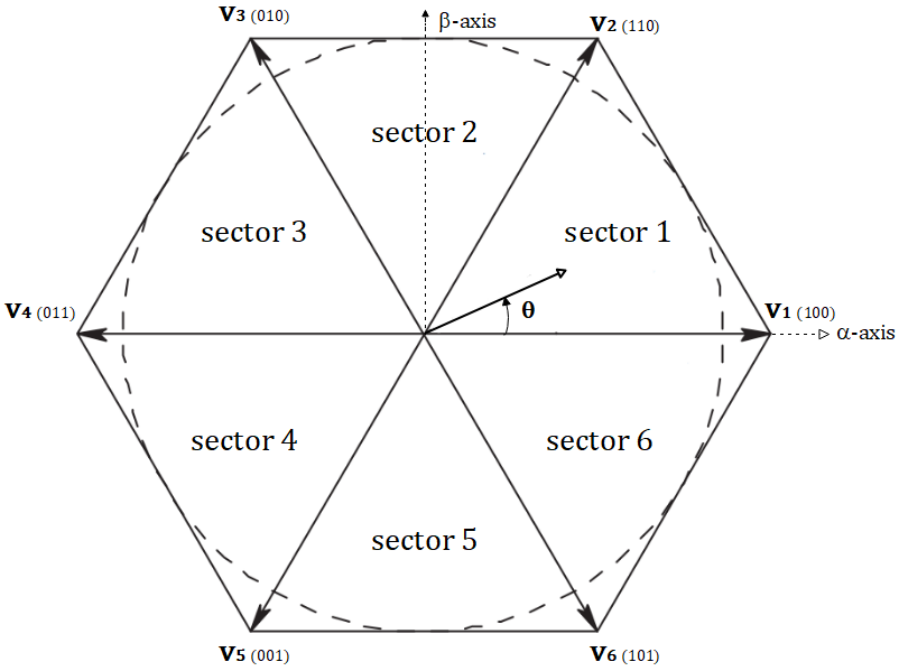


Figure 3.4: Representation of a three phase inverters active vector switching states, in the stationary reference frame [34].

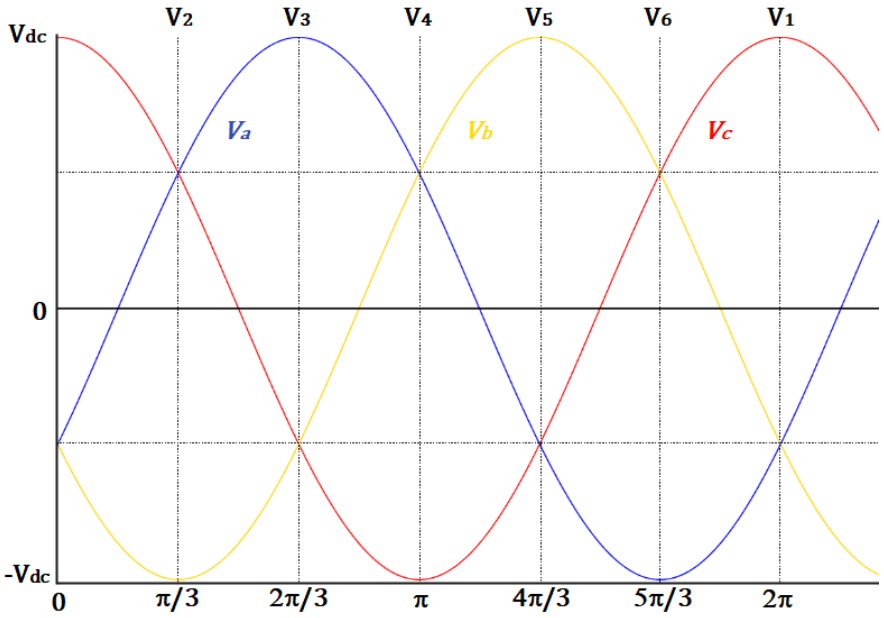


Figure 3.5: Angular position of the three phase voltages [8].

By considering the division of the six sectors, where the voltage vectors are generated by the inverter in the $\alpha\beta$ plane as shown in figure 3.4. A given reference voltage vector termed $\mathbf{v}^*$, positioned within a generic sector k, is able to be synthesized by using the adjacent vectors known as $\mathbf{V}_k$, $\mathbf{V}_{k+1}$ and $\mathbf{V}_0$ as shown in figure 3.6.

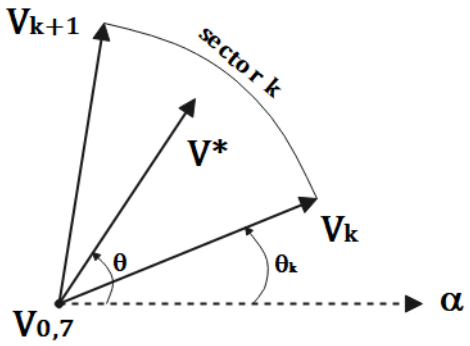


Figure 3.6: Reference vector in a generic voltage sector k [12].

Each vector is applied during their respective time t_k, t_{k+1} and t_0. This can be expressed with the following equations which have been adapted from [12].

$$\mathbf{v^*} = \frac{\mathbf{V}_k t_k + \mathbf{V}_{k+1} t_{k+1} + \mathbf{V}_0 t_0}{T} \tag{3.14}$$

$$T = t_k + t_{k+1} + t_0 \tag{3.15}$$

where T is the carrier period, often known as sampling period T_s and will be used interchangeably in this section. It should be notated that in SVM there are no separate modulators of each phase as one can find in carrier based PWM, and that the reference vector $\mathbf{v^*}$ is sampled with a fixed clock frequency expressed as $2f_s = \frac{1}{T_s}$. furthermore the vectors respective duty cycles are $\frac{t_k}{T_s}$, $\frac{t_{k+1}}{T_s}$ and $\frac{t_0}{T_s}$. the application time for each vector can be calculated by using trigonometric relations as follows:

$$t_k = \frac{3T|\mathbf{v^*}|(cos(\theta - \theta_k) - \frac{sin(\theta - \theta_k)}{\sqrt{3}})}{2V_{dc}} \tag{3.16}$$

$$t_{k+1} = \frac{3T|\mathbf{v^*}|}{V_{dc}} \frac{sin(\theta - \theta_k)}{\sqrt{3}} \tag{3.17}$$

$$t_{0,7} = t_0 + t_7 = T - t_k - t_{k+1} \tag{3.18}$$

in the equations above the angle of the reference vector $\mathbf{v}^*$ is termed θ and the angle of the vector $\mathbf{V}_k$ is termed θ_k. There are numerous methods of utilizing SVM, however primarily the difference is in the variations of the placement and duration of the zero vectors $(\mathbf{v}_0, \mathbf{v}_7)$, while remaining within the conditions of 3.18. Each method gives different

equations defining t_0 and t_7. The most popular three phase SVM method is by using symmetrical zero states as shown:

$$t_0 = t_7 = \frac{T - t_1 - t_2}{2} \tag{3.19}$$

What remains similar between the different methods is that the equations expressed in 3.16, 3.17 and 3.18 is applied to all of them. another variation using space vector is by applying vector modulation with what is known as Third harmonic injection Pulse Width Modulation (THIPWM), giving the resulting waveforms illustrated in figure 3.7

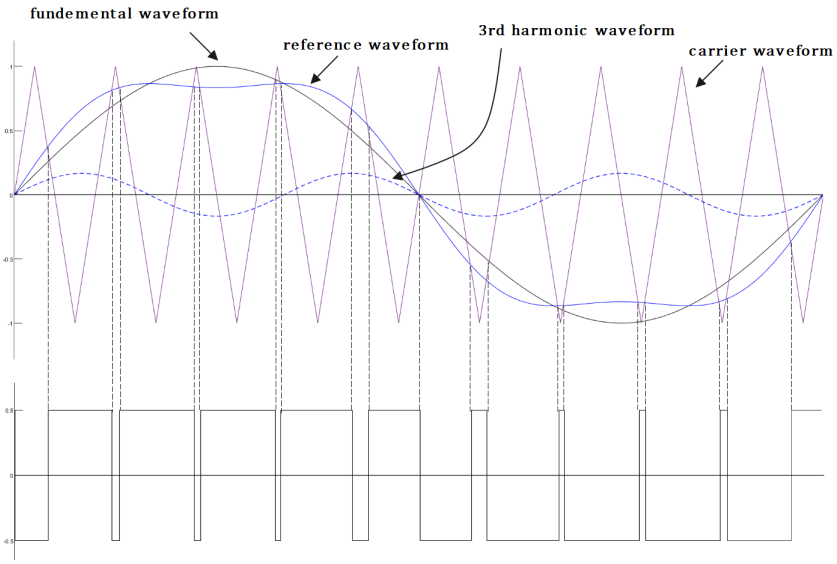


Figure 3.7: THIPWM waveform and output waveform.

The calculation of the zero vectors can be expressed as:

$$t_0 = \frac{T_s(1 - \frac{4}{\pi}M(cos\alpha - \frac{1}{6}cos3\alpha))}{2} \tag{3.20}$$

$$t_7 = T_s - t_0 - t_1 - t_2 \tag{3.21}$$

Where M refers to the modulation index, which in this case has an extended linear region of $M = 0.907$ as compared to SPWM. With the benefit of having low current distortions, however as can be observed in equation 3.20 and 3.21. There are more complicated calculations of the zero vectors [35]. The THIPWM is not intended to be used in this thesis and is only mentioned as an alternative complex modulation strategy which can be used.

3.3 Phase Locked Loop - PLL

GTIs are generally operated by using a PLL which is capable of tracking the phase of the connected grid accurately, and the controller uses the estimated phase angle to generate the synchronous reference signals which can be used for PWM [36]. The PLL technique which is proposed for this thesis is the Synchronous Phase Locked Loop technique, often termed as Synchronous reference frame PLL (SRF-PLL). Implemented by transforming the three phase abc voltage quantities into the rotating reference frame and using a standard PI controller to drive the q component of the transformed dq voltage to zero, thereby eliminating the steady state error and detecting the phase angle. This is part is commonly known as as the loop filter of the PLL structure. The structure of the proposed PLL technique has been illustrated in 3.8

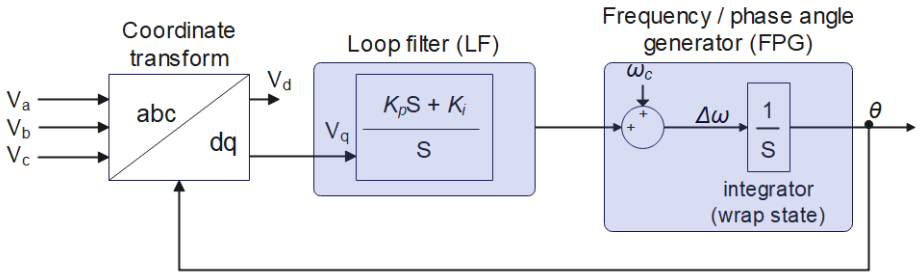


Figure 3.8: Topology of the Phase Locked Loop - PLL [37].

where the PI controller reduces the error by implementing a feedback loop and the output value is summed with the angular frequency ω_c=2·π·50, thereby the control signal $\Delta\omega$ is calculated and then integrated to generate the instantaneous phase angle. The angle however is wrapped at an angle of 2π to ensure that we produce a sawtooth waveform and do not gain a continuously increasing ramp. This can be achieved by adding a cosine block after the integrator, or as this is a common feature simply using "wrap state" directly on the integrator block should the software used allow for it. When the PLL angle which can be represented as θ is as close to the actual voltage vector angle ω_c then the difference will be close to zero (ω_c - $\theta \approx 0$), and the PLL is considered locked.

The PI controllers proportional (Kp) and integral components (Ki) can be tuned based on the TF of the PLL topology. By using the TF of a general PI controller which has been expressed in 2.20. We can derive both the closed loop TF of the PLL topology, as is expressed in [38]:

$$G_{OL} = \frac{V_{grid}(k_p s + k_i)}{s^2} \tag{3.22}$$

$$G_{CL}(s) = \frac{G_{OL}}{1 + G_{OL}} = \frac{V_{grid}(k_p s + k_i)}{s^2 + V_{grid} k_p s + V_{grid} k_i} \tag{3.23}$$

By comparing the closed loop TF with a generic second order system TF:

$$G_{CL}(s) = \frac{V_{grid}(k_p s + k_i)}{s^2 + V_{grid}k_p s + V_{grid}k_i} = \frac{k\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.24}$$

where k is the gain of the system, the natural frequency ω_n and damping ratio ζ can be derived as shown below:

$$\omega_n = \sqrt{v_{grid}k_i} \tag{3.25}$$

$$\zeta = \frac{k_p v_{grid}}{2\sqrt{v_{grid}k_i}} \tag{3.26}$$

3.4 Control strategy

Before the control strategy is presented it is important to understand the single phase equivalent circuit model of the grid connected inverter and the decoupling equations. For this reason the mathematical model of the inverter will be presented before the proposed control strategies.

Single phase equivalent circuit Model of the LCL filter

A single phase equivalent circuit of a standard LCL filter is presented in Figure 3.9 [39]. The filter model is built up with the following components: an inverter side inductance L_i, grid side inductance L_g and their parasitic resistances termed as R_i and R_g. There is also a filter capacitor C_f, and as is commonly used a damping resistance R_d has been added, however during design and simulation the damping resistance has been set to zero, as the methodology that is used does not require a damping component.

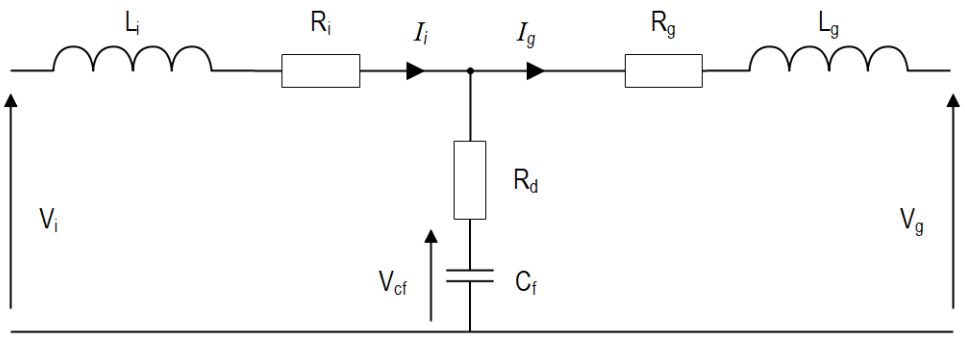


Figure 3.9: Single phase equivalent circuit of an LCL filter.

The voltage and current on the inverter side are termed as V_i and I_i, and on the grid side the voltage and current are termed as V_g and I_g on the LCL filter. The differential equation of the LCL filter in the stationary abc reference frame can be derived as follows:

$$L_i \frac{dI_i}{dt} = V_i - V_{cf} - (R_i + R_d)I_i + R_d I_g \tag{3.27}$$

$$L_g \frac{dI_g}{dt} = V_{cf} - V_g - (R_g + R_d)I_g + R_d I_i \tag{3.28}$$

$$C_f \frac{dV_{cf}}{dt} = I_i - I_g \tag{3.29}$$

in the synchronous dq reference frame voltage and current vectors are rotating with the same frequency termed ω. the converters phase voltage and currents can then be expressed using the synchronous dq frame. By using the previously expressed coordinate transformations seen in section 3.1 we can derive the voltage and current equations in the dq rotating frame as shown below.

d-axis equations:

$$L_i \frac{dI_{i,d}}{dt} = V_{i,d} - V_{cf,d} - (R_i + R_d)I_{i,d} + L_i \omega I_{i,q} + R_d I_{g,d} \tag{3.30}$$

$$L_g \frac{dI_{g,d}}{dt} = V_{cf,d} - V_{g,d} - (R_g + R_d)I_{g,d} + L_i \omega I_{g,q} + R_d I_{i,d} \tag{3.31}$$

$$C_f \frac{dV_{cf,d}}{dt} = I_{i,d} - I_{g,d} + \omega C_f V_{cf,q} \tag{3.32}$$

q-axis equations:

$$L_i \frac{dI_{i,q}}{dt} = V_{i,q} - V_{cf,q} - (R_i + R_d)I_{i,q} - L_i \omega I_{i,d} + R_d I_{g,q} \tag{3.33}$$

$$L_g \frac{dI_{g,q}}{dt} = V_{cf,q} - V_{g,q} - (R_g + R_d)I_{g,q} - L_i \omega I_{g,d} + R_d I_{i,q} \tag{3.34}$$

$$C_f \frac{dV_{cf,q}}{dt} = I_{i,q} - I_{g,q} - \omega C_f V_{cf,d} \tag{3.35}$$

3.4.1 Voltage oriented control - VOC

In this section VOC in three phase GTIs is introduced. The VOC structure can be separated into two parts, the outer Voltage Control Loop (VCL) and the inner Current Control Loop (CCL). This is a common method of control similar to the cascaded control loops often seen used in motor control structures. An illustration of the three phase inverter with an LCL filter using a VOC scheme can be seen in figure 3.10. Where the "controller" block contains the control loops which will be explained in this section [35]. The grid currents (i_a,i_b,i_c) and voltages (V_{ga},V_{gb},V_{gc}) are extracted and transformed from the *abc* reference frame to dc values, following the Clarke and Park transformation which has been explained in section 3.1.2. The grid has a nominal frequency of 50Hz, a PLL block has been implemented to obtain the correct angular position θ. In addition to tracking and regulating the angular position according to any form of deviation, following what has been explained in section 3.3.

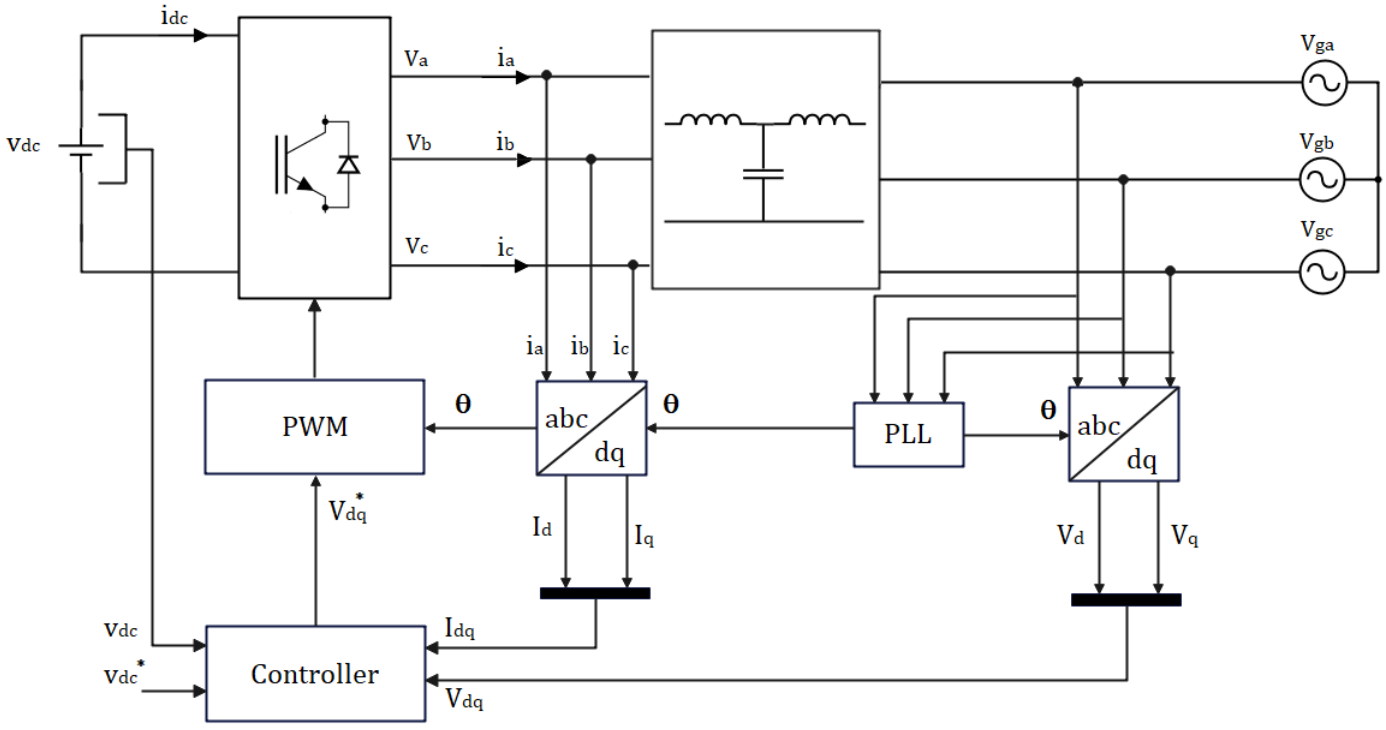


Figure 3.10: VOC structure with LCL-filter. The controller block has been illustrated in further detail in figure 3.11.

The VCL calculates the error between the desired DC-link voltage $V_{dc}*$ and the measured DC-link voltage V_{dc}. This error can then be reduced to zero by using a PI controller, where the output will contain the desired d-axis current component. The process of tuning the PI controllers gain constants are according to the MO criterion which has been introduced in section 2.2.3 and will be further detailed for the intended system in

section 4.4.

In the CCL the currents are controlled in the synchronous rotating dq reference frame by using decoupled feedback control. The voltage and current components dq-axis equations have been previously derived in (3.30 - 3.35). These equations however can be further simplified to allow for a feed forward compensation approach by using decoupled components in the current control loop. The feed forward will compensate the cross coupling components and allow for the d-axis and q-axis components to be controlled separately. The implementation of a feed forward compensated current controller in the synchronous reference frame has been represented in figure 3.11, where the desired dq-axis reference currents are termed i_d* and i_q* respectively. These reference currents are compared to the real dq-axis currents and produce an error signal which is corrected using a PI controller as has been described previously.

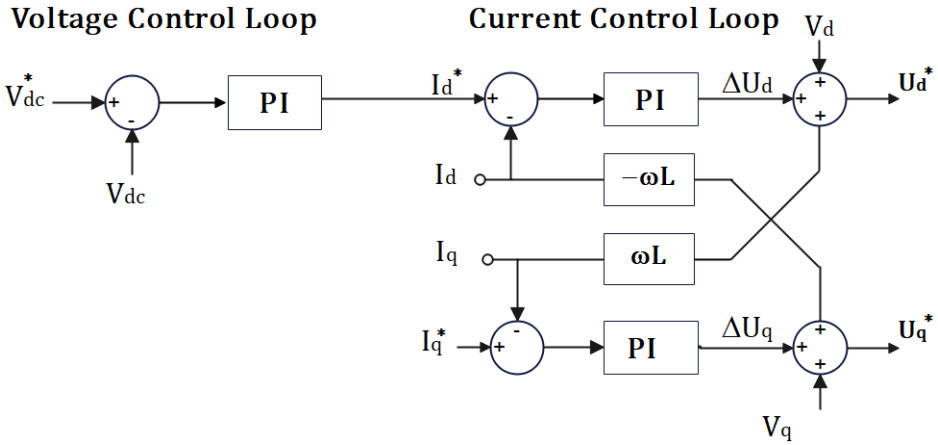


Figure 3.11: synchronous controller in dq reference frame showing both VCL and CCL, used in the VOC illustrated in 3.10.

Similarly the dq-axis voltages are termed V_d and V_q respectively. The d-axis reference current i_d of the controller is extracted by measuring the system and conducting a coordinate transformation of the natural abc frame components as shown in figure 3.10. Commonly the q-axis reference current i_q is set to zero, thereby achieving the often desirable Unity Power Factor (UPF) given that the controller is properly tuned. The mathematical description of the VOC scheme shown in figure 3.10, is derived while neglecting the LCL-filter capacitor C_f. Furthermore for the sake of simplicity the inductor termed L is the sum of the LCL-filter inductors L_i and L_g, while also neglecting the internal resistances of the inductors as the voltage drop is much lower than of the inductors.

$$V_{grid} = L\frac{di_{abc}}{dt} + V_{conv} \tag{3.36}$$

$$\begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.37}$$

As stated previously the abc reference frame current and voltages are transformed into the dq-frame by using Park and Clark coordinate transforms. According to figure 3.11 the decoupled control equations are given as follows:

$$U_d* = L\frac{di_{Ld}}{dt} - \omega L i_{Lq} + v_d \tag{3.38}$$

$$U_q* = L\frac{di_{Lq}}{dt} + \omega L i_{Ld} + v_q \tag{3.39}$$

Both the active and reactive power can be calculated by using the dq-frame current and voltage components as shown:

$$p = \frac{3}{2}(v_d i_d + v_q i_q) \tag{3.40}$$

$$q = \frac{3}{2}(v_q i_d - v_d i_q) \tag{3.41}$$

as stated previously to achieve UPF the q-axis reference current I_q is set to zero. thereby the active and reactive power equations 3.40 and 3.41 can be simplified as followed:

$$\begin{cases} p = \frac{3}{2} v_d i_d \\ q = \frac{3}{2} v_q i_d \end{cases} \qquad \text{Given that: } I_q = 0 \tag{3.42}$$

3.4.2 Direct Power Control - DPC

A means of controlling the DC-AC converter is by using the DPC method. The fundamental objective of DPC is to control the instantaneous active power P and reactive power Q. The DPC method can be obtained in the stationary $\alpha\beta$ reference frame, by following the instantaneous power control theory sourced by [40]. As has been mentioned previously, by using the power invariant $\alpha\beta$ coordinate transform, one can calculate and determine an estimation of the instantaneous power and reactive power as seen in equation 3.7. Furthermore with some alterations to the equation, it becomes possible to obtain the estimated current quantities in $\alpha\beta$ coordinate from the instantaneous active and reactive power calculation. Which is expressed as:

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2}\begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix}\begin{bmatrix} P* \\ Q^* \end{bmatrix} \tag{3.43}$$

Following this equation we can acquire a method of controlling the converter, by simply selecting the desired active and reactive power. This will calculate the estimated $\alpha\beta$ current quantities, which will undergo the CCL structure similarly to what has been explained in the previous section.

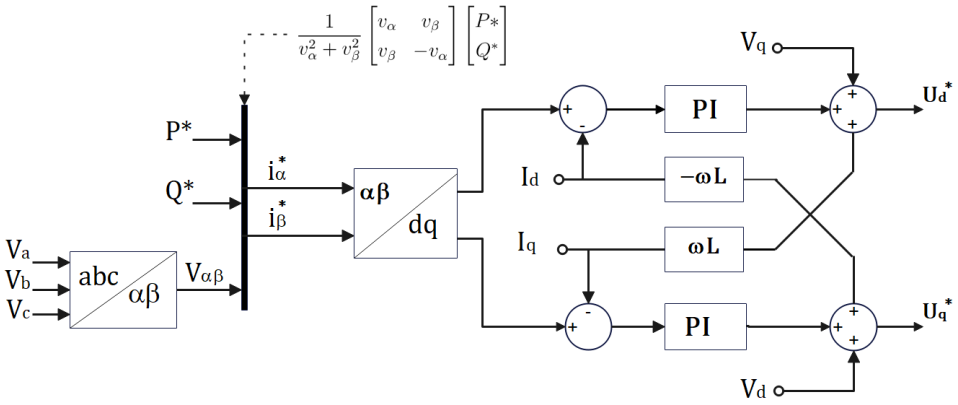


Figure 3.12: DPC using the dq reference frame and CCL.

The controller is intended to reduce the error between the current quantities to zero. However the PI controllers which will be used in this thesis are more suitable for controlling components in the rotating reference frame, instead of the stationary reference frame. Which is why the DPC method can be altered, so that the estimated $\alpha\beta$ current components can be transformed to the dq reference frame. Once the dq current components are acquired, these components can be used in the same decoupled CCL illustrated in 3.11. The DPC using this methodology in the dq reference frame has been illustrated in figure 3.12.

Chapter 4

Converter Modelling and Design

This chapter presents the proposed methodology of designing a grid connected inverter as well as the components of the LCL-filter based on the theoretical framework that has been presented by the previous chapters. Additionally a DC-DC topology connected to the dc-link and the battery storage system will be presented. However as this thesis revolves around the control of a GTI, thus DC-DC converters components will not be presented with as much detail as the rest of the system. However sources have been provided explaining the DC-DC converter in further detail.

The grid side converter which is used in this thesis is compromised of a three phase two-level PWM converter connected to a LCL-filter. Furthermore as has been illustrated in figure 4.1, the proposed model will use a grid-tied inverter structure connected to a bidirectional DC-DC buck-boost converter. This converter is connected in between the dc-link and battery supply while allowing bidirectional power flow.

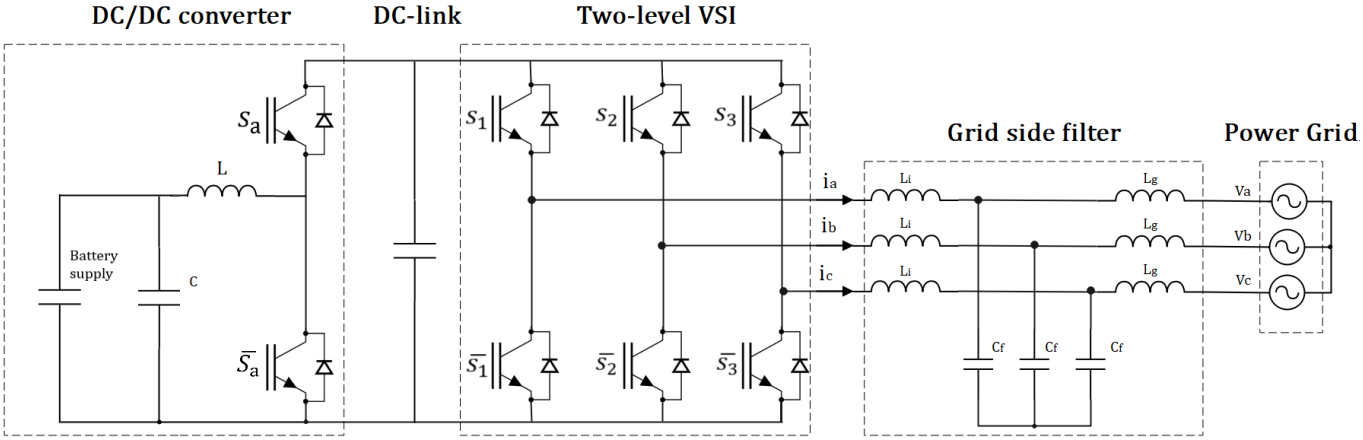


Figure 4.1: Proposed GTI, with DC-DC buck-boost converter.

4.1 LCL Filter Design methodology

The proposed LCL filter design is based on the methodology adapted from [41], the mathematical model of the filter has been properly described previously in section 3.4. This method of filtering aims to provide a simple, robust and systematic design methodology for the tuning parameters of a LCL filter. Furthermore it is capable of overcoming the shortcomings of some of the more common design methodologies, such as the robustness of the LCL filter during large grid impedance variations. The chosen methodology should allow for a stable steady state operation without the use of any damping for a PI controlled converter. The accuracy of the capacitor standard values and inductor saturation are also taken into account.

The LCL filter design methodology intends to meet the grid code requirements by reducing the high-order current harmonic components at the used switching frequency f_{sw}. The required input data for the initial step of the design methodology is shown in table 4.1. It should be noted that the rated power in the code calculation has been set to a lower value than the intended nominal value. In order to be able to run tests with lower than nominal phase currents, without breaking the limit of the 5% IEEE THD requirement. The code used to calculate the filter values according to the following design methodology can be found in appendix A.3, with some assumptions taken based on recommended values from the source of the methodology.

Input Data	
Line-to-Line RMS grid voltage	V_{LL} (RMS)
Rated active power of the system	P
Grid frequency	f_g
Converter switching frequency	f_{sw}
Saturation current of the LCL filter inductors	I_{sat}

Table 4.1: LCL filter design, Input variables

Once the required input data is set the filter parameters can then be tuned using the following steps which will be explained in further detail during this section:

- Resonance frequency condition
- Maximum value of the total inductor
- Tuning of the converter side inductor
- Tuning of the gird side inductor

Resonance frequency condition

Problems can arise due to resonance and are avoided by properly tuning the filter parameters to be contained within a stable frequency region, which requires no additional damping. As is shown in equation 4.1 the resonance frequency f_{res} is based on a function on the filter capacitor and inductors L_i and L_g, where L_g is assumed to be the sum of the grid side filter inductance and the grid inductance.

$$f_{res} = \frac{\sqrt{\omega_{res}}}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{L_g + L_i}{L_g L_i C_f}} \tag{4.1}$$

Filter inductors are considered constant as their corresponding saturation current is not surpassed. While the grid inductor can have large variating values based on the ratio of the grid resistance/reactance (R_{grid}/X_{grid}). This in turn depends on a number of grid configurations such as: low, medium or high voltage lines and the conditions (weak or stiff grid) to name a few. Taking into consideration all the variations in the grid inductance and making the assumption of weak grid, the range of the possible resonance frequencies are shown to be restricted into a stable region within the grid frequency f_g and switching frequency f_{sw} as is depicted in the following expression as:

$$10 f_g \leq f_{c,min} < f_{res,min} \leq f_{res}(L_g, C_f) \leq f_{res,max} < f_{c,max} \tag{4.2}$$

The resonance frequency is a decreasing function for both L_g and C_f as shown in equation 4.2, within [$f_{res,min}$,$f_{res,max}$]. However in order to avoid the resonance problems, it is important that f_{res} is higher than 10 times the grid frequency f_g and less than half of the switching frequency f_{sw}. Furthermore in the case of using a PI-based current control method with grid current feedback, two critical frequencies are defined as [$f_{c,min}$,$f_{c,max}$]. The resonance frequency variables have been expressed in Table 4.2.

Resonance frequency Variables	
$f_{c,min}$	$\frac{f_{sw}}{6}$
$f_{c,max}$	$\frac{f_{sw}}{2}$
$f_{res,min}$	$\frac{1}{2\pi}\sqrt{\frac{L_i+L_{g,max}}{L_{g,max}L_iC_{f,max}}}$
$f_{res,max}$	$\frac{1}{2\pi}\sqrt{\frac{L_i+Lg,min}{L_iL_{g,min}C_{f,min}}}$

Table 4.2: LCL filter design, Resonance frequency Equation Variables

Maximum value of the total inductor

For the sake of efficiency in reducing the losses and the voltage drops in the filter, the sum of the LCL filter inductor values should be made as small as possible. This condition leads to improvements in speed and the dynamic of the system. Following this notion the maximum total inductance termed $L_{t,max}$ should be lower than 0.1 pu as is shown in the following expression:

$$L_{t,max} = 10\%\frac{V_{LL}^2}{2\pi f_g P} \tag{4.3}$$

Maximum LCL Filter Capacitor Value

The filter capacitor is designed to limit the consumption of reactive power Q_c within $\lambda\%$ or less than the rated power P as is depicted in equation 4.4. where λ is a positive factor chosen to be less than or equal to 5%. The reactive power consumption is given by equation 4.5. Using these two equations the maximum value of the filter capacitor can be determined and is expressed in equation

$$|Q_c| \leq \lambda\%|P| \tag{4.4}$$

$$Q_c = -V_{LL}^2 C_f 2\pi f_g \tag{4.5}$$

$$C_{f,max} = 5\%\frac{P}{2\pi f_g V_{LL}^2} \tag{4.6}$$

It is important to note that when the capacitor value is too low, this would lead to the inductor values being too high. Thus a recommended method is to set the capacitor value equal to 1/2 of $C_{f,max}$, and gradually increase the value until the constraints are satisfied up to the maximum value.

Tuning of the converter side inductor

When tuning the converter side inductor, it is important that the inductances are large enough to attenuate the maximum switching ripple current Δi_{max}, in addition to avoiding saturation. The maximum converter current ripple is given by Equation 4.7 and with some alterations the converter side inductor value is given by Equation 4.8.

$$i_{max} = \frac{V_{dc}}{6 f_{sw} L_i} \tag{4.7}$$

$$L_{i,min} = \frac{V_{dc}}{6 f_{sw} \Delta i_{max}} \tag{4.8}$$

However in order to avoid inductor saturation problems there are limitations set on the minimum converter side inductor value.Notedly during high frequencies the maximum converter side current becomes equal to the grid side current as shown in Equation 4.9. Equations 4.8 and 4.10 shows the conditions which must be met for the saturation current I_{sat}.

$$I_{i,max} = I_{g,max} = \sqrt{\frac{2}{3}} \frac{P}{V_{LL}} \tag{4.9}$$

$$|I_{i,max} + \frac{\Delta i_{max}}{2}| < I_{sat} \tag{4.10}$$

Following these equations and conditions it becomes possible to determine the minimum converter side inductor value as is shown in Equation 4.11.

$$L_{i,min} > \frac{V_{dc}}{(I_{sat} - I_{i,max}) 12 f_{sw}} \tag{4.11}$$

Tuning of the grid side inductor

The relationship between the grid current and the converter at switching frequency is determined by an attenuation constant δ. This constant must be first be selected for sake of tuning the filters grid side inductor. Some of the variables used in the following equations for tuning of the grid side inductor are defined in Table 4.3. The constant δ represents the harmonic attenuation rate and can be expressed by equation 4.12 followed by its positive solution given by equation 4.13:

$$\delta = |\frac{i_g}{i_i}|_{sw} = \frac{1}{|1 + a(1 - L_i C_f \omega_g^2)|} \tag{4.12}$$

$$a = \frac{1 + \delta}{\delta a_1} \tag{4.13}$$

where a must satisfy the following conditions $0 \leq a \leq a_{max}$ and a_{max} is given by the following equation:

$$a_{max} = \frac{L_{t,max}}{L_i} - 1 \tag{4.14}$$

The current harmonics can be reduced significantly based on the value of the attenuation constant δ, due to the ratio being proportional to the THD. Therefore it is desirable during the design that the attenuation is as low as possible, given that it is within the requirements. According to equation 4.2 and the critical frequencies equations $f_{res,min}$ and $f_{res,max}$ from table 4.2, must verify the conditions presented in Equations 4.15 , 4.16 and 4.17. However the desired attenuation rate must have a greater value than the minimum attenuation rate δ_{min}, which corresponds to

Equation Variables
$a_1 = L_i C_f \omega^2 - 1$
$a_2 = (a_1 + 1)L_i + a_1 L_{g,max}$
$a_3 = (L_i + a_1 L_{g,max}) L_i C_{f,max}$
$b_2 = (a_1 + 1)L_i + a_1 L_{g,min}$
$b_3 = (L_i + a_1 L_{g,min}) L_i C_{f,min}$

Table 4.3: LCL filter design, Equation Variables

$$\delta < \frac{36L_i - (2\pi f_{sw} L_i)^2 C_{f,max}}{a_3 (2\pi f_{sw})^2 - 36a_2} \rightarrow 1st\ \delta\ condition \tag{4.15}$$

$$\delta < \frac{4Li - (2\pi f_{sw} L_i)^2 C_{f,min}}{b_3 (2\pi f_{sw})^2 - 4b_2} \rightarrow 2nd\ \delta\ condition \tag{4.16}$$

$$\delta > \delta_{min} = \frac{1}{|1 + a_{max} a_1|} \rightarrow 3rd\ \delta\ condition \tag{4.17}$$

Where the equations of the variables have been depcited in Table 4.3. The grid side inductor is tuned in order to restrict the grid current harmonics according to the grid code requirements and standards. As mentioned in an earlier chapter the IEEE standard for harmonics, has a requirement of the grid current THD to be under 5% [6]. Following the equations that have been shown in this section, the grid side inductor is determined by the relation between the converter side and the grid side inductors as expressed by Equation 4.18.

$$L_g = aL_i = \frac{L_i(1 + \delta)}{\delta a_1} \tag{4.18}$$

Following all of these steps concludes the tuning of the LCL filter parameters and all that is left is the verification of said parameters. Given that some of the steps have initial recommended values it is important to redo all the iterations with adjusted values until the most efficient parameters are determined.

4.2 DC-link

The DC-link should be capable of handling the induced ripple current generated from the PWM, and any transients in power regulation. For this purpose as has been previously stated the internal diodes of IGBTs will function as a diode rectifier against an active grid. Leading to a large inrush current when the DC link is not precharged and the converter is connected to the grid. While the inrush current can be attenuated by the LCL-filter, it comes with the disadvantage of possibly causing the dc link voltage to overshoot [42]. Following the proposed design methodology for the LCL filter from [41]. The LCL filter can be approximated to an L filter by neglecting the filter capacitor C_f, where the inductor value will be equal to the total inductance $L_T = L_g + L_i$. This approximation can be used due to the fact that the capacitor of the LCL filter is designed to have a great impedance value for fundamental signals. With this simplified approximation and neglecting the influence of internal resistance elements, the relation between the grid and converter voltages can be expressed in complex forms as shown in the equation below:

$$V_i = V_g + jL_t\omega_g i_g \tag{4.19}$$

Given this equation we can derive the maximum converter output magnitude voltage $V_{i,max}$, and express it as:

$$V_{i,max} = \sqrt{V_{g,max}^2 + (L_t\omega I_{g,max})^2} \tag{4.20}$$

$$\text{where,} \quad I_{g,max} = \sqrt{\frac{2}{3}}\frac{P}{V_{LL}} \tag{4.21}$$

Once $V_{i,max}$ has been determined, the minimum DC voltage with respect to SVM can be calculated as:

$$V_{dc,min} = \sqrt{3}V_{i,max} \tag{4.22}$$

The DC-link capacitor size is primarily determined by the acceptable dc ripple voltage ΔV_{dc} and the switching frequency, as well as the Line to line voltage V_{LL} and rated power P of the system. By using the known parameters such as ΔV_{dc} and the switching frequency which has been used in the design of the LCL-filter. It is possible to calculate

the minimum dc-link capacitance needed, which can be derived as[8]:

$$C_{dc,min} = \frac{P(\sqrt{2}V_{dc} + \sqrt{3}V_{LL})}{2\sqrt{3}V_{LL}V_{dc}\Delta V_{dc}f_{sw}} \tag{4.23}$$

4.3 Proposed DC-DC Model

It is common for the voltage of the energy storage system (ESS) to be lower than the dc-link voltage, therefore it is often necessary to implement a buck-boost type of DC-DC converter as an answer to this problem. The proposed bidirectional DC-DC converter has been illustrated in figure 4.2, and is a combination of the buck and boost converter presented in section 2.1.4 and 2.1.4 respectively. The proposed topology consists of two IGBT switches (S_a, $\overline{S_a}$), two anti-parallel diodes, a capacitor C and an inductor L. Furthermore the dc-link voltage has been termed V_{DC} with a dc-link capacitor C_{dc}, and finally the voltage of the battery supply/load is termed V_{ESS}.

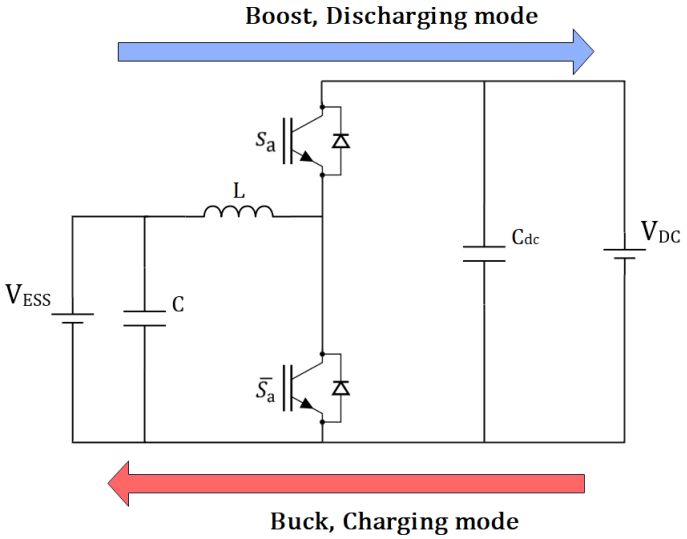


Figure 4.2: DC/DC bidirectional converter topology.

In figure 4.2 the Energy Storage Systems (ESSs) battery is connected to the low-voltage side, while the high-voltage side is connected to the dc-link. The inductor is responsible for the output current ripple and is considered to be the main component for energy transfer of the converter. as indicated in figure 4.2 the converter is designed to be fully capable of operating in both buck and boost mode. Furthermore the designed converter allows for current flow in both direction while keeping the same voltage polarity of the dc-link voltage during both operating modes. The converter is capable of obtaining a smooth output current/voltage, however due to the DCM operation of the converter it is necessary to have proper dc-link filtering and high switching frequency.

Both the minimum inductor and capacitor size have been determined using the following equations 2.11 and 2.12, from section 2.1.4. Assumptions have been made when setting the value of the voltage and current ripples. With the intention to reduce the size of the inductor and capacitor components, while remaining. The operation of the converter and whether the converter is conducting in buck or boost mode, is determined by the following switching conditions [43]:

- **Buck Mode:**

  When IGBT switch S_a is on and $\overline{S_a}$ is off, the $\overline{S_a}$ diode is operating in forward bias. The converter is then operating in buck mode, thereby charging the inductor L. The voltage equation in this point of time is as follows:

  $$L\frac{di_L}{dt} = V_{ESS} - V_{DC} \tag{4.24}$$

  When IGBT switch S_a is off and $\overline{S_a}$ is off, the $\overline{S_a}$ diode will be operating in forward bias. Thus the inductor will attempt to maintain the current in the same direction leading to the discharging of the inductor. The voltage across the inductor in this point of time is as follows:

  $$L\frac{di_L}{dt} = V_{ESS} \tag{4.25}$$

  Combining both equation 4.24 and 4.25 and adding a variable a, where a is equal to 1 when S_a and a is 0 when S_a is off. Gives the following equation when considering the state of the upper IGBT S_a:

  $$\frac{di_L}{dt} = \frac{V_{ESS}}{L} - \frac{aV_{DC}}{L} \tag{4.26}$$

- **Boost Mode:**

  when IGBT switch S_a is off and $\overline{S_a}$ is on. The converter is operating in boost mode and the inductor L charges. The voltage equation during this time can be derived as follows:

  $$L\frac{di_L}{dt} = V_{ESS} \tag{4.27}$$

  When both IGBT switches S_a and $\overline{S_a}$ are off, S_a diode will be forward biased. During this time the inductor will begin to discharge as it attempts to maintain the current in the same direction. Giving the following voltage equation:

$$L\frac{di_L}{dt} = V_{ESS} - V_{DC} \tag{4.28}$$

equation 4.27 and 4.28 can also be combined when considering the state of the lower IGBT $\overline{S_a}$, as follows:

$$L\frac{di_L}{dt} = \frac{V_{ESS}}{L} - (a-1)\frac{V_{DC}}{L} \tag{4.29}$$

In this case when a is equal to 1 when $\overline{S_a}$ is on and a is equal to 0 when $\overline{S_a}$ is off.

The converter system is can be controller by using VOC in order to assure the desirable voltage reference in the dc-link, while controlling the DC-DC converter to generate the desired current flow. This can be obtain by using a CCL which compares the desired current reference with the battery current, and similar to what has been explained previously a PI controller can be used to reduce the error and provide the gate signals of the DC-DC converter [44].

4.4 PI Controller Optimization and Analysis

Modulus Optimum

The methodology of determining the PI controllers gain constants in the control loop, is based on the theory presented in section 2.2.3. For the sake of analysing the system stability a bode plot is used to derive the two quantitative measures known as the gain margin (GM) and the Phase margin (PM). These two quantities will be able to determine the systems stability dynamics and stability margins. Bode plots have been widely used in the field of system stability along side other methods, both the GM and PM have been thoroughly explain in literature such as [45], and will not be explained in further detail in this thesis. In order to determine the controllers proportional and integral gain constants k_p and k_i, the high frequency TF from V_g to I_g of the LCL filter as seen in figure 3.9 is derived [46]:

$$\frac{I_g}{V_g} = \frac{1}{L_i L_g C_f s^3 + C_f(L_g R_i + L_i R_g)s^2 + (C_f R_g R_i + L_i + L_g)s + (R_i + R_g)} \tag{4.30}$$

By combining the TF of the PI controller $PI(s)$ from equation (2.20) and the filter TF from equation (4.30) in series, the open loop and subsequently closed loop TF ($G_{OL}(s)$,

$G_{CL}(s)$) of the current controller can be determined as:

$$G_{OL}(s) = \frac{k_p s + k_i}{L_i L_g C_f s^4 + C_f(L_g R_i + L_i R_g)s^3 + (C_f R_g R_i + L_i + L_g)s^2 + (R_i + R_g)s} \tag{4.31}$$

$$G_{CL}(s) = \frac{k_p s + k_i}{L_i L_g C_f s^4 + C_f(L_g R_i + L_i R_g)s^3 + (C_f R_g R_i + L_i + L_g)s^2 + (R_i + R_g + k_p)s + k_i} \tag{4.32}$$

By simplifying the systems TF into a more desirable form, it becomes possible to use a systematic design process for modulus optimization as stated in [23]. Thus the TF from equation 4.30 is then further simplified by excluding the high frequency terms in equation 4.33. By using the simplified equation, the filters time constant T_{LCL} can be derived as shown in equation 4.34.

$$\frac{I_g}{V_g} = \frac{1}{(Lg + Li)s + (R_g + R_i)} \tag{4.33}$$

$$T_{LCL} = \frac{L_i + L_g}{R_g + R_i} \tag{4.34}$$

Furthermore the converter TF is expressed in equation 4.35, with a converter time delay T_a. An assumption has been made to determine the converter time delay, $T_a = \frac{1}{5 f_{sw}}$.

$$C(s) = \frac{1}{1 + T_a s} \tag{4.35}$$

Using the simplified filter TF shown in 4.33 and combining it with the TF of the PI controller from equation 2.21 and the converter TF from equation 4.35. A simplified open and closed loop transfer function ($G_{OL,s}(s)$, $G_{CL,s}(s)$) is obtained as shown:

$$G_{OL,s}(s) = k_p \left[\frac{T_i s + 1}{T_i s}\right] \left(\frac{1}{T_a s + 1}\right) \frac{\frac{1}{R_t}}{T_{LCL} s + 1} \tag{4.36}$$

$$G_{CL,s}(s) = \frac{k_p (T_i s + 1)\frac{1}{R_t}}{T_i s (T_a s + 1)(T_{LCL} s + 1) + k_p (T_i s + 1)\frac{1}{R_t}} \tag{4.37}$$

For the sake of simplicity both internal resistances R_i and R_g are assumed to be equal to 0.1Ω and the total is defined as $R_t = R_i + R_g$. Similar to what was shown in section 2.2.3, the system presented in this section has a large and a small time constant, where $T_{LCL} >> T_a$. in which case the MO tuning method can be applied, where the controllers parameters are defined below using equations adapted from [23].

$$T_i = T_{LCL} \tag{4.38}$$

$$k_p = \frac{T_{LCL} R_t}{2T_a} \tag{4.39}$$

By substituting equations 4.38 and 4.39 into equation 4.36 we acquire the new open and closed loop TF:

$$G_{OL,mo}(s) = \frac{1}{2T_a s(T_a s + 1)} \tag{4.40}$$

$$G_{CL,mo}(s) = \frac{1}{2T_a s(T_a s + 1)} = \frac{\frac{1}{2T_a^2}}{s^2 + \frac{1}{T_a} s + \frac{1}{2T_a^2}} \tag{4.41}$$

It can be observed that both equation 4.40 and 4.41 have the same form as the TF from section 2.2.3, from the theoretical framework. Thus the closed loop TF 4.41 resembles the form of a generic second order TF. Which means that both the natural frequency and the damping factor are defined just as in equations 2.30 and 2.31. The Bode plots of the TFs are shown in Figure 4.3, 4.4, 4.5 and have been created using Matlab. The Matlab code has been provided in appendix A.4.

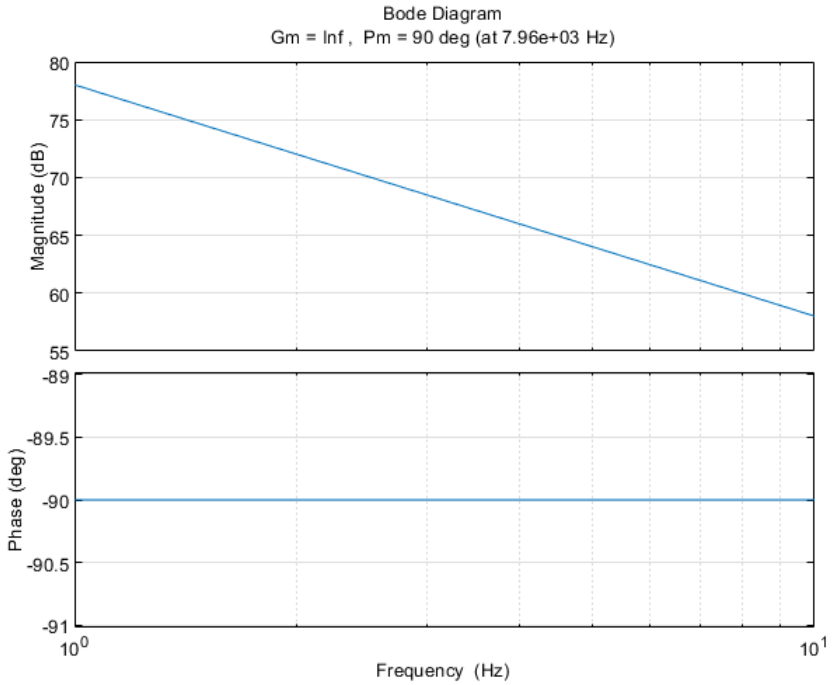


Figure 4.3: Bode plot with the first order approximation, $G_{OL,s}(s)$ without the converter TF added.

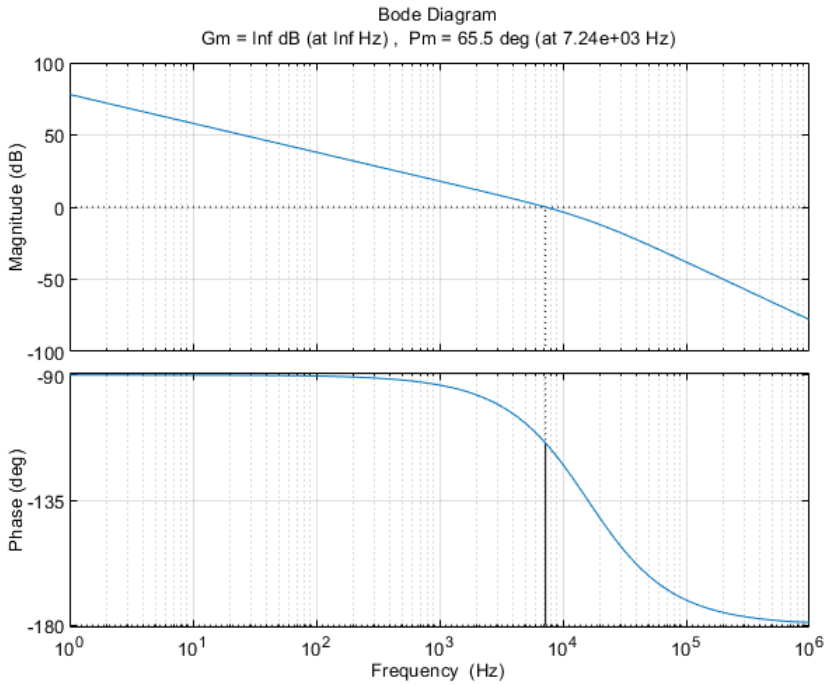


Figure 4.4: Bode plot of the first order approximation $G_{OL,s}(s)$.

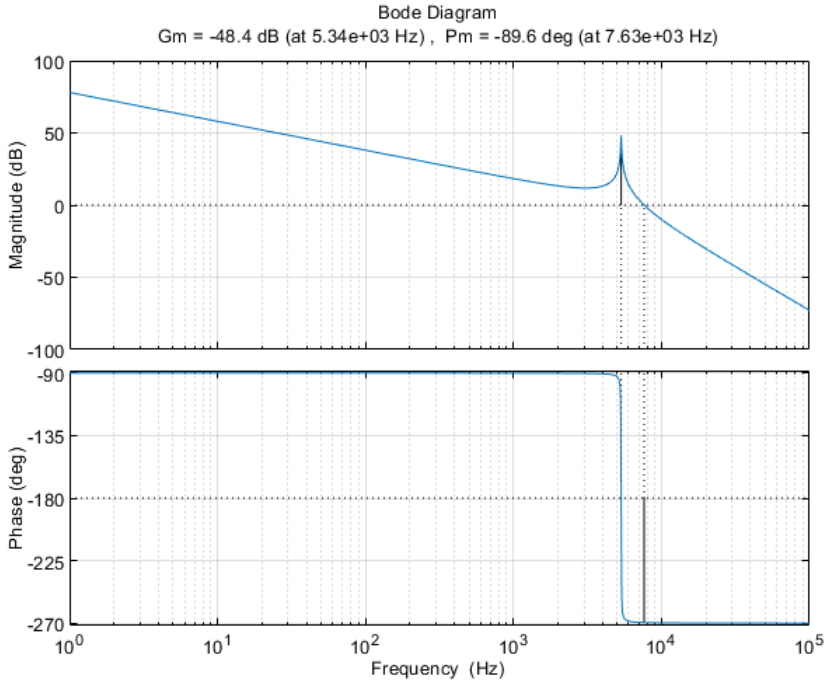


Figure 4.5: Bode plot using TF $G_{OL}(s)$ from equation 4.31.

Chapter 5

Simulation Model

In this chapter the simulation model and the results of the chosen topology will be presented. The entirety of the simulation model has been designed using the MATLAB based application Simulink, which allows for the user to build their system in a block diagram environment. The application allows the user to simulate the constructed models within either the discrete or continuos time domain. Using the *powergui* block provided in the Simulink library the selected sample time has been chosen to be 1 µs, which determines the speed in which differential equations of the system are solved. In order to simulate the dynamic system, the simulation solver located in the configuration parameter settings, is set to a variable step solver. The variable step solver allows for the step size during the simulation to vary, with the intention to reduce the step size to increase the accuracy of the simulated model during certain events, such as rapid state changes [47]. The discrete blocks obtained from the Simulink library have had their sample time set to -1, which indicates that the sample time is inherited and Simulink is able to determine the best sample time for the block, based on the given model [48]. The parameters of the simulation model can be found in table 5.1. The calculations and assumptions of the parameters have been made following the recommendations of the sources, and can be found in different sections of appendix A. An overview of the Simulation model has been provided in figure 5.1, each of the elements used to build this system will be discussed in more detail during this chapter. while the final sections will review the results on different modes of operation.

Parameter	Symbol	Value	Unit
Grid			
Rated power	P	8	kW
Grid voltage	V_{LL}	400	V
Grid frequency	f_g	50	Hz
Rated current	$I_{n,rms}$	10	A
LCL-filter			
Inverter side filter inductor	L_i	5.1	mH
Grid side filter inductor	L_g	0.485	mH
Inverter side filter resistance	R_i	0.1	Ω
Inverter side filter resistance	R_g	0.1	Ω
LCL filter capacitor	C_f	2	µF
DC-link			
DC-link voltage	V_{dc}	600	V
DC-link capacitor	C_{dc}	1.3	mF
DC-DC converter			
ESS voltage	V_{ess}	360	V
DC-DC converter inductor	L	14.4	mH
DC-DC converter capacitance	C	10.4	µF
Controller gain			
CCL proportional gain	k_p	276.86	
CCL integral gain	k_i	10000	
VCL proportional gain	$k_{p,v}$	0.5	
VCL integral gain	$k_{i,v}$	10	
PLL proportional gain	$k_{p,pll}$	1.115	
PLL integral gain	$k_{i,pll}$	247.5	
Other			
Switching frequency	f_{sw}	20	kHz
Sampling rate	f_s	1	MHz

Table 5.1: Simulation Model Parameters

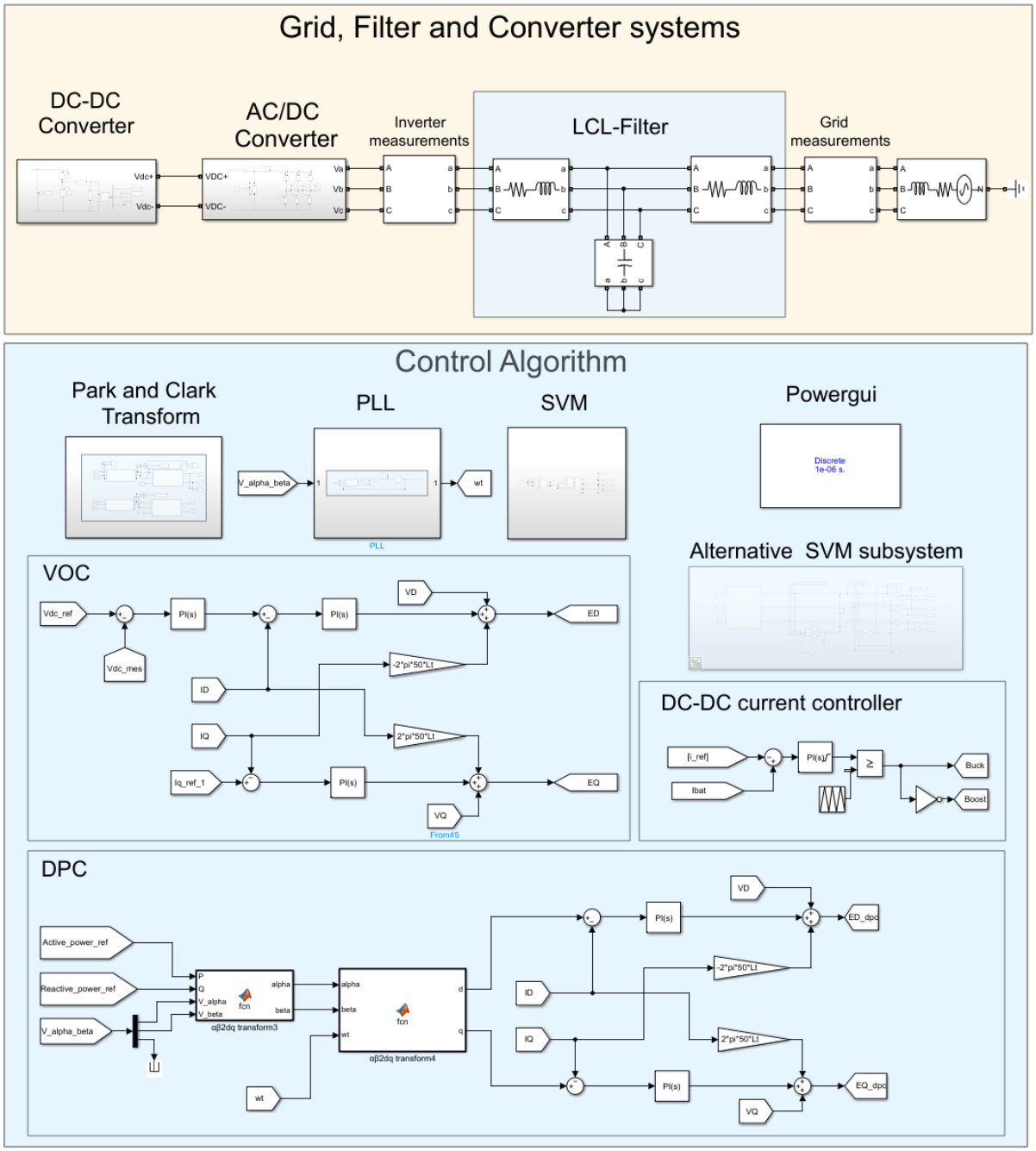


Figure 5.1: Simulation Model Overview.

5.1 Coordinate transformations - Clark and Park

Clarke and Park coordinate transformations have been implemented in Simulink as shown in figure 5.2. The coordinate transformations have been achieved by using two different sets of Matlab functions blocks. The first block labelled as "*abc2alpha_beta*" transforms the *abc* components to the $\alpha\beta$ domain. While the second block labelled as "*ab2dq*" transforms the $\alpha\beta$ components to further to the *dq* domain.

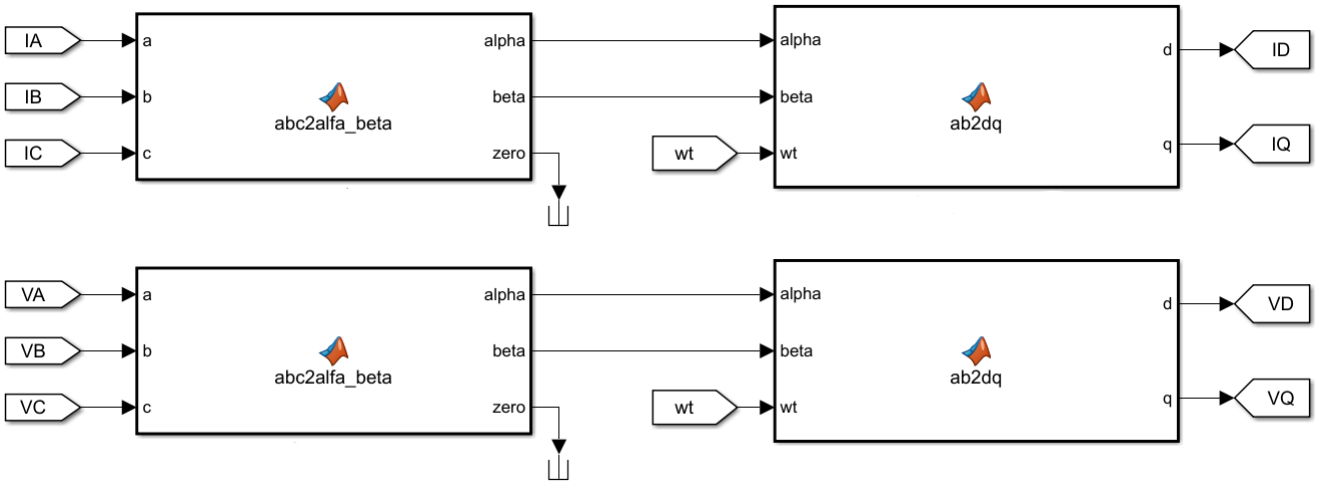
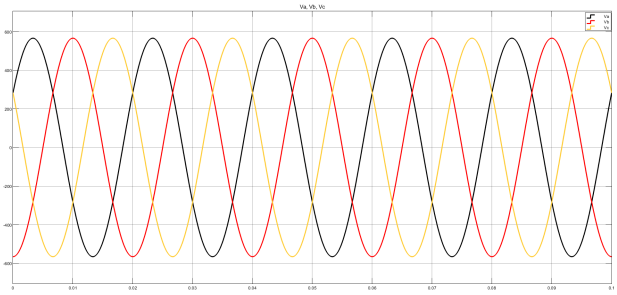
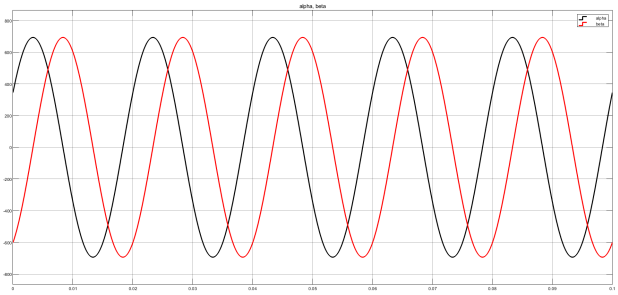


Figure 5.2: Matlab Simulink Coordinate transform blocks

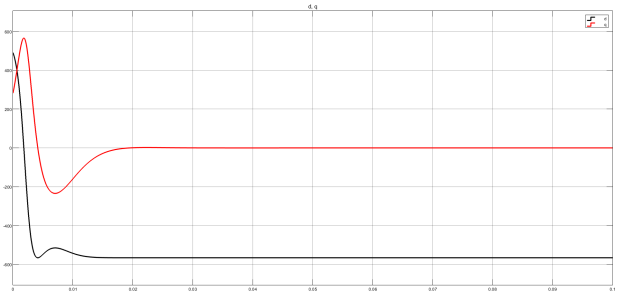
Furthermore the different signals have been illustrated by using a scope block as seen in figure 5.3. The coordinate transform function blocks Matlab code can be found in appendix A.1, this also includes the reverse transformations which are used but not shown in this section.



(a) Three phase abc voltages



(b) $\alpha\beta$ - voltage components

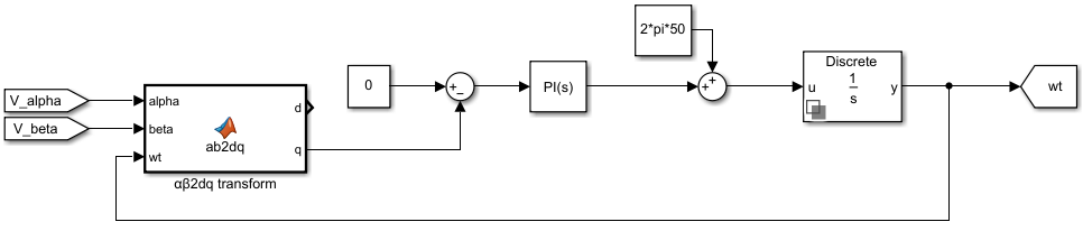


(c) dq - voltage components

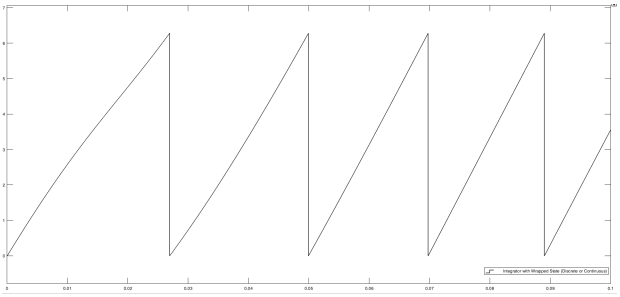
Figure 5.3: Matlab Simulink coordinate transformation signals using Park and Clark.

5.2 Phase Locked Loop - PLL

The Phase Locked Loop structure has been constructed just as described previously in section 3.3, the simulation model of the PLL can be seen in 5.4a. Furthermore the simulated sawtooth waveform using an integrator block with wrap state is shown in 5.4b by using a Simulink scope block.



(a) Phase Locked Loop structure.



(b) Sawtooth waveform of the PLL with wrap state.

Figure 5.4: Matlab Simulink, PLL structure and waveform.

To control the error signal a PI controller has been used, therefore it is important to derive the proportional and integral gain constants $k_{p,pll}$ and $k_{i,pll}$. Both gain constants have been found following the previously presented equations 3.22 to 3.26. By selecting the damping constant to be equal to $\zeta = \frac{1}{\sqrt{2}}$, and the natural frequency $\omega_n = 2\pi 50$, the proportional and integral gain constants are determined in the following equations:

$$k_{p,pll} = \frac{\omega_n^2}{V_{LL}} = 1.115 \tag{5.1}$$

$$k_{i,pll} = \frac{2\zeta\omega_n}{V_{LL}} = 247.5 \tag{5.2}$$

5.3 PWM

The previously described PWM can be achieved using computer simulation software, such as Simulink by comparing control voltages with a triangular waveform signal at the switching frequency to generate the desired gate signals. A modulation structure has been developed to obtain SVPWM. The structure is built up by several subsystem function blocks as shown in figure 5.5, using the theory and methodology shown in section 3.2.2. Each of the Matlab function block's code that has been used, can be found in appendix A.2.

The inputs of the modulation structure are from the outputs of the control structure and undergo a coordinate transform to generate necessary components to produce the IGBT gate signals.

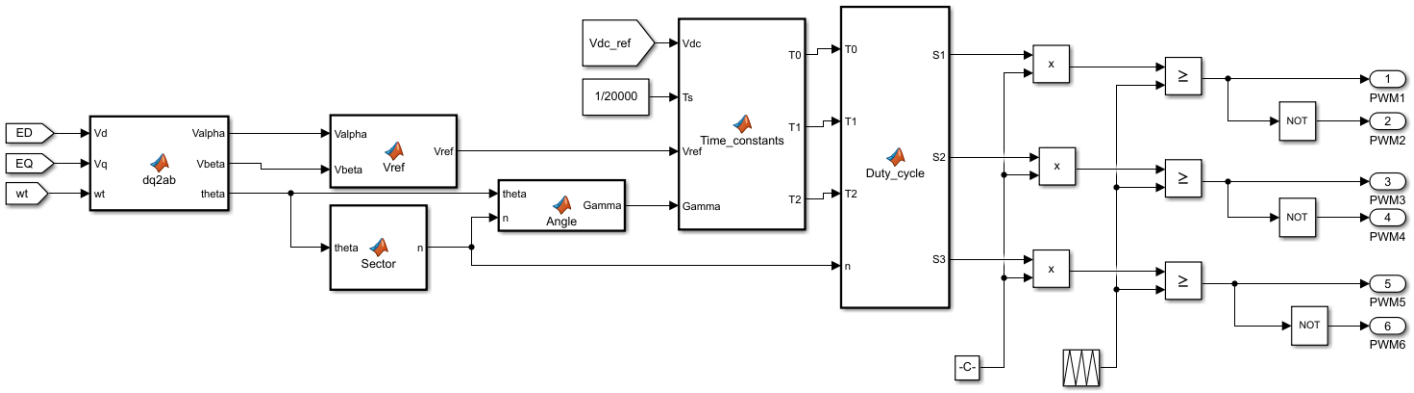


Figure 5.5: Matlab Simulink SVPWM subsystem.

The initial Matlab function block labelled "dq2ab" is simply used for coordinate transformations as shown in previous sections. The $\alpha\beta$ voltage components are necessary to calculate the magnitude of the voltage vector modulus and the angle θ between the adjacent voltage vectors v_k and v_{k+1} as shown previously in figure 3.6, which is calculated respectively as:

$$V_{modulus} = \sqrt{V_\alpha^2 + V_\beta^2} \tag{5.3}$$

$$\theta = \arctan(\frac{V_\beta}{V_\alpha}) \tag{5.4}$$

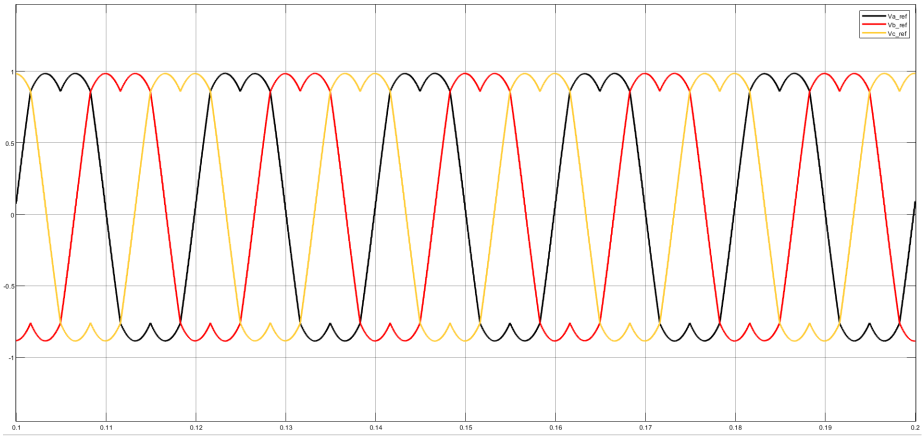
With θ the sector selection block uses series of "if" statements to determine the sector n, with each of the sectors being separated by 60°. The angle function block uses both the determined sector n and θ as inputs to derive the angle termed γ to be between 0°to 60°. Following this the *Time_constant* function block determines the application time ($T0$, $T1$, $T2$) for each of the voltage vectors. $T0$ has been calculated as shown in equation 3.19, while $T1$ and $T2$ are calculated with the following equations based on the theory from section 3.2.2:

$$t_1 = \sqrt{3}T_s\frac{V_{modulus}}{V_{dc}}sin(60-\gamma) \tag{5.5}$$

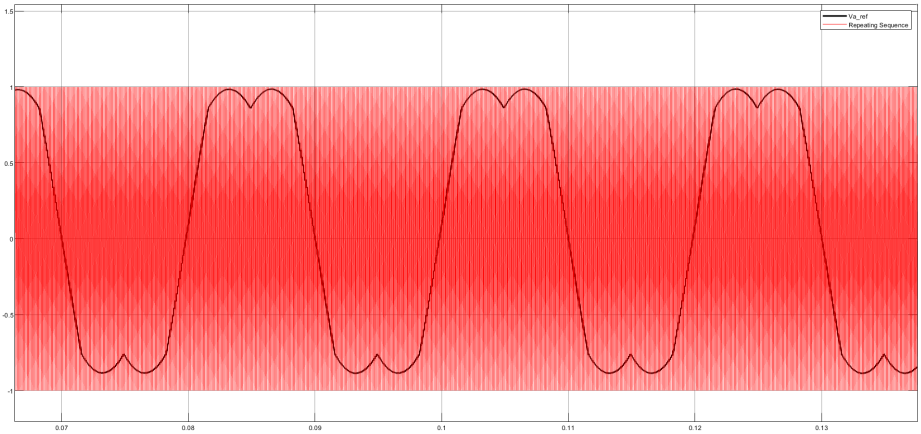
$$t_2 = \sqrt{3}T_s\frac{V_{modulus}}{V_{dc}}sin(\gamma) \tag{5.6}$$

The last function block termed *Duty_cycle* uses the derived time constants ($T0$, $T1$, $T2$)

as inputs to determine the switching time signal for each of the upper legs of the inverter termed $S1$, $S2$ and $S3$. Following this a gain constant depending on the sampling time T_s is multiplied to each of the switching time signals to get a signal between one and negative one. Finally the signals are compared with a sawtooth waveform which oscillates at frequency of 20kHz, thereby generating each of the gate signals of the IGBTs of the inverter. The resulting waveforms from the SVPWM structure and triangular waveform comparison has been illustrated in figure 5.6.



(a) SVPWM reference control values S1, S2 and S3.



(b) SVPWM reference control value S1 compared to triangular waveform.

Figure 5.6: SVPWM modulation structures control signals and triangular waveform comparison using the following modulation structure shown in figure 5.5.

An alternative method of obtaining SVPWM has also been developed, and can be seen in figure 5.7. furthermore with a small alteration it is possible to obtain SPWM, by comparing the *abc* input reference voltages directly with the triangular waveform. The control voltage components from 5.7 have been measured using the MATLAB Simulink scope block and are illustrated in the following figures of this section. The sinusoidal control voltage components can be seen in Figure 5.8a.

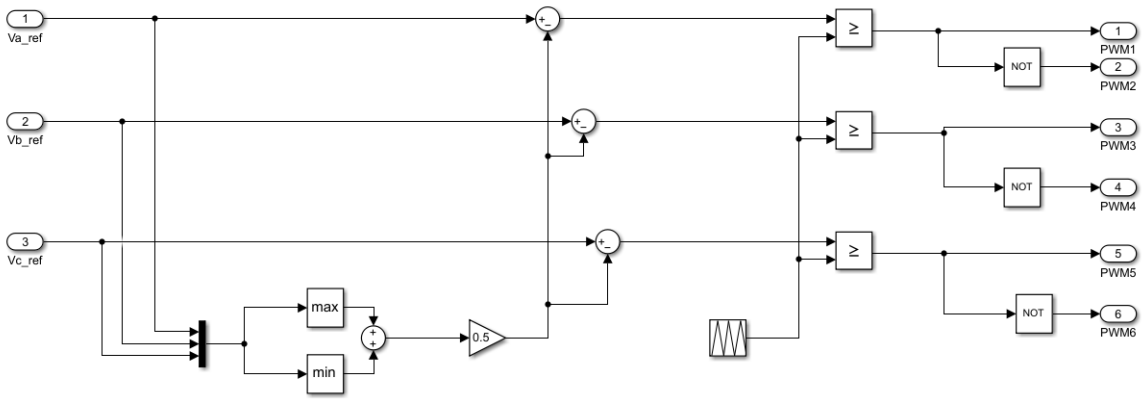


Figure 5.7: Matlab Simulink modulation structure

In SVPWM the control voltages do not have a pure sinusoidal shape as is used in the more common SPWM, the SVPWM waveform can be seen in figure 5.8b. Synthesizing an average space vector with the phase voltages (v_a, v_b, v_c) can be done by expressing the control voltages in terms of the phase voltages. where the control voltage can be expressed as a ratio of the triangular waveform amplitude signal as follows [31]:

$$\frac{V_{control,a}}{V_{tri}} = \frac{v_a - v_k}{V_{dc}/2} \tag{5.7}$$

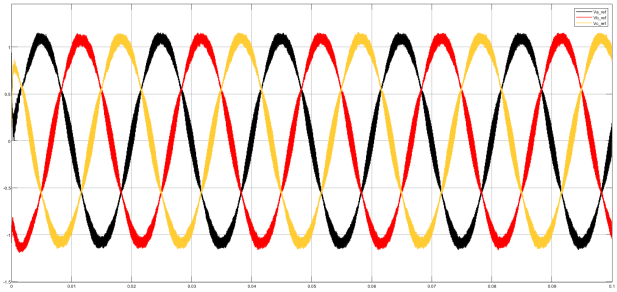
$$\frac{V_{control,b}}{V_{tri}} = \frac{v_b - v_k}{V_{dc}/2} \tag{5.8}$$

$$\frac{V_{control,c}}{V_{tri}} = \frac{v_c - v_k}{V_{dc}/2} \tag{5.9}$$

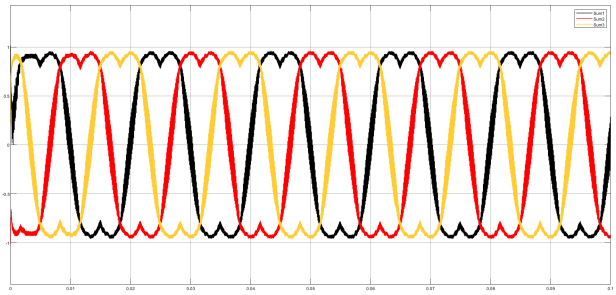
where the variable v_k can be defined as:

$$V_k = \frac{max(v_a, v_b, v_c) + min(v_a, v_b, v_c)}{2} \tag{5.10}$$

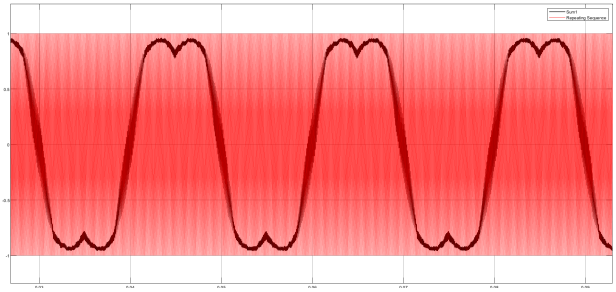
This method of obtaining the SVPWM is different to the methodology of what has been described in section 3.2.2. However we achieve the desired modulation using this method with much more simplicity with the added benefit of a lower compilation time when simulating the system. Unlike the previously described methodology this method does not use any Matlab function blocks which during testing, have shown to noticeably slow down the simulation time.



(a) *abc* reference control values



(b) SVPWM reference control values



(c) SVPWM signal compared with repeating triangular waveform

Figure 5.8: PWM structures control signals and triangular waveform comparison.

5.4 PI Controller

A PI controller has been used for the sake of reducing the error signals and to produce the desired output response, while retaining a simple design as shown in 5.9. The PI controller can be seen being used to control several parts of the system such as the PLL and the decoupled control loops. The previously described PLL control structure utilizes one of such controllers, as can be seen from figure 5.4a. The decoupled controller uses a total of three PI regulators: The inner CCL contains two of such PI regulators, while the outer VCL uses one. However the PI blocks from the Simulink library work just as well as the design shown in figure 5.9, and have been used as well. The gain constants k_p and k_i for the CCL along with their equations using MO have been defined in table 5.2, following the methodology presented in section 4.4. The gain parameters for the VCL, however have been found using a practical approach of trial and error.

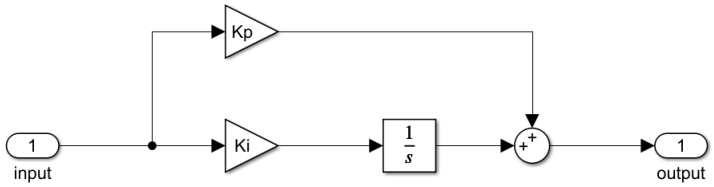


Figure 5.9: Simulink block diagram of the PI regulator.

Parameter	Equation	Value
k_p	$\frac{T_{LCL}R_t}{2T_a}$	55.37
k_i	$\frac{k_p}{T_i}$	4000

Table 5.2: PI controller gain equations and parameters using MO.

5.5 Converter Control loops

Voltage Oriented Control - VOC

The voltage oriented control loops as seen in figure 5.10, has been developed following the block design shown in figure 3.11. The developed VOC is based on the presented theory in section 3.4.1. By using VOC the control system assures that the dc-link voltage remains within desirable levels. Which contains a VCL using a reference voltage Vdc_ref to generate the required d-axis current $I_{d,ref}$ for the CCL. The q-axis reference current $I_{q,ref}$ is set to zero, as is common practice to achieve UPF.

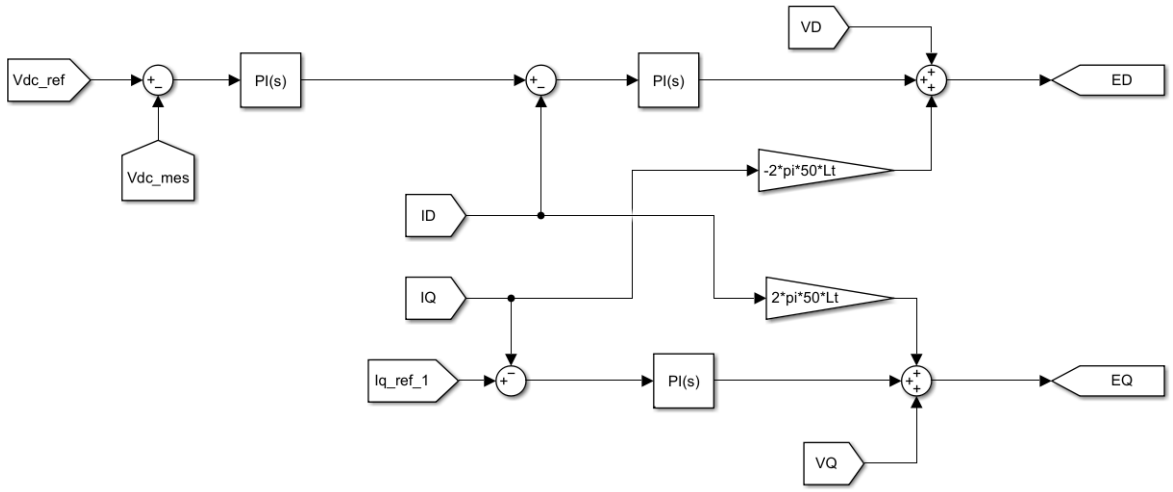


Figure 5.10: Block diagram of the VOC, containing both the VCL and the CCL.

The DC-DC converter is controlled using a CCL which can be found in figure 5.11.

In order to generate the desirable current value an input reference current i_{ref} is compared with the battery current I_{bat}. The output difference goes through a PI controller which eliminates the error. The output of the controller is compared with a triangular waveform,thereby generating the gate signals of the DC-DC converter switches.

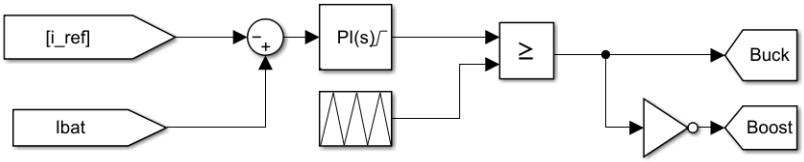


Figure 5.11: Block diagram of the DC-DC converter control system, using a simplified CCL.

Direct Power Control - DPC

A method of controlling the GTI by means of DPC has been developed based on the theory provided in section 3.4.2. The block diagram has been constructed as shown in figure 5.12, with the design being based around the previously shown figure 3.12. The method of controlling the DPC is by selecting the desired active and reactive reference power P and Q respectively. Where the reactive power Q is commonly set to zero, thereby attaining the often desirable UPF. The active and reactive reference values, in addition to the measured $\alpha\beta$-domain voltages are feed into a transformation block which produces the $\alpha\beta$-domain reference currents. The Matlab transformation block has been built using the previously shown equation 3.43. The reference currents are then transformed into their receptive dq-axis components and input into the same CCL which has been explained in section 3.4.1. The Matlab code of both the transformation blocks used in 5.12can be found in appendix A.1.

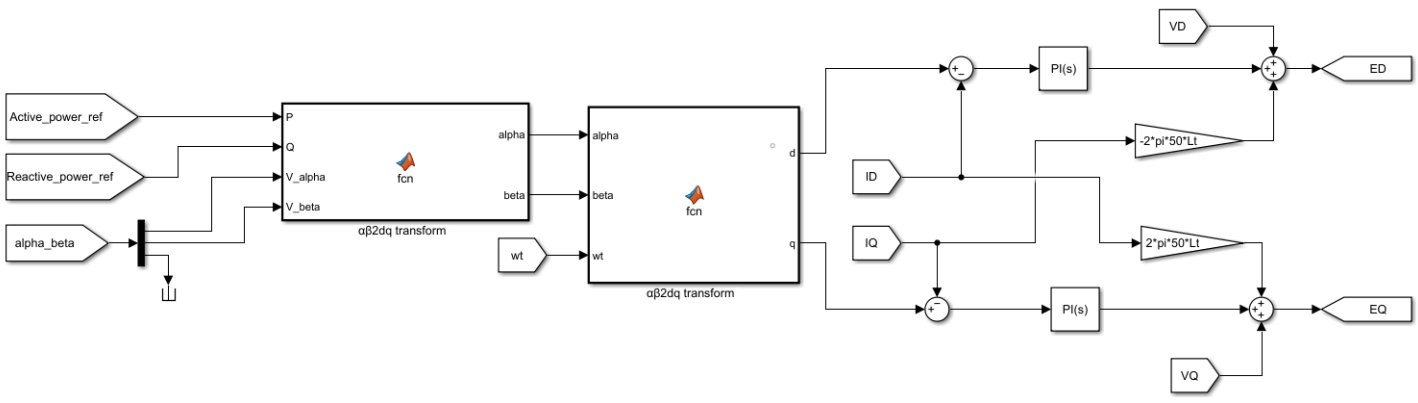


Figure 5.12: Inverter DPC with CCL

5.6 Simulation Tests and results

An analysis of the harmonics is carried out on the grid currents by comparing the Total harmonic distortion using the Fast Fourier Transform (FFT) analysis tool, which can be found in the "Powergui" block of Matlab Simulink. The purpose of this section is to validate the models used to develop the control strategies that have been presented from the previous chapters and sections. The system parameters that have been used during the tests conducted in this section have been giving by table 5.1.

5.6.1 Initial Simulation tests

Initially when the simulation model was created a dc-source was used instead of the battery model as the load/supply. Which was done in order to determine the overall function of the control system over the GTI when the dc-link was at an ideal state. Furthermore due to the dc-link voltage remaining constant in the desired voltage value, the VCL in the VOC was thereby not required. This subsection will present the simulation results when the dq-axis reference current components are controlled directly into the CCL and the DPC method controlling the active and reactive reference power, while using an ideal dc-source. The resulting simulation tests have been separated into the following two sub sections. Where the initial simulated test will be using inverting operation, while the second test which will use the DPC method will be rectifying to show that the converter is fully capable of operating with bidirectional power flow.

Test 1: Current control

This test has been conducted by initially setting a desired d-axis reference current $i_{d,ref}$ value and increasing it incrementally every second by a value of two. The initial $i_{d,ref}$ is set to be equal to -10 while the q-axis reference current $i_{q,ref}$ is set to zero throughout the entire simulation. The simulation runtime T_{sim} lasts for a total of 5 seconds, thereby the reference current $i_{d,ref}$ decreases from a value of -10 to -18 throughout this simulated test. Table 5.3 has been provided to present the reference current values during the simulated runtime, as well as the resulting THD value of the grid phase current during the given time frame. The control method used is an alteration of the VOC shown in figure 5.10, where the voltage loop has been removed and the d-axis reference current is controlled directly.

T_{sim} [s]	$I_{d,ref}$ [A]	$I_{q,ref}$ [A]	THD [%]
<1.0	-10	0	2.02
<2.0	-12	0	1.68
<3.0	-14	0	1.52
<4.0	-16	0	1.26
<5.0	-18	0	1.13

Table 5.3: Simulation reference values and THD based on simulation run time.

The resulting step-change of the d-axis reference current along with the measured dq current components during the simulation, can be seen in figure 5.13. This figure indicates that the measured d-axis current $I_{d,measured}$ is in fact keeping up with the desired reference signal with a relatively fast dynamic response time, even when the step changes are initiated every second. Furthermore it can be observed that the measured q-axis current $I_{q,measured}$, is being held at a value close to zero with only slight deviations during the initial transient time period whenever the reference current value has a new step input.

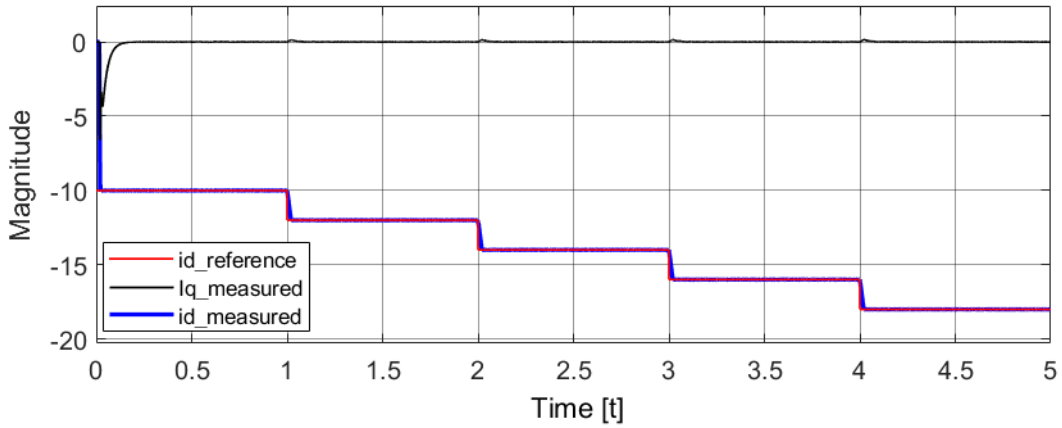


Figure 5.13: d-axis reference current [red], d-axis current measurement [blue] and q-axis current measurement [black].

The resulting grid phase current and voltage are both shown in figure 5.14. Where the signal scope time frame has been restricted from 0.1 to 0.2 seconds and the phase voltage has been scaled down to 10% of its size, in order to display the waveforms in a more visually appealing manner. In addition to showing that the PLL has extracted the grid phase angle with more visual clarity and that the phase current is properly aligned with the phase voltage.

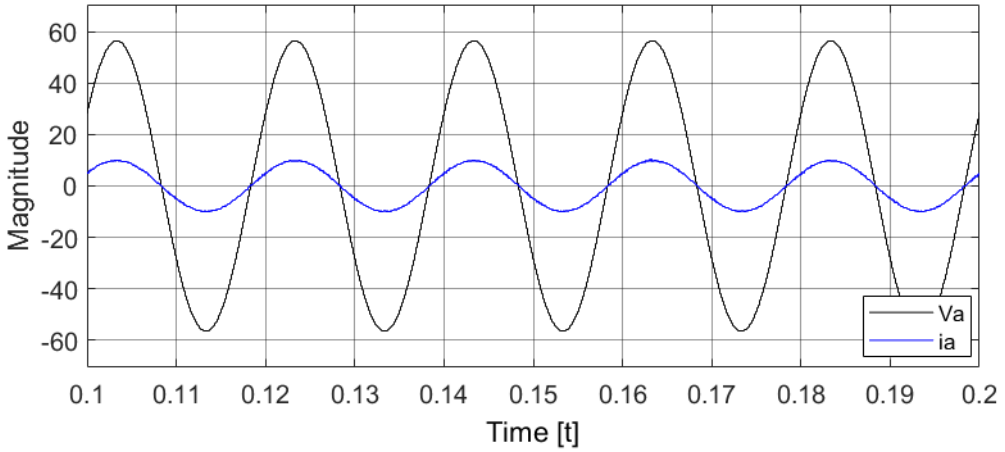


Figure 5.14: Scaled down phase voltage [black] and respective current [blue].

A comparison of the phase current before and after going through the LCL-filtering between an arbitrary time of 0.5 to 0.6 seconds, can be found in figure 5.15. The resulting FFT analysis of the variating grid side phase current waveforms are provided in appendix B.1.

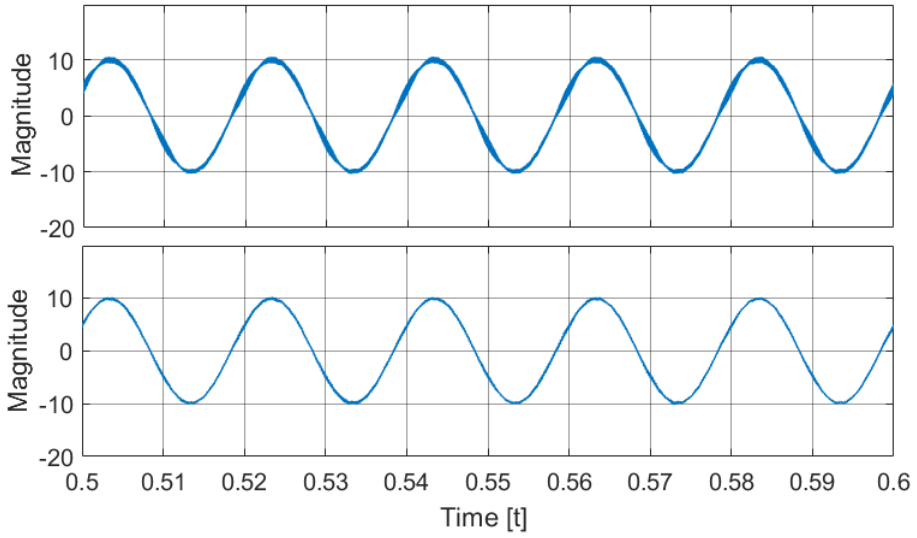


Figure 5.15: Phase current waveform comparison, inverter side current [upper], grid side current [lower].

Test 2: Direct power control

In this test the GTI is controlled by using the DPC method. Where the control system which has been presented in figure 5.12 is used. Throughout this test the reactive power reference Q_{ref} has been set to zero in an attempt to achieve UPF, while the active power reference P_{ref} will be increased incrementally every second. To present the parameters of this test a table showing the simulation time frame T_{sim}, Active power reference P_{ref},

reactive power reference Q_{ref} and the respective THD percentage during each time frame can be seen in table 5.4

T_{sim} [s]	P_{ref} [A]	Q_{ref} [A]	THD [%]
<1.0	-8	0	2.41
<2.0	-10	0	2.02
<3.0	-12	0	1.89
<4.0	-14	0	1.98
<5.0	-16	0	1.79

Table 5.4: Simulation reference values and THD based on simulation run time.

The initial value of the P_{ref} has been set to $-8\ kW$ with the simulation runtime lasting a total of five seconds, following the initial input the active power has a step input applied every second throughout the simulated test. The resulting step-change of the reference and measured active power, along with the measured reactive power can be seen in figure 5.16. The simulated test shows that the measured values are keeping up with the given reference value adequately, with only slight deviations during transient time periods lasting only a fraction of a second.

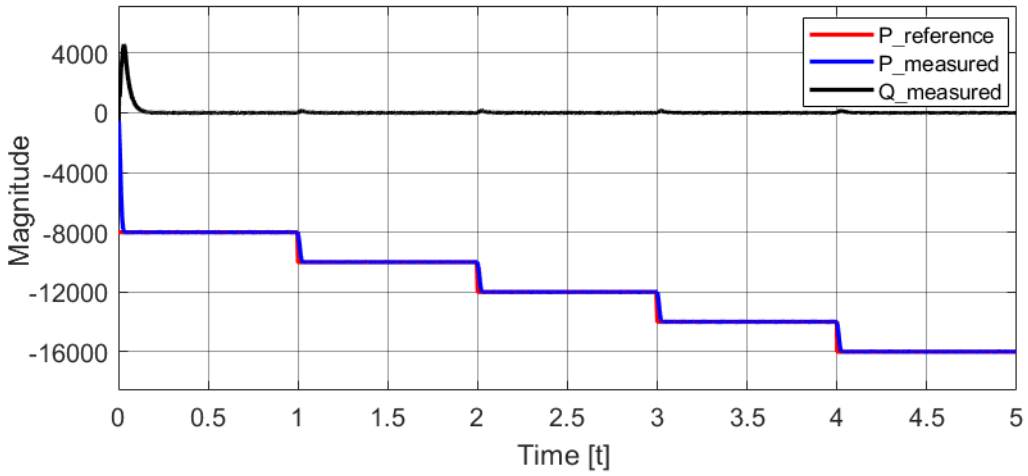


Figure 5.16: Active reference power [red], measured active power [blue] and measured reactive power [black].

Similar to the previous test the resulting the resulting phase current and voltage has been illustrated in figure 5.17. Where the signal scope time frame has been restricted from 0.7 to 0.8 seconds and the phase voltage has been scaled down to 10% of its size, for the same reasons mentioned in the previous test.

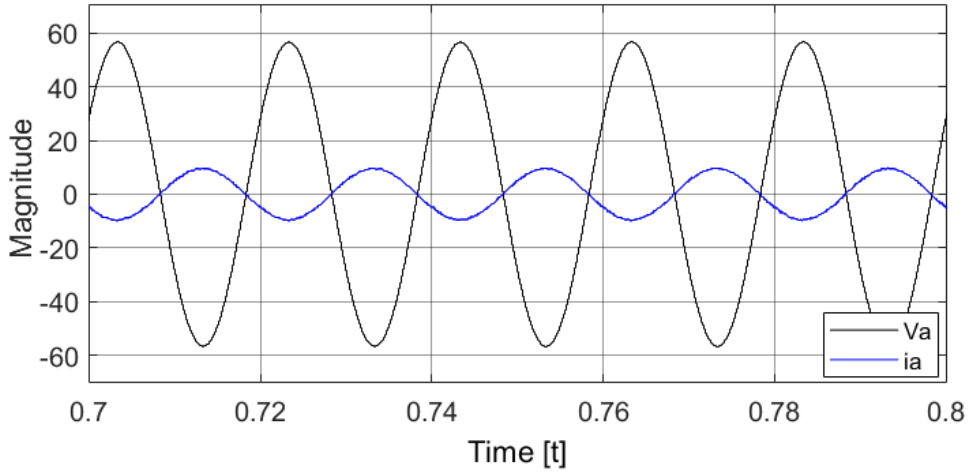


Figure 5.17: Phase voltage [black] and respective phase current [blue], with scaled down voltage value.

The inverter side phase current and grid side phase current comparison showing the effects of the LCL-filter between an arbitrary time of 0.5 to 0.6 seconds, can be found in figure 5.18. The resulting FFT analysis of the variating grid side phase current waveforms while using DPC has been provided in appendix B.2. This analysis shows that the THD remains well below 5% , and is therefore within the standards required by IEEE.

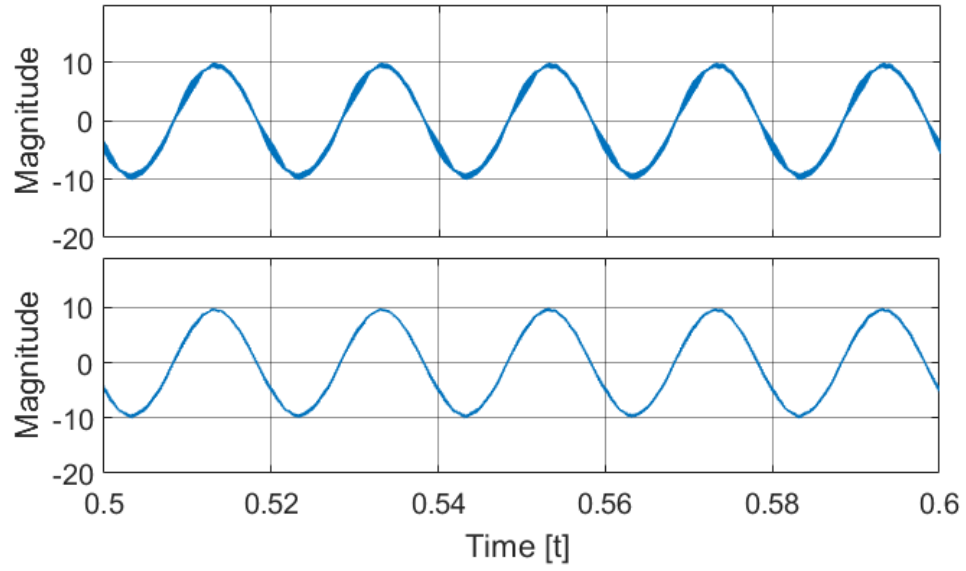


Figure 5.18: Phase current waveform comparison, inverter side current [upper], grid side current [lower].

5.6.2 Inverter Operation

This section presents the results from controlling the simulation system presented in figure 5.1 through inversion. While using the VOC strategy presented in figure 5.10 and

the DC-DC controller presented in figure 5.11. In the following test, a step input will be applied to the DC-DC converters reference current every second for a total duration of five seconds. Which means that the DC current will see a gradual increase a total of 4 times from its initial value over the course of the simulation run time. The battery model of the simulation, consists of a lead acid battery from the Simulink library. Although the battery model presented in theoretical framework section 2.5 was considered and should work adequately. The pre-made battery block from the Simulink library offers more accuracy and functions, therefore the Simulink block was selected. The reference dc-link voltage has been set to $V_{dc} = 600\ V$. The dq-axis reference currents values with respect to simulation time, and the measured THD of the grid side phase current has been given in table 5.5. Where T_{sim} represents the simulation time, $I_{d,ref}$ and $I_{q,ref}$ represents the respective dq reference currents.

T_{sim} [s]	$I_{d,ref}$ [A]	$I_{q,ref}$ [A]	THD [%]
<1.0	-8	0	2.63
<2.0	-10	0	2.07
<3.0	-12	0	1.67
<4.0	-14	0	1.42
<5.0	-16	0	1.32

Table 5.5: Simulation reference values and THD based on simulation run time.

The comparison of the d-axis reference current and the measured dq-axis currents throughout the simulation run time can be seen in figure 5.19. Showing that after a transient response the system obtains the desired values for both dq current components. Where the q-axis current is set to zero to achieve UPF, and a step input is applied leading to the incremental decrease of the d-axis current per second with a value of two. The THD values as shown in appendix B.3 or in 5.5, indicate that the systems THD level is well within the scope of IEEEs required standard of less than 5%.

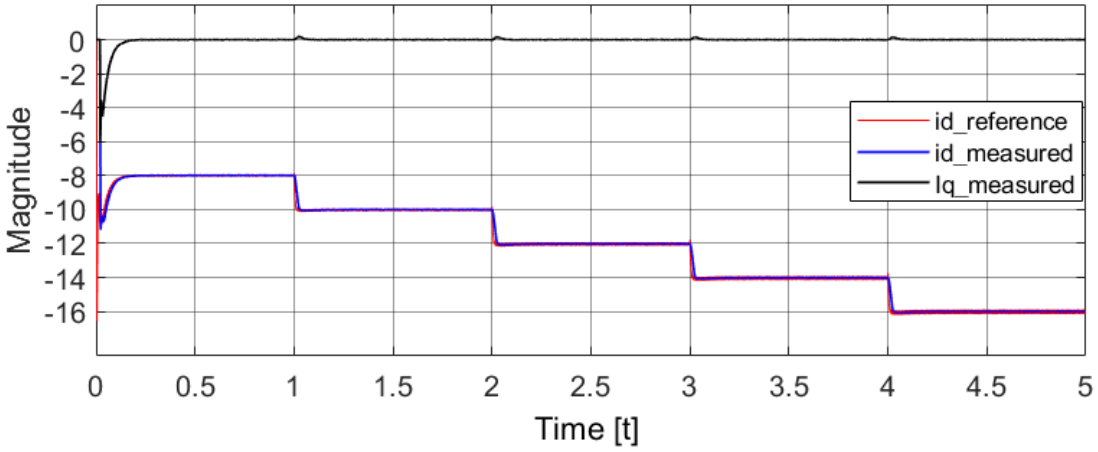


Figure 5.19: d-axis reference current [red], d-axis current measurement [blue] and q-axis current measurement [black].

The LCL-filters effect on the grid current can be seen graphically in figure 5.20, which compares both the converter side- and the grid side phase current.Where the above waveform represents the converter side phase current, whilst the lower waveform represents the respective grid side phase current. It can be visually observed that the THD levels of the phase current is reduced, the FFT analysis comparison indicates that the filter reduces the THD by a significant amount.

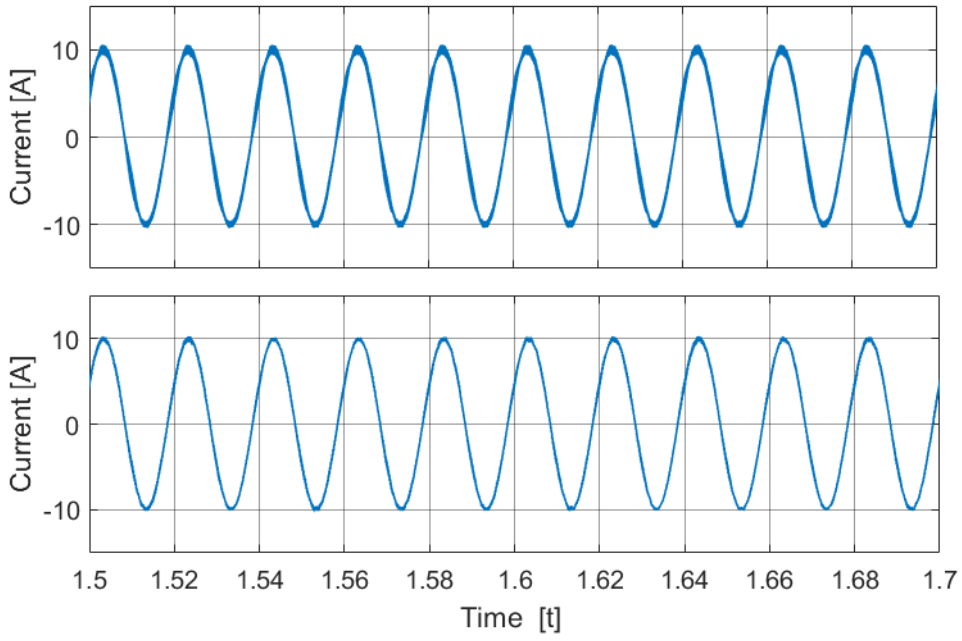


Figure 5.20: Phase current waveform comparison, inverter side current [upper], grid side current [lower].

The phase current as compared to its respective phase voltage can be seen in figure 5.21. Where the signal scope time frame has been restricted within 0.2 seconds at an arbitrary

time and the phase voltage has been scaled down to 10% of its size, for visual clarity. It can be visually observed that the grid phase angle extraction of the PLL is successful in showing no deviation from the intended angle, by observing the phase current and voltage superimposed on each other.

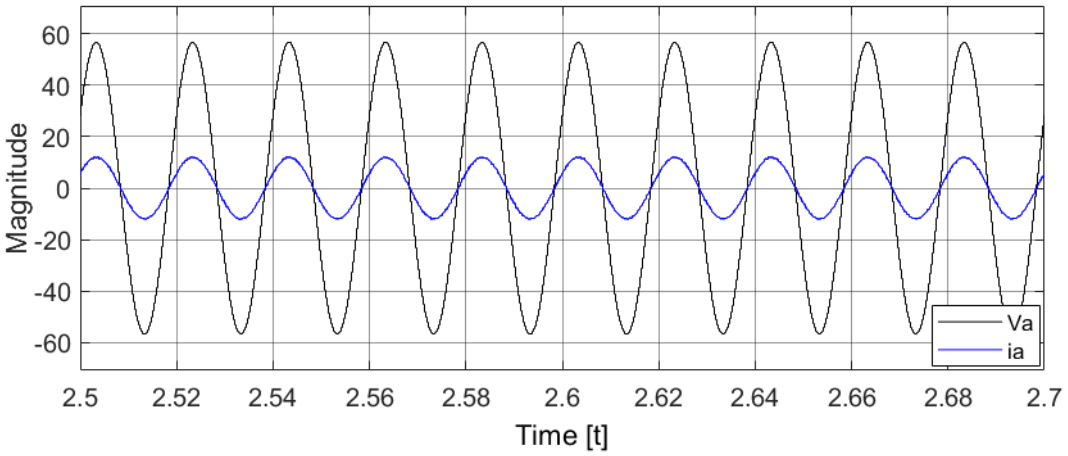


Figure 5.21: Phase voltage [black] and respective phase current [blue], with scaled down voltage value.

The gradual increase of the active power as the variable reference current changes during the simulated runtime can be seen in figure 5.22. Along with the reactive power going towards zero during steady state operation, having only deviations during the transient time period when the simulation is initially ran. With addition to deviations within a slight time period when a step change to the reference current is applied per second.

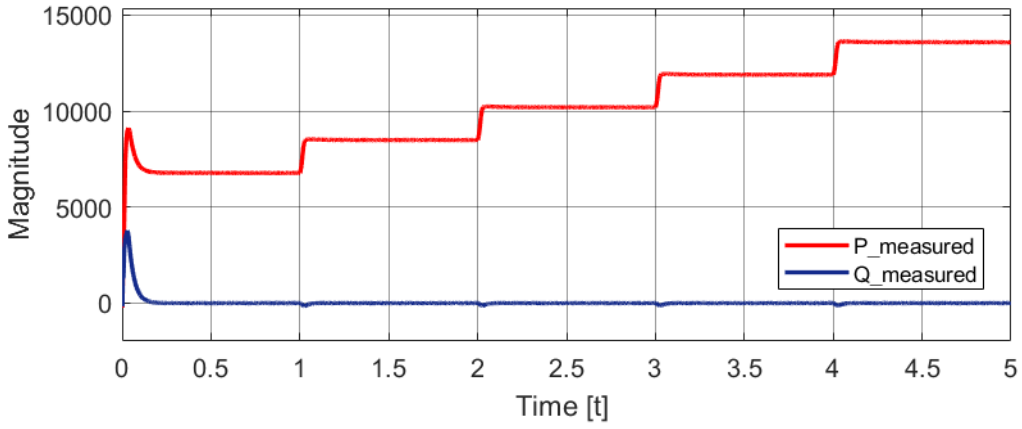


Figure 5.22: Active reference power [red], measured active power [blue] and measured reactive power [black].

5.6.3 Rectifier Operation

This section presents the results from controlling the simulation system presented in figure 5.1 through rectification. Which in essence is similar to the test shown in the previous section, where the same components and control strategy will be utilized. With the only difference being the input reference current of the DC-DC controller. In this test a step input to the reference current will be conducted every second, leading to the incremental increase of the d-axis current thereby the phase currents every second. The dc voltage reference has been set to $V_{dc} = 600\ V$, this reference value is fed to the VCL thereby regulating the dc-link voltage. Just as in every test which has been conducted previously the q-axis reference current $I_{q,ref}$ has been set to zero. A table showing the simulation runtime T_{sim}, the respective dq reference current values $I_{d,ref}$, $I_{q,ref}$ as well as the resulting THD, has been presented in table 5.6.

T_{sim} [s]	$I_{d,ref}$ [A]	$I_{q,ref}$ [A]	THD [%]
<1.0	8	0	2.90
<2.0	10	0	2.35
<3.0	12	0	2.04
<4.0	14	0	1.98
<5.0	16	0	1.95

Table 5.6: Simulation reference values and THD based on simulation run time.

The comparison of the d-axis reference current and the measured dq-axis currents during the simulated runtime is shown in figure 5.23. Which shows the resulting measured current waveforms are achieving the desired result during steady state operation. The only graphically noticeable deviations are during the transient time periods which only last for a slight time frame less than a millisecond. Overall the system is shown to be able to keep up with the variable reference current during the simulated run time, with a fast and dynamic response time.

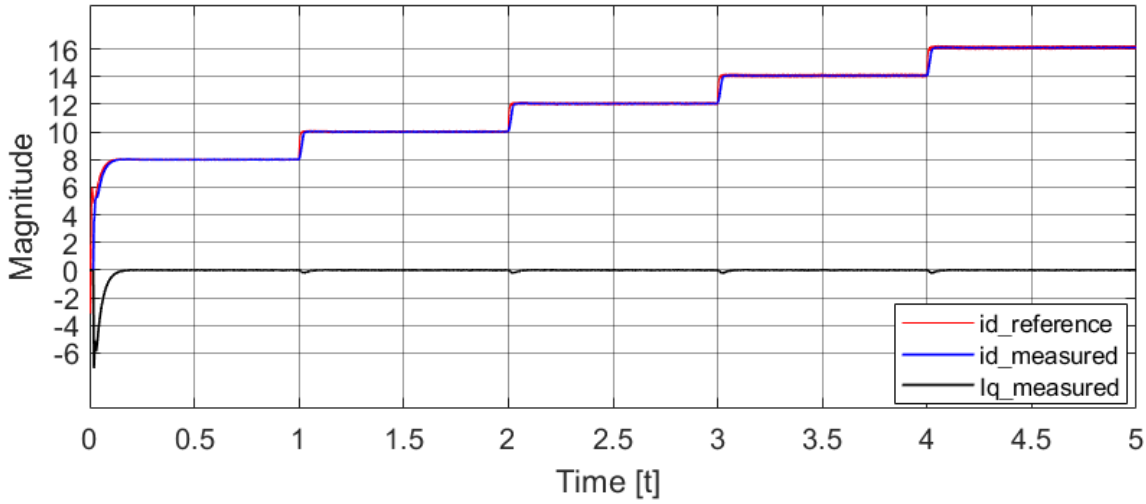


Figure 5.23: d-axis reference current [red], d-axis current measurement [blue] and q-axis current measurement [black].

The grid phase current and its respective phase voltage from an arbitrarily chosen time frame within the simulated runtime can be seen in figure 5.24, where the voltage waveform has been scaled down to 10% of its original size. The resulting THD values of the grid phase current can be seen in appendix B.4 or in table 5.6. The results indicate that the systems THD level remains below 5% as is required by IEEE standards for grid tied applications.

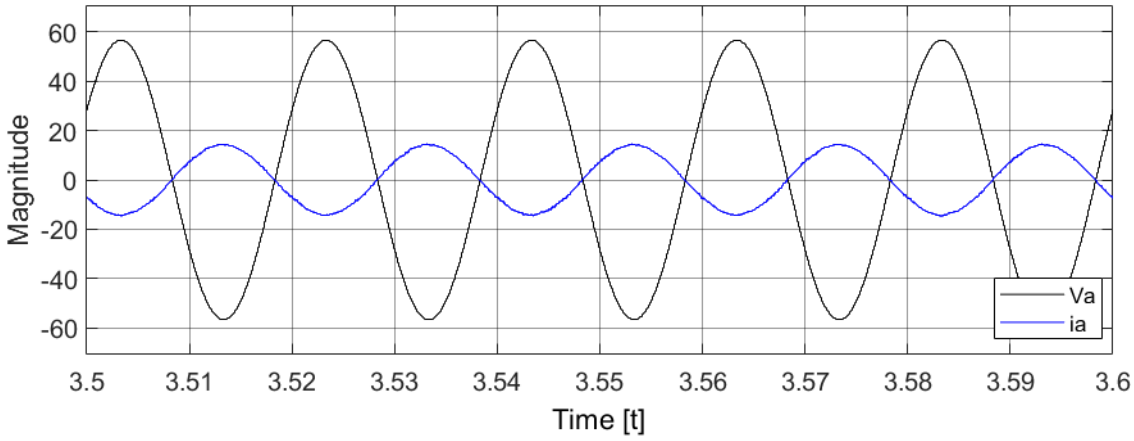


Figure 5.24: Phase voltage [black] and respective phase current [blue], with scaled down voltage value.

The measured active- and reactive power during the simulated runtime has been provided in figure 5.25. Showing that the reactive power is regulated to be approximately zero which is desired for obtaining UPF, during steady state operation. With only minor deviations over the course of a small transient time frame during every step change input.

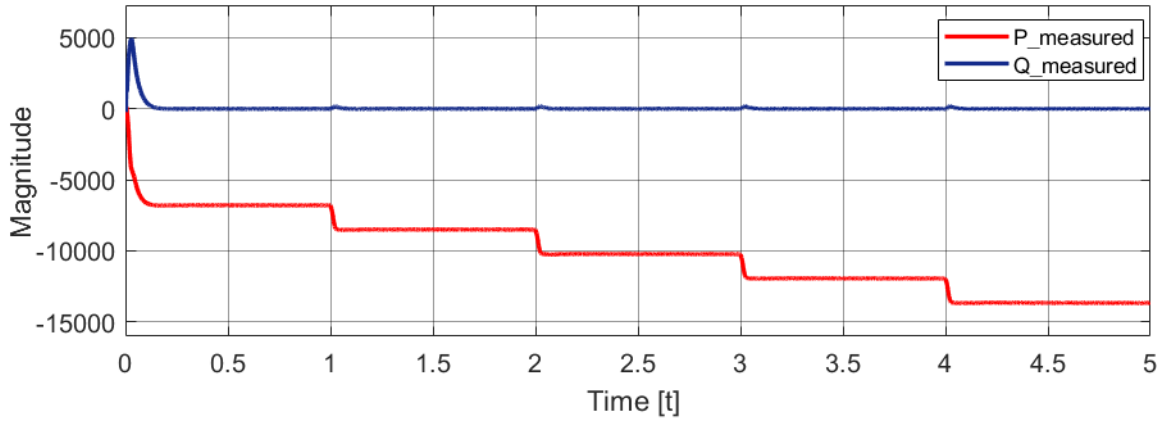


Figure 5.25: Active reference power [red], measured active power [blue] and measured reactive power [black].

5.6.4 Bidirectional Operation

This section aims to showcase the bidirectional capability of the converter system, by allowing the grid connected converter to operate in inverting mode followed by rectifying mode and then finally back to inversion. The simulated runtime for this test has been reduced down to 0.6 seconds, with the variable change to the reference being input every 0.2 seconds changing the operational mode. A table showing each operation mode, simulated time frame T_{sim}, dq-axis reference current components and the resulting THD value can be seen in 5.7. The test has shown that the THD during each mode of operation is within the required IEEE standard of 5% or less.

Operation	T_{sim} [s]	$I_{d,ref}$ [A]	$I_{q,ref}$ [A]	THD [%]
Inverting	<0.2	-10	0	2.22
Rectifying	<0.4	10	0	2.57
Inverting	<0.6	-10	0	2.08

Table 5.7: Simulation reference values and THD based on simulation run time.

A figure showing the comparison of the d-axis reference current with the measured value throughout the simulated runtime has been provided in figure 5.26. The measured value of the q-axis current has also been included and just as in every previous test the q-axis reference current has been set to zero to reach UPF. The resulting wave form indicates that the converter system has the ability to operate in bidirectional modes. While also doing so with smooth transitions from operational mode without causing significant instability, showing only deviations during transient time periods lasting barely a mil-

lisecond. Both the active and reactive power flow during the simulated runtime has been measured, and is provided in figure 5.27.

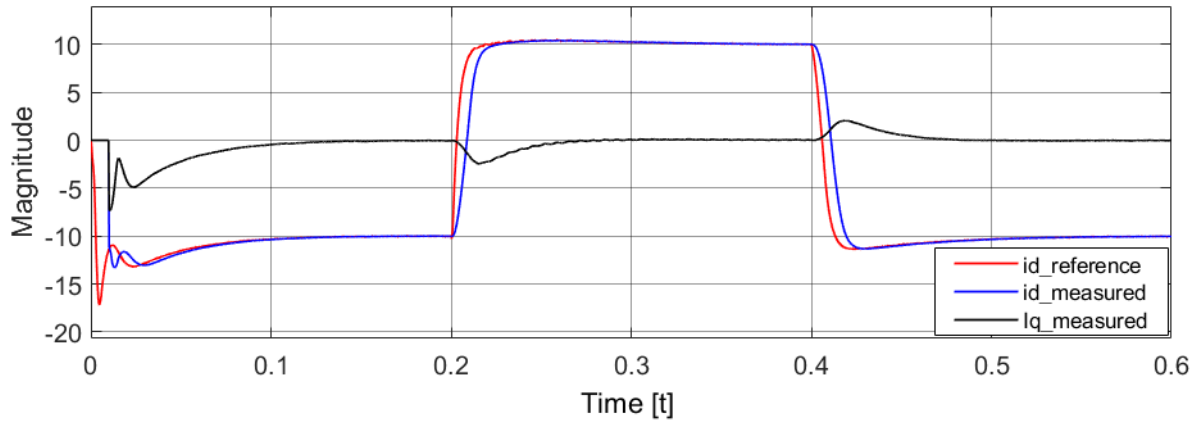


Figure 5.26: d-axis reference current [red], d-axis current measurement [blue] and q-axis current measurement [black].

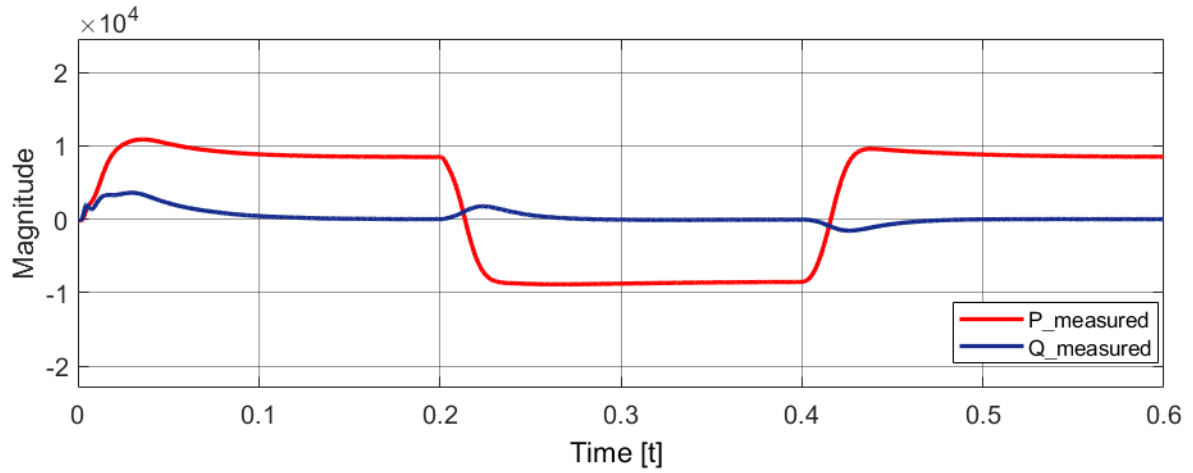


Figure 5.27: Active power [red], reactive power [blue].

The grid side phase current has been compared to its respective phase voltage which is provided in figure 5.28, it should be noted that the phase voltage has been reduced to 10% of its original size when measuring the scope. As mentioned in table 5.7 the system is initially running in inversion mode, the PF of the system when it has stabilized should be close to 1. The PF of the system can be deduced visually by observing the phase difference of the grid side current compared to the respective phase voltage. While the inversion is being maintained the phase difference between the current and voltage should be close to zero. However when the simulated time frame reaches to 0.2 seconds a step signal is input to the reference signal, thereby the power flow changes direction leading to the phase current having a 90°difference when compared to the voltage. In this case the PF is equal to -1, thus the grid is in a state of where it is feeding power to the BESS.

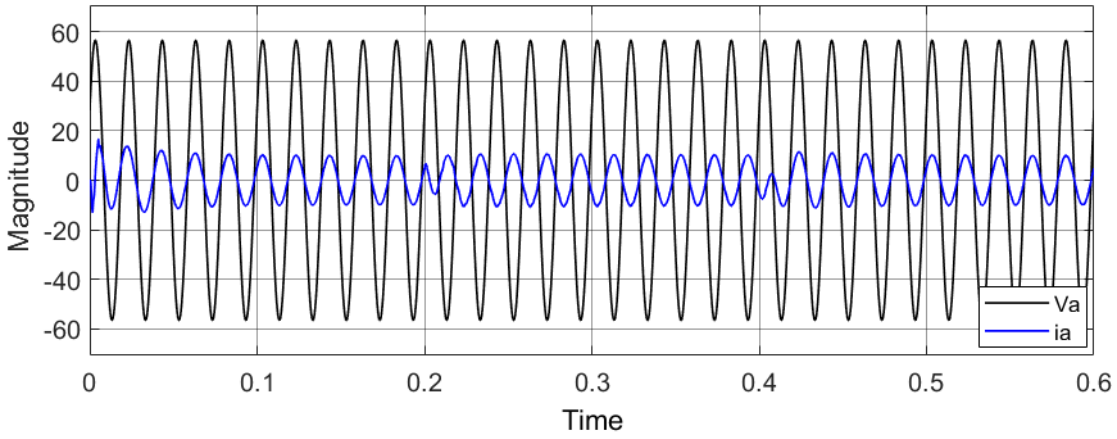


Figure 5.28: Phase voltage [black] and respective phase current [blue], with scaled down voltage value.

Chapter 6

Hardware and Prototype PCB circuits

In this chapter the physical hardware components that are to be used for the prototype GTI will be presented as well as a proper explanation in the selection of hardware and development of the circuit boards.

All circuit boards for the prototype have been designed for this thesis using the software *Kicad*. This software allows for the user to draw both schematics and PCB design. The schematics drawings can be directly incorporated to the PCB, making the process of developing a circuit board very suitable for electronic projects. Additionally it is possible to display the PCB in a 3D setting should the required footprints be available for the board, giving further insight too how the board will look once developed physically.

It should be stated that before designing the PCB boards for this thesis, the circuits where tested using breadboards with the intended design. It should also be noted that i have had next to no experience in circuit board design, other than simple circuits used for my bachelor thesis. Which is why the boards may be oversized to simplify the process of soldering on the components and compensating for the lack of experience. With the possibility of some necessary details being overlooked due to this lack experience.

Furthermore considerable time has been spent to properly learn and develop the circuit boards, with several design iterations which have been made prior to the completion of the designed Printed Circuit Board (PCB) boards that will be shown in this chapter. All things considered the designed circuit boards should be considered as test modules that could possibly contain some form of error or is still in the development/prototype phase. Additionally after the completion of the initial designed circuits for both the current and voltage measurement modules, there was a shortage of the necessary Microcontroller

(MCU) cards making the originally intended modules for this thesis no-longer viable. Nevertheless the originally intended modules will be presented in this chapter grouped together in one section and subsequent subsections. There has been an attempt at solving the lack of components purchasable by using available components found in the laboratory facilities, thus alternative modules have been designed. However there are still lacking components for the prototype to function such as the filtering and BESS.

6.1 Microcontroller unit - MCU

The MCU intended to be used in this thesis is the STM32L476RG chosen for its ultra low power feature. In addition to being based on the high performance Arm-Cortex-M4 32-bit RISC core, operating at a frequency of up to 80MHz. STM32 Nucleo boards are considerably affordable and are produced by STMicroelectronics as a development platform. These boards are aimed at rapid prototyping, allowing for testing of new ideas with relative ease. There are variations on the boards based on the size and the number of available pins on the unit, such as the Nucleo-32 (32 pins) and the Nucleo-64 (64 pins) [49].

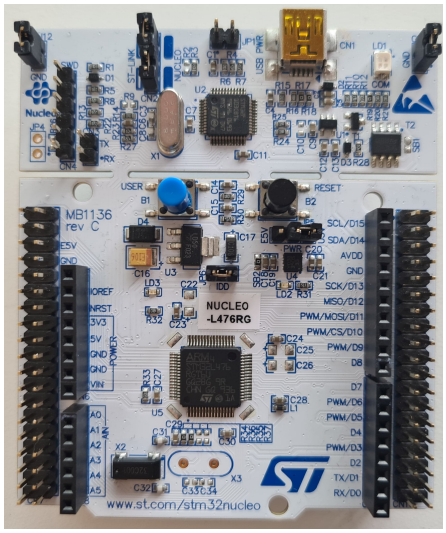


Figure 6.1: Power module - PCB

These boards are intended to be used with their specific software such as: $STM32CubeIDE$ and $STM32CubeMX$. Where the $STM32CubeIDE$ is an advanced C/C++ development platform, allowing for code generation and compilation in addition to having debugging features for the microcontrollers/microprocessors. While the $STM32CubeMX$ is a graphical tool that allows for the configuration of the pinout and the STM32 microcontroller/microprocessor. Both of these software's have been used due to their features

and for code generation during this thesis along with Matlab Simulink.

6.2 Scaling and offset

During the design period of the initial prototype measurement circuits a microcontroller had not been properly selected, however a standard high-end microcontroller such as Texas instruments TMS320 Delfino series or STM32 from STMicroelectronics were considered. Due to this an effort has been made to ensure the compatibility of the measurement modules and the microcontroller that would be selected. One of the microcontrollers which was considered, consisted of single-ended input ADCs to convert the analog output voltage into digital. For this thesis some of the chosen measurement cards give out a differential signal which can be negative or positive, thus can be damaging to the ADC port. A method of differential to single-ended output conversion is used to scale the input voltage signal of the ADCs, to only positive values (for example 0-5V). The circuit design has been adapted based on the recommended methods given by the data-sheet of the measurement cards, with some alterations to allow for offset voltage control as sourced by [50]. It should be mentioned that some of the capacitors which are added are optional and can be neglected, and serve only to filter the signals to stabilize them. The scaling and offset circuit has been illustrated in Figure 6.2.

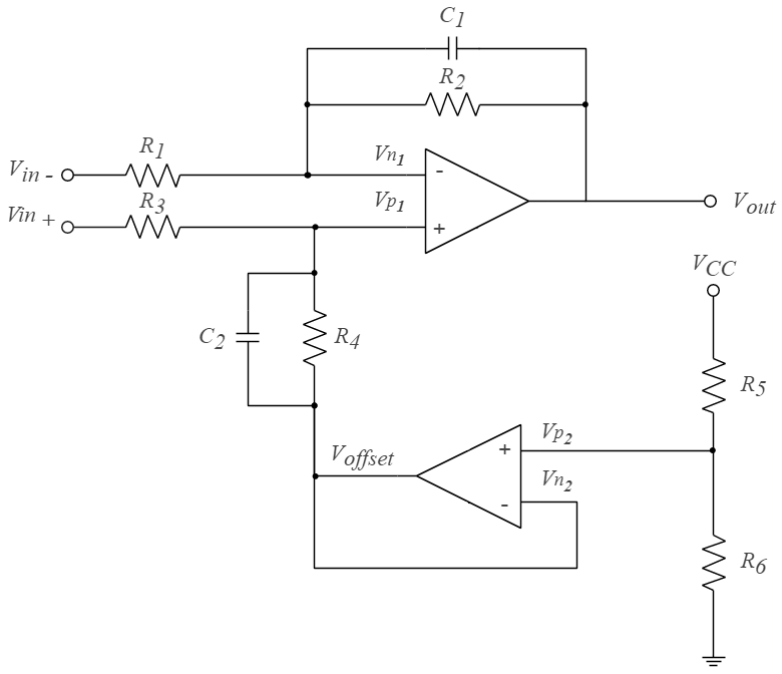


Figure 6.2: Differential to single-ended conversion, offset and scaling circuit

The circuit consists of two op-amps, the lower one determines the offset voltage. The

upper op-amp consists of the scaling circuit which determines the output voltage. Assuming ideal op-amp operation with infinite gain and input resistance. The offset output signal of the op-amp can be determined as $v_{offset} = v_{n2} = v_{p2}$, by using basic operational amplifier theory. Thus the lower op-amp circuit from figure 6.2. Is analysed and the bottom op-amp output signal v_{offset} can be derived, where V_{CC} represents an auxiliary supply voltage by the following expression:

$$v_{offset} = V_{CC}\frac{R_6}{R_5 + R_6} \tag{6.1}$$

Similarly the upper op-amp circuits voltage output from figure 6.2, can be determined by using the same assumptions. In addition in order to simplify the circuit we can assume that $R_1 = R_2$ and $R_3 = R_4$. The equations of the voltage division can be expressed as followed:

$$\frac{v_{in} - v_{p1}}{R3} + \frac{v_{offset} - v_{p1}}{R4} = 0 \tag{6.2}$$

$$v_{out} = \frac{v_{in}R_2 + v_{offset}R_1}{R_1} \tag{6.3}$$

Following these equations and the circuit topology the implementation becomes simple, and we acquire our desired single ended output ADC signal from both the current and voltage measurement circuits. Which will be introduced in the coming sections of this chapter.

6.3 Initially intended Modules

The development of the measurement boards are based on the PCB schematics provided by the supervisor. The schematic design of each module which was sourced by the thesis supervisor has been been provided in appendix D. However there has been made some changes to the original design from the sourced schematic, in order to incorporate it to the prototype. The measurement boards have been designed to convert the measurements into a signal which the MCU is capable of sampling through its ADC ports.

6.3.1 Power module (transistors and driver)

The power module circuit boards were sourced by the master thesis supervisor, and contain the ability to drive the controllable switch gate signals. Each of the power module circuit boards contain two IGBTs which makes up one leg of the three phase

inverter, hence the need of three modules too obtain the required amount of switches. An image of the power module is shown in figure 6.3. These boards were originally created to be used in another project however with small alterations to the original design, the modules should be suitable for the prototype in this thesis.

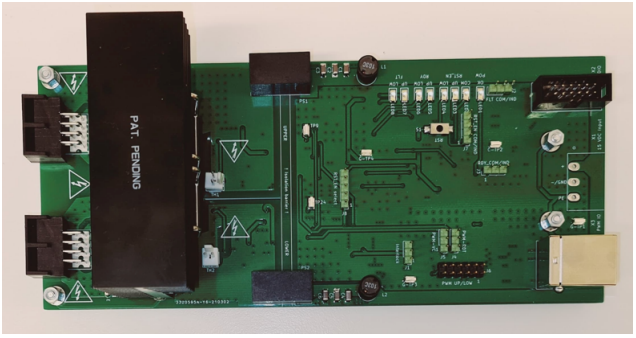


Figure 6.3: Power module - PCB

6.3.2 Voltage Measurement Module

MCU description and overview

The voltage measurement module consists of an AMC3330, which is a precision isolated amplifier with a fully integrated isolated DC-DC converter. The performance of the device is suitable for accurate voltage monitoring and control, as stated in the data-sheet provided in appendix D. Furthermore sections of the device are separated, protecting the low-voltage domains from being damaged. An illustration of the functional block diagram is shown in Figure 6.4

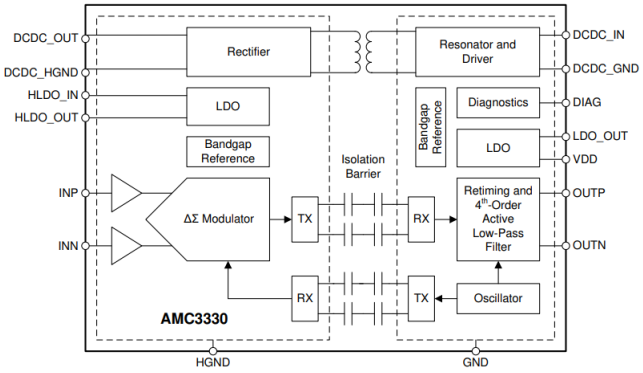


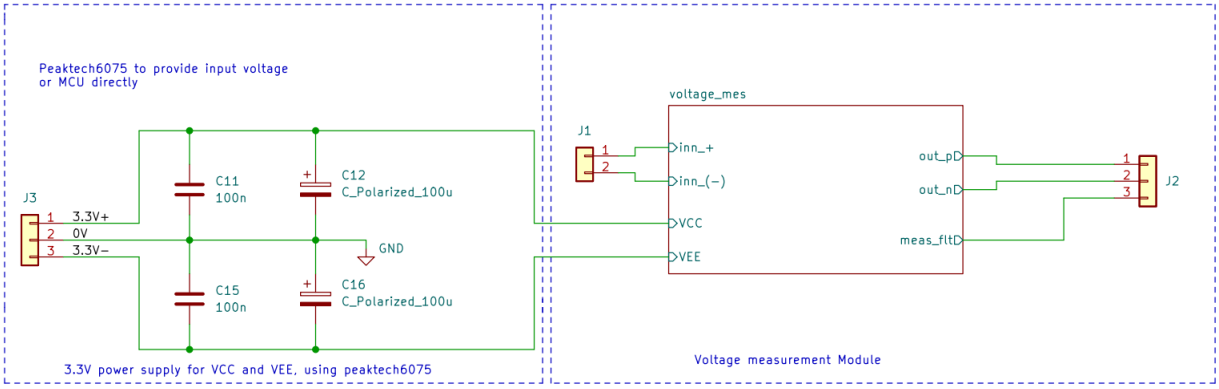
Figure 6.4: functional block diagram of AMC3330 , sourced from the data-sheet.

The open-drain DIAG pin is optional. With its intended purpose of determining whether the output voltage is valid, thereby operational or not. for the designed PCB the pin has been connected in the recommended way for its proper use. However during the

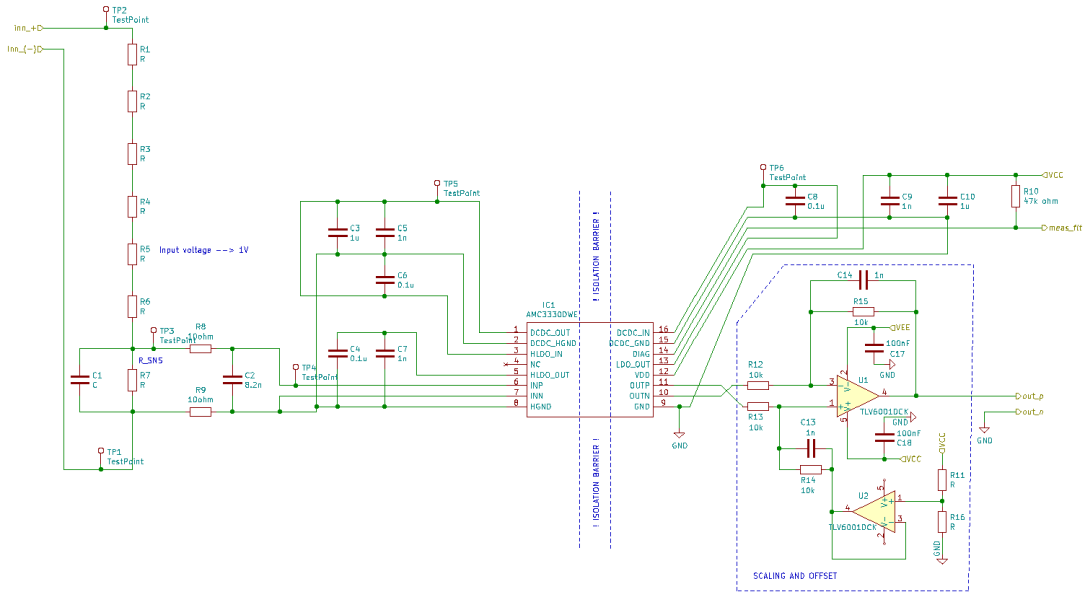
design period of the PCB. This feature was not intended to be used in the actual prototyping during lab tests, as this is an optional feature. Nevertheless this pin was added, considering any possible future work which could have some added benefit with this feature.

Designed module

A designed schematic of the proposed voltage measurement module has been illustrated in Figure 6.5a, while figure 6.5 shows the circuit inside the voltage measurement module block.



(a)



(b)

Figure 6.5: a) Voltage measurement circuit, b) Voltage measurement circuit and scaling circuit

The design parameters of the module follow these limitations on the device:

- Low-side supply voltage V_{DD} = 3.3V or 5V

- Voltage drop across sensing resitor R_{sns} for linear response = 1 V (Maximum)
- Current through resistive divider (I_{cross}) = 100μA (maximum)

In most voltage sensing applications, resistors are placed in series to scale down the input voltage signal in front of the isolated amplifier. In this particular device it is recommended to scale down the voltage to 1V or less, allowing for a signal within the limitations of the AMC3330 device.

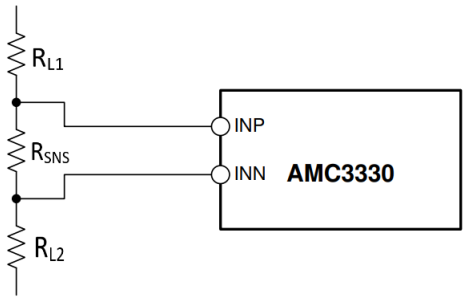
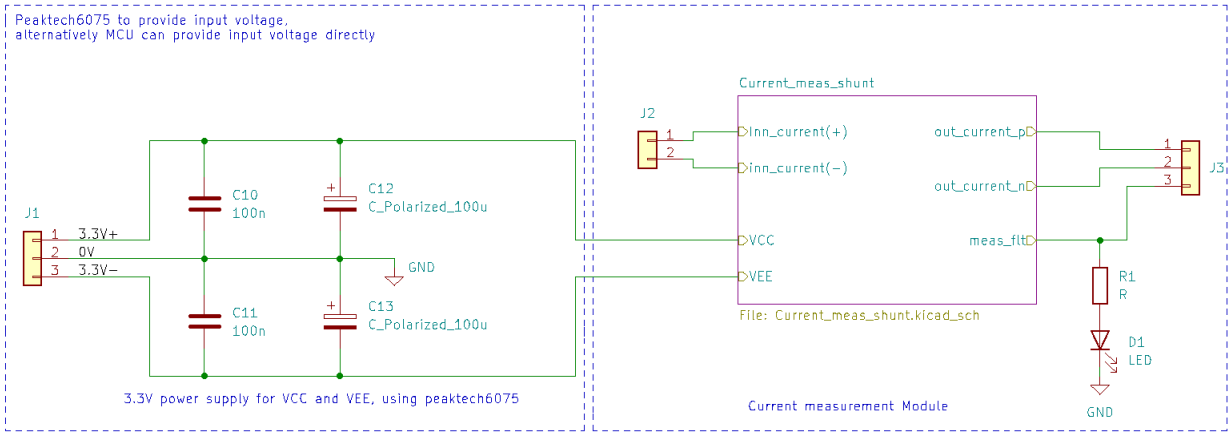


Figure 6.6: Simplified voltage divider circuit

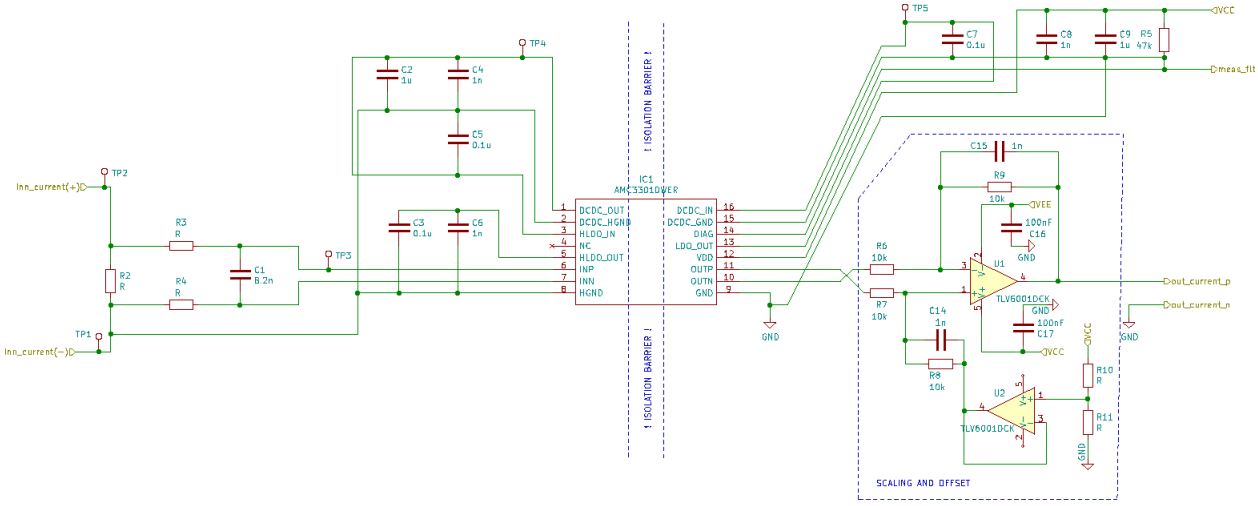
A simplified circuit of the resistor divider is shown in Figure 6.6. By using ohm's law we can derive the minimum total resistance of the resistive divider in order to limit the cross current (I_{cross}) to our desired value, $R_{Total} = \frac{V_{Line-peak}}{I_{cross}}$. where $V_{Line-peak}$ is the peak line voltage. Similarly the required sensing resistor (R_{sns}) which is to be connected to the AMC3330 device can be calculated as, $R_{sns} = \frac{V_{sns}}{I_{cross}}$.

6.3.3 Current Measurement Module

The Current measurement module consists of an AMC3301, which is a precision amplifier optimized ideally for shunt based current sensing applications. This component is designed quite similarly to the voltage measurement AMC3330 presented in the previous section as both components have been developed by *Texas instruments*. The AMC3301 includes an integrated DC/DC converter with an isolation barrier, and the input of the component has been optimized for the direct connection to a low-impedance shunt resistor. Furthermore the component is considered suitable for when accurate current monitoring is required with high-common mode voltages. The designed schematic of the proposed current measurement module has been illustrated in Figure 6.7.



(a)



(b)

Figure 6.7: a) Current measurement circuit b) Current measurement circuit and scaling circuit

6.4 Alternative Measurement Modules

Due to the lack of components to build the originally intended circuit models, the decision was made to build a converter control board via an alternative method which will be presented in this section. This has been achieved by using available components from the laboratory facility in the Western Norway University of Applied Sciences. This section will begin to present the voltage and current measurement modules as individual circuits to explain the overall theory and function of their design. Furthermore these individual measurement circuits have undergone laboratory tests individually and their function is therefore assured. The later part of the section will present the converter control board design circuit which incorporates the voltage and current measurement modules into a single PCB board needed to control a GTI.

6.4.1 Voltage Measurement circuit

The voltage sensing device is a LEM LV-25-P voltage transducer. The inner circuit diagram of the voltage transducer has been illustrated in figure 6.8, which was adapted from the datasheet of the measuring device provided in appendix D. The sensor contains an amplifier which is connected to a hall sensor as shown in figure 6.8, therefore the transducer requires a DC supply ($+U_c$ and $-U_c$). The voltage sensing device is capable of being supplied either ±12 V or ±15 V. The LEM LV-25-P voltage transducers working principle is based on the hall effect. To put it simply the transducer contains a primary and secondary circuit, when a voltage is applied on the input terminals of the primary side a magnetic field is generated by the current flowing through the circuit. The generated magnetic field is then compensated by a reverse magnetic field caused by the current flowing through the coil of the secondary circuit. The device uses a hall effect sensor which can detect the field compensation, for a more detailed explanation a source from the producer of the component has been provided [51].

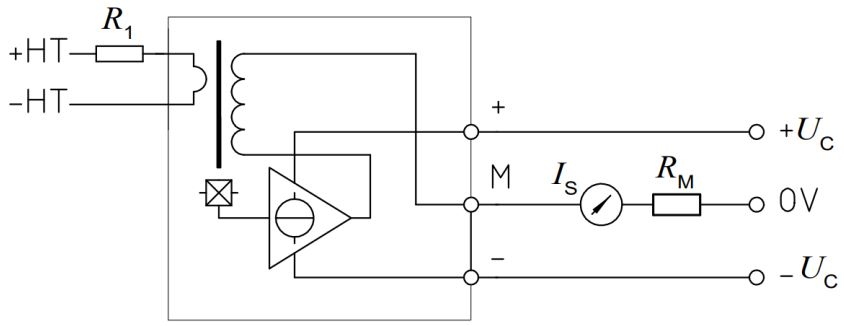


Figure 6.8: Inner circuit diagram of the voltage transducer sourced by the datasheet which can be found in appendix D.

Design considerations for the construction of the measurement module have been taken, based on the parameters given by the datasheet of the product. Such as the primary current termed I_p has a nominal value of 10 mA. While the external primary measurement resistor termed R_1 must be dimensioned in accordance to the nominal voltage, so that the current which flows through the primary sensor is approximately 10 mA. Additionally the primary side resistor will cause the voltage to be stepped down, thus the transducer remains well within the maximum voltage of 500 V. The nominal abc line voltages which will be measured are assumed to be:

$$V_n = 230\sqrt{2} \approx 325V \tag{6.4}$$

To obtain 10 mA at the primary side of the voltage transducer the resistors are determined based on the applied voltage. The calculation of the external primary side resistor

$R_{primary}$ is derived by using ohms law as follows:

$$R_{primary} = \frac{V_p}{I_p} - R_{internal} = \frac{325}{0.01} - 225 \approx 32.5k\Omega \tag{6.5}$$

Where V_p and I_p represent the primary side voltage and current, while $R_{internal}$ is the measured resistance of the internal winding of the transducer. The primary side current can be expressed as:

$$I_p = \frac{V_p}{R_{primary} + R_{internal}} = \frac{325}{32500 + 225} = 9.931mA \tag{6.6}$$

However the resistors have been over-dimension slightly in case of deviations or over-voltages when constructing the circuit. Therefore the line voltages have been dimensioned with a 10% increase resulting in $R_{primary} \approx 36k\Omega$, when the measurement module was tested. The schematic drawing of the voltage measurement circuit which was used during tests is presented in figure 6.9. The measurement modules have been adapted from [50], and where designed by another author to be used in their project.

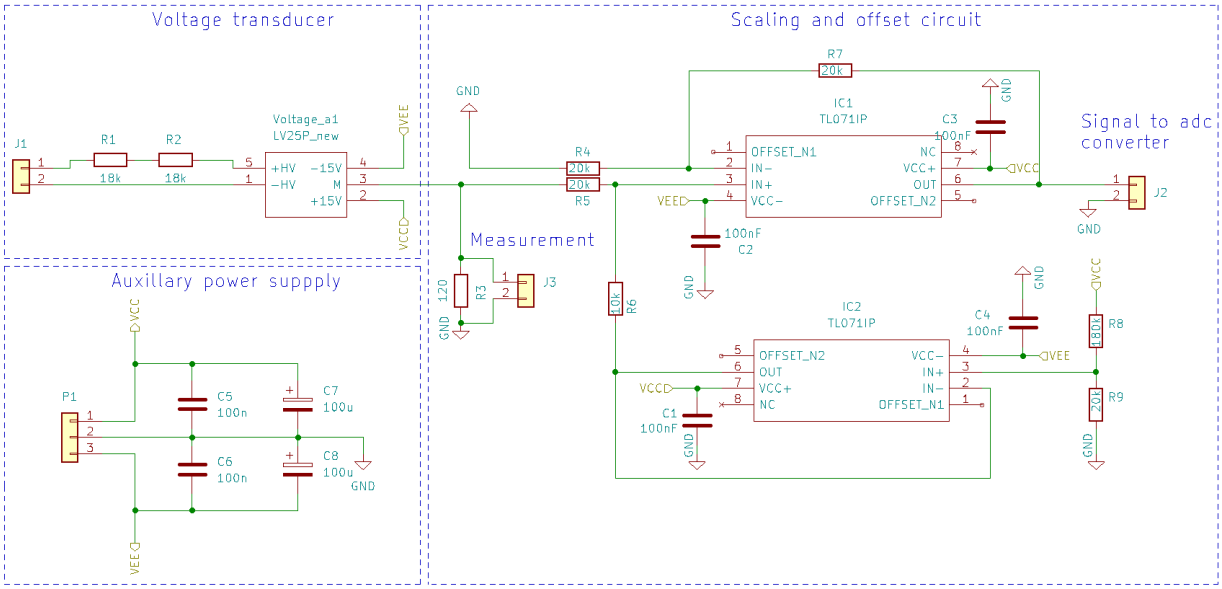


Figure 6.9: Voltage measurement schematic overview for the grid line voltages, adapted from [50].

However due to the similarity and lack of components it was deemed suitable for this thesis. Note that the schematic drawing contains three separate sections: the voltage transducer, the scaling and offset circuit and finally the auxiliary power supply. The prototype voltage measurement modules as well as the operational amplifiers from the scaling and offset circuit where designed to be supplied with ±15 V. The primary side external resistors have been divided into a series connection of two, thereby lowering

the amount of dissipating power over each individual resistor needed. The resistors in series R_1 and R_2 have been selected to be capable of dissipating 5 W as this is what was available in the laboratory.

The primary and secondary circuits are separated by a conversion ratio K which is given by the datasheet as:

$$K = \frac{n_1}{n_2} = \frac{2500}{1000} \tag{6.7}$$

In which case the nominal primary input current rated at 10 mA, leading to the nominal output current being subsequently 25 mA. The measurement resistor on the output side is calculated as:

$$R_m = \frac{V_m}{I_s} = \frac{3\ V}{25\ mA} = 120\Omega \tag{6.8}$$

Where V_m is the maximum voltage for the ADC port, and the output voltage from the circuit is given as a sine wave with ±3 V. The output measurement voltage V_m when measuring over R_m can be used to calculate the line voltage value by using the following expression:

$$V_{m,cal} = \frac{V_m(R_{internal} + R_{primary})}{K\ R_m} \tag{6.9}$$

The scaling and offset circuit which was previously derived in section 6.2, is used to transform the output voltage in order to give out a voltage value between 0 and 3 V. The circuit scales down the transducer voltage output from ± 3V down to ± 1.5V, then it offsets the the output so that the resulting output will be restricted to a value of 0 to 3 V as desired. Given the assumption that $R_4 = R_6$ and $R_5 = R_7$, the output voltage from the scaling and offset circuit termed V_{adc} can be derived by using the following equation:

$$V_{adc} = \frac{V_m R_7 + V_{offset} R_6}{R_6} \tag{6.10}$$

DC voltage measurement circuit

The DC voltage measurement circuit was designed in a similar way to the line voltage measurement circuit. However seeing as the nominal measurement range is 0-600V, the scaling and offset circuit has been omitted. This is due to the output of the voltage sensor will be providing a voltage in the range of 0-3 V, which is compatible with the MCU and no scaling or offset is deemed necessary. Thereby the circuit was designed to resemble the one shown in figure 6.8, where the external resistor $R1$ is redimensioned. Due to the different nominal voltage measurement range the external primary side resistor R_1 is calculated as follows:

$$R_1 = \frac{V_p}{I_p} = \frac{600\ V}{10\ mA} = 60\ k\Omega \tag{6.11}$$

The external resistors are divided into a series connection of four resistors each with

a value of 15 kΩ. With the possibility of over-voltage the measurement resistor R_m is calculated by using the maximum input current $I_{p,max}$. Which is provided in the datasheet as 14 mA, leading to a maximum voltage of 840 V. Following the datasheet a lower limit of 100Ωis selected as the calculated value using the same formula as equation 6.8 was shown to be slightly less than 100 Ω.

6.4.2 Current Measurement circuit

The current sensor device used is a LEM LA-100-TP, with a similar working principle as the voltage transducer from the previous section. An illustration of the inner circuit diagram of the current transducer has been provided in figure 6.10. From the figure we can deduce that when the primary side current I_p flows in the direction of the arrow, the secondary side current I_s will be positive. And similar to the voltage transducer this sensor requires a dc-voltage supply of either ±12 V or ±15 V.

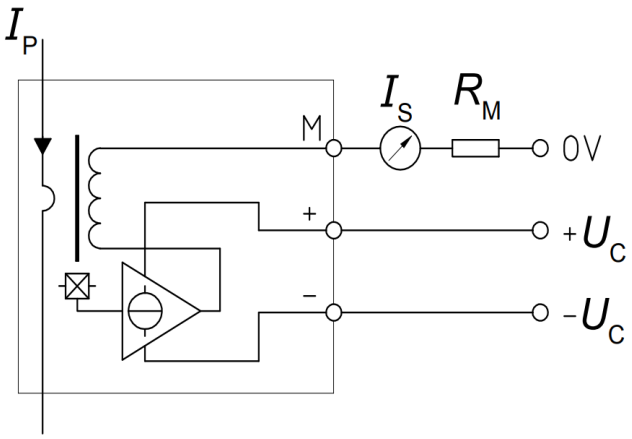


Figure 6.10: LEM LA 100-TP circuit diagram, adapted from the datasheet.

An illustration of the schematic drawing of the current measurement circuit which was used during testing has been provided in figure 6.11. The current measurement circuit has been adapted from [50]. The schematic as shown in the figure is divided into the following separate sections: the auxiliary power supply, the current measurement device, the measurement output and finally the scaling and offset circuit.

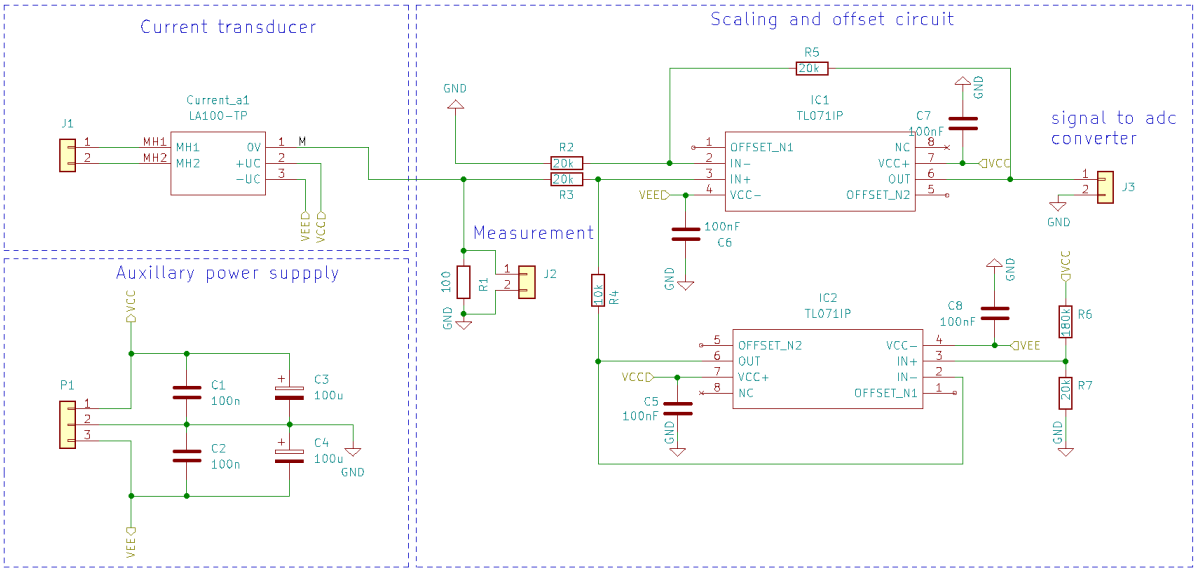


Figure 6.11: Current measurement schematic overview for the converter side currents, adapted from [50].

The primary and secondary circuit are galvanically separated with a conversion ratio K which is given by the datasheet as:

$$K = \frac{n_1}{n_2} = \frac{1}{2000} \tag{6.12}$$

Assuming that the nominal primary current I_{pn} is equal to 10 A, the secondary current I_s can be measured by using the conversion ratio of the transducer as follows:

$$I_s = I_{pn}K = \frac{10A}{2000} = 0.005A \tag{6.13}$$

A measuring resistor R_m is placed on the secondary side, the measurement resistor must not exceed 110 Ωas this is the maximum value as given by the datasheet provided in appendix D. By using a measurement resistor with a value of 100Ωthe resulting output voltage is expressed as:

$$V_{output} = I_s R_m = \pm 0.005 \cdot 100 = \pm 0.5V \tag{6.14}$$

The scaling and offset circuit is identical to the one used in the voltage measurement circuit presented in the previous section.

6.4.3 Converter Control Board

A converter control board has been constructed to house all the voltage and current transducers presented in the former measurement sections into one board. The schematic overview and the different layouts of the PCB has been illustrated in figure 6.12-6.14. Only the overview of the schematic has been presented in figure 6.12, while the remaining parts have been provided in appendix C. As one can observe from the layout in figure 6.13 the line voltage transducers have been placed on the left side along with their respective scaling and offset circuitry. While the line current transducers and their respective offset and scaling circuitry have been placed on the top right. The dc-link voltage sensor is located in the middle. Each of the transducers as previously explained require a dc voltage supply of $\pm$12V or $\pm$15V, this requirement is met by using two auxiliary power supplies named "EA-PS 2032-050" which can be connected to the input terminal labelled as $P1$. The inputs and output signals for the microcontroller have been labelled and placed on the lower right side, with the pin-mapping being the same as is seen in the schematic of figure 6.12.

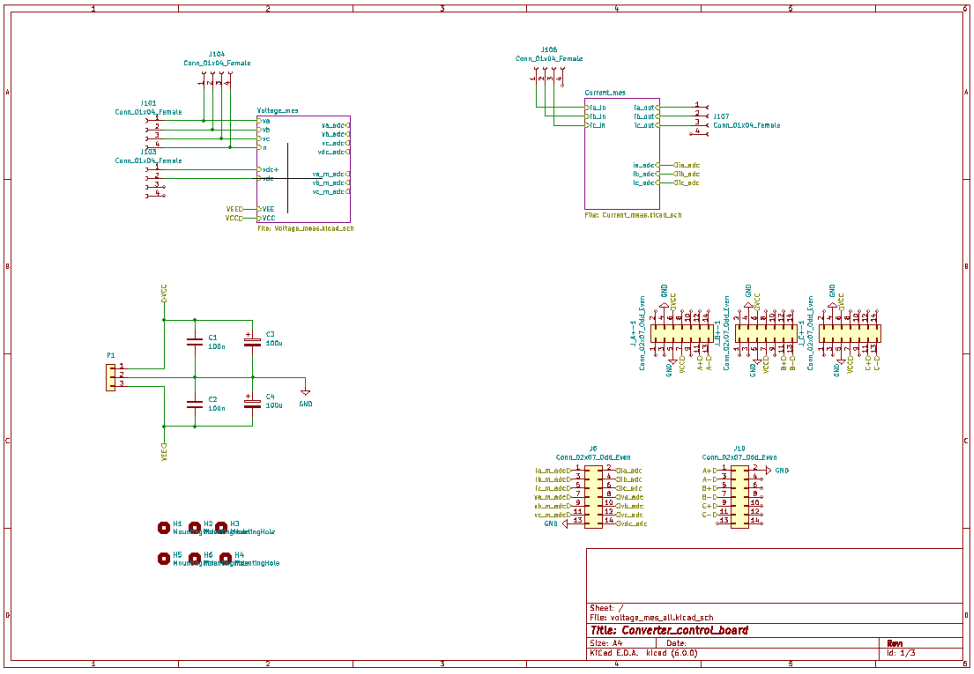


Figure 6.12: Converter control board circuit schematic overview.

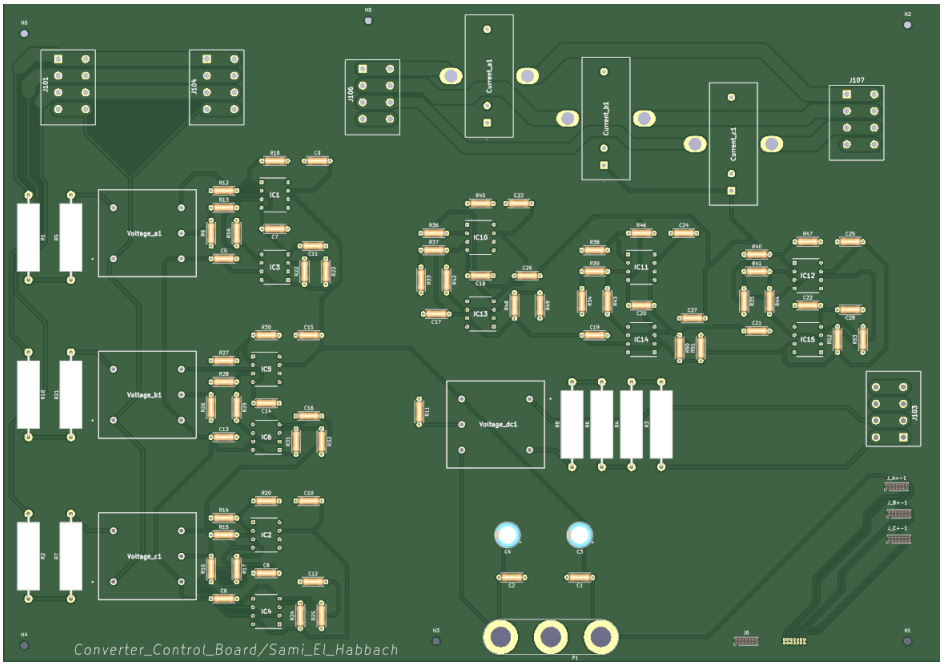


Figure 6.13: Converter control board - 3D layout.

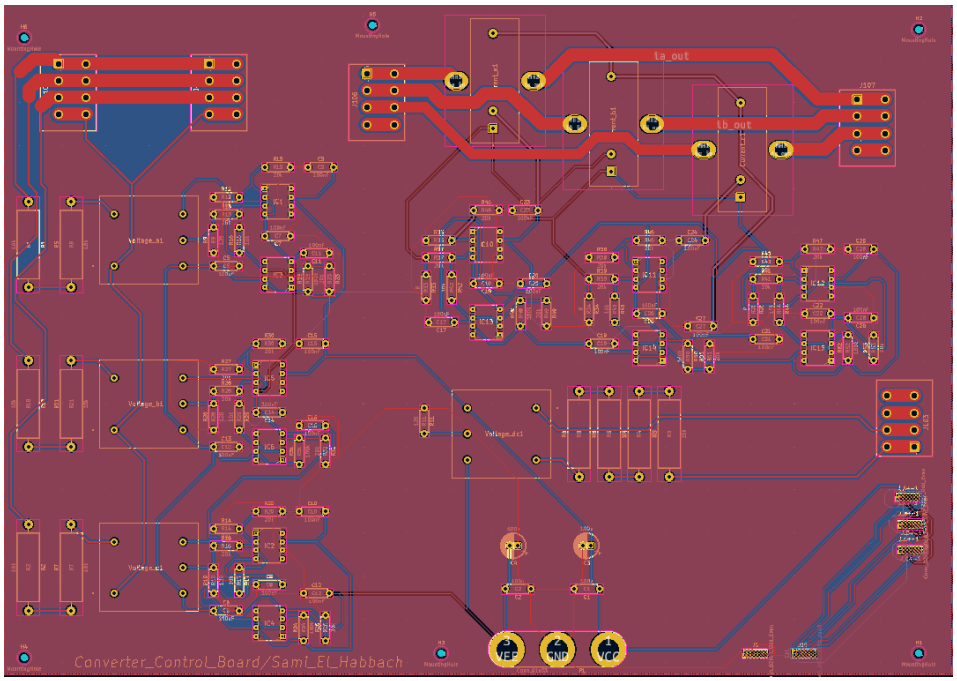


Figure 6.14: Converter control board PCB layout, showing all layers. The red lines are electrical connections/routes which are located at the top side of the board, while the blue connections/routes are located at the bottom of the board. The component mounting holes with connection to the pins of the electrical components are coloured yellow. The light blue mounting holes on the outer edges are mounting holes for the board.

6.5 IGBT component

The originally intended power module was designed to contain the IGBT switches, however as previously stated a number of components where not available for this specific module to be used. Thus alternative IGBT switches which are available at the lab where selected for prototyping instead. The Selected IGBT modules have been produced by Semikron and their specific product name is SKM100GB12T4, the datasheet of the component is provided in appendix D. From the datasheet an illustration of the component as well as the inner circuit diagram has been adapted in figure 6.15.

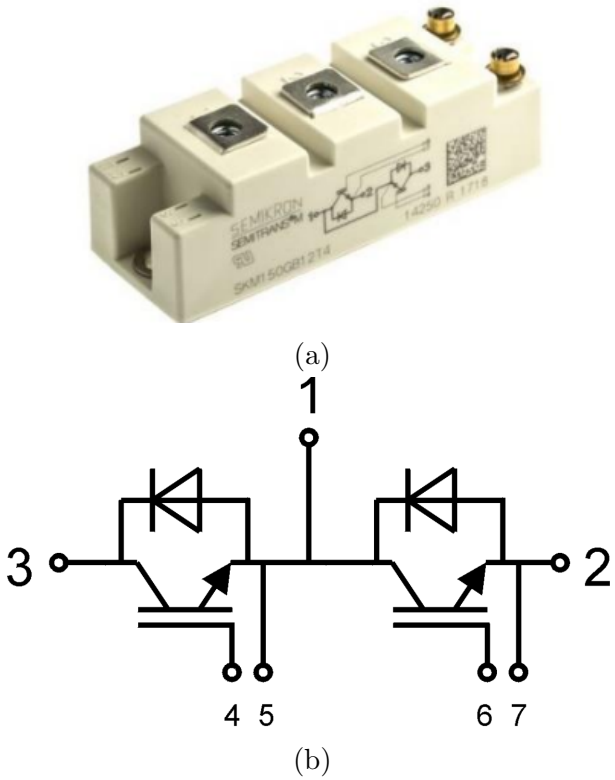


Figure 6.15: a) IGBT module, b) inner circuit diagram of the module

The IGBT module contains two IGBT switches an upper and lower switch, thereby a GTI will require three of such modules one for each of the converter legs. According to the datasheet the maximum rated switching frequency is 20 kHz and the collector to emitter junction is capable of supporting up to 1200 V, with a nominal current of 100 A. The ratings of the module are well within the scope of this thesis project and are deemed appropriate for use. Every individual module contains three terminal connections used for the converter leg and two pins for each transistor labelled as pin 4-5 and 6-7 respectively as shown in the inner circuit diagram. The grid phase voltage is connected to terminal 1. While the dc-link terminals are connected to 3 and 2 with their respective polarity. The modules can be driven by using a transistor driver for optimal switching.

6.6 Transistor Driver card

In order for the IGBT switches to be controlled with high frequency a signal must be provided to the gate of the transistor switches. Additionally the gate capacitor requires a current in the order of hundreds of milliamps, to charge and discharge. Thereby to achieve high frequency switching a transistor driver card is deemed necessary considering that the signals from the MCU will only provide a current flow of a few milliamps. From the available components in the lab this gate signal can be provided by using a transistor driver card developed by Semikron with the product name : SKHI 23/12 R. The datasheet of the driver card has been provided in appendix D. While a picture of the transistor driver card as well as the connection diagram sourced by the datasheet of the component is presented in figure 6.16. The driver card contains several functions, a short description of some of these functions is presented as follows:

- **Interconnected circuit**

  The driver card as shown in the datasheet contains two interconnected circuits. This in turn allows for a single driver card to control both transistors in an individual Semikron IGBT module such as the one presented in section 6.5.

- **Interlocking Time Function**

  An interlocking time function which prevents both transistor gates from each half bridge from turning on at the same time. accomplished by having a dead time between the switching of the gates. Furthermore the factory adjusted dead time is $\tau_{dt} = 10\mu s$, which can be adjusted by soldering on additional resistors between pins J3 to K3 and J4 to K4 as shown in the connection diagram.

- **Short Circuit Protection**

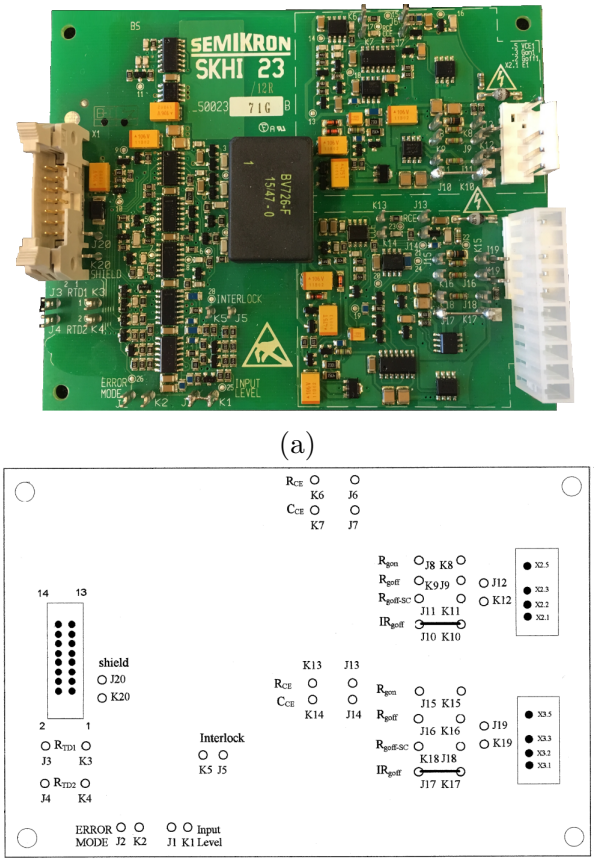
  A short circuit protection is provided through a monitoring circuit which measuresx the collector-to-emitter voltage V_{CES}. Furthermore there is a error memory which blocks all signals to the IGBT if a short circuit is detected, or if there is a malfunction in the input voltage supply of the driver card.

- **Output Buffer**

  The output buffer provides the correct current to the gate of the IGBT, assuring sufficient power to the gate for proper switching and preventing losses and failures.

The interconnected circuit allowing for the control of two gate transistors, is why only three such transistor driver cards are required to drive the gate signals of the three IGBT modules. Which are needed in the GTI prototype. The driver cards can be

controlled by the MCU output, given that pin J1 and K1 are connected to have an input voltage range of 0-5V. Otherwise the driver cards require an input voltage of 15V , which means the voltage signals from the MCU must be stepped up. One of the methods in which the signal can be stepped up is by using operational amplifiers or alternatively by using optocouplers one can also achieve galvanic isolation. However such a solution will introduce a time delay which although remaining small could lead to errors during the operation of the converter system. It is recommended by the datasheet to solder bridge the connection points J12 to K12 and J19 to K19. Which limits the amount of outputs for the gate signal and saves the need for an additional external connection.



(a)

(b)

Figure 6.16: a) the transistor driver: SKHI 23/12 R , b) connection diagram adapted from the datasheet.

Chapter 7

Discussion and Conclusion

The objective of this master thesis was the design and control of a grid tied bidirectional converter for the sake of charging and discharging a battery. While also taking into consideration the capability of having the system be slightly altered, so that it may be adapted towards different projects for future work. This objective has been partially fulfilled throughout the course of the two semester spent for the completion of this thesis.

The initial work was accomplished by thoroughly studying research articles, textbooks and previous dissertations containing information which could be relevant for this thesis. While also getting an overview of the standards and requirements which where necessary in regards to grid tied systems. The topology of the AFE converter was presented, while a single- and two stage topology was considered for the charging and discharging of the battery load/supply. A two stage charge topology was finally selected as this would offer more flexibility of designing the control strategy and providing a more stable dc-link voltage. Evidently this came with its own disadvantages, as adding more stages increases the complexity of the system and leads to more power loss.

When it came to selecting an inverter topology going with a traditional three phase inverter approach, was deemed suitable as it naturally contains bidirectional capabilities. In addition to being a very well established topology with a lot of research articles and textbooks containing information regarding the control and the function of such systems. However when attempting to select a topology for the DC-DC converter, there where requirements such as being able to boost and buck the input and output. While also being able to both control and integrate the DC-DC converter to the GTI. While going through different methods which have previously been used successfully with a high efficiency, my research indicated that a Dual Active Bridge (DAB) converter might be more suitable as the DC-DC converter. However after attempting to integrate a simulated model to the

GTI the design, tuning and control was not properly constructed due to its complexity. Leading to an unstable model and the idea was replaced by a much simpler buck-boost converter topology. Which was a combination of the buck and boost converter topologies introduced in the theoretical framework. Although for future work constructing a DAB converter properly could lead to a better result.

As presented in the theoretical framework in chapter 2, there where a number of filtering methods which could be used between the grid and the inverter. After going through the advantages and disadvantages, in addition to what is used in state of the art GTI systems. The LCL-filter topology was selected, and a design approach which determined the size of the components without the use of a damping resistor was chosen. The resulting filter design methodology was explained in great detail in chapter 4, and resulted in a desirable outcome. For future work however adding a damping resistor or applying a different design methodology, is something to be considered. As this could lead to better results and can be further researched and compared.

Several considerations where taken when selecting the different control structures and strategies, where multiple modulation techniques where considered. However SVPWM was the main modulation strategy which was chosen, as this was the one which gave the least amount of THD although it increased the complexity of the design. Primarily the goal was to utilize VOC and DPC while allowing for bidirectional capabilities. Which was constructed in a simulation environment using the Simulink application. The initial simulated design used an ideal dc voltage source to supply the GTI, this was in order to test the control methods in a more ideal environment. In the case of the VOC everything went as intended and it was fully capable of being integrated with the DC-DC converter, while remaining within IEEEs 5% THD requirement. The DPC method worked as intended during the simulated testing phase where an ideal dc-link voltage was being supplied. However the DPC came with its challenges when attempting to integrate the DC-DC converter. When applied during simulated testing the dc-link voltage would become unstable after running the system for a short while. This instability was caused due to the lack of a voltage control loop to regulate the dc-link so that it would provide a stable voltage for the GTI. It is therefore concluded that in order to use the DPC after integrating the two-stage topology, alterations to the method presented in this thesis must be added. This is to regulate the dc-link voltage to ensure a stable voltage level to supply the GTI.

The biggest challenge of this thesis was the implementation of the system from a simulated environment onto a physical hardware prototype. After having spent most of the time during the thesis in the research, design, tuning and integration of the two stage topology of the overall system. The initial prototype model was meant to be built us-

ing pre-existing modules (power and measurement), with slight alterations for the final construction. However after working on these initial modules design alterations it came to light that the components which where necessary to build these modules where not available without a considerable waiting time. In some cases the waiting time exceeded that of a year, due to the international chip shortage. This lead to an attempt in trying to build alternative modules. The alternative modules where made by using mainly components which where already available in the laboratory facilities provided by the Western Norway University of Applied Sciences.

The converter control board PCB was designed after assuring that all the necessary components where available in the lab, some of which where soldered on pre existing boards such as the measurement transducers. The transistor driver cards which would be needed to drive the IGBT switches where available but used in another project. While the IGBT switch modules where available, however after testing several of the components individually only three where fully functioning. Unfortunately these three where intended to be used in a similar although different project. Due to these occurring challenges and limitations not everything needed to build a functioning prototype was acquired and constructed. Notably the filter was not constructed, and although there where several batteries they where not at a suitable size for the prototype model and where therefore not included. Due to the prototype model not being completed in time the comparison between the simulated and physical model measured results could not be compared.

The MCU was tested and it showed that signals where being output, however the integration of the MCU and the converter control board module was not conducted and its overall function can therefore not be fully determined. However based on the data given by the datasheet there should not be any issues. The tests on the measurement boards where done individually, with and without their scaling and offset circuit. the tests resulted in the desired output voltage, showing ± 3 V when measuring V_m. While also showing the correct Analog to digital conversion. (ADC) output voltage after the scaling and offset circuit, giving an output value of 0-3V. Considerable time was taken during the design of the converter control board, however it has not been tested properly as the components where not soldered on to the board in time for this thesis. The final results on the tests and the components for the prototype module suggest that further research and testing is needed for an appropriate fully functioning prototype.

List of Figures

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Appendix A

Matlab code

A.1 Clarke and Park transform block codes

abc to $\alpha\beta$ using Clark transform

```
function [alpha,beta,zero] = abc2alfa_beta(a,b,c)
    alpha=sqrt(2/3)*(a-b/2-c/2);
    beta=sqrt(2/3)*(sqrt(3)/2*b-sqrt(3)/2*c);
    zero=0;
end
```

$\alpha\beta$ to dq by using Park transform

```
function [d,q] = ab2dq(alpha,beta,wt)
%90 degrees behind A axis, sqrt(2/3) for power invariance.
d=(alpha*cos(wt-pi/2)+ beta*sin(wt-pi/2))*sqrt(2/3);
q= (-sin(wt-pi/2)*alpha+beta*cos(wt-pi/2))*sqrt(2/3);
end
```

dq to $\alpha\beta$ By using inverse Park transform

```
function [Valpha,Vbeta] = dq2ab(Vd ,Vq ,wt)
Valpha=Vd*cos(wt-pi/2)- Vq*sin(wt-pi/2);
Vbeta=Vd*sin(wt-pi/2)+ Vq*cos(wt-pi/2);
end
```

dq to abc by using inverse Park and Clark transform directly

```
function [a,b,c] = dq2abc(d,q,wt)
%Power invariant and q-axis alignement
a= sqrt(2/3)*(d*sin(wt)+q*cos(wt));
b= sqrt(2/3)*(d*sin(wt-2*pi/3)+q*cos(wt-2*pi/3));
c= sqrt(2/3)*(d*sin(wt+2*pi/3)+q*cos(wt+2*pi/3));
end
```

$\alpha\beta$ to dq currents using active and reactive power - DPC

```
function [alpha,beta] = fcn(P,Q,V_alpha,V_beta)
alpha=(1/(V_alpha^2+V_beta^2))*(P*V_alpha+Q*V_beta)
beta=(P*V_beta-Q*P)*(1/(V_alpha^2+V_beta^2))
end
```

A.2 SVPWM block codes

dq to $\alpha\beta$ and theta

```
function [Valpha,Vbeta, theta] = dq2ab(Vd ,Vq ,wt )
Valpha=Vd*cos(wt-pi/2)- Vq*sin(wt-pi/2);
Vbeta=Vd*sin(wt-pi/2)+ Vq*cos(wt-pi/2);
theta=atan2(Vbeta,Valpha);
end
```

Vref

```
function Vref = Vref(Valpha,Vbeta)
Vref=sqrt(Valpha^2+Vbeta^2);
end
```

Sector

```
function n = Sector(theta)
n=0; % initial value
if(theta>0)&(theta<=pi/3)
 n=1;
```

```
5  end;
6  if(theta>pi/3)&(theta≤2*pi/3)
7   n=2;
8  end;
9  if(theta>2*pi/3)&(theta≤pi)
10  n=3;
11 end;
12 if(theta≤-2*pi/3)&(theta>-pi)
13  n=4;
14 end;
15 if(theta≤-pi/3)&(theta>-2*pi/3)
16  n=5;
17 end;
18 if(theta≤0)&(theta>-pi/3)
19  n=6;
20 end;
21 end
```

Angle

```
1  function Gamma = Angle(theta,n)
2  Gamma=0;
3  if(n==1)
4   Gamma=theta;
5  end;
6  if(n==2)
7   Gamma=theta-pi/3;
8  end;
9  if(n==3)
10  Gamma=theta-2*pi/3;
11 end;
12 if(n==4)
13  Gamma=pi+theta;
14 end;
15 if(n==5)
16  Gamma=2*pi/3+theta;
17 end;
18 if(n==6)
19  Gamma=pi/3+theta;
20 end;
21 end
```

Time constants

```
function [T0,T1,T2] = Time_constants(Vdc,Ts,Vref,Gamma)
ma=Vref/Vdc;
T1=Ts*sqrt(3)*ma*sin(pi/3-Gamma);
T2=Ts*sqrt(3)*ma*sin(Gamma);
T0=(Ts-T1-T2);
end
```

Duty cycle

```
function [S1,S2,S3] = Duty_cycle(T0,T1,T2,n)
S1=0;
S2=0;
S3=0;
if(n==1)
 S1=T1+T2+T0/2;
 S2=T2+T0/2;
 S3=T0/2;
end;
if(n==2)
 S1=T1+T0/2;
 S2=T1+T2+T0/2;
 S3=T0/2;
end;
if(n==3)
 S1=T0/2;
 S2=T1+T2+T0/2;
 S3=T2+T0/2;
end;
if(n==4)
 S1=T0/2;
 S2=T1+T0/2;
 S3=T1+T2+T0/2;
end;
if(n==5)
 S1=T2+T0/2;
 S2=T0/2;
 S3=T1+T2+T0/2;
end;
if(n==6)
 S1=T1+T2+T0/2;
 S2=T0/2;
 S3=T1+T0/2;
end;
end
```

A.3 LCL-filter code

LCL filter and dc-link capacitance code

```
%% LCL FILTER
% Input data: SYSTEM
clc
Vg = 230; % Vll = 230*sqrt(3) = 400V
P = 4e3; % rated power set to 4kW to allow for simulation of lower ...
    current values
fg = 50;
fsw = 20e3;
Lgrid = 13e-3; % estimation in weak grid conditions
Vll = Vg*sqrt(3);
w = 2*pi*fg;
w_sw = 2*pi*fsw;
Ri=0.1;
Rg=Ri;
Rt=Ri+Rg

%% max inductor value
% recommended value to be 0.1 pu of base value
Ltmax = 0.1*Vll^(2)/(2*pi*fg*P)

%% minimum DC-link voltage
Igmax = P/Vll*0.8; % safer with reduction
Vimax = sqrt((Vg*sqrt(2))^(2)+(Ltmax*w*Igmax)^(2));
Vdc = sqrt(3)*Vimax % for SVM, recommended to round up for selection.
Vdc = roundn(Vdc,2);

%% max filter capacitance
Cfmax = 0.05*P/(w*Vll^(2));
Cf = Cfmax *0.5; % recomended to try 0.5 and increase incrementally ...
    until max is reached

%% Converter side inductor
Iimax = Igmax; % for high frequencies
Isat = Iimax + 10; % (conditional)
i_rip = (Isat-Iimax)*2;
RF = i_rip/Iimax; % Converter side ripple factor
Limin = Vdc/(6*fsw*i_rip);
Li = 0.4 * Ltmax;
if(Li ≤ Limin)
 error('Inverter side inductor too small, increase the total ...
    inductance or ripple current')
```

```
39 end
40
41 %% Grid side inductor calculation
42 Lgridmax = Lgrid; %weak grid
43 Lgridmin = 0; %stiff grid
44
45 %% capacitor accuracy range (5%)
46 Cfmax = Cf*1.05;
47 Cfmin = Cf*0.95;
48
49 %% Equation variables
50 a_max = (Ltmax/Li) - 1;
51 a1 = Li*Cf*w_sw^(2)-1;
52 a2 = (1+a1)*Li+Lgridmax
53 a3 = (Li+a1*Lgridmax)*Li*Cfmax;
54 b2 = (1+a1)*Li+a1*Lgridmin;
55 b3 = (Li+a1*Lgridmin)*Li*Cfmin;
56
57 %% attenuation conditions, expressed from the freq range
58 Δ_1 = (36*Li-(2*pi*fsw*Li)^(2)*Cfmax)/(a3*(2*pi*fsw)^(2)-36*a2)
59 Δ_2 = (4*Li-(2*pi*fsw*Li)^(2)*Cfmin)/(b3*(2*pi*fsw)^(2)-4*b2)
60 Δ_min = 1/abs(1+a_max*a1);
61 if(Δ_1 > Δ_2)
62  Δ_max = Δ_1;
63 else
64  Δ_max = Δ_2;
65 end
66
67 %% Grid side Filter value
68 Δ = 0.07; %attenuation! lower Δ gives lower THD
69 Lg = Li*(1+Δ)/(Δ*a1);
70
71 %% Frequency range and filter verification
72 f_res = (1/(2*pi)) * sqrt((Lg+Li)/((Lg)*Li*Cf));
73 f_res_min = (1/(2*pi)) * ...
       sqrt((Lg+Lgridmax+Li)/((Lg+Lgridmax)*Li*Cfmax));
74 f_res_max = (1/(2*pi)) * ...
       sqrt((Lg+Lgridmin+Li)/((Lg+Lgridmin)*Li*Cfmin));
75 fc_min = fsw/6;
76 fc_max = fsw/2;
77 if (10*fg ≥ fc_min || fc_min > f_res || f_res > f_res_max || ...
       f_res_max > fc_max)
78  error('Outside of Frequency range condition')
79 end
80 if (Δ > Δ_max || Δ < Δ_min)
81  error('outside acceptable region')
82 end
```

```
83 if ( 1/(w*Cf) < w*Lg*10)
84  error('Filter capacitor impedance too small')
85 end
86 if (10/(w_sw*Cf) > w_sw*Lg)
87  error('Grid side inductor impedance too small')
88 end
89
90 %% DC-link capacitor
91 Cdmin= P*(sqrt(2)*Vdc+sqrt(3)*Vll)/(2*sqrt(3)*Vll*Vdc*0.3*fsw)
92 Cd=Cdmin*1.05
```

A.4 Modulus optimum

Modulus optimum and Bode plot code

```
1  %% Modulus optimum tuning technique
2  %Time constants
3  Lt=Lg+Li
4  Ta=1/(5*fsw) %Ta is converter time delay, assumed to be 0.2*Tsw
5  Ti=Lt/(Ri+Rg)
6  TLCL=Lt/(Ri+Rg)
7
8  % Proportional and integral gain constant calculation
9  Kp=((Lt/(Ri+Rg))*(Ri+Rg))/(2*Ta) % changing the Kp value adjusts the ...
       crossover freq
10 Ki=Kp*1/(Ti)
11
12 %PI controller transfer function using Kp and Ti
13 G_I=tf([Ti 1],[Ti 0])
14 G_PI=Kp*G_I
15 G_PI2=tf([Kp Ki],[1 0]) %Alternative method
16
17
18 % L approximation TF
19 GL=tf([1],[Lt/(Ri+Rg) 1])*tf([1],[(Ri+Rg)]) % L approximation
20 GL_PI=GL*G_PI
21
22 % L approximation TF with converter TF added
23 GL_MO=tf([1],[Ta 1])* tf([1/(Ri+Rg)],[TLCL 1])
24 GL_PI_MO=GL_MO*G_PI
25
26 % L approximation transfer function using the alternative PI term
27 GL2=tf([Kp Ki],[Ta+Lt Ri+Rg+1 0]) % L approximation
```

```
GL_PI2=GL2

% LCL filter transfer function
GLCL=tf([1],[Li*Lg*Cf Cf*(Lg*Ri+Li*Rg) Cf*Rg*Ri+Li+Lg Ri+Rg]) % plant
GLCL_PI=GLCL*G_PI

% Bode plots of the system, options to change into Hz
options = bodeoptions;
options.FreqUnits = 'Hz';

%figure 1 is the L approximation without converter TF added
figure(1)
margin(GL_PI,options)
grid on

%Figure 2 is the L approximation with converter TF added
figure(2)
margin(GL_PI_MO,options)
grid on

%Figure 3 L approx with alternative PI term
figure(3)
margin(GL_PI2,options)
grid on

%Figure 4 is the LCL TF without capacitor damping resistor
figure(4)
margin(GLCL_PI,options)
grid on
```

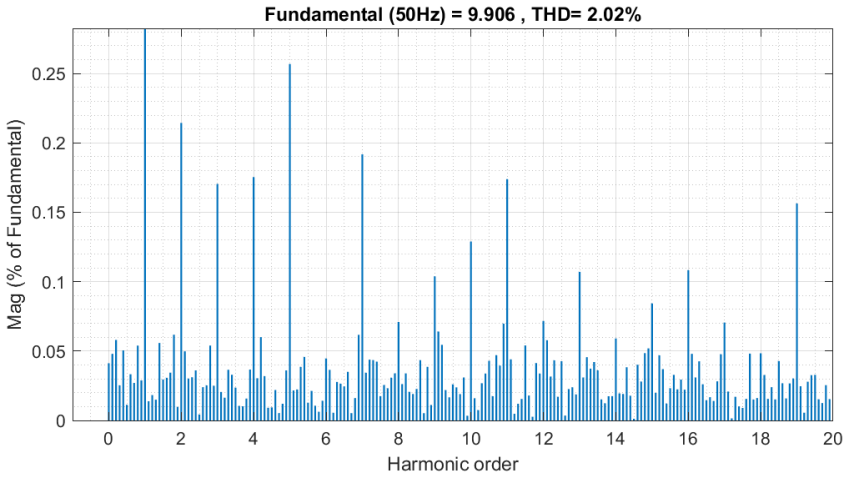
Appendix B

FFT analysis

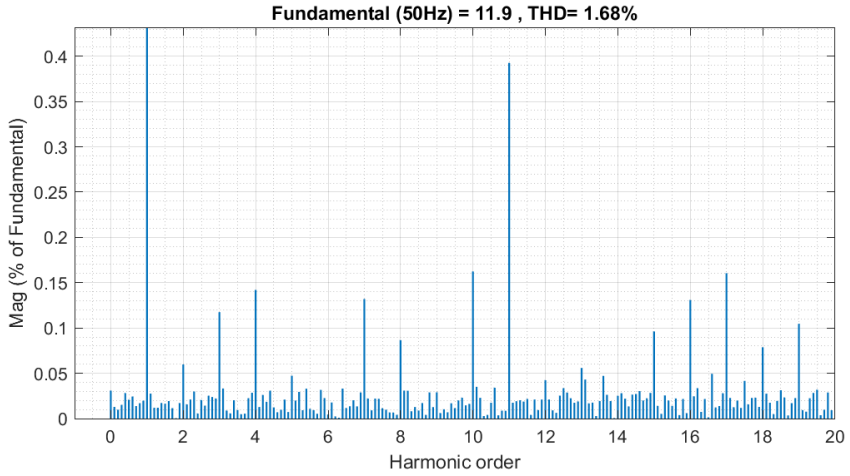
The resulting FFT analysis on the tests conducted in section 5.6

B.1 CCL Test

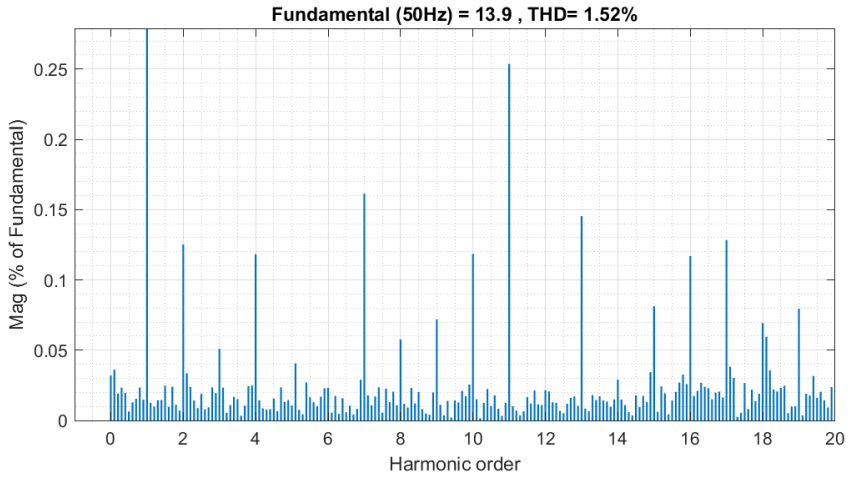
B.1.1 10 A



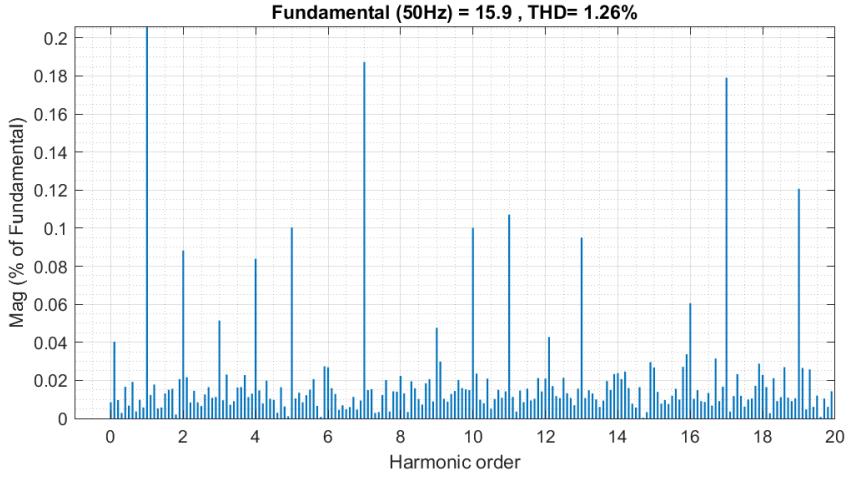
B.1.2 12 A



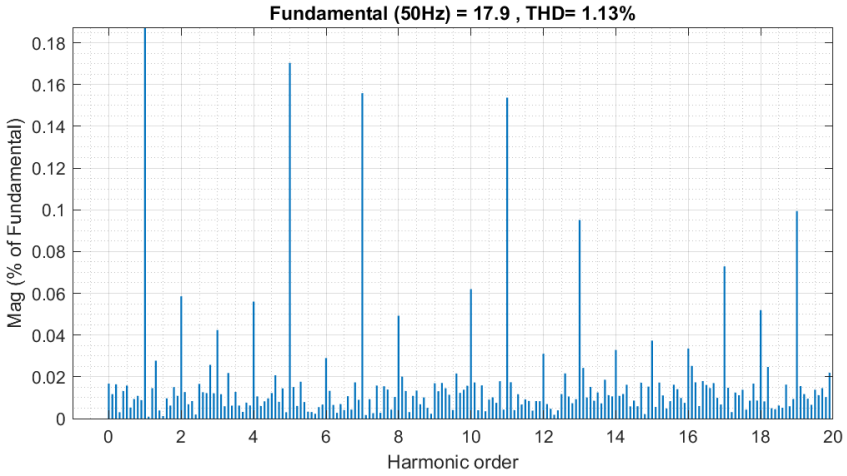
B.1.3 14 A



B.1.4 16 A

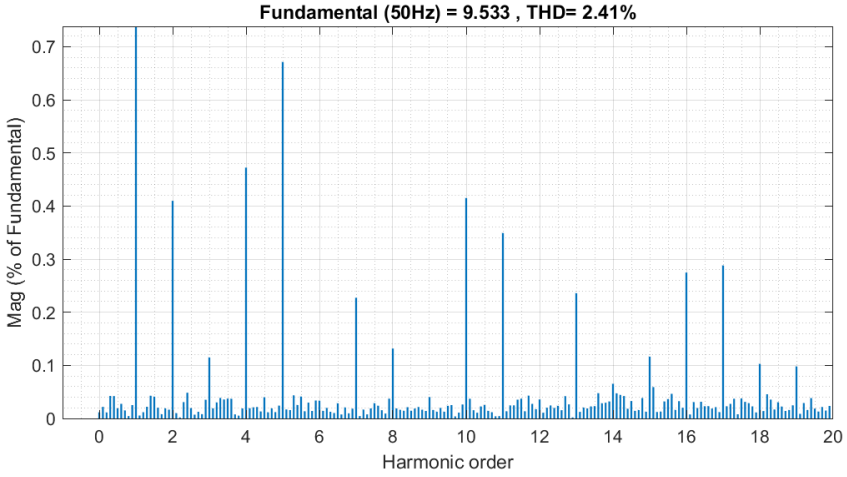


B.1.5 18 A

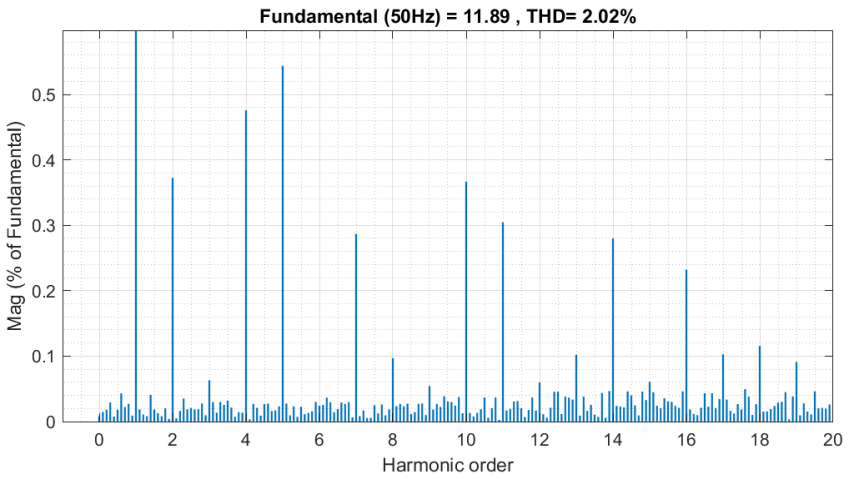


B.2 DPC TEST

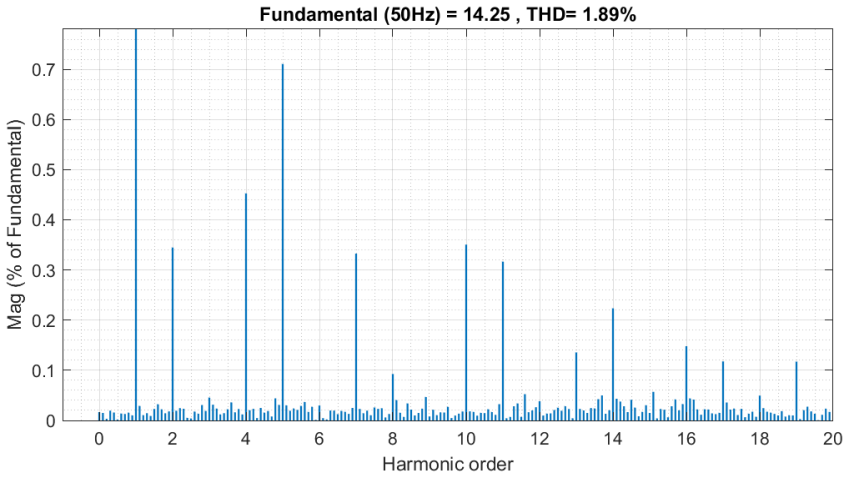
B.2.1 -8 kW



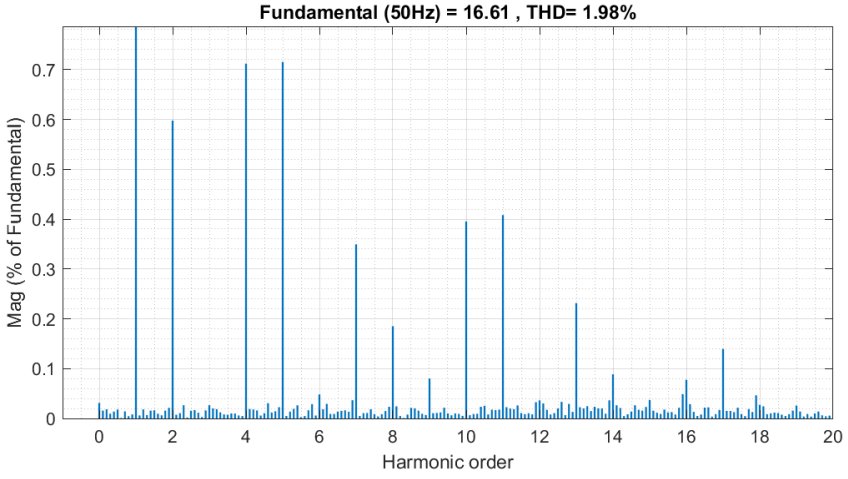
B.2.2 -10 kW



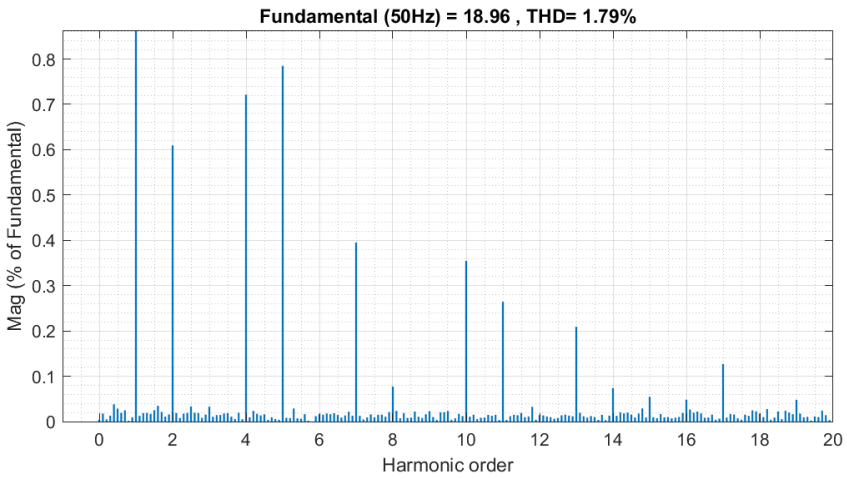
B.2.3 -12 kW



B.2.4 -14 kW

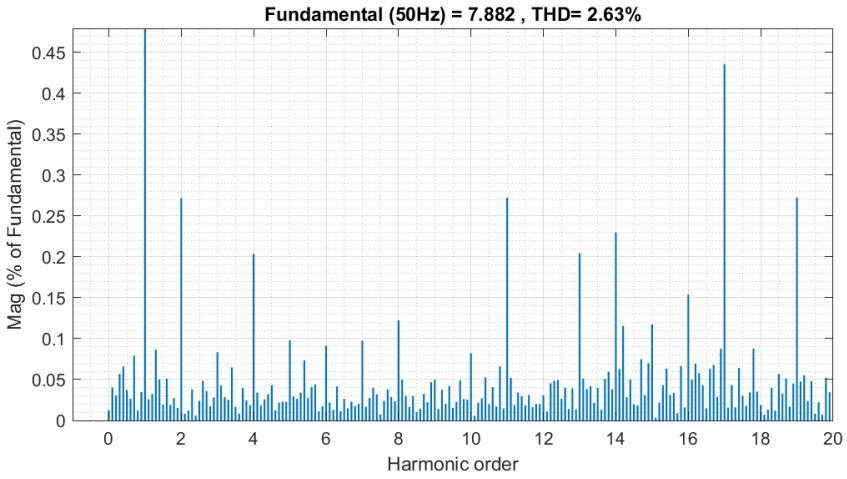


B.2.5 -16 kW

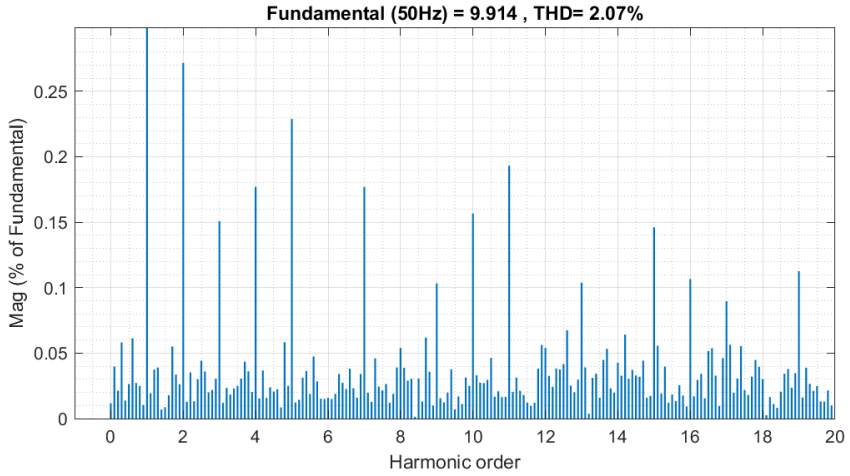


B.3 Inverter operation

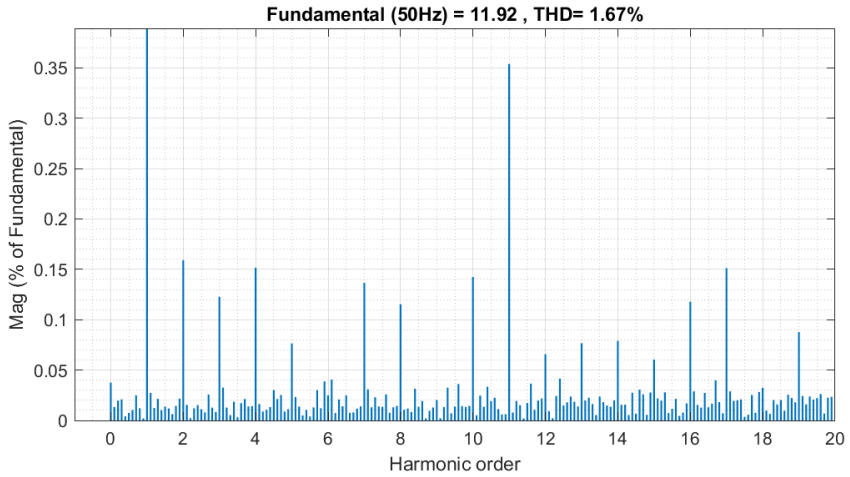
B.3.1 -8 A



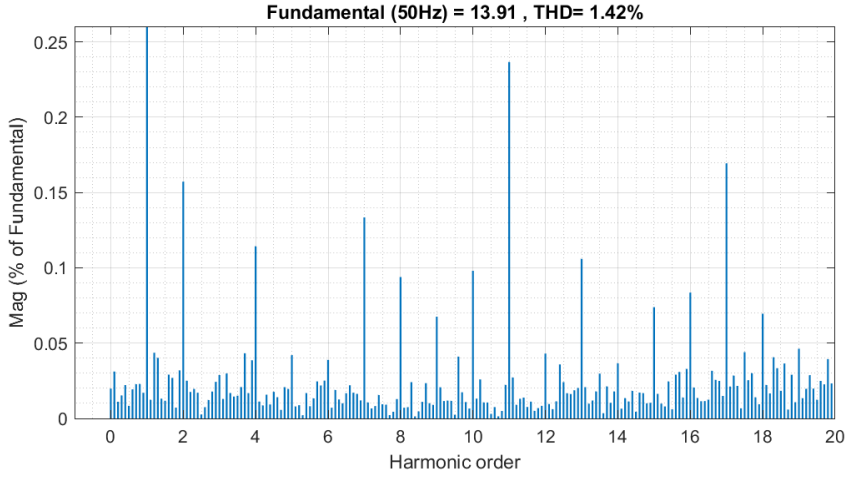
B.3.2 -10 A



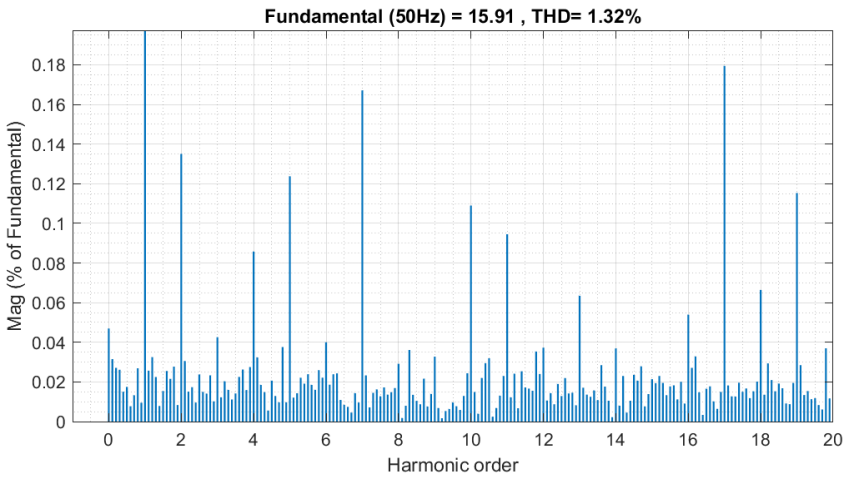
B.3.3 -12 A



B.3.4 -14 A

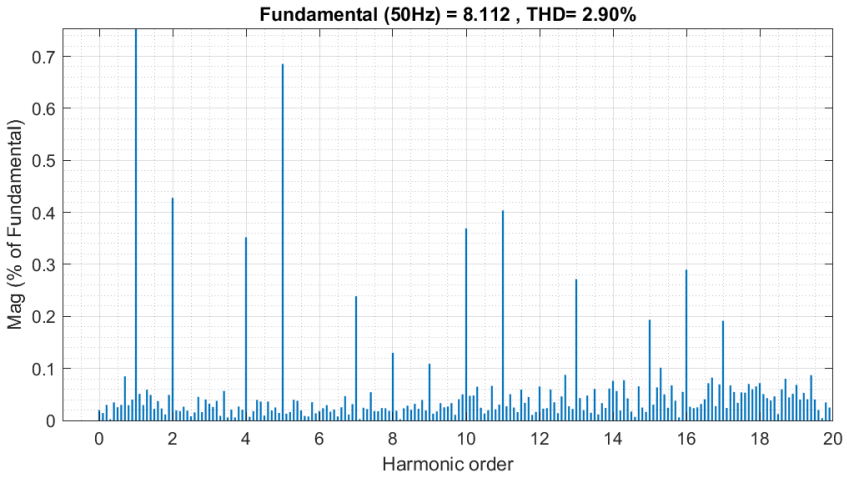


B.3.5 -16 A

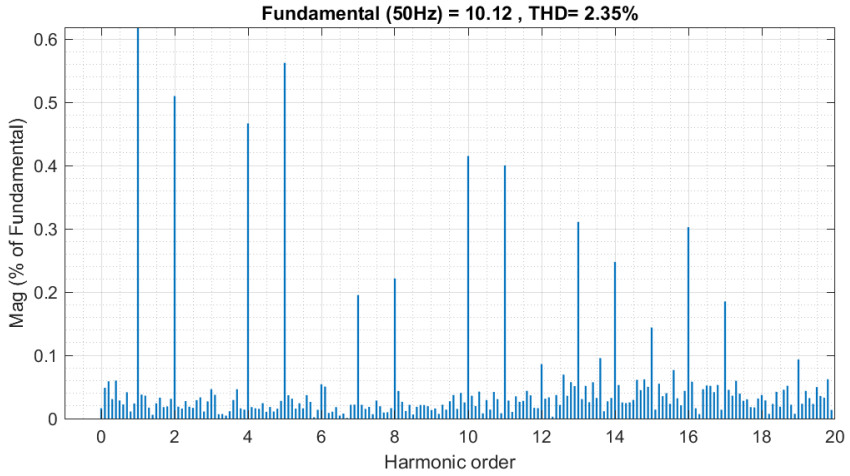


B.4 Rectifying operation

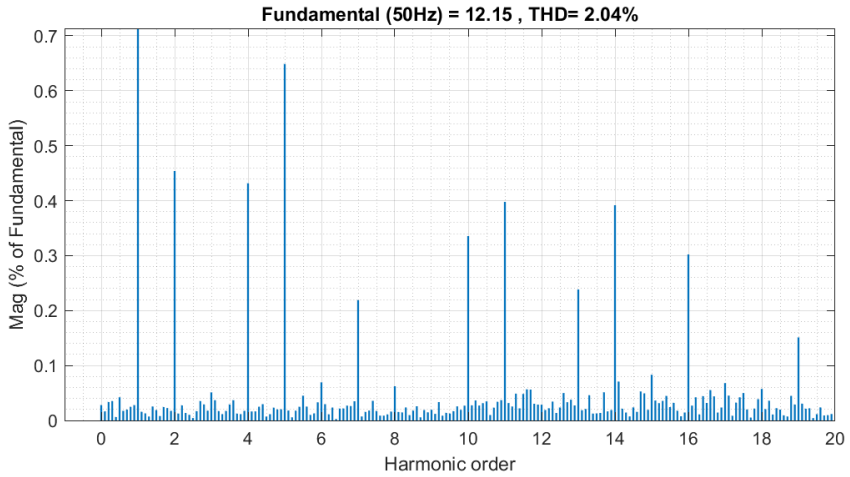
B.4.1 8 A



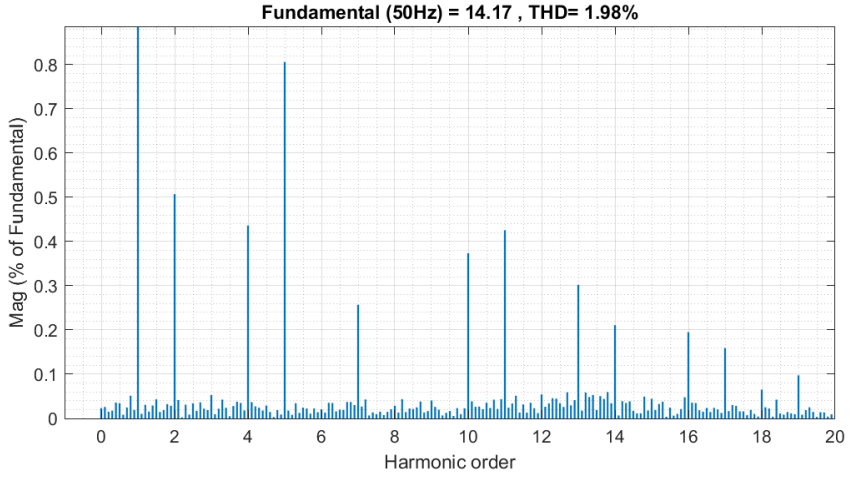
B.4.2 10 A



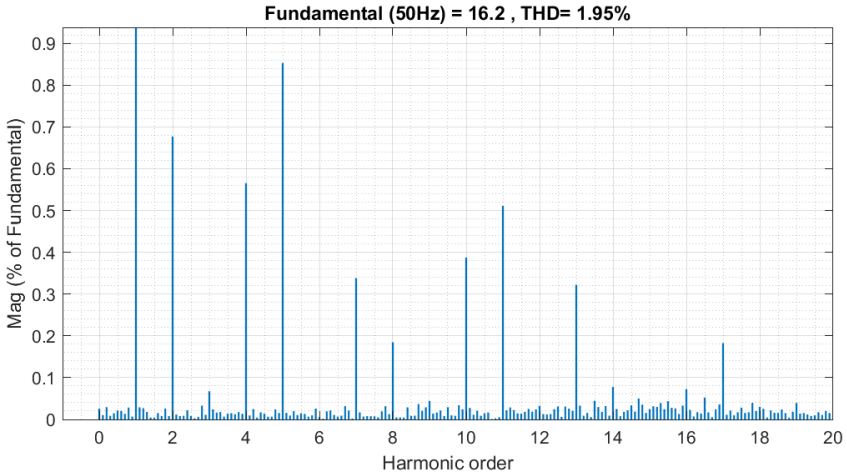
B.4.3 12 A



B.4.4 14 A



B.4.5 16 A

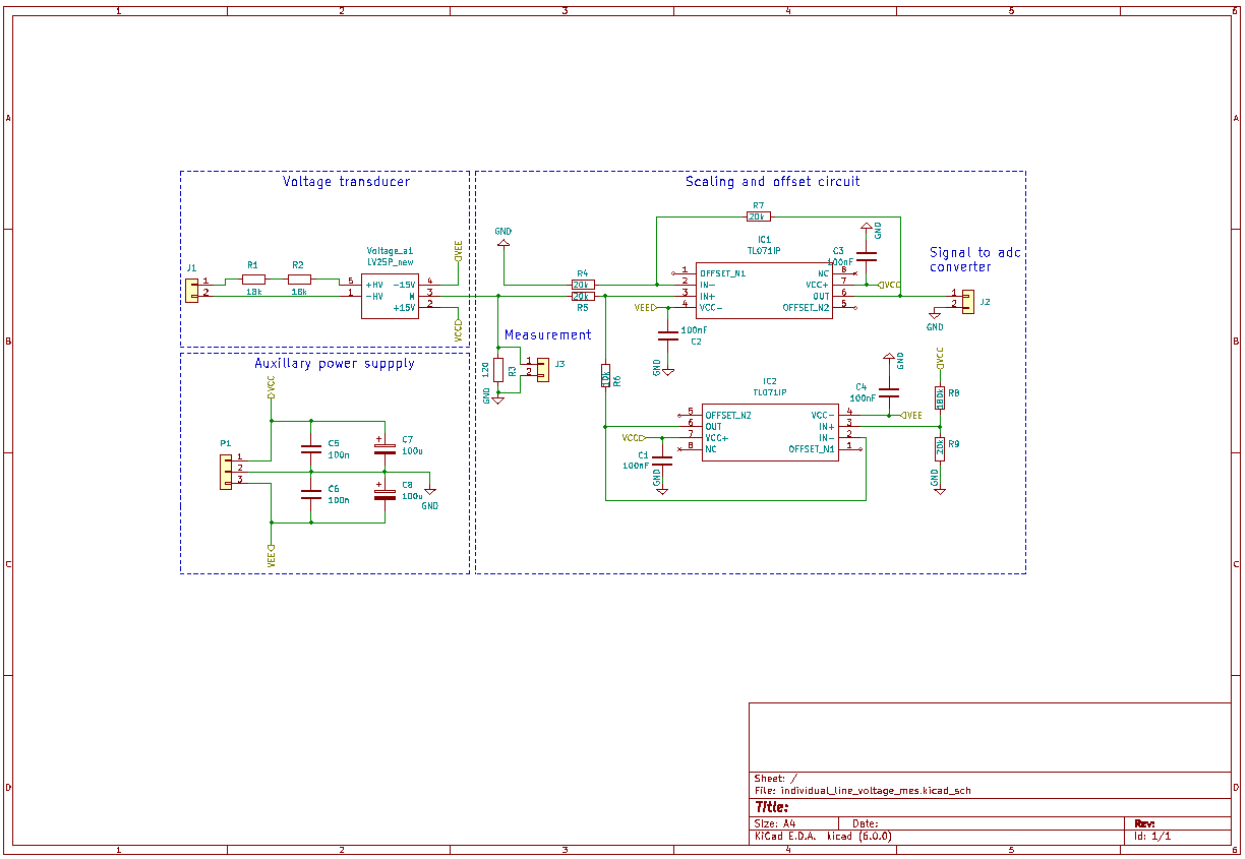

Fundamental (50Hz) = 16.2 , THD= 1.95%
Mag (% of Fundamental)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
0
2
4
6
8
10
12
14
16
18
20
Harmonic order

Appendix C

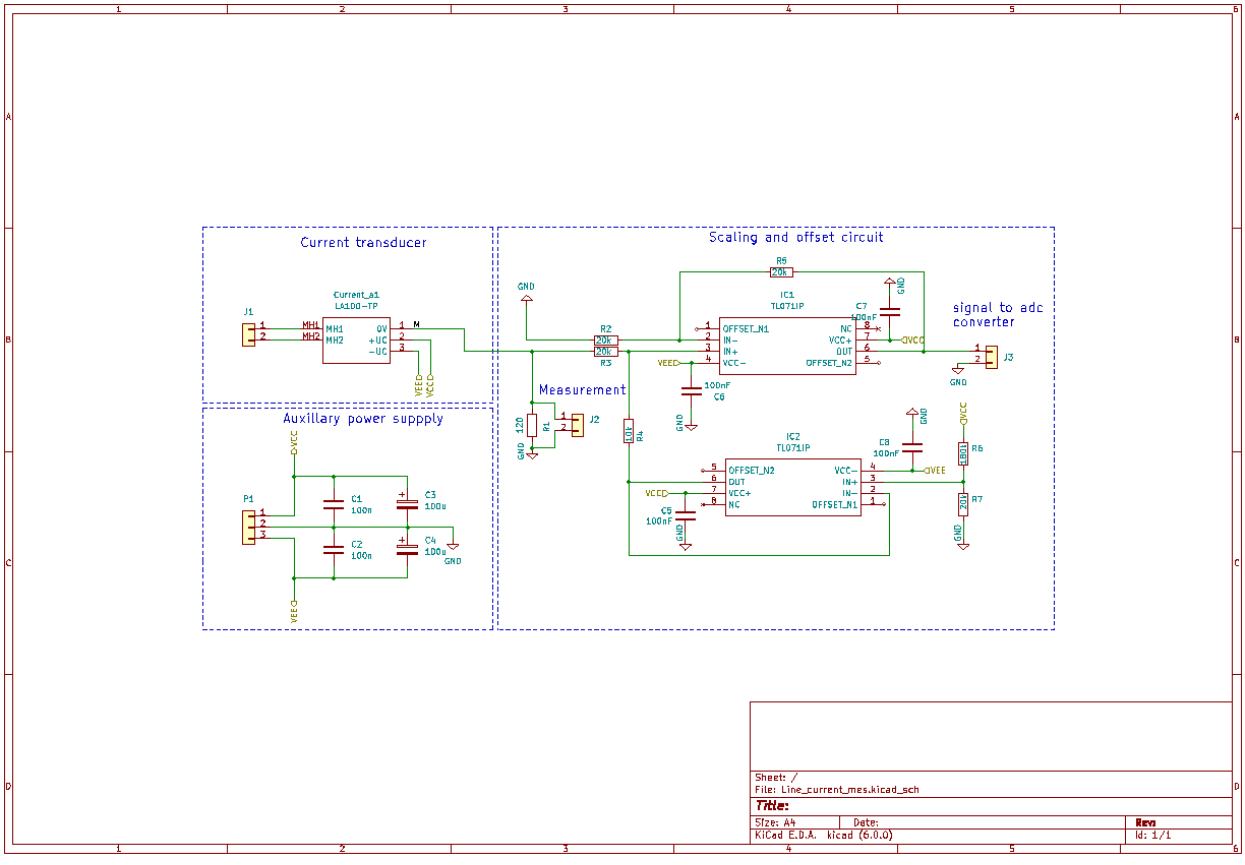
Schematics

The schematic drawings of the different measurement boards PCB circuits is provided in this section.

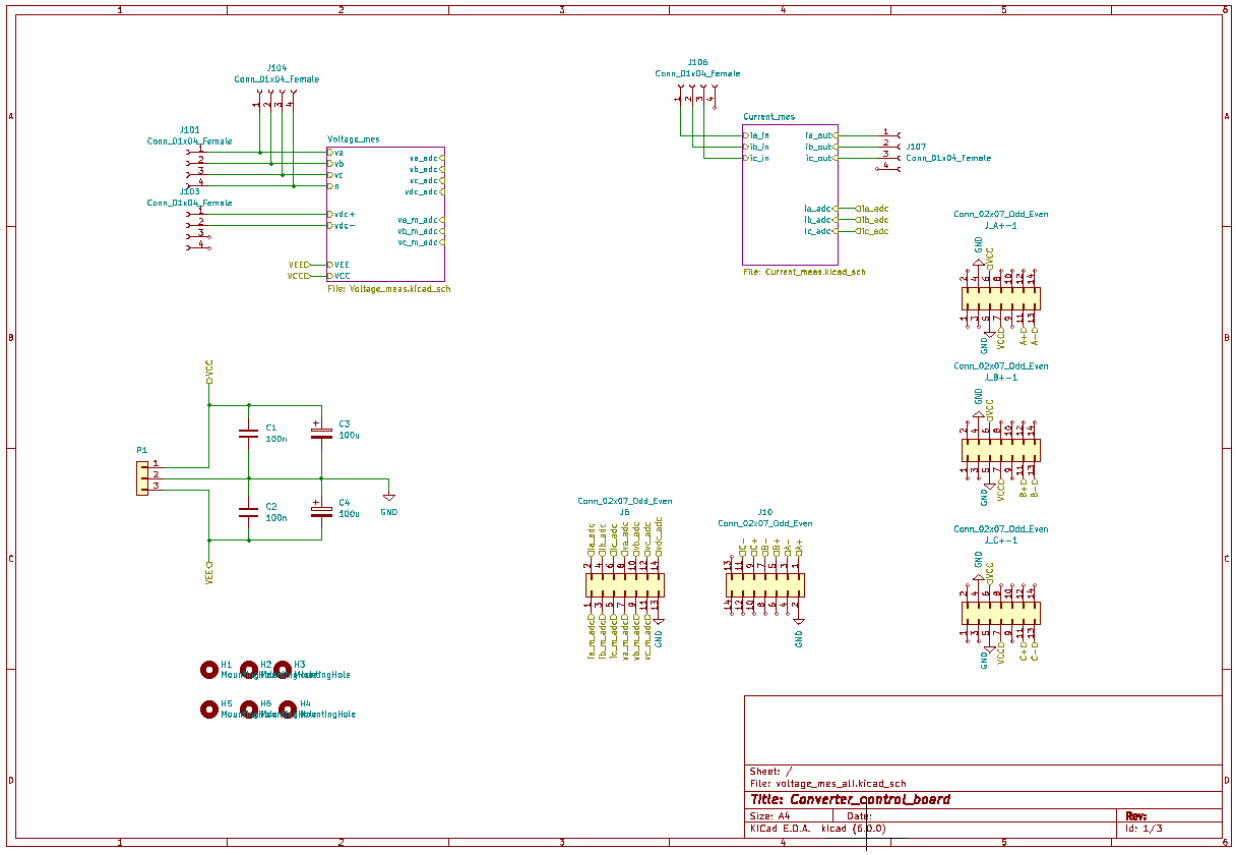
C.1 Voltage Measurement Circuit

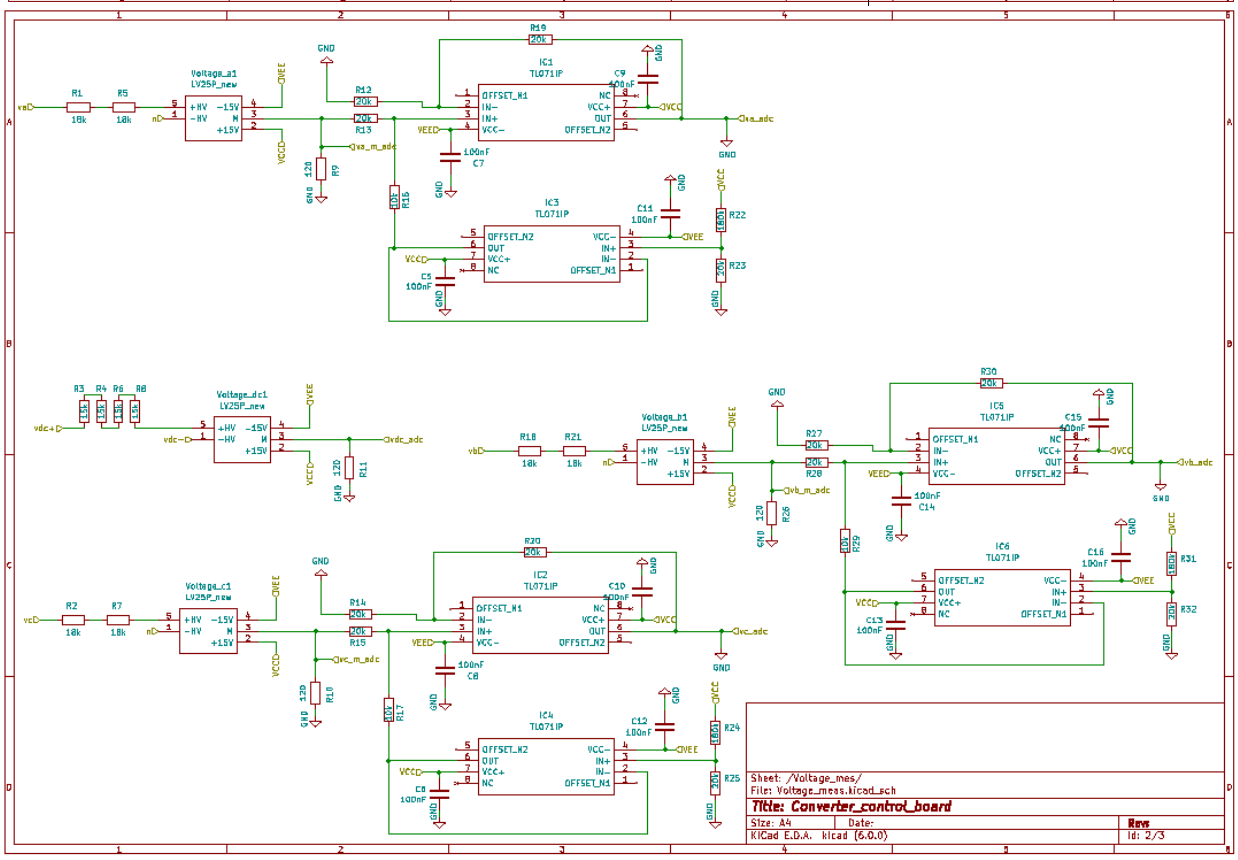


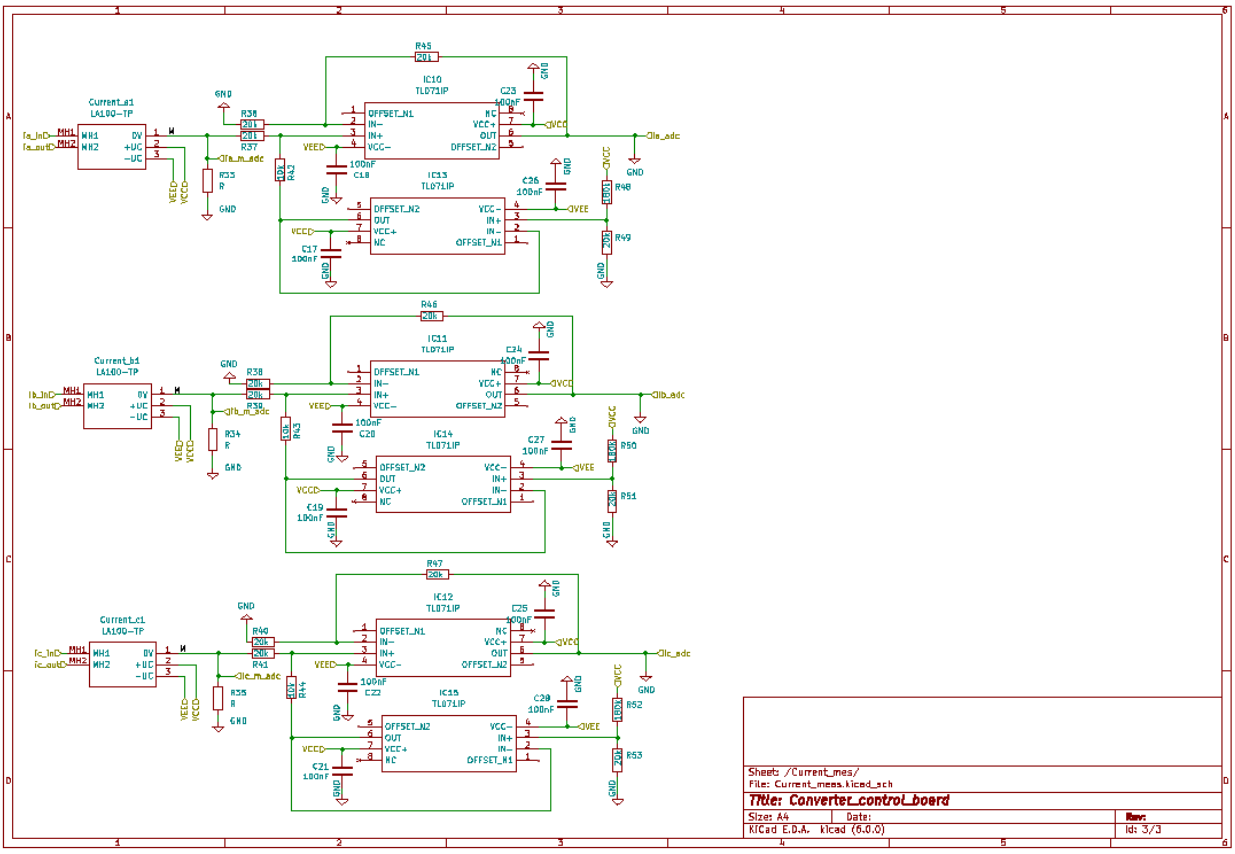
C.2 Current Measurement Circuit



C.3 Converter Control Board






Sheet: /Current_mes/
File: Current_meas.kicad_sch
Title: Converter_control_board
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.0)
Id: 3/3

Appendix D

Datasheets

The datasheets and provided schematics from the supervisor which have been used during this thesis have been listed below. Each of the external links can be accessed by clicking on the respective icon ( ) at the end of each item , provided in the list below. It should be noted that the schematics provided by the supervisor have been bundled together and placed into a GitHub repository.

- AMC3330, Reinforced Isolated Amplifier With Integrated DC/DC Converter
- AMC3301, Reinforced Isolated Amplifier With Integrated DC/DC Converter
- PCB schematics (from supervisor)
- LEM LV-25-P voltage transducer
- LEM LA 100-TP Current transducer
- Semikron IGBT SKM100GB12T4 module
- Semikron transistor driver card SKHI 23/12 (R)