# Design of a 60 GHz Power Amplifier in a 0.13 μm SiGe BiCMOS Process

a thesis by

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for the degree of

Master of Science in Physics


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June 2016

## Abstract

The wide bandwidth in the unlicensed 60 GHz band enable short range wireless data transfer in the order of tens of gigabit per second. This, combined with the relatively low-cost, very high performance SiGe fabrication processes, has led to a feasibility study of a 60 GHz transceiver at Heidelberg University. Such a wireless system is useful in very many applications, and is proposed as the read-out of the future upgraded trackers in the ATLAS detector in the Large Hadron Collider. The work presented here is the design of the power amplifier block in the transceiver.

The power amplifier design consists of three cascaded stages of common emitters, using the heterojunction bipolar transistors in the 0.13 µm SiGe BiCMOS process from IHP. Class AB operation ensures a good trade-off between efficiency and linearity. With load pull simulation, the output impedance was optimized for maximum output power. This was achieved without suffering from a bad output return loss and reflections, because conjugate matching was also attained at the output. Performance simulations yield a power gain of 21.5 dB, a bandwidth of 9 GHz and a peak power added efficiency of 19%. The output referred 1 dB compression point was simulated to 6.5 dBm, for which the amplifier consumes 24 mW.

A layout of the power amplifier circuit measuring 0.15 $mm^2$ is proposed. Verification tests like electromagnetic simulation and corner and yield analysis remain, after which the presented block design can be implemented in the top level design of the transceiver chip.

# Preface

This work has been carried out at the University of Bergen in collaboration with Hans Kristian Soltveit at the Physikalisches Institut, Heidelberg University. Radio frequency electronics is a fairly new field for the microelectronics group at the University of Bergen, where a fellow student of mine, Magnus Pallesen, and I took the challenge of designing two blocks of an integrated 60 GHz transceiver. We had no previous knowledge in microwave engineering, and much time was dedicated to learning the theory and new design techniques. This thesis covers my work on the main and final project of my master's degree, which started August 2015.

## Acknowledgments

First and foremost I would like to thank my supervisor Kjetil Ullaland for his guidance and support. My gratitude also goes to Hans Kristian Soltveit for making this project possible, for his encouragement and for sharing his vast ASIC design experience. I would like to acknowledge Yngve Thodesen at the Royal Norwegian Naval Academy, his help and guidance on RF design has been invaluable.

I will also recognize my friends and fellow students for two good years at the university. Special thanks to Magnus Pallesen for good teamwork in mastering new fields of electronics. I am also thankful for the support and motivation I have received from family and friends throughout the work.

Hans Schou
Bergen, June 2016

# Contents

CHAPTER 1

# Introduction

The demand for wireless electronics is ever increasing as more and more gadgets are connected wirelessly, and technological devices are being improved constantly. This drives the research and development of tomorrow's electronics, and the performance of wireless technology is advanced in all possible aspects. To mention a few, the data transfer rates are improved for faster communication, and better efficiency allows for smaller batteries in handheld devices. There is always a trade-off between performance and cost, but positive trends are apparent regarding this as well.

Wireless technology is usually utilized to allow a device to be mobile. However, the advancements made in radio frequency electronics has in some specific applications enabled wireless data transmission to outperform the traditional wired connections. The work presented in this thesis is a part of a feasibility study of a 60 GHz wireless system for applications requiring short range multi-gigabit data transfer.

## 1.1 Background and Motivation

The European Organization for Nuclear Research (CERN[1]) is upgrading the ATLAS silicon micro-strip trackers in the Large Hadron Collider (LHC). The trackers are detecting the trajectory, momentum and energy of new particles created in a collision of particles[21]. A full read-out of the upgraded detector will require a data transfer rate of 50-100 Tb/s. The optical links of current trackers restrict the data bandwidth due to limitations in power budget, mass and physical measures [5]. The feasibility of 60 GHz wireless data transfer is being studied at Heidelberg University [28], and this work is a part of the development of a prototype in that study.

[1] An acronym for the French *Conseil Europen pour la Recherche Nuclaire*.

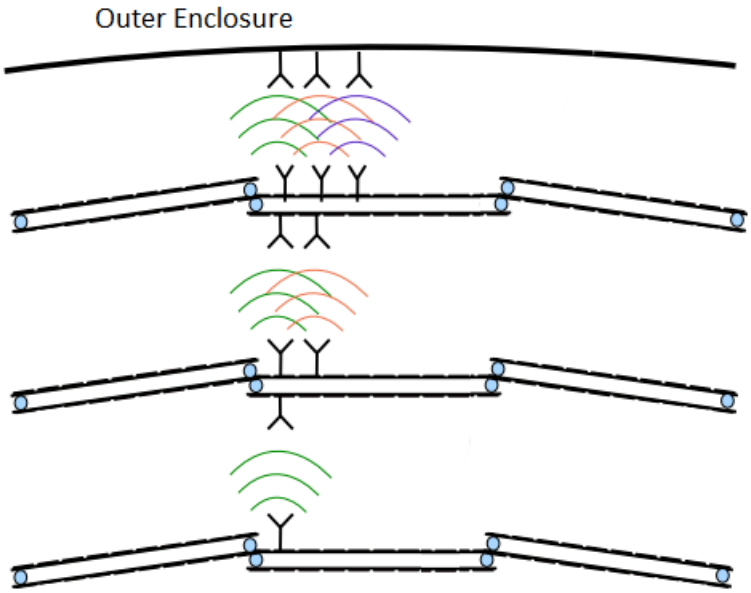



**Figure 1.1:** A cross-section of the trackers layered around the collision point. The antennas illustrate the radial read-out of each tracker [28].

Figure 1.1 illustrates the detectors placed in layers around the collision point, and the proposed radial wireless readout of the tracker data. Each layer detects particles as they traverse the trackers towards the outer enclosure. Data recorded by the detectors must be read out, for which the proposal is a wireless radial read-out. The distance between the tracker layers are approximately 10 cm. The silicon trackers attenuate millimeter waves,[2] which is why the signal is brought through subsequent trackers by additional sets of antennas.

### 1.1.1 Wireless Systems

In order to communicate wirelessly, a radio transmitter and receiver (combined they are called a transceiver) are necessary, both of which are shown in Figure 1.2. To transmit, the data signal is modulated and mixed to a carrier frequency supplied by a local oscillator. The mixed signal is then amplified by a power amplifier and filtered before it is transmitted by the antenna.

An antenna picks up the signal that has weakened in strength during transmission to the receiver. The signal must be amplified and discriminated from noise by a low noise amplifier. Then the signal is filtered and down-converted with a mixer. Once the signal is demodulated, it should be the same as the data signal that was provided

[2]Millimeter waves range from 30 GHz to 300 GHz, where the wavelengths range from 10 mm to 1 mm, respectively.

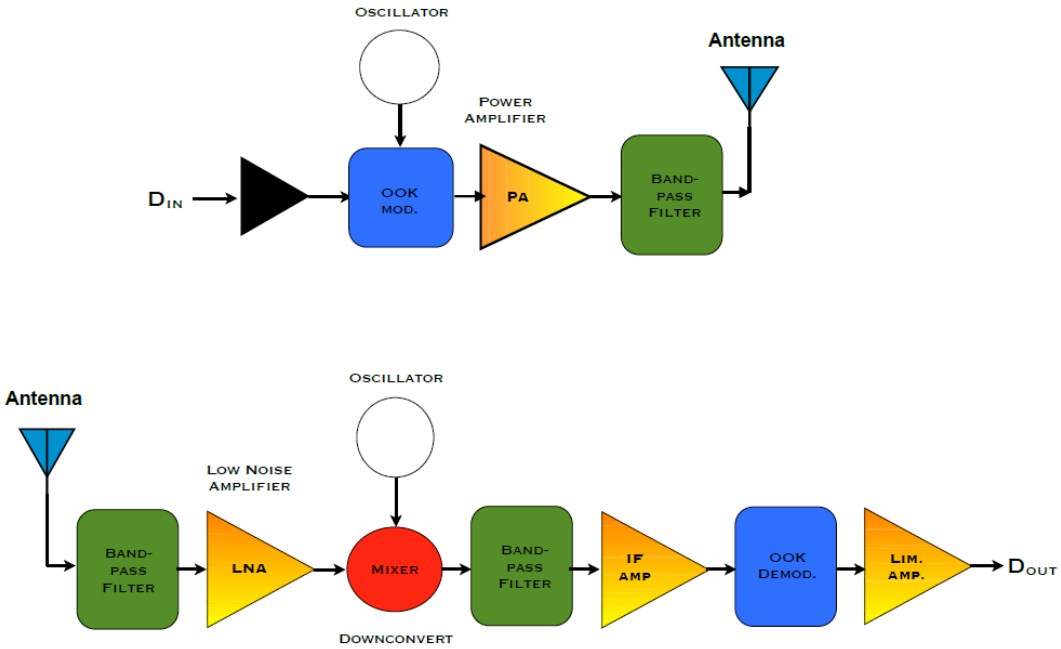



**Figure 1.2:** The basic building blocks of a transmitter (top) and a receiver [28].

to the transmitter to begin with. The transmission depends on the performance of all the system blocks not to lose too much information.

### 1.1.2 Why 60 GHz?

With the increasing number of wireless devices and their rising performance requirements, the usable frequency spectrum is very crowded. Large parts of the spectrum are licensed, and the allocated bands for specific applications require very advanced modulation techniques to enable high data transfer rates. Communication is also heavily encoded to reduce interference between different channels in the same band [1].

Advances in technology increase the useable spectrum by enabling wireless systems to utilize frequencies far into the GHz-range, at fairly low cost. The globally unlicensed 60 GHz band varies in some regions, as shown in Figure 1.3, but most of these regions have a total bandwidth of 7 GHz. This enables very high data transfer rates. Dependent on the modulation scheme, 7 GHz bandwidth is capable of tens of gigabits per second.[3]

Higher carrier frequency increases the free space path loss and the signal attenuation in materials. This means shorter transmission range and that the receiver should

[3] 16-QAM (quadrature amplitude modulation), with its spectral efficiency of 4 bps per hertz, is capable of 28 Gbps. On-off keying can provide 3.5 Gbps at the same bandwidth.

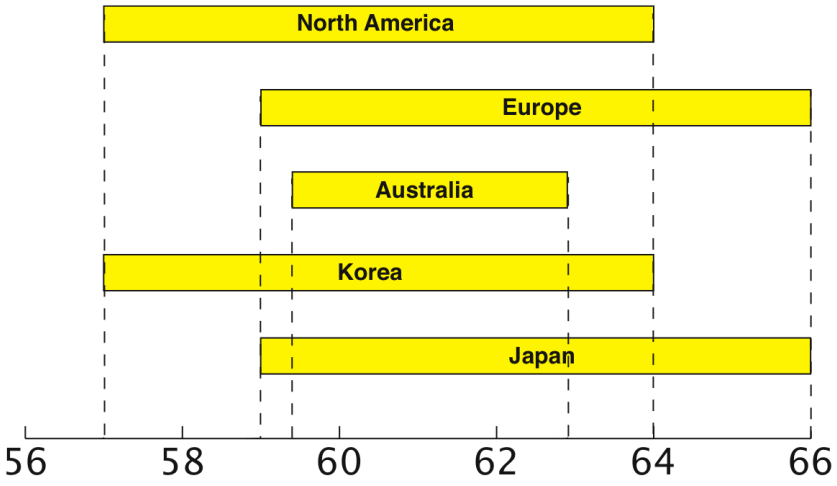



**Figure 1.3:** The unlicensed spectrum around 60 GHz for different regions [10].

be in the line of sight from the transmitter. These disadvantages are considered advantages in applications with short transmission ranges; high attenuation reduces the likelihood of interference of separate systems. Short range transmission is also less susceptible to eavesdropping since the receiver has to be fairly close to the transmitter.

The short wavelength of 60 GHz (5 mm in vacuum), enables very small antenna dimensions. In some applications, the antenna can be integrated on chip, acquiring a remarkably small form factor of the wireless system.

## 1.2 Power Amplifier Design Goals

The goal of this work is to design a power amplifier, shown as the last active block of the transmitter in Figure 1.2. It is responsible for providing the antenna with a signal strong enough to be picked up by the antenna in the receiver. To do so, the power amplifier in this work must be designed to meet the requirements listed in Table 1.1, which is the main goal. The power gain and 1 dB compression point is specified for the center frequency, 61.5 GHz. The power amplifier should be ready to be integrated on the transceiver chip with the other system blocks. Electromagnetic simulation should verify the performance of the power amplifier. The fabrication technology chosen for the chip is the 0.13 µm SiGe BiCMOS process provided by IHP Microelectronics.

The obtained bandwidth is defined by where the reflection coefficients, $S_{11}$ and $S_{22}$ are within specification. Inside the passband, the gain should be as flat as possible, and outside it, the gain should be kept at a minimum. The input and output should both be matched to 50 Ω.

**Table 1.1:** The required performance specifications for the PA.

| Specification | Goal | Unit |
|---|---|---|
| Power gain ($S_{21}$) | 20 | dB |
| 1 dB compression point | >5 | dBm |
| Power consumption | <30 | mW |
| Bandwidth | 57 - 66 | GHz |
| Input reflection coefficient($S_{11}$) | <10 | dB |
| Output reflection coefficient($S_{22}$) | <10 | dB |

## 1.3 Outline of the Thesis

The thesis is organized as follows:

**Chapter 2** introduces the silicon germanium process technology and the fabrication process chosen for the chip in this work.

**Chapter 3** comprises microwave theory necessary for the electronics engineer to design high-frequency electronics.

**Chapter 4** is all about microwave amplifier design in general and some considerations specific to power amplifiers.

**Chapter 5** describes the circuit design of the power amplifier presented in this work.

**Chapter 6** continues with the design from Chapter 5 with realistically modeled circuit elements. Finally, the layout is presented.

**Chapter 7** is a discussion of the work.

**Chapter 8** concludes the thesis.

CHAPTER 2

# Process Technology

This chapter briefly introduces Silicon Germanium (SiGe) as a semiconductor material. The characteristics of the chosen technology from IHP is then described.

## 2.1 The SiGe HBT

Silicon is the preferred semiconductor in many applications because of good yield, low cost and many manufacturing advantages. However, the charge carrier mobility of silicon is relatively low, resulting in slow speed compared to III-V semiconductors.[1] III-V devices generally has better mobility and enables bandgap engineering, making them tailorable for specific applications [8]. The good analog and microwave performance of III-V technologies comes at a cost of poor integration and expensive fabrication. Due to fabrication difficulties (some mentioned below), the growth of SiGe epitaxy was a theory for nearly 30 years, before it was accomplished practically in 1985 [8]. The SiGe Heterojunction Bipolar Transistor (HBT) benefits from the same advantages of both silicon and III-V devices.

The lattice constant of germanium is about 4.2% larger than that of silicon, and an alloy of the two will have a lattice constant somewhere in between their initial values. Depositing SiGe on silicon will introduce compressive strain on the SiGe because it must adopt the lattice constant of the silicon. If the deposited SiGe film is unstable, it will relax to its natural lattice constant. This movement breaks the crystallinity, which ultimately reduces yield. SiGe relaxation happens if the strain energy is too high and this restricts the film thickness. Combining silicon and germanium enables

[1] III-V denotes compound semiconductors made of elements from group three and five in the periodic table, e.g. GaAs, GaN and InP. Both Si and Ge are group four elements.

bandgap engineering because the energy bandgap of silicon is larger than that of germanium (1.12 eV vs. 0.66 eV). With increasing amounts of germanium in the SiGe compound, the bandgap of SiGe will shrink compared to that of pure silicon [8].

Both the smaller bandgap and the compressive strain contribute to a larger carrier mobility. SiGe HBT allows a less doped emitter and a more doped base compared to silicon Bipolar Junction Transistor (BJT), increasing transistor performance [14]. SiGe HBT also has a low turn-on voltage (0.8 V compared to about 1.2 V for GaAs HBT) [13], enabling a lower operating voltage. SiGe BiCMOS[2] is good for Monolitic Microwave Integrated Circuits (MMICs) design because it enables integration of high performance Radio Frequency (RF) and analog circuitry (with SiGe HBT) and low power logic and high density memory (with Si CMOS) on a single chip, which is very cost-effective [8].

## 2.2 IHP SG13S

IHP (Innovations for High Performance Microelectronics) is an institute that conducts research and development of silicon-based ultra high-frequency circuits and technology. IHP SG13S is the fabrication process chosen for the development in this work. It is a 0.13 µm SiGe HBT BiCMOS technology that provides excellent performance at high frequencies with HBTs and is suitable for a single-chip 60 GHz transceiver. The process provides seven layers of aluminum and an additional *MIM-layer*[3] as illustrated in Figure 2.1. The insulator is silicon dioxide with a relative dielectric constant of 4.1.

### 2.2.1 Bipolar Transistors

SG13S has a bipolar module that enables the use of three npn transistors. The one used in this work is called *npn13p* and its key features are listed in Table 2.1. It has a BEC layout configuration as illustrated in Figure 2.2, which also shows the configuration of *npn13pl2*. The latter has a CBEBC layout configuration, which has a decreased base resistance per emitter length compared to BEC. This is important for high power applications that require a long emitter, because the base resistance increases with emitter length. Other than a different configuration and limitations to the layout, these two BJTs seems to be very similar. However, IHP recommends using npn13p over npn13pl2 for most applications, except for when very high power

[2]BiCMOS is a technology that combines bipolar transistors and Complementary Metal Oxide Semiconductor (CMOS) for better integration.

[3]The MIM-layer constructs a metal-insulator-metal-capacitor with Metal 5.

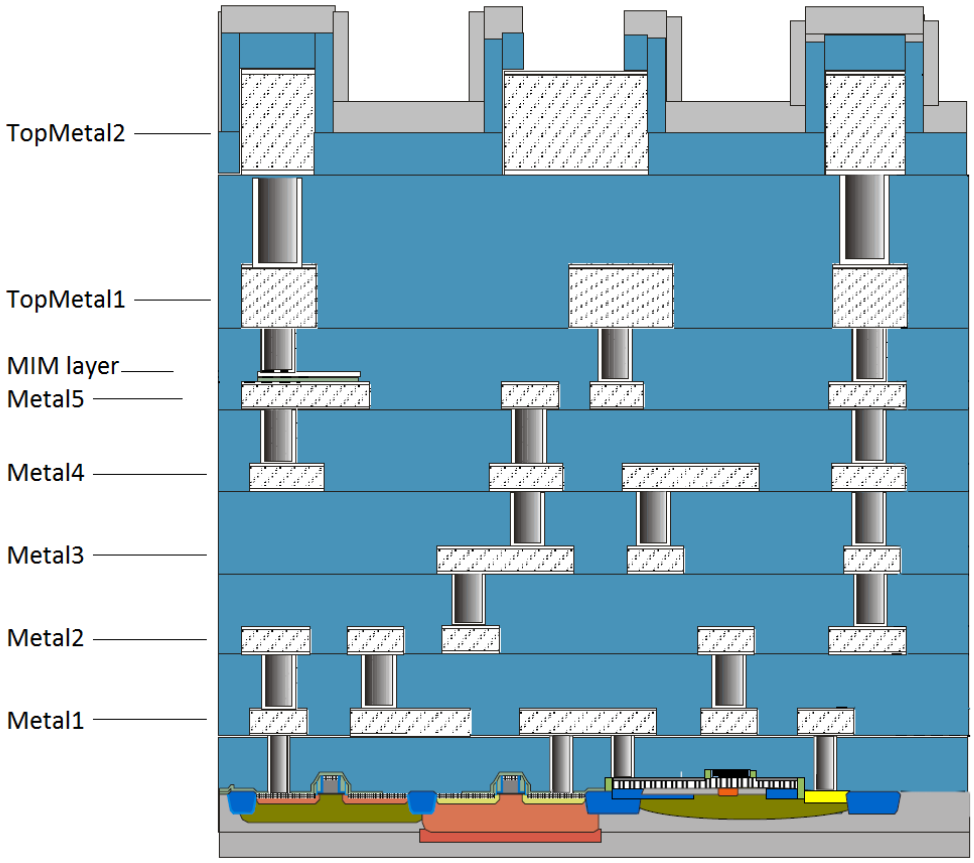
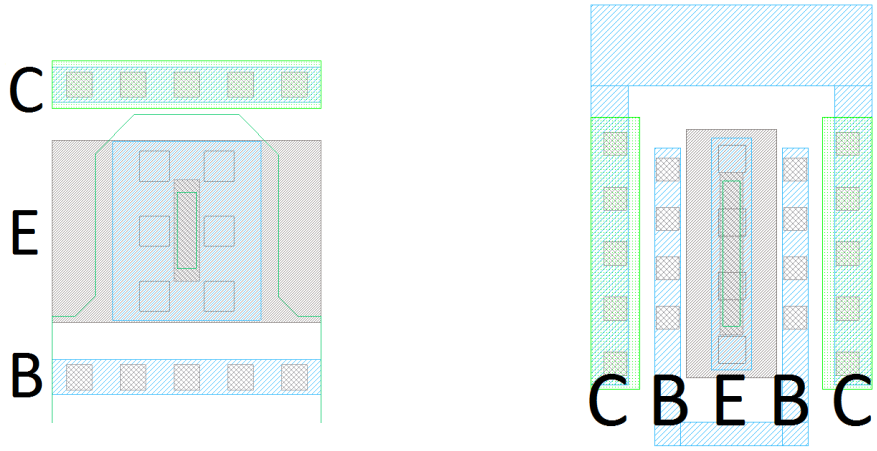



**Figure 2.1:** A cross-section of the SG13S process stack-up (not to scale) [16] (disclosed with permission from IHP).

**Table 2.1:** Key figures for the SG13S bipolar transistor npn13p [15].

| Parameter | Target | Unit |
|---|---|---|
| Emitter area | 0.12 x 0.48 | $\mu m^2$ |
| Peak $f_{max}$ | 340 | GHz |
| Peak $f_T$ | 250 | GHz |
| $BV_{CEO}$ | 1.7 | V |
| $BV_{CBO}$ | 5.0 | V |
| *Beta* | 900 | - |

is needed. The third BJT is made for high voltages and is of no use for 60 GHz devices since it has a transition frequency of about 50 GHz [15].




(a) (b)

**Figure 2.2:** Transistor layout, (a) shows the npn13p with its BEC configuration, and (b) is the npn13pl2 which is configured as CBEBC (not to scale).

### 2.2.2 Passive Components in IHP SG13S

In high frequency circuit design, signal loss and noise pose as problematic. Resistors are thus avoided when possible. On the contrary, capacitance and inductance are crucial and need to be realized either with lumped elements or with transmission lines (explained in section 3.1). The lumped elements (resistors, capacitors, inductors) included in the SG13S library are briefly described here.

There are three resistors available in SG13S that cover a wide range of sheet resistance as listed in Table 2.2. Included in the SG13S process library is a MIM capacitor. It is basically a parallel plate capacitor utilizing Metal5 and MIM layer achieving a high specific area capacitance of 1.5 fF/$\mu m^2$ [15].

There is an inductor model in the SG13S library. It is not documented, but it is apparent in the layout that the inductor is placed in TopMetal2 with connections in TopMetal1 (see Figure 2.1 for layer details). Physical constraints in TM2 render the smallest possible inductor quite large, thus, its benefit to very high frequency applications is limited.

**Table 2.2:** The resistors in SG13S library [15].

| Name | Sheet resistance | Resistor material |
|---|---|---|
| Rsil | - | N+ polysilicon |
| Rppd | 250 Ω | P+ polysilicon |
| Rhigh | 1300 Ω | High polysilicon |

CHAPTER 3

# Microwave Theory

Radio frequencies introduces many new aspects to conventional electronics that the circuit designer should keep in mind. This chapter is intended to give insight to basic principles essential to high-frequency circuit design.

## 3.1 Transmission Lines

At high frequencies, signal wavelengths become comparable to the physical size of the circuit elements. When a structure is more than a tenth of the wavelength, it is normal to consider them comparable [32]. In this regime of operating frequency, circuit elements must be treated as distributed rather than lumped. In lumped elements, voltages and currents do not vary over the element's physical length. A transmission line is a distributed element, in which voltages and currents do vary in magnitude and phase over its physical length [25]. In [32] a transmission line is defined as *a set of conductors that are long compared to a wavelength and have a uniform cross section along their length for which a characteristic impedance $Z_0$ can be defined.* This section describes the behavior of transmission lines. The proof of this can be derived with two methods, from a specialization of Maxwell's equations and from circuit theory, however, only the latter is derived here. Most literature on microwave engineering (e.g. [18], [24], [32]) describe both methods.

### 3.1.1 Telegrapher Equations

A transmission line is shown between the source and load impedances in Figure 3.1 (a). Illustrated in Figure 3.1 (b) is the equivalent lumped-element circuit model for

an infinitesimal length of transmission line, where all the elements are quantities *per unit length*. The inductance $L$ represents the lead inductance and the series resistance $R$ models the finite conductivity of the conductors. The shunt capacitor $C$ models the adjacency of the conductors and the shunt conductance $G$ represents dielectric loss between the conductors [24]. By applying Kirchhoff's voltage and current laws to the circuit of Figure 3.1 (b), the following two expressions are derived:

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0, \tag{3.1a}$$

$$i(z,t) - G\Delta z v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0. \tag{3.1b}$$

By dividing (3.1) by $\Delta z$ and let $\Delta z \to 0$, what is left are the differential equations:

$$\frac{\partial v(z,t}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t}, \tag{3.2a}$$

$$\frac{\partial i(z,t}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t}. \tag{3.2b}$$

Equations (3.2a) and (3.2b) are called the *telegrapher equations*, and are the time domain form of transmission line equations [24]. Note that this analysis may be applied to any waveform [32].

### 3.1.2 Travelling Waves on a Transmission Line

From (3.2) it can be shown that the wave equations for a transmission line are

$$V(z) = V_{I0}e^{-\gamma z} + V_{R0}e^{\gamma z}, \tag{3.3a}$$

$$I(z) = I_{I0}e^{-\gamma z} + I_{R0}e^{\gamma z}, \tag{3.3b}$$

where $\gamma$ is the complex propagation constant:

$$\gamma = \sqrt{(R+j\omega L)(G+j\omega C)} \tag{3.4}$$

and where $V_0$ and $I_0$ are the voltage and current at distance $z = 0$. The voltage and current waves labeled $_I$ and $_R$ denotes the *incident* and *reflected* waves respectively.

The characteristic impedance can be found to be

$$Z_0 = \frac{\gamma}{R+j\omega L} = \sqrt{\frac{R+j\omega L}{G+j\omega C}}. \tag{3.5}$$

If a transmission line is terminated at its characteristic impedance, no reflections will occur. The loss is often ignorable, and then the characteristic impedance reduces to

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{3.6}$$

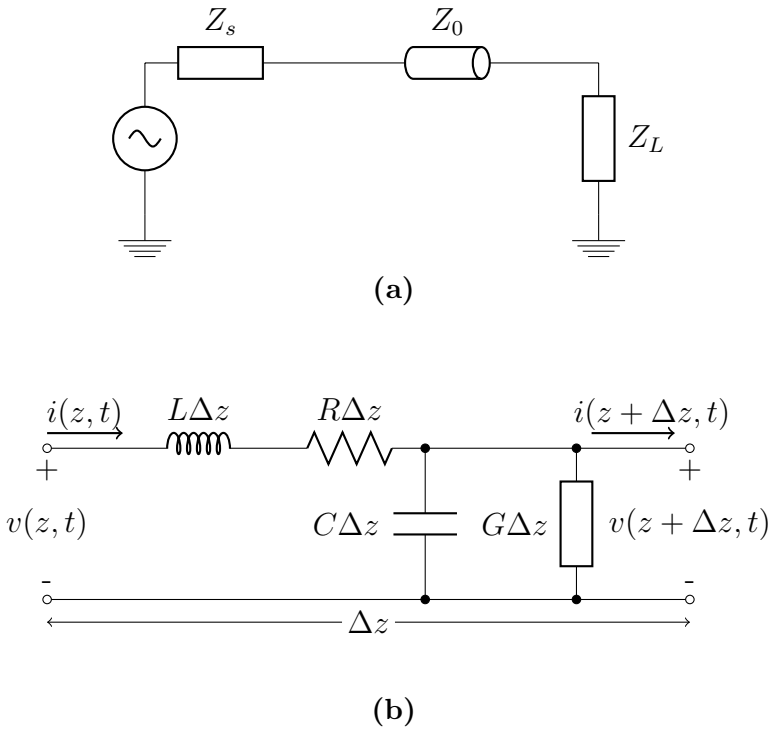



**Figure 3.1:** (a) illustrates a general transmission line network and (b) is a lumped circuit model of an infinitesimal length of transmission line.

A lossless transmission line terminated in an open circuit will reflect the entire incident signal back towards the generator. This is illustrated in Figure 3.2 (a), where $Z_G = Z_0$ which means the entire reflected signal is absorbed in the source impedance. If a continuous sine wave is applied to the line and the length of the line is *a multiple of half a wavelength*, standing voltage waves will occur as in Figure 3.2 (b). The maxima take place when $V_I$ and $V_R$ are in phase, and minima when they are out of phase. The distance between maxima and minima is half a wavelength, this is because their opposite propagation direction doubles their relative velocities [32]. The voltage at any point on the transmission line is the sum of $V_I$ and $V_R$, and varies from zero to the double of the signal amplitude. The current is $2I_A$ at its maximum (where $I_A = V_A/Z_0$) when the voltage is at its minimum, and at a voltage maximum, the current is zero.

A wave propagates at the speed of light if the conductor is surrounded by vacuum, which has a dielectric constant $\epsilon_R = 1$. The propagation velocity is reduced in proportion to the square root of $\epsilon_R$ of the dielectric medium. Thus, the effective wavelength $\lambda$ is reduced to the same proportion:

$$\lambda = \frac{\lambda_0}{\sqrt{\epsilon_R}}, \tag{3.7}$$

where $\lambda_0$ is the wavelength in vacuum.

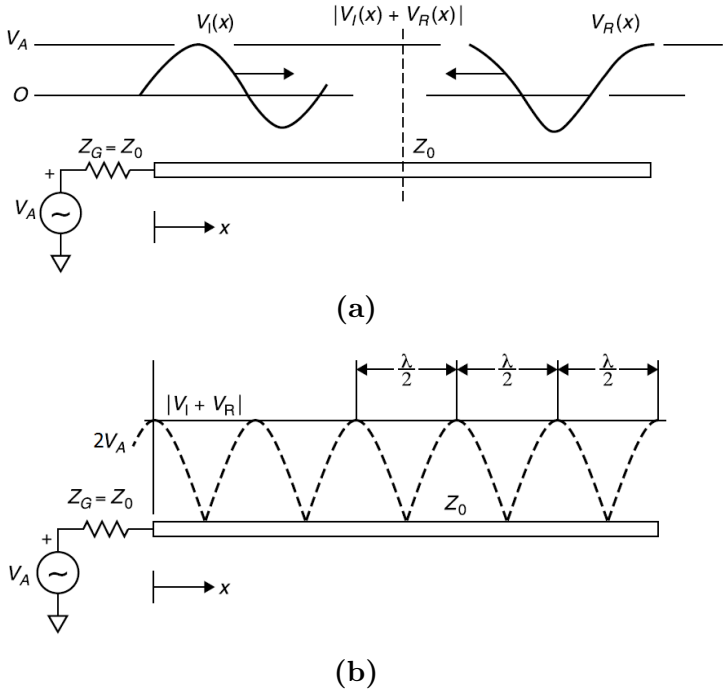



**Figure 3.2:** (a) illustrates an incident and a reflected wave on a lossless open circuited transmission line. (b) shows a standing wave on the same line [32].

### 3.1.3 Reflection Coefficients

To evaluate the reflection coefficient at the load, $z$ is set to 0 at the load and (3.3a) divided by (3.3b). This yields

$$Z_L = \frac{V(0)}{I(0)} = Z_0 \frac{V_{I0} + V_{R0}}{V_{I0} + V_{R0}} = Z_0 \frac{1 + \frac{V_{R0}}{V_{I0}}}{1 + \frac{V_{R0}}{V_{I0}}}. \tag{3.8}$$

The voltage reflection coefficient $\Gamma$ is defined as the amplitude of the reflected voltage wave normalized to the amplitude of the incident voltage wave, $\Gamma = V_{R0}/V_{I0}$. Rewriting (3.8) and solving for $\Gamma$ gives

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{3.9}$$

which substantiates that there are no reflections if a transmission line is terminated at its characteristic impedance, as stated in subsection 3.1.2.

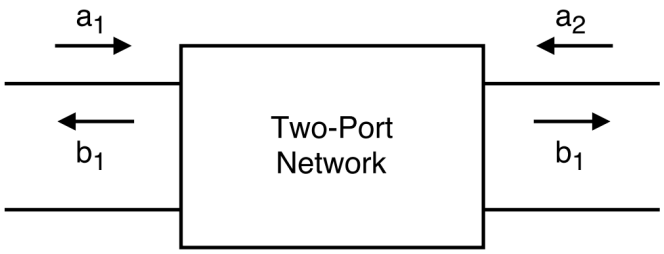



**Figure 3.3:** A two-port network.

## 3.2 Scattering Parameters

To simplify the analysis of a system, a macroscopic description like port parameters is often beneficial. These port parameters describes the behavior of the system at its input and output ports and neglects the details of the system core. At lower frequencies impedance or admittance parameters are often used. Impedance parameters express the relationship between voltages and currents at the ports, and the parameters are found by shorting and opening the circuits at the ports in question [18]. Due to lead inductance and capacitance, short and open circuits are hard to obtain at high frequencies. Scattering parameters (s-parameters) don't require circuits to be shortened or opened, and prevail over other parameters in high frequency electronics [2]. S-parameters are based on the fact that there will be no reflections in a line terminated in its characteristic impedance [18]. In addition, S-parameters defines the input and output variables as incident and reflected *voltage waves*. This is valuable because voltages and currents are difficult to define at high frequencies. Figure 3.3 shows a two-port network where

- $a_1$ is the wave incident on port 1, originating from the source.
- $b_1$ is the wave reflected from port 1, propagating towards the source.
- $a_2$ is the wave incident on port 2, originating from the load.
- $b_2$ is the wave reflected from port 2, propagating towards the load.

Quantifying the signal waves at the two-port network gives

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.10}$$

where

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad \text{is the input reflection coefficient.} \tag{3.11}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad \text{is the reverse transmission coefficient.} \tag{3.12}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad \text{is the forward transmission coefficient.} \tag{3.13}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad \text{is the output reflection coefficient.} \tag{3.14}$$

S-parameters can tell a lot about a two-port network, e.g. gain and stability. A designer should keep in mind that the macroscopic description might have discarded important information about the two-port, such as a sensitive parameter or process variation [18].

## 3.3 Smith Chart

The Smith chart is a handy tool widely used in RF circuit design and has been in use since Philip Smith developed it while working at Bell Telephone's Radio Research Lab in 1939.[1]. It is of use in many different applications, but mostly for impedance matching (described in section 4.5.4) in this thesis. Every book on basic RF theory have the details of the Smith chart explained to some extent, [18], [4] and [25], to mention a few. The next section will focus on what is necessary to know about a Smith chart in order to take advantage of it in RF circuit design.

### 3.3.1 Using the Smith Chart

A Smith chart makes plotting real numbers from zero to infinity and all imaginary numbers possible. In this thesis, it will be used solely for impedances and admittances. Consider an ordinary Cartesian coordinate system where the horizontal axis represent real numbers and the vertical axis the imaginary ones. The vertical axis is turned around zero so that the ends (infinity and negative infinity) meet and make the unity circle of the Smith chart as seen in Figure 3.4 (b). Then the lines of constant reactance are now arcs of circles of different radii highlighted in red. Any point along one of these lines will have the same reactance. The horizontal line where the reactance is zero is considered a part of a circle of infinite radius.

[1] A very similar chart was published by T. Mizuhashi in 1937 [30] Some call it the Mizuhashi-Smith chart, but in this thesis, the name Smith chart will be used, as in most literature.

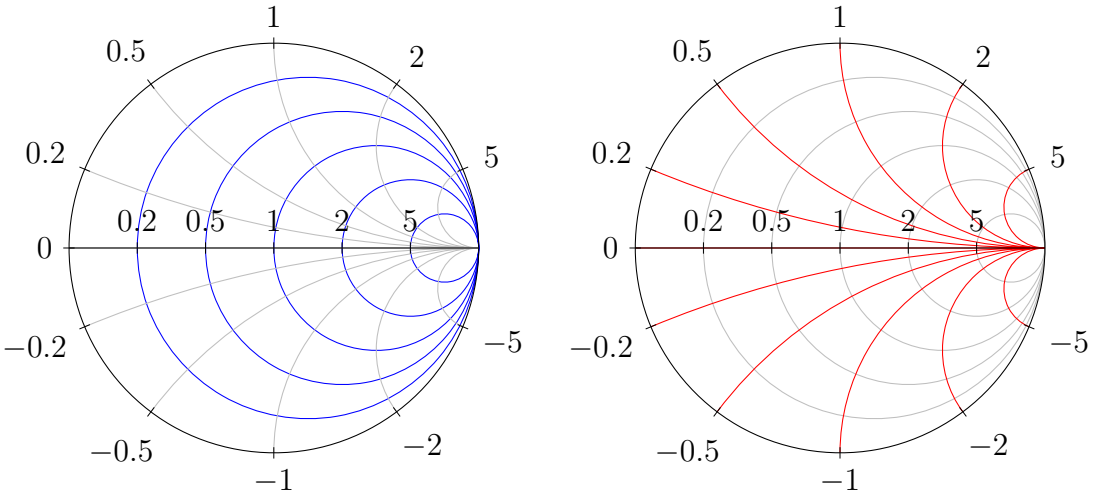



**Figure 3.4:** (a) shows the lines of constant resistance and (b) the lines of constant reactance, both mapped into a polar plot.

Highlighted in blue Figure 3.4 (a) are the circles of constant resistance, where the unity circle is zero ohms. As the radius decreases and the center of the circle moves to the right, the resistance increases. At the rightmost point of the Smith chart, an infinite resistance can be plotted.

As the center of the Smith chart is 1 Ω, large impedances must be normalized prior to plotting. The top half of the chart where the reactance is positive represent an inductance, and similarly, the bottom half represent a capacitance. Admittances, given by

$$Y = \frac{1}{Z} = \frac{1}{R + jX} = G + jB, \tag{3.15}$$

where $G$ is the conductance and $B$ is the susceptance, is easily plotted if the Smith chart is flipped as seen in Figure 3.5 (b). The impedance Smith chart is often combined with a admittance chart, resulting in a $YZ$ Smith chart.

Using the Smith chart is somewhat imprecise as the user often draws by hand and make subjective judgements doing so. However, the error introduced is usually negligible in practical situations [4].

## 3.4 Skin Effect

The skin effect is undesirable and appear in conductors at high frequencies. The phenomenon results in increased resistance due to the fact that current tend to flow primarily on the surface (hence *skin* effect) of the conductor. This means

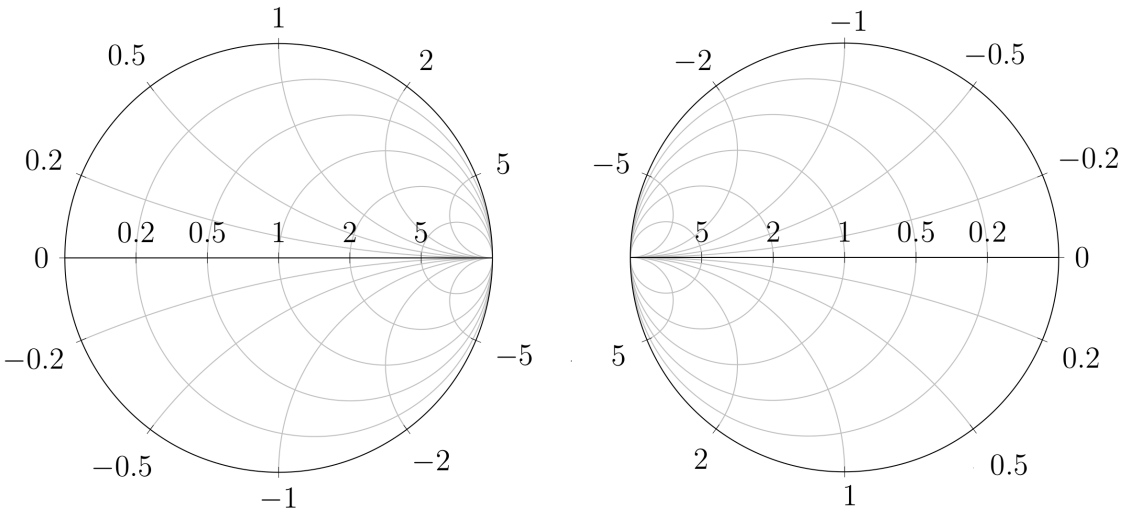



**Figure 3.5:** (a) is an ordinary Smith chart which presents an impedance plane, but it is easily converted to an admittance plane by flipping it as in (b). They are often combined to a YZ chart.

the effective area of the conductor has decreased, which consequently increases the resistance.

Assuming the return current is far enough away to be neglected, when the current $I$ in Figure 3.6a varies with time, the magnetic field $H$ also varies with time. Faraday's law then says that the magnetic field induces a voltage on the conductor. The induced voltage produces a current around the rectangle illustrated in the same figure according to Ohm's law. Kirchhoff's voltage law for the rectangle obtains

$$J_B \rho l - J_A \rho l + \frac{d\phi}{dt} = 0, \tag{3.16}$$

where $J$ is the current density, $\rho$ is the resistivity, $l$ is the length of the rectangle and $\phi$ is the flux perpendicular to the rectangle. As the arrows in Figure 3.6 (a) imply, Equation (3.16) states that the current subtracted from the center adds to the surface [18]. Increased depth, frequency and magnetic field and decreased resistivity all exacerbates the skin effect.

In integrated circuits the interconnections usually have a rectangular form (except in bond wires), the current density of which are given by

$$J_s = J_{s0} \exp\left(-\frac{z}{\delta}\right) \exp\left(-\frac{jz}{\delta}\right), \tag{3.17}$$

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{2}{\omega\mu\sigma}}, \tag{3.18}$$

where $z$ is the distance from the center to the surface of the conductor, $\delta$ is the *skin depth*, $\omega$ is the frequency in $rads/s$, $\mu$ is the permeability (equal to the free-space value in nearly all integrated circuits [18]) and $\sigma$ is the conductivity. The subscription $s$ is chosen arbitrarily and denote the magnitude of these skin effect variables, and subscription 0 denote the surface value. The skin depth is the distance from the conductor surface where the current density has dropped by a factor of $e$ (63% of the current in a wire flows between the surface and the skin depth). Equation (3.17) describes an exponentially decreasing current density compared to its surface value. This means that a conductor much thicker than the skin depth will experience a negligible decrease in resistance, because the current carried by the added material is very small.

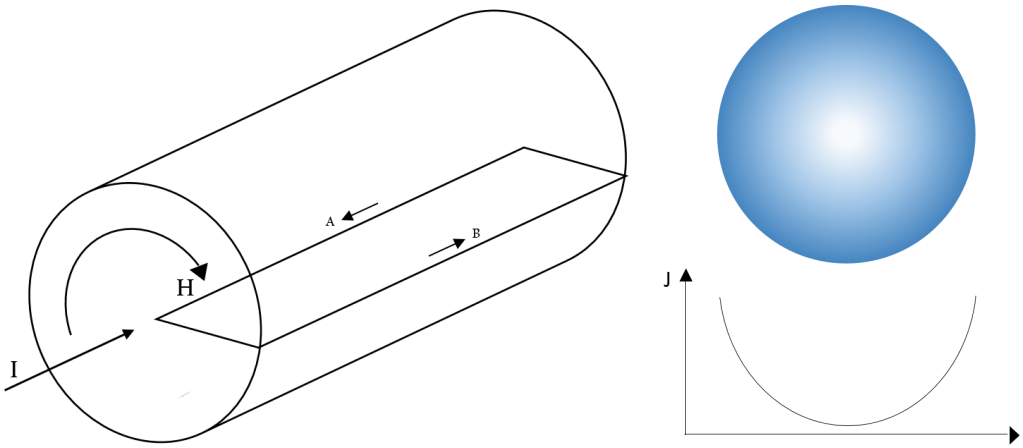



**Figure 3.6:** (a) illustrates a cylindrical conductor [18], and (b) depicts the current distribution of a cross section of the same conductor.

CHAPTER 4

# Amplifier Design

This chapter introduces some considerations and procedures that follow integrated RF amplifier design. Many of the theories and methods discussed here rely on S-parameters and Smith charts as explained in the previous chapter. The focus will be on power amplifiers, but many of the following topics are applicable to amplifiers in general.

## 4.1 Classification

Amplifiers are categorized by different classes. Class A, AB, B and C are *conventional* amplifiers, distinguished by their current conduction angle ($\alpha$) as summarized by Table 4.1. The current conduction angle is set by the bias voltage and therefore the transistor's operating region. Then there are the *switching* amplifiers (e.g. class D, E, F) which use the transistor as a switch. Switching amplifiers differ in the way they are tuned in terms of harmonics and signal shaping. The switching frequencies must be much higher than operating frequencies. This makes switch mode amplifiers inconvenient at very high frequencies, because the transistors are unable to switch fast enough.

The bias voltage for class A is usually the one that yields a quiescent current is in the middle of its minimum and maximum. This is the most linear amplifier class with its full conduction angle as shown in Figure 4.1. As the current conduction angle decreases, so does the linearity. Class B is biased at the turn-on voltage, where the transistor is on the threshold of current conduction. A class AB amplifier is, as the name implies, biased somewhere between class A and B. This introduces a trade-off between linearity and efficiency, where the bias is set closer to class A

**Table 4.1:** The conventional amplifier modes. $\eta_{\max}$ is the maximum theoretical efficiency.

| **Class** | $\alpha$[radians] | $\eta_{\max}$[%] |
|---|---|---|
| **A** | $2\pi$ | 50 |
| **AB** | $\pi - 2\pi$ | <78.5 |
| **B** | $\pi$ | 78.5 |
| **C** | $0 - \pi$ | <100 |

for linearity or towards class B bias for efficiency. Class C is biased beneath the turn-on voltage. With a sinusoidal input signal, collector current of the amplifiers with reduced conduction angle will be a partially rectified sinusoid, as illustrated in Figure 4.1. The output signal must then contain harmonics. Harmonics arise from non-linear effects due to the reduced conduction angle. They are currents at multiples of the fundamental frequency $f_0$, i.e. the second harmonic frequency is $2f_0$, the third is $3f_0$, and so on. In Figure 4.2, it is obvious that the bias current (DC) decreases and the harmonics increases as $\alpha$ decreases. To maintain the original signal waveform, the harmonics must be filtered out, leaving only the sinusoid at the fundamental frequency. The efficiency as used in Table 4.1 is defined as the ratio of RF output power to DC input power:

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}}. \tag{4.1}$$

Since the gain in power amplifiers usually is relatively low, the input power should be accounted for when calculating the efficiency. A common measure is Power Added Efficiency (PAE), given by

$$PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} = \left(1 - \frac{1}{G}\right)\eta. \tag{4.2}$$

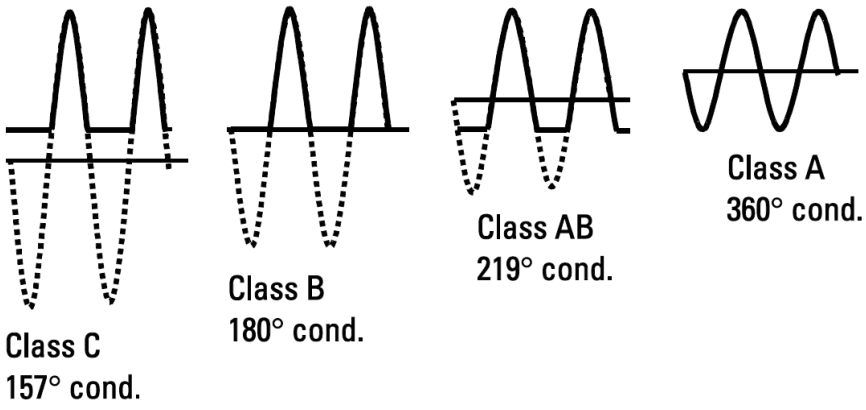



**Figure 4.1:** The collector current plotted for the four amplifier classes. The conduction angle of class AB and C are chosen arbitrarily [26].

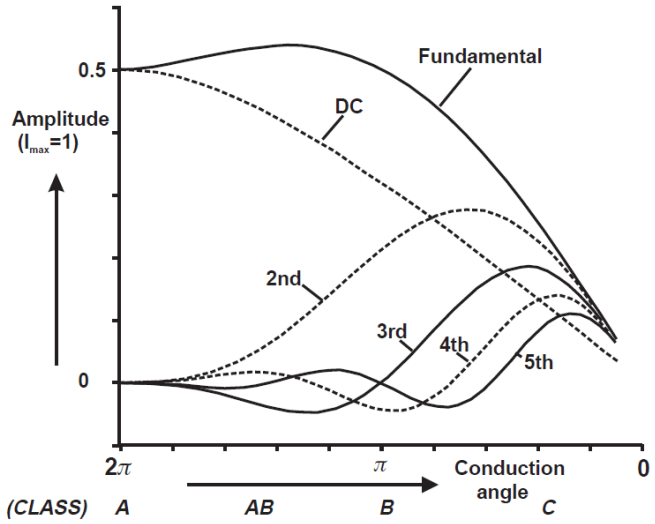



**Figure 4.2:** The amplitude of the current waveforms for different conduction angles [9].

## 4.2 Amplifier Gain

There are mainly three different two-port gains defined as follows:

$$G = \text{ Power gain } = \frac{P_L}{P_{\text{in}}} = \frac{\text{Power dissipated in the load}}{\text{Power delivered to the input}}$$

$$G_T = \text{ Transducer gain } = \frac{P_L}{P_{\text{avs}}} = \frac{\text{Power dissipated in the load}}{\text{Power available from the source}}$$

$$G_A = \text{ Available gain } = \frac{P_{\text{avn}}}{P_{\text{avs}}} = \frac{\text{Power available from the two-port network}}{\text{Power available from the source}}$$

The gain definitions differ primarily in how well the source and load are matched to the two-port network. In case of maximum power transfer at both the input and output, the gain is maximized and $G = G_A = G_T$ [25]. By matching only the input, available gain predicts the gain of the device when the output is matched as well.

## 4.3 Linearity

Transistors are very nonlinear devices. The *dynamic range*, over which the device operates as desired, is often defined by noise at very low power levels and compression or even destruction at high levels of power [24]. Two nonlinear effects will

be considered here, *gain compression* and the *third-order intercept point*. A Taylor series can be used to create a general model of the nonlinear behavior of a network with an input voltage $v_i$ and an output voltage $v_o$:

$$v_0 = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + ..., \tag{4.3}$$

where the coefficients $a_n$ can be found empirically. Considering only the terms through the third order, the voltage gain can be found to be:

$$G_v = \frac{v_0}{v_i} = a_1 + \frac{3}{4} a_3 V_0^2, \tag{4.4}$$

where $V_0$ is the amplitude of the input signal. The coefficient $a_3$ is usually negative, and reduces gain when $V_0$ is high. This is termed gain compression, and when the gain has dropped 1 dB compared to its ideal response it is called the 1 dB Compression Point ($P_{1dB}$), as shown in Figure 4.3. For power amplifiers, the output referred $P_{1dB}$ is of interest (in contrast to LNAs, where if is referred to the input). Compression happen when the output signal puts the transistor in saturation (triode or linear region for a FET).

Frequency components are generated in nonlinear amplifiers. If the input consists of a single frequency $\omega_0$, harmonics will be generated. The harmonic frequencies are given by $n\omega_0$ for $n = 0,\ 1,\ 2, ...$, which usually can be filtered out. If intermodulation products are generated inside the passband of the amplifier, these can not be filtered. This is the case if the input signal consists of two closely spaced frequency components $\omega_1$ and $\omega_2$. Analysis of the output when a two-tone input signal is applied, show that the output spectrum consists of:

$$m\omega_1 + n\omega_2, \tag{4.5}$$

where $w,\ n = 0,\ \pm 1,\ \pm 2, ....$ The order of these intermodulation products are given by $|m| + |n|$ [24]. It can be shown that two of the third-order intermodulation products ($2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$) will be placed in the passband of the amplifier if $\omega_1$ and $\omega_2$ are close in frequency. The output power of the third-order intermodulaton products increase as the cube of the input power. Figure 4.3 show the Third-Order Intercept Point (IP3), where the linear and the cubic response would intersect if compression is ignored. A high IP3 is desirable, but it will be degraded by cascading amplifiers.

## 4.4 Stability

The stability of the amplifier is important to make sure oscillations does not occur. In Figure 4.4 the circuit is prone to oscillation if either $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$, which happen if the real part of the input or output impedance is negative [25]. Source and load matching networks are thus essential to the stability because $|\Gamma_{in}|$ and $|\Gamma_{out}|$ depend on them. [25] defines two types of stability:

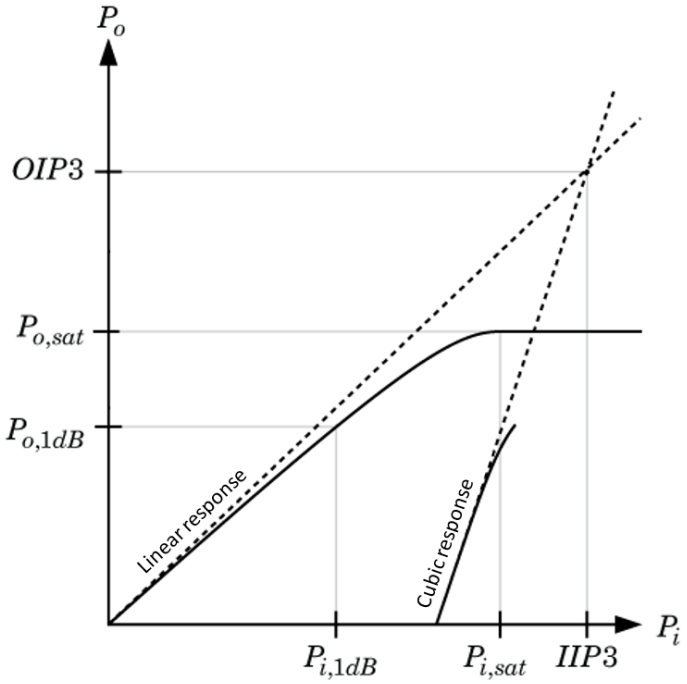



**Figure 4.3:** Gain compression and third order intercept point for a nonlinear device [19].

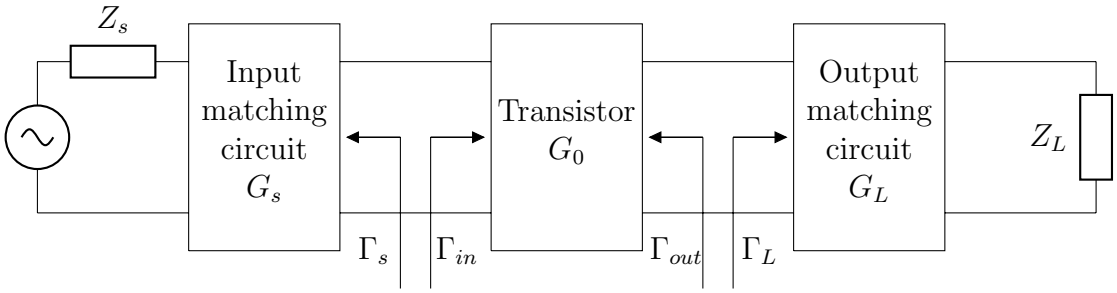



**Figure 4.4:** A general amplifier circuit [25].

- *Unconditional stability*: The network is unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances.
- *Conditional stability*: The network is conditionally stable if $|\Gamma_{in}| < 1$ or $|\Gamma_{out}| < 1$ for a certain range of passive source and load impedances. This case is also referred to as potentially unstable.

### 4.4.1 Tests for Stability

There are numerous ways to reveal the stability condition for a device. The following two tests for stability are adequate for a linear amplifier circuit. The $K - \Delta$ test

may prove the amplifier to be unconditionally stable if *Rollet's condition* is satisfied:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}} > 1, \tag{4.6}$$

and an additional criterion is satisfied simultaneously:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1, \tag{4.7}$$

or

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0. \tag{4.8}$$

(4.8) is added because $B1$ is usually a parameter ready to simulate with Computer-Aided Design (CAD) tools where the $\Delta$ might not be.

An alternative test to the previous is the *geometric stability factor*, in which only one condition needs to be met for unconditional stability: $\mu > 1$. The geometric stability factor calculates the distance from the center of the Smith chart to the nearest unstable point in the load plane [3]. With increasing value of $\mu$ the stability of the amplifier also increases, as opposed to the $K - \Delta$ test, in which the degree of stability is not apparent [25].

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|}. \tag{4.9}$$

Both the $K - \Delta$ test and the geometric stability factor are individually sufficient for testing stability condition. As stability is frequency dependent, testing for multiple frequencies close to the design frequency is advised. Do note that for multistage amplifiers, these tests may not detect oscillations between stages, see subsection 4.4.3.

### 4.4.2 Stability Circles

If the device in question proves not to be unconditionally stable, additional stability analysis is required. *Stability circles* are used to determine stable values for $\Gamma_s$ and $\Gamma_L$. The reflection coefficients seen when looking towards the source and load, $\Gamma_s$ and $\Gamma_L$ respectively, is given by

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{4.10a}$$

and

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{4.10b}$$

Applying the requirements for unconditional stability to (4.10) results in

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{4.11a}$$

and

$$|\Gamma_{out}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{22}\Gamma_s} \right| < 1, \tag{4.11b}$$

where the inequalities establish a set of values for $\Gamma_s$ and $\Gamma_L$ that make the amplifier stable. Input and output stability circles can be drawn on a Smith chart, as seen in Figure 4.5. They define the boundaries (where $\Gamma_s$ and $\Gamma_L$ make $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$) of a stable region and an unstable region for $\Gamma_s$ and $\Gamma_L$. The equations[1] for the center point C (a complex number) and radius R (a real number) of the source stability circle is

$$C_s = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2}, \tag{4.12a}$$

$$R_s = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|, \tag{4.12b}$$

and for the load stability circles:

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2}, \tag{4.13a}$$

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|. \tag{4.13b}$$

The determinant of the S-parameters is given by

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{4.14}$$

When $|S_{22}| < 1$ then $|\Gamma_s| < 1$ outside the source stability circle. Then, the device is unstable if $|\Gamma_s|$ is inside the stability circle or outside the Smith chart. If $|S_{22}| > 1$, the stable region for $|\Gamma_s|$ would be inside the region enclosed by both the stability circle and the Smith chart. Similarly, the stable area would be outside the load stability circle for $\Gamma_L$ when $|S_{11}| < 1$. $\Gamma_L$ must be inside both the stability circle and the Smith chart for the device to be stable when $|S_{11}| > 1$.

If $|S_{11}| > 1$ or $|S_{22}| > 1$, the amplifier cannot be unconditionally stable. In this case, $\Gamma_s$ and $\Gamma_L$ must be chosen within stable regions. In case of an unconditionally stable amplifier, the stability circles appear completely outside the Smith chart.

### 4.4.3 Interstage Stability

To ensure stability in a multi-stage microwave amplifier design, a generally accepted method is to test the stages individually. If any of them are conditionally stable, they must be proved that they will still be stable as such (e.g. with stability circles) [31]. Cascading stable amplifiers and stating they are still stable is a questionable

[1] Consult [25] for the complete derivation.

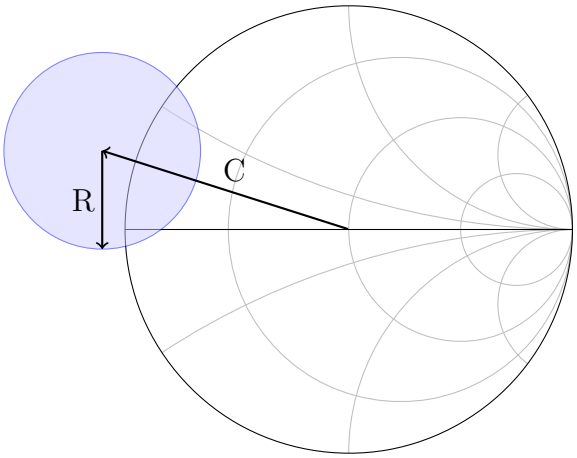



**Figure 4.5:** A Smith chart with a stability circle.

procedure, as several approximations and assumptions are made. To mention one, the $K - \Delta$ test require the source and load reflection coefficients to be less than 1. In a multi-stage design, reflection coefficients can exceed 1 frequently [31].

A more thorough test which operates directly in the circuit-simulator environment is presented in [31]. This approach apply the Nyquist stability criteria to the open loop frequency domain response given by

$$G = -\Gamma_1\Gamma_2, \tag{4.15}$$

where $\Gamma_1$ and $\Gamma_2$ are the reflection coefficients seen in each direction at the input or output of a transistor. The Nyquist criteria states that if $G$ encircles the $-1 + j0$ point in the clockwise direction when plotted as a function of frequency, the closed loop system will be unstable [3].

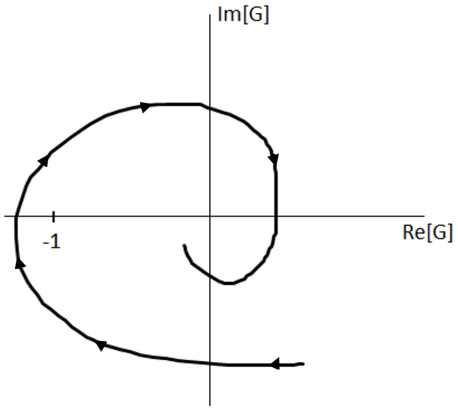



**Figure 4.6:** A plot of an open loop frequency domain response. According to the Nyquist criteria, this would indicate instability.

## 4.5 Impedance Matching

Radio frequency signals are often very weak, and any loss of signal must be avoided anywhere possible. In order to deliver the maximum possible power from a source to a load in a DC circuit, the maximum power transfer theorem states that the source resistance should be equal to the load resistance. With AC circuits, the same theorem states that the source impedance should be equal to the complex conjugate of the load impedance, the proof of which follows in the next section.

### 4.5.1 Conjugate Matcing

Consider the circuit of Figure 4.7 (a), if the impedances are purely resistive, i.e. $Z_s = R_s$ and $Z_L = R_L$, the power delivered to the load is given by

$$P_L = I^2 R_L = \frac{V^2 R_L}{(R_s + R_L)^2} = \frac{V^2}{\frac{R_s}{R_L} + 2R_s + R_L}, \tag{4.16}$$

which is plotted in Figure 4.7 (b). The value for $R_L$ which results in maximum $P_L$ is found by differentiating with respect to $R_L$ and setting it equal to zero:

$$\begin{aligned} \frac{\partial}{\partial R_L}\left(\frac{V^2}{\frac{R_s}{R_L} + 2R_s + R_L}\right) = 0 \\ R_s = \pm R_L, \end{aligned} \tag{4.17}$$

where only the positive soulution is viable. When the impedances have an imaginary part, i.e. $Z_s = R_s + X_s$ and $Z_L = R_L + X_L$, the average power delivered to the load is given by

$$P_L = \frac{1}{2}\left(\frac{|V_s|}{|Z_s + Z_L|}\right)^2 R_L = \frac{1}{2}\frac{|V_s|^2 R_L}{(R_s + R_L)^2 + (X_s + X_L)^2} \tag{4.18}$$

Because reactances can be negative, it is apparent from (4.18) that if they cancel each other out, i.e. $X_s = -X_L$, their contribution to power loss is minimized. What is left of the expression then is the same as for the purely resistive circuit in (4.16). In conclusion, the maximum power transfer from a source with a source impedance to a load impedance, is achieved when the load impedance is the complex conjugate of the source impedance, i.e. $Z_s = Z_L^*$. Conjugate matching eliminate reflections and, logically, RF designers strive to achieve this in general.

### 4.5.2 Loadline Matching

The maximum power transfer theorem explained in the previous section does not accommodate for real-world device constraints. Considering the output of a transistor as a current generator, there are physical limits to the current it can supply

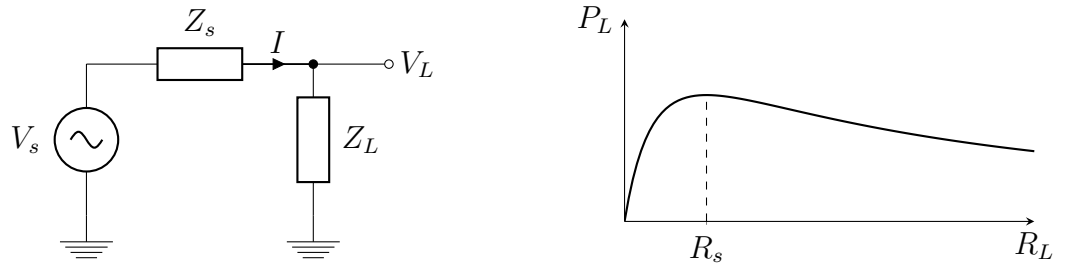



**Figure 4.7:** (b) shows the power delivered to the load with respect to the load impedance $Z_L$ in (a) if the impedances are purely resistive.

and the sustainable voltage at its terminals, as illustrated in Figure 4.8. *Loadline matching* makes sure the output power of the device is maximized, while accounting for the greatest permissible current and voltage swing at the transistor output [9].

Loadline match is also known as *power match*, which is not to be confused with maximum power transfer obtained with a conjugate match. Power matching means presenting the transistor output to a load resistance optimal for output power. This resistance, $R_{opt}$, is given by

$$\frac{R_g R_{opt}}{R_g + R_{opt}} = \frac{V_{max}}{I_{max}} \tag{4.19}$$

and if $R_g \gg R_{opt}$ is assumed, then

$$R_{opt} = \frac{V_{max}}{I_{max}}. \tag{4.20}$$

Using the optimal resistance in a PA will result in the more desirable loadline shown in Figure 4.8 (b). There is some controversy related to this method, in which

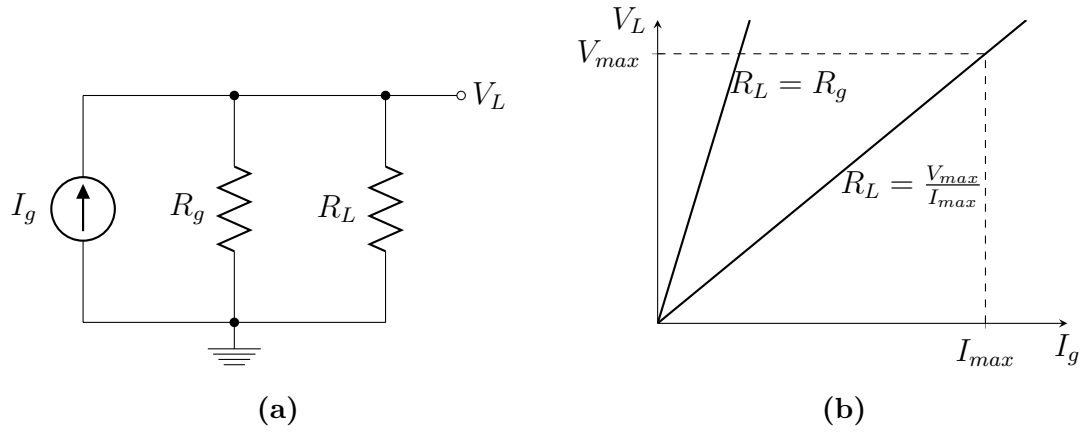



**Figure 4.8:** (b) shows a plausible difference in conjugate matching and loadline matching in the circuit of (a).

some claim the loadline match will result in problematic reflections [9]. It is likely that the input termination of the subsequent stage will deviate from its specified condition. However, this depends on what impedance the PA presents at its output, which to some extent remain constant in linear operation. In addition, reflections only appear if the connections between the stages are long enough to be considered as transmission lines.

In addition, loadline matching might also increase the linear region of a device as shown in Figure 4.9. It is also apparent in Figure 4.9 that the loadline match reduces the power gain compared to conjugate matching, as would be expected when conjugate matching yields the best power transfer.

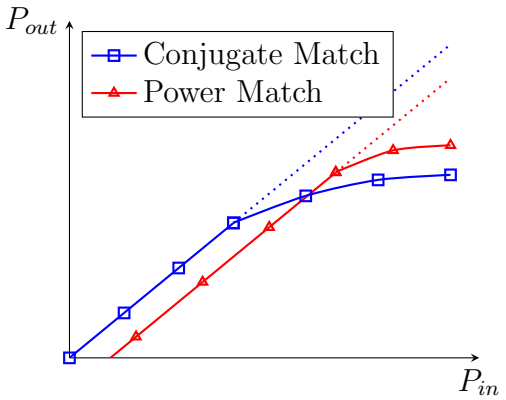



**Figure 4.9:** Output power of an amplifier matched for maximum gain and maximum output power.

### 4.5.3 Load Pull

To find a relationship between the output power and output impedance, as Figure 4.9 indicates there is, *load pull* simulations or measurements can be performed. Load pull collects data on a setup comprising a device under test with a calibrating tuner on its input and output [9]. The input is preferably fixed close to a conjugate match for maximum power gain and then the load impedance is tuned while collecting data points. A typical result is shown in Figure 4.10. Source pull can also be performed, but it prove less effective for increasing the maximum output power than load pull.

### 4.5.4 Impedance Transformation with Lumped Elements

The Smith chart is a visual and quick method for a designer to do approximate calculations on matching networks which later can be optimized with CAD tools.

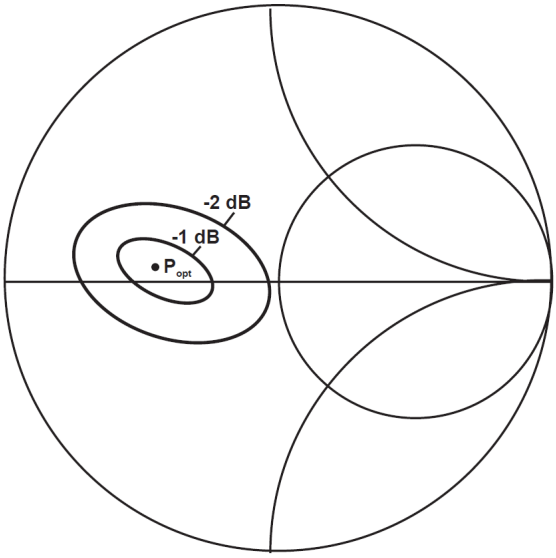



**Figure 4.10:** The load pull contours indicating the optimal output impedance on a Smith chart. The contours track the reduction in output power as the load impedance deviate from the optimal value.[9]

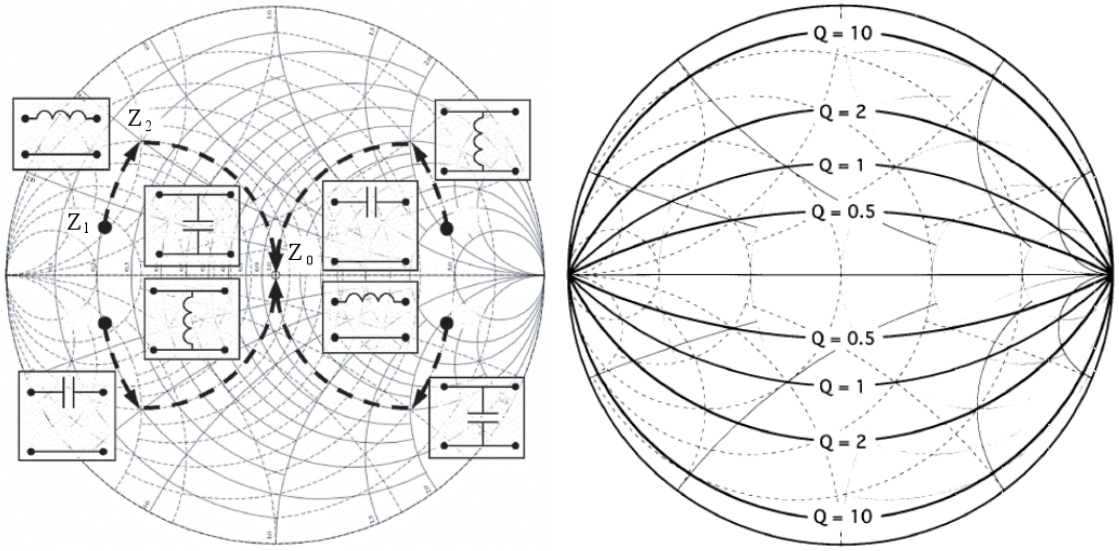
Any given impedance (or admittance) can be manipulated by *moving* along lines of constant resistance and conductance with inductors and capacitors. Series elements move along a circle of constant resistance, i.e. they can not change the resistance, only the reactance. When using a series inductor, the impedance moves clockwise along a circle of constant resistance, as illustrated in Figure 4.11 (a) where $Z_1$ is moved to $Z_2$. A series capacitor will move in the opposite direction of a series inductor, i.e. counter-clockwise. The distance moved is quantified as the change in reactance. The inductance or capacitance of the series element necessary to move the desired distance is given by

$$L = \frac{\omega X}{N}, \tag{4.21}$$

$$C = \frac{1}{\omega X N}, \tag{4.22}$$

respectively, where $N$ is the number to which the Smith chart is normalized (often the characteristic impedance $Z_0$).

The shunt elements operate in the admittance plane, which means they move the impedance along lines of constant conductance instead of resistance. The admittance plane of the Smith chart is flipped compared to the impedance plane, and thus shunt inductors will move the impedance in a counter-clockwise direction. Shunt capacitors counteract the movement of shunt inductors, as illustrated by Figure 4.11 (a), where the shunt capacitor moves the impedance from $Z_2$ to $Z_0$. With a series inductor and a shunt capacitor as shown in Figure 4.12, $Z_1$ has now been matched to $Z_0$. For shunt elements, the susceptance $B$ quantifies the distance moved. Using the relation between impedance and admittance in (3.15) on (4.21) and (4.22), the




**(a)** **(b)**

**Figure 4.11:** (a) shows how inductors and capacitors transform impedances in the Smith chart [17]. A Smith chart with lines of constant Q is displayed in (b) [27].

inductance or capacitance of the shunt element necessary for a given movement can be calculated with

$$L = \frac{N}{\omega B}, \tag{4.23}$$

$$C = \frac{B}{\omega N}, \tag{4.24}$$

respectively. Impedance matching is frequency dependent, and the quality factor (*Q factor* or $Q$) of the matching network described the bandwidth relative to the center frequency of the match. The Q factor is defined as the ratio of reactance to resistance. A few lines of constant Q is illustrated in Figure 4.11 (b), Q=0 is along the line of zero reactance, and infinite Q factor is located along the perimeter of the Smith chart. When tuning a matching network, the Q factor can be increased but not decreased. To keep the lowest possible Q, more matching elements are used.

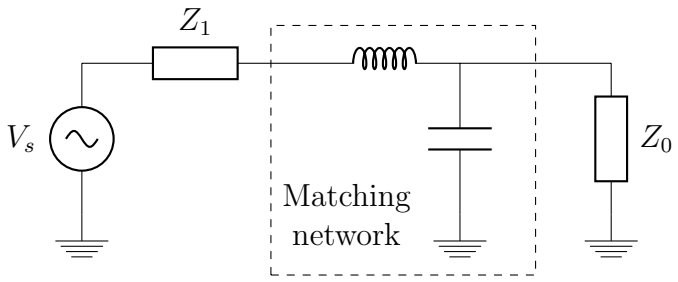



**Figure 4.12:** The matching network for transforming $Z_1$ to $Z_0$.

### 4.5.5 Impedance Transformation with Transmission Lines

In MMIC design, it may be a challenge to achieve inductor values fitting for the design. Inductors tend to be too large, and a solution might be to use transmission lines. At high frequencies they have the potential to fit on the chip, especially if the dielectric plays along to reduce their physical length according to (3.7). Transmission lines are highly capable of transforming impedances, for which they are frequently used. To transform a load impedance $Z_L$ to the desired input impedance $Z_{IN}$ (see Figure 4.13) with a lossless transmission line, the following equation is used:

$$Z_{IN} = Z_0 \left[ \frac{Z_L + jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta} \right], \tag{4.25}$$

where $\theta$ is the *electrical length*, which is a measure of the transmission line length in degrees given by

$$\theta = \frac{l}{\lambda} 360^\circ, \tag{4.26}$$

where $l$ is the length in meters. Losses accounted for, the input impedance will be

$$Z'_{IN} = Z_0 \left[ \frac{Z_L + Z_0 \tanh\gamma l}{Z_0 + Z_L \tanh\gamma l} \right], \tag{4.27}$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}. \tag{4.28}$$

Using these complex expressions is comprehensive, so the lossless one is further analyzed here. A simulator is commonly used for more accurate calculations. Three special cases of transmission lines' behavior are worth mentioning:

- A lossless transmission line of zero length or a multiple of half a wavelength (0°, 180°, 360°, 540° ...) results in $\tan\theta = 0$, and will not transform the load impedance, i.e.
$$Z_{IN} = Z_L \tag{4.29}$$
- The input impedance of a lossless transmission line terminated in a short circuit is reduced to
$$Z_{IN} = jZ_0 \tan\theta, \tag{4.30}$$
which makes it inductive up to an electrical length of 90°, capacitive when $90^\circ < \theta < 180^\circ$, and then the behavior repeats itself every half wavelength [32].
- Terminated in an open circuit, a lossless transmission line behaves like a short circuited one with a phase shift of $\lambda/4$. Thus, it is capacitive up to an electrical length of 90°, inductive when $90^\circ < \theta < 180^\circ$, and then the behavior repeats itself every half wavelength [32]. The input impedance is
$$Z_{IN} = jZ_0 \frac{1}{\tan\theta}. \tag{4.31}$$

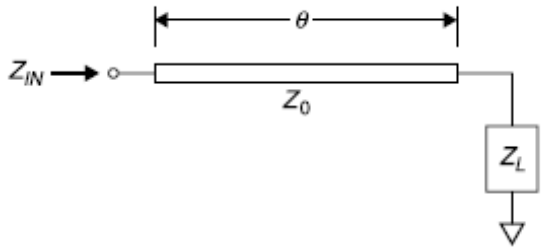



**Figure 4.13:** A terminated transmission line [32].

### Impedance matching with a single transmission line

Utilizing the Smith chart for impedance transformation with transmission lines is helpful, but the procedure is a little more comprehensive than that of lumped elements. Considering an ideal series line, on the Smith chart $Z_{IN}$ moves in a clockwise circular motion around the resistive part of $Z_0$ with a radius $r$, as illustrated in Figure 4.14. The electrical length of the line determines how far $Z_{IN}$ moves; at 180° it has moved an entire circle and is back where it started. With the following procedure, a single transmission line is sufficient for transforming a load impedance if it is located inside one of the two circles $R = 1$ or $G = 1$ where $G$ is the conductance [30].

1. Normalize the Smith chart to the desired input impedance.
2. Draw a line between $Z_L$ and $Z_{IN}$ (at the center), then draw the perpendicular bisector to locate $Z_0$ on the real axis. The radius $r$ is the distance from the center of the Smith chart to $Z_0$.
3. Renormalize the Smith chart to $Z_0$ and replot $Z_L$ ($Z'_L$ in Figure 4.14).
4. Read the angle needed to move $Z_L$ along the circle to the real axis. The angle corresponds to the electrical length necessary for the transmission line to transform the impedance as described.
5. Renormalize the Smith chart to the desired input impedance.

### Two-element transmission line impedance matching

A transmission line in parallel, called a *stub*, can be shorted or open circuited. Its contribution to impedance transformation is less complicated than that of the series lines. An open stub will only move the impedance clockwise along a circle of constant conductance as the length increases. If the electrical length of the open stub is 90°, the impedance is moved to $0 + j0\ \Omega$. At $\theta = 180°$, the impedance is back to where

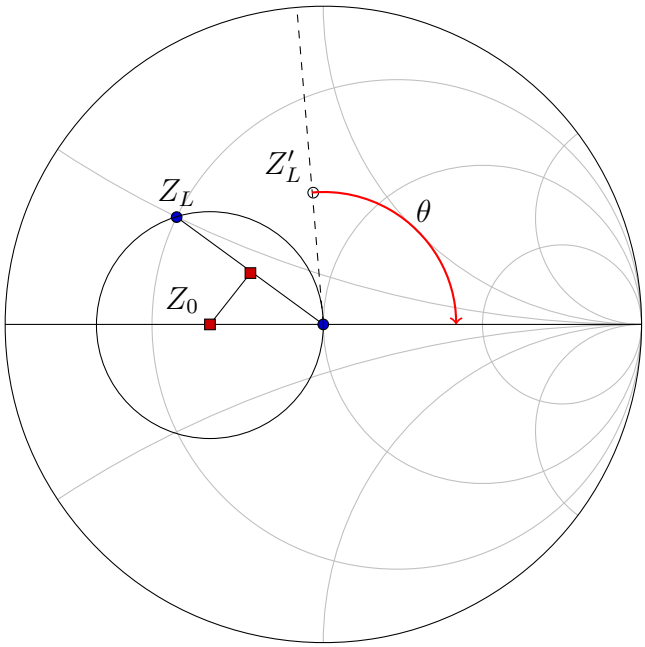



**Figure 4.14:** Transmission line impedance transformation.

it started; equal to the load impedance. This behavior will repeat itself for every 180° the line length increases.

The shorted stub is very similar to the open one, the only difference being that there will always be a 90° shift between the two at the same electrical length. At $\theta = 0°$, the impedance will naturally be zero, because the connection is directly to ground with no transmission line present. When $\theta = 90°$, the transformed impedance will be equal to the load impedance, at $\theta = 180°$ it has completed a full circle and so on.

A common method for transforming a load impedance with two distributed elements is with a stub and a series line. The procedure goes as follows:

1. The series line is connected closest to the load impedance, and has a characteristic impedance $Z_0$ equal to the desired input impedance $Z_{IN}$ to which the Smith chart is normalized to.

2. Now the impedance can be rotated around the center of the Smith chart to a point where the admittance $Y = 1 + jB$.

3. The stub should then be designed to transform the impedance to $Z_{IN}$ by canceling the susceptive part of the admittance.

**Lossy transmission lines**

The theory to transmission lines have so far omitted losses and real-world considerations to make it more perceivable. Circuit designers must keep in mind dielectric losses and variations in the effective wavelength in different dielectrics. The finite resistivity of the conductors will change their characteristic impedance as apparent in (3.4), making the line width a factor as well. Careful layout is essential to avoid influential parasitics. Designing transmission lines susceptible to undesirable effects is done with CAD tools for accurate results.

## 4.6 Amplifier Topologies

Considered in Table 4.2 are the three most popular topologies for Power Amplifier (PA) and Low Noise Amplifier (LNA) design [11]. Some additional deliberation is appropriate, especially for the RF domain. Perhaps most used is the Common Emitter (CE) configuration illustrated in Figure 4.15 (a). At high frequencies the feedback through $C_{\text{bc}}$ makes the reverse transmission $S_{12}$ significant. That results in an input impedance dependent on the output impedance and vice versa, as seen in (4.32). This makes tuning the input and output more complicated. The low reverse isolation also leaves the device more prone to instability.

$$\Gamma_{\text{in}} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.32}$$

The Common Base (CB) has much less feedback at high frequencies than the common emitter, which makes it more stable and easier to match to the desired source and load impedances. The noise in the common base is initially low, but increases rapidly with increasing frequency [11]. This topology has an input impedance of $\frac{1}{g_m}$ which might help tuning the input impedance.

The *cascode* is basically a combination of a common emitter and a common base sometimes called CE-CB. It is shown in Figure 4.15 (c) and with the common base at the output, feedback is minimal. The cascode has better gain than the other two topologies, but requires a higher supply voltage than that of common emitter and common base, thus also increasing power consumption. Due to the reduced Miller-effect, the cascode has better gain bandwidth. The cascode also provides a higher level of bandpass-filtering [18].

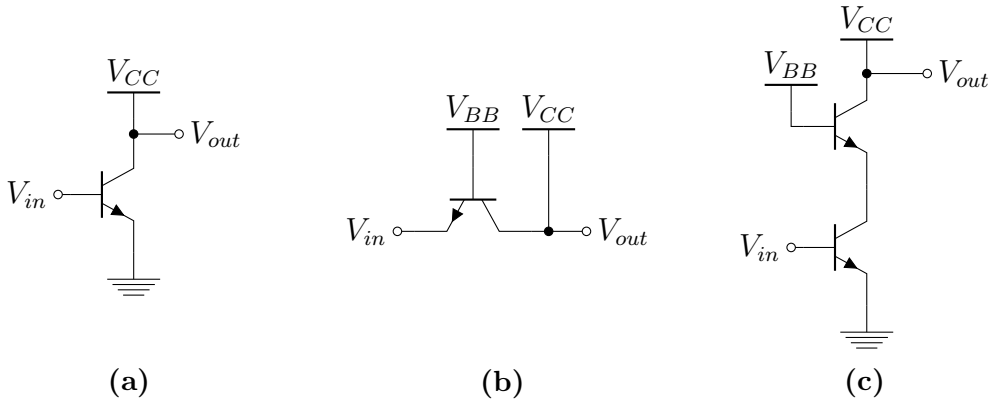



**Figure 4.15:** Three common circuit topologies: (a) is a common emitter, (b) is a common base and (c) is a cascode.

**Table 4.2:** Comparison of the most common amplifier topologies [11].

| **Characteristic** | **Common Emitter** | **Common Base** | **Cascode** |
|---|---|---|---|
| **Noise Figure** | Lowest | Increases with frequency | Low |
| **Gain** | Moderate | Lowest | Highest |
| **Linearity** | Moderate | High | Highest |
| **-3 dB frequency** | Low | Moderate | High |
| **Stability** | Moderate | High | High |
| **Reverse isolation** | Low | High | High |
| **PVT[1] sensitivity** | High | Low | Low |

[1]Process, voltage and temperature.

CHAPTER 5

# Schematic Design and Simulation

This chapter includes procedures and details about the actual design of the power amplifier. The design of each separate amplifier stage is explained. The bias network is demonstrated before presenting the design of the complete amplifier where all stages are put together.

## 5.1 Topology

The PA in this work comprises three stages of common emitters. The topology is chosen mostly due to the fact that it is the only one that achieved the full bandwidth of 9 GHz. Considering Table 4.2, the cascode topology seems to prevail both common base and common emitter, but the Q-factor of the output impedance is intrinsically too high to achieve the required bandwidth (compare Figure 5.1 with Figure 4.11 (b) for proof).[1] This is the case for the CB as well, leaving the CE as the best topology for this work.

## 5.2 Transistor Characterization

With the discussion on the transistors modeled by IHP in section 2.2, only a few additional characteristics are worth mentioning. Firstly, there is an option for two emitter lengths, 0.48 $\mu$m and 0.84 $\mu$m. A longer emitter increases the current

[1] This problem is also faced in [7], where it is implied that the high output impedance in small transistor sizes makes matching $S_{22}$ very difficult. The cascode topology is utilized in mm-wave applications (e.g. [20],[23],[28]), where the transistors are larger than in this work.

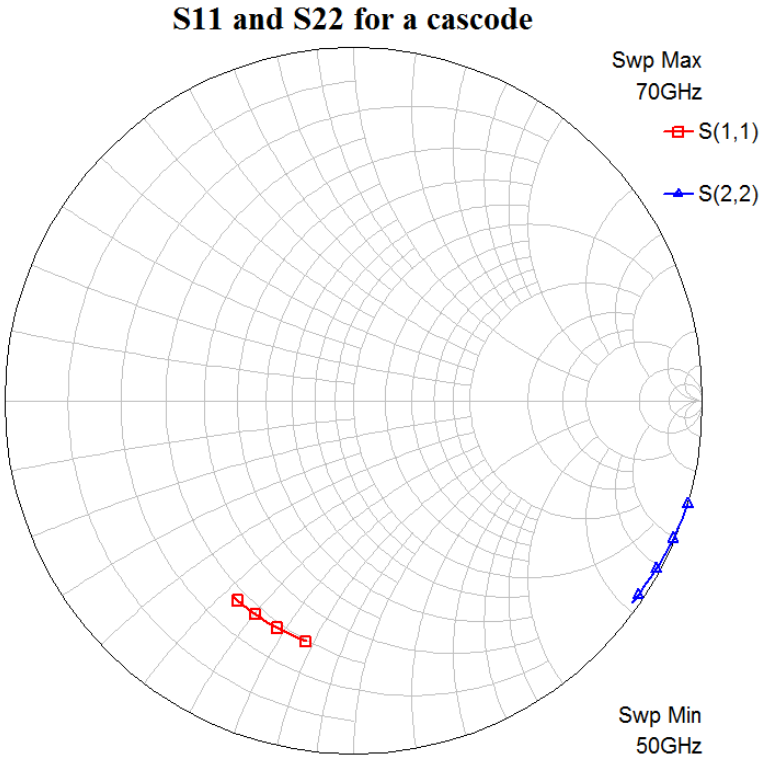
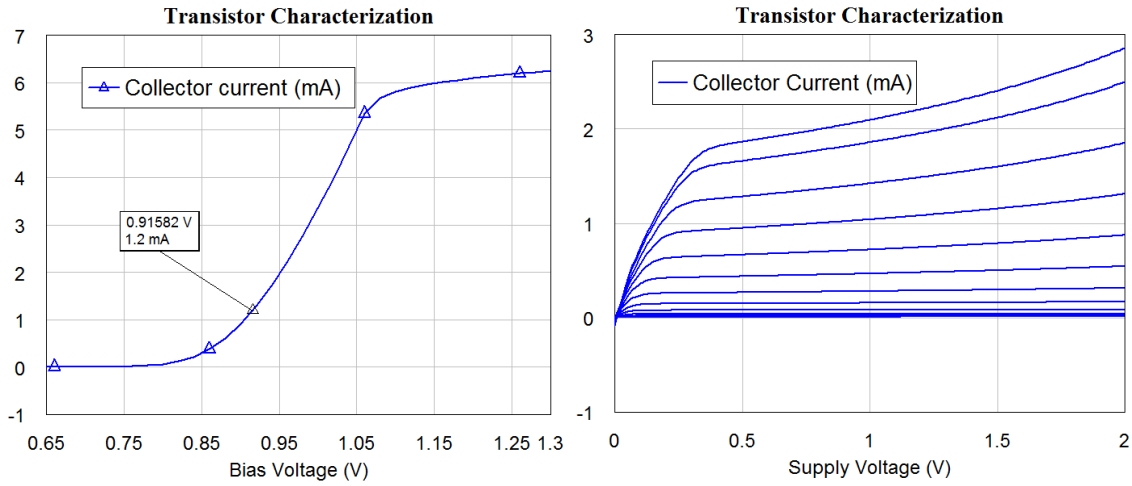



**Figure 5.1:** $S_{11}$ and $S_{22}$ of a cascode. The Q factor of the output impedance is very high. Test bench shown in Figure E.1.

capability of the transistor, which is good for high power applications. As the current capability with an emitter length of 0.48 $\mu$m is sufficient, it is the best choice because it has the lowest base resistance. There is also an option of multiple emitters in parallel, eight being the maximum. This is very similar to adding the same number of transistors in parallel; it multiplies the collector current. Where a large current is required, the number of emitters is maximized before putting transistors in parallel. That way, layout complexity is reduced and unwanted parasitcs and delays avoided.

In room temperature, the HBT starts conducting at about 0.8 V at the base terminal, and maximum transition frequency $f_{\text{T-max}}$ is obtained when $I_C = 1.2$ mA per emitter and with a supply voltage of 1.2 V. The bias voltage corresponding to $f_{\text{T-max}}$ is 0.92 V shown by the marker in Figure 5.2 (a). It should be noted that the models from foundry are only valid within a certain range of voltages, currents, temperatures, etc. As for the transistors, this range include most of the normal operating conditions.[2]

[2]The ranges for which IHP's models are valid are confidential and will not be disclosed.




(a) (b)

**Figure 5.2:** Transistor transfer (a) and IV characteristics (b). In (b) the collector current is plotted while sweeping $V_{CC}$ and stepping $V_{BB}$ (0.75 V to 0.96 V at 0.02 V increments)

## 5.3 Three Stage Design

Using only one topology, three cascaded stages of common emitters was found to be sufficient by simulations on the test bench in Figure E.3 (Appendix E). This provided the required power gain and output power while consuming little power. With only two stages, the amplifier would consume very much power to be able to provide enough power gain and the probability of instability would be higher. A multistage PA is usually designed in an opposite chronological fashion, meaning that for three stages, the third and last stage is designed first, then the second and then the first stage. To avoid confusion, the three stages are named *output stage*, *driver* and *pre-driver*, see Figure 5.3.

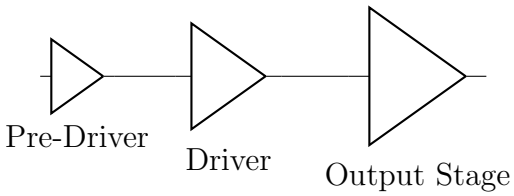



**Figure 5.3:** The three power amplifier stages sized according to power capability.

### 5.3.1 Output Stage

Power amplifiers are responsible for providing the antenna with a signal strong enough to be transmitted the full range specified for the wireless system. This PA has to deliver 5 dBm (3.16 mW) to the antenna with a gain compressed no more

than 1 dB. Obtaining good efficiency is very important, but will trade for linearity. On-Off Keying (OOK) does not stress high linearity, so class AB was chosen for good efficiency without losing too much gain compared to class A. The transistor current needed to deliver an arbitrary output power can easily be calculated for class A operation, but is complicated with a reduced conduction angle. As a starting point for biasing, some considerations about the transistor and input drive were taken. As the transistor IV characteristics in Figure 5.2 shows, the turn-on voltage is about 0.8 V, which is the bias point for class B operation. At about 0.92 V, the transistor achieves maximum $f_{\mathrm{T}}$ and this is a good bias for class A. A starting point for biasing was chosen at $V_{\mathrm{BB}} = 0.85\ V$ to ensure class AB operation. At this point, an increase in bias voltage would result in higher quiescent current and more gain, but efficiency would be reduced.

At a given bias voltage, the current per emitter is absolute, thus the quiescent current increases linearly with emitters in parallel. To size the output stage, compression point was simulated while increasing the number of parallel emitters. This empirical procedure relies on crude impedance matches at both input and output. When a good result was approached, optimization was performed by varying bias voltage and the number of emitters, and tuning the load impedance to the optimal for maximum output power. The latter is best done by load pull analysis, which in Microwave Office (MWO) is performed with a *load pull script* on the test bench in Figure E.4. The load pull simulation is shown in Figure 5.4.

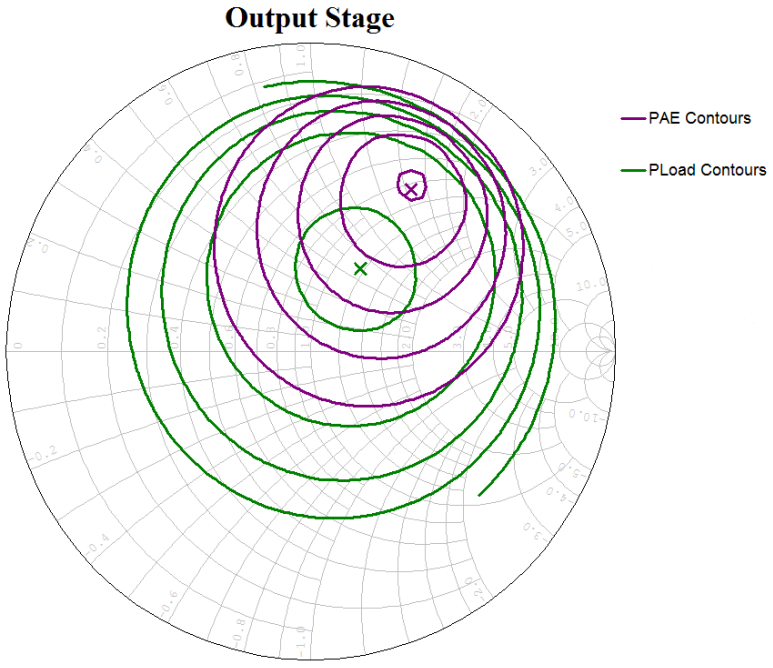



**Figure 5.4:** The load pull analysis showing contours for power delivered to the load and PAE, at the threshold of compression. The X indicates maximum, and the contour intervals are 1 dBm for Pload and 5% for PAE.

To ensure that the amplifier was unconditionally stable, an inductor at the emitter was used. This is emitter degeneration, trading gain for stability. To narrow down the possible combinations, lower limits of 5.5 dB gain and a $P_{1dB}$ of 6.5 dBm was set for good measure. The final design kept the initial bias voltage, and a total of 12 emitters are used, as shown in Figure 5.5. Table 5.1 summarizes its performance and simulation results follows in Figure 5.6, Figure 5.8 and Figure B.1. Figure 5.7 shows the port parameters and Noise Figure (NF), which is a measure of the degradation in signal-to-noise ratio, commonly used in radio systems. $S_{21}$ peaks at a frequency lower than the 57 GHz. This enables a signal outside the passband to put the amplifier in saturation earlier than a signal at 61 GHz with the same amplitude. Filtering is then very important. In Figure B.1 it is apparent by the loadline that the signal at 57 GHz is the first signal to cause gain compression as predicted.

**Table 5.1:** Key figures of the output stage.

| Performance metric | Value | Unit |
|---:|:---:|:---:|
| Bias voltage | 0.85 | V |
| Number of parallel emitters | 12 | - |
| Power gain | 6.0 | dB |
| Quiescent current | 3.5 | mA |
| Peak power added efficiency | 43 | % |
| Output referred $P_{1dB}$ | 8 | dBm |

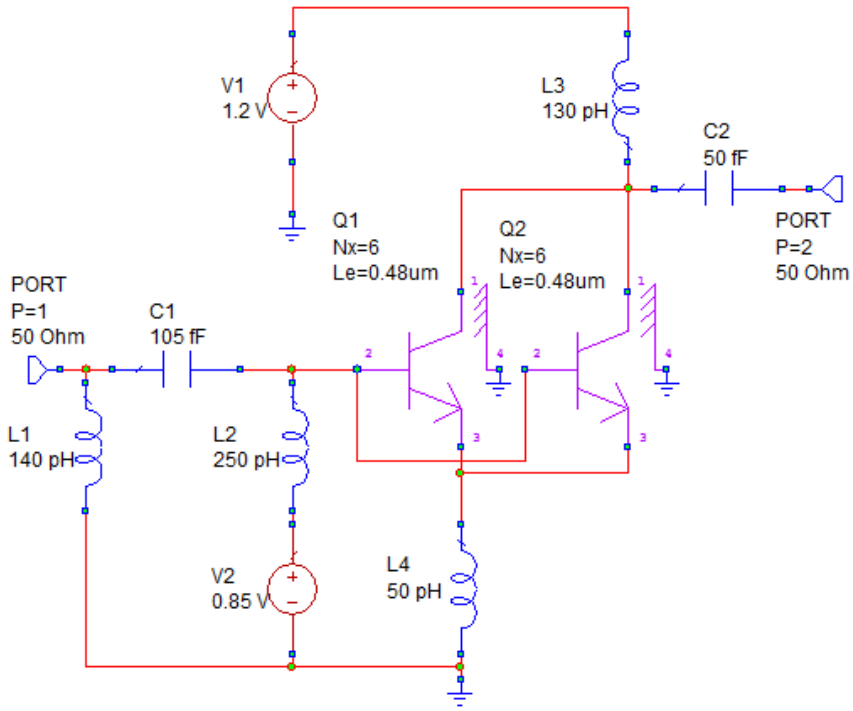



**Figure 5.5:** The circuit schematic of the stand-alone output stage.

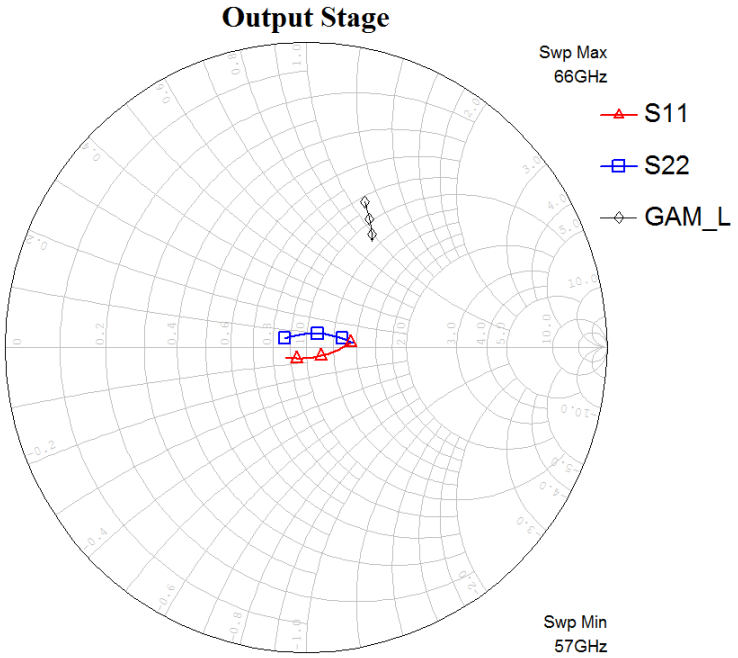
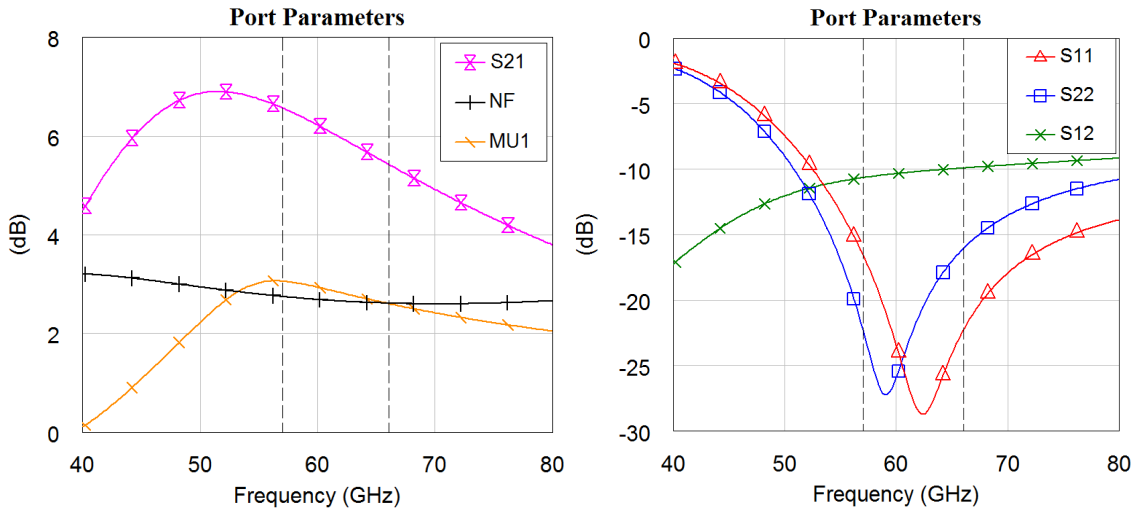



**Figure 5.6:** The Smith chart showing the roughly matched output stage. $\Gamma_L$, plotted as GAM_L, is tuned to the impedance optimal for output power as proven with load pull analysis in Figure 5.4.




**(a)** **(b)**

**Figure 5.7:** The port parameters of the output stage. The dashed vertical lines indicates the bandwidth of the 60 GHz band.

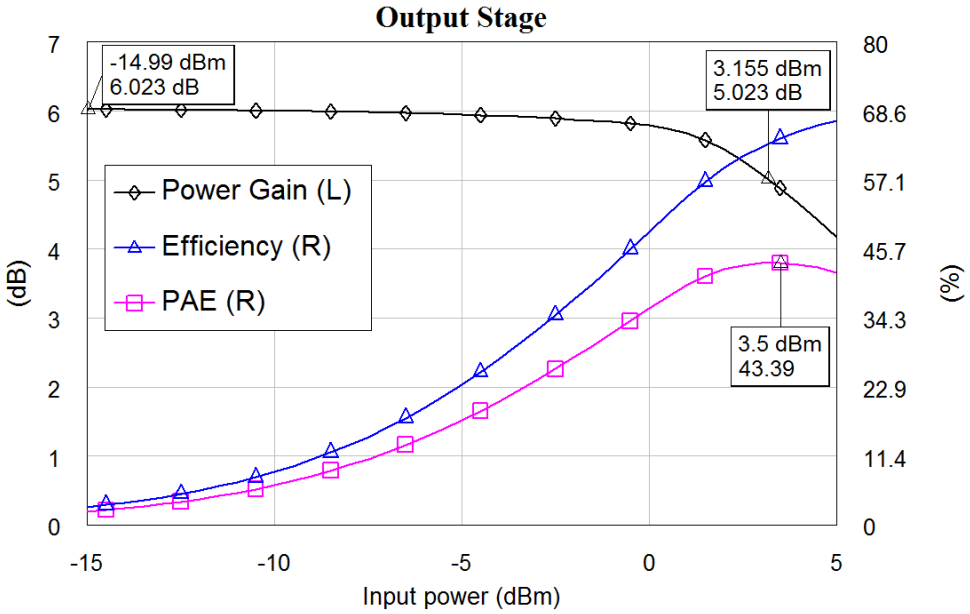



**Figure 5.8:** Large signal parameters simulated at 61.5 GHz.

### 5.3.2 Driver and Pre-Driver

The main goal for the stages preceding the last is to provide sufficient gain. However, it is crucial that they do not inflict on the large signal compression characteristics before the output stage. Also, the input stages have the potential of significantly undermining the output stage in terms of efficiency, and greatly reduce the overall effectiveness of the PA.

A common procedure when designing the stages preceding a power stage, is to halve the area of the amplifier compared to the subsequent stage (requires at least 3 dB power gain from each stage [33]). In this case that was a transistor with six and three emitters for the driver and pre-driver, respectively, both biased with 0.85 V. This was a good starting point, with a few adjustments necessary. With the designed output stage providing about 6 dB gain, the driver and pre-driver had to make up for the remaining 14 dB according to the specifications. A lower limit of 15 dB gain was set for the two input stages combined, with the aim of biasing them both with the same voltage for simplicity. It is likely that the pre-driver has a little more gain than the driver with the same bias. This is because more emitters in parallel reduce the gain slightly. With the bias voltage needed for 7.5 dB gain in the driver also applied to the pre-driver, they should exceed the limit of 15 dB combined power gain. With the bias voltage raised to 0.86 V, the gain increased to 7.8 dB gain for the driver with six parallel emitters, as displayed in Figure 5.11. The circuit schematic is shown in Figure 5.9. Table 5.2 list the performance of the driver, which is simulated in Figure 5.10 and Figure 5.12.

**Table 5.2:** Key figures of the driver/pre-driver.

| Performance metric | Value | Unit |
|---|---|---|
| Bias voltage | 0.86 | V |
| Number of parallel emitters | 6 | - |
| Power gain | 7.8 | dB |
| Quiescent current | 2.3 | mA |
| Peak power added efficiency | 39 | % |
| Output referred $P_{1dB}$ | 3.9 | dBm |

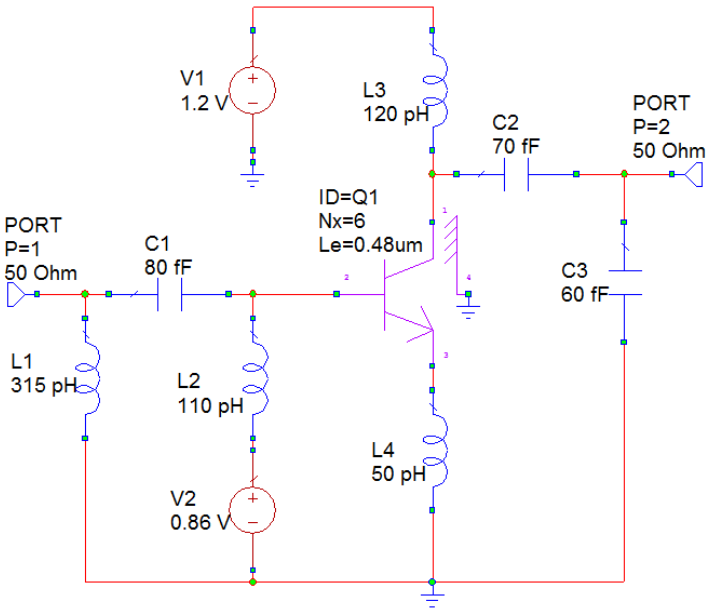



**Figure 5.9:** The schematic of the stand-alone driver/pre-driver.

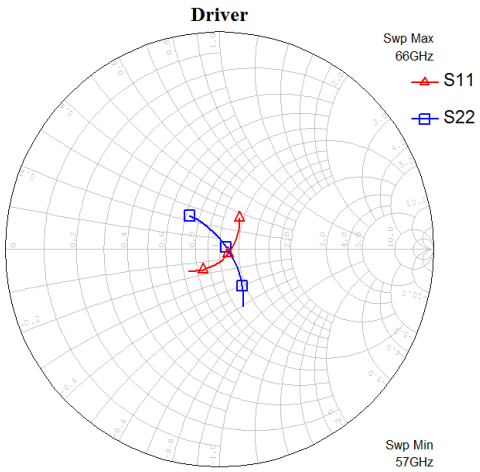



**Figure 5.10:** The matched S-parameters of the driver.

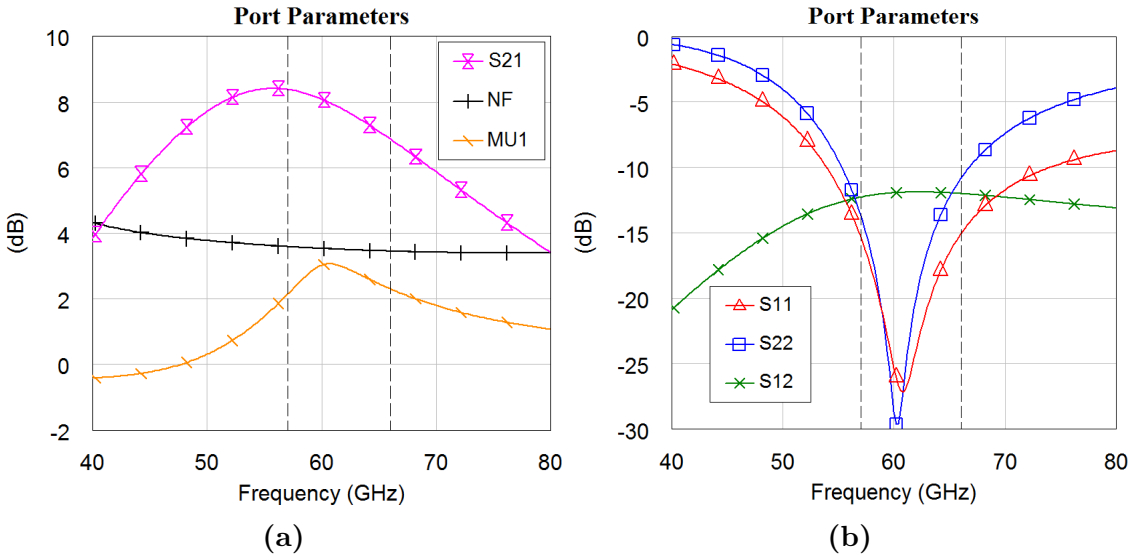



**Figure 5.11:** The port parameters of the driver/pre-driver. The dashed vertical lines indicates the bandwidth of the 60 GHz band.

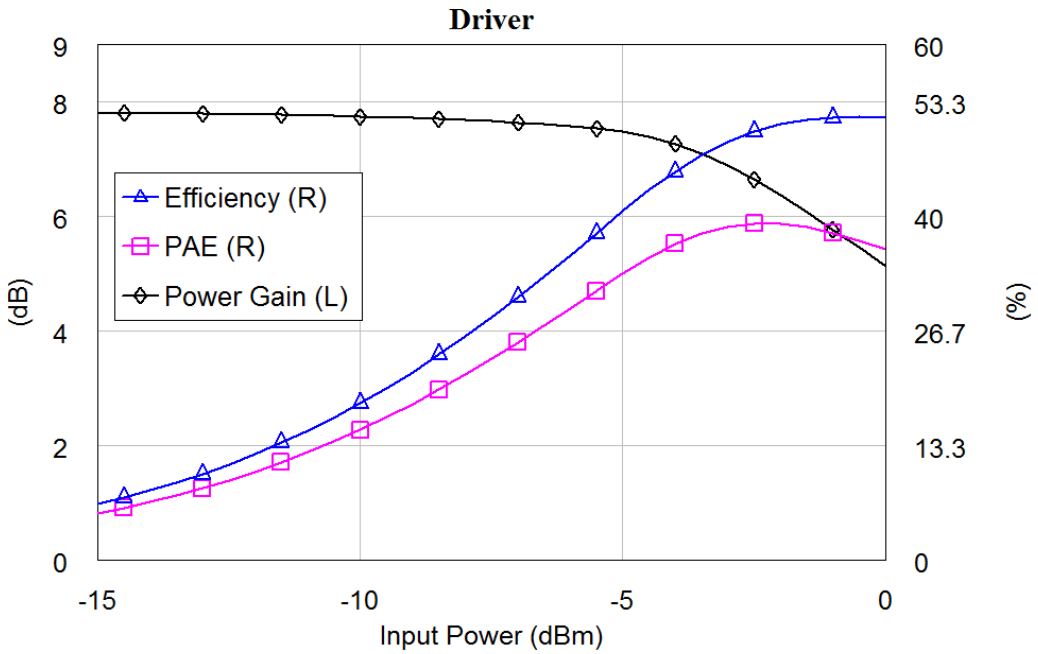



**Figure 5.12:** Large signal parameters simulated at 61.5 GHz.

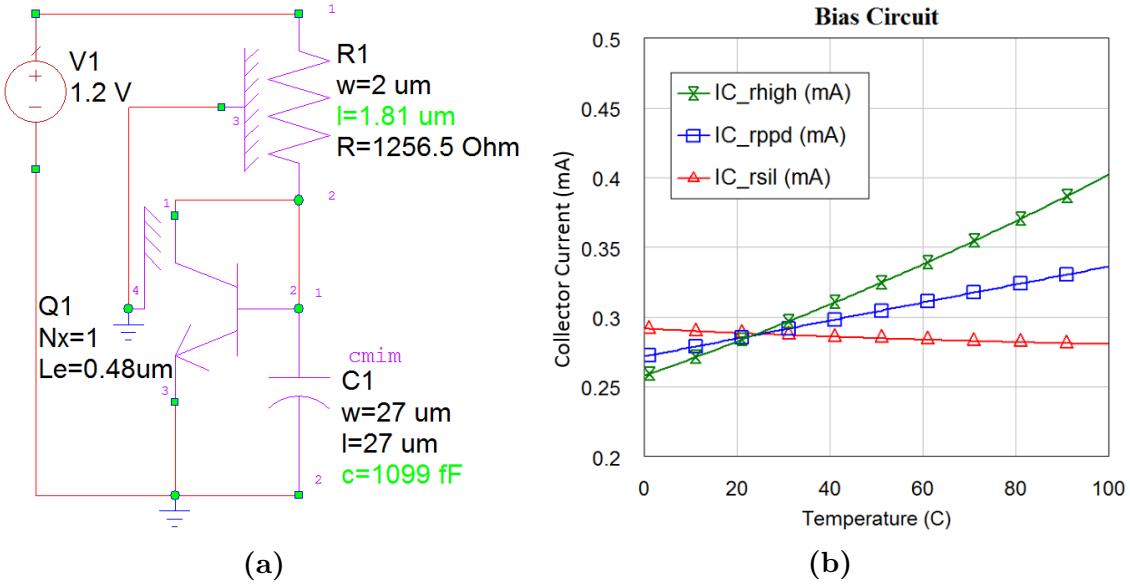
Trying to achieve the goal of 9 GHz bandwidth proved difficult with less than 6 emitters at 0.86 V bias voltage. This was solved by leaving the two stages identical, which consumes a little more power than what was intended. This was not a big issue, because the power consumption was well within specification at this point, and because two stages with 7.8 dB gain was sufficient. The circuit schematic for the pre-driver is then the same as for the driver shown in Figure 5.9. The performance

is also the same as for the driver, but the signal levels the pre-driver handle are lower. This means the pre-driver will operate at a lower efficiency than the driver will.

### 5.3.3 Bias Networks

The biasing of the power amplifier is implemented with the simple network in Figure 5.13 (a). The circuit is supplied with the global supply voltage of 1.2 V as specified for this power amplifier. Resistor $R1$ sets the bias current of $Q1$, and the current is mirrored to any transistor biased with the base/collector voltage of the bias network. The capacitor $C1$ ensures low noise and introduces a low impedance to ground for unwanted RF signals.

Simulation results in Figure 5.13 (b) show the temperature dependency of the collector current in a transistor for which the bias network is used. Three bias currents are plotted, one for each of the three resistors modeled in SG13S as $R1$ in the bias circuit. The best choice for minimal temperature variation is *rsil*. This is also the only option that prevents self-heating, because it will reduce the collector current with increased temperature. *Rsil* has a very low sheet resistance, which results in unpractical lengths for resistors in the order of kiloohms. The chosen resistor is the descent trade-off *rppd*, with a sheet resistance of 250 Ω. Another advantage *rppd* possess compared to *rsil* and *rhigh*, is better precision in the obtained resistance.




**(a)** **(b)**

**Figure 5.13:** The circuit schematic of the bias network is shown in (a). The simulated change in collector current with increased temperature in a single transistor biased with the network presented in (a).

## 5.4 Complete Amplifier

One way of achieving interstage impedance matches is to tune all stages separately to the same input and output impedance, e.g. 50 Ω. Then, when they are put together, the multistage amplifier is matched to 50 ohms at the input, output and in between stages. Some of the components in the matching network can be eliminated, but there might still be an excess of passive elements. This procedure requires more thorough impedance matching than presented in the previous sections on the output stage and driver/pre-driver.

Another way of achieving interstage matching is to tune the circuit after all stages are combined. Then the actual impedance values are mostly of only minor concern. Most important when matching between stages is maximum power transfer, which is obtained with conjugate matching. This approach was used when designing the complete amplifier shown in Figure A.1. After combining the three amplifier stages, only the necessary DC-block capacitors, RF-block inductors and emitter inductors were left in the schematic. Then, since the necessary components construct high-pass filters at the input and interstage, an additional low-pass filter was added at the output in order to obtain a better bandpass response, short circuiting most of the harmonics.

At this point, all transistor inputs and outputs had to be simultaneously matched. Looking at Figure 4.4, maximum power transfer at the input is achieved when the reflection coefficients $\Gamma_s = \Gamma_{in}^*$ and $\Gamma_{out} = \Gamma_L^*$ at the output. By plotting these reflection coefficient *pairs* (where one is the complex conjugate of itself) on the Smith chart, they can be determined as conjugately matched when they are very close at the frequency of interest.[3] $S_{11}$, $S_{22}$ and interstage reflection coefficients were tuned to conjugate matches in MWO, while also placing the load impedance of the output stage (*GAM3 load* in Figure B.2) in the area of optimal output power depicted by Figure 5.4. Table 5.3 lists the key figures of the simulated complete amplifier.

**Table 5.3:** Key figures of the power amplifier with ideal components.

| Performance metric | Value | Unit |
|---|---|---|
| Power consumption | 11 | mW |
| Power gain | 21.5 | dB |
| PAE | 30 | % |
| Output referred $P_{1dB}$ | 8 | dBm |
| Output referred IP3 | 18 | dBm |
| NF | 3.8 | dB |

[3]In MWO, a *gamma probe* can be implemented in any circuit connection, and calculate the reflection coefficients in both directions without changing the circuit behavior [3].

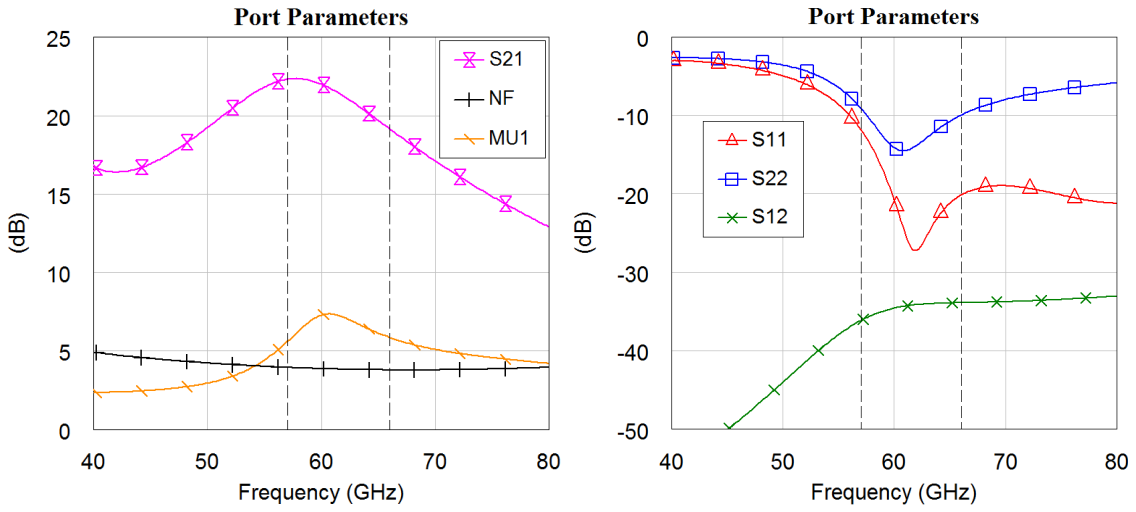



**Figure 5.14:** The port parameters of the complete amplifier. The dashed vertical lines indicates the bandwidth of the 60 GHz band.

The simulation results in Figure 5.14 show that the cost of achieving optimal load impedance was suboptimal interstage matches and $S_{22}$ a little worse than $-10$ dB at the far edges of the bandwidth. The trends in $S_{22}$ when a power amplifier has been optimized for maximum output power is normally worse than $-10$ dB in the whole passband. The results obtained here are thus relatively good. Large signal behavior is simulated in Figure 5.15 and Figure B.3.

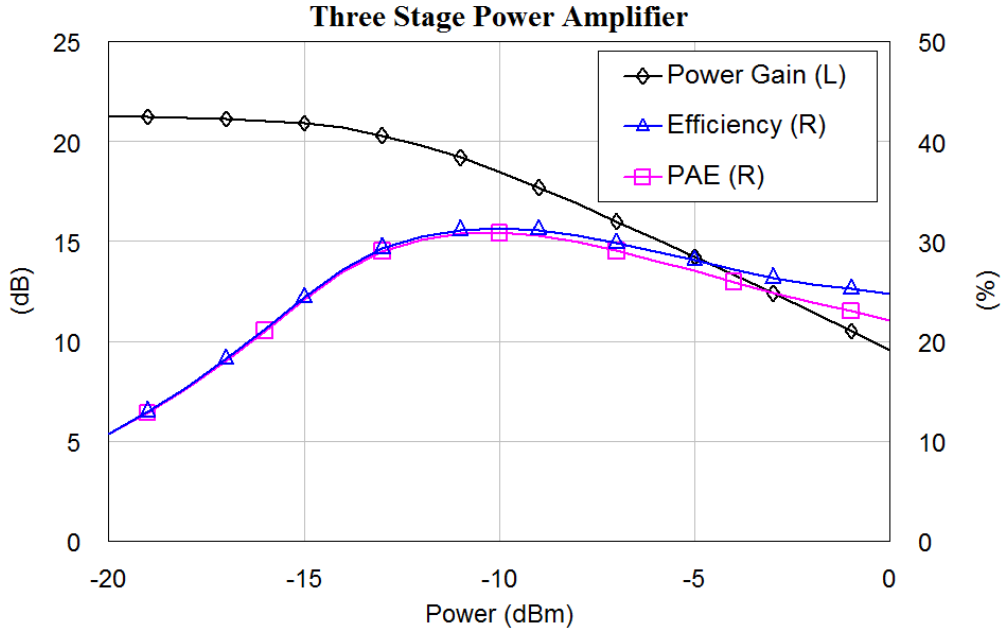



**Figure 5.15:** Large signal parameters simulated at 61.5 GHz.

### 5.4.1 Stability

To ensure that the PA is stable, each amplifier stage was emitter degenerated and separately designed unconditionally stable for a wide range of frequencies as documented in the previous section. However, the circuits have changed significantly and a thorough stability test is due, especially in between stages and for low frequencies. From around 11 GHz to about 27 GHz, $S_{22}$ is larger than 0 dB as shown in Figure B.5, which requires careful attention. The stability test explained in subsection 4.4.3 states that if the open loop frequency domain response $G = -\Gamma_1\Gamma_2$ encircles the $-1 + j0$ point in a clockwise direction, the system is unstable. $G$ is plotted for the base, collector and emitter of all amplifier stages in Figure 5.16. The simulations state that there are no instabilities. The $G$ calculated with the *gamma probe* at the emitter of the output stage encircles $-1+j0$, but in a counter-clockwise direction which does not indicate instability.

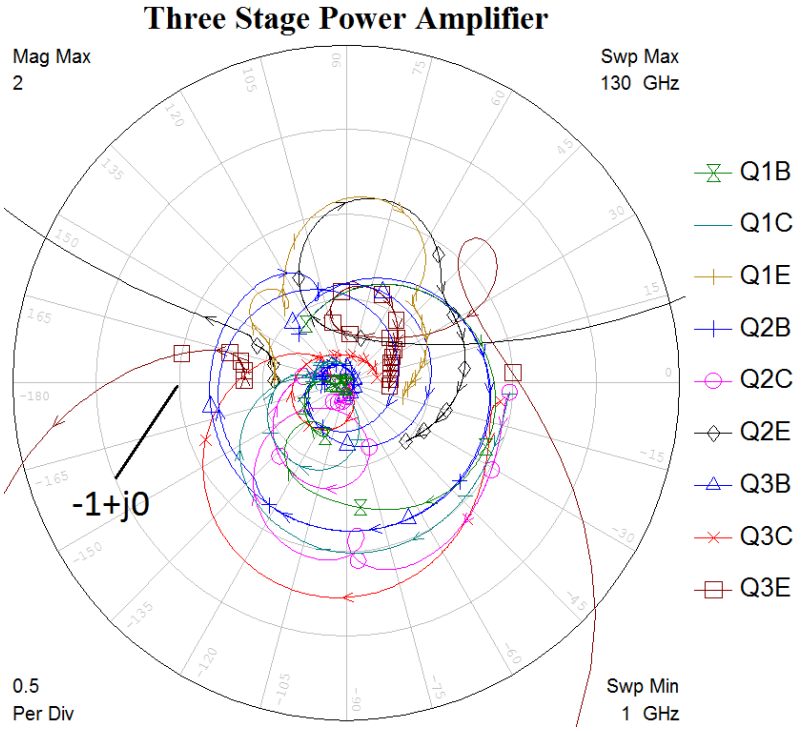



**Figure 5.16:** $G$ plotted for all transistor terminals. Stability simulations meet the Nyquist stability criterion explained in subsection 4.4.3.

CHAPTER 6

# Design Realization and Layout

The design from the preceding chapter is realized with non-ideal circuit elements. This includes resistors and capacitors modeled by foundry, as well as transmission lines characterized by the actual chip stack-up. A layout of the circuit is presented and optimized with simulations considering some additional structures from the layout.

## 6.1 Replacing Inductors with Transmission Lines

As mentioned in section 2.2, inductors are difficult to utilize at 60 GHz. The one included in the process library is useful for several hundred picohenries or more, and in its smallest possible size, the lead is about 110 μm, or 20° electrical length, which affects the frequency response significantly.[1] A decision was made to replace all inductors for transmission lines.

Inductors are fairly easy to realize with transmission lines, both series and shunt coupled. By swapping one by one and tuning the line length and width to reestablish the frequency response previously obtained, all inductors were excluded from the design. In addition, a quarter-wave short circuited stub was added at the output. It provides a high impedance to ground for odd harmonics, and basically short circuits the even harmonics. This is a good filter for the second harmonic frequency components, which are the largest in class AB as depicted by Figure 4.2

[1] With a dielectric constant of 4.1, the effective wavelength at 60 GHz is about 2.5 μm according to (3.7).

## 6.2 MIM Capacitors

The ideal capacitors were replaced with the MIM capacitors modeled in SG13S. The width and length was set equal for the best precision, and then the capacitance was approximated to the value of the capacitors being replaced. The simulated frequency response was essentially unaffected by the modeled MIM capacitors, so optimization of the real capacitors was unnecessary.

## 6.3 Layout

Considering the top view of the layout in Figure 6.1, the circuit was laid out with a signal path (input to output) from left to right, and with power supply at the top of the layout. The transmission line stubs were laid below the signal path. Metals in higher layers was used for RF signals because they have lower resistance and lower capacitance to the substrate than the lower layer metals. *Metal1* was chosen as a ground plane and *TopMetal2* for power supply. M2 - TM1 were utilized for interconnections, and for transmission lines TM1 was chosen. The lower metal layers have a lower maximum current density than the top layers. For M1 and M2 (and vias), the maximum currents had to be accounted for (e.g. where the AC current should not exceed 22 mA at the output stage, the metal connections were dimensioned to handle 30 mA). The use of vias was minimized in general, and they were made large for better reliability.

Interconnections were added in the layout to obtain a necessary space between the circuit elements. These were also included in the circuit schematic as short transmission lines. This way, their effect on the circuit behavior was simulated and compensated for.

Bending a transmission line affects the circuit behavior as if the transmission line was shorter. To reduce this effect, mitered bends was used.[2] By doing the layout while tuning and optimizing, the bends were considered because MWO models their effect on the circuit. The lines were laid out with coupling in mind; the distance was maximized between to lines where coupling is critical. This mainly concerned lines that can increase $S_{12}$, e.g. by introducing capacitance between base and collector of a transistor. Meandered structures were kept to a minimum while also minimizing the total area. These efforts to improve the circuit simulation should provide a good starting point for Electromagnetic (EM) simulation. A proper EM analysis is crucial to simulate coupling and other parasitics introduced by the structures in the layout. The power amplifier layout shown in Figure 6.1 measures 380 µm × 395 µm. More detailed pictures of the layout can be found in Appendix C.

[2] A mitered bend has some of the outer corner cut away, because it is essentially unused and causes reflections [3].

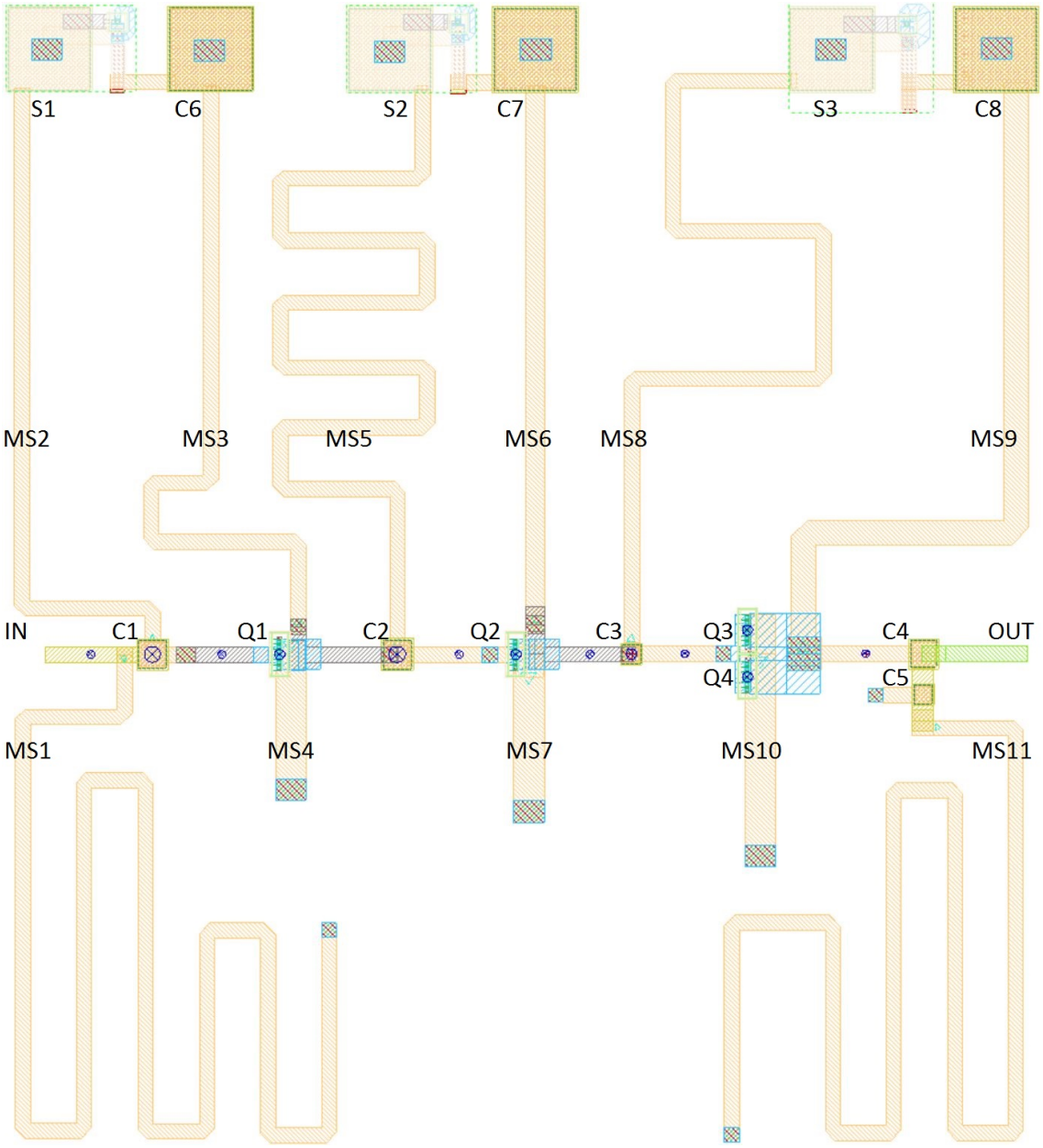



**Figure 6.1:** The layout of the entire power amplifier shown in Figure A.2. Ground plane and connection to $V_{CC}$ are not shown.

## 6.4 Post-Layout Simulation

With nearly all circuit components modeled (only vias remain), including the transmission line bends, the performance of the design was yet again simulated. The same simulations shown for the ideal design in chapter 5 were performed on the post-layout circuit schematic shown in Figure A.2. The port parameters and large

signal characteristics are shown in Figure 6.2 and Figure 6.3, respectively, and Appendix D contain more simulation results.

**Table 6.1:** Key figures of the complete amplifier.

| Performance metric | Value | Unit |
|---|---|---|
| Power gain | 21.5 | dB |
| Peak power added efficiency | 19 | % |
| 1 dB compression point | 6.5 | dBm |
| Output referred IP3 | 16.8 | dBm |
| Standby power consumption | 11 | mW |
| $P_{1dB}$ power consumption | 24 | mW |
| Area | 0.15 | $mm^2$ |
| Noise figure | 5.7 | dB |

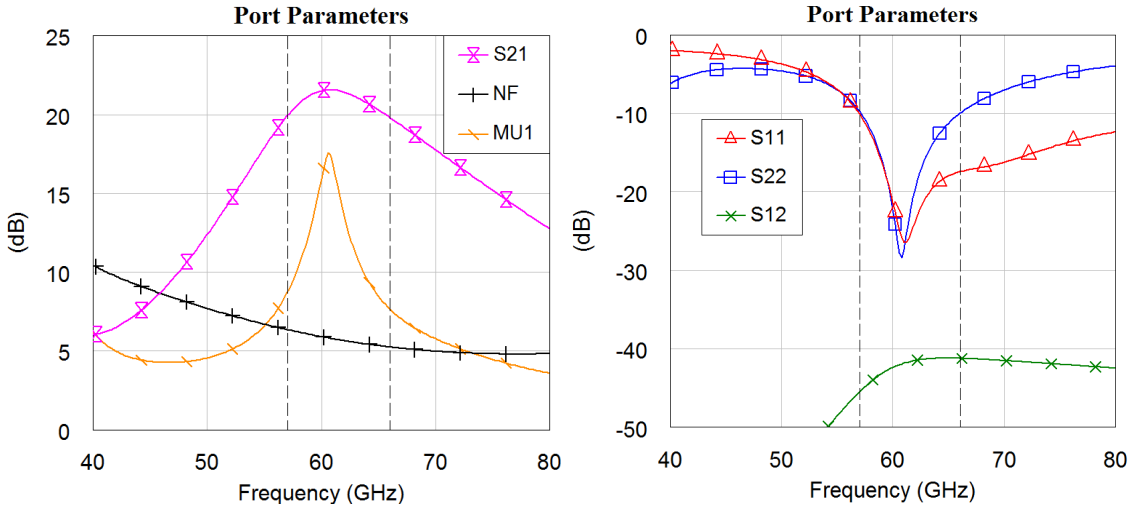



**Figure 6.2:** The port parameters of the complete PA in Figure A.2. The dashed vertical lines indicates the bandwidth of the 60 GHz band.

The simulation results show significant reductions in PAE and the 1 dB compression point compared to the ideal design in chapter 5. Figure 6.4 shows the load pull simulation illustrating the optimal load impedance for the best PAE and highest output power (Pload). Comparing the contours with those of Figure 5.4, the contours has moved slightly, because the 50 pH inductor in Figure E.4 was replaced with a 73 µm transmission line. The output impedance in Figure 6.4 has also moved compared to that of the ideal design, shown in Figure B.2. It is now further away from the optimal for maximum PAE. This is one of the causes for the reduction in efficiency, and another reason is the loss in the resistive transmission lines. There is a potential for optimizing for better PAE, but that would trade for lower output power, as the load pull contours depict.

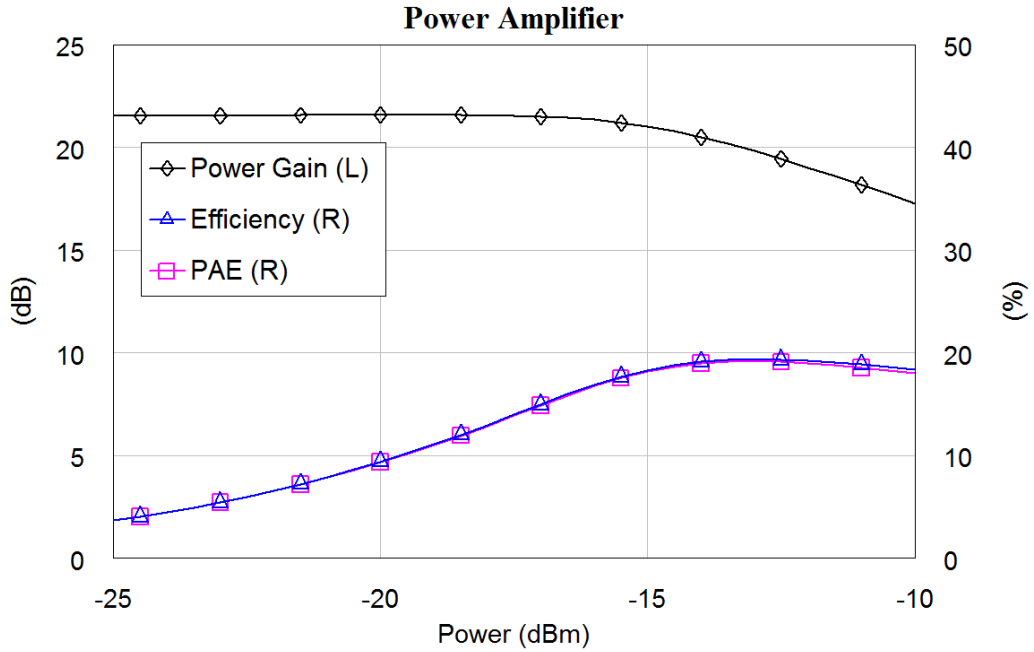



**Figure 6.3:** The large signal characteristics of the complete PA in Figure A.2.

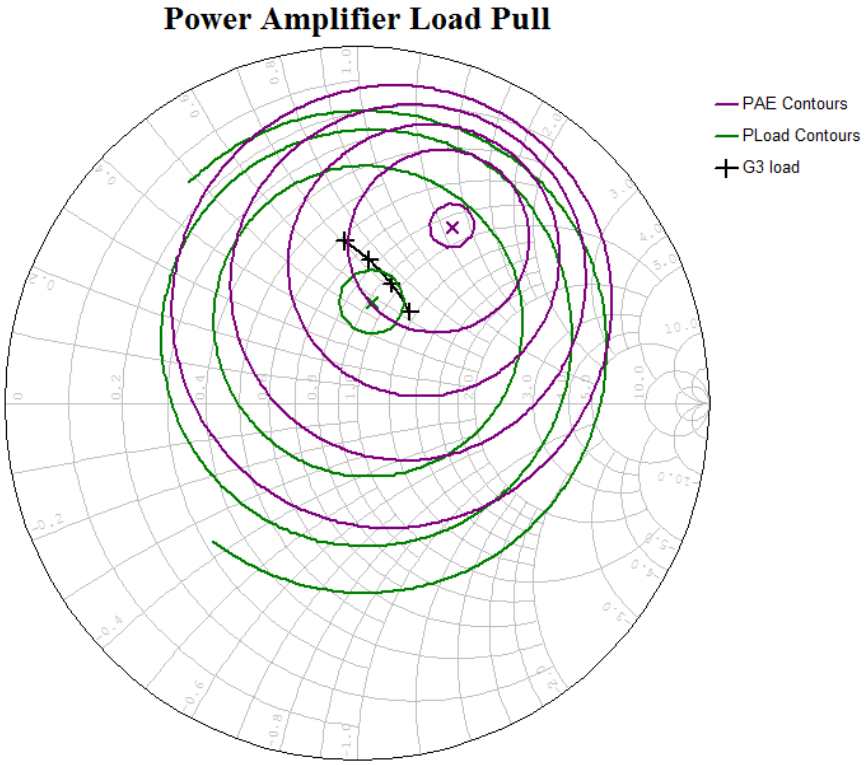



**Figure 6.4:** The impedance seen from the output stage (G3 load) overlayed on the load pull simulation. For every contour, Pload drops 1 dB while PAE drops 5%.

Some advancements are also seen compared to the pre layout simulations. No reflection coefficients exceed 0 dB and the stability analysis in Figure 6.5 looks better than the one in chapter 5. This improvement corresponds well with the reduction in the reverse transmission ($S_{12}$), seen in Figure 6.2. More resistance in the modeled circuit elements is also a contributor to stability improvements.

Since the power amplifier produces harmonics with its reduced conduction angle and gain compression, Fast Fourier Transformation (FFT) was performed on the simulated output signal at the 1 dB compression point. The results in Figure D.6, show that the second harmonic power is $-24$ dBc.[3] This is the the biggest of the harmonics, but all of them suffer a much greater free space path loss than the fundamental components and they are easily filtered at the receiver.

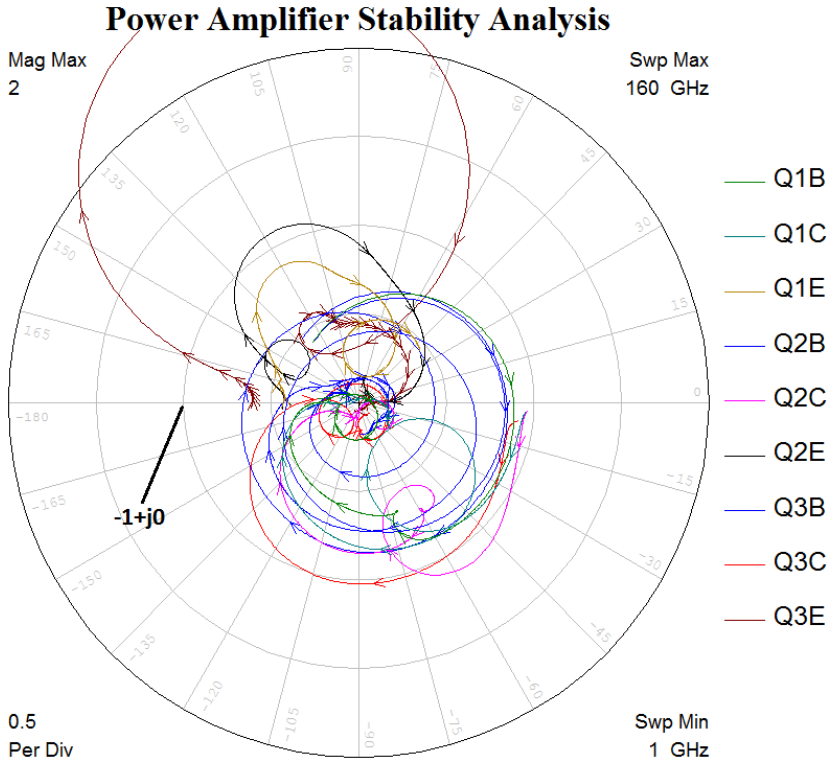



**Figure 6.5:** Stability analysis of the complete PA in Figure A.2. The PA is stable according to Nyquist's stability criterion.

[3]The power of a signal relative to the signal power at the carrier frequency can be expressed in dBc.

CHAPTER 7

# Discussion

This chapter contains a discussion of the work presented previously. Aspects regarding design, performance and simulation accuracy will be reviewed. Suggestions to future work to finish and improve the power amplifier are then proposed.

## 7.1 Performance

The presented amplifier performs within specification of the goals presented in Table 1.1. The power gain, $S_{21}$, peaks at the center frequency and declines nearly equally to both of the passband limits. To achieve the center frequency peak, $S_{22}$ suffered an increase at the lower end of the band. At 0.2 dB above the specified $-10$ dB, the added signal loss and reflections are insignificant, and thus $S_{22}$ is considered within specification. A common challenge in power amplifier design is the bad output return loss due to a poor conjugate match when optimizing for maximum output power (e.g. in [22], $S_{22}$ is between $-10$ dB and $-7$ dB in the passband, which is far from the worst results reported). In this work, both conjugate match and power match was achieved at the output stage.

The power consumption is about 24 mW when the power amplifier is operating at the 1 dB compression point. This is more than double the standby power consumption, which is due to the reduced conduction angle operation of the transistors. To compare the power amplifier to other published works, Table 7.1 lists five power amplifiers resembling the one in this work. Most of the SiGe millimeter wave PAs deliver around 20 dBm. They have been omitted not to make an unfair comparison. Some of the results listed are measured and can not be compared directly with the results in this work. Their measured results can be expected to be a little worse

**Table 7.1:** Comparison of SiGe mm-wave power amplifiers.

| | **This work** | [20]* | [29]* | [22] | [22] | [12]* |
|---|---|---|---|---|---|---|
| SiGe Technology [µm] | **0.13** | 0.13 | 0.13 | 0.18 | 0.18 | 0.25 |
| Frequency [GHz] | **61.5** | 77 | 58 | 60 | 60 | 60 |
| $P_{1dB}$ [dBm] | **6.5** | 12 | 10.2 | 7.2 | 5.5 | 14.5 |
| PAE [%] | **19** | 15.7 | 20.7 | 16.5 | 13.1 | 19.7 |
| Power Gain [dB] | **21.5** | 19 | 4.2 | 13.5 | 22.5 | 18.8 |

*Measured results.

than the simulated, as is frequently seen when these are plotted together.

## 7.2 Gain Flatness

The gain of a power amplifier is ideally flat within the passband, and simply zero for frequencies outside it. Reducing gain outside the passband can be achieved by filtering, but the flatness of the gain should be considered while designing the amplifier. A flat response is desirable in order to keep the ratio of the frequency components of the output signal the same as for the input signal. Depending on the requirements of the system, gain variation must be compensated for in order not to lose the information contained in the signals. The compensation of gain variation must be performed before the signal is down-converted [6]. As illustrated by Figure 1.2, the down-conversion takes place after the LNA on the receiver end of the wireless system.

Another consideration to be taken about the variation in gain is regarding gain compression. Even though the PA is capable of delivering more than 6 dBm with a single-tone input signal at 57 GHz and 66 GHz as displayed in Table D.1, the gain compression will be lower at the outer frequencies due to lower gain. Figure 6.2 shows a peak in $S_{21}$ at the center frequency, and it drops approximately 1.7 dB at both 57 GHz and 66 GHz. The signal component at the carrier frequency can put the amplifier in saturation because it is the largest at the output. This means that the output referred gain compression for signal components at the passband limits will be 1.7 dB lower than at the center. With the reported $P_{1dB}$ of 6.5 dBm at the center frequency, the $P_{1dB}$ at 57 GHz and 66 GHz is approximately 4.8 dBm because of gain variation.

A flatter gain can be achieved by making all the impedance matches broader, which enables a better power transfer at the outer frequencies. Another approach is to add more gain (e.g. with more amplifier stages) and spread it evenly over the passband. There is always a trade-off, both approaches mentioned increase the complexity of the power amplifier, and the second suggestion increases the power consumption.

## 7.3 Simulation Accuracy

All the simulations done in this work are based on the Process Design Kit (PDK) from IHP. It contains the circuit elements and their associated behavioral models. It also includes a chip *stackup*, containing all the relevant information about the materials, layer dimensions, dielectric constants, etc. in the fabrication process. The models have a specified range for which they are valid, where the accuracy is within a certain tolerance.

An important aspect to power amplifiers is gain compression, which usually occur when the collector voltage hits the *knee voltage*.[1] The transistors used in this work have a knee voltage that is below the valid range of the model, increasing the uncertainty of these results compared to results regarding S-parameters for instance. All simulation results should be verified with measurements.

## 7.4 CAD Tools

The computer-aided design (CAD) tool used for circuit design and analysis in this work was at first Cadence Virtuoso, and then National Instrument's AWR Design Environment Microwave Office (MWO). The change was made because Virtuoso does not offer all of the features important in microwave circuit design that MWO does. For instance the ability to simulate and plot the frequency response of a circuit, and then change the value of the circuit elements while observing the change in frequency response in real time. This saves a lot of time when optimizing and tuning a circuit, which is very frequent when designing microwave electronics.

## 7.5 Future Work

In order to have the PA block ready to be implemented in the top level design of the transceiver, certain tests and verifications should be performed. The power amplifier's performance should be verified with EM simulation, which takes account of all physical structures and parasitics. Further optimization should then take place to re-establish the wanted circuit behavior. Experiments on reducing the size of the layout can also be carried out. The supply voltage must be modeled correctly, and transient analysis is important to reveal any oscillations during start-up. Corner analysis will give insight to how well the power amplifier operates under process, voltage and temperature variations. Finally, Monte Carlo simulation is due to estimate the yield.

[1] The knee voltage is the lower limit of the collector voltage in linear mode, below which the transistor is in saturation.

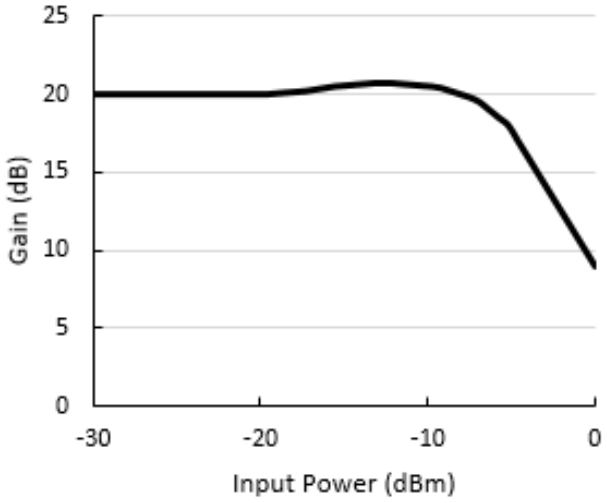



**Figure 7.1:** At large input power levels, the gain can increase a little before the transistor reaches saturation.

As for future changes in design to improve the power amplifier, a few design techniques can be experimented with. One of these is to design for *gain expansion* in some stages to compensate for overall gain compression. [12] has used this technique, which moves the 1 dB compression point closer to saturation and may increase the linear region and efficiency. Gain expansion happen in lower class AB operation at large drive levels, as illustrated in Figure 7.1.

An attempt was made to size pre driver smaller than the driver to save power, but this proved to be difficult in terms of bandwidth as mentioned in subsection 5.3.2. This is probably caused by the increased output impedance by having fewer transistors in parallel. Future work could include an effort to down-scale the pre-driver using transmission lines, which behaves differently than inductors and might enable a feasible reduction in size.

The load pull simulations in Figure 6.4 indicate that the optimal load impedance for maximum output power and the one for maximum PAE differ somewhat. It seems as if the PAE reduces more drastically than the output power when moving away from their respective optimal load impedance in the Smith chart. Thus it would be interesting to investigate whether a load impedance optimized more for PAE would result in a lower power consumption, even with an enlarged output stage to compensate for any loss in output power.

CHAPTER 8

# Conclusion

A comprehensive study in the field of RF circuits and microwave engineering has been conducted. This ultimately led to the design of a 60 GHz power amplifier, one block of a single-chip wireless transceiver. Performance wise, the simulations prove the power amplifier to meet the requirements, most of them with good margin.

A layout has been presented and is all set for electromagnetic simulation. There was not enough time to conduct the concluding tests and verifications, which remain for the power amplifier block to be implemented in the top-level design of the transceiver.

In other published works of 60 GHz power amplifiers, the trends in degradation of the measured results compared to the simulated are fairly good. This provides reason for believing that the finalized power amplifier designed in this work may meet the requirements also in measurements.

APPENDIX A

# Circuit Schematics

This appendix contains the two schematics of the three stage power amplifier, one with ideal components and one with modeled components. The latter is the final design of the power amplifier. The bias circuits are implemented as sub-circuits, shown separately.

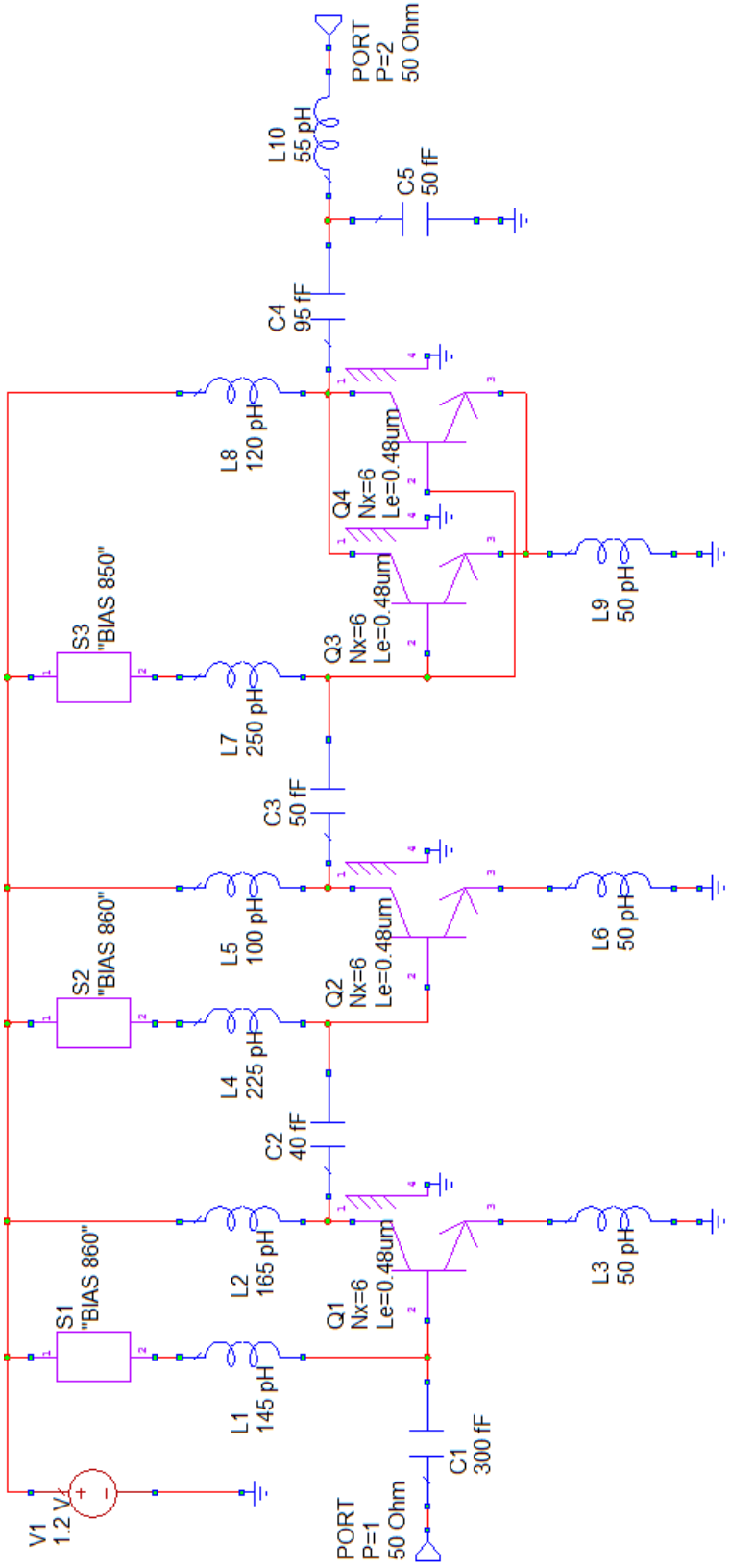



**Figure A.1:** The schematic of the complete ideal amplifier.

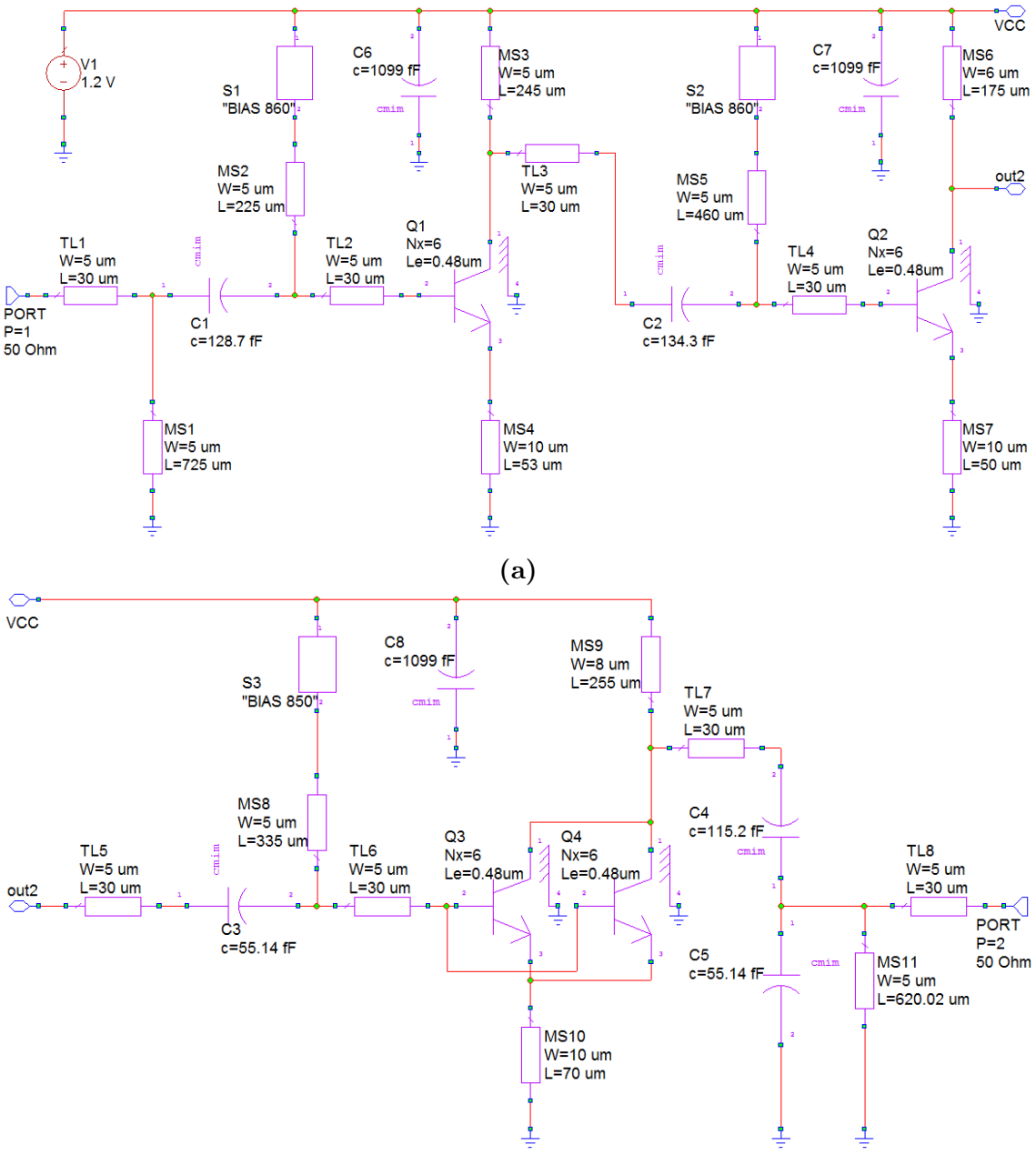



**Figure A.2:** The circuit schematic of the full power amplifier.

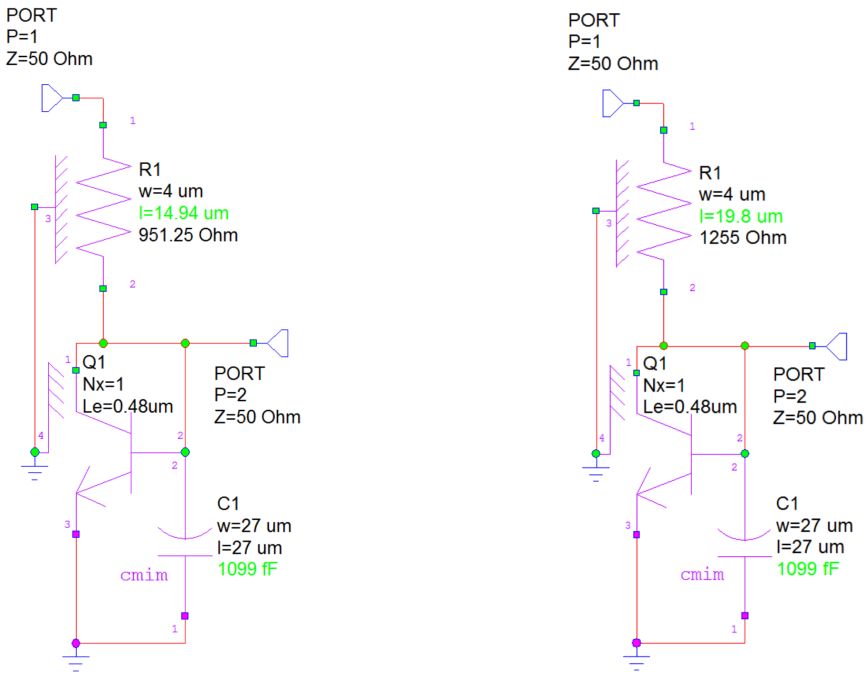



**Figure A.3:** The bias circuits shown as subcircuits in Figure A.2. $S1$ and $S2$ showed in (a), and $S3$ in (b). The ports are omitted in simulation when used as connectors as in subcircuits.

APPENDIX B

# Ideal Simulation Results

The design of the power amplifier with ideal circuit components is documented in chapter 5. Some of the less important simulation results are gathered here.

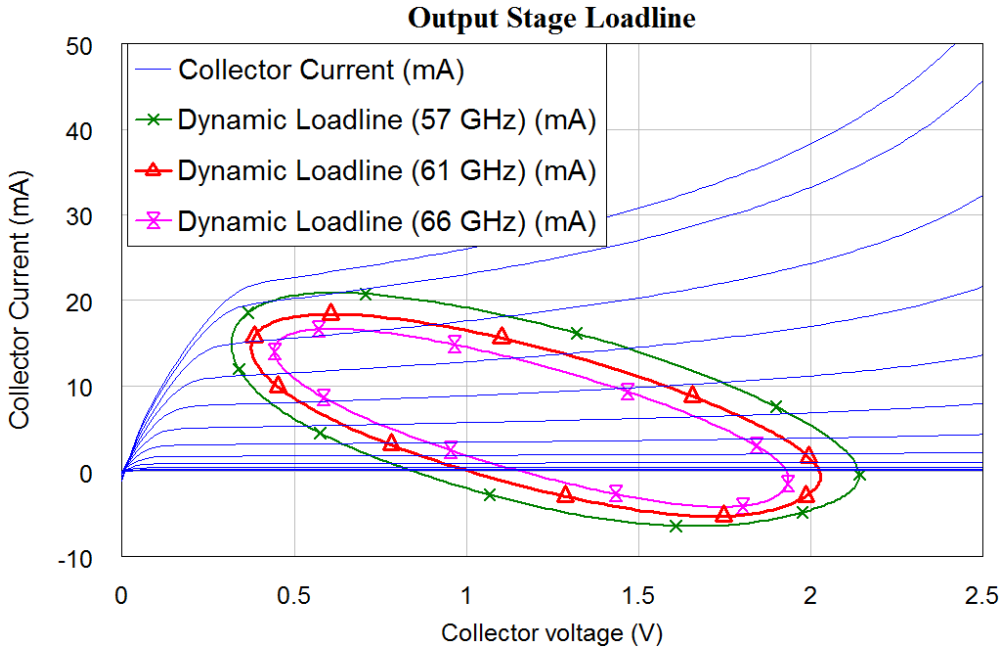



**Figure B.1:** The loadline plotted at the threshold of compression.

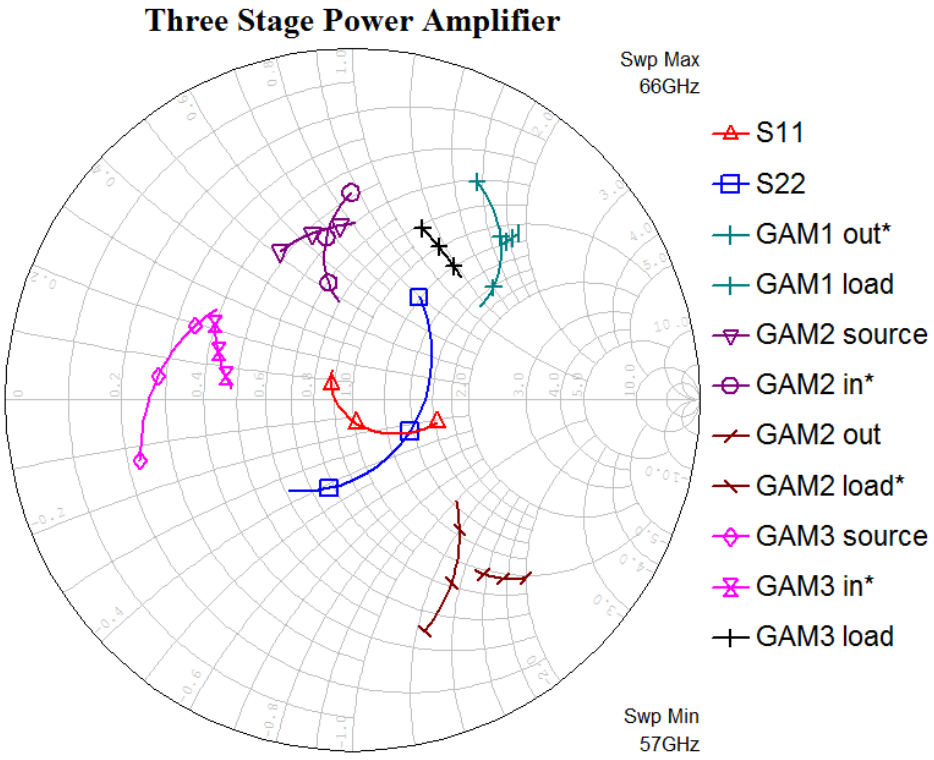



**Figure B.2:** The Smith chart showing $S_{11}$ and $S_{22}$, and the matched reflection coefficients. *G3 load* is placed where Figure 5.4 indicates optimum output power and good PAE.

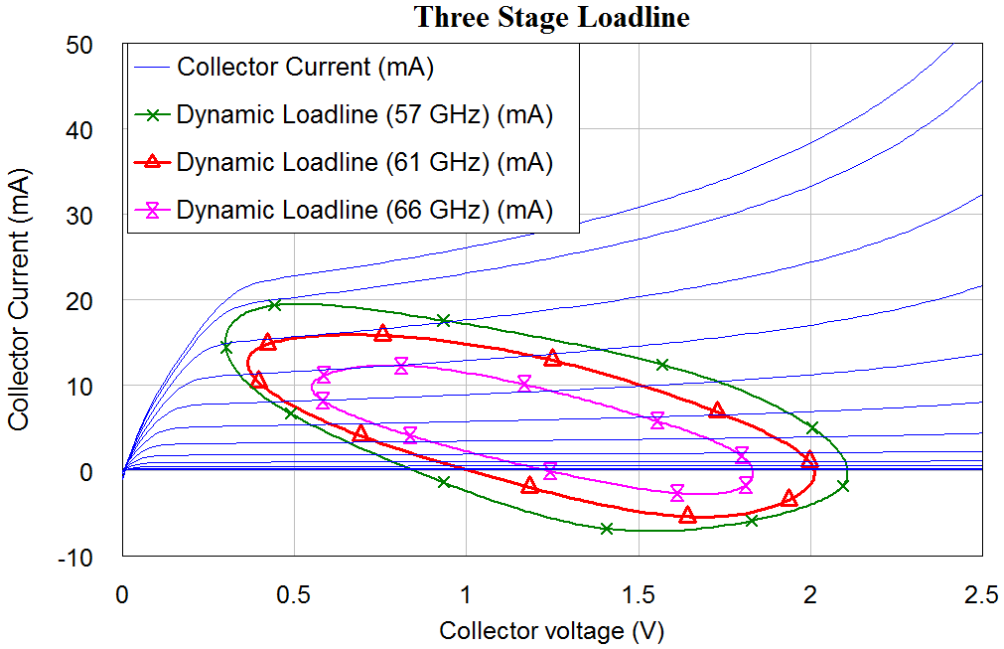



**Figure B.3:** The loadline plotted at the threshold of compression.

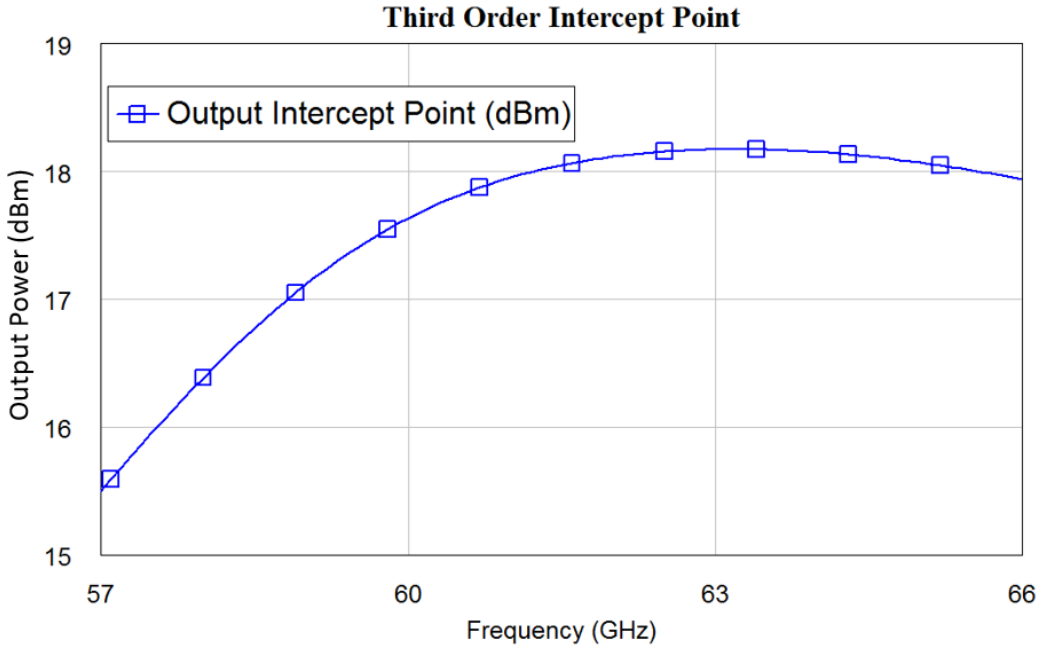



**Figure B.4:** The simulated output referred third-order intercept point.

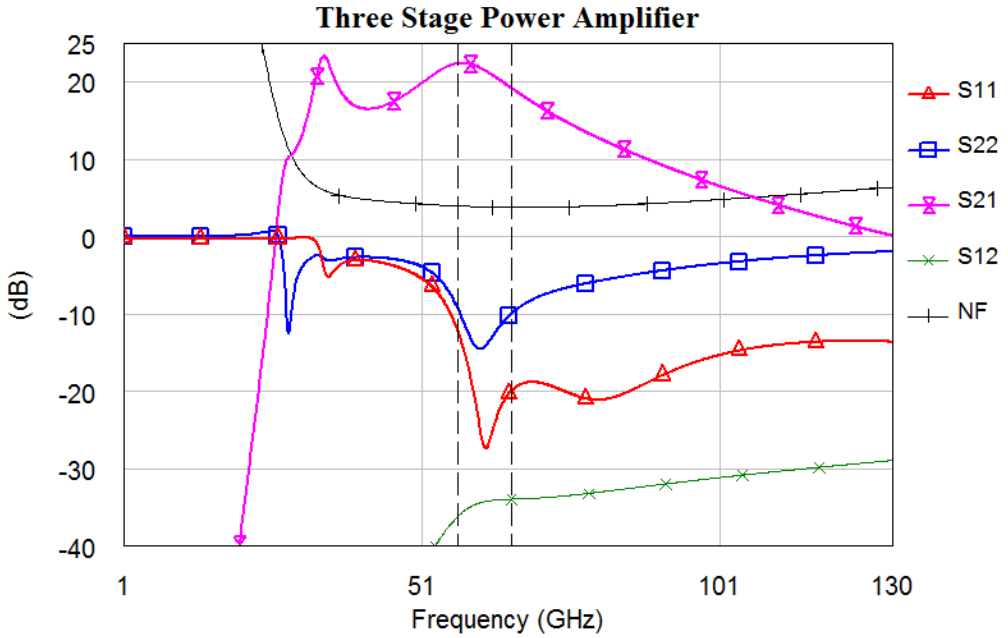



**Figure B.5:** Simulated port parameters for a very wide range of frequencies. S22 pose as problematic at low frequencies where it exceeds 0 dB.

# APPENDIX C

# Layout

Additional pictures of the layout in 3D are displayed here.

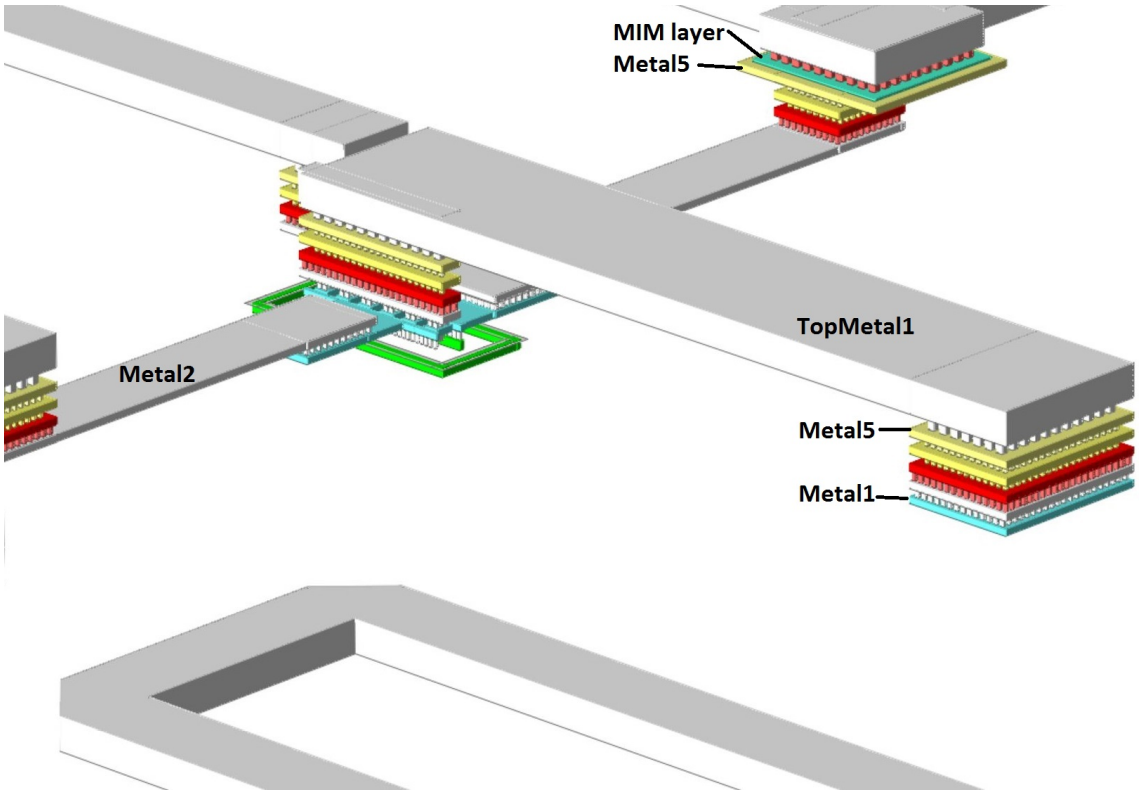



**Figure C.1:** 3D zoom of the input stage of the complete PA in Figure A.2.

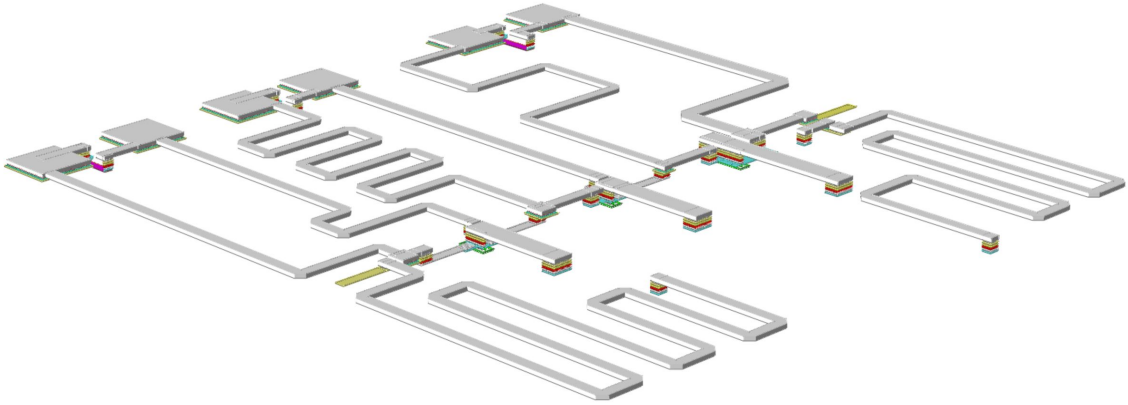


**Figure C.2:** The layout of the complete PA in Figure A.2 in 3D.

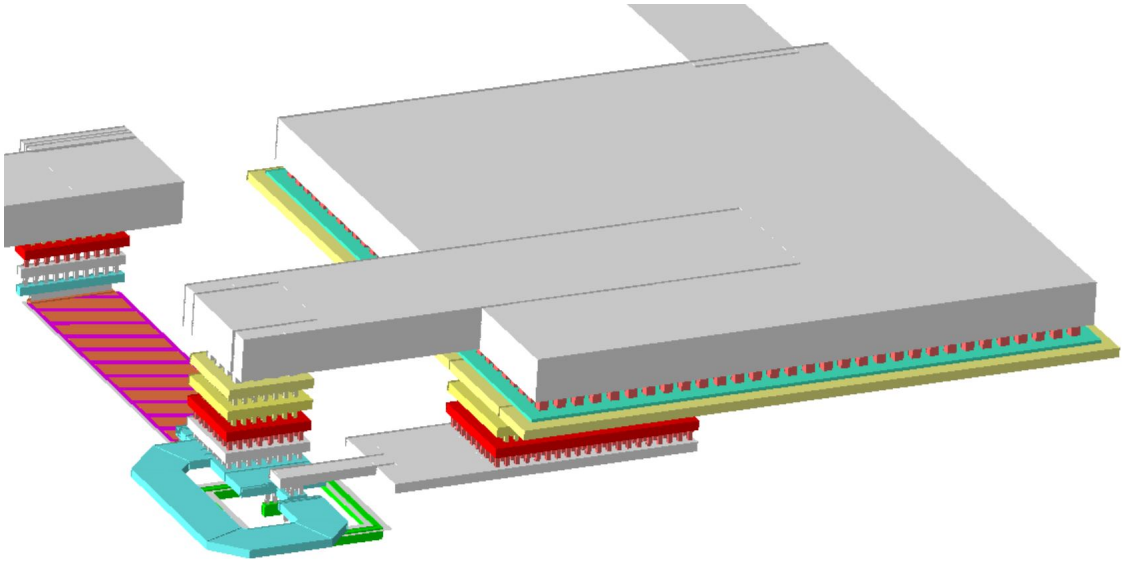


**Figure C.3:** 3D zoom of the bias circuit shown as component $S1$ in Figure A.2.

# APPENDIX D

# Post Layout Simulation Results

Documented in chapter 6 is the layout of the power amplifier with modeled circuit components, including transmission lines. The circuit behavior was then re-optimized and some of the less important simulation results are gathered here.

**Table D.1:** A detailed list of the key figures of the complete amplifier.

| Performance metric | 57 GHz | 61.5 GHz | 66 GHz | Unit |
|---:|:---:|:---:|:---:|:---:|
| $S_{11}$ | -10.1 | -22.9 | -17.5 | dB |
| $S_{22}$ | -9.8 | -25.7 | -10.0 | dB |
| $S_{21}$ | 19.9 | 21.5 | 19.8 | dB |
| $S_{12}$ | -45.5 | -41.7 | -41.2 | dB |
| Peak PAE | 16 | 19 | 21 | % |
| Output referred $P_{1dB}$ | 6.4 | 6.5 | 6.9 | dBm |
| Noise figure | 6.4 | 5.7 | 5.3 | dB |

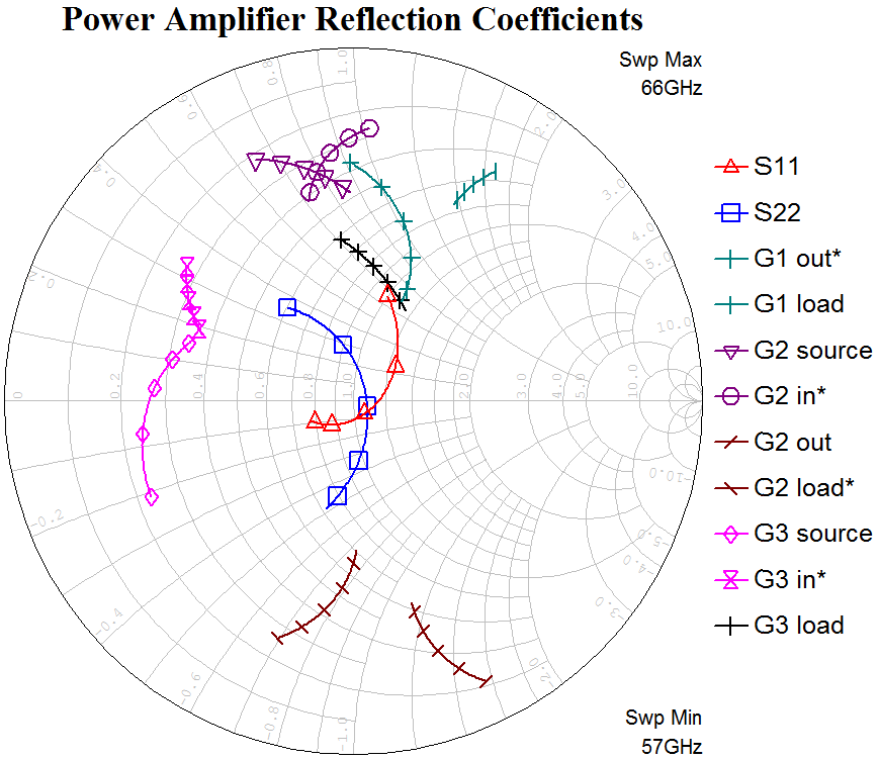



**Figure D.1:** Simulated reflection coefficients of the complete PA in Figure A.2.

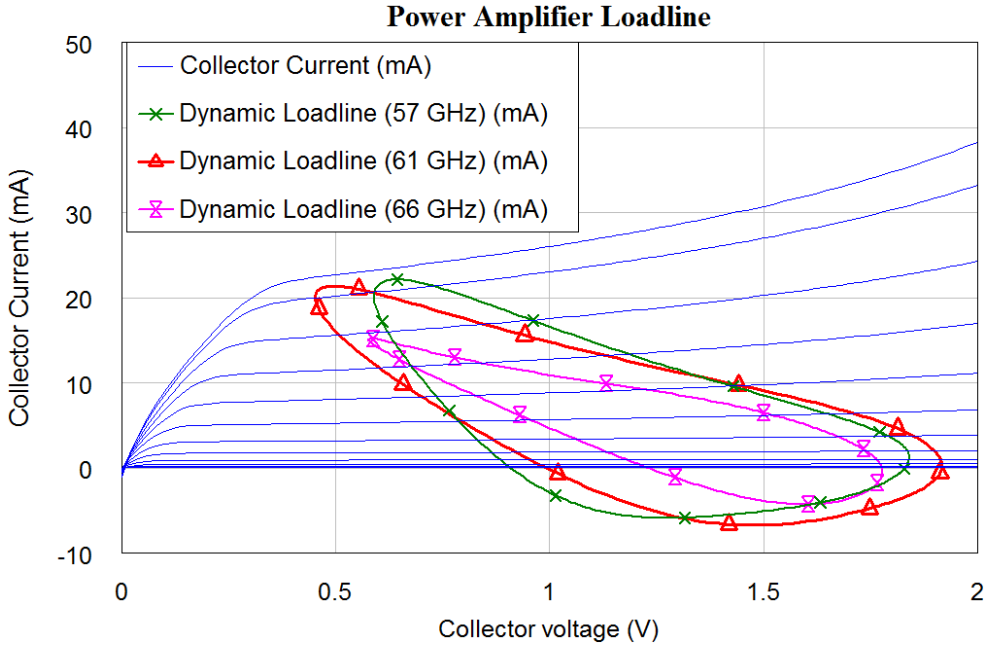



**Figure D.2:** The loadline of the complete PA in Figure A.2.

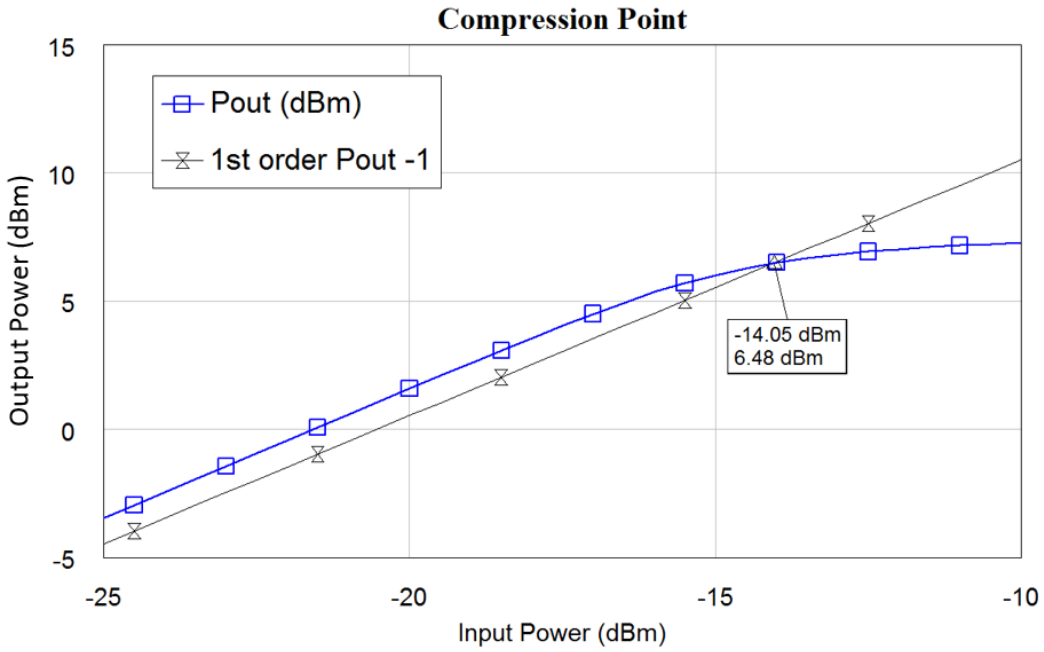



**Figure D.3:** The output power plotted with respect to input power. The first order response is 1 dB lower than *Pout*, indicating the 1 dB compression point at the intersect of the two lines.

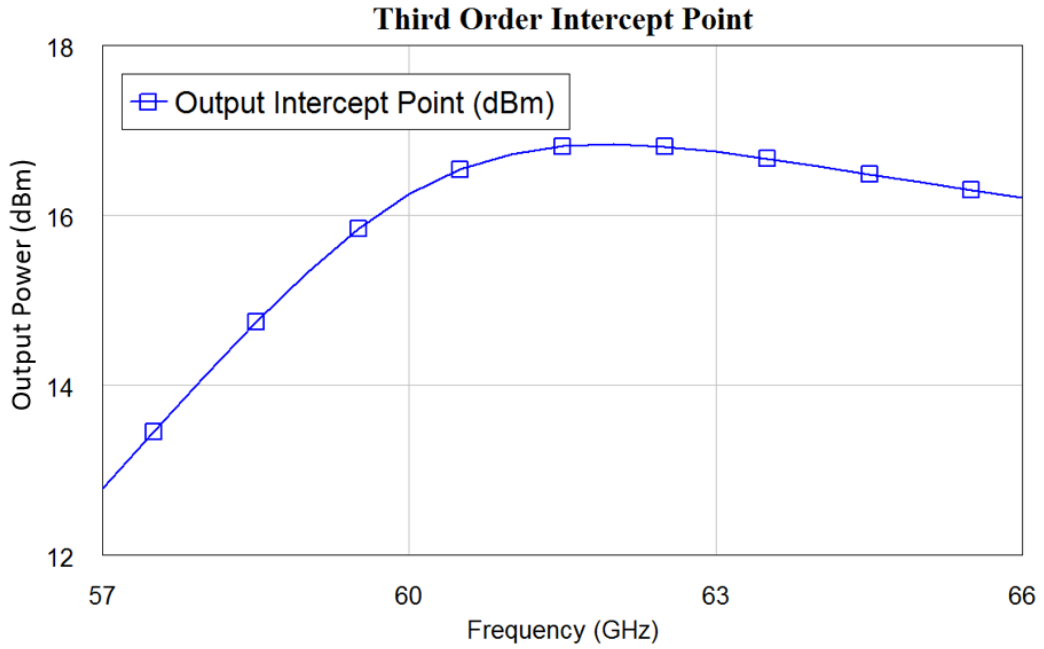



**Figure D.4:** The third order intercept point of the complete PA in Figure A.2.

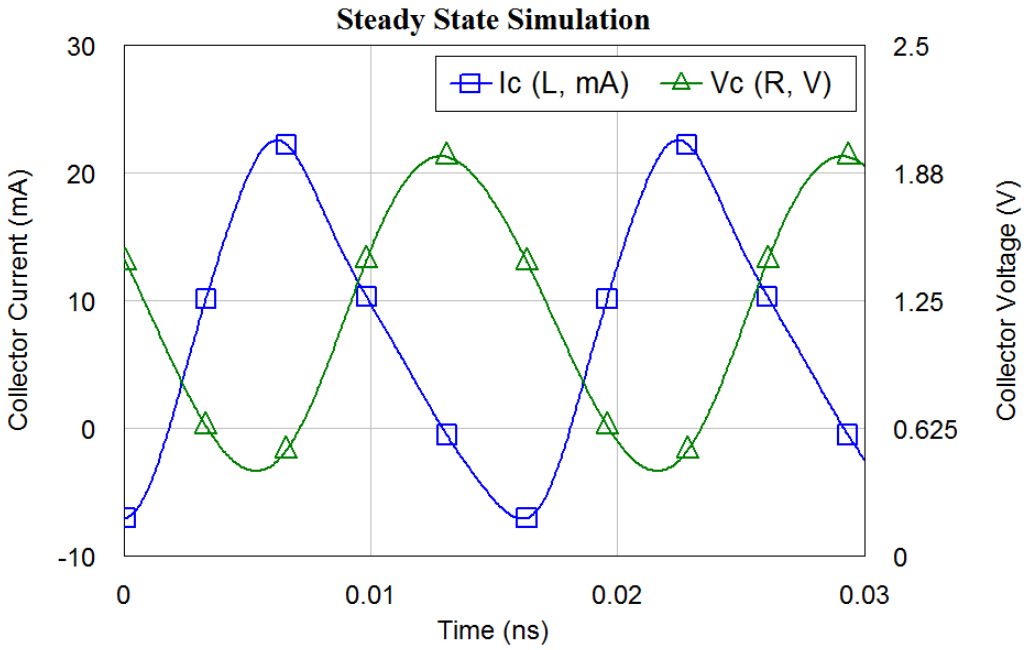



**Figure D.5:** Steady state analysis of the current and voltage at the collectors of the output stage. The signal is 61.5 GHz, driving the power amplifier in 1 dB compression.

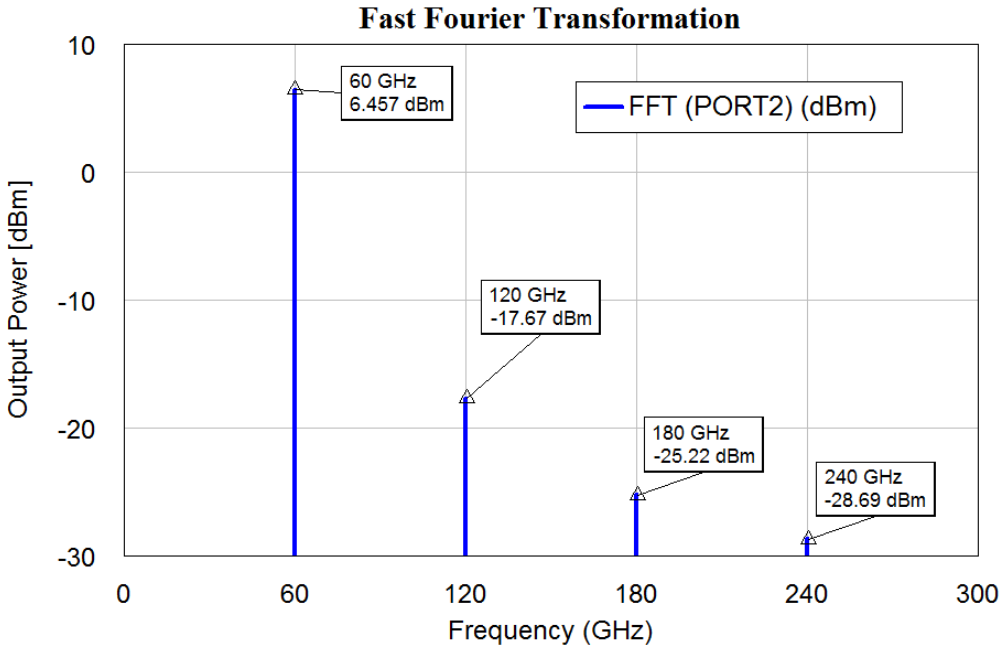



**Figure D.6:** Fast Fourier transformation of the output signal in 1 dB gain compression, simulated at 60 GHz for simplicity.

# APPENDIX E

# Test Benches

This appendix contains the circuit schematics used in specific simulations performed in the power amplifier design.

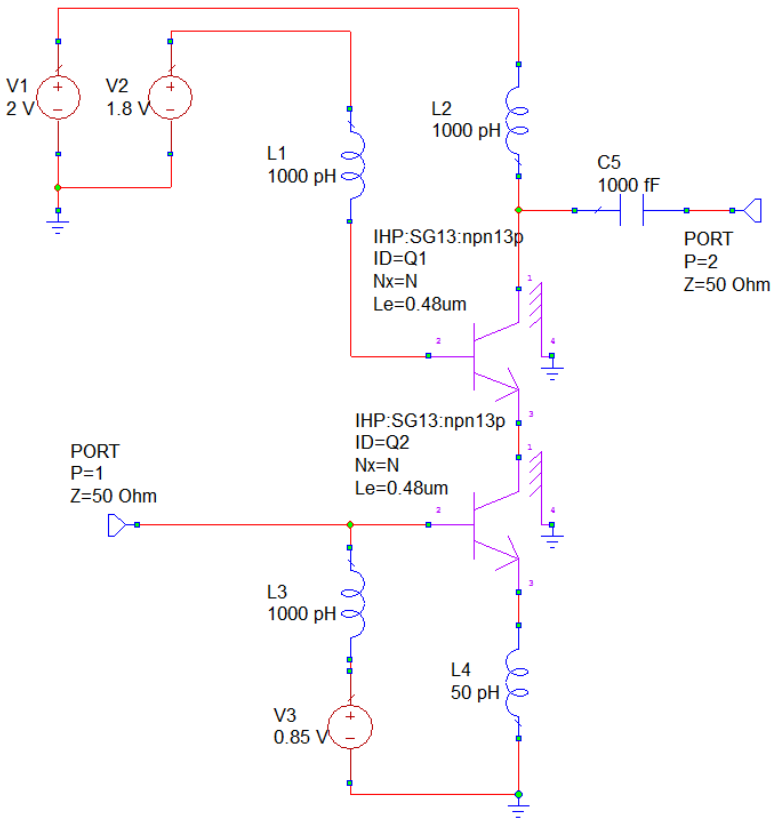
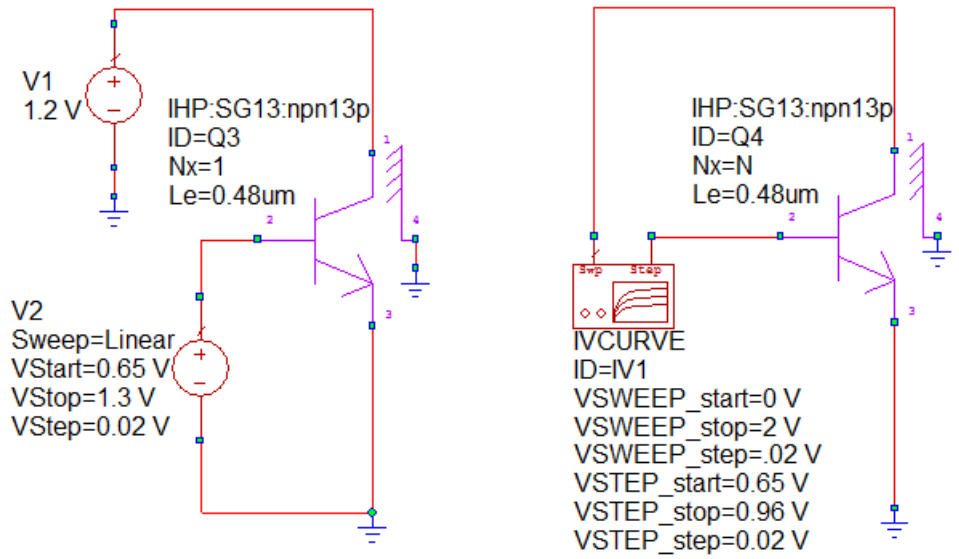



**Figure E.1:** The test bench for simulation on the cascode configuration. Matching networks are not shown.




**(a)** **(b)**

**Figure E.2:** Test benches used for simulating DC characteristics.

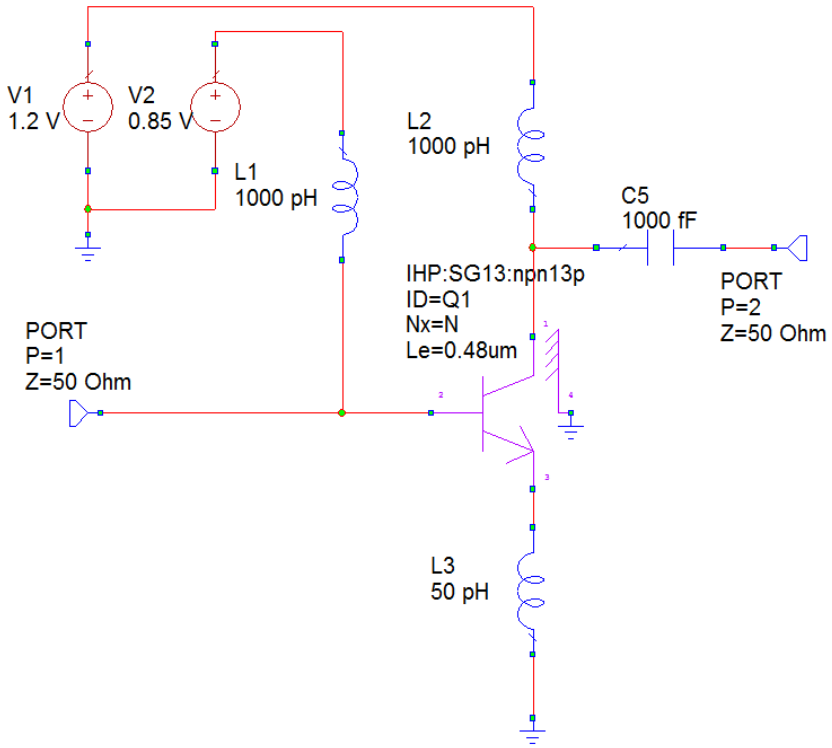



**Figure E.3:** A common emitter test bench, matching networks are not shown.

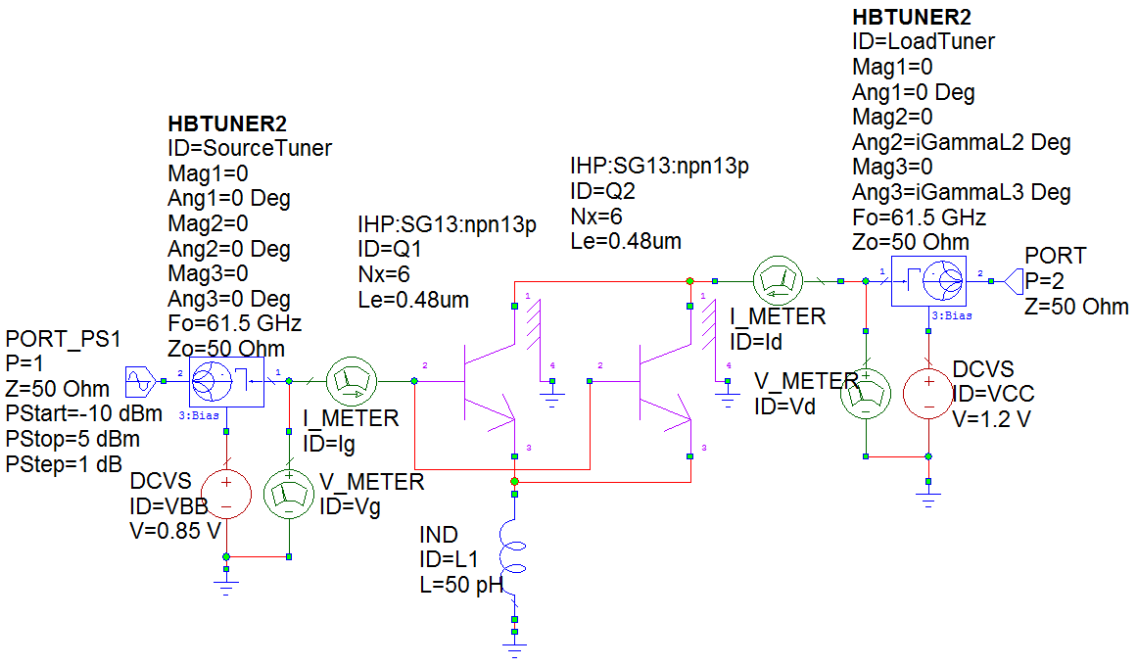



**Figure E.4:** The test bench for load pull analysis in MWO.

# Glossary

**BJT** Bipolar Junction Transistor.

**CAD** Computer-Aided Design.

**CB** Common Base.

**CE** Common Emitter.

**CMOS** Complementary Metal Oxide Semiconductor.

**EM** Electromagnetic.

**FFT** Fast Fourier Transformation.

**HBT** Heterojunction Bipolar Transistor.

**IP3** Third-Order Intercept Point.

**LNA** Low Noise Amplifier.

**MMIC** Monolitic Microwave Integrated Circuit.

**MWO** Microwave Office.

**NF** Noise Figure.

**OOK** On-Off Keying.

$\mathbf{P_{1dB}}$ 1 dB Compression Point.

**PA** Power Amplifier.

**PAE** Power Added Efficiency.

**PDK** Process Design Kit.

**RF** Radio Frequency.

**SiGe** Silicon Germanium.

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