

DEVELOPMENT OF A TRANSMITTER
FOR HIGH TEMPERATURE
ULTRASOUND IMAGING

A THESIS BY
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Abstract

This thesis presents the development and testing of a new transmitter in an ultrasound imaging tool used for imaging the inside of oil wells in temperatures of up to 180 °C. The imaging tool can have up to 288 transducer elements, driven by 16 transmitters. This generates a need for lots of switches, increasing the load capacitance, which results in a demanding current requirement.

Every part of the original transmitter is analyzed and potential improvements is proposed and implemented. After improving the design and component choices, a new layout is performed for one channel, using the same area as the old channel. Both the old and new design is soldered on one PCB to test them under the exact same circumstances.

Tests have been done during the design process to verify components and to obtain coefficients for calculating core loss. This is used for calculating core loss and optimizing the core size.

With ultrasound imaging, the resolution is highly dependent on signal frequency. This is why Bergen Technology Center uses ultrasound transducers with upper frequencies of up to 6 MHz, especially for thickness measurements. But, the transmitter in use today for driving the transducers is only capable of maximum output signals up to 2 MHz.

The new design has been tested both with dummy loads and in a complete tool. Tested with a complete ultrasound imaging tool, the new transmitter showed an increase in amplification from the old design of 24 dB at 6 MHz.

Temperature tests have been performed with dummy loads up to an ambient temperature of 180 °C. With maximum frequency, temperature and frame rate, the new design shows an amplification of 36 dB, 23 dB higher than the old design under the same circumstances. Temperature rise of the critical components has been logged during the tests, and is used with power dissipation for calculating thermal resistance.

Improvements has also been proposed for other parts of the imaging tool. New switches are proposed that will reduce the switch capacitance with 29 %, improving slew rate and output signal amplitude. A modification of the input signal is proposed that will decrease the output pulse duration and give better axial resolution.

Preface

The work in this thesis has been carried out within the Research and Development department at Bergen Technology Center (BTC) between August 2015 and June 2016. It is submitted for the degree of Master of Science in Physics at the University of Bergen June 1st, 2016.

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Espen Håland
Bergen, June 2016

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Introduction

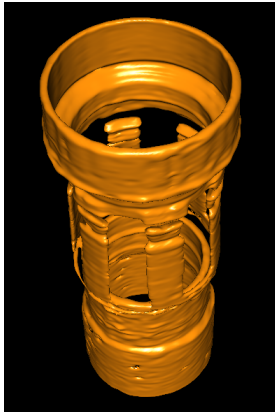
1.1 Oil Well Imaging

Oil wells consist of a large number of steel pipes joined together to achieve a continuous hollow tube, extending several kilometers down through the earth surface. Oil companies are dependent on continuous production and need to be able to image the inside of the well to discover corrosion, fractures and other irregularities that can threaten well integrity. Objects can also get stuck in the oil well, making it essential to have an image of the situation to be able to perform a successful fishing operation.

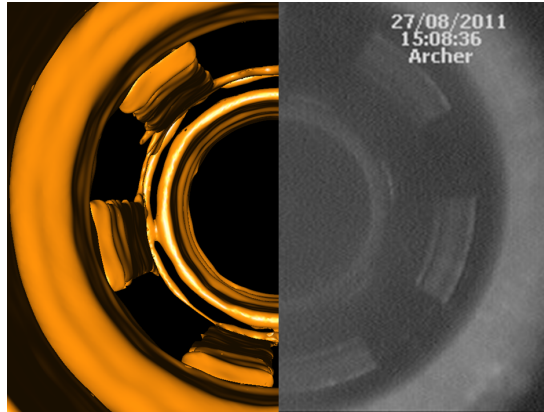
A fishing operation is performed when an object is stuck in the well. The object and its surroundings is mapped in 3D to be able to choose an appropriate tool to retrieve it to the surface.

There are many imaging tools on the market today, including mechanical finger tools, optical cameras, X-ray imaging tools and ultrasound imaging tools. What makes developing downhole imaging tools challenging is the size restriction due to small pipe diameter as well as the demand for operating in high temperature and high pressure as depth increases. It can also be difficult to image through a mixture of oil, gas and water, depending on the imaging technology.

Mechanical finger tools are available for use in temperatures up to 177 °C. The principle is to let a set of fingers be pressed out from the cylindrical tool and continuously touch the inner wall. By monitoring the position of the fingers it is possible to measure the inner diameter. This tool is not suited for fishing operations. The accuracy depends on mechanical tolerances which will increase due to continuous wear of the fingers. The fingers can also get stuck in cracks and sediments.



(a) 3D ultrasound image of a slotted steel pipe [3].



(b) Ultrasound image (left) and optical image (right) of a slotted steel pipe [3].

Figure 1.1: Images of a slotted steel pipe.

In optical cameras, light is converted to electrical signals. The high opacity of oil allows only small amounts of light to pass through, reducing the signal received in the camera. This can be prevented by filling the well with a transparent liquid, but is time consuming and costly. There are optical cameras that only fill a small volume in front of the tool with a transparent liquid, but these are limited to a maximum depth of 1000 m.

The principle behind ultrasound imaging is to transmit an acoustic signal and measure the time it takes to reach the inner wall, reflect and return to the tool. Water and oil have similar acoustic properties, making it possible to capture images with high accuracy through this mixture, which is the most common content of production wells.

The large difference in acoustic impedance between gas and fluids like oil and water causes high signal reflection. This reduces the amount of acoustic energy making it all the way to the object you want to image, and thus low signal amplitudes for the received signal. Imaging through a mixture of oil and gas can therefore be difficult, especially if the bubbles are large, blocking the entire scan area.

A comparison between an image from the Ultrasound Imaging Platform (UIP) and an image from an industry leading optical camera is shown in 1.1b. The image shows a steel pipe which is slotted to allow flow from the reservoir into the pipe.

When drilling a well, drilling fluids (often referred to as mud) can be injected at the point of the drill bit to cool down and lubricate the drill bit. It also transports rock fragments towards the surface[28]. The acoustic properties of drilling fluids makes it difficult to use ultrasound imaging. Another situation showing difficulties for the UIP is through thick layers of sand that typically occur on the low side of non-vertical wells, depending on the inclination.

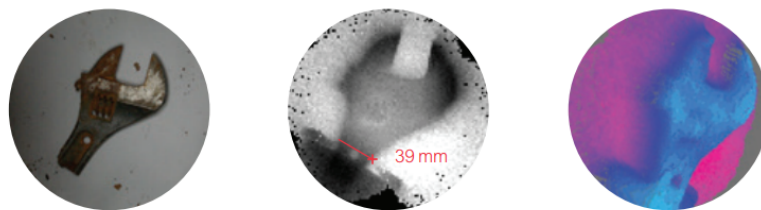


Figure 1.2: X-ray images of a wrench. 2D (middle) and 3D (right). The left image is from an optical camera [27].

A downhole imaging tool based on X-ray technology was recently announced, being able to image in all production fluids. It can also image through drilling muds[26] and sand covered objects, but is at the time limited for use up to a temperature up to 100 °C. A tool able to operate in temperatures up to 130 °C is said to be available in the second half of 2016[27]. 2D and 3D images from this X-ray tool is shown in Figure 1.2.

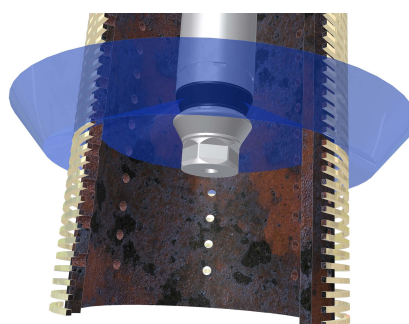
1.2 Ultrasound Imaging Platform

Bergen Technology Center AS (BTC), a wholly owned subsidiary of Archer AS, designs, develops and manufactures ultrasound imaging tools for downhole operation. The newest tool, UIP, produce high-resolution 3D images and measurements of well components. It has no moving parts and can operate in all production fluids.

By changing transducers it can be configured to look along the well for fishing operations, as shown in 1.3a. It can also look sideways for measuring cracks, corrosion and sediments, as shown in 1.3b.



(a) UIP configured for looking along the well [3].



(b) UIP configured for looking sideways [3].

Figure 1.3: UIP configurations.

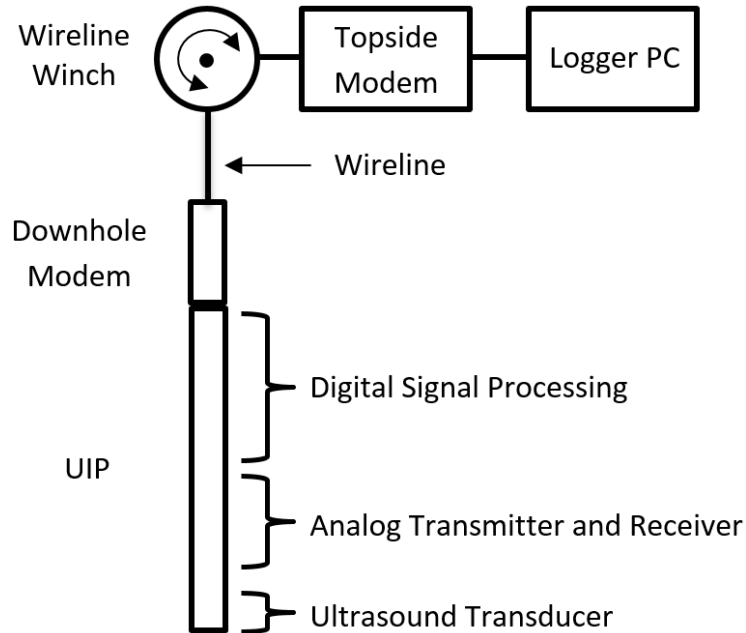


Figure 1.4: Block schematic of complete system for using UIP.

UIP is the second generation ultrasound imaging tool and is currently being field tested. To increase the number of imageable wells, the outer diameter has been reduced from 76 mm to 54 mm. The maximum operating temperature is increased from 105 °C to 150 °C, and it is a goal to increase it further to 180 °C in the near future.

A block schematic including all parts needed to capture ultrasound images with the UIP is shown in Figure 1.4.

UIP also offers the ability to take high precision measurements in all three dimensions, including measurement of the wall thickness. The measurements can be used to check if critical components are within acceptable tolerances and can be compared with earlier measurements to predict future durability.

Right now the maximum transmit frequency for full output signal is 2 MHz, which inhibits realizing the full potential of the transducers that have higher upper frequency limits. This results in reduced resolution in both the lateral direction (perpendicular to the ultrasound beam), shown in Figure 1.6 and the axial resolution (parallel to the ultrasound beam) shown in Figure 1.7.

This thesis will document the process of improving the upper frequency to 6 MHz while still satisfying all other requirements. To understand the link between resolution and frequency, a little basic ultrasound theory is presented.

Ultrasound imaging is based on transmitting an ultrasound wave and recording the time it takes to travel from the source to the wall where it is reflected, and back

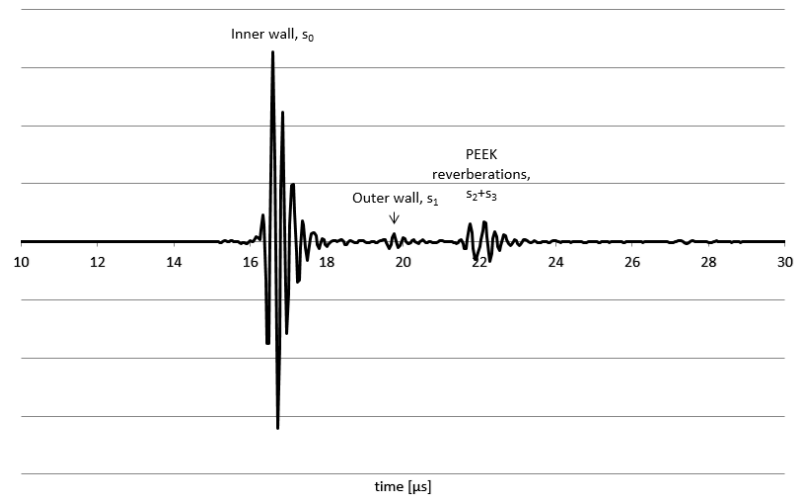


Figure 1.5: Thickness measurement trace showing importance of pulse duration.

to the source again. By knowing the speed of sound in the medium where the sound wave travels, it is possible to calculate the distance traveled. An example of a received signal is shown in Figure 1.5.

If the pulse duration is too long, the two first echoes will overlap each other making it hard to detect the outer wall, and thus the wall thickness. The pulse duration therefore limits the minimum measurable wall thickness, as shown in Figure 1.6.

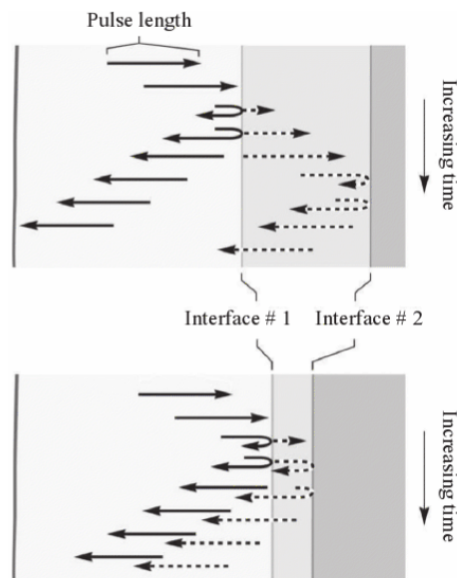


Figure 1.6: Axial resolution and pulse length. In the upper figure, echoes do not overlap and can be resolved. In the lower figure, the surfaces are closer than half a wavelength, and can therefore not be resolved[29].

The lens thickness limits the maximum measurable wall thickness by causing the third echo seen in the trace, but this is not discussed in this thesis. The lens is needed to protect the transducers from high pressure, and the echo has a high amplitude because of the large difference in acoustic impedance between the lens and the well fluid.

Shorter pulses result in higher precision in thickness measurements where the axial resolution is important. The axial resolution is the minimum distance between two objects along the ultrasound beam needed to be able to separate them. The formula for calculating axial resolution is shown in (1.1) [20, p. 163].

$$\text{Axial resolution} = \frac{1}{2}p_d c \quad (1.1)$$

Where p_d is the pulse duration calculated in (1.2).

$$p_d = \frac{1}{BW} \quad (1.2)$$

BW in (1.2) is the bandwidth of the signal, limited by the frequency response of the complete UIP, including both transmitter and transducer. The frequency response of the electrical circuit should be so good that the only thing limiting the system bandwidth is the transducer. To achieve this the maximum electrical signal reduction at the upper frequency of the transducer should be less than a tenth of the reduction caused by the transducer. The upper frequency of the transducer is defined as the point where the amplitude is reduced to the half of maximum amplitude, a reduction of 6 dB. The amplitude reduction of the original transmitter is measured to 18 dB at a frequency of 6 MHz.

The lateral resolution is the minimum distance needed between two objects perpendicular to the ultrasound beam to be able to separate them. It is inversely proportional to the signal frequency, as shown in (1.3) [20, p. 164]. D is the diameter of the transducer, while F is the distance from focal point to the face of the transducer. F is called the focal distance. c is the speed of sound in the medium.

$$\text{Lateral resolution} = \frac{\lambda F}{D} = \frac{cF}{fD} \quad (1.3)$$

1.3 About This Work

BTC has identified the transmitter circuit as the main part limiting the frequency response of the UIP. The transmitter has been developed by a subcontractor for BTC. My task has been to improve the frequency response of the transmitter circuit for temperatures up to 180 °C.

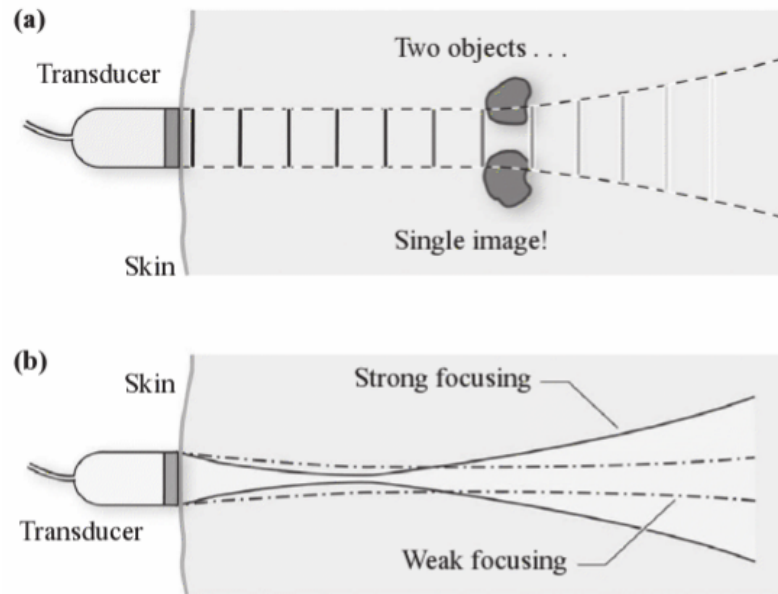


Figure 1.7: Lateral resolution. (a) Lateral resolution without focusing is no better than transducer dimensions. (b) Two representations of reducing the cross-sectional area of the beam by focusing [29].

In Chapter 2, the original transmitter design is analyzed, starting with a characterization of the load it has to drive. By characterizing the load, requirements can be set up for the output stage of the transmitter. The chapter continues like this by analyzing one block at a time, possibly improving the block and setting up requirements for the next block. The chapter ends with a new design schematic for the transmitter, including all component changes.

To save time and money, the new design is only implemented for one of the 16 channels on the transmitter board. This process is documented in Chapter 3, where I started with the original printed circuit board (PCB) layout done by the subcontractor. I did a new layout for one of the channels, implementing the new design with the existing power planes and shared circuitry. The total area used per channel is the same as in the original design and the layout can easily be copied for the other 15 channels.

I soldered on components for the new design channel, as well as one channel with the old design and the shared circuitry. The toroidal ferrite cores were obtained as samples from Magnetics and wound by hand.

Chapter 4 starts with mentioning the tests performed by the subcontractor before the thesis. It then proceeds with all the testing done by me in the process of arriving at a complete working design. This includes characterization and verification of component functionality, as well as tests performed on the complete new design.

Design Analysis

Before designing the original transmitter, some important requirements were defined as listed below. The maximum output amplitude is set equal to the maximum supply voltage from the power supply unit. This is not a requirement that has to be exceeded, but is rather a limit for when other parameters should be prioritized.

- Operational temperature: 0 °C to 180 °C
- Bandwidth: 2 MHz to 6 MHz
- Output Amplitude: ± 100 V
- Supply Voltages: ± 5 V and ± 100 V

After the design and manufacturing of the original transmitter, the performance was tested and compared to the specifications. Tests documented in section 4.5 shows that the upper frequency for a maximum output signal is only 2 MHz for the original transmitter. This is the main motivation for improving the design.

The original design is split into smaller parts and analyzed according to the specifications. The design parts and external connections are analyzed starting at the load and ending at the input signal. After analyzing each part, improvements are considered and implemented. All implemented improvements are taken into consideration when analyzing the next part.

A complete schematic of the original transmitter is shown in Figure 2.1.

The complete tool is made to fit oil wells with an inner diameter down to 54 mm. The transmitter board is stacked together with two other boards as shown in Figure 2.2. On the bottom side of the board, the maximum component height is limited by

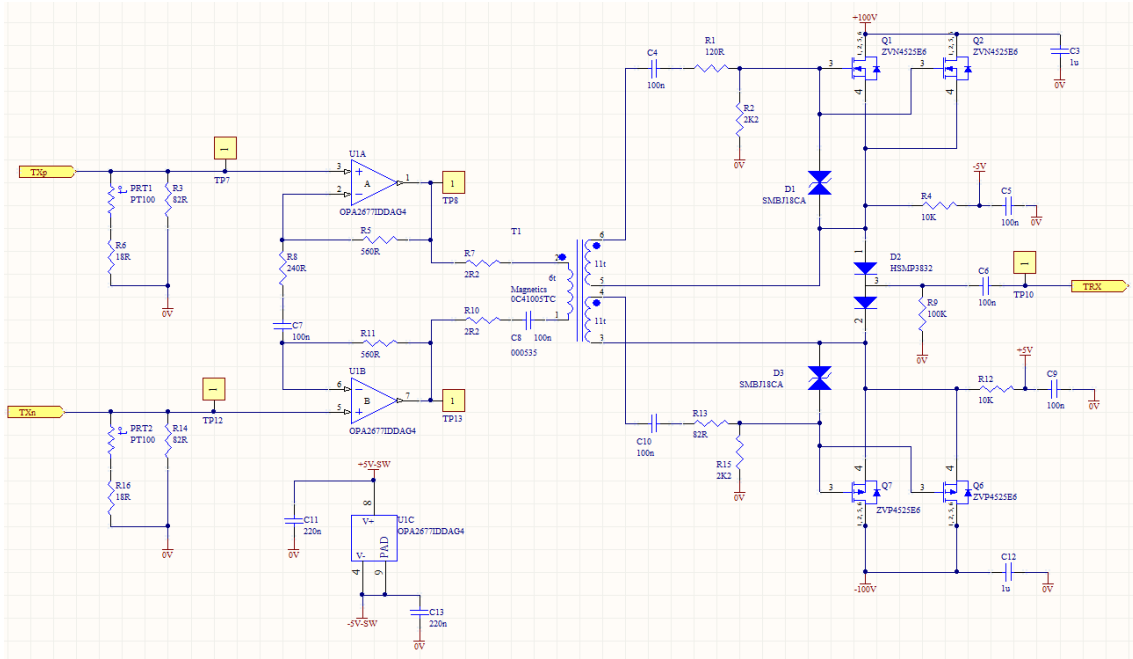


Figure 2.1: Schematic of the original transmitter.

the distance to components on the middle board. Maximum component height on the middle board in the position of the channels is 1.6 mm. The distance between the boards is 6 mm, resulting in a maximum available component height of 4.4 mm, minus a margin for uncertainties.

Each transmit channel currently occupies an area of 5.8 cm^2 on the PCB. There is almost no free space in each channel. In case some components need more space after replacement, others need to be downsized.

2.1 Transmitter Load

Each transmitter will be connected to two transducer elements at a time through a switch board. BTC currently use 4 different ultrasound transducers which differ in center frequency, bandwidth and number of elements. The complex impedance of these has been measured as a function of frequency by the manufacturer, as shown in Table 2.1. Dummy transducers for testing are made of a resistor and a capacitor in series, which model the transducers at the center frequency.

Each of the 16 channel outputs can be connected to a total of 288 output connection points. This allows for connecting a maximum amount of 288 transducer elements. To achieve this a total of 800 switches are used. Each transmitter is connected to 32 switches which are connected to 32 common connection points for all transmitters, called $X[0..31]$.

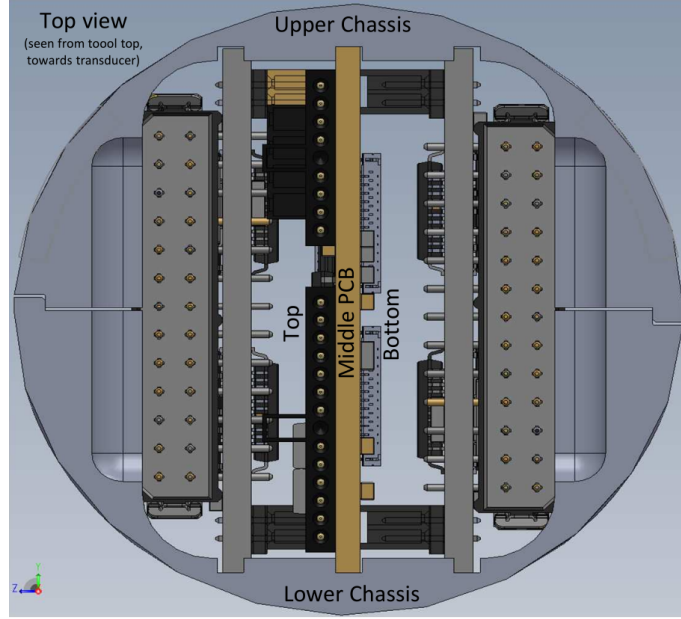


Figure 2.2: Inner mechanics of the UIP tool [3].

The 32 common connection points are each connected to 9 switches connected to separate transducers. In this way each of the connection points can be connected to 9 different transducers. Multiplying this with the number of connection points, 32, each transmitter can be connected to 288 different transducers.

An open switch is modeled as a capacitor to ground. The capacitance for each open switch is typically 12 pF at 1 MHz [21]. A model for a single closed switch is shown in Figure 2.3.

The second stage of switches also includes bleed resistors to discharge the capacitance in between two switches when both switches are open. These bleed resistors exist on each side of the switch in both open and closed state. A model of the switch with bleed resistors in closed state is shown in Figure 2.4.

By using these two models it is possible to create a model for the impedance at each transmitter output when connected to two transducers, shown in Figure 2.5. The first node consists of 30 open switches and two closed switches in parallel, as the

Table 2.1: Transducer data measured by manufacturer Imasonic.

Transducer	f_c [MHz]	Z _r	Z _i	R [Ω]	C [pF]
6071A101	3.10	60.7	-291.4	60.7	176
9887B101	4.00	27.6	-150	27.6	265
R5813B101	3.60	109	-420.6	109	105
4475A101	4.76	26.0	-152.3	26.0	220

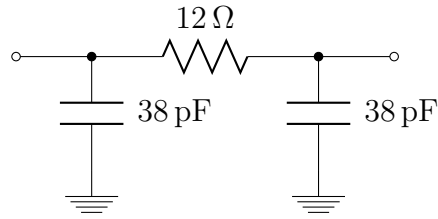


Figure 2.3: Model for closed switch.

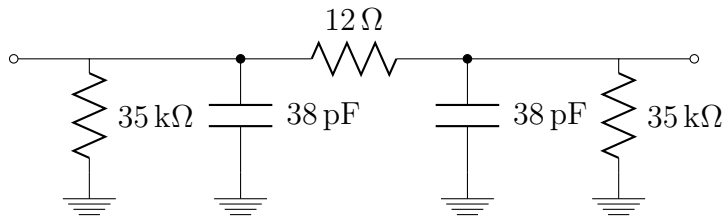


Figure 2.4: Model for closed switch with bleed resistors.

transmitter is connected to two of 32 connection points.

The nodes X_a and X_b show the impedance at each connection point. Each connection point can be connected to 16 transmitters and nine transducers, a total of 25 switches. When connecting one transmitter to two transducers, this equals 23 open switches and 2 closed switches in parallel. The nine switches on the transducer side also include bleed resistors. The nodes S_c and S_d represent connection points for transducers.

In addition to the impedance of the switches, the PCB tracks will introduce series resistance and inductance, as well as capacitance and resistance to ground.

The 9887B101 transducer used for thickness measurements has the highest upper frequency of the transducers in use by BTC. Imaging done with this transducer will theoretically receive the greatest improvements in resolution by improving the electrical frequency response. It has the highest capacitance value and will result in the highest current requirement in calculations. This makes it natural to use its impedance values in all calculations.

2.1.1 Possible Improvements on Transmitter Load

The two switch circuits HV2601 and HV2701 can be replaced with HV2605 and HV2705 from the same manufacturer. These switches have 17% lower capacitance when open and 66% lower capacitance when closed. A replacement will reduce the total switch capacitance seen by the transmitter circuit by 29%.

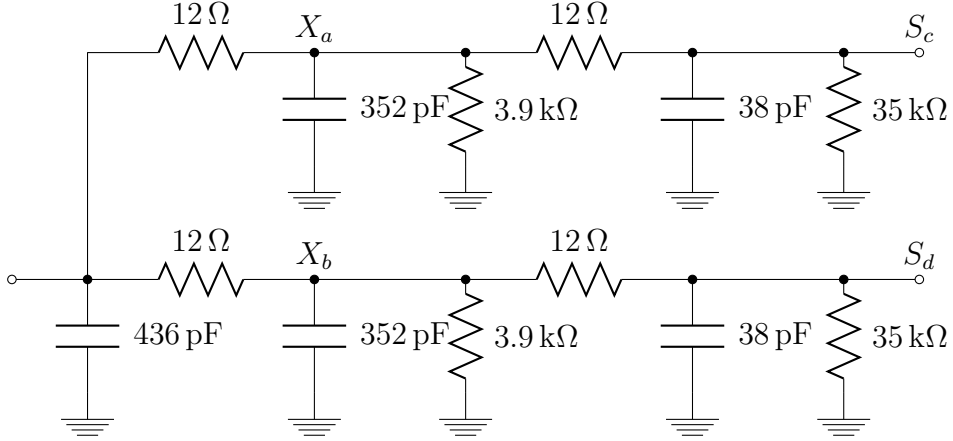


Figure 2.5: Model for switch circuit, 1 channel. S_c and S_d is connection points for the two transducer elements.

The switches are placed on a separate circuit board and will require a revision of the design before ordering a new batch. The board also needs to be tested separately to verify functionality up to 180 °C. The replacement is treated as a possible future improvement, but not used in calculations as it is not guaranteed to work in the specified operating conditions. The capacitance value of the original switches will be used in all calculations.

2.2 Output Stage

The transmitter is specified to output sinusoidal signals with a peak-to-peak amplitude up to 200 V_{pp} and frequency up to 6 MHz.

The maximum rate of voltage change of a sinusoidal signal occurs when crossing the offset level. This gives the following slew rate requirement:

$$SR = \left. \frac{dV_o}{dt} \right|_{max} = \omega \hat{V}_i = 3770 \text{ V}/\mu\text{s}$$

Slew rate is the maximum voltage change per unit of time in a node of a circuit. The slew rate is limited by maximum current sink or source, as well as the impedance of the node. The voltage change of a capacitor is shown in (2.1). Resistance in parallel with the capacitor will reduce the amount of current to the capacitor and thus reduce the slew rate.

$$\frac{dV_c}{dt} = \frac{I_c}{C} \quad (2.1)$$

The output node capacitance will be dominated by the switches and transducer

elements. For simplicity when calculating the current requirement of the output transistors, resistances are ignored. The output node capacitance is calculated in (2.2), based on the models proposed in section 2.1.

$$C_L = 436 \text{ pF} + 2(352 \text{ pF} + 38 \text{ pF} + 270 \text{ pF}) = 1.76 \text{ nF} \quad (2.2)$$

The output capacitance of each output transistor will also add to this sum, but has to be considered after finding a transistor with a satisfying drain current specification. This gives the following current requirement for each of the output transistors, before considering the output capacitances $C_{ds-pmos}$ and $C_{ds-nmos}$:

$$I_{max} = SR \times C_L = 6.62 \text{ A} \quad (2.3)$$

The original output stage is able to source 1.8 A at 150 °C and $V_{GS} = 10 \text{ V}$, and sink 1.0 A at 150 °C and $V_{GS} = -10 \text{ V}$. This is much lower than the calculated current requirement and will cause slew rate limitations.

2.2.1 Improvements Needed for Output Stage

The ideal requirements for new output transistors is listed below. The most important requirement is listed output current and drain-source breakdown voltage, while the limit for total package area can be increased by exchanging other components on the board. The minimum drain-source breakdown voltage for each transistor needs to exceed the nominal rail-to-rail voltage at 200 V to account for variations. The breakdown voltage has a positive temperature coefficient, which needs to be considered for low temperatures. A stated maximum junction temperature of 150 °C is common for most transistors and can be tolerated, but requires reliability testing.

- Operational temperature: 0 °C to 180 °C
- Output current: 6.6 A at $|V_{GS}| = 10 \text{ V}$
- Drain-source breakdown voltage: $>200 \text{ V}$
- Total package area: $<4 \text{ cm}^2$

In addition to be able to drive the load without any slew rate limitations, the output transistors should be easy to drive. This includes being able to deliver the specified current with low input voltage and low gate to source capacitance. The load capacitance seen from the transformer only consist of gate to source capacitance C_{GS} , as the gate to drain capacitance C_{GD} is isolated by a series resistor of 10 k Ω . The

maximum current requirement to drive one of the output transistors is calculated in (2.4).

$$I_{in} = \omega \hat{V}_{S_x} C_{GS} \quad (2.4)$$

The resulting current requirement for the primary side of the transformer is dependent on the transformer configuration and calculated in (2.5). This should be as low as possible to be able to find a suitable operational amplifier.

$$I_P = \frac{I_{S_n} V_{S_n} + I_{S_p} V_{S_p}}{V_P} \quad (2.5)$$

Two transistors which meet these requirements are FQD6N25 and FQD4P25, both from Fairchild Semiconductor. They have a maximum drain-source voltage of 250 V with temperature coefficients of 0.19 V/°C and -0.21 V/°C. They are both in a surface mounted TO-252 package measuring a maximum of 7.0 cm². This makes it necessary to reduce the area of other components by a total of 10 cm² if the board size is to be held constant. The typical input capacitance is 230 pF for FQD6N25, and 325 pF for FQD4P25.

FQD4P25 has the highest voltage requirement of $V_{GS_{max}} = 9.2$ V for delivering a current of 6.6 A at a temperature of 150 °C. The maximum current requirement of the FQD6N25 and FQD4P25 gate node is calculated in (2.6) and 2.7, respectively. Maximum C_{iss} and C_{rss} ¹ capacitance values from the datasheets are used, as well as a typical bias voltage of 4 V.

$$I_{in-max-n} = \omega \hat{V} C_{GS_{max}} = 2\pi \times 6 \text{ MHz} \times (8.1 \text{ V} - 4 \text{ V}) \times 290 \text{ pF} = 44.8 \text{ mA} \quad (2.6)$$

$$I_{in-max-p} = \omega \hat{V} C_{GS_{max}} = 2\pi \times 6 \text{ MHz} \times (9.2 \text{ V} - 4 \text{ V}) \times 407 \text{ pF} = 79.7 \text{ mA} \quad (2.7)$$

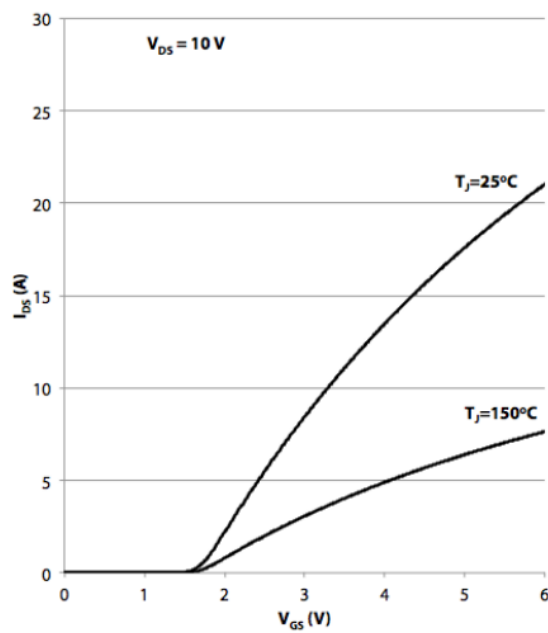
Gallium Nitride (GaN) and Silicon Carbide (SiC) transistors were also considered for use as output transistors. Both types are only commercially available as n-type transistors, which inhibits the use of the current bias circuit. A new bias circuit for an output stage with two n-type transistors, low transition distortion and low bias current has not been found. To achieve this, the gate to source voltage needs to fall with increased I_{ds} , stabilizing at a low bias current and V_{gs} close to the threshold voltage. The best transistor alternatives are still listed in Table 2.2 with relevant parameters. The V_{gs} values listed are the needed voltage to conduct a current of 6.6 A.

The GaN transistor stands out as the best alternative, but shows a strong temperature dependency in its forward transconductance. This dependency is shown in Figure 2.6.

¹ $C_{iss} = C_{gd} + C_{gs}$, $C_{rss} = C_{gd}$ [25]

Table 2.2: Comparison of transistor technologies.

Name	Technology	A [mm ²]	C_{iss} [pF]	$V_{gs} _{T=150\text{ }^\circ\text{C}}$	$V_{gs} _{T=25\text{ }^\circ\text{C}}$	$R_{\theta JA}$
FQD6N25	Si	70	230	8.1	7.5	110
GS66502B	GaN	32	64	6.0	3.0	31
C3M0280090J	SiC	176	150	6.5	7.0	40

Figure 2.6: I_{DS} as a function of V_{GS} for GS66502B [6].

FQD6N25 and FQD4P25 is chosen as new output transistors. This keeps the bias current at a low level by enabling use of the original bias circuit. These transistors have a maximum junction temperature of 150 °C requiring reliability testing.

2.2.2 Thermal Considerations for Output Transistors

The output transistors need to be able to source and sink the current requirement calculated in section 2.2. The maximum power dissipation in each transistor is limited by the maximum junction temperature $T_{jmax} = 150\text{ °C}$. The junction temperature depends on the temperature of the mounting base, T_{mb} and thermal resistance between junction and mounting base, R_{thj-mb} , shown in (2.8).

$$P_{totmax} = \frac{\Delta T_{j-mbmax}}{R_{thj-mb}} \quad (2.8)$$

Dissipated power in the output transistors consists of static power caused by bias current and dynamic power from switching the load. The gate-source voltage of each transistor stabilizes at the threshold voltage of 4 V. This results in a potential of 1 V over the 10 kΩ resistors and a bias current of 0.1 mA. The static power per transistor is calculated in (2.9).

$$P_{static} = V_{DS}I_{bias} = 104\text{ V} \times 0.1\text{ mA} = 10\text{ mW} \quad (2.9)$$

When temperature increases, the bias current at a given gate-source voltage will increase. As the gate-source bias voltage is inversely proportional to the drain-source bias current, the change in bias current is negligible.

When the capacitive load is switched between the supplies, only one of the output transistors is conducting at a time. This also means that only one of the supplies is delivering energy per half period. The energy delivered from the supply during one half period when the NMOS is on and the load is switched from V_{SS} to V_{DD} is calculated in (2.10). As the supplies are symmetrical, the same amount of energy will be supplied during the other half period when the PMOS is on and the load is switched from V_{DD} to V_{SS} .

$$\begin{aligned} E &= \int_0^\infty I(t)V_{DD}dt = \int_0^\infty C \frac{dV}{dt} V_{DD}dt \\ &= C(V_{DD} - V_{SS}) \int_{V_{SS}}^{V_{DD}} dV = CV_{DD}(V_{DD} - V_{SS}) \end{aligned} \quad (2.10)$$

The above equation calculates the dissipated energy in each transistor per period. If the load switches continuously at a frequency, f_{sw} , over a time interval T , the load has been switched Tf_{sw} times. Approximately all the energy delivered by the

supplies will be dissipated as heat in the output transistors. The dissipated power per transistor with continuous switching is calculated in 2.11.

$$P_{switching} = \frac{E}{T} = \frac{T f_{sw} C V_{DD} (V_{DD} - V_{SS})}{T} = f_{sw} C V_{DD} (V_{DD} - V_{SS}) \quad (2.11)$$

When the load is not switched continuously, but has a certain activity factor, the average dissipated power can be calculated in (2.12).

$$P_{switching} = \alpha f_{sw} C V_{DD} (V_{DD} - V_{SS}) \quad (2.12)$$

Activity factor is calculated in (2.13).

$$\alpha = \frac{n_{pulse} T_{pulse}}{T_{ping}} = \frac{n_{pulse}}{f_{pulse} T_{ping}} \quad (2.13)$$

The pulse frequency is the same as the switching frequency and thus cancels in the power equation. The ping period is the time between two subsequent pings. Ping period is calculated in (2.14) with 10 frames/s and 288 pings/frame.

$$T_{ping} = T_{frame} \frac{n_{frame}}{n_{ping}} = 0.1 \text{ s} \times \frac{1}{288} = 347 \text{ } \mu\text{s} \quad (2.14)$$

By including the activity factor, the switching frequency has no influence on the average dissipated effect. The resulting maximum average power dissipation per output transistor is calculated in (2.15) with a maximum number of 16 pulses.

$$\begin{aligned} P_{switching} &= \frac{n_{pulse}}{T_{ping}} C V_{DD} (V_{DD} - V_{SS}) \\ &= \frac{16}{347 \text{ } \mu\text{s}} \times 1.8 \text{ nF} \times 100 \text{ V} [100 \text{ V} - (-100 \text{ V})] = 1.7 \text{ W} \end{aligned} \quad (2.15)$$

The maximum temperature increase when using the minimum pad and copper thickness of 70 μm is calculated in (2.16).

$$\Delta T_{JA_{max}} = P_{tot_{max}} \times R_{\theta_{JA}} = 1.7 \text{ W} \times 110 \text{ }^\circ\text{C/W} = 183 \text{ }^\circ\text{C} \quad (2.16)$$

The thermal resistance used in the above equation is from junction to ambient with no heat sink attached. If an ideal heat sink is assumed, the thermal resistance is specified as $R_{\theta_{JC}} = 2.78 \text{ }^\circ\text{C/W}$. Maximum temperature assuming an ideal heat sink is calculated below.

$$\Delta T_{JC_{max}} = P_{tot_{max}} \times R_{\theta_{JC}} = 1.7 \text{ W} \times 2.78 \text{ }^\circ\text{C/W} = 4.6 \text{ }^\circ\text{C} \quad (2.17)$$

As can be seen from the two equations above, the output transistors are dependent on an effective heat sink to operate in high temperature. As the temperature rise is directly proportional to the activity factor, a limitation of pulses and/or frame rate is a possibility to increase maximum operational temperature.

Thermal resistance from junction to mounting base can be reduced from $110\text{ }^\circ\text{C/W}$ to $50\text{ }^\circ\text{C/W}$ by increasing the pad area to 6.5 cm^2 , but this is not possible with the board area constraints existing today. By replacing the transistor with a TO-263 package, the thermal resistance can be reduced to $62.5\text{ }^\circ\text{C/W}$. This will increase the pad area to 1.7 cm^2 , which would be hard to fit on the current board size. These alternatives will be considered based on results from testing.

2.3 Transformer

Increasing the size of the output transistors creates a need for reducing the size of other components on the board. As the transformer used in the original transmitter design is the largest component on the board, the possibilities for replacing it with a smaller transformer has been evaluated. The major drawback when reducing core size is the increased temperature rise for a given power dissipation. This is thoroughly calculated in this section, and a new core has been chosen.

The new core used for the transformer in the new transmitter is produced by Magnetics, type 0C40502TC, with an inductance per square turn of $A_L = 129\text{ nH} \pm 25\%$ [15]. This core is a replacement for 0C41005TC, reducing the transformer area by 112 mm^2 . This gives enough area to place the new output transistors and keep the board size constant. Several other toroidal ferrite cores of the same size were considered, but 0C40502TC had the flattest frequency and temperature response, shown in Figure 2.7.

The relative permeability, μ_r , of the core material, type C, is $900 \pm 25\%$. It is shown as a function of frequency and temperature in Figure 2.7. The Curie temperature is $200\text{ }^\circ\text{C}$ and the maximum usable frequency, defined at a 50% roll-off is 8 MHz.

2.3.1 Core Saturation

The saturation flux density for a ferrite core with type C material is 380 mT. Saturation flux density declines for all ferrites when the temperature increases[17], as shown in Figure 2.8. Magnetics does not provide information about flux density as a function of temperature for type C material, only for type R and type J material. All three materials consist of Iron (Fe), Manganese (Mn) and Zinc (Zn), and as the two graphs are very similar, it is assumed that type C material also show a similar behavior.

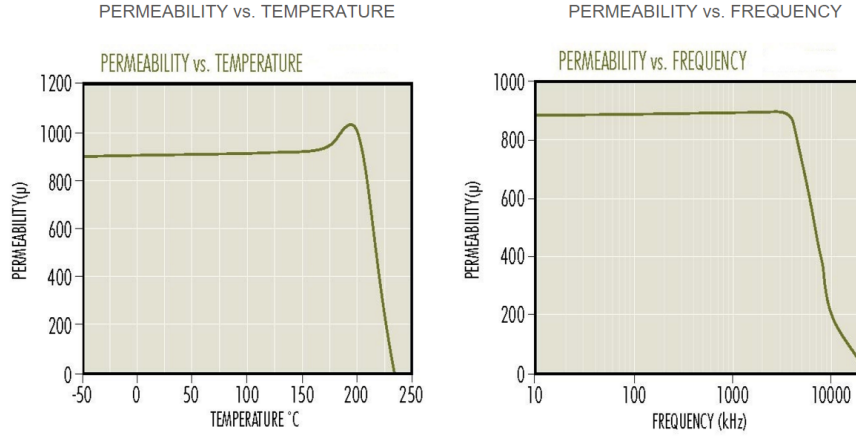


Figure 2.7: Permeability as a function of temperature and frequency [14].

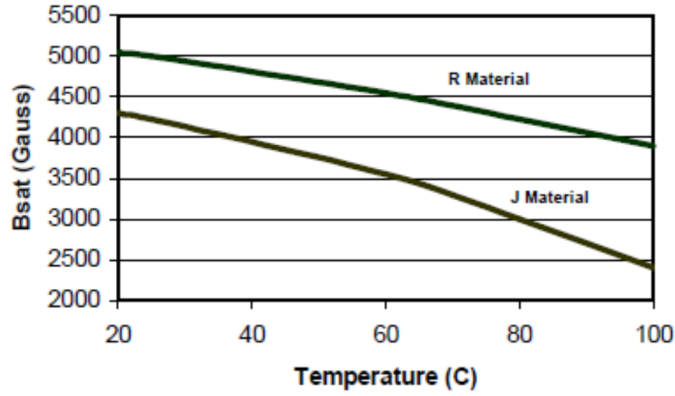


Figure 2.8: Saturation flux as a function of temperature [17].

The behavior of type C material is believed to be closest to type R as their Curie temperatures only differ by 10 °C, and the type J material has a Curie temperature 55 °C lower than type C. Type R shows a reduction of 22 % during a temperature increase from 20 °C to 100 °C. The relationship is approximately linear and by linear extrapolation, the reduction will be 50 % at 200 °C.

To calculate the maximum flux density, the maximum voltage at the primary winding in the original transmitter circuit is calculated in (2.19). The apparent load impedance is calculated in (2.18).

$$\begin{aligned}
 Z'_L &= \left(\frac{N_P}{N_{S_n}}\right)^2 Z_{L_n} \parallel \left(\frac{N_P}{N_{S_p}}\right)^2 Z_{L_p} \\
 &= \left(\frac{6}{11}\right)^2 \left(120 \Omega + \frac{1}{s72 \text{ pF}}\right) \parallel \left(\frac{6}{11}\right)^2 \left(82 \Omega + \frac{1}{s73 \text{ pF}}\right) \\
 &= (35.7 - j329) \parallel (24.4 - j324) = 15.0 - j163
 \end{aligned} \tag{2.18}$$

$$V_P = V_O \frac{Z'_L}{Z'_L + 2R_S} = 5.67 \text{ V} \frac{15.0 - j163}{15.0 - j163 + 2.2 + 2.2 - j0.8} = 5.63 \text{ V} \angle -0.1^\circ \quad (2.19)$$

The minimum number of primary windings needed to avoid saturating the core is calculated in (2.20), using the calculated maximum primary voltage of 5.63 V. As flux density is inversely proportional to frequency, a minimum frequency of 2 MHz is used. The equation is derived from (2.38) and shows that a minimum number of three primary windings is advised at the given conditions.

$$N_{1_{min}} = \frac{V_{1_{rms}}}{4.44 f_{min} B_{sat} A_c} = \frac{5.63 \text{ V} \times \frac{1}{\sqrt{2}}}{4.44 \times 2 \text{ MHz} \times 190 \text{ mT} \times 1.05 \times 10^{-6} \text{ m}^2} = 2.2 \quad (2.20)$$

2.3.2 Asymmetrical Drive of the Output Transistors

The two new output transistors have different input voltage requirements to deliver the same output current. This suggests an asymmetrical drive done by different winding number in the transformer. The voltage requirement to deliver 6.6 A of output current at 150 °C is 8.1 V and 9.2 V, which gives the following winding ratio with a typical bias voltage of 4 V:

$$\frac{N_{SP}}{N_{SN}} = \frac{V_{GS_P}}{V_{GS_N}} = \frac{9.2 \text{ V} - 4 \text{ V}}{8.1 \text{ V} - 4 \text{ V}} = 1.27 \quad (2.21)$$

Different winding ratios are tested and documented in subsection 4.2.2. Chosen winding ratios are 4/2 for NMOS secondary winding and 5/2 for the PMOS secondary winding.

The maximum current requirement at the secondary windings is calculated in (2.6) and (2.7). As the primary winding current, I_P , is given by winding ratio and the current in secondary windings, the resulting operational amplifier output current requirement is calculated in (2.22). A specific number of windings will be chosen after considering losses.

$$I_P = \frac{I_{S_n} N_{S_n} + I_{S_p} N_{S_p}}{N_P} = \frac{45 \text{ mA} \times 4 + 80 \text{ mA} \times 5}{2} = 290 \text{ mA} \quad (2.22)$$

2.3.3 Thermal Considerations for Transformer

As already mentioned, reducing the core size reduces the maximum allowed power dissipation at a given temperature. This is calculated in (2.23), derived from (A.1) in Appendix B. Maximum temperature of the ferrite core is limited by the Curie

temperature at 200 °C. The maximum ambient temperature is listed in the specifications as 180 °C, resulting in a maximum allowed temperature increase of 20 °C.

$$P_L[\text{mW}] = A_S[\text{cm}^2]\Delta T^{1.2}[^\circ\text{C}] = 0.334 \text{ cm}^2 \times 20^{1.2} \text{ }^\circ\text{C} = 12 \text{ mW} \quad (2.23)$$

The surface area of the transformer is calculated in (2.24).

$$A_S = 2\pi r_e \times l_e = 2\pi \times 0.578 \text{ mm} \times 9.21 \text{ mm} = 3.34 \times 10^{-5} \text{ m}^2 = 0.334 \text{ cm}^2 \quad (2.24)$$

Where r_e is the effective radius of a structure with uniform cross section equivalent to the 0C40502TC core, calculated in (2.25). A_e is the effective cross sectional area and l_e is the effective magnetic path length from the datasheet [16].

$$r_e = \sqrt{\frac{A_e}{\pi}} = \sqrt{\frac{1.05 \times 10^{-6} \text{ m}^2}{\pi}} = 5.78 \times 10^{-4} \text{ m} \quad (2.25)$$

The dissipated power in a transformer consists of copper loss and core loss, which both depend on the number of windings in the transformer. Copper loss increases with increased number of windings, while core loss decreases. To determine a suitable number of windings, both copper loss and core loss is calculated during the two next sections.

Copper Loss

Copper loss exists due to the inevitable resistance in the transformer windings. When current passes through the windings, this will contribute to a loss of power in the circuit. Total copper loss is shown in (2.26), including both DC resistance and factors for AC effects increasing the resistance as frequency increases. The skin effect factor, K_s , and proximity effect factor, K_p , is explained in section A.1 and A.2.

$$P_{Cu} = I_{RMS}^2 R_{DC} K_s K_p \quad (2.26)$$

To calculate the maximum transformer current, the apparent load impedance at 6 MHz is calculated in (2.27), using (2.18). Winding ratios are calculated in subsection 2.3.2, while isolation resistances are calculated in subsection 2.4.1.

$$\begin{aligned} Z'_L &= \left(\frac{1}{2}\right)^2 \left(30 \Omega + \frac{1}{s223 \text{ pF}}\right) \parallel \left(\frac{2}{5}\right)^2 \left(36 \Omega + \frac{1}{s315 \text{ pF}}\right) \\ &= (7.5 - j23) \parallel (5.8 - j10) = 3.4 - j7.2 \end{aligned} \quad (2.27)$$

The resulting maximum primary winding current is calculated in (2.28).

$$\begin{aligned} I_{O_{max}}|_{f=6\text{MHz}} &= \frac{V_P}{Z'_L} = \frac{V_O}{Z'_L + 2R_S} \\ &= \frac{5.67\text{V}}{(3.4 - j7.2)\Omega + 2 \times 2.2\Omega} = 532\text{mA}/43^\circ \end{aligned} \quad (2.28)$$

The relationship between primary and secondary current in a transformer with two secondary windings is shown in (2.29).

$$I_P = \frac{I_{S_n} N_{S_n} + I_{S_p} N_{S_p}}{N_P} \quad (2.29)$$

And from that the average secondary winding current with winding ratios of $\frac{N_{S_n}}{N_P} = 2$ and $\frac{N_{S_p}}{N_P} = 2.5$.

$$I_{S_{avg}} = \frac{I_{S_n} + I_{S_p}}{2} = \frac{I_P \frac{N_P}{N_{S_n}} + I_P \frac{N_P}{N_{S_p}}}{2} = 0.45 I_P = 239\text{mA}/43^\circ \quad (2.30)$$

The windings are made of copper which have a resistivity of $\rho = 1.7 \times 10^{-8} \Omega \cdot \text{m}$ [19] at 20 °C. This resistivity has a temperature coefficient of $\alpha = 3.9 \times 10^{-3}/^\circ\text{C}$ [19], leading to increased loss at higher temperature. The resistivity of copper at the ferrite core Curie temperature of 200 °C is calculated in (2.31).

$$\rho_{200} = \rho_{20} \times [1 + \alpha(200^\circ\text{C} - 20^\circ\text{C})] = 2.9 \times 10^{-8} \Omega \cdot \text{m} \quad (2.31)$$

The conductivity of copper at the ferrite core Curie temperature of 200 °C is calculated in (2.32).

$$\sigma_{200} = \frac{1}{\rho_{200}} = 34.5\text{M}\Omega^{-1} \cdot \text{m}^{-1} \quad (2.32)$$

The DC resistance of the winding wires is shown in (2.33).

$$R_{DC} = \frac{l\rho}{A} = \frac{N \times MLT \times \rho}{\pi r_w^2} \quad (2.33)$$

Where N is the total number of turns and MLT is the mean length of each turn. The mean length of each turn depends on the diameter of both core and wire, and is shown in (2.34) for a one layer winding.

$$MLT = \pi(D_{core} + r_{wire}) \quad (2.34)$$

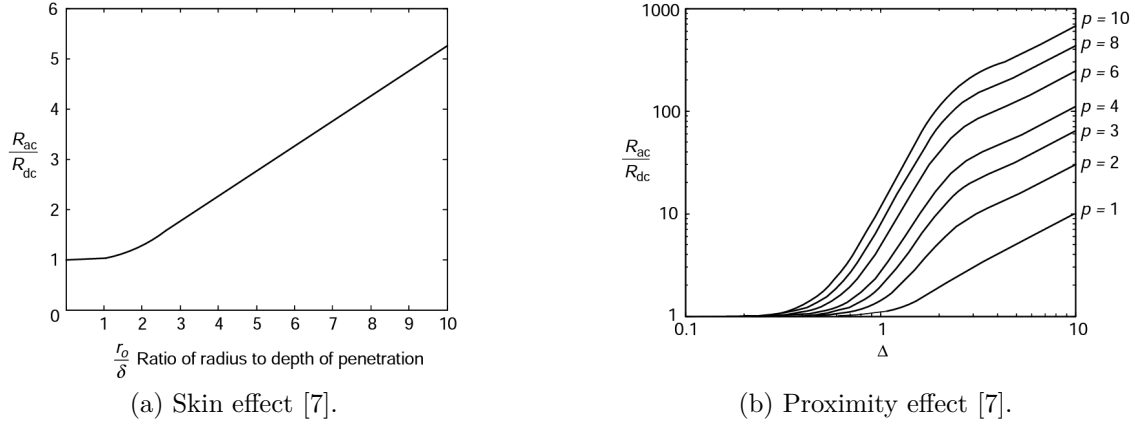


Figure 2.9: R_{ac}/R_{dc} due to high frequency effects.

Diameter of the core is calculated from the effective cross-sectional area, A_e , stated in the datasheet.

$$D_{core} = 2\sqrt{\frac{A_e}{\pi}} = 2\sqrt{\frac{1.05 \times 10^{-6} \text{ m}^2}{\pi}} = 1.16 \times 10^{-3} \text{ m} \quad (2.35)$$

When an isolated round conductor carries AC current, a concentric alternating magnetic field is created, which induces eddy currents in the conductor, canceling some of the current at the center of the conductor and increasing current near the surface. At high frequencies, the current flows in an equivalent annular cylinder with thickness δ , called the skin depth [7].

The skin effect factor, K_s , is the factor between the AC and DC resistance, due to skin effect. It is shown as a function of the ratio of wire radius to depth of penetration in 2.9a. Depth of penetration, also known as skin depth is calculated in (2.36) [7].

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad (2.36)$$

Proximity effect is similar to skin effect, but is caused by AC current carried by nearby conductors. The proximity effect factor, K_p , is the factor between the AC and DC resistance due to proximity effect. It is shown as a function of Δ in 2.9b. Δ is the ratio of equivalent layer thickness, d , to skin depth, δ_0 .

Total copper loss with winding ratios of $\frac{N_{S_n}}{N_P} = 2$ and $\frac{N_{S_p}}{N_P} = 2.5$ is shown as a function of the number of primary windings in Figure 2.10. Maximum current amplitudes of $I_P = 532 \text{ mA}$ and $I_{S_{avg}} = 239 \text{ mA}$ is used in the calculations, as well as a maximum temperature of 200°C .

The plot suggests a wire diameter of 0.16 mm to obtain the lowest possible copper loss when the number of primary windings is between 3 and 10. Copper wire with a

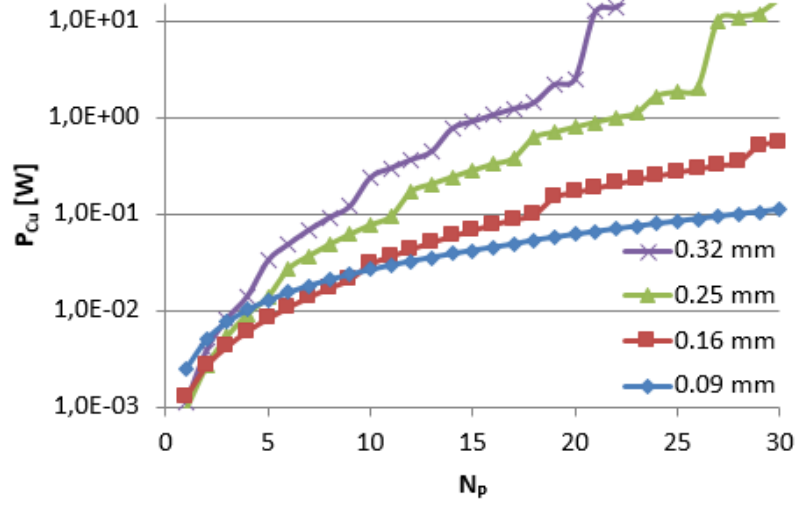


Figure 2.10: Calculated copper loss for different wire diameters as a function of primary windings.

diameter of 0.16 mm is the thinnest wire with a coating specified for 200 °C available in quantities less than 5 kg. Due to availability and low copper loss, a minimum wire diameter of 0.16 mm is selected.

A wire diameter of 0.09 mm will according to the plot lead to lower loss when the number of primary windings exceeds ten. Since proximity effect is calculated assuming no influence between primary and secondary windings, this is not certain. In a practical transformer, interleaving primary and secondary windings will cause partial cancellation of magnetic fields and decreased proximity losses [18, 163-164]. As proximity losses for a given number of windings is proportional to wire diameter, this will favor thicker wires and 0.16 mm will have the lowest loss up to a higher number of windings.

Core Loss

The total core loss has been calculated using the general Steinmetz equation [7] for core loss, shown in (2.37). Measurement of core loss and determination of the Steinmetz coefficients is shown in subsection 4.2.3.

$$P_{fe} = K_c f^\alpha B_{max}^\beta = 1.47 \times 10^{-13} \times f^{2.37} \times B^{2.79} \quad (2.37)$$

The maximum flux density is calculated using the transformer equation for sinusoidal excitation [7], shown in (2.38).

$$B_{max} = \frac{V_{1rms}}{4.44 f N_1 A_c} \quad (2.38)$$

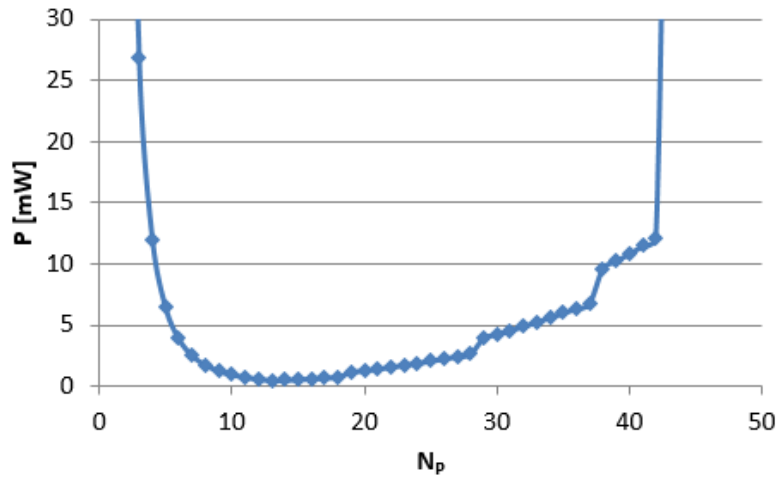


Figure 2.11: Calculated maximum total transformer loss as a function of primary windings.

With a fixed input voltage, $V_{1_{rms}}$, frequency, f , and core cross-sectional area, A_c , the number of primary windings, N_1 , will be the determining factor. A high number of primary windings will give a low flux density and thus a low core loss. Core loss and copper loss are oppositely dependent on the number of windings, resulting in a graph showing an optimal number of windings.

Measurement of core loss as a function of temperature is documented in subsection 4.2.3. This test shows a factor 2.1 increase in power loss when the temperature is increased from 23 °C to 200 °C. All calculations of transformer loss include this factor to account for worst case values.

Total transformer loss, including both copper and core loss is calculated for frequencies of 2 MHz and 6 MHz. The maximum value for each number of windings is plotted in Figure 2.11. The maximum number of 16 periods per ping is used in the calculations.

The plot suggests minimum loss to be with 14 primary windings, but all values between three and 47 are below the maximum power of 12 mW. Ten primary windings is chosen to be able to fit the windings when interleaving them. Choosing ten primary turns gives a theoretical power loss of 1.0 mW. With winding ratios of $\frac{N_{S_N}}{N_P} = 2$ and $\frac{N_{S_P}}{N_P} = 2.5$, the number of secondary turns is $N_{S_N} = 20$ and $N_{S_P} = 25$.

Temperature Increase

The maximum ambient temperature of the ferrite core is limited by its Curie temperature and temperature increase due to losses. The temperature increase is calculated

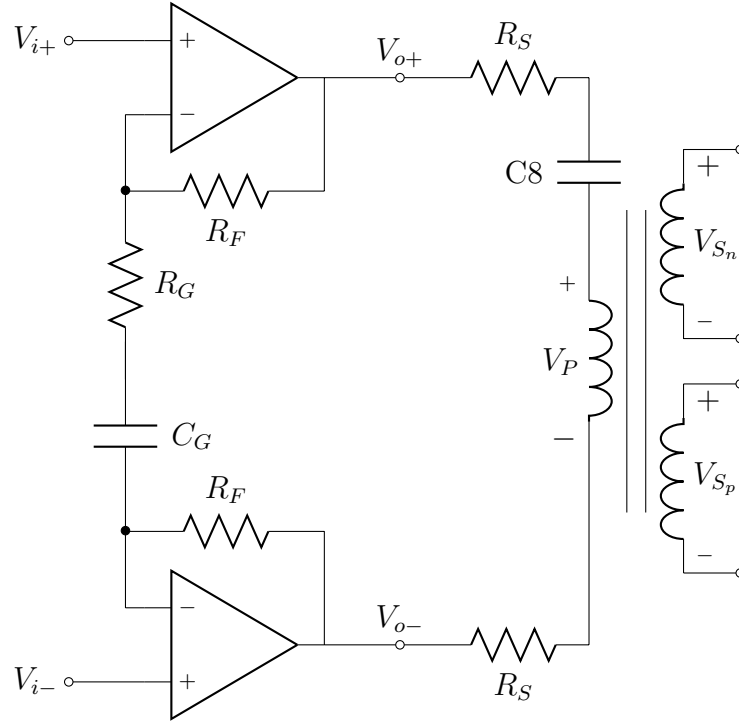


Figure 2.12: Differential amplifier circuit with transformer

in (2.39) using the empirical (A.1), provided by Magnetics Inc.

$$\Delta T = \left(\frac{1.0 \text{ mW}}{0.334 \text{ cm}^2} \right)^{0.833} = 2.5 \text{ }^\circ\text{C} \quad (2.39)$$

Ferrites can easily crack when exposed to rapid temperature changes, but a rate of change of $2 \text{ }^\circ\text{C}/\text{min}$ to $3 \text{ }^\circ\text{C}/\text{min}$ is regarded as safe [17]. Flow of hot air from other parts of the tool can cause rapid temperature change, and in order to protect the ferrite cores they are completely covered by a silicone adhesive, type 3145 from *Dow Corning*. This is also done to fasten the core to the board, reducing the possibility for wire breakage caused by mechanical vibrations.

2.4 Differential Amplifier

The dual operational amplifier OPA2677 in Figure 2.12 is used to amplify the differential input signal, calculated in (2.40). The capacitor C_G is used to limit the voltage amplification to 1 V/V at frequencies below $f = \frac{1}{2\pi R_G C_G} = 6.6 \text{ kHz}$.

$$A_v = 1 + 2 \frac{R_F}{R_G} = 5.67 \text{ V/V} \quad (2.40)$$

Table 2.3: List of considered operational amplifiers.

Name	T_{jmax} [°C]	Thermal Shutdown	I_{Omax} [mA]	Slew rate [V/μs]
Required	180	No	465	214
OPA2677	150	No	500	2000
OPA2673	150	Yes	700	3000
OPA820-HT	210	No	110	240

A high output current is important when driving a capacitive load. The minimum continuous output current of OPA2677 is 380 mA at 25 °C, and the peak output current is limited to 1.2 A sourcing and -1.6 A sinking. The rated output current decreases by approximately 10% when the temperature increases to 125 °C. Data is not available for 180 °C, as the maximum rated junction temperature is 150 °C.

Required slew rate is calculated in (2.41).

$$SR = \omega \hat{V}_o = 2\pi \times 6 \text{ MHz} \times 5.67 \text{ V} = 214 \text{ V}/\mu\text{s} \quad (2.41)$$

An attempt was done to find a new operational amplifier to replace the OPA2677, as its temperature range is specified to be -40 °C to 85 °C. Specifications the amplifier ideally should meet is listed in Table 2.3. In addition, the amplifier should be small, have a low thermal resistance and low quiescent current. No operational amplifier meet all requirements, but some of the best alternatives are listed below.

OPA820-HT has the highest output current of the amplifiers meeting the temperature specification, but a maximum output current of 110 mA will cause slew rate limitations. All the amplifiers that have the same or better specifications than OPA2677 on the selected parameters have a thermal shutdown functionality. This makes the amplifier shut down at a given temperature, making them unsuited for use at 180 °C. Not all datasheets state the specific temperature of thermal shutdown, but the ones that do, state 165 °C.

2.4.1 Stability

The OPA2677 is a current feedback amplifier (CFA) with a loop gain equation as shown in (2.42) [22]. Impedances used in the equation is shown in Figure 2.13.

$$A\beta = \frac{Z}{Z_F \left(1 + \frac{Z_B}{Z_F || Z_G} \right)} \quad (2.42)$$

Where Z is the open loop transimpedance, shown as a function of frequency in Figure B.1 in Appendix B. Z_B is the input buffer output impedance, given as R_I in

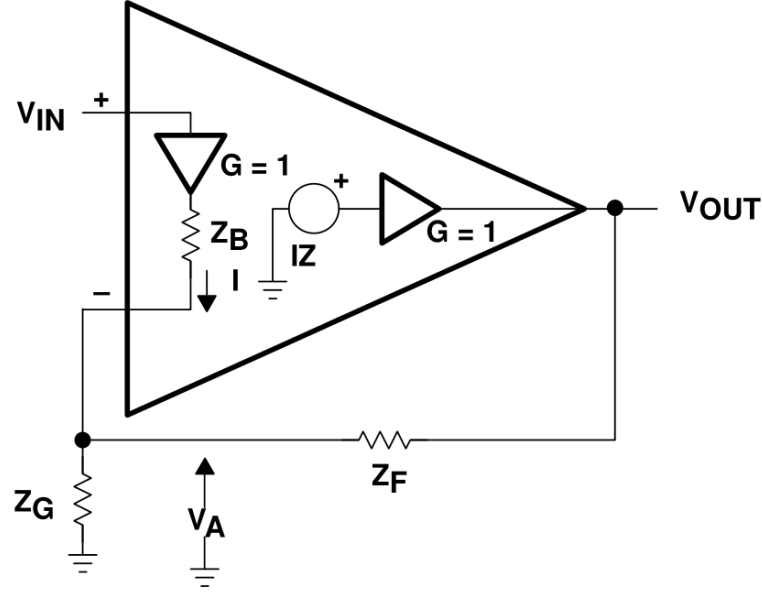


Figure 2.13: Model of a non-inverting CFA [22].

the OPA2677 datasheet with a typical value of $22\ \Omega$ [23]. Together with $Z_F = 560\ \Omega$ and $Z_G = 240\ \Omega$ this results in a feedback factor $\beta = -56\ \text{dB}$. The loop gain reaches 0 dB at 100 MHz, giving a phase margin of $PM = -115^\circ - (-180^\circ) = 65^\circ$.

The capacitive load at the gate of the output transistors can also cause instability, as it forms a pole with the open-loop output resistance of the operational amplifiers. The datasheet recommends putting a series isolation resistor between the output node and the capacitive load. The recommended value for the series resistor depends on the load capacitance, as shown in Figure B.2 in Appendix B.

Series resistors are currently placed at the primary as well as both secondary windings to achieve stability. Series capacitors is placed at all windings to avoid DC current flow through the transformer windings. The apparent load capacitance when ignoring the series resistors and external capacitors is calculated in (2.43). The turn ratios are $\frac{N_{SN}}{N_P} = 2$ and $\frac{N_{SP}}{N_P} = 2.5$.

$$C'_L = \left(\frac{N_S}{N_P}\right)^2 C_{gs} = \left(\frac{N_S}{N_P}\right)^2 (C_{iss} - C_{rss}) \quad (2.43)$$

The maximum apparent load capacitance when using the new output transistors FQD6N25 and FQD4P25 is calculated in (2.44) and 2.45.

$$C'_{L-nmos} = \left(\frac{2}{1}\right)^2 \times (300\ \text{pF} - 10\ \text{pF}) = 1.16\ \text{nF} \quad (2.44)$$

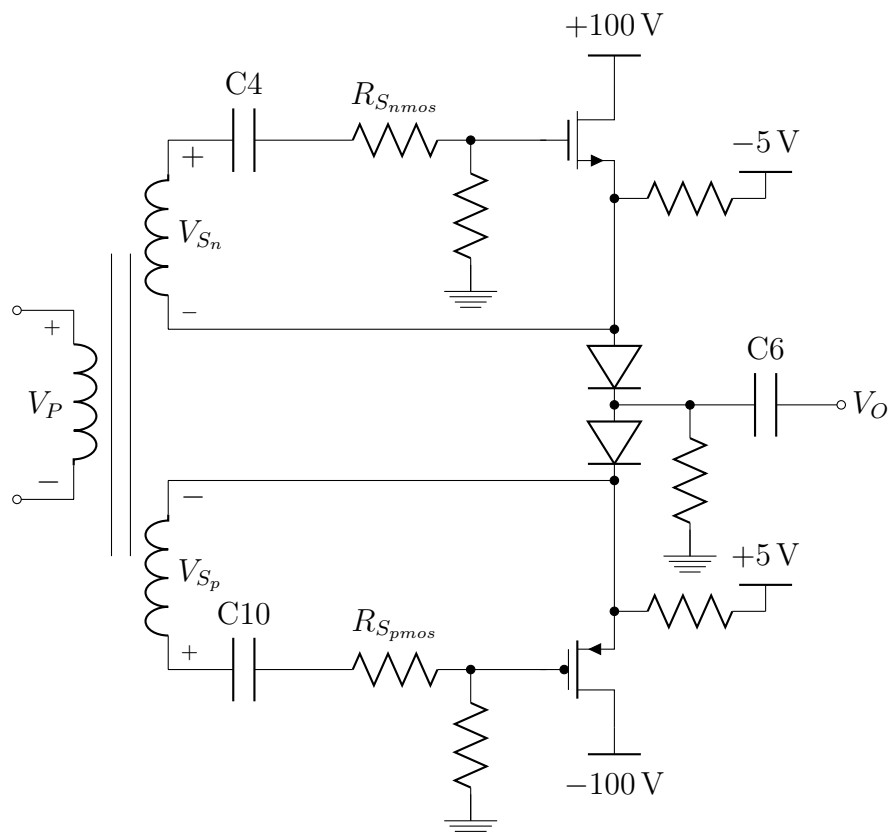


Figure 2.14: Transformer and output stage with bias resistors.

$$C'_{L-pmos} = \left(\frac{2.5}{1}\right)^2 \times (420 \text{ pF} - 13 \text{ pF}) = 2.54 \text{ nF} \quad (2.45)$$

From Figure B.2, the recommended series isolation resistor value is found to be less than 6Ω . When using a differential circuit, the total resistance from one operational amplifier output to the other needs to be doubled. Using two series resistors of 2.2Ω each, at the primary side, the NMOS needs an additional apparent load resistance of 7.6Ω to get a total isolation resistance of 12Ω . The PMOS with its 2.54 nF needs an additional apparent load resistance of 5.6Ω to achieve a total isolation resistance of 10Ω . The actual resistance values are calculated in (2.46) and 2.47.

$$R_{S_{nmos}} = R'_{S_{nmos}} \times \left(\frac{N_{S_{nmos}}}{N_P}\right)^2 = 7.6 \Omega \times \left(\frac{2}{1}\right)^2 = 30 \Omega \implies R_{S_{nmos}} = 30 \Omega \quad (2.46)$$

$$R_{S_{pmos}} = R'_{S_{pmos}} \times \left(\frac{N_{S_{pmos}}}{N_P}\right)^2 = 5.6 \Omega \times \left(\frac{2.5}{1}\right)^2 = 35 \Omega \implies R_{S_{pmos}} = 36 \Omega \quad (2.47)$$

The load impedance referred to the primary, also known as the apparent load impedance, Z'_L is calculated in (2.48). The last line is calculated with a frequency of 6 MHz .

$$\begin{aligned} Z'_L &= \left(\frac{N_P}{N_{S_n}}\right)^2 Z_{L_n} \parallel \left(\frac{N_P}{N_{S_p}}\right)^2 Z_{L_p} \\ &= \left(\frac{1}{2}\right)^2 \left(30 \Omega + \frac{1}{s223 \text{ pF}}\right) \parallel \left(\frac{1}{2.5}\right)^2 \left(36 \Omega + \frac{1}{s315 \text{ pF}}\right) \\ &= (7.5 - j29.8) \parallel (5.76 - j13.5) = 3.44 - j9.35 \end{aligned} \quad (2.48)$$

This results in the following maximum voltage amplitude at the primary transformer winding with a signal frequency of 6 MHz .

$$\begin{aligned} V_P &= V_O \frac{Z'_L}{Z'_L + 2R_S} \\ &= 5.67 \text{ V} \frac{3.44 - j9.35}{3.44 - j9.35 + 2.2 + 2.2 - j0.098} = 4.60 \text{ V} \angle -19.5^\circ \end{aligned} \quad (2.49)$$

2.4.2 Possible Improvements for Differential Amplifier

To improve the output swing, the amplifier input can be ac-coupled and biased to 0 V . This will change the DC output level of each amplifier from 0.5 V to 0 V , increasing the maximum differential output amplitude by 0.5 V . It requires four extra

components, one capacitor and one resistor at each input. This is not implemented in the first prototype due to area limitations, but can be reconsidered if a higher output voltage is needed.

The low pass characteristic frequency response of the output stage can be compensated by implementing a high pass characteristic in the differential amplifier. This is tested and documented in section 4.8.

By switching to a QFN-16 package, the thermal impedance can be decreased by $5^\circ\text{C}/\text{W}$. The resulting maximum allowed ambient temperature is calculated in (2.50).

$$T_{A-max} = T_{J-max} - P_D \times \theta_{JA} = 150^\circ\text{C} - 195\text{ mW} \times 50^\circ\text{C}/\text{W} = 140^\circ\text{C} \quad (2.50)$$

The area will also be reduced from 29.4 mm^2 to 23.0 mm^2 . The advantages are not sufficient to overcome the disadvantages when it comes to robustness. In a typical thermal cycling test between -40°C to 125°C , a QFP package can stand over 10 000 cycles whereas QFN tends to fail between 1000 to 3000 cycles. QFNs may also be more susceptible to flex-induced joint and laminate cracks [13]. The difference between QFP and QFN is the absence of leads in a QFN package, implying that a HSOP package will also have the same advantage in robustness.

2.4.3 Thermal Considerations

The dynamic power dissipation is calculated in (2.51) by using the same equations as for the output transistors. By using the superposition theorem, each operational amplifier can be treated as an output stage with a capacitive load to ground.

The single ended peak-to-peak output voltage and the apparent load capacitance is used to calculate the current. The energy delivered from each supply is added, as everything is dissipated in one package. Lastly, the power dissipation should be doubled to account for the fact that there are two operational amplifiers in one package. This is rather done by using the differential peak-to-peak voltage in the equation.

$$\begin{aligned} P_{OPA} &= \frac{n_{pulse}}{T_{ping}} C 2V_{DD} V_{O_{p-p}} \\ &= \frac{16}{347\ \mu\text{s}} \times 2.9\ \text{nF} \times 2 \times 5\ \text{V} \times 11.3\ \text{V} = 15\ \text{mW} \end{aligned} \quad (2.51)$$

The temperature increase due to quiescent power consumption P_{DQ} is calculated in (2.52). The current used is the maximum quiescent current at a temperature up to 85°C . This is expected to increase as the temperature increases.

$$P_{DQ-max} = I_{Q-max} \times (V_{DD} - V_{SS}) = 19.5\ \text{mA} \times [5\ \text{V} - (-5\ \text{V})] = 195\ \text{mW} \quad (2.52)$$

A switch circuit for the $\pm 5\text{ V}$ supplies is included in the original design to reduce the static power dissipation. Each of the $\pm 5\text{ V}$ supplies is split into two power planes, one switched and one that is always on. This reduces the static power dissipation, but increases the dynamic power dissipation due to charging the decoupling capacitors. The added dynamic power dissipation in the operational amplifiers is calculated in (2.53). The same amount of power is dissipated in the resistance between the power supply and the decoupling capacitors, but this power does not contribute to temperature rise in the operational amplifiers.

$$P_{Decoupling} = \frac{1}{T_{ping}} C 2V_{DD}^2 = \frac{1}{347\ \mu\text{s}} \times 2.2\ \mu\text{F} \times 2 \times (5\ \text{V})^2 = 317\ \text{mW} \quad (2.53)$$

An added dynamic power dissipation of 317 mW exceeds the reduced static power dissipation and is thus unnecessary. The original design had decoupling capacitors at 220 nF, resulting in an added dynamic power consumption of 32 mW. If the switching circuit is to be used to reduce power consumption, a reduction of decoupling capacitance is required.

OPA2677 comes in three different packages, each with different thermal impedance. The package used in the current revision is a "Heatsink Small Outline Package" (HSOP) with a thermal impedance from junction to ambient of $55\text{ }^\circ\text{C/W}$. The maximum allowed ambient temperature with a HSOP package and a total power dissipation of 210 mW is calculated in (2.54).

$$T_{A-max} = T_{J-max} - P_D \times \theta_{JA} = 150\text{ }^\circ\text{C} - 195\ \text{mW} \times 55\text{ }^\circ\text{C/W} = 138\text{ }^\circ\text{C} \quad (2.54)$$

2.5 Input termination

The input of the transmitter circuit is two complementary current outputs of an AD9740 DAC. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply $V_{OUT} = I_{OUT} \times R_{LOAD}$. The voltage output of each node should not be lower than -1 V or higher than $+1.2\text{ V}$ when using the maximum full-scale output current of 20 mA [1].

This input current is fed into termination resistors to achieve the wanted voltage input at the operational amplifier. The termination resistors used in the current revision is shown in Figure 2.15.

The peak input voltage is calculated in (2.55) for a temperature of $25\text{ }^\circ\text{C}$ and in (2.56) for a temperature of $180\text{ }^\circ\text{C}$. The PT100 element is used as a temperature compensation which increases the input voltage as the temperature increases. Resistance values for the PT100 elements are given in tables for each degree celsius [24].

$$\hat{V}_{in}|_{T=25\text{ }^\circ\text{C}} = \hat{I}_{in} \times R_{in} = 20\ \text{mA} \times (109.7\ \Omega + 18\ \Omega) \parallel 82\ \Omega = 1.00\ \text{V} \quad (2.55)$$

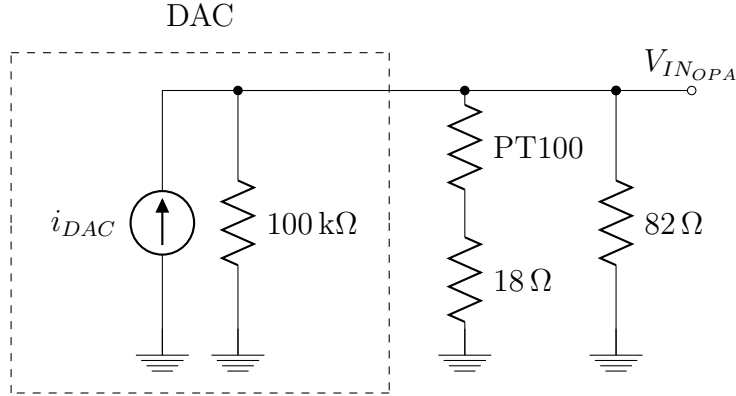


Figure 2.15: Input network with DAC model.

$$\hat{V}_{in}|_{T=180^\circ\text{C}} = \hat{I}_{in} \times R_{in} = 20 \text{ mA} \times (168.5 \Omega + 18 \Omega) \parallel 82 \Omega = 1.14 \text{ V} \quad (2.56)$$

2.5.1 Possible Improvements for Input Stage

The temperature compensation functionality of the input termination network is not very accurate. By using only one resistor of 62Ω for each of the inputs, the input voltage range is 0 V to 1.24 V . This exploits the positive compliance range, which is limited to 1.25 V . To extend the input voltage range to $\pm 1 \text{ V}$, a bias voltage of -1 V is needed. If a voltage source with an output resistance of 0Ω was available, a resistor at 100Ω could have been used to achieve a voltage range of $\pm 1 \text{ V}$. The output resistance of the bias circuit is included when calculating DAC output voltage, as shown in (2.57). R_T is a termination resistor between the DAC output and the bias voltage.

$$\begin{aligned} V_{O_{DAC}} &= I_O \times (R_T + R_{bias}) \\ 1 \sin(\omega t) &= 10 \times 10^{-3} (1 + 1 \sin(\omega t)) \times (R_T + R_{bias}) \\ \implies (R_T + R_{bias}) &= 100 \Omega \end{aligned} \quad (2.57)$$

A suggested solution is shown in Figure 2.16. This increases the amount of components from one to three per input, but by using this circuit, an AC-coupling between DAC and differential amplifier is not necessary to improve output swing. A drawback by introducing this input network is increasing the quiescent current at the -5 V supply by 8 mA . It is therefore not implemented in the first revision, but noted as a possible future implementation. The quiescent current can be reduced by increasing the resistance and reducing the full scale output current, but this will increase the noise level as thermal noise in resistors is proportional to resistance.

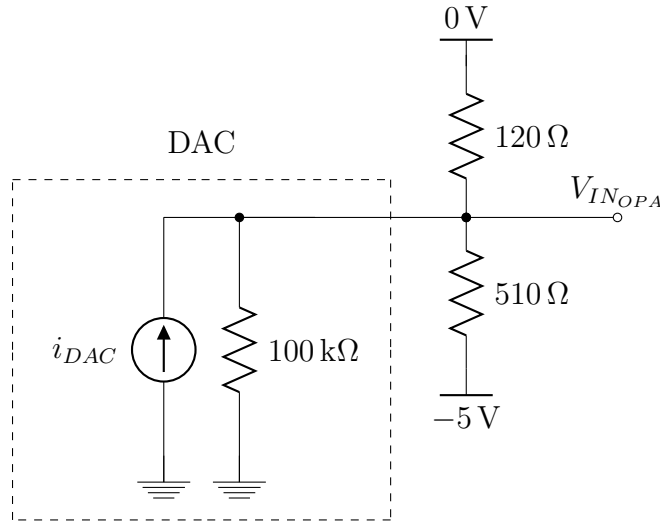


Figure 2.16: Amplifier input network to maximize symmetric DAC output swing.

2.6 Passive Components

The AC-coupling capacitors need to have a high enough capacitance to reach a negligible impedance in the signal frequencies. When the impedance is a factor 100 lower than the load impedance, it will lead to a voltage drop of less than 1% and is thus considered negligible. The capacitance is affected by temperature and DC voltage, which also has to be accounted for. Capacitance vs temperature performance for X7R capacitors rated to 175 °C is shown in Figure 2.17.

The voltage rating has to be higher than the maximum voltage over the capacitor to prevent it from failing. The package size should be as small as possible to minimize area and parasitic effects. Voltage over each AC-coupling capacitor is calculated using (2.58). The minimum signal frequency of 2 MHz is used as it results in the highest capacitor impedance.

$$V_{C_{ac}} = V_{DC} + V_s \frac{Z_{C_{ac}}}{Z_{C_{ac}} + Z_L} \quad (2.58)$$

The two AC-coupling capacitors, C4 and C10, between each secondary winding and output transistor is currently 100 nF rated to 100 V. The capacitance is over 300 times larger than the gate-source capacitance, making it negligible at signal frequencies. The maximum voltage over the capacitors is calculated in (2.59). Maximum DC voltage is the maximum threshold voltage of the transistor. The AC voltage used is for the PMOS secondary winding, as it has the highest voltage.

$$V_{C10_{max}} = V_{DC} + V_{S_{n-max}} \times \frac{-0.80i \Omega}{-0.80i \Omega + (36 - 196i) \Omega} = 5.06 \text{ V} \quad (2.59)$$

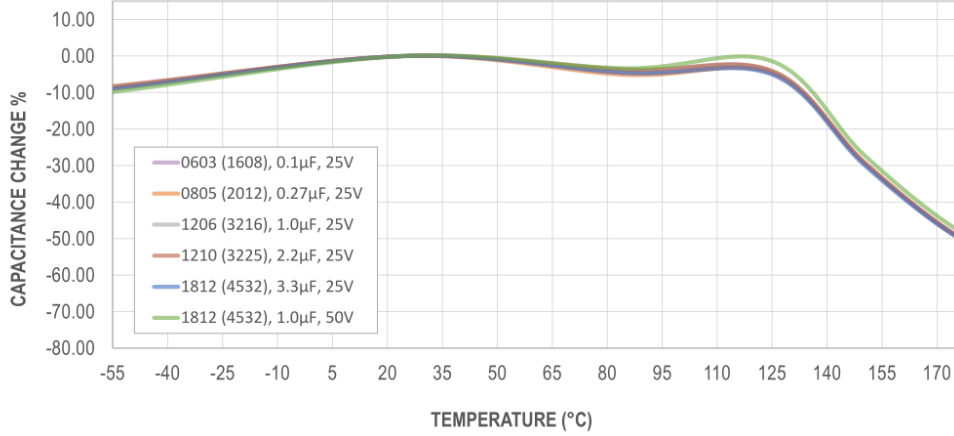


Figure 2.17: Capacitance vs. temperature for a high temperature X7R capacitor [11].

The AC-coupling capacitance at the input of the output transistors can be reduced by a factor three, together with reducing the voltage rating, getting a smaller package and higher temperature rating. All implemented capacitor replacements is summarized at the end of section 2.6 in Table 2.6.

The AC-coupling capacitor at the output, C6, is also 100 nF rated to 100 V. The capacitance is over 50 times higher than the load capacitance, and should be doubled to meet the negligibility criteria. The maximum voltage over the output AC-coupling capacitor is calculated in (2.60), at a frequency of 2 MHz.

$$V_{C6_{max}} = V_O \frac{Z_{C_{ac}}}{Z_{C_{ac}} + Z_L} = 100 \text{ V} \frac{-0.80i \Omega}{-0.80i \Omega + (6.39 - 45.9i) \Omega} = 1.7 \text{ V} \quad (2.60)$$

The output AC-coupling capacitor should therefore be replaced by a larger value, smaller package, lower voltage rating and higher temperature rating.

The AC-coupling capacitor at the primary winding of the transformer, C8, is 100 nF rated to 50 V. The impedance at 2 MHz is over 200 times smaller than the impedance of the ten turn primary winding with the 0C40502TC core. The maximum voltage between its terminals is calculated in (2.61), at a frequency of 2 MHz.

$$V_{C8_{max}} = V_O \frac{Z_{C_{ac}}}{Z_{C_{ac}} + Z_L} = 5.67 \text{ V} \frac{-0.80i \Omega}{-0.80i \Omega + (17.3 - 130i) \Omega} = 35 \text{ mV} \quad (2.61)$$

The primary winding capacitor should also be replaced to achieve smaller package and higher temperature rating in return for reducing the voltage rating.

Table 2.4: Equivalent series resistance and inductance for decoupling capacitors [12].

Package	ESR [mΩ]	ESL [nH]
2220	4	1.8
1210	19	1.4

2.6.1 Decoupling

Ceramic capacitors are used for decoupling the $\pm 5\text{ V}$ and $\pm 100\text{ V}$ supplies. This is done to reduce current transients from the power supply unit and rather maintain a static current. The capacitors act as energy reservoirs and deliver high current for short periods. When assuming no current supplied from the power supply, the voltage reduction at the decoupling capacitor should be as low as possible.

The amount of delivered energy per supply during one period of a sinusoidal signal with a capacitive load is calculated in (2.62) from subsection 2.2.2.

$$E_{C_L} = CV_{supply}(V_{C_{max}} - V_{C_{min}}) \quad (2.62)$$

When the reservoir capacitor delivers energy to a capacitive load, the supply voltage is reduced. The minimum supply voltage after a maximum of 16 periods is calculated in (2.63). When the temperature increases to $175\text{ }^\circ\text{C}$, a derating of the capacitance at about 50% is realistic [11]. The minimum voltage at the reservoir capacitor with a temperature of $175\text{ }^\circ\text{C}$ is therefore also calculated.

$$\begin{aligned} E_{res_{min}} &= E_{res_{nom}} - nE_{C_L} \\ \frac{1}{2}C_{res}V_{res_{min}}^2 &= \frac{1}{2}C_{res}V_{res_{nom}}^2 - n_{pulse}CV_{res_{nom}}(V_{C_{max}} - V_{C_{min}}) \\ V_{res_{min}} &= \sqrt{V_{res_{nom}}^2 - 2n_{pulse}\frac{C_L}{C_{res}}V_{res_{nom}}V_{O_{pp}}} \end{aligned} \quad (2.63)$$

There will also be a voltage drop over the equivalent series resistance and inductance of the capacitor, calculated in (2.64). Values are obtained from KEMETspice and listed in Table 2.4.

$$V_{drop} = V_{res_{nom}} \frac{ESR + i \times ESL}{ESR + s \times ESL - \frac{1}{s \times C_L}} \quad (2.64)$$

Decoupling of Output Transistor

Two ceramic capacitors, C3 and C12, at $1\text{ }\mu\text{F}$ each are used for decoupling the $\pm 100\text{ V}$ supplies at the output. These act as energy reservoirs for charging the

load capacitance at the output. The resulting minimum voltage at a 1 μF reservoir capacitor over a maximum of 16 periods is calculated in (2.65).

$$V_{res_{min}} = \sqrt{100 \text{ V}^2 - 2 \times 16 \times \frac{1.8 \text{ nF}}{1 \mu\text{F}} \times 100 \text{ V} \times 200 \text{ V}} = 94.1 \text{ V} \quad (2.65)$$

The voltage drop due to equivalent series resistance and inductance is calculated in (2.66).

$$V_{drop} = 94.1 \text{ V} \times \frac{(4 + 68i) \text{ m}\Omega}{(0.004 - 15i) \Omega} = 0.44 \text{ V} \quad (2.66)$$

The capacitance is increased to 2.2 μF , increasing the minimum voltages to 97.4 V at 25 $^\circ\text{C}$ and 94.6 V at 175 $^\circ\text{C}$. These values assume equal signals at all channels and no energy transferred between channels. This is worst case assumptions, as the signal is often separated slightly in time between channels when imaging.

Decoupling of OPA2677

Two ceramic capacitors, C11 and C13, at 220 nF each are used for decoupling the $\pm 5 \text{ V}$ supplies. These act as energy reservoirs for charging the apparent load capacitance at the primary winding. The resulting minimum voltage at a 220 nF reservoir capacitor over a maximum of 16 periods is calculated in (2.67). This calculation assumes no charging of the reservoir capacitor during the 16 periods, but the result shows that a lot of the energy needs to be delivered by the power supply unit, causing noise on the power line.

$$V_{res_{min}} = \sqrt{5 \text{ V}^2 - 2 \times 16 \times \frac{3.7 \text{ nF}}{220 \text{ nF}} \times 5 \text{ V} \times 9.20 \text{ V}} = 0.49 \text{ V} \quad (2.67)$$

During a period of a sinusoidal output signal, the $\pm 5 \text{ V}$ capacitors charge the transistor input capacitors through the transformer. The apparent load capacitance charged by the reservoir capacitors is calculated in (2.68) using results from equations 2.44 and 2.45.

$$C'_P = \left(\frac{N_{S_n}}{N_P}\right)^2 \times C_{S_n} + \left(\frac{N_{S_p}}{N_P}\right)^2 \times C_{S_p} = 1.16 \text{ nF} + 2.54 \text{ nF} = 3.70 \text{ nF} \quad (2.68)$$

The voltage drop due to equivalent series resistance and inductance is calculated in (2.69).

$$V_{drop} = 5 \text{ V} \times \frac{(19 + 53i) \text{ m}\Omega}{(4.4 - 7.1i) \Omega} = 34 \text{ mV} \quad (2.69)$$

The original decoupling capacitor is compared to the maximum capacitance for each package size in a capacitor series rated for 175 $^\circ\text{C}$ in Table 2.5. The resulting

Table 2.5: Decoupling capacitor possibilities for OPA2677.

C[nF]	V_{min} [V], 25 °C	V_{min} [V], 175 °C	V_{max} [V]	T_{max} [°C]	Package
220	0.49	0	100	125	1206
680	4.1	3.0	25	175	805
1000	4.4	3.8	25	175	1206
2200	4.7	4.5	25	175	1210
3300	4.8	4.7	25	175	1812

Table 2.6: All implemented capacitor changes for the new transmitter.

Designator	C [nF]		V_{max} [V]		T_{max} [°C]		Package	
	Old	New	Old	New	Old	New	Old	New
C5, C7, C9	100	100	50	50	125	175	0805	0603
C8	100	680	50	25	125	175	0805	0805
C4, C10	100	100	100	50	125	175	1206	0603
C6	100	270	100	50	125	175	1206	0805
C11, C13	220	2200	50	25	125	175	1206	1210
C3, C12	1000	2200	250	250	125	125	1825	2220

minimum voltage is also shown at 25 °C and 175 °C, not including the voltage drop due to ESL and ESR.

The 2.2 μ F capacitor is chosen for the new design, but due to availability a similar capacitor rated to 125 °C is used. This is also a KEMET X7R MLCCs with flexible termination, and is likely to have a similar behavior to the high temperature version.

All capacitor changes are summarized in Table 2.6.

2.7 Diodes

2.7.1 Transient Voltage Suppression

The voltage of an inductor is proportional to the rate of change of current through the inductor. If the input signal to the transmitter circuit is suddenly turned off, the current through the transformer windings will also change suddenly. This results in a high voltage over the windings, which can exceed the maximum transistor gate-source voltage.

To protect the transistor from voltages exceeding $V_{GS_{max}} = \pm 30$ V, a transient voltage suppressor (TVS) diode is connected between gate and source of each output

transistor. The TVS diodes are shown in Figure 3.1 with reference designators D1 and D3. Disadvantages include added capacitance and area usage on the PCB. SMBJ18CA, which is currently used in the design has a junction capacitance of approximately 3 nF at a reverse voltage of 10 V. This is seven times the maximum transistor input capacitance and will dominate the capacitive load seen by the operational amplifier.

The original TVS diode is replaced by CDSOD323-T18C in the new design, reducing junction capacitance to 3 pF and the area is reduced by 83%. Maximum clamping voltage is 29.0 V at a peak current of 1 A. This is below the maximum gate-source voltage $V_{GSS} = \pm 30$ V as well as the current exceeds the maximum secondary current of 0.8 A, calculated in (2.70).

$$I_{SN_{max}} = I_{P_{max}} \times \frac{N_P}{N_{SN}} = 1.6 \text{ A} \times \frac{10}{20} = 0.8 \text{ A} \quad (2.70)$$

As a bonus, the CDSOD323-T18C is rated for ESD protection up to a maximum of 30 kV and meets the requirements of the IEC 61000-4-2 *Electrostatic Discharge Immunity Test* [4].

2.7.2 Output Diodes

Two diodes are placed in series between sources of the output NMOS and PMOS. This is done to be able to set the gate source voltages approximately equal to the threshold voltage with a minimal bias current. Biasing the gate source voltages to the threshold voltage results in low crossover distortion, and makes it easier to drive the the output transistors by reducing the needed AC-voltage. Reducing the bias current reduces the output transistor case temperature.

The diodes used in the original design is HSMP-3832 from Avago Technologies, supplied in an SOT-23 package measuring a maximum of 8.5 mm². It has a maximum series resistance of 1.5 Ω , measured at a forward current of 100 mA. The maximum junction temperature is 150 °C. The maximum total capacitance is 0.3 pF measured at a reverse voltage of 50 V.

Any leakage current through the diodes will result in a voltage drop over the bias resistor and thus reduced gate-source voltage. To minimize variation in gate-source voltage, the bias current has to be much larger than the variation in diode leakage current. This makes it important to have diodes with low leakage current variation. In addition, the diodes needs to endure the maximum current of 16 half sine-wave current pulses with an amplitude of 6.6 A and frequency 6 MHz. The maximum rating for HSMP-3832 is a 1 ms pulse at 1 A.

Alternatives include Schottky diodes, PN diodes as well as other PIN diodes, all listed in Table 2.7. The schottky barrier diode has a low forward voltage drop, but

Table 2.7: Output diode alternatives from different technologies.

Type	Name	A_{tot} [mm ²]	I_{fsm} [A]	V_f [V]	T_{max} [°C]	I_r [mA]
PIN	HSMP3832	8.5	1 (1 ms)		150	
SiC	DB2G42600L1	1.2	10 (5 ms)	0.51	150	1
SBR	SBR1U200P1	13	40 (8.3 ms)	0.75	175	0.1
PN	BAV103	9.6	1 (1 s)	1.25	200	0.1

is easily susceptible to thermal runaway due to its high leakage characteristics. PN diodes have lower leakage, but higher forward voltage drop. All leakage currents are given for 150 °C.

Two super barrier rectifier diodes, type SBR1U200P1 are recommended for use in the new design. These diodes exceed the current requirement both in amplitude and duration, as well as having a maximum operating temperature of 175 °C. Reverse current is given for four different temperatures in the datasheet and by exponential extrapolation, the typical reverse current at 175 °C is 0.41 mA. The original diodes, HSMP-3832 were used in all tests.

Prototype

This chapter describes the process from design schematic to a working prototype ready for testing. A complete schematic of the new transmitter circuit is shown in Figure 3.1.

The PCB made by the subcontractor was a natural starting point for the PCB design. The same outer dimensions and connectors were used to be able to test it with the rest of the tool. To keep cost and time consume at a low level, components were only mounted for two of the channels. This makes it possible to test both designs at the same time under the same conditions.

3.1 Printed Circuit Board Layout

The PCB consists of eight copper layers with a copper thickness of $35\ \mu\text{m}$. A total of seven different power planes are used, including +5VSW and -5VSW, which can be switched to 0 V by a control circuit. The layers are stacked as follows, where the upper and lower designators on split planes are from a view perpendicular to the top signal layer with inputs to the right and outputs to the left:

- Top Signal Layer
- Top Power Plane: Upper half $-100\ \text{V}$, lower half +5 VSW
- Mid Signal Layer 1
- Mid Power Plane 1: Upper 15 % $-5\ \text{V}$, lower 85 % +5 V
- Mid Power Plane 2: 0 V

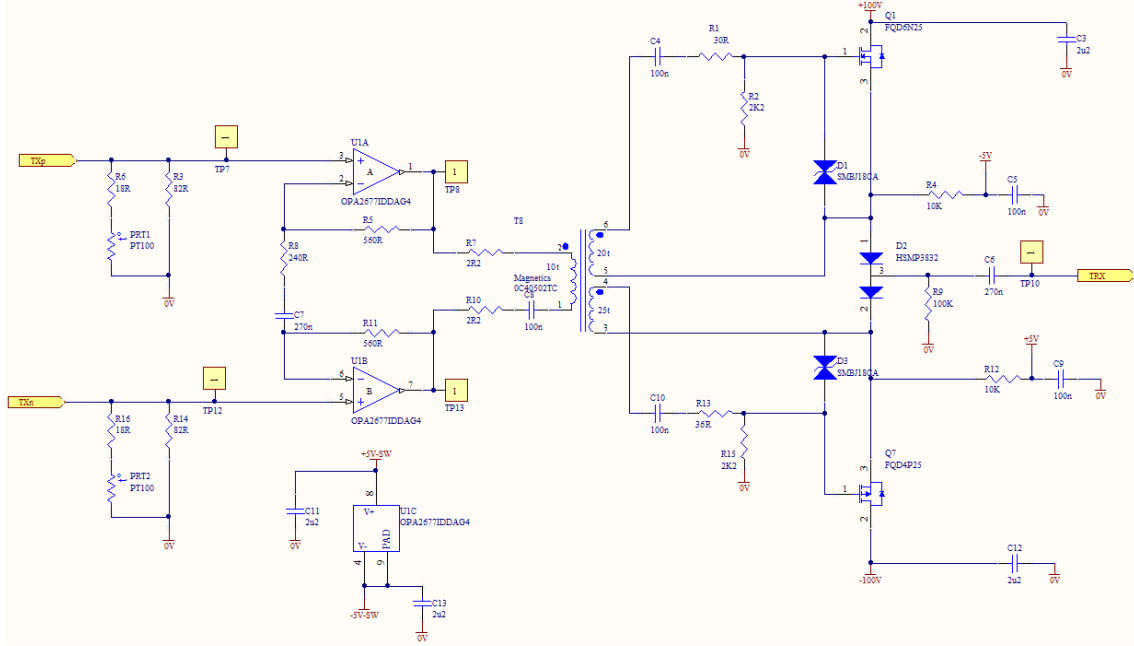


Figure 3.1: Schematic of new transmitter circuit.

Table 3.1: Minimum spacing between conductors [9].

Voltage	Pads	Traces
0 V to 30 V	0.1 mm	0.05 mm
31 V to 100 V	0.6 mm	0.13 mm
101 V to 150 V	0.6 mm	0.4 mm
151 V to 250 V	1.25 mm	0.4 mm

- Mid Signal Layer 2
- Bottom Power Plane: Upper half +100 V, lower half -5 VSW
- Bottom Signal Layer

When placing the components it is important to consider how the PCB traces can be placed to minimize parasitic effects. Inductance and resistance of a PCB trace is inversely proportional to trace width. Both parameters lead to an unwanted voltage loss over the trace, and resistance also lead to increased temperature in the trace. This encourages a trace that is as wide as possible, limited by space, accepted capacitance and electrical clearance. Recommended clearance between traces from IPC-2221A standard is shown in Table 3.1 for pads and coated traces.

The inductance of a PCB trace can be calculated with the formula in (3.1) [5].

$$L = 2 \times 10^{-3} \left[\ln \left(\frac{2l}{w+t} \right) + 0.5 + 0.2235 \left(\frac{w+t}{l} \right) \right] \mu\text{H} \quad (3.1)$$

The tool also has height limitations as mentioned in the beginning of chapter 2. The $\pm 100\text{ V}$ decoupling capacitors are the tallest components with a maximum height of 4.5 mm which inhibits placing them on the bottom layer where the maximum component height is less than 4.5 mm.

The Syfer Stackicap is chosen because it is 1 mm lower than other capacitors with the same specifications. When placed on the top layer, they have to be placed at a minimum of 3.6 mm from the PCB edge. If a 1 mm taller capacitor had been chosen, they would have to be placed at a minimum of 5.5 mm from the PCB edge.

The decoupling capacitors are placed with the 0 V pad closest to the board edge, minimizing electrical insulation needs, as well as minimizing resistance and inductance to the transistor drain pads. The output transistors with a maximum height of 2.39 mm are safely placed on the inside of the decoupling capacitors.

The operational amplifier has a maximum height of 1.75 mm, and should be placed at a minimum distance of 1.75 mm from the edge of the PCB. The $\pm 5\text{ V}$ decoupling capacitors have a maximum height of 2.3 mm and should be placed at a minimum distance of 2.0 mm from the PCB edge.

The mid signal layers are used for traces from the input side of the board to each channel input and from channel output to the output side of the board. To minimize resistance and inductance, the traces are as short as possible and via count as low as possible. This is especially for the traces conducting high current, which is why the signal traces between $\pm 100\text{ V}$ and the output is placed only on the top side. This is shown in Figure 3.2a.

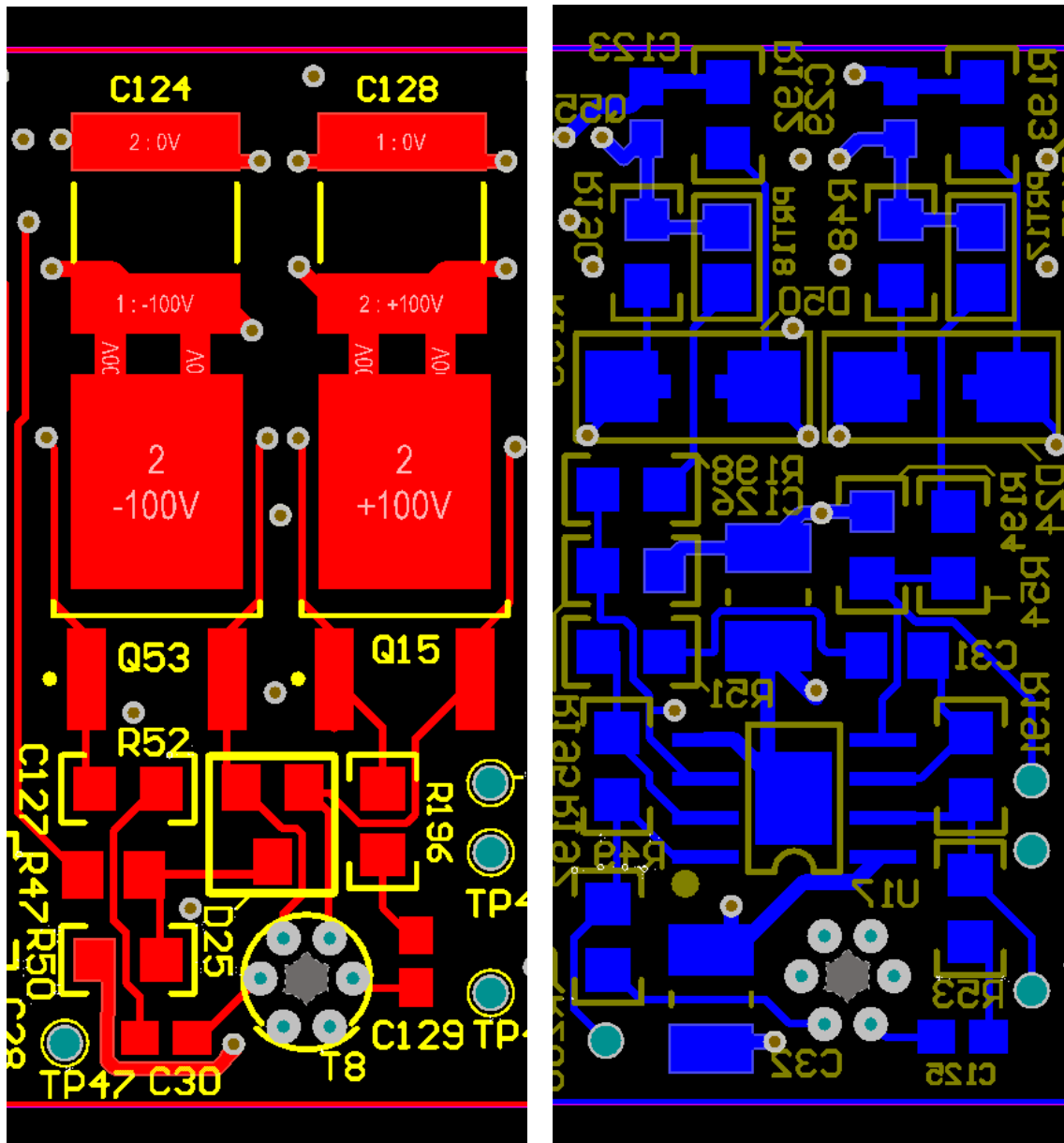
Critical traces like the signal traces from amplifier input to transformer primary is as short as possible on the bottom side. Traces between decoupling capacitors and power inputs are also kept short. Traces only carrying DC currents are not critical and placed along with the TVS diodes on the upper half of the bottom signal plane.

3.1.1 Footprints

The IPC-7351 [10] land pattern standard provides three land pattern geometry variations for surface mounted devices. Density Level A provides the most robust solder joint and is used for all transmitter components. All footprints are designed in Altium Designer 16, using the *IPC Compliant Footprint Wizard* when applicable.

A footprint for the transformer is designed for density level A of IPC-2221A [9], using a maximum wire diameter of 0.18 mm. Minimum hole size is no less than 0.25 mm over maximum lead diameter, in accordance with level A of IPC-2222 [8]. Geometry calculations are shown below:

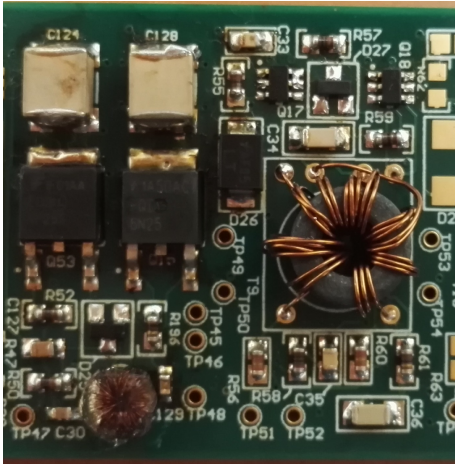
$$D_{hole_{min}} = D_{wire_{max}} + 0.25\text{ mm} = 0.43\text{ mm} \quad (3.2)$$



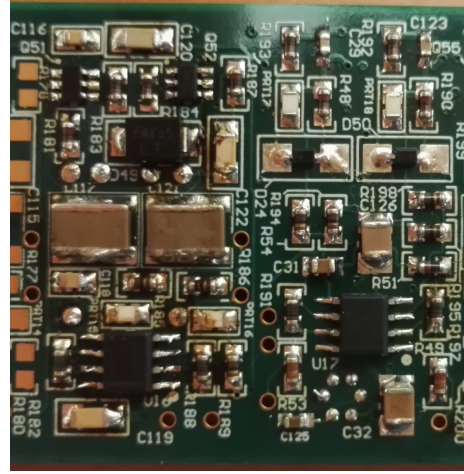
(a) Top Layer.

(b) Bottom Layer (view from topside).

Figure 3.2: PCB layout for one transmitter channel.



(a) Top Layer. New design to the left and old design to the right.



(b) Bottom Layer. New design to the right and old design to the left.

Figure 3.3: Two channels on the PCB layout with all components soldered on.

Minimum through-hole pad size is limited by maximum hole size, minimum annular ring requirements and a standard fabrication allowance. Minimum external annular ring for a supported hole (a hole that contains plating or other types of reinforcement) is 0.050 mm. Minimum standard fabrication allowance for density level A is 0.4 mm.

$$D_{pad_{min}} = D_{hole_{min}} + 2 \times 0.05 \text{ mm} + 0.4 \text{ mm} = 0.93 \text{ mm} \quad (3.3)$$

Minimum spacing between transformer footprint pads is found in IPC-2221A. A minimum spacing of 0.6 mm is sufficient for uncoated external conductors when the peak voltage difference is limited to a maximum of 150 V, while a minimum spacing of 0.1 mm is sufficient for voltages up to 30 V. This is valid for altitudes up to 3050 m. Voltages over 30 V only occur between the secondary windings and the primary windings, while voltages from secondary to secondary and primary to primary is limited below 30 V. This is made use of to minimize footprint area, while still abiding the rules, as can be seen at the bottom of Figure 3.2.

The two channels on the PCB is shown in Figure 3.3 with all components soldered on. The picture is taken after temperature testing.

Test and Characterization

This chapter starts with analyzing tests done by a subcontractor on the original transmitter, and then proceeds with all tests performed throughout this thesis. This includes tests done during the design period to verify components and final tests on the complete design.

4.1 Tests Performed Before the Thesis

All tests performed by the subcontractor is done with two parallel dummy loads of $50\ \Omega$ in series with $180\ \text{pF}$ per channel. This is approximately equivalent of two transducers, type 6071. By not including the impedance of the switch circuit in their measurements, the results are better than what they would be with a realistic load.

The gain of the original transmitter circuit is in these tests stable up to a signal frequency of $3.5\ \text{MHz}$. This drop in gain is tested to be due to the section between the primary of the transformer and the output, as seen in Figure 4.1.

The transmitter circuit has been tested up to $180\ ^\circ\text{C}$. In this test the output voltage dropped from approximately $200\ \text{V}_{pp}$ at $30\ ^\circ\text{C}$ to $150\ \text{V}_{pp}$ at $180\ ^\circ\text{C}$. The signal frequency was $3\ \text{MHz}$.

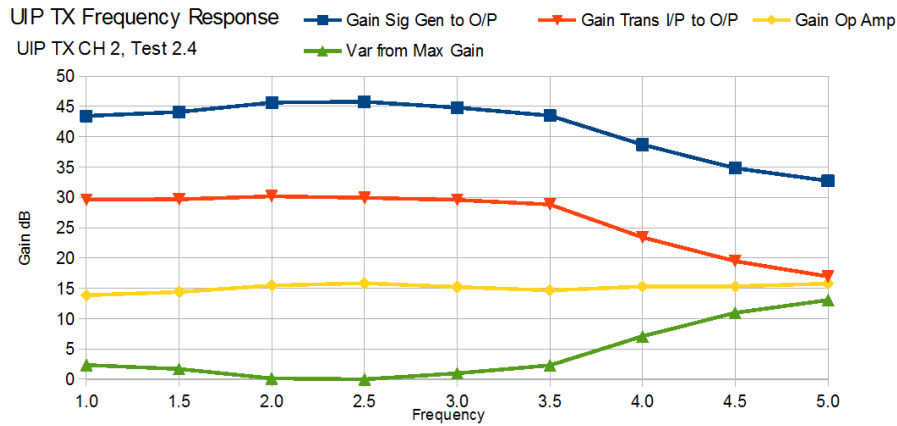


Figure 4.1: Transmitter frequency response measured by a subcontractor [3]. The blue graph shows total gain, yellow shows operational amplifier gain, orange shows combined gain of transformer and output transistors.

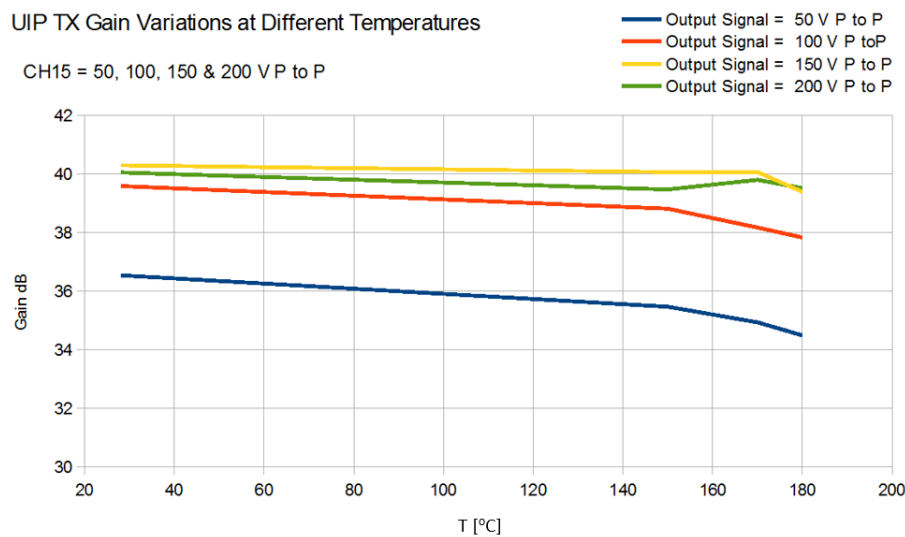


Figure 4.2: Transmitter temperature response measured by a subcontractor [3].

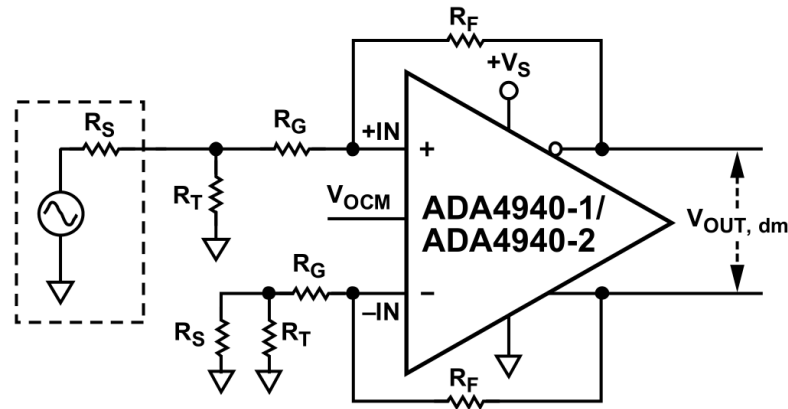


Figure 4.3: Schematic of single-ended to differential signal conversion.[2]

4.2 Preliminary Tests

Instead of using the DAC, the single-ended signal from a signal generator is converted to a differential signal with an offset of 0.5 V. This is done by using an ADA4940 fully differential amplifier. The complete circuit diagram is shown in Figure 4.3. By adjusting the signal generator output from 0 to $2V_{pp}$, the same amplitude will appear between the two differential outputs.

The common mode output voltage is set by applying the desired voltage to the V_{OCM} pin. This voltage is applied by using a voltage divider from +2.5 V to 0 V. The input resistance of the V_{OCM} pin is typically 250 k Ω , but not very accurate. To minimize the quiescent current and influence of R_{in} , R_2 is set to 2.5 k Ω . To achieve a voltage of 0.5 V, R_1 is set to 10 k Ω , which leads to a quiescent current of 200 μ A.

4.2.1 Operational Amplifier

A test was performed to check maximum current output of the OPA2677 with ± 5 V supplies. The input signal came from a signal generator, Tabor 2571A, through the single ended to differential amplifier shown in Figure 4.3.

The operational amplifier functionality is tested to a maximum ambient temperature of 180 $^{\circ}$ C by using a heat gun. It is tested with a resistive load of 11 Ω , delivering a maximum current of 515 mA. The test signals has a delay of 347 μ s between the start of each burst to simulate maximum frame rate and number of elements. A maximum amplitude of $2V_{p-p}$ is set at the signal generator with a 50 Ω load setting.

The first test signal consisted of a one period sine, like the thickness measurement signal. This was incremented to a 16 period burst, resulting in increased internal heating. The tests were successful, and it was decided to proceed using OPA2677.

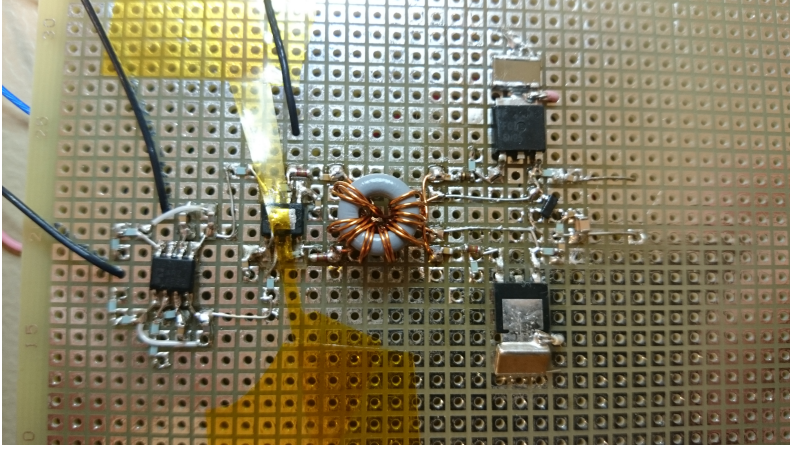


Figure 4.4: First prototype test circuit.

Table 4.1: Measured output voltage for various numbers of windings

N_P	N_{S_n}	N_{S_p}	$V_{IN_{pp}}$	$V_{O_{pp}}$	$V_{O_{max}}$	$V_{O_{min}}$
3	5	7	2	190	93.9	-96.3
2	4	5	1.5	179	90.9	-88.2
2	4	5	2	195	99.9	-94.6
3	6	8	1.5	180	91.1	-89.3
3	6	8	2	194	99.7	-94.6

4.2.2 Output Transistors

The two output transistors FQD6N25 and FQD4P25 were tested along with the original transmitter circuit, using the original 0C41005TC ferrite core. Several different winding ratios were tested to find the lowest gate-to-source voltage resulting in an output voltage of ± 100 V.

The input voltage was set to a maximum of $2V_{pp}$, while measuring the output voltage over a capacitive load of 2 nF. A capacitance of 2 nF is chosen to account for tolerance in the calculated typical load capacitance of 1.8 nF. Some of the measured output voltages is listed in Table 4.1.

As seen in Table 4.1, a winding ratio of 3/5 for the NMOS secondary is not enough to achieve full output amplitude. There is no difference in the minimum output voltage between a winding ratio of 5/2 and 8/3 for the PMOS secondary. A ratio of 4/2 for the NMOS secondary and 5/2 for the PMOS secondary is therefore chosen for further calculations. The balance between the transistors is measured as the difference between maximum and minimum absolute output voltage. For an input voltage of $1.5V_{pp}$ the difference is only $2.7V_{pp}$ with an output voltage of $179V_{pp}$.

The measured voltage amplification as a function of frequency is compared to results

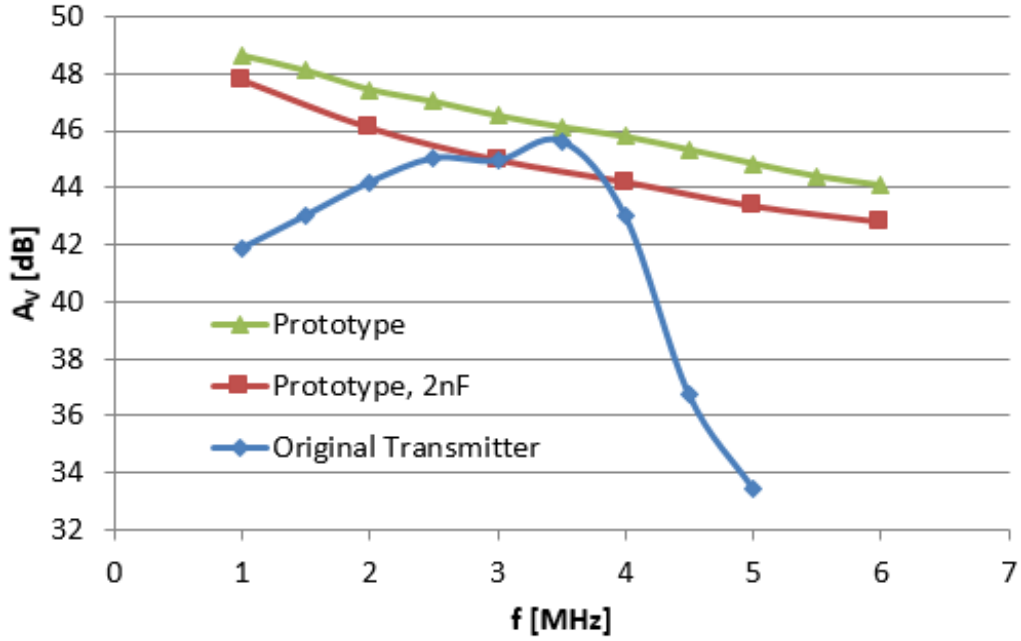


Figure 4.5: Comparison of amplification between original and prototype.

from tests done by the subcontractor on the original transmitter. These tests were done with a lighter load consisting of two dummy transducers in parallel, each consisting of 180 pF and 50 Ω in series. The new prototype was tested both with two dummy transducers in parallel and with a 2 nF load, modeling the switch circuit and transducers. A comparison is shown in Figure 4.5.

Results from the prototype show an amplification over 40 dB for frequencies of 1 MHz to 6 MHz with both loads. This implies that the prototype is able to meet the requirement of an output voltage amplitude of 200 V_{pp} with the maximum input voltage of 1 V_{pp}.

4.2.3 Core Loss

Core loss is tested at frequencies of 2 MHz and 6 MHz using the test setup shown in Figure 4.6. The single-ended to differential circuit and the differential amplifier from testing the output transistors in subsection 4.2.2 is used to drive the transformer.

Core loss is calculated using (4.1), with a winding ratio $a = \frac{N_P}{N_S} = \frac{2}{2} = 1$. v_2 and v_{ref} are measured using differential probes. v_{ref} is measured over a 2.2 Ω resistor.

$$P_{fe} = av_2 \frac{v_{ref}}{R_{ref}} \cos \theta \quad (4.1)$$

Input signal is set up as ten period bursts with a delay of 1 ms between each burst,

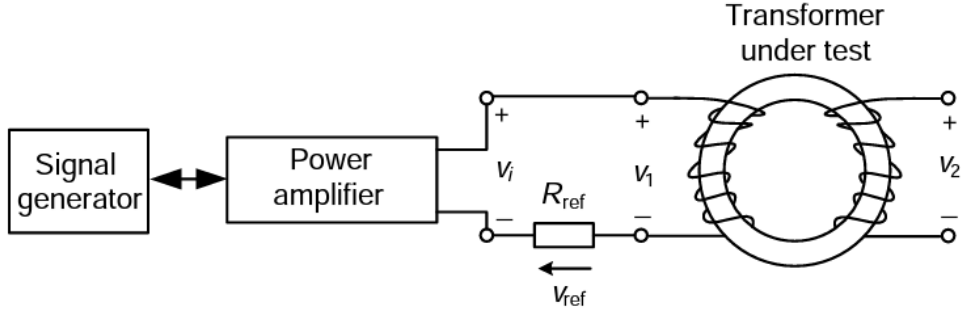


Figure 4.6: Test setup for measuring core loss [7].

Table 4.2: Measurements for determining Steinmetz coefficients.

Measurement	f [MHz]	B_{max} [mT]	v_{2pp} [V]	v_{refpp} [V]	Δt [ns]	θ [rad]	P_{fe} [mW]
A	2	35	1.85	0.621	388	4.9	10.4
B	2	70	3.69	1.11	400	5.0	72.2
C	6	35	5.54	0.663	145	5.5	141

done to reduce temperature rise in the ferrite core. Three measurements with different frequency and magnetic flux is done in room temperature to determine parameters for use in the empirical Steinmetz equation in (4.2). Measurement parameters and results are shown in Table 4.2.

$$P_{fe} = K_c f^\alpha B_{max}^\beta \quad (4.2)$$

The coefficients are calculated in (4.3), (4.4) and (4.5).

$$\alpha = \frac{\ln\left(\frac{P_C}{P_A}\right)}{\ln\left(\frac{f_C}{f_A}\right)} = 2.37 \quad (4.3)$$

$$\beta = \frac{\ln\left(\frac{P_B}{P_A}\right)}{\ln\left(\frac{B_B}{B_A}\right)} = 2.79 \quad (4.4)$$

$$K_c = \frac{P_C}{f_C^\alpha B_C^\beta} = 1.47 \times 10^{-13} \quad (4.5)$$

Which results in the following equation for calculating core loss in room temperature:

$$P_{fe} = 1.47 \times 10^{-13} \times f^{2.37} B_{max}^{2.79} \quad (4.6)$$

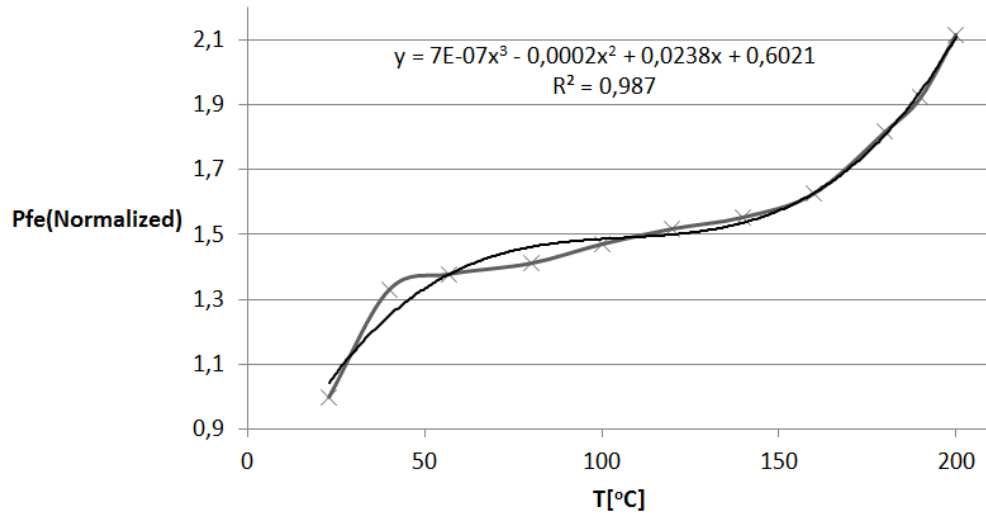


Figure 4.7: Measured normalised core loss as a function of temperature at $f = 6$ MHz and $B_{max} = 35$ mT.

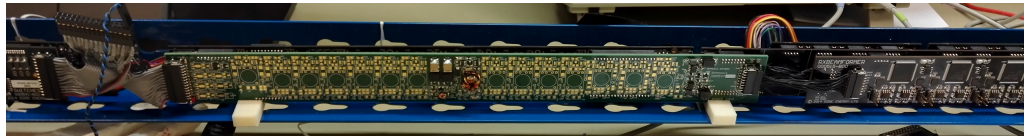


Figure 4.8: Transmitter prototype connected to complete UIP tool.

To determine the coherence between core loss and temperature, the same test was done at a constant frequency of 6 MHz, maximum flux density of 35 mT and a varying temperature from 23 °C to 200 °C.

Measured core loss as a function of temperature is normalized to $P_{fe} = 1$ at 23 °C. By using Microsoft Excel to perform a polynomial regression on the relationship between temperature and normalized core loss, a third degree polynomial with a chi squared value of 0.987 is found. The polynomial is shown in (4.7), while the graph of normalized core loss together with the polynomial is shown in Figure 4.7.

$$P_{fe_{norm}}(T) = 7 \times 10^{-7}T^3 - 2 \times 10^{-4}T^2 + 2.38 \times 10^{-2}T + 0.602 \quad (4.7)$$

4.3 System Test

The transmitter circuit is connected to a complete UIP imaging tool, as shown in Figure 4.8. The system is set up with a transducer type 6071. Both channels are connected to two transducer elements each. Measured output voltage is shown as a function of frequency in Figure 4.9.

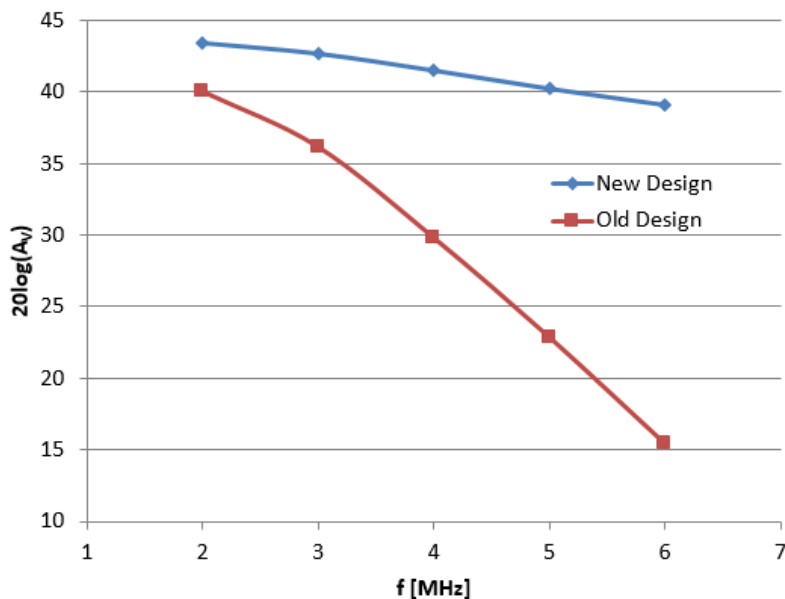


Figure 4.9: Measured voltage amplification as a function of frequency at $V_{in} = 1 V_{pp}$.

The old design shows a reduction of 25 dB from 2 MHz to 6 MHz, while the new design only shows a reduction of 4 dB.

4.4 Linearity Characterization

Non-linearity makes it more complex to accurately control the output voltage, and it is important to characterize it. Linearity of both the old and new design is tested with the full dummy load proposed in section 2.1. The input signal is varied from $0.1 V_{pp}$ to $2.0 V_{pp}$ in steps of $0.1 V_{pp}$ at the center frequency of 4 MHz.

The peak to peak output signal was measured and used to calculate the voltage amplification. The amplification of the transmitter circuit is dependent on the input voltage, as shown in Figure 4.10a and Figure 4.10b. Amplification values used in later graphs are maximum values if not anything else is specified.

The new design show a gain variation of only ± 1.7 dB with an input signal amplitude from $0.8 V_{pp}$ to $2.0 V_{pp}$. The old design show a gain variation of ± 4.3 dB within the same input range.

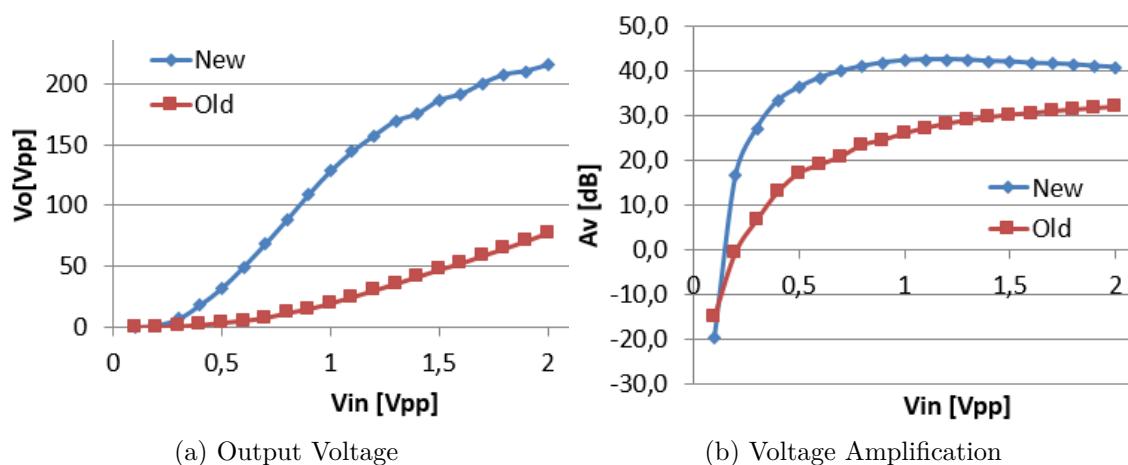


Figure 4.10: Output voltage and amplification as a function of input voltage at 4 MHz.

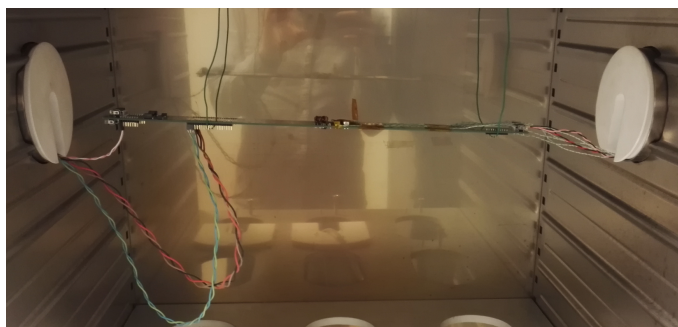


Figure 4.11: Test setup for testing in high temperature. Input signal and power connected to the left, temperature probes and load to the right.

4.5 Temperature Test

Both channels on the prototype transmitter board were tested up to a temperature of 180 °C. Rate of temperature was limited below 2 °C/ min to avoid thermal shock for the ferrite cores, as described in Appendix A. After reaching 180 °C the temperature was kept constant for 2 hours while testing. Test setup is shown in Figure 4.11.

The load model for switches shown in 2.5 was used, replacing the capacitor values of 436 pF with 470 pF and 352 pF with 330 pF. Two dummy transducer elements were connected to the switch, each consisting of a 270 pF capacitor in series with a 27 Ω resistor. This represents the load a transmitter will experience when used with a type 9887 transducer used for thickness measurements.

Temperature probes are placed at the components expected to have the highest temperature rise, and one probe is used for measuring the air temperature. The transformer, operational amplifier and the output transistors are all monitored.

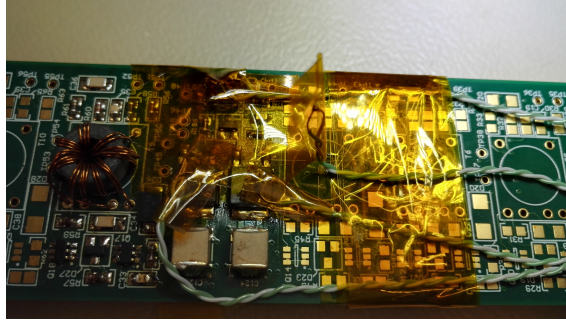


Figure 4.12: Temperature probes attached to the PCB with Kapton tape.

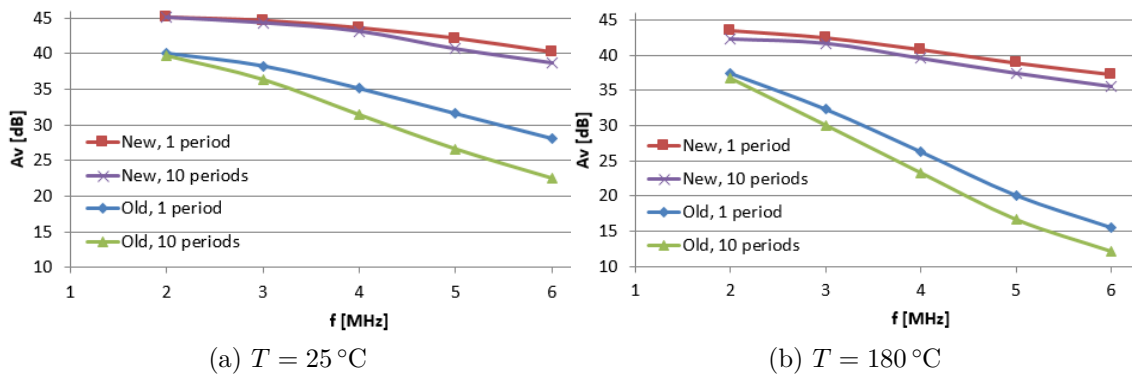


Figure 4.13: Measured frequency response of the old and new transmitter.

Temperature probes attached to the board with Kapton tape are shown in Figure 4.12.

Measurements show a great difference between the original transmitter and the new prototype. The maximum voltage amplification at each frequency is shown in Figure 4.13a for $T = 25\text{ }^{\circ}\text{C}$ and in Figure 4.13b for $T = 180\text{ }^{\circ}\text{C}$. Measurements are done with one or 10 sine periods, repeated after a delay of $347\text{ }\mu\text{s}$. The delay is calculated for a frame rate of 10 frames per second and a number of elements equal to 288.

Measurements also show a small difference of approximately 1 dB to 2 dB between single period and 10 period signals. This is also seen at the first period of the 10 period signals, and happens because the output transistor first activated only needs to charge the load from 0 V to 100 V instead of from -100 V .

Maximum amplification is shown as a function of temperature in Figure 4.14, where a signal of 10 periods is used. It shows a variation in amplitude of 2.6 dB to 3.6 dB over a temperature range of $25\text{ }^{\circ}\text{C}$ to $180\text{ }^{\circ}\text{C}$.

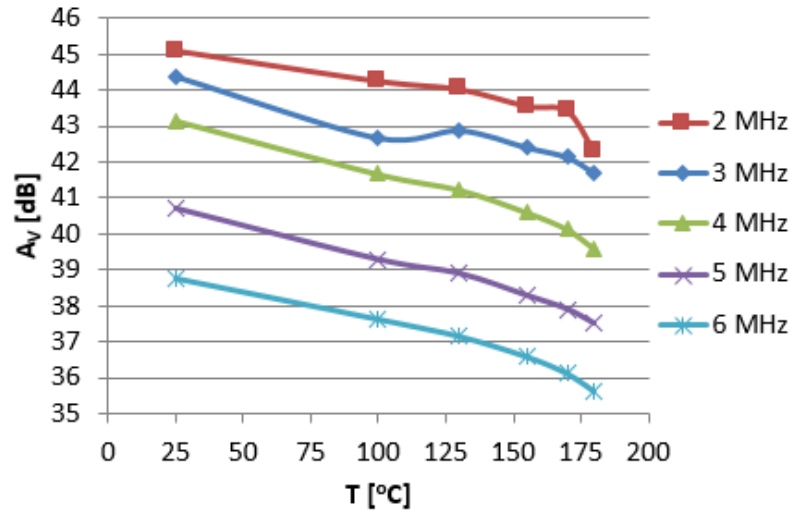


Figure 4.14: Maximum amplification for ten period signals at 2 MHz to 6 MHz as a function of temperature.

4.6 Temperature Rise

The temperature rise of the operational amplifier, transformer and output transistors is monitored during the temperature test. This is done to discover which components experience the highest temperature and to be able to define operational limits for each component.

4.6.1 Output Transistors

Dissipated power in each transistor is calculated by replacing the voltage change in (2.15):

$$P_{switching} = \frac{n_{pulse}}{T_{ping}} CV_{DD} V_{O_{p-p}} \quad (4.8)$$

Thermal resistance from case to ambient is calculated for the output transistors by using measured temperature rise at six different scenarios in Table 4.3. Calculated thermal resistance is far lower than the 110 °C/W from the datasheet. The calculated thermal resistance when the fan is off, is 24 °C/W for the NMOS transistor and 23 °C/W for the PMOS transistor. The differences in thermal resistance between PMOS and NMOS transistors is due to the difference in voltage swing, as the output swing is not symmetrical around 0 V.

Table 4.3: Calculated thermal resistance for output transistors

n_{pulse}	$V_{O_{p-p}}$	Air Fan	ΔT_{nmos}	ΔT_{pmos}	P_D	$R_{\theta JA_{nmos}}$	$R_{\theta JA_{pmos}}$
10	173	Off	22	20	0.90	24	23
10	152	On	11	13	0.79	14	16
10	144	On	9	11	0.75	12	15
10	135	On	7	10	0.70	10	14
10	128	On	6	9	0.66	9	14
10	121	On	6	8	0.63	10	13
16	176	On	13	18	1.46	9	12

4.6.2 Transformer

Choosing a wire diameter of 0.16 mm and number of turns as $N_P = 10$, $N_{S_N} = 20$ and $N_{S_P} = 25$ leads to the following parameters.

$$MLT = \pi(1.16 \times 10^{-3} \text{ m} + 0.08 \times 10^{-3} \text{ m}) = 4.14 \times 10^{-3} \text{ m} \quad (4.9)$$

DC resistance per turn as a function of temperature in celsius:

$$\begin{aligned} \frac{R_{DC}}{N} &= \frac{MLT \times \rho_{20} \times [1 + \alpha(T - 20)]}{\pi r_w^2} \\ &= 3.5 \text{ m}\Omega \times [1 + 3.9 \times 10^{-3}/^\circ\text{C}(T - 20)] \end{aligned} \quad (4.10)$$

Primary winding current calculated with typical values for gate to source capacitance, $C_{gs_n} = 223 \text{ pF}$ and $C_{gs_p} = 315 \text{ pF}$.

$$\begin{aligned} I_P &= \frac{I_{S_n} N_{S_n} + I_{S_p} N_{S_p}}{N_P} \\ &= \frac{2\pi f (V_{S_N} C_{gs_n} N_{S_N} + V_{S_P} C_{gs_p} N_{S_P})}{N_P} \\ &= \frac{2\pi f V_P (N_{S_N}^2 C_{gs_n} + N_{S_P}^2 C_{gs_p})}{N_P^2} \\ &= 1.80 \times 10^{-8} \times f V_P \end{aligned} \quad (4.11)$$

The skin effect factor is calculated and listed in Table 4.4 for tested temperatures and a frequency of 6 MHz.

To calculate the proximity effect factor the effective conductivity and skin depth needs to be calculated. Effective conductivity is calculated as a function of number

Table 4.4: Calculated skin effect factor for signal frequencies at 20 °C and 200 °C.

T [celsius]	Skin Depth [μm]	Skin Effect Factor
42.5	27.9	1.71
113	31.3	1.57
138	32.4	1.52
163	33.4	1.49
176	34.0	1.47
187	34.4	1.45

Table 4.5: Proximity effect factor at a frequency of 6 MHz.

T [celsius]	Δ		Proximity Effect Factor	
	Primary	Secondary	Primary	Secondary
42.5	2.4	3.5	2.3	11.2
113	2.1	3.2	2.0	10.1
138	2.0	3.1	1.9	9.8
163	2.0	3.0	1.9	9.4
176	1.9	2.9	1.8	9.3
187	1.9	2.9	1.8	9.1

of windings and temperature in (4.12).

$$\begin{aligned}\sigma_w &= \eta\sigma = \frac{Nd}{w}\sigma = \frac{N\sqrt{\frac{\pi}{4}}D_{wire}}{\pi(D_{core_{inner}} - D_{wire})}\sigma \\ &= N \times \frac{1.28 \text{ M}\Omega^{-1} \cdot \text{m}^{-1}}{[1 + 3.9 \times 10^{-3}/^{\circ}\text{C}(T - 20)]}\end{aligned}\quad (4.12)$$

Effective skin depth:

$$\begin{aligned}\delta_w &= \frac{1}{\sqrt{\pi f \mu_0 \sigma_w}} \\ &= 0.445 \sqrt{\frac{[1 + 3.9 \times 10^{-3}/^{\circ}\text{C}(T - 20)]}{fN}}\end{aligned}\quad (4.13)$$

Proximity factor is calculated and listed in Table 4.5 for frequencies within the signal bandwidth.

Copper loss is calculated as a function of primary voltage and temperature is calculated in (4.14). A number of ten primary windings and a frequency of 6 MHz is used in the calculations.

$$P_{cu} = I_{rms}^2 R_{dc} K_s K_p \quad (4.14)$$

Table 4.6: Core loss and transformer temperature rise as a function of temperature.

$T_{transformer}$	P_{fe} [mW]	P_{cuP} [mW]	P_{cuS} [mW]	P_{tot} [mW]	ΔT_{calc}	ΔT_{meas}
42.5	0.04	0.09	0.39	0.53	1	15
113	0.06	0.09	0.41	0.55	2	9
138	0.06	0.09	0.41	0.56	2	8
163	0.07	0.09	0.41	0.57	2	7
176	0.08	0.09	0.41	0.58	2	6
187	0.09	0.09	0.41	0.59	2	6

Core loss as a function of temperature is calculated by combining (2.37), (2.38) and (4.7).

$$\begin{aligned}
 P_{fe}(T) &= 1.47 \times 10^{-13} \times f^{2.37} \times B^{2.79} \times P_{fe_{norm}}(T) \\
 &= 45.3 \times 10^{-3} f^{-0.42} V_P^{2.79} \times P_{fe_{norm}}(T)
 \end{aligned} \tag{4.15}$$

Calculated core loss and transformer temperature rise is listed in Table 4.6 and compared to measured values. Input signals of $V_{in} = 1$ V and $f = 6$ MHz is used.

The measured transformer temperatures are very different from calculated values. The core loss has been measured at flux densities of 35 mT and 70 mT, while the temperature rise has been measured at a flux density of 12 mT. This could have resulted in wrong coefficients for calculating core loss and needs to be retested at a lower flux density.

4.7 Single Period Test

A test is performed with a single period sine to measure pulse duration. The input signal has a frequency of 4.2 MHz and an amplitude of $1.5 V_{pp}$.

The output signal of a single period sine is shown in Figure 4.15a. This shows a correct sine signal until the output reaches its peak positive value and the input signal is turned off. From this point the charged load capacitance will release its charge through the resistance to ground. This results in a natural response shown in Figure 4.15a.

The pulse duration can be reduced by extending the input signal to 1.25 periods, allowing the output transistors to conduct until the output voltage has reached 0 V. The output signal measured with a 1.2 period input signal is shown in Figure 4.15b. Measured fall time is reduced from 158 ns to 31 ns, while the amplitude is slightly decreased.

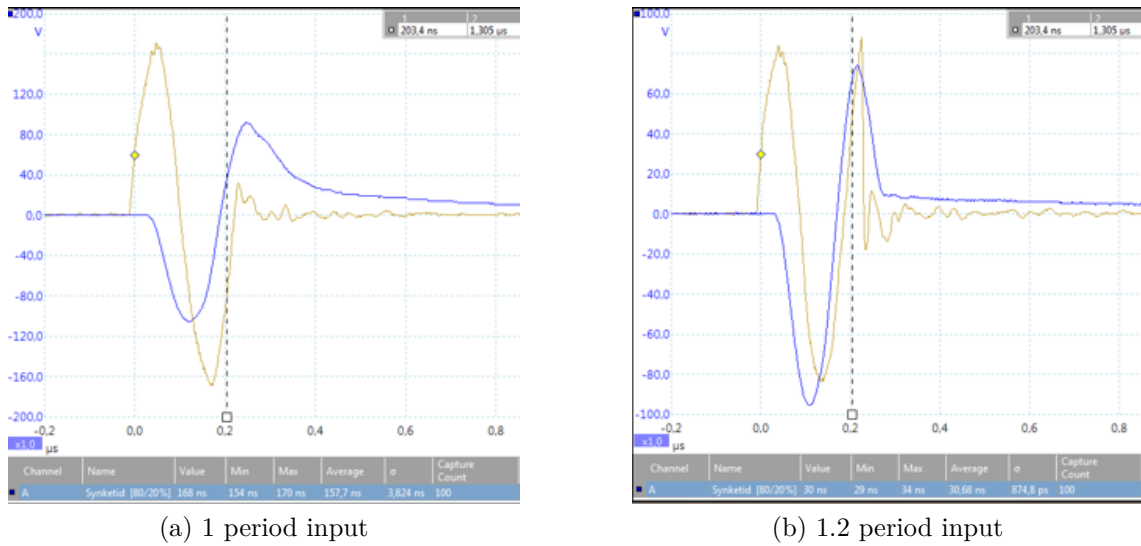


Figure 4.15: Measured output voltage (blue) of a single sine input (yellow) at $f = 4$ MHz. The y-axis range is ± 200 V in (a) and ± 100 V in (b).

4.8 Amplifier Filter

Due to the fact that the amplification is higher than needed for low frequencies, a high-pass filter characteristic can be implemented for the operational amplifiers to obtain a flatter frequency response within the signal bandwidth. Simulations show that a cutoff frequency around 3 MHz will suffice.

A 100 pF C0G capacitor, type C0603H101J5GACTU with a maximum operational temperature of 200 °C is used in the filter. Resistors are replaced for $R_G = 510 \Omega$ and $R_F = 1.2 \text{ k}\Omega$ to obtain a cutoff frequency at 3.1 MHz and an amplification of 5.71 V/V. Measured amplification for the new transmitter at an input voltage of 0.5 V and a load capacitance of 1.8 nF is shown in Figure 4.16. This input voltage is chosen to avoid saturation levels.

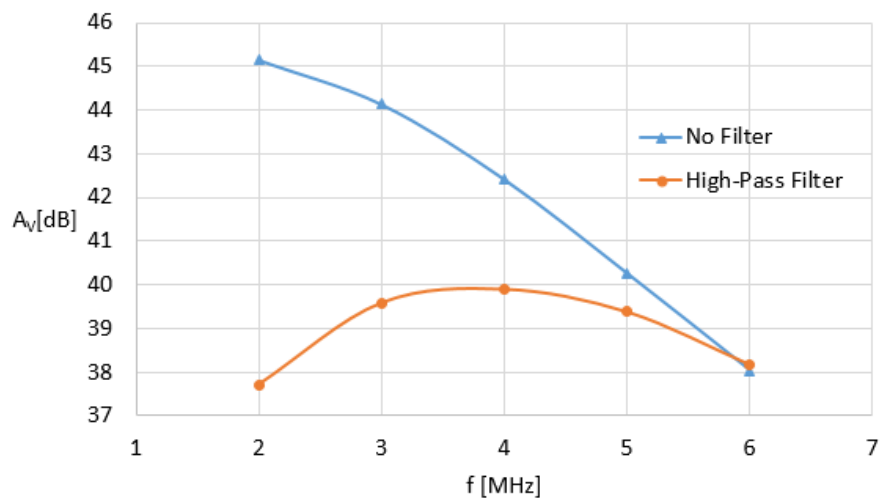


Figure 4.16: Measured amplification with and without high-pass filter

Discussion

This chapter discusses what is achieved throughout the thesis compared to the original design and the design requirements stated at the start of the thesis. The consequences of the results are evaluated, and further improvements are proposed if needed.

5.1 Results

A main goal has been to achieve a maximum output amplitude of $200 V_{pp}$ over the entire bandwidth, as this is the maximum supply voltage. Tests show that the maximum output signal at 6 MHz and 180°C is $121 V_{pp}$. This is still much higher than the original design and is mostly due to the current capabilities of the output transistors.

A further increase in output current capability will result in a decreased number of channels due to larger transistors. It will also cause a more capacitive load for the operational amplifier, increasing the current demand and power dissipation in the operational amplifiers and the transformer.

The output current can be slightly improved by setting the DC-level of the input signal to 0 V and increasing gain in the operational amplifier. This will increase the power dissipation in the operational amplifiers and the transformer, and has to be tested to verify that it can operate at a higher case temperature than already tested.

A new switch with less capacitance is proposed in the analysis chapter. The switches are responsible for most of the capacitance at the output, which is the main factor for both slew rate requirements and power dissipation in the output stage. The two

datasheets show identical properties except for the capacitance values and is omitted from the thesis due to the need for high temperature verification before it can be implemented. This is an independent upgrade that can and should be performed after the thesis.

Area is scarce in this design, and a major improvement done in the thesis is replacing the original ferrite core to reduce area by 1.1 cm^2 . Tests show that the replacement core has an expected functionality, but care has to be taken to not overheat the core. An overheated core will result in reduced permeability, causing more leakage flux and thus reducing the voltage at the secondary windings.

Linearity of the transmitter circuit has been improved both as a function of input signal and frequency, making it less complex to control the output signal amplitude. Due to the highly capacitive load and small area available, perfect linearity is a difficult goal. By implementing a high-pass filter in the operational amplifiers, a better linearity can be achieved by reducing amplification in the lower end of the signal bandwidth. It is not implemented due to the fact that it will reduce output signal amplitude below the requirement for more frequencies, but can be implemented if amplification at the upper frequency meets the requirements in the future.

5.2 Test Setup

The temperature tests are performed with a flow of air that will not exist in the tool casing, improving the thermal conductivity between components and ambient air. The test has been performed according to BTC guidelines to obtain comparable results with tests done on other boards. When the tool is immersed in oil at a maximum temperature of $177 \text{ }^\circ\text{C}$ (official specification), the inside should only differ by a few degrees. A high thermal resistance can be achieved for the most critical components by thermally connecting them to the inner tool casing.

Temperature measurements on output transistors and ferrite cores is different than what was calculated in the analysis chapter. For the output transistors, thermal resistance was calculated for an ideal heat sink as well as for a minimum pad and still air. The measured temperatures is used to calculate thermal resistance for this specific board, giving valuable experience for choosing components in the future.

The tests done on temperature rise of the transformer ferrite core is very different from the calculated values. This can be due to the fact that the coefficients for calculating core loss is collected at higher flux densities than what is used in the temperature test. New tests should be performed at relevant flux densities to be able to more accurately predict the temperature rise of the transformer.

TVS diodes are installed to protect the output transistors from transient voltages caused by the transformer. A specific test for the TVS diodes has not been per-

formed, but they have been installed while testing up to 180 °C, and the transistors have not shown any signs of failure.

When soldering on components for two channels on the board, both channels will share the parallel decoupling capacitance. The decoupling capacitance has therefore not been tested specifically in this design, and should rather be tested by comparing two separate boards with all channels installed. It should also be tested with the actual power supply unit and power lines.

This thesis has not focused on a complete reliability test, but tests have verified the ability for continuous use for at least two hours in 180 °C. To get reliable data on operational lifetime of the transmitter, several boards should be tested until failure. This will give an indication of transmitter life time at high temperatures and failures will expose the weakest links, providing essential information for improving reliability.

Conclusion

Frequency response of the transmitter has been greatly improved in the new design, verified in tests up to 180 °C. Amplification at 6 MHz and 180 °C has been increased from 12 dB in the original transmitter to 36 dB in the new design. This is achieved without any increase in board size.

For thickness measurements where the signal is a single period, maximum amplification is increased to 37 dB, which is 22 dB higher than the original design. This substantially improves the thickness measurement accuracy. As a further improvement, a new method for reducing output pulse length is proposed and verified in testing. This is easily implemented in software, and improves the axial resolution for both thickness measurements and imaging with signals of more than one period.

Several tradeoffs between reliability of the electronics and imaging parameters have been identified. Case temperature of critical components are strongly dependent on the number of pulses in a burst as well as frame rate and number of elements. The product of these parameters need to be limited to maintain reliability at increased ambient temperatures.

Transformer Loss Theory

The explanations on transformer loss in this section is largely based on information found in *Transformers and Inductors for Power Electronics: Theory, Design and Applications* [7]. Transformer loss includes copper loss, hysteresis, eddy current and residual loss in the core.

Losses contribute to a temperature increase in the core and needs to be limited to avoid reaching the Curie temperature. At the Curie temperature the thermal agitation is great enough to cause a random orientation of the magnetic moments and the substance becomes paramagnetic [19, p. 921]. The temperature increase is dependent on the core surface area, as seen in the empirical (A.1), supplied by Magnetics Inc [17]. P_D includes both copper loss and core loss and the equation assumes still air at room temperature.

$$\Delta T = \left(\frac{P_D [\text{mW}]}{A_s [\text{cm}^2]} \right)^{0.833} \quad (\text{A.1})$$

A.1 Skin Effect

Operating the transformer at high frequencies increase the winding losses by introducing eddy currents in the windings. An isolated round conductor carrying alternating current generates a concentric alternating magnetic field which, in turn, induces eddy currents in accordance with Faraday's law. These eddy currents oppose the flux, which results in canceling some of the current in the center of the conductor and increasing the current near the surface.

This decreases the effective cross-sectional area of the conductor, thus increasing the

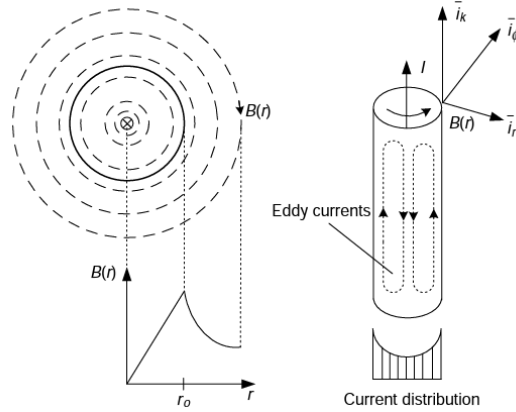


Figure A.1: Magnetic field and resulting eddy currents in a circular conductor [7].

resistance. The skin effect factor, k_s , is calculated by the approximations in (A.2).

$$k_s = \begin{cases} 1 + \frac{\left(\frac{r_0}{\delta_0}\right)^4}{48 + 0.8\left(\frac{r_0}{\delta_0}\right)^4} & \text{if } \frac{r_0}{\delta_0} < 1.7 \\ 0.25 + 0.5\left(\frac{r_0}{\delta_0}\right) + \frac{3}{32}\left(\frac{\delta_0}{r_0}\right) & \text{if } \frac{r_0}{\delta_0} > 1.7 \end{cases} \quad (\text{A.2})$$

Where δ_0 is the skin depth of the conducting material, calculated in (A.3).

$$\delta_0 = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \quad (\text{A.3})$$

A.2 Proximity Effect

Proximity effects occur when two conductors are in such close proximity that the current distribution in one conductor is influenced by the current distribution in the other conductor. The resulting proximity factor between AC and DC resistance for sinusoidal excitation is calculated by using Dowell's formula in (A.4).

$$k_p = \Delta \left[\frac{\sinh 2\Delta + \sin 2\Delta}{\cosh 2\Delta - \cos 2\Delta} + \frac{2(p^2 - 1)}{3} \frac{\sinh \Delta - \sin \Delta}{\cosh \Delta + \cos \Delta} \right] \quad (\text{A.4})$$

Where p is the number of layers and Δ is the ratio of the layer thickness d to the skin depth δ_0 . The formula is derived for foil layers which extend to the full height of the window. Windings consisting of N round conductors within a layer can be

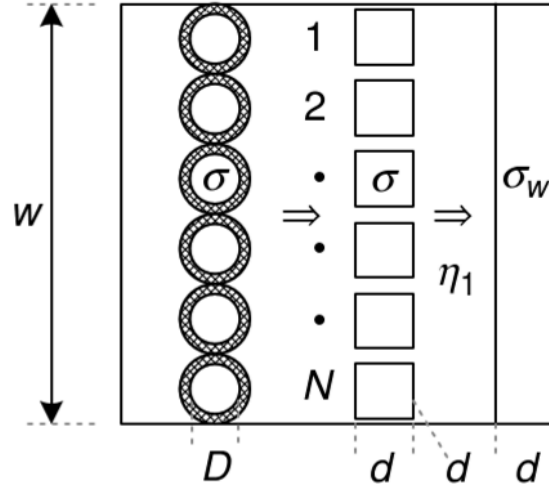


Figure A.2: Conversion of circular conductors [7].

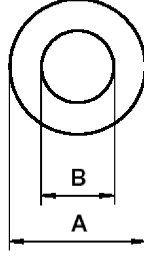


Figure A.3: Illustration showing inner and outer diameter of ferrite core [15].

treated as N foils with equivalent thickness $d = \sqrt{\frac{\pi}{4}}D$ and effective conductivity $\sigma_w = \eta\sigma$. The conversion process is shown in Figure A.2.

η is called the porosity factor and is calculated in (A.5).

$$\eta = \frac{Nd}{w} \quad (\text{A.5})$$

Where w is the window width, calculated in (A.6).

$$w = \pi(D_{core_{inner}} - r_{wire}) \quad (\text{A.6})$$

Inner core diameter used in the calculations is shown as B in Figure A.3.

The porosity factor is used to calculate the effective conductivity in (A.7).

$$\sigma_w = \eta\sigma \quad (\text{A.7})$$

The effective skin depth is then calculated in (A.8).

$$\delta_w = \frac{1}{\sqrt{\pi f \mu_0 \sigma_w}} \quad (\text{A.8})$$

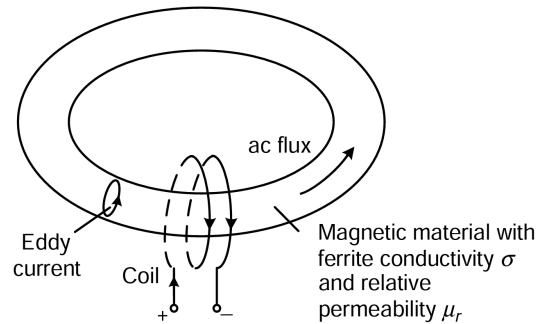


Figure A.4: Eddy current loss in a toroidal core [7].

A.3 Core Loss

A part of the power applied to the transformer is lost in the core, dissipated as heat and sometimes noise. The alternating magnetic flux induces eddy currents with its direction such that it will oppose the change that produced it. This is in accordance with Lenz's law and shown in Figure A.4.

Datasheets

This chapter includes relevant data collected from datasheets.

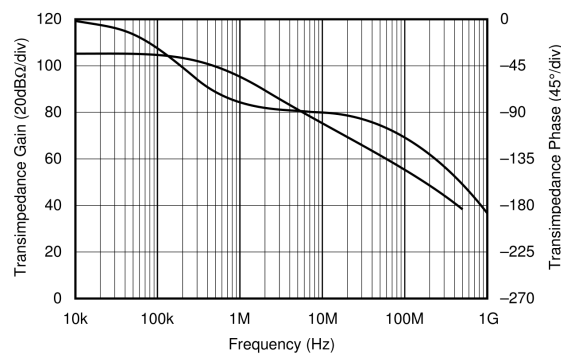


Figure B.1: Open-Loop Transimpedance Gain and Phase of OPA2677 [23].

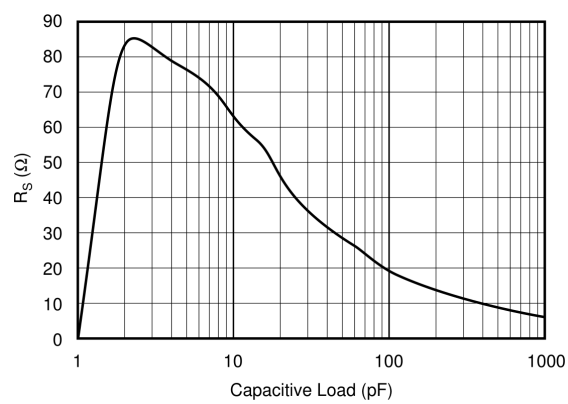


Figure B.2: Recommended R_S vs Capacitive Load [23].

Measurements

This chapter includes oscilloscope images taken while testing the new transmitter at 180 °C. The blue signal is measured at the output of the transmitter, while the red signal is measured over the dummy transducer. The yellow signal is the input signal.

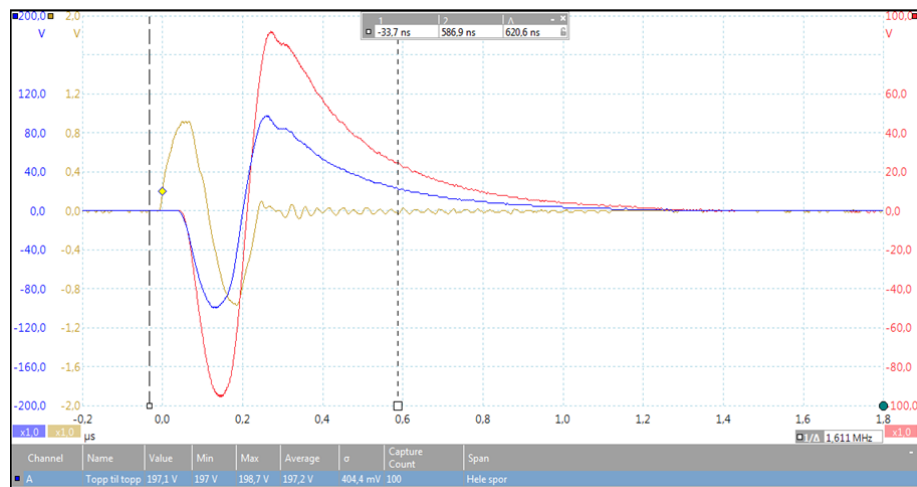


Figure C.1: One period input signal at 4 MHz and $1.8V_{pp}$.

APPENDIX C. MEASUREMENTS

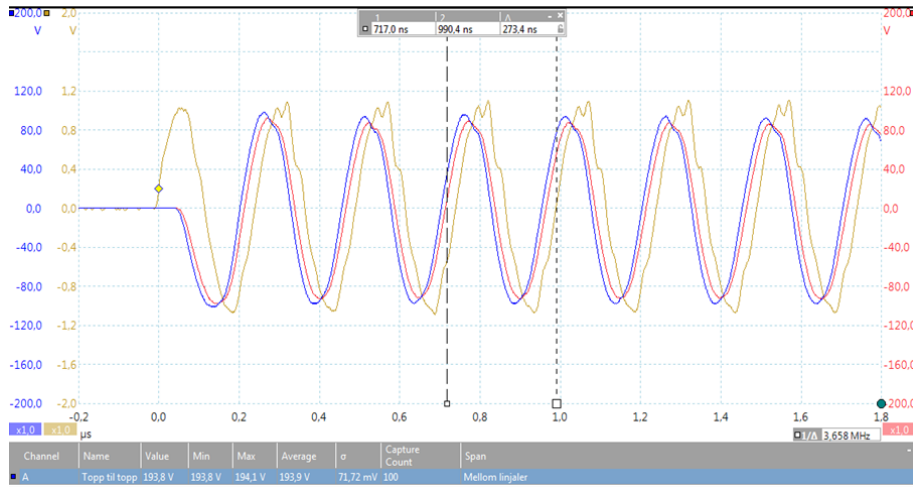


Figure C.2: Ten period input signal at 4 MHz and $2.0 V_{pp}$.

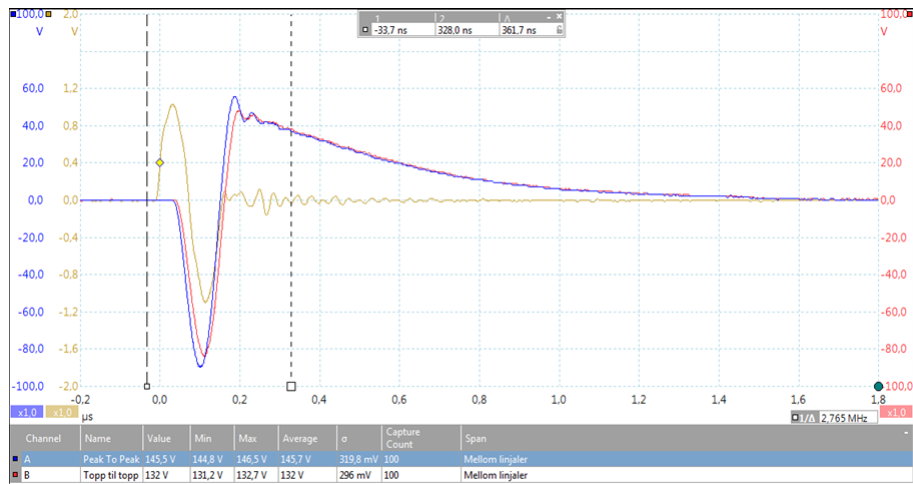


Figure C.3: One period input signal at 6 MHz and $2.0 V_{pp}$.

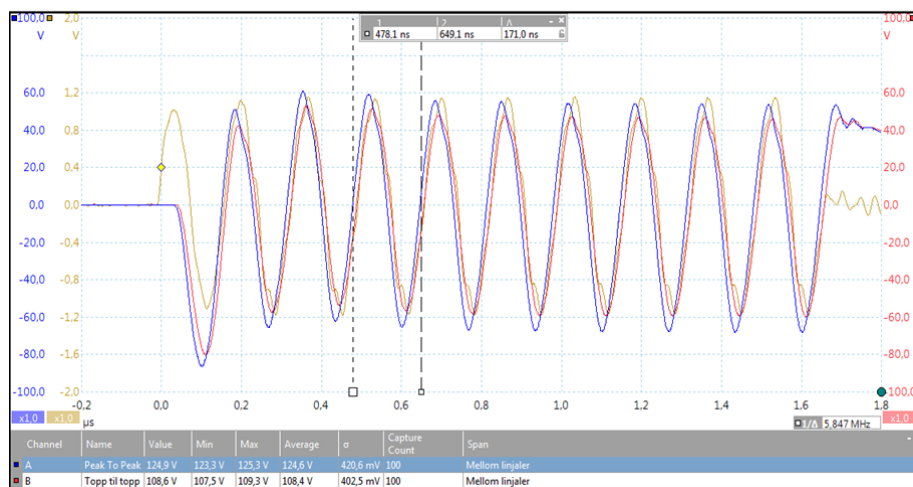


Figure C.4: Ten period input signal at 6 MHz and $2.0 V_{pp}$.

Abbreviations

BTC	Bergen Technology Center
BW	Bandwidth
CFA	Current Feedback Amplifier
DAC	Digital to Analog Converter
HSOP	Heatsink Small Outline Package
MLT	Mean Length of Turn
PCB	Printed Circuit Board
QFN	Quad Flat No Leads Package
QFP	Quad Flat Package
SR	Slew Rate
TVS	Transient Voltage Suppression
UIP	Ultrasound Imaging Platform

ABBREVIATIONS

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