Design Of a 60 GHz VCO Hybrid Microstrip Resonator in a 0.13-μm SiGe Process

A thesis by

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Abstract

Augmented reality, 4K television and video gaming. These are just some examples were the wireless products lacks performance in terms of multi-gigabit data transfers. A solution to this challenge is the **60 GHz band**. The 60 GHz band is able to support high data rates, ranging from **2-20 Gbps** with bit-error rate less than $\mathbf{10^{-12}}$ [36, 8, 37, 19, 5].

A proposal for a transceiver chip, supporting data rates above **5 Gbps** has been designed here at the University of Bergen. For this thesis a **Voltage Controlled Oscillator** (VCO), with a fundamental oscillating frequency of **61.5 GHz** has been designed and verified with EM-structures and corner analysis. Simulation results for the VCO yields, **-79 dBc/Hz at 1 MHz Offset** Single Sideband phase noise (SSB), **19.5 mW** Total Power Dissipation (TPD), **-10 dBm** Output Power (Ps) and **2.5 GHz** tuning range. The VCO is classified as a single ended **Hybrid Microstrip Resonator.** To our knowledge, this oscillator has never been designed at frequencies this high.

The applied design technique is a open-loop cascade, **2-port method**. This method along with Leeson's Phase Noise formula for the open-loop cascade [11] was used to develop a **9-Step-Method**. This method shows how to calculate SSB, loaded Q, Output Power and Gain Margin based on the open-loop cascade. It was then used to exhibit a thorough analysis of the npn13p transistor with various types of resonator setups. The npn13p is a heterojunction bipolar transistor (HBT) which is provided by the **0.13 µm SiGe BiCMOS** process from IHP (SG13s). It has a high f_t of **250 GHz** which makes them ideal for operating in the V-band.

All critical components and microstrip lines where build using **EM-structures** to validate results. The VCO was also verified in all corners, sweeping the temperature from $\mathbf{0 - 140^{\circ}}\boldsymbol{C}$. A total of **0.17 mVrms** with **white noise** was also added to the supply voltage nodes. Simulation results from the corner analysis showed that the VCO had a maximum SSB of **-75 dBc/Hz at 1 MHz Offset** below $\mathbf{100^{\circ}}\boldsymbol{C}$.

Preface

This work has been carried out between August 2016 and June 2017 at the University of Bergen (UiB), in a collaboration with Hans Kristian Soltveit at the Physikalisches Institut, Heidelberg University. The work on the 60 GHz transceiver chip started in August 2015 by former students, Magnus Pallesen and Hans Schou who designed a Low Noise Amplifier and a Power Amplifier recpectivly.

My past experience mainly revolved around low frequency analog design. Oscillator design, microwave engineering and EM-simulation were new subjects to me. Much of the work related to this thesis was therefore dedicated to learning about the different subjects. Luckily Magnus R. Ersdal, a fellow studen, was working with EM-simulations to verify earlier work on the Low Noise Amplifier and Power Amplifier using Microwave Office. This and the fact that two thesis already had been written on the subject made it easier to address certain challenges. In summary this led to a very educational experience learning about oscillators, microwave engineering, layout and EM-simulations.

Acknowledgment

First I would like to thank my supervisor **Kjetil Ullaland** at the University of Bergen for guidance and good advice based on his vast experience in electronics.
I would also like to show my gratitude to **Hans Kristian Soltveit** for his expert advice in RF and IC design, he has also been an inspiration with his passion to commercialize the 60 GHz band.
Thanks to **Yngve Thodesen** at the Royal Norwegian Naval Academy for his expertise in RF design and for always showing great interest.
A special thanks to **Magnus R. Ersdal** for the collaboration throughout the whole year and for his advice in EM-simulations.
I would also like to thank my fellow students for good laughs and discussions at the office.
Last but not least, I would like to thank my family for great support and inspiration.

Contents

Chapter 1

Introduction

People do not like wires! They are old fashion and if we had the choice to remove them, we would. What we do like, is transferring huge amounts of data, wireless, in a blink of an eye. The only problem with wireless products, like Bluetooth and Wi-Fi standards [35, 24, 12], is that the data rates are bandwidth limited and everyday the technology is constantly moving forward. Because of this, the demands for high speed wireless solutions is exceeding the capacity of these products and wires is left as the only solution [28, 7].

Some of these areas might be,

- Docking between devices like smartphones, laptops, external hard drive, projectors, blue-ray, decoders and tablets
- Streaming ultra-high definition videos/movies, full HD or 4K
- Gaming, augmented reality and virtual reality
- Fast download of HD movies
- Public kiosk services

In order to replace cables with wireless connections for these services, data rates exceeding 2 Gbps would be the minimum demand and somewhere between 5-10 Gbps would be preferred [7]. The most commonly used Wi-Fi standard, IEEE standard 802.11n, can deliver a maximum data rate of 600 Mbps and uses 2.4 GHz and 5 GHz [7].

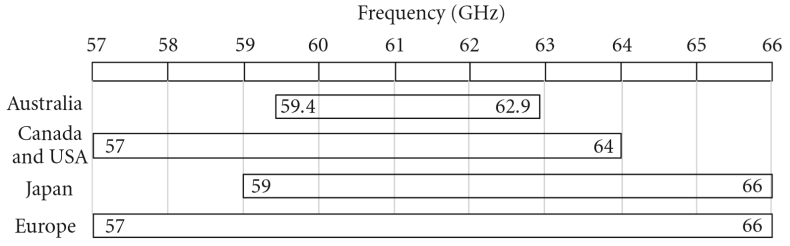


Figure 1.1: Worldwide commercial frequency bands in 60 GHz [7].

In may 2009, a bandwidth of 9 GHz in the 57-66 GHz range, Figure 1.1, was opened by the European Telecommunications Standards Institute (ETSI) for unlicensed use over the European Union [7].

Some of the R&D that has been done in the 60 GHz band shows very promising results, with data rates ranging from 2-20 Gbps and with bit-error rates (BER) lower then 10^{-12} [36, 8, 37, 19, 5]. This is more than enough to support uncompressed full-HD video format [7]. The technology has also been implemented in the Wi-Fi standards, namely the IEEE standard 802.11ad. It uses 60 GHz as the carrier frequency and supports data rates up to 7 Gbps [26, 28].

The 60 GHz band also contains features like [29],

- **High frequencies:** This leads to smaller components, less area usage, lower power consumption and smaller antennas.
- **Low interference**: Makes it possible to send multiple signals in a high density channel. This makes it a good candidate for Multiple-Input Multiple-Output (MIMO).
- **Unlicensed use:** A total of 3.5-9 GHz bandwidth for unlicensed use world wide makes it easier to commercialize.

1.0.1 Signal Attenuation

The main challenge with using 60 GHz as carrier frequency is a high signal attenuation. This will put some restrains on the transferring distance. To illustrate this we use the Friis equation, eq.1.1.

The Friis equations shows the maximum power received by an radio antenna, Figure 1.2.

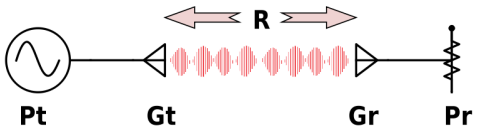


Figure 1.2: The consept of received power, based upon the Friis eq.1.1.

$$P_r = \frac{G_t G_r \lambda^2}{(4\pi R)^2} P_t \, W \tag{1.1}$$

- P_t is the transmitted power
- G_t is the gain for the transmit antenna
- R the distance between the receive and transmit antennas

- G_r is the gain for the receive antenna
- P_r is the received power delivered to a matched load
- $\lambda = c/f$, wavelength.

From eq.1.1 it can be shown that the power received by the antenna is proportional to $\frac{1}{R^2 f^2}$ given that the antenna gains and transmit power are constant. This means that doubling the frequency shortens the transmitting distance by a factor 2, given the same received power.

1.1 60 GHz Radio System

There are many different ways to design a radio system. For a 60 GHz Radio Frequency (RF) system some modulation schemes are more favorable than others because of phase noise related issues. Phase noise represent the amount of phase drift from the fundamental frequency in a oscillator. In digital circuits phase noise is referred to as jitter to the reference clock. In analog systems, phase noise limits the quality or resolution for a given type of modulation scheme.

A modulation technique that is prone to phase noise is the Offset Quadrature Phase-Shift Keying (OQPSK). In Figure 1.3 the BER is plotted versus distance using different levels of phase noise. We can see that if OQPSK where to be used at 60 GHz, the phase noise should be less then -90 dBc @ 1 MHz. Normal values for phase noise at 60 GHz is approximately -85 dBc/Hz at 1 MHz Offset [7]. For this reason it might not be the first choice in modulation scheme when designing a transceiver for 60 GHz .

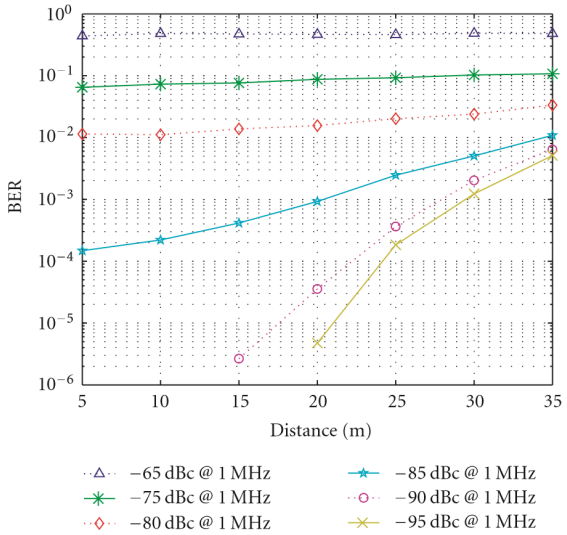


Figure 1.3: BER versus distance for different levels of phase noise [7].

A technique that is not so prone to phase noise is On-Off Keying (OOK). OOK is a single carrier modulation scheme and can support 2 Gbps over an Line Of Sight (LOS) link

with 2-GHz bandwidth [3]. If larger bandwidth is used, data rates exceeding 10 Gbps with $BER \leq 10^{-12}$ has been achieved in earlier work [36, 5, 37]. The OOK scheme can also use non-coherently detection (envelope detection) at the receiving end of the radio system [17]. This means, no need for phase alignment at the receiver, fewer components, less area usage, better yield, lower power consumption and cost.

OOK is also known as Amplitude Shift Keying (ASK) and can basically be seen as a oscillator that is controlled by a switch. When the data-in is a logic 1 the switch is closed and the signal from the LO is transmitted through the antenna, (left) Figure 1.4. When the data-in is a logic 0 the switch is open and ideally nothing is sent. At the receiving end the signal gets integrated in the envelope detector and when it passes a certain threshold, a logic 1 or 0 is detected, (right) Figure 1.4.

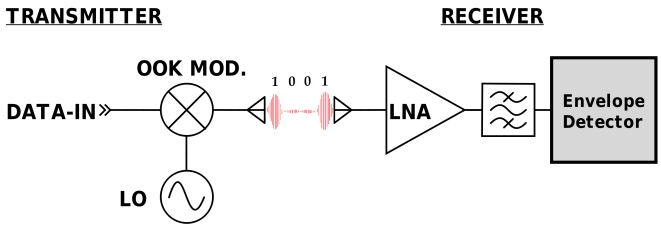


Figure 1.4: OOK concept. Modulation for the transmitter (left) and demodulation at the receiver (right) [17].

This thesis will mainly be focusing on designing the LO, creating the carrier frequency for the transceiver, but first a short briefing for the thesis,

- **Chapter 2:** A 2-port analyze and design method will be explained in detail. The reader should be able to design his or her own oscillator after reading this.
- **Chapter 3:** Some basic simulation tools and library components are introduced.
- **Chapter 4:** The goals and requirements for this thesis are discussed.
- **Chapter 5:** Design methodology will be applied and various oscillator typologies will be evaluated and chosen based on this analysis.
- **Chapter 6:** Layout and Optimizing of the oscillator.
- **Chapter 7:** Thorough EM-simulations of critical paths and process corner analysis for verification.
- **Chapter 8:** Reflecting upon the work that has been done and what needs to be done.

1.2 Oscillators In General

The oscillator is one of the most fundamental components in RF and microwave systems. It creates the carrier frequency for the modulated signal and so, consistency and stability is crucial. To represent the deviations from the ideal oscillator, Single Sideband Phase Noise (SSB) is used as a Figure Of Merit (FOM).

A oscillator consists of a sustaining stage (amplifier) and a resonant element, see Figure 1.5 for illustration. The term sustaining stage is often used when dealing with oscillators, it is more explanatory because the amplifier sustains the resonator by compensating for loss in energy. Different types of topologies can be used to sustain oscillations, in this example a Common Emitter (CE) stage bias network consists of two resistors and one voltage source. The R_f resistor also works as a shunt feedback resistor. The inductor L_{RF} blocks the RF signal and prevents it from being ac grounded. The capacitors C_1 and C_2 blocks DC-signal. The parallel resonator consists of L_r and C_r, these two components will set the resonating frequency and is often referred to as the tank circuit.

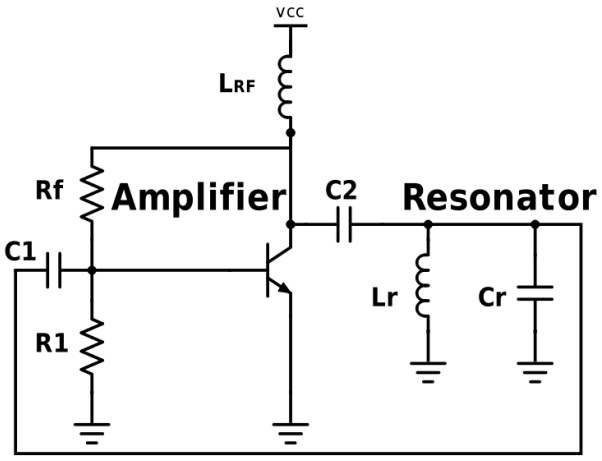


Figure 1.5: Concept oscillator.

1.2.1 The Tank Circuit

This section will explain the concept of how to sustain oscillations, using the RLC tank circuit as an example. For simplicity the resistance is not modeled.

In the tank circuit (left) Figure 1.6 the capacitor is charged through an external source of energy. The source of energy is then removed and the capacitor is connected back into the tank circuit, (right) Figure 1.6.

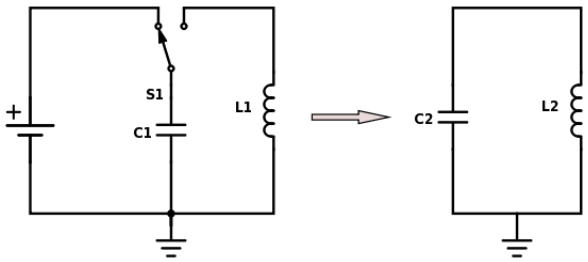


Figure 1.6: Charging of LC tank circuit.

Next the charging and discharging of the tank circuit is explained,

- **A, Figure 1.7:** The capacitor starts with discharging trough L_2, this makes the current flow into the coil and the magnetic field of the coil expands.
- **B, Figure 1.7:** The current starts to decrease, the field around the coil will disintegrate thus changing the polarity of the circuit while keeping the same current flow. When the field is fully disintegrated the current flow will be zero and the capacitor is fully charged.
- **C, Figure 1.7:** Now the capacitor will start to discharge through the coil again, but this time with opposite polarities. The field of the coil will expand.
- **D, Figure 1.7:** The field starts to collapse, polarities changes and the process is repeated.

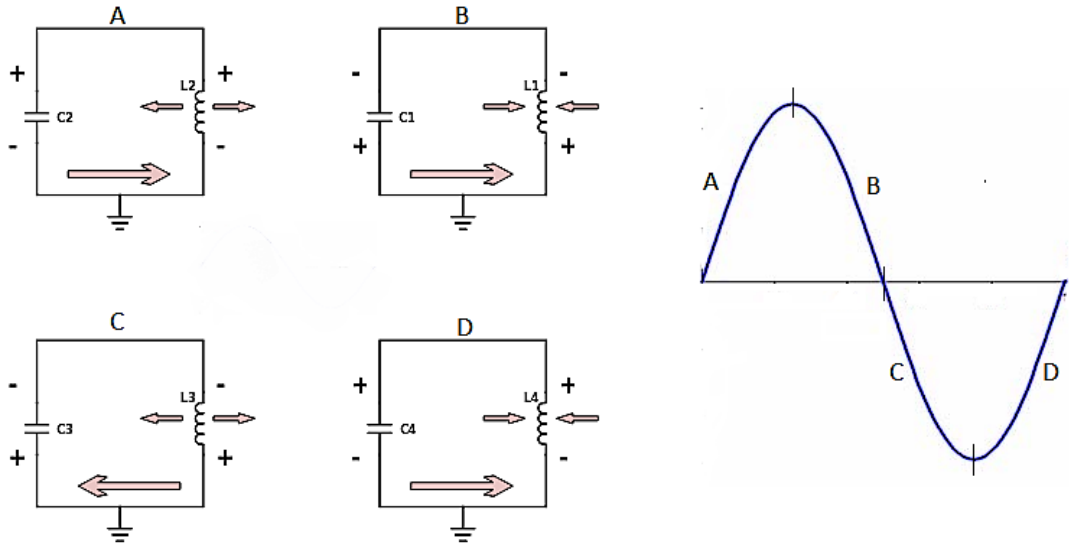


Figure 1.7: LC Tank propagation.

This process will keep on repeating it self forever as long as there is no loss, this however is not the case in real life. In real life there will be losses to the environment

due to electrical resistance in the circuit and the signal will disintegrate as illustrated in Figure 1.8. To prevent the sinusoidal signal to die out new energy has to fed to the circuit at just the right time. If positive energy where to be fed to the circuit at time T/2, which would be equal to 180°in phase, negative feedback would occur and the signal would be canceled out or degraded depending on the amount of energy. However if the right amount of positive energy where to be fed at time T which equals to 360°or n multiplications of 2π , $n = 0, 1, 2, 3...n$ which also equals to 0° given that it is periodic, the sinusoidal signal would be kept at a constant level of amplitude and ideally no change in phase.

In Chapter 2 techniques and theory used to achieve these goals are presented.

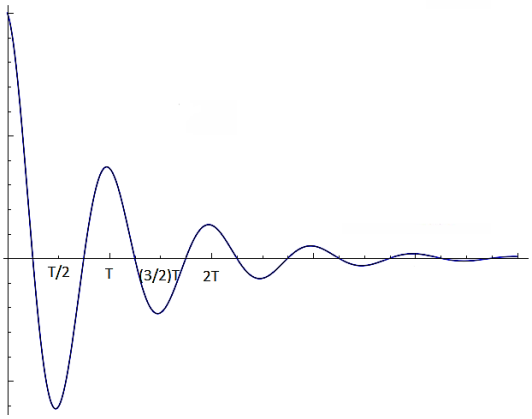


Figure 1.8: Damped sinusoidal signal.

1.2.2 Single Sideband Phase Noise (SSB)

SSB is used as FOM in oscillator methodology and so a short introduction of the Leeson's phase noise formula is presented [11]. This will give more context to Chapter 2. The formula for Leeson's SSB is,

$$L(fm) = 10log\left[\frac{1}{2}\left(1+\frac{f_c}{f_m}\right)\left(1+\left(\frac{f_0}{2f_mQ_L}\right)^2\right)\left(\frac{FkT}{P_s}\right)\right](dBc/Hz) \tag{1.2}$$

Where,

- F is an empirical factor loosely correlated to the device (amplifier) noise, Noise Factor (NF)
- fc is the flicker corner frequency
- Ps is the output power
- f_0 is the carrier frequency
- Q_L is the open-loop loaded Q

- k is Boltzmann's constant $\left(1.38 * 10^{-23} \ \frac{m^2 kg}{s^2 K}\right)$
- T is operating temperature in kelvin (nom. 300 K)
- fm is the offset, modulation or baseband frequency

Chapter 2

Oscillator Design Methodology

Theory, methods and statements in this chapter are mainly from the book "Discrete Oscillator Design: Linear, Nonlinear, Transient, and Noise Domains [20]". Figures and examples were made to explain the concept of oscillator design, and are not copied from the book.

When designing oscillators there are different methods that can be used. In this thesis we will focus on the 2-port method. This is a intuitive and efficient way to design oscillators and gives great insight, and control over the design. The 2-port method was originally used for piezoelectric resonators and low-frequency oscillator designs while the 1-port negative-resistance or negative-conductance method was used for microwave designs. However, the open-loop method is suitable for microwave design as well and gives better insight in terms of starting criteria and loaded Q. These factor have great impact on phase noise and many other parameters.

The main reason for choosing the 2-port method is because of the bipolar transistor npn13p that is found in the IHP SG13s process. This is the process that the University of Bergen is licensed for. The npn13p has a f_t of 250 GHz and a f_{max} of 300 GHz. It is stated that f_t, when designing for negative resistance-conductance, should not exceed 1 to 3 times the resonating frequency. This is explained further in section 2.6, but it means that f_t should be somewhere between 60 and 180 GHz for a 60 GHz negative resistance-conductance oscillator. For the 2-port method, a minimum f_t of 4 times the resonating frequency is recommended. This equals to $f_t \geq 240$ GHz for a 60 GHz 2-port oscillator.

The book "Discrete Oscillator Design: Linear, Nonlinear, Transient, and Noise Domains" uses four steps when designing and analyzing a oscillator, these steps are as the title of the book implies. In the next sections these methods will be explained with examples and they will also be used to do a more rigorous analysis of different oscillator typologies in Chapter 5.

2.1 Linear Analysis

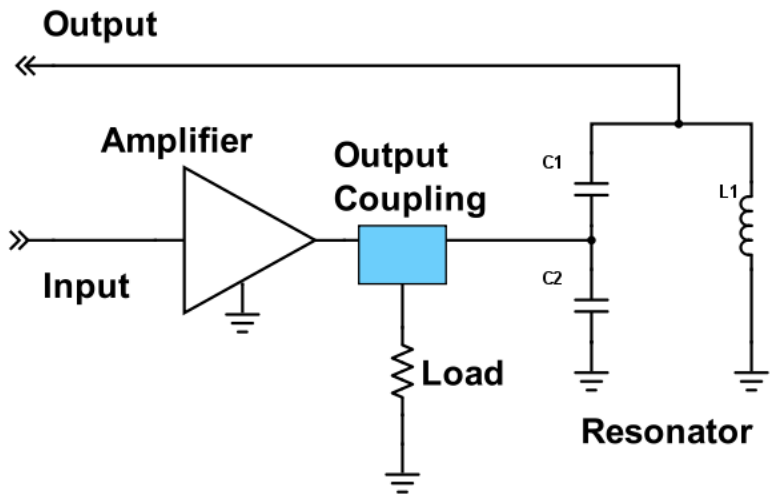


Figure 2.1: Amplifier-Resonator Cascade.

In Figure 2.1 a amplifier-resonator cascade is presented. This is referred to as the open-loop cascade, to form the actual oscillator the loop is closed. The amplifier serve as a sustaining stage for the resonator, providing it with energy to sustain oscillations. Power can be extracted from almost any node of the circuit and it will have different features which will be explained later in this chapter. The resonator sets the oscillating frequency and is a very important element.

In Figure 2.2 the S_{21} forward scattering parameter amplitude and phase is plotted against frequency, this is the Bode plot of the open-loop cascade. The phase-zero crossing, ϕ_0, occurs at approximately 60 GHz and the small-signal gain of S_{21} at this point is called the Gain Margin (GM) which is 3.8 dB.

Ideally, when the loop is closed, the gain margin will be consumed by nonlinear action, and the resonating frequency (f_0) will occur at ϕ_0. This happens because the positive feedback in the closed-loop will eventually force the amplifier to operate in the nonlinear area, and so the gain in the amplifier will be reduced.

Non-ideally this nonlinear action will reduce the gain, shift the phase and modify the impedance of the amplifier. How to deal with this will be explained in section 2.3, but first some necessary starting conditions for the open-loop cascade is established called the Barkhausen's criterion, these are:

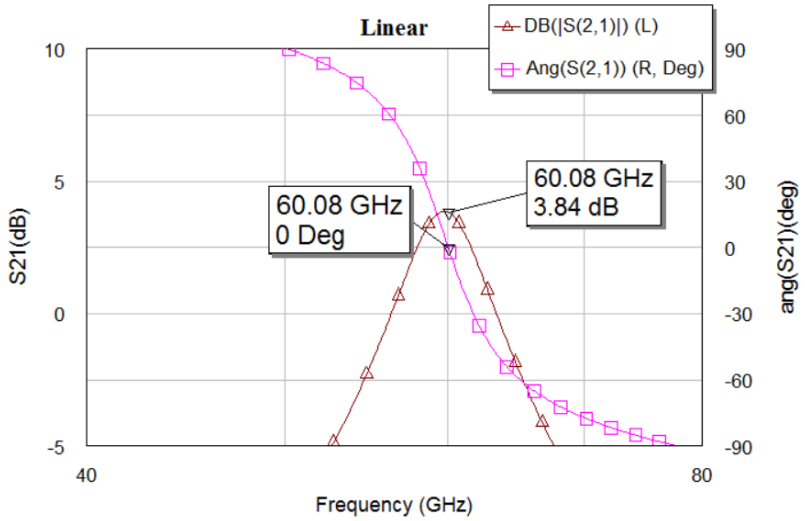


Figure 2.2: S_{21} forward scattering parameter amplitude and phase of the amplifier-resonator cascade.

1. The frequency of phase zero crossing, ϕ_0, is the oscillation frequency;
2. The initial gain must be greater than 0 dB at ϕ_0;
3. The phase slope at ϕ_0 must be negative and if there are multiple ϕ_0, the quantity with a negative phase slope must exceed the quantity with a positive slope.

Other goals to achieve in the open-loop analysis are:

1. the maximum $\frac{\partial \phi}{\partial \omega}$ occurs at ϕ_0;
2. the amplifier is stable;
3. S_{11} and S_{22} are small;
4. the maximum gain occurs at ϕ_0;
5. the gain margin should be moderate, typically 3 to 8 dB.

Next, the reason for these conditions are explained.

2.1.1 The frequency of phase zero crossing, ϕ_0, is the oscillation frequency

In a steady state for a oscillator the complex loop gain in Figure 2.3 has to equal unity, eq.2.1. Where $A = I_{out}/Vin$ and $\beta = Vin/Iout$.

$$T(Vin, \omega) = A(Vin, j\omega)\beta(j\omega) = 1 \tag{2.1}$$

The feedback transfer function can be written in terms of the input and output voltage and current, eq.2.2. Where $K = Vin/Vout$ and $Z = Vout/Iout$.

$$\beta(j\omega) = K(j\omega)Z(j\omega) \tag{2.2}$$

By presenting this with complex phase vectors we get,

$$A\,exp(j\phi_A) * K\,exp(j\phi_K) * Z\,exp(j\phi_Z) = 1 \tag{2.3}$$

By looking at eq.2.3 it follows that the sum of the phases must equal to 0, 2π.... and so on in order to equal unity [6]. From this spurs eq.2.4.

$$\phi_A + \phi_K + \phi_Z = 0,\ 2\pi.. \tag{2.4}$$

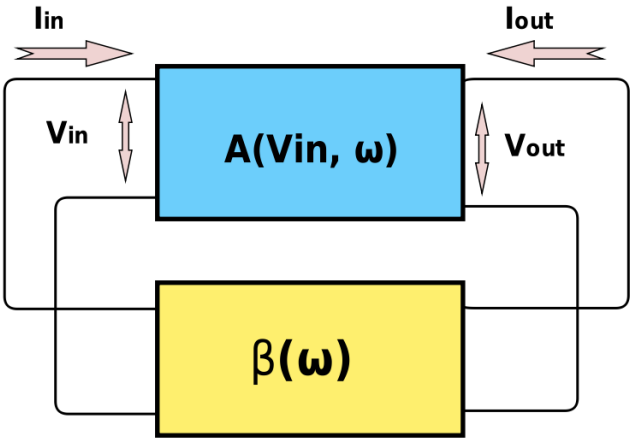


Figure 2.3: 2-port feedback block diagram.

2.1.2 The initial gain must be greater than 0 dB at ϕ_0

The reason for this is, quote [6] "Because an oscillator is an autonomous circuit, electronic noise in the active device or power supply turn on transient and leads to the self-excitation of the oscillations."

So in order for the circuit to amplify the noise it needs a gain margin. The gain margin can then be absorbed and establish a steady state signal.

2.1.3 Maximum Phase Slope At Phase Zero Crossing

The steeper the phase slope, the less effect changes in phase will have on the frequency. If the phase of $S_{21}(dB)$ in the Bode plot of Figure 2.4 where to shift up 10% this would lead to a resonating frequency of approximately 61 GHz. If the phase slope was steeper, ideally infinite $\frac{\partial\phi}{\partial\omega} = \infty\ deg/rad/s$ it would have non effect on the frequency.

Such changes can arise from bias instability, temperature variations, noise and termination impedance changes.

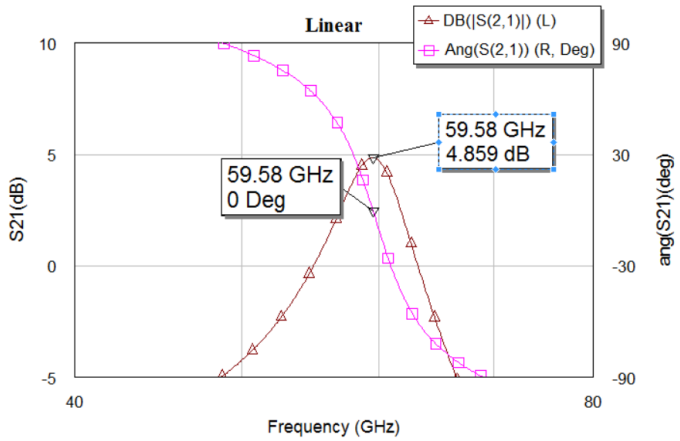


Figure 2.4: Maximum phase slope at ϕ_0 for S_{21}.

2.1.4 Stable Amplifier

To prevent spurious oscillations a stable amplifier is important. Conventional techniques that are used to stabilize amplifiers are also used to stabilize the sustaining stage for the oscillator, using feedback resistors. For CB and CC base resistance can be applied to give stability. For the CE either shunt or series feedback can be used to improve stability, but be aware of noise.

In order to make the amplifier unconditional stable the Rollet stability factor K, eq.2.5, must be greater then 1 and B_1 must be positive, eq.2.6.

$$K = \frac{(1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|}{2|S_{12}||S_{21}|} \tag{2.5}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{2.6}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.7}$$

The amplifier can also be made conditional stable, but requires a certain input/output termination impedance. In this case stability circles are used to determine if the amplifier is stable.

2.1.5 Matching (S_{11} and S_{22} are small)

When the open-loop is closed the reference impedance for the ports will not necessarily match S_{11} and S_{22}. This will affect the gain margin and is referred to as MismatchError, eq.2.8. In addition to this, the phase slope and the frequency at ϕ_0 can also change.

The reference impedance at the ports when measuring S_{11} and S_{22} can be changed to fit the design and is especially wise if S_{11} and S_{22} is similar and near the real axis, this will make S_{11} and S_{22} smaller and a more authentic Bode plot is then produced .

If the reversed transmission S_{12} is small, the open-loop mismatch error loop output driving the input is given by,

$$MismatchError = 20log\frac{1}{1 - S_{11}S_{22}} \tag{2.8}$$

S_{11} and S_{22} are complex numbers, the MismatchError in dB can therefore have a positive or a negative impact on the Bode plot. In other words, the Bode plot can either be optimistic or pessimistic. In Table 2.1 various settings for the S_{11} and S_{22} are used to calculate the maximum MismatchError in dB for a total of 0 and 180 degrees phase shift.

$S_{nn}(dB)$	$S_{mm}(dB)$	Error(dB)
-20.00	-20.00	+0.087,-0.086
-20.00	-10.00	+0.279,-0.270
-20.00	-6.00	+0.447,-0.425
-20.00	-3.00	+0.638,-0.594
-11.00	-6.00	+1.323,-1.148
-10.00	-10.00	+0.915,-0.828
-10.00	-6.00	+1.499,-1.278
-10.00	-3.00	+2.201,-1.755
-6.00	-6.00	+2.513,-1.946
-6.00	-3.00	+3.806,-2.638
-3.00	-3.00	+6.041,-3.529

Table 2.1: Maximum mismatch error when the open-loop cascade is mismatched.

In (bottom right) Figure 2.5 magnitude and phase for the S_{11} and S_{22} are normalized to 50 ohm ports and plotted for for the open-loop cascade of (top) Figure 2.5. The sustaining stage is a Common Emitter with a shunt feedback resistor of 400 ohm. The npn13p uses 8 emitter fingers (Nx) and the bias current is 1.2 mA/Nx. The reference impedance of the ports are 50 ohms.

Comparing the magnitude plot of Figure 2.5 to Table 2.1 it would seem like the maximum error is somewhere between +1.323 and -1.148. Using eq.2.8 shows that the bode-plot is pessimistic by 1.108 dB.

The coupled parallel resonator in this examples can use L_1 and L_2 to match the resonator to the CE stage. This will increase the validation of the open-loop Bode plot analysis.

In Figure 2.6, L1 = 0.07 nH and L2 = 0.2 nH and eq.2.8 shows that the bode-plot is pessimistic by only 0.007 dB. This is nearly a perfect match and the gain margin shown in the open-loop bode plot will be the gain margin of the closed loop.

If great precision is needed the Randall/Hock equation can be used. Their equation for the true complex gain of a self-terminated cascade is given by eq.2.9.

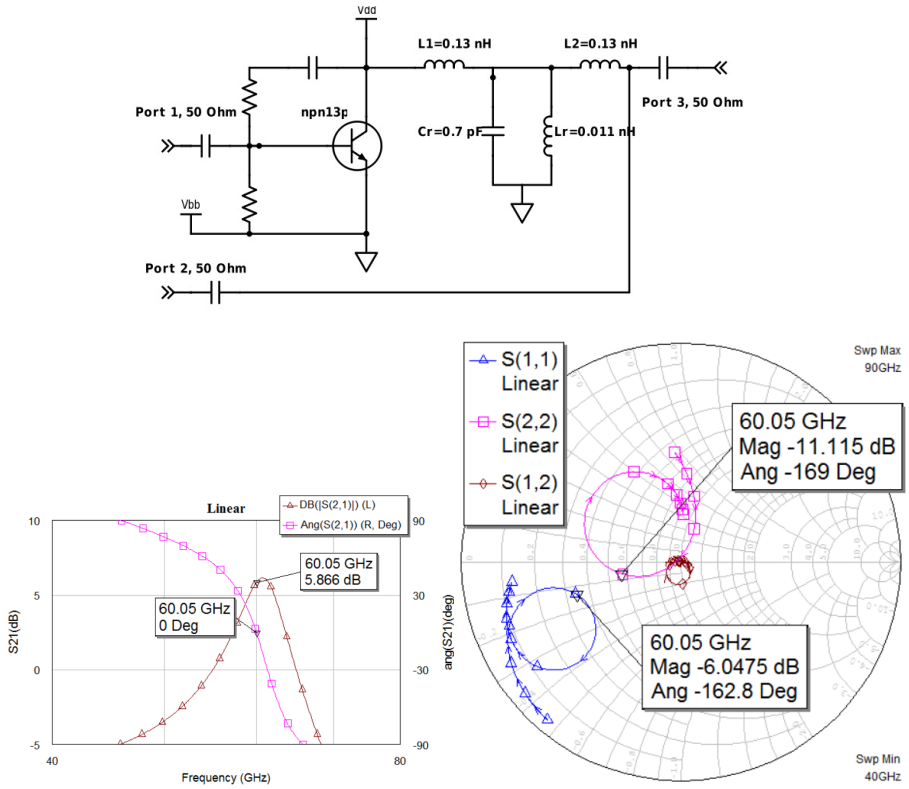


Figure 2.5: Open-loop cascade with Common Emitter and coupled parallel resonator (top). Bode-plot showing gain margin and phase slope for the open-loop cascade (left). S_{11} and S_{22} for the cascade plotted on smith chart (right).

$$G = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}} \tag{2.9}$$

The results using eq.2.9 for L1=0.07 nH and L2=0.2 nH was G=4.839 dB. Unlike eq.2.8 eq.2.9 also contains the reversed transmission S_{12}. For a mismatch to be 0 dB it would mean that $S_{12} = S_{11}$ *or* $S_{22} = 0$ dB this would lead to $G = S_{21}$. So to establish the MismatchError in therms of G we need to subtract the magnitude $|S_{21}|\,(dB) = 4.858$ dB from G which leads to mismatch error, in this case, -0.019 dB. Because S_{12} is fairly small the results from eq.2.8 and eq.2.9 did not deviate much from each other.

If S_{12} somehow were to increase the validity of eq.2.8 would decrease. To compare eq.2.8 and 2.9 an illustration were made in Figure 2.7. S_{11} and S_{22} are kept at constant level of -10 dB and $S_{21} = 6.02$ dB. The magnitude of S_{12} varies from 1-50 % of S_{21} magnitude. G has triangle indicators and the uncorrected open-loop prediction, MismatchError has circle indicators. The uncorrected predictions are not dependent on S_{12} and is therefore kept at a constant.

Based on this analysis it is fair to say that if the $|S_{12}| \geq 0.1\,|S_{21}|$ it can be good idea to validate the results using the Randall/Hock equation.

To quote [20], "The Randall/Hock expression was truly an essential contribution to

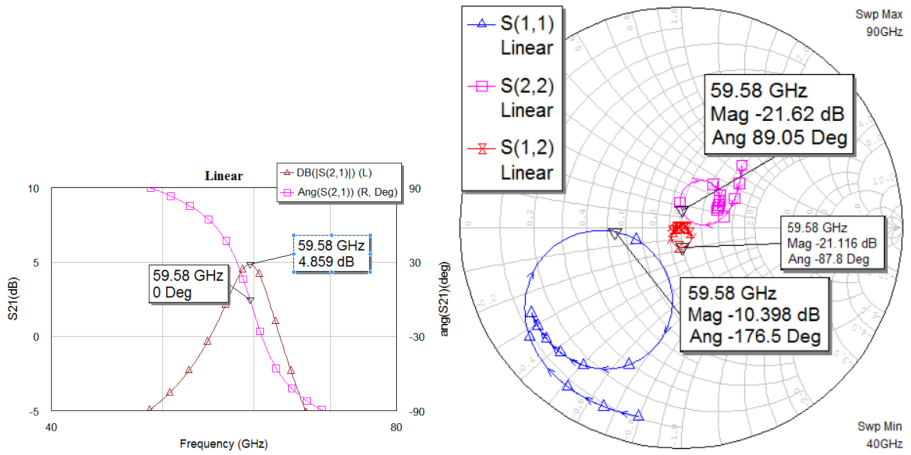


Figure 2.6: Results after matching the resonator and amplifier. S_{11} and S_{22} are smaller.

the art", and so it needs to be recognized. Mitch Randall and Terry Hock published this method for oscillator analysis in June of 2001 [18].

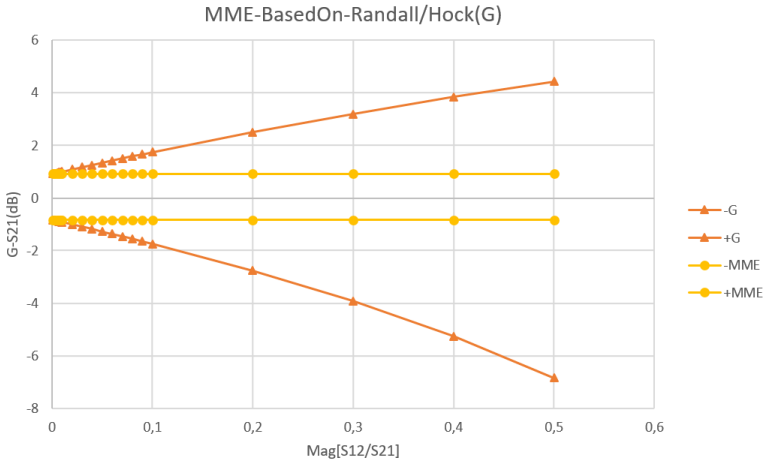


Figure 2.7: Comparing eq.2.8 versus the Randall/Hock equation G. S_{11} and S_{22} are kept at constant of -10 dB, $S_{21} = 6.02$ dB constant and $|S_{12}|$ varies from 1 - 50 % of $|S_{21}|$.

2.1.6 Gain Peak at Phase Zero Intersection

If the gain peaks at the resonating frequency, ϕ_0, all the available gain margin will be utilized when nonlinear action occurs. As gain margin is absorbed by nonlinear action the amplifier moves into compression thus more power is extracted from the amplifier. Read more about this in section 2.3.

2.1.7 Moderate Gain

Higher gain margin leads to higher compression which leads to higher harmonic distortion, spurious oscillation modes and degraded phase noise performance. 3 to 8 dB is a

typical target. If phase noise is of concern then the lower case of 3 dB should be considered and if high output power and fast start up is important the higher case of 8 dB is preferred.

2.1.8 Load Pulling

When load variations causes a shift in frequency it is called load pulling. The load impedance can change and this might lead to frequency shifts and in some cases pull the gain margin to fall below 0 dB and stop oscillation. Load pulling is specified as the frequency shift resulting from a 2:1 load VSWR with any phase angle, such as a 25 ohm in a 50 ohm.

The 25 ohm's electrical length in this example is 24 000 degrees at 60 GHz and the results from the open-loop cascade is show in Figure 2.8. To the left in Figure 2.8 the gain margin pulls below the 0 dB line and the risk of oscillation stop must be considered. This can also be the result of poor matching and so the Randall/Hock eq.2.9 can be applied to verify this. The 2:1 VSWR pulls the phase-zero crossing from 59.59-62.13 GHz and therefore the frequency 2.54 GHz. Because the phase zero crossing originally was 62.13 GHz the pulling can be presented as 4% frequency pulling. A typical specification for a 2:1 VSWR load pull is 0.1%. From the input and output impedance plot right Figure 2.8 it is clear that the open-loop cascade match changes, this can be resolved with better matching.

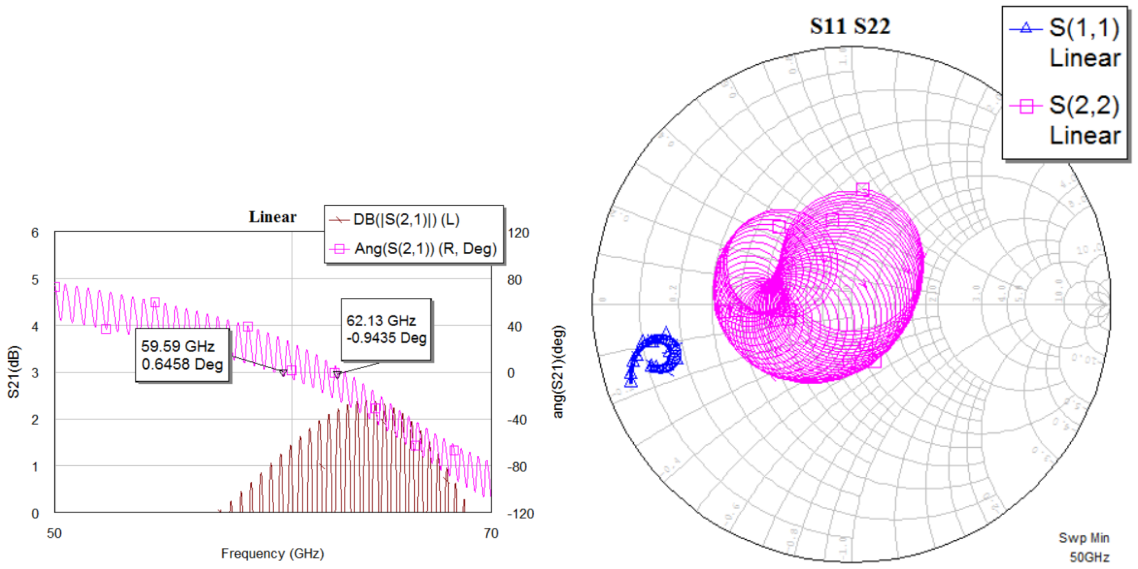


Figure 2.8: Simulated load pulling for the open-loop cascade using a 2:1 load VSWR with any phase angle. If the gain margin magnitude pulls below 0 dB the risk of oscillation stoppage must be considered.

2.2 RLC Resonators

The RLC resonator comes in various forms. In this section the theory of three RLC resonators will be presented and discussed, namely the series resonator, parallel resonator and the Colpitt resonator.

2.2.1 Series Resonator

For a basic series RLC circuit, Figure 2.9, the input impedance seen by the source is,

$$Z_s = j2\pi fL + R - j\frac{1}{2\pi fC} \tag{2.10}$$

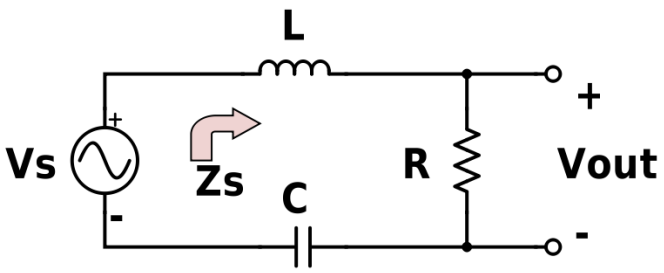


Figure 2.9: Basic RLC series resonator.

The undamped frequency of the circuit is when the reactive part from the capacitance cancels the reactive part from the inductance and so $2\pi f_0 L = \frac{1}{2\pi f_0 C}$ where f_0 is the undamped resonating frequency. Solving for f_0 gives,

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.11}$$

The loaded Q for a series resonator is denoted Q_s and is the reactance of either the capacitor or the inductance at f_0 divided by series resistance R, given by eq.2.12. This parameter is very important because it determines how steep the phase slope is at phase zero crossing. In (right) Figure 2.10 the phase slope of Z_s is presented for different values of Q_s.

$$Q_s = \frac{X}{R} \tag{2.12}$$

Z_s can now be rewritten in therms of Q_s and then solved for the transferfunction eq.2.13.

$$H(j\omega) = \frac{V_{out}}{Vs} = \frac{1}{1 + jQ_s(f/f_0 - f_0/f)} \tag{2.13}$$

The magnitude of eq.2.13 is presenter versus frequency in (left) Figure 2.10 .

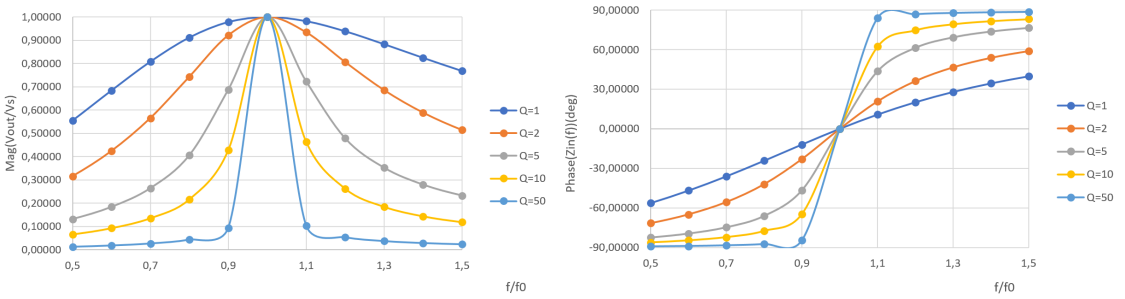


Figure 2.10: Magnitude for the transferfunction (left) and phase for the input impedance (right) versus frequency for the series resonator.

2.2.2 Parallel Resonator

For a basic parallel RLC circuit, see Figure 2.11, the input impedance seen by the source is,

$$Z_p = \frac{1}{1/R + j2\pi fC - j(1/2\pi fL)} \tag{2.14}$$

The approach to find f_0 for the parallel resonator is the same as for the series resonator and the results are identical, eq.2.11.

The loaded Q for a parallel resonator is denoted Q_p and is the parallel resistance seen by the terminals divided by the reactance of either the capacitor or the inductance at f_0, eq.2.15.

$$Q_p = \frac{R}{X} = \frac{Z_0}{2X} \tag{2.15}$$

Z_p can now be rewritten in therms of Q_p and then solved for V_{out},

$$V_{out} = \frac{IR}{1 + jQ_p(f/f_0 - f_0/f)}$$

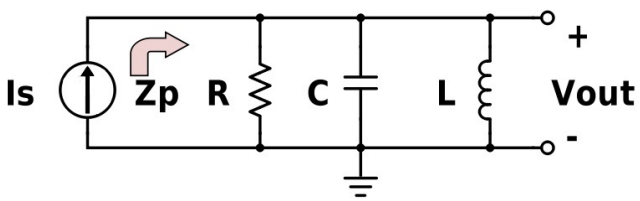


Figure 2.11: Basic RLC parallel resonator.

2.2.3 Loaded Q – Q_L and Unloaded Q – Q_U

We want steep phase slope at ϕ_0, referring to section 2.1.3. To obtain this a high Q_L is important as illustrated in Figure 2.10.

Q_L for a series resonator increases as the characteristic impedance at terminals decreases and reactance at f_0 increases, eq.2.12. This means that a amplifier with a low input/output impedance would be favored, the resonator should have high inductance and small capacitance.

For the parallel resonator it is the opposite, eq.2.15, so a amplifier with high input/output impedance would be favored and the resonator should have low reactance at resonance.

A more correct presentation of Q_L, for either a parallel or series resonator, is given by eq.2.16.

$$Q_L = -\frac{\omega_0}{2}\frac{\partial \phi}{\partial \omega} \tag{2.16}$$

2.2.3.1 Unloaded Q – Q_U

Another form of Q is considered and is referred to as the component Q or the unloaded Q.

The Definition of **Unloaded Q** is 2π times the energy stored in a reactor divided by the energy dissipated per cycle. For loss mechanisms that are in series with a reactor this refers to,

$$Q_U = \frac{X}{R_S} \tag{2.17}$$

where R_S is the series loss resistance which can be metal loss in leads and the plates of capacitors.

For parallel loss mechanisms with the reactor the definition is,

$$Q_U = \frac{R_P}{X} \tag{2.18}$$

where R_P is the parallel loss resistance of the reactor. This can be dielectric loss in a capacitor or core losses for the inductor.

The dominant source for loss mechanisms are often in series, so normally eq.2.17 is used, but this has to be evaluated by the designer.

2.2.3.2 Total Unloaded Q – Q_R

Because the series and parallel resonator are a combination of both inductance and capacitance, total unloaded Q for the whole resonator is denoted Q_R and is given by eq.2.19. Where Q_{ind} is the Q_U for the inductance and Q_{cap} is the Q_U for the capacitance.

$$Q_R = \frac{1}{1/Q_{ind} + 1/Q_{cap}} \tag{2.19}$$

Since Q_U defines the quality of the components it is only natural that they come with a loss defined by quality. This loss is referred to as the Insertion Loss (IL) and represent the loss in dB through the resonator, eq.2.20.

$$IL = 20log\frac{Q_R}{Q_R - Q_L} \tag{2.20}$$

It is important that Q_R is bigger then Q_L or else IL will be to great. A representation of insertion loss versus the relationship between the amount of Q_L in percentage of Q_R is plotted in Figure 2.12.

From Figure 2.12 we can see that if the resonator has twice the amount of Q_R in terms of Q_L the IL is approximately 6 dB. This means that the loss through the resonator would be 6 dB. If a amplifier has 7 dB gain this would leave us with only 1 dB gain margin. To increase the gain margin Q_L has to be lowered, but then again the phase-slope would decrease and so would the oscillator performance, eq.1.2.

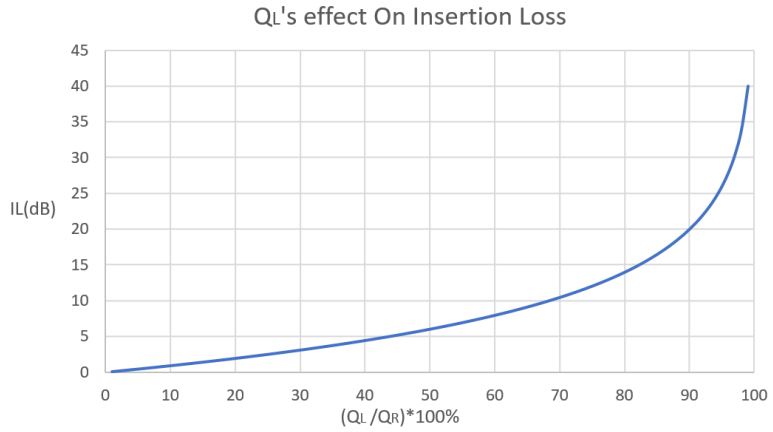


Figure 2.12: The effect of loaded Q versus unloaded Q for the insertion loss in a resonator.

The Q_L that has been defined by now is referred to as the lossless loaded Q , but in reality Q_R also degrades Q_L and can be written as,

$$Q_{Lossy} = \frac{1}{1/Q_R + 1/Q_{L-lossless}} \tag{2.21}$$

For simplicity the the lossy loaded Q will be referred to as Q_L if not else is stated.

Eq.2.21 can now be used to recalculate eq.2.20.

2.2.4 Colpitts Resonator

The Colpitts resonator has a phase shift near 0° at resonance and have dissimilar input and output impedance. This makes it great for matching with amplifier typologies which have dissimilar input and output impedance like the Common Base (CB) and Common Collector (CC).

To match this resonator with a amplifier we need to know R_{top} and R_{tap} which relates to the real part of the parallel collector impedance, and the real part of the parallel emitter impedance respectively in Figure 2.13.

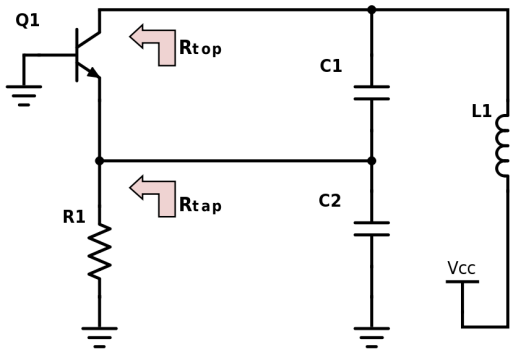


Figure 2.13: A basic concept for a Colpitt Oscillator.

To calculate the value of the inductor L_1, eq.2.22, a value for Q_L must be chosen. At this point it would be wise to know something about the Q_R of the resonator and the gain of the sustaining stage so that the IL does not get to big, figure 2.12.

Next use eq.2.23 and eq.2.24 to calculate the C_2 and C_1. In order to calculate C_1 the reactance of C_2 is needed.

$$L_1 = \frac{R_{top}}{2Q_L\omega_0} \tag{2.22}$$

$$C_2 = \frac{1}{\omega_0}\sqrt{\frac{R_{top}^2 + X_L^2 - X_L^2 R_{top}/R_{tap}}{X_L^2 R_{top} R_{tap}}} \tag{2.23}$$

$$C_1 = \frac{1}{\omega_0}\left(\frac{R_{top}^2 X_L}{R_{top}^2 + X_L^2} + \frac{R_{tap}^2 X_{C2}}{R_{tap}^2 + X_{C2}^2}\right)^{-1} \tag{2.24}$$

2.2.5 Resonator Coupling

In order for Q_L to become large for a parallel resonator the load resistance need to be of a high order, eq.2.16. For CE typologies the input and output impedance are often too low to achieve a high Q_L. In this case coupling reactors can be used either in series with parallel resonator (left) Figure 2.14 or in a shunt mode with a series resonator (left) Figure 2.15.

The coupling also presents a shift in phase that will be useful when aligning the maximum phase-slope at ϕ_0.

2.2.5.1 Coupling Phase Shift

From the Bode plot of (top right) Figure 2.14, series inductance is used as coupling. This will shift the phase down and so the maximum phase slope with gain peak occurs at -89.62 degrees instead of 0 degrees. In (bottom right) Figure 2.14 series capacitance coupling is used and so the phase is shifted up, the maximum phase slope occurs with a gain peak at 84.21 degrees.

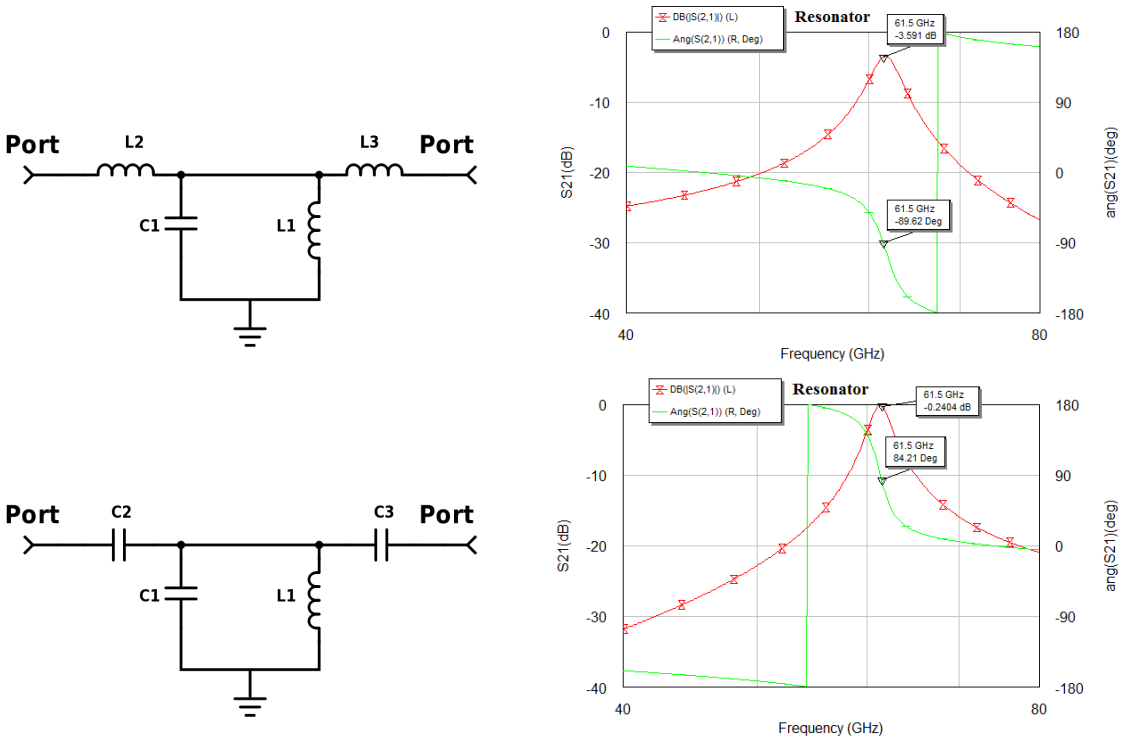


Figure 2.14: Coupled parallel resonators.

The same concept goes for the shunt reactance in Figure 2.15 except that the inductance will shift the phase up and the capacitance will shift down. This can be used to align the maximum phase slope with gain peak at 0 degrees in the open-loop cascade. If no coupling is used the maximum phase slope would occur at a given phase from the amplifier.

An example. If the phase of a CE stage is 80 degrees at 60 GHz, the phase needs to be shifted down 80 degrees. This will align the maximum phase slope at 0 degrees at 60 GHz and the Barkhausen's criterion is fulfilled. This can be done with either series inductance or shunt capacitance. This coupling shift is given by eq.2.25 where R_1 and R_2 is the resistance at port 1 and port 2.

$$\phi = 180^\circ - tan^{-1}(\frac{-R_1}{X_{C1}}) - tan^{-1}(\frac{-R_2}{X_{C2}}) \tag{2.25}$$

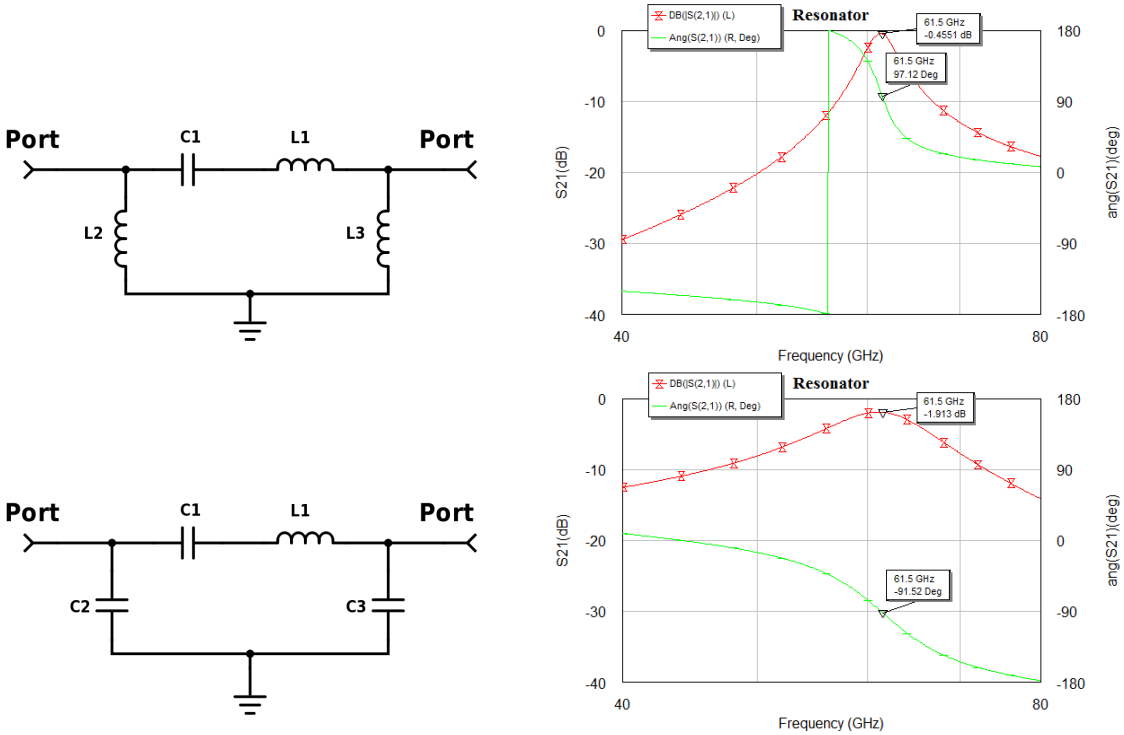


Figure 2.15: Coupled series resonators.

2.2.5.2 Coupling increases Q_L

In Figure 2.16 a reactance in series with the load is transformed to a equivalent circuit with a parallel load and reactance. The relationship between R_P, R_s, X_p *and* X_s is given by eq.2.26 and 2.27.

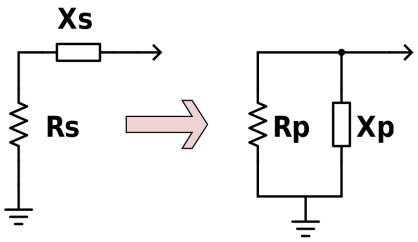


Figure 2.16: Coupling reactance X_s in series with load (left), the equivalent parallel load resistance and reactance (right).

$$R_p = \frac{R_s^2 + X_s^2}{R_s} \tag{2.26}$$

$$X_p = \frac{R_s^2 + X_s^2}{X_s} \tag{2.27}$$

If the reactance of $X_s = 2 * R_s \implies R_p = 5 * R_s$ and so the resistance seen by the resonator is shifted up and a higher Q_L is achieved.

It sprouts from the fact that,

$$Y_p = 1/Z_s = \frac{1}{R_s + jXs} = \frac{R_s}{R_s^2 + X_s^2} + \frac{jX_s}{R_s^2 + X_s^2} = G_p + jB_p \tag{2.28}$$

Transforming from parallel to series is given by eq.2.29 and 2.30.

$$R_s = \frac{G_p}{G_p^2 + B_p^2} \tag{2.29}$$

$$X_s = \frac{B_p}{G_p^2 + B_p^2} \tag{2.30}$$

2.3 Nonlinear Analysis

As the signal builds in a oscillator nonlinear action absorbs the small signal gain margin from the open-loop cascade to establish a steady state condition for the oscillator. As the steady state is established, gain margin, phase and port impedance of the active device can changes.

- Gain margin shifts could result in loss or gain in output power, subsection 2.1.6.
- If the phase shifts it could degrade or upgrade the Q_L and the frequency of oscillation would shift, eq.2.31.

$$\frac{\Delta f}{f_0} = -\frac{\pi \Delta \phi^0}{360 Q_L} \tag{2.31}$$

- The cascade gain margin is at ϕ_0 and is a function of impedance match, section 2.1.5.

All these deviations could affect the phase noise of the oscillator. Phase noise will be discussed later in this chapter and is a important way of describing the quality of the oscillator.

In the next subsection the operation of the sustaining stage in a nonlinear environment is discussed.

2.3.1 Sustaining Stage

As mentioned earlier the nonlinear effects of the amplifier absorbs the gain margin when port 1 and port 2 from the open-loop cascade are connected, first then does it really be-

come a oscillator. To get an idea of how much power the amplifier is able to sustain we look at the large-signal S-paramters (LSnm). LSnm are level-dependent and is a generalization of small-signal S-parameters.

In Figure 2.17 a compression plot of a CE stage with 7 fingers is shown. The marker with time glass shapes shows 5 dB compression at 0.68 dBm input power (input power is shown in dBm along the x-axis). The line with the diamond markers is LS_{21}. Because LS_{21} is approximately 4 dB at a input power of 0.68 dBm the output power is approximately 4.68 dBm. The output power is shown with squared markers. So if we have a gain margin of 5 dB in the open-loop cascade the expected output power from the amplifier would be 4.68 dBm at steady state. This can be used to estimate the output power of the oscillator P_S. A normal conversion efficiency for oscillators ranges between 2-15%, eq.2.32.

$$\eta(\%) = 100\frac{P_{out}}{I_{DC}V_{DC}} \tag{2.32}$$

Compression leads to higher harmonics and is one of the reasons why a upper limit of 8 dB gain margin is recommended, subsection 2.1.7.

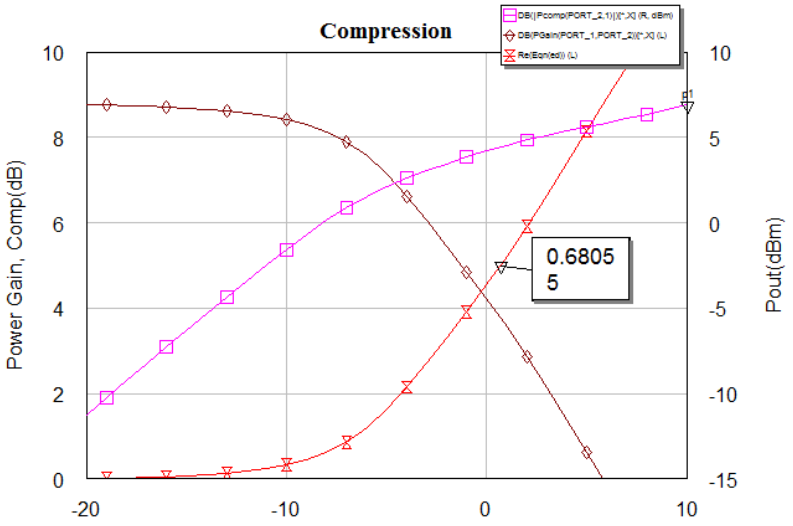


Figure 2.17: Compression plot of a Common Emitter stage using 7 emitter fingers.

2.3.2 Nonlinear Open-Loop Cascade

To validate the linear open-loop cascade analysis, input power is applied at port 1. The nonlinear effect will reveal them self as the gain margin approaches 0 dB, Figure 2.18. In this case almost no change in phase was detected, which is a good validation of the small-signal open-loop analysis. The gain peak however shifts a bit to the left and aligns it self at ϕ_0 with 0 dB. Now we have unity gain at phase zero and this is the open-loop representation of the steady state behavior for the oscillator. The output power from the coupling node under these conditions will approximately be the output power (P_S) for the oscillator, given that S_{11} and S_{22} are small.

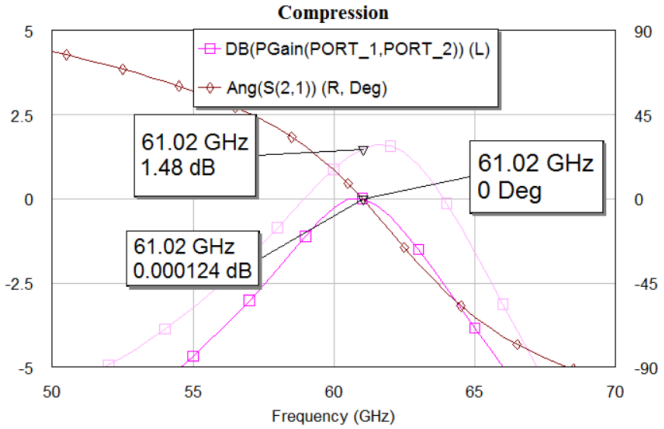


Figure 2.18: Nonlinear open-loop cascade analysis with a CE stage (Nx = 13) and coupled parallel resonator. For the faded line of LS_{21} -30 dBm is applied at port 1 and has a gain margin of 1.48 dB. For the non-faded line 1.78 dBm is applied to the input and so the LS_{21} peaks at 0 degrees with 0 dB gain.

2.3.3 Coupling Node

The node used to extract output power is referred to as the coupling node. It is usually placed between the resonator and the sustaining stage, but not necessarily. The output coupling can be realized with the use of a simple capacitor or coupled inductors. The degree of coupling and where it is placed will give different attributes to the oscillator. In general the best harmonic performance is achieved when extracting power from the resonator and the greatest output power is achieved when taken from the collector node. The amount of coupling will also influence the resonating frequency, gain margin, and load pulling. Larger coupling capacitor results in more extracted power and usually Q_L decreases. Both these factors will influence the phase noise characteristic and so it has to be chosen carefully.

2.3.4 The Ultimate Test

This test is taken from the book [20] and is used to provide a high degree of performance confidence.

1. Oscillation should start at a voltage well below the desired operating voltage, perhaps 50% to 70% of the operating voltage. This suggests adequate gain margin. Some bias schemes may preclude this, but you should at least understand why.

2. As the voltage is increased, the output power generally increases because of increasing output capability of the sustaining stage. At voltages higher than the operating voltage the output power may decline due to thermal stress or device operation above the current for optimum f_t. If the output power declines at voltages below the operating voltage the design should be evaluated for device thermal stress or excessive device current.

3. The device should not fail at voltages moderately higher than the operating voltage. This insures breakdown voltages and dissipation limits are not exceeded.

4. Output power changes with supply voltage should be smooth with no sudden jumps. Sudden jumps are indicative of spurious modes.

5. The output frequency should change smoothly with the supply voltage. It may first rise or fall and then change direction, but sudden jumps in frequency are indicative of spurious modes.

6. The output frequency change should be as expected by the pushing specification. Larger than expected shifts are indicative of loaded Q lower than expected or high bias sensitivity to the supply voltage.

7. A final refinement involves testing the oscillator with variations in the load impedance using a sliding transmission-line tuner. The above "ultimate" tests, temperature testing and finally "in system" testing provide a high degree of performance confidence.

2.4 Transient Analysis

In the start up of the oscillator the signal grows and the active device operates in the linear area. Near the end of the signal build-up the active device enters saturation and starts operating in the nonlinear area. At a certain point the gain from the active device along with the resonator will have a total gain of 0 dB and the oscillator goes into steady state, Figure 2.19. If the sustaining stage had infinite linear operating area as in a ideal amplifier the signal would never stop growing because of the positive feedback. The limitations that comes with a amplifier insures that it will reach the nonlinear operating area at some point depending on the amplifier.

If the gain margin is 6 dB when the loop is closed, this gain will start to amplify the initial signal that stems from noise in the circuit, eq.2.33. k is the Boltzmann's constant, T is temperature in kelvin, B is the 3-dB bandwidth of the resonator in Hz and F is amplifier noise factor. As the the device moves into saturation the gain margin decreases and steady state is reached.

$$v_{init} = \sqrt{\frac{2kTBF}{Z_0}} \tag{2.33}$$

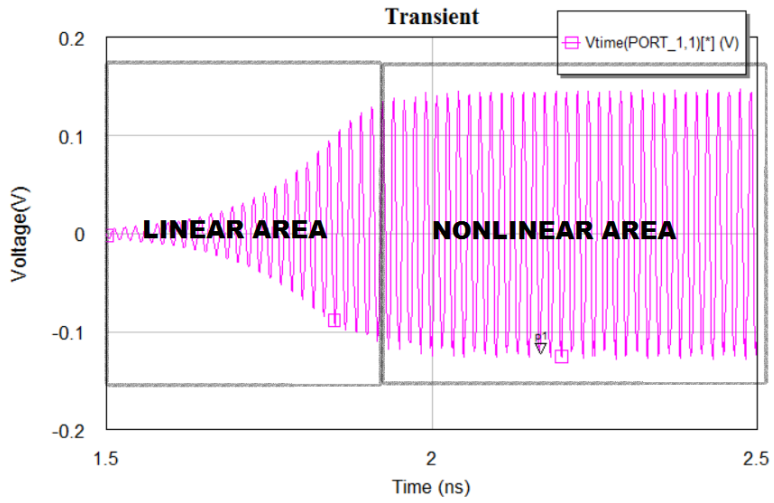


Figure 2.19: The linear and non-linear operating area of a oscillator is illustrated in the time domain.

2.5 Phase Noise

The ideal output voltage for a oscillator is given by,

$$V(t) = V_0 sin(2\pi f_0 t) \tag{2.34}$$

however the real output signal has fluctuations in the amplitude and phase and are given by,

$$V(t) = [V_0 + \varepsilon(t)]\, sin\,[2\pi f_0 t + \phi(t)] \tag{2.35}$$

$\varepsilon(t)$ is zero mean random amplitude noise and $\phi(t)$ is zero mean random phase noise. In Figure 2.20 noise is represented in the complex plane, the red arrows represent the noise variation in phase and amplitude.

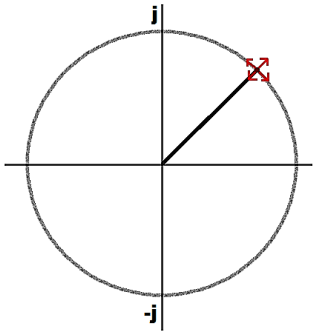


Figure 2.20: Phase and amplitude fluctuation represented in the complex plane with red arrows.

2.5.1 SSB Phase Noise

Single-sideband phase noise (SSB), eq.2.36, is used as a FOM when it comes to oscillators. The SSB is the ratio of the power in one phase-modulated sideband to the total signal power. It is given by the spectral density, eq.2.37, with 1-Hz resolution bandwidth divided by 2 given that the $\Delta\phi_{peak} \ll 1$. If $\Delta\phi_{peak} \geq 1$ this would make SSB in dB potential positive which is an impossibility.

The SSB is specified at a given offset. Example: $L(f_m) = -80\,dBc$ at 1 MHz Offset means that the power in one phase-modulated sideband 1 MHz from the carrier is 80 dB below the carrier.

$$L(f_m) = \frac{1}{2} S_\phi(f_m) \tag{2.36}$$

$$S_\phi(f_m) = \frac{\Delta\phi^2_{rms}(f_m)}{BW_{\Delta\phi_{rms}}}\,(rad^2/Hz) \tag{2.37}$$

2.5.2 Leeson's Phase Noise Formula[11, 22]

The SSB can be calculated based upon the open-loop cascade using eq.2.38. This equation will be used in chapter 5 to analyze different amplifier topologies and resonators, and will serve as guide line for choosing sustaining stage and resonator.

In order to calculate the SSB there are several things we need to know about the open-loop cascade. Starting with the amplifier,

- F is an empirical factor loosely correlated to the device noise, Noise Factor (NF)
- fc is the flicker corner frequency

for the open-loop cascade,

- Ps is the output power
- f_0 is the carrier frequency
- Q_L is the open-loop loaded Q

Other factors and constants,

- k is Boltzmann's constant
- T is operating temperature in kelvin (nom 300K)
- fm is the offset, modulation or baseband frequency

$$L(fm) = 10log\left[\frac{1}{2}\left(1+\frac{f_c}{f_m}\right)\left(1+\left(\frac{f_0}{2f_mQ_L}\right)^2\right)\left(\frac{FkT}{P_s}\right)\right](dBc/Hz) \tag{2.38}$$

2.5.3 Flicker Corner Frequency

A high flicker noise frequency ruins the SSB. It is associated with crystal impurities that catches and releases carriers in a random fashion. It has a $1/f$ noise distribution in the amplifier and increases with decreasing frequency, see Figure 2.21. The flicker corner frequency can be found by drawing a linear line from the $1/f$ line and see where NF crosses 0 dB. For SiGe devices, a flicker corner frequency below 10 kHz is normal. For this particular amplifier setup it is 3.5 kHz.

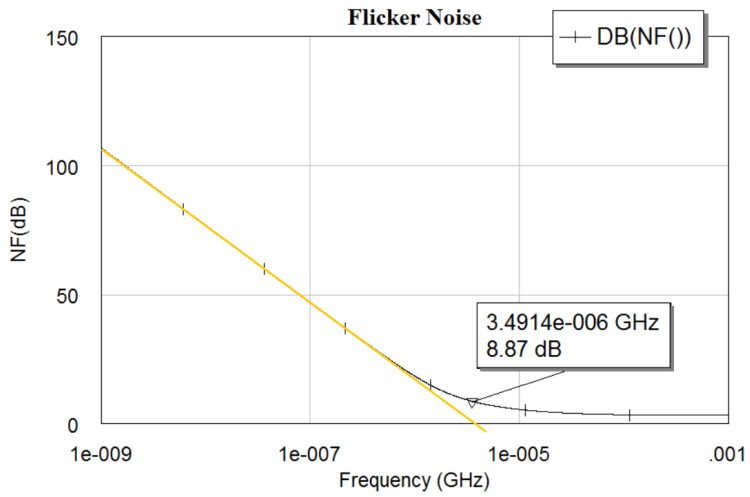


Figure 2.21: Flicker Noise frequency.

2.6 1-port Design

Negative resistance and conductance oscillators is referred to as 1-port oscillators in [20] and states that they require a unstable device topology which is the opposite of what is needed for the 2-port design methodology. This instability is then controlled by a resonator. The main difference between the negative resistance and conductance topology is that they use series and parallel resonators respectively.

The 2-port method uses the amplifier to supply energy and isolates the device characteristics from the oscillators performances. For 1-port design the active device needs to be unstable, quot [20], "Device instability is intrinsically a function of the device. Therefore, Device selection is critical in one-port oscillator design and effective oscillator design does not begin with an oscillator design, but rather with the device".

In Figure 2.22 an equivalent circuit is drawn for a negative resistance oscillator with Common Collector topology as the active device. $C_{eff} = 2pF$ and is the effective input capacitance of the device, $L_{res} = 27nH$ and $C_{res} = 1.8pF$ makes a series resonator at the base input. These will force oscillation upon the device. As the signal builds the negative resistance will be consumed by nonlinear actiont and a steady state will be reach with

$NegR = 0$ ohms. However the net series capacitance of C_{res} and C_{eff} of this oscillator is 0.92 pF and so the the oscillating frequency will be 1 GHz instead of 0.7 GHz which would have been the case if not for C_{eff}. This shows that the device has a enormous impact on the oscillators frequency.

Because of this it is recommended that f_t for the device should not exceed 1 to 3 times the oscillating frequency. A high f_t device leads to small C_{eff} and so C_{res} has to be small in order to isolate the device from the resonator and so the L_{res} has to be large as well. The same goes for the negative conductance which also is highly dependent on the selection of device.

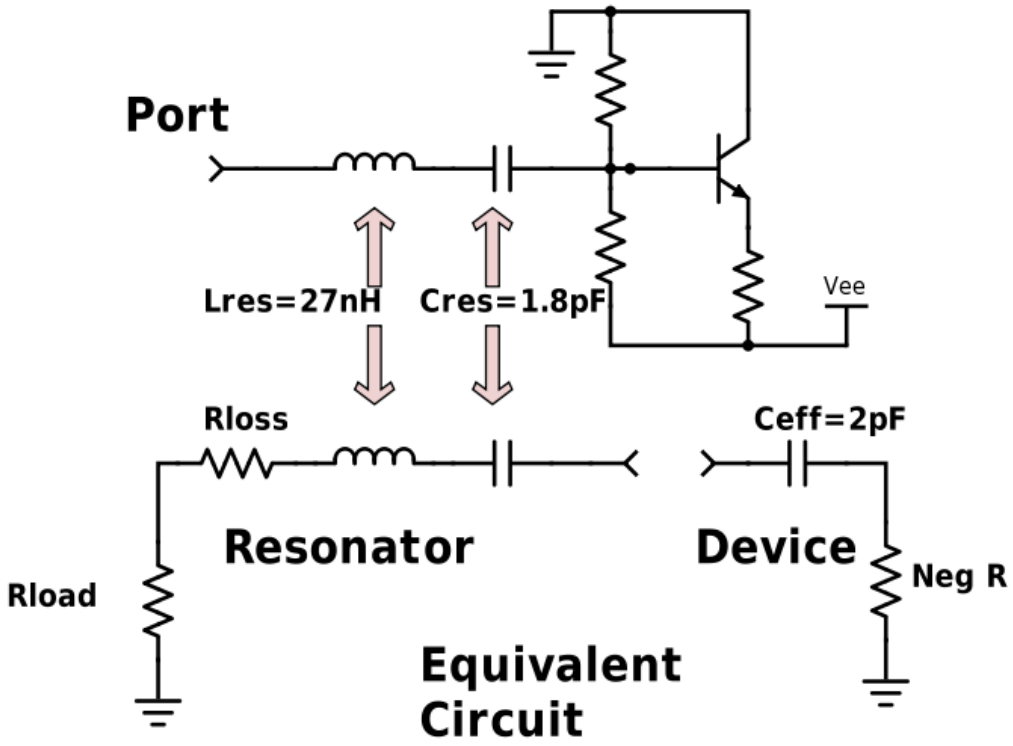


Figure 2.22: A basic concept for a negative resistance oscillator is presented with a equivalent circuit.

Chapter 3

Microwave Office and IHP Library.

In this section tools and techniques used for analyzing the open-loop cascade and closed-loop oscillator are presented. Also a short introduction to the library components are presented.

3.0.1 Open-Loop

To analyze the open-loop cascade AWR has a very useful tool called OSCTEST, Figure 3.1. The OSCTEST is used to determine the open-loop gain by breaking the feedback loop from the resonator. It can be placed anywhere in the loop and will give slightly different results and so it has to be verified with closed-loop results. First the OSCTEST measure $\mid S21 \mid$ under small signal conditions, $\mid S21 \mid > 1$. When a large signal excitation is applied at port 1 and is increased. The monitored large signal S-parameter S21 will decrease because the amplifier enters saturation. At some excitation level the $\mid S21 \mid = 1$ at phase-zero. This point is the oscillation frequency, and the output power under these conditions is the oscillator's output power. Examples are given in section 2.1 and 2.3. When applying large-signal excitation we are looking at the nonlinear behavior of the open-loop cascade.

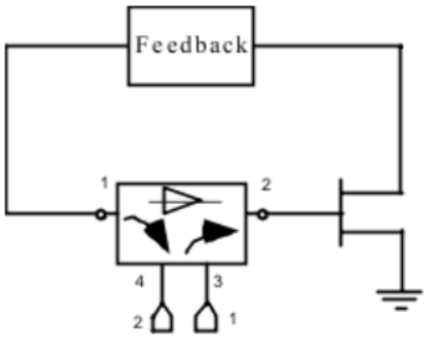


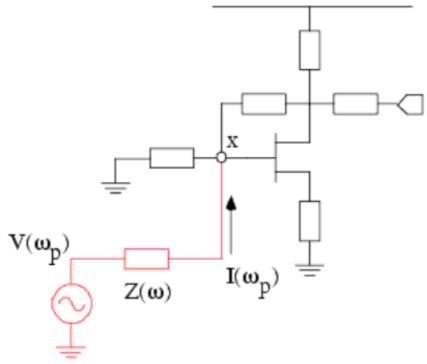
Figure 3.1: OSCTEST is a useful tool when analyzing the open-loop cascade of an oscillator.

3.0.2 Closed-Loop

In the closed-loop we look at phase noise, output power of fundamental and harmonic components, waveforms and transients. When looking at these parameters except for the transient analysis, microwave office uses a technique called harmonic balance (HB). This is a steady-state analyses and is used to analyze high-frequency nonlinear circuits in the frequency domain rather in the time-domain which can be very slow.

To analyze a oscillator we need to apply OSCAPROBE to the oscillator. Quote AWR simulation guide, "OSCAPROBE is an ideal source $V(\omega_p)$ in series with an ideal impedance $Z(\omega)$ element. The impedance presents an open circuit at all frequencies other than the fundamental frequency of oscillation." , see Figure 3.2. If node X oscillates at the same frequency as $V(\omega_p)$ no current $I(\omega_p)$ flows through the impedance and it will not disturb the circuit, the same principle goes for the harmonic content. It is recommended to place the probe somewhere in between the resonator and the sustaining stage.

By only using the OSCPROBE we can measure the resonating frequency and output power. To measure phase noise OSCNOISE needs to be added, quote AWR simulation guide, "OSCNOISE instructs the simulator to compute oscillator phase noise following large-signal oscillator analysis".



The source impedance is given by:

$$Z(\omega) = \begin{cases} 0 & \omega = \omega_p \\ \infty & \omega \neq \omega_p \end{cases}$$

Figure 3.2: OSCPROBE measure the the steady-state operation of a oscillator in closed-loop.

3.0.3 EM-simulation

Quote AWR simulation guide, "Electromagnetic (EM) simulators use Maxwell's equations to compute the response of a structure from its physical geometry."

In this thesis we are restricted to the IHP SG13S process. The components used in the library of this process have a model made by the vendor. These models are only valid within a set of specific rules, a upper/lower frequency, distance from some other

component etc. So when designing a circuit there will be stray capacitance between the different layers and inductance that are not modeled by the vendor because it is impossible for them to predict a infinite number of designs. So it is then in the hand of the designer that does the EM-simulations to decide, what part needs some extra attention and what part is god enough. When the EM structures are built and analyzed it is also the designers task to verify if this is within reason of what is expected for a given structure. This and more will be illustrated with examples in chapter 7.

3.1 IHP SG13S library

SG13s is a high performance BiCMOS technology with a 0.13 µm CMOS process. It contains bipolar devices made in silicon germanium (SiGe). BiCMOS integrates two technologies, bipolar junction transistor and the CMOS. The SiGe bipolar devices is in the category heterojunction bipolar transistor (HBT) which means that the emitter and base uses different semiconductor material thus, creating a heterojunction (unequal band gaps).

This section contains information about the different components used from the library.

3.1.1 Varactor

The varactor works as a voltage controlled capacitance and is a key component in VCO's. Actually it is two back-to-back diodes which is reversed biased and the capacitance will decrease as the reverse biasing increases. No information on this component was found and is marked as TBD (to be determined).

In Chapter 5 this component is simulated for effective capacitance and unloaded Q.

3.1.2 MIM Capacitor

The MIM Cap. is drawn on Metal5 – insulator – TopMetal1.

In chapter 7 when doing EM-simulations it will become clear that this component is very dependent on frequency which is not shown in the model.

3.1.3 Bipolar Device

For this design the npn13p has been chosen for the bipolar device mainly because it has a high transit frequency, $f_t = 250$ GHz.

Device current for maximum transit frequency, valid for UCE = 1.2V and 1.2-2mA*Nx. Nx is the number of emitter fingers.

3.1.4 Resistor

The library contains three resistors. Because stability with temperature is considered RPPD is chosen, it is the most stable resistor in therms of temperature.

Chapter 4

Goals And System Requirements

This chapter contains two sections. In the first section earlier work on state of the art oscillators, transceiver chips and PLL's are compared. In the second section a OOK scheme is discussed and system goals are derived based on work done at UiB by Magnus Pallesen, Hans Schou, Magnus Ersdal and published work on transceivers.

4.1 Earlier Work On Oscillators

In Table 4.1 state of the art Millimeter Wave (MMW) oscillators specifications are shown. The oscillators ranges from 47-190 GHz, they consume everything from 57-250 mW and phase noise from -73 to -105 dBc/Hz at 1 MHz offset. The oscillators also differ in tuning range, output power and harmonic suppression.

Attributes\Articles	[34]	[31]	[32]	[33]	[21]	[25]	[13]	[30]
TPD(mW)	280	140	192	57	250	70	130	215
SSB(dBc/Hz) @ 1MHz	-105	-105	-104	-103	-99 @ 0.1MHz	-94	-80	-73
Ps(dBm)	3.9	3.5	0	-0.6	13.1	-	-0.5	-4.5
2.Harm. (dBc)	-30	-29	-39	-28	-	-	-	-15
Tuning %	2.2	6.1	2.1	9.7	-	-	3.8	3.9
f_{osc}(GHz)	82	75	47	72	47	122	100	190

Table 4.1: State of the art MMW oscillators.

In Table 4.2 oscillators that are used in transceivers and phase locked loops (PLL) designs are listed. These are in general more power friendly, in which is reflected upon the performance. The phase noise is larger and output power lower.

Normal SSB phase noise for a oscillator at 60 GHz is -85 dBc/Hz at 1 MHz offset [7].

Attributes\Articles	[9]	[2]	[5]	[23]	[19]	[27]	[16]
TPD(mW)	78	57	17.9	32	120	-	-
SSB(dBc/Hz) @ 1MHz	-80	-72	-80	-85	-85	-90	-90
Ps(dBm)	-7	-10	-8	-	-	-	-
2.Harm. (dBc)	-	-	-	-	-	-	-
Tuning %	3.3	9	-	15	8	12	7
f_{osc}(GHz)	60	50	135	52	60	60	60

Table 4.2: Oscillators specifications in receiver, transceiver and PLL design.

4.2 System Goals

In Figure 4.1 a on-off keying (OOK) scheme transceiver concept is illustrated. This concept has been developed in a collaboration with Magnus Ersdal who is working on the OOK modulator for the transmitter. In the next subsections we will take a look at the different components in the transceiver and derive the system goals based on this information.

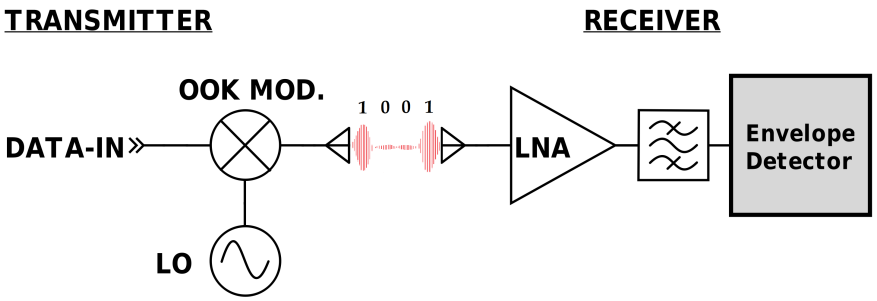


Figure 4.1: Transceiver concept for the OOK modulation.

4.2.1 Modulator

The modulator is basically a three staged Common Emitter amplifier that is turned on and off by the DATA-IN signal, therefore the term On-Off Keying. When it is turned on it amplifies the carrier frequency signal that is produced by the local oscillator (LO), the signal is then transmitted by the antenna. It has 50 dB on-off isolation with a -5 dBm input signal, meaning that the output of the modulator is 5 dBm when on and -45 dBm when off. Another requirement for the modulator is a maximum SSB of -60 dBc/Hz at 1 MHz offset for the LO.

4.2.2 Antenna

The antenna has not yet been designed, but gain larger then 9 dBi has been achieved in earlier work [1]. Covering the frequency range from 52.2 to 67.7 GHz by using directional patch antennas, $W\ x\ L$ = 2x3 mm^2.

4.2.3 Low-Noise Amplifier

The 60-GHz LNA designed by Magnus Pallesen in 2015/16 has 20.4 dB gain, BW = 57-66 GHz, 4.3 dB noise figure and 9.8 mW power consumption [14].

4.2.4 OOK Demodulator

There are various methods for designing OOK detectors with bit-error rates below 10^{-12} and data rates exceeding 10 Gbps [10, 8, 37, 4]. In the SiGe-130 nm technology a 10 Gbps demodulator has been achieved with input signal as low as -28 dBm and 9.7 dB gain [4].

4.2.5 Transmission Range Line Of Sight (LOS)

By using the Friis eq.4.1 in dB a estimate of transmission distance is presented in Figure 4.2. The transmitted power P_t = 5 dBm and the LNA has a gain of 20 dB. The figure shows the result with antenna gains of 3 dB, 9 dB and 28 dB. 28 dB gain is possible to achieve if using horn antennas [15].

On the y-axis, input-power received by the OOK Demodulator is shown. With a input power of -28 dBm we expect a data rate of minimum 4.5 Gbps and a bit-error rate of 10^{-12} based on the results by [10, 8, 37, 4].

$$P_r(dB) = G_r(dB) + G_t(dB) + P_t(dBm) - 10log\left(\frac{4\pi R}{\lambda}\right)^2 \tag{4.1}$$

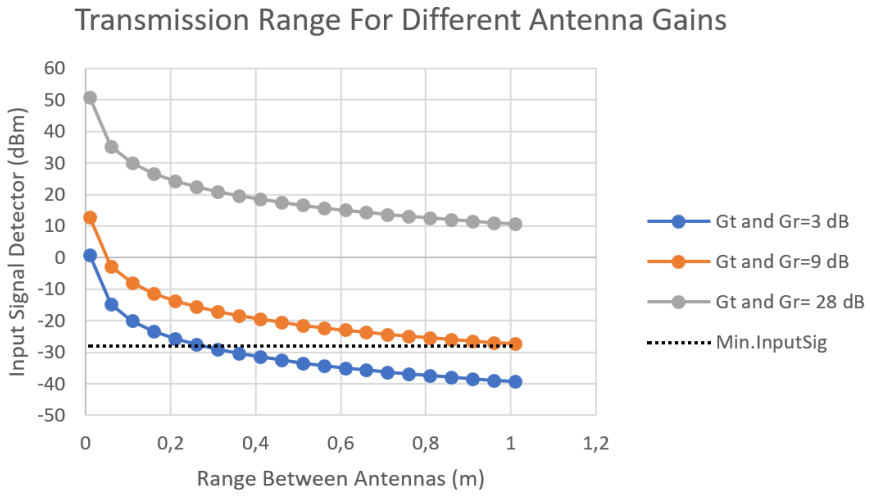


Figure 4.2: Input signal received by the OOK-demodulator (y-axis) and distance between antennas (x-axis).

4.3 Summary

Based on this information some system goals are proposed in Table 4.3. The total power consumption (TPD) is estimated to be 110 mW which can be categorized as a low power transceiver. In Table 4.4 expected transceiver performance is shown.

LO	Tuning range 10%	(SSB) -85 dBc/Hz @ 1 MHz offset	20 mW
LNA	20.4 dB gain	4.3 dB (NF)	10 mW
Modulator	10 dB gain	50 dB on-off isolation	40 mW
Detector	10 dB gain	Minimum -28 dBm input signal	40 mW
Tx	9 dB gain	small in size as possible	—
Rx	9 dB gain	small in size as possible	—

Table 4.3: Goal for different parts in the tranceiver.

BER	$\leq 10^{-12}$
Data Rate	$\geq$ 4.5Gbps
TPD	$\leq$110 mW
Operating BW	57-66 GHz
Transmission Range LOS (using patch antennas)	0.2-1 m
Transmission Range LOS (using horn antennas)	90 m

Table 4.4: Transceiver performance.

Chapter 5

Choosing Topology

The results presented in this chapter is the results from a second iteration of designing, realizing and verifying. The first time EM-simulation was not considered when designing. Because the resonator used in this thesis is highly dependable on microstrip lines, it was critically to do a thorough analysis of the resonator when choosing topology using EM-structures.

The chapter is divided into four sections and will be the foundation for choosing which type of oscillator to go forward with. The first three sections are based on the analysis of the open-loop cascade. By analyzing the amplifier and resonator as a cascade we can estimate the phase noise by using eq.2.38. By doing so, several hundred different combinations of oscillator setups can be analyzed without actually building them. This will give useful insight in terms of phase noise, output power, gain margin, loaded Q_L and how they behave with different combinations of amplifiers and resonators. Some simplification are done to make the analysis more comprehensible and so the results will work more as a guide line rather than a high precision design.

In the fourth section, a couple of oscillator setups from the open-loop cascade analysis are picked for Harmonic Balance (HB) and transient analysis. The circuit must be realized and the loop closed.

To calculate the phase noise a **nine-step method** was developed here at UiB based on oscillator methodology found in [22, 11, 20].

5.1 Amplifier Analysis

The amplifier should be stable, low noise and preform adequate gain.

Four different amplifier typologies are analyzed and considered, namely the Common Emitter (CE), Common Base (CB), Common Collector (CC) and the Cascode. The number of emitter fingers (Nx) is swept from 1-13, $I_C = 1.2mA * Nx$ and $V_{CE} = 1.2$ V. All measurements are preformed at 61.5 GHz because this is the center of the bandwidth

57-66 GHz and so it is chosen as the fundamental frequency. One of the goals for the LO is power consumption below 20 mW. This refers to the maximum of Nx = 13 when considering DC power for the CE, CC and CB, and Nx = 7 for the Cascode.

The CE stage has been made unconditional stable by using using two different techniques. One is with shunt feedback resistor, Figure 5.1, and the other is with a series feedback inductance, Figure 5.2. For the other three amplifiers there has not been preformed any feedback and they are only conditional stable meaning that they need a specific source and output termination to be stable and therefore need more simulation using stability circles if realized. The reason for not making them unconditional stable with feedback was because of loss in gain.

These four amplifier topologies have single ended outputs, a differential topology was also considered. A differential amplifier has certain advantages like high CMRR and high dynamic output range. This leads to a high signal-to-noise ratio (SNR) and is especially useful when dealing with a noisy substrate. However, the differential amplifier uses more components and more power then single-ended solutions, this will lower the yield and increase power consumption. Because the OOK is not very prone to phase noise and because we want a low power consumption this topology was discarded.

5.1.1 Common Emitter (CE) With Shunt Feedback

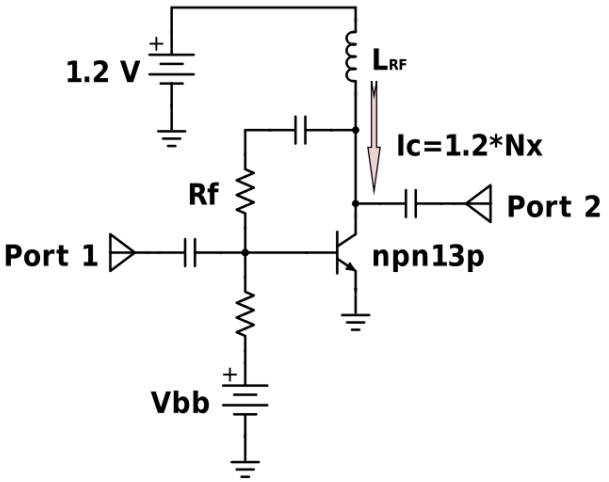


Figure 5.1: Common Emitter with shunt feedback resistor.

Rf is the feedback resistor and is varied to make the amplifier unconditional stable as the number of emitters changes, subsection 2.1.4. The capacitors serves as DC-block capacitors for the ports and L_{RF} is preventing RF-signals to get ac grounded.

From Table 5.1 we can see that the gain peaks at 6 fingers with almost 9 dB. This means that we could suffer an insertion loss of 6 dB through the resonator and still have

a 3 dB gain margin, given a perfect match, eq.2.20 and 2.8. The real part of the input and output impedance decreases as the number of fingers increases. This means that a series resonator will have a increase in Q_L as the number of emitters increase and a parallel resonator will have a decrease in Q_L.

Though the gain peaks at 6 fingers the amplifier delivers more power at 13 fingers which will affect the phase noise in a positive way.

Nx	Rf(ohm)	R_{input}(ohm)	R_{out}(ohm)	$\phi(degrees)$	$NF(dB)$	$G(dB)$	$f_t(GHz)$	$I_C(mA)$
1	3175	247	498	133	8.1	1.6	100	1.2
2	1580	118	248	123	6.1	6	190	2.4
3	1060	74	153	115	5.2	7.8	226	3.6
4	800	53	109	109	4.8	8.6	241	4.8
5	645	40	84	105	4.5	8.9	244	6
6	530	32	68	102	4.4	8.9	241	7.2
7	460	27	57	100	4.3	8.8	238	8.4
8	400	23	49	98	4.3	8.6	232	9.6
9	355	20	43	97	4.3	8.3	214	10.8
10	320	17	38	96	4.4	8.0	202	12
11	280	15	34	96	4.4	7.7	193	13.2
12	260	14	32	96	4.5	7.5	184	14.4
13	245	13	29	95	4.5	7.2	178	15.6

Table 5.1: Analysis of the Common Emitter With shunt feedback resistor. The number of emitters is varied from 1-13.

5.1.2 Common Emitter (CE) With Series Feedback

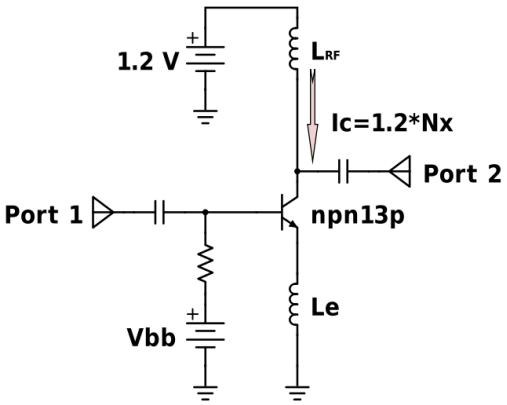


Figure 5.2: Common Emitter with series feedback inductance.

In Figure 5.2 L_e the series feedback inductance is used to make the stage unconditional stable. L_e also works as a low-pass filter, the higher the frequency the more negative feedback. L_{RF} blocks RF-signal and the capacitors blocks the DC-signal. The resistor is used to adjust V_{BE} for different numbers of emitters. In Table 5.2 we expect much of the

same results as for the CE with shunt feedback given the same topology. However the noise factor is somewhat lower and the gain peaks at Nx = 8 rather with 9 dB gain. The noise factor is somewhere between 0.5-1 dB lower at all fingers. The phase is also a bit lower meaning that we will not need so much coupling from the resonator in order to get a steep phase slope at phase-zero, subsection 2.2.5.

Emitters Nx	Le(pH)	R_{input}	R_{out}	$\phi(degrees)$	$NF(dB)$	$G(dB)$	$f_t(GHz)$	$I_C(mA)$
1	80	218	300	117	7.5	0.2	67	1.2
2	45	110	180	107	5.5	5	145	2.4
3	30	70	128	100	4.6	7.1	200	3.6
4	25	54	102	94	4.1	8	226	4.8
5	20	42	84	89	3.8	8.6	241	6
6	15	33	69	87	3.6	8.9	250	7.2
7	15	29	62	83	3.5	8.9	245	8.4
8	10	26	56	82	3.5	9	245	9.6
9	10	24	49	81	3.4	8.7	230	10.8
10	10	19	41	79	3.4	8.6	220	12
11	8	17	37	78	3.5	8.3	210	13.2
12	8	15	34	77	3.5	8	205	14.4
13	6	13	31	77	3.6	7.9	196	15.6

Table 5.2: Analysis of the Common Emitter With series feedback inductance. The number of emitters is varied from 1-13.

5.1.3 Amplifier Summary

The CC, CB and Cascode was not as stable as the CE. This made them rather unpredictable and they were not chosen to go forward with, but simulation results can be found in APPENDIX A. If the goal however was to make a negative resistance/conductance oscillator these typologies would have been preferred, sec.2.6.

The CE with series feedback has fewer components and better noise factor than the Common Emitter with shunt feedback. Because of this the Common Emitter with series feedback is chosen to be the sustaining stage for the oscillator.

5.2 Resonator Analysis

The Common Emitter has relatively low input and output impedance especially when increasing the number of emitter fingers, Table 5.2. However they are quite similar, and so the coupled series and parallel resonator is a good choice section 2.2.5.

When looking at Table 5.2 the phase is positive and so we need to shift the phase down. For this phase shift we can either use the Coupled Parallel Resonator with series inductance or the Coupled Series Resonator with shunt capacitance, section 2.2.5.

When realizing the components of the resonator there are several ways in which to do so. For these two resonators the MIM capacitor has been chosen for capacitance, a me-

ander microstrip inductor has been chosen as the inductance for the series resonator and a simple shunt microstrip lines has been chosen for inductance in the parallel resonator.

When making a good resonator Q_R value is very important because Q_U is limited by this, eq.2.20. The Q_R value is determined by the quality of the components in the resonator and is a measure of how good the components can hold on to energy. See APPENDIX B simulated, unloaded Q results for different components.

Next the series and parallel resonator components are simulated for Q_U using EM structures. By doing EM-simulations we will get more accurate results than by just using the models from the vendor, subsection 3.0.3. When simulating the goal is to achieve a high Q_U, while keeping the reactance high for the series resonator and low for the parallel resonator.

5.2.1 The Coupled Parallel Resonator Unloaded Q

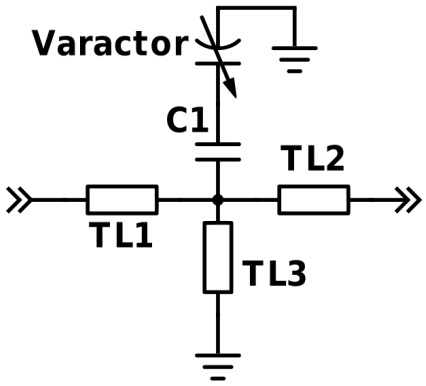


Figure 5.3: Coupled parallel resonator with series inductance and varactor for tuning.

The resonator in Figure 5.3 is composed by a varactor in series with a MIM capacitor C1, a shunt microstrip TL3 as the inductive element and two microstrip lines for inductive coupling, TL1 and TL2. The C1 will serve as a DC-block, preventing the varactor from getting forward biased. The varactor has a rather poor Q_U, APPENDIX B. By placing C1 in series with the varactor it will decrease the effective tuning capabilities, but also increase Q_U.

First the Q_U value for TL3 will be simulated for possible inductance values Table 5.3. The width of TL3 was set to 60 μm and is drawn on layer TM2_M1 because this gave the best Q_U. In Table 5.4 calculated values for the varactor in series with the MIM capacitor are chosen so that it is possible to tune from 57-66 GHz. 8 varactors are placed in parallel to get a sufficient tuning range of approximately 10-15%. For the varactor 10 columns were chosen, width = 9.74 μm and length = 0.8 μm.

Width	Length	Inductance pH	Unloaded Q-EM	Tune 57-66 GHz (pF)
60	50	8	22.8	0.98-0.73
60	60	9	22.7	0.87-0.65
60	70	11	23	0.71-0.53
60	80	13	23.2	0.60-0.45
60	90	14	23.3	0.56-0.42
60	100	16	23.1	0.49-0.36
60	110	18	23	0.43-0.32
60	120	20	23	0.39-0.29
60	130	21	22.9	0.37-0.28
60	140	23	22.0	0.34-0.25
60	150	25	22.0	0.31-0.23
60	160	27	21.9	0.29-0.21
60	170	29	21.7	0.27-0.20
60	180	31	21.5	0.25-0.19
60	190	33	21.3	0.24-0.18

Table 5.3: Unloaded Q for the shunt microstrip line, parallel resonator.

Col.	Width	Length	MIM Cap (pF)	Tot.Cap. (pF)	Q_U	Nom.Q_U
10	9.74	0.8	3.76	1.01-0.59	4.8-7.6	6
10	9.74	0.8	2.37	0.88-0.54	5.6-8.3	6.8
10	9.74	0.8	1.46	0.71-0.47	6.9-9.4	8
10	9.74	0.8	1.09	0.61-0.42	8.0-10.5	9.2
10	9.74	0.8	0.94	0.56-0.40	8.7-11.1	9.8
10	9.74	0.8	0.76	0.49-0.36	9.9-12.2	11.0
10	9.74	0.8	0.63	0.44-0.33	11.2-13.4	12.3
10	9.74	0.8	0.55	0.39-0.31	12.5-14.6	13.6
10	9.74	0.8	0.51	0.37-0.29	13.1-15.1	14.1
10	9.74	0.8	0.45	0.34-0.27	14.3-16.2	15.4
10	9.74	0.8	0.41	0.31-0.26	15.5-17.3	16.6
10	9.74	0.8	0.37	0.29-0.24	16.6-18.4	17.7
10	9.74	0.8	0.33	0.26-0.22	18.2-19.8	19.2
10	9.74	0.8	0.30	0.25-0.21	19.6-21.0	20.6
10	9.74	0.8	0.29	0.24-0.21	20.3-21.7	21.3

Table 5.4: Unloaded Q, varactor setup for the coupled parallel resonator.

5.2.2 The Coupled Series Resonator Unloaded Q

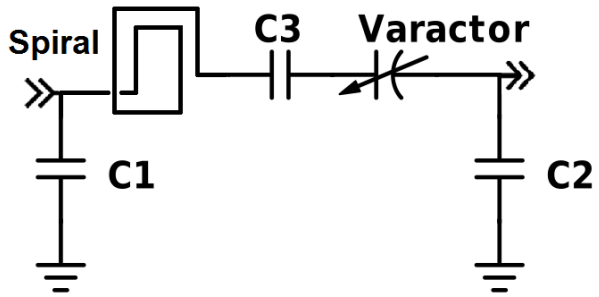


Figure 5.4: Coupled series resonator with shunt capacitors and varactor for tuning.

The resonator in Figure 5.4 contains two MIM capacitors C1 and C2 for coupling, one varactor for tuning with a DC-block capacitor C3 and one spiral inductor made of microstrip. C3 is to prevent the varactor from getting forward biased.

In Table 5.5 Q_U for the meander inductor is simulated for different possible values. The width and spacing was chosen to give the best possible Q_U while keeping a high level of inductance.

In Table 5.6 Q_U for a varactor with a series MIM cap has been simulated. The values for the varactor in series with the MIM capacitor will correspond to a tuning range from 57-66 GHz with meander inductor. For the varactor 10 columns were chosen, width = 9.74 μm and length = 0.8 μm.

Turns	Width	Spacing	L1/Ln	L2/L3	nH	Q_U	Tune 57-66 GHz (pF)
1	15	5	45	90	0.19	19.6	0.041-0.031
1	15	5	50	100	0.24	19.6	0.033-0.024
1	15	5	55	110	0.29	19.1	0.027-0.020
1	15	5	60	120	0.34	18.3	0.023-0.017
1	15	5	65	130	0.41	17.3	0.019-0.014
1	15	5	70	140	0.49	16	0.016-0.012
1	15	5	75	150	0.58	14.6	0.013-0.01
1	15	5	80	160	0.70	12.6	0.011-0.008
1	15	5	85	170	0.84	10.9	0.009-0.007

Table 5.5: Unloaded Q for spiral inductor, microstrip layer TM2_M1(topmetal2-metal1).

Col.	Width	Length	MIM Cap (pF)	Tot.Cap. (pF)	Q_U	Nom.Q_U
10	3.74	0.8	0.098	0.043-0.031	9.3-11.9	10.7
10	3.74	0.8	0.059	0.033-0.025	12-14.4	13.3
10	3.74	0.8	0.042	0.027-0.022	14.9-17	16.2
10	3.74	0.8	0.033	0.023-0.019	17.5-19.4	18.8
10	3.74	0.8	0.026	0.019-0.016	20.7-22.3	21.9
10	3.74	0.8	0.020	0.016-0.014	25.2-26.4	26.3
10	3.74	0.8	0.015	0.013-0.012	31.2-31.9	32.2
10	3.74	0.8	0.013	0.011-0.010	35.7-36.0	36.7
10	3.74	0.8	0.010	0.009-0.008	44.5-44.0	45.3

Table 5.6: Varctor setup for series resonator.

5.3 Calculating Phase Noise

The results from analyzing the sustaining stages and resonators is now used to calculate the phase noise. For the sustaining stage the Common Emitter with Series feedback resistor has been chosen. Two different resonators will be considered, the Coupled Series Resonator using shunt capacitor and the Coupled Parallel Resonator using series inductor.

The results for single sideband phase noise (SSB), output power (Ps), lossy loaded Q (Q_L) and gain margin (GM) will be shown in a graph for different numbers of emitter fingers, Nx = 2-13. For every emitter finger the values from the resonator analysis are plotted on the x-axis and SSB, lossy-loaded Q, Output Power and Gain Margin on the y-axis. By doing this a visual plot of how the parameters behave in terms of resonator and amplifier setup will be revealed. For the parallel resonator a total of 180 different configurations will be shown and 111 for the series resonator.

A **9-Step-Method** for calculating SSB, lossy-loaded Q, Output Power and Gain Margin has been developed based on oscillator methodology found in [22, 11, 20]. So before we continue a short introduction to this method is given, calculating one configuration.

5.3.1 Example: 9-Step-Method

For the example, Nx = 6 will be used and results from amplifier analyze can be found in Table 5.2,

- $R_{in} = 33$ ohm, $R_{out} = 69$ ohm, $\phi = 87^0$, NF = 3.6 dB, Gain = 8.9 dB and $I_C = 7.2$ mA

A coupled parallel resonator has been chosen Figure 5.3, component values can be found in Table 5.3 and 5.4. For this example these values were chosen,

- TL3 = 20 pH with Q_U = 23 and the Varactor in series with MIM cap. = 0.39-0.31 pF with a nominal Q_U = 13.6

Nine steps on how to estimate SSB, lossy-loaded Q, Output Power and Gain Margin from the open-loop cascade:

1. Find the coupling reactance that will make the maximum phase-slope cross ϕ_0.
   The phase for the CE is 87^0 so the phase needs to be shifted down 87^0.
   Using eq.2.25 and solving for L using the same amount of coupling on each side, we get
   L1 = L2 = 0.12 nH

2. Now that we know the coupling inductance L = 0.12 nH we can estimate the lossless loaded Q, eq.2.15
   $Q_P = \frac{R_{total}}{X_P}$ where,
   $R_{total} = R_{p1} \,||\, R_{p2} = \frac{R_{in}^2+X_L^2}{R_{in}} \,||\, \frac{R_{out}^2+X_L^2}{R_{out}} = \frac{33^2+\left(2\pi*61.5*10^9*L\right)^2}{33} \,||\, \frac{69^2+\left(2\pi*61.5*10^9*L\right)^2}{69}$ and
   $X_p = \frac{R_{in}^2+X_L^2}{X_L} \,||\, \frac{R_{out}^2+X_L^2}{X_L} \,||\, 2\pi*61.5*10^9*20*10^{-12}$ and so the lossless Q becomes
   $Q_{L-Lossless} = 7.2$.
   This will not accommodate for the frequency shift given by the coupling inductor and so the calculated reactance will be slightly off .

3. Next the unloaded Q_R for the resonator is calculated, eq.2.19
   $Q_R = \frac{1}{1/Q_{ind}+1/Q_{cap}} = \frac{1}{1/23+1/13.6} = 8.5$.
   This does not consider the Q_U for the coupling inductors.

4. Now the lossy loaded Q_L can be found using eq.2.21,
   $Q_{L-Lossy} = \frac{1}{1/Q_R+1/Q_{L-Lossless}} = 3.9$

5. Next the insertion loss is calculated, eq.2.20
   $IL = 20log\frac{Q_R}{Q_R-Q_{L-Lossless}} = 5.3$ dB.

6. The gain margin is found by subtracting IL from the gain of the amplifier,
   GM = 8.9-5.3 = 3.6 dB.

7. The output power is set to be approximately 5 % of what the amplifier can deliver at 3.6 dB compression,
   $P_s = -6.5$ dBm. (This requires a nonlinear analyses of the CE stage)

8. Find the corner flicker noise frequency and the noise factor NF from amplifier analyze,
   $f_c = 3.3$ kHz and
   NF = 3.6 dB.

9. Finally use these steps to calculate the phase noise at f_m =1 MHz offset.
   $L(fm) = 10log\left[\frac{1}{2}\left(1+\frac{3300}{10^6}\right)\left(1+\left(\frac{61.5*10^9}{2*10^6*3.9}\right)^2\right)\left(\frac{2.3*1{,}38*10^{-23}*300}{0.00045}\right)\right] = -88.8$ dBc/Hz
   at 1 MHz Offset

5.3.2 Common Emitter With Coupled Parallel resonator

In this section the **9-Step-Method** will be used to analyze 180 different scenarios for the Common Emitter With Coupled Parallel Resonator.

In Figure 5.5 the results from the Common Emitter With Coupled Parallel Resonator open-loop cascade are presented. By looking at the gain margin plot one can see which values of capacitance is possible to use without breaking the Barkhausen's Criterion, the initial gain margin must be greater than 0 dB at ϕ_0. Remember that though the criterion was 0 dB it was recommended that GM $\geq$ 3 dB. This is reflected upon the phase noise plot were the SSB peaks for a gain margin between 3-4 dB. When the gain margin gets to low, GM < 2 dB, we can see that both the output power and SSB drops significantly.

The gain margin decreases with higher capacitance as expected because of a increase in insertion loss. The gain margin is also higher for a larger number of emitter fingers, though the gain from the amplifier reaches a peak at Nx = 8. This is because the input/output impedance of the amplifier is lower for a high number of Nx and will decrease the loaded Q. This will then give a lower insertion loss and the gain margin will rise.

The $Q_{L-Lossy}$ reaches a peak (bottom) Figure 5.5. The $Q_{L-Lossy}$ is dependent on the $Q_{L-Lossless}$ and Q_R , eq.2.21. Because $Q_{L-Lossless}$ will increase with higher capacitance and because Q_R will decrease with higher capacitance $Q_{L-Lossy}$ reaches a peak. The only exception is for Nx = 2. Because of the relatively high input/output impedance of the amplifier, $Q_{L-Lossless}$ is high and $Q_{L-Lossy}$ response is more or less only dependent on Q_R.

At this point Nx = 8 with 0.35 pF capacitance seems like a good choice for several reasons, GM = 4.8 dB, SSB = -89 dBc/Hz at 1 MHz Offset, Ps = -5 dBm and it only consumes 11.5 W DC-power. For Nx = 8 calculations states that the coupling inductance should be 0.085 nH to make the phase-slope cross 0 dB, eq.2.31.

5.3.3 Common Emitter With Series Resonator

In this section the **9-Step-Method** will be used to analyze 111 different scenarios for the Common Emitter With Coupled Series Resonator.

In Figure 5.6 the results from the Common Emitter with Coupled Series Resonator are presented.

As apposed to the parallel resonator the gain margin for the series resonator decreases with a higher number of emitter fingers. This is because the loaded Q increases as the input/output impedance decreases. As a result of this the insertion loss will increase, making the gain margin lower. The phase noise and output power increases to certain point where the gain margin is to low.

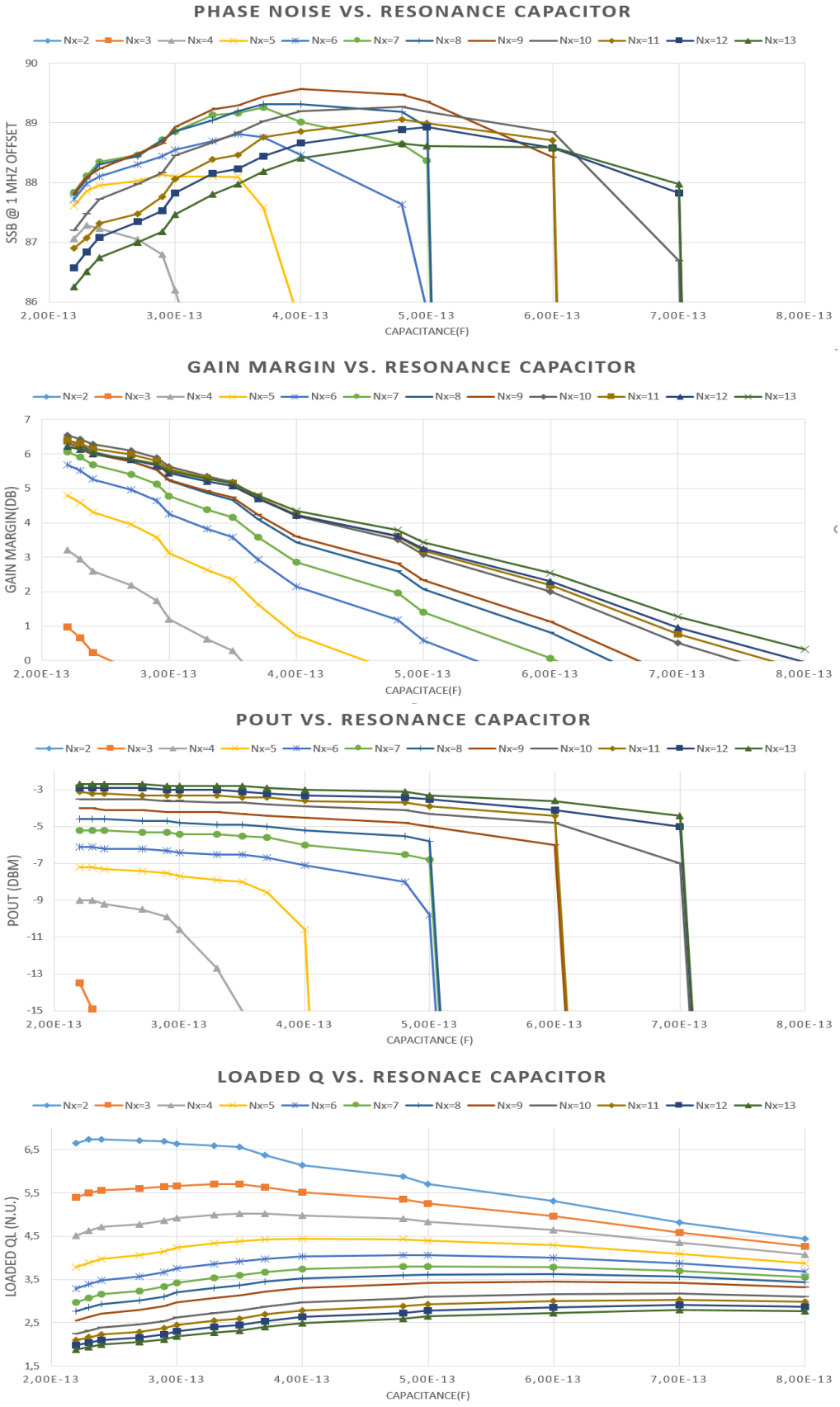


Figure 5.5: Phase Noise for Common Emitter with coupled parallel resonator.

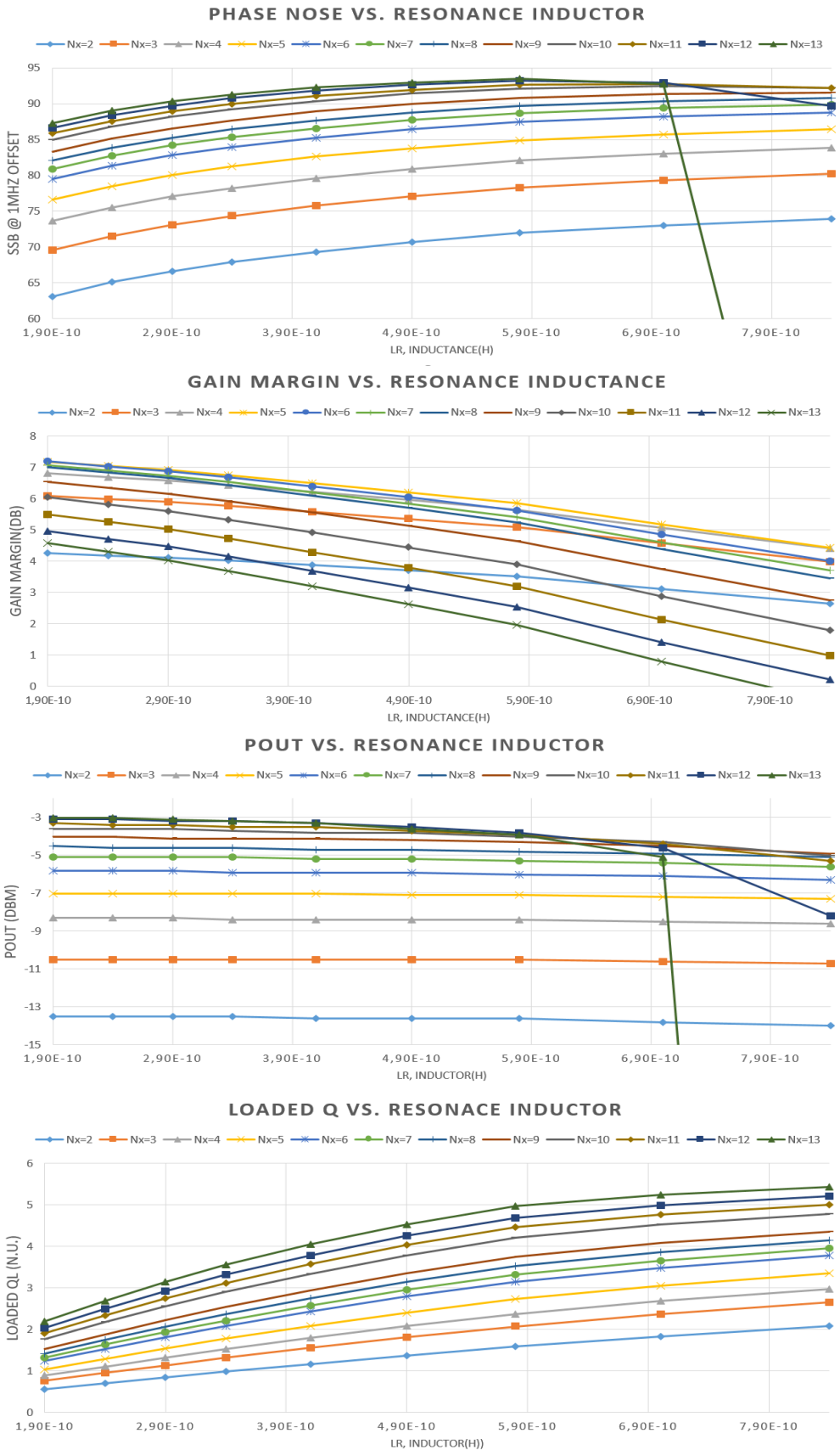


Figure 5.6: Analyze of Common Emitter with coupled series resonator

When the gain margin is to low, because of the high loaded Q, the amplifier delivers insufficient amounts of power and oscillations are no longer sustained. This can be seen by a sudden drop in output power and phase noise.

Nx = 8 with a resonating inductance of 0.7 nH seems like a good choice because GM = 4.5 dB, SSB = -89 dBc/Hz at 1 MHz, Ps = -4 dBm and it only consumes 11.5 W DC-power. For Nx = 8 calculations states that the coupling capacitance should be 0.058 pF.

5.4 Nonlinear Verification

In this section the two oscillators setups, one with series resonator and one with parallel resonator will be realized with the component values found in the previous section. The coupling reactors unloaded Q was not considered when doing the analysis of the open-loop cascade and so ideal coupling will be used.

To simulate these circuits we will use the APLAC Harmonic Balance (HB) simulator, provided by Microwave Office, see subsection 3.0.2 for more information on tools used for simulations.

5.4.1 Common Emitter with Coupled Parallel Resonator

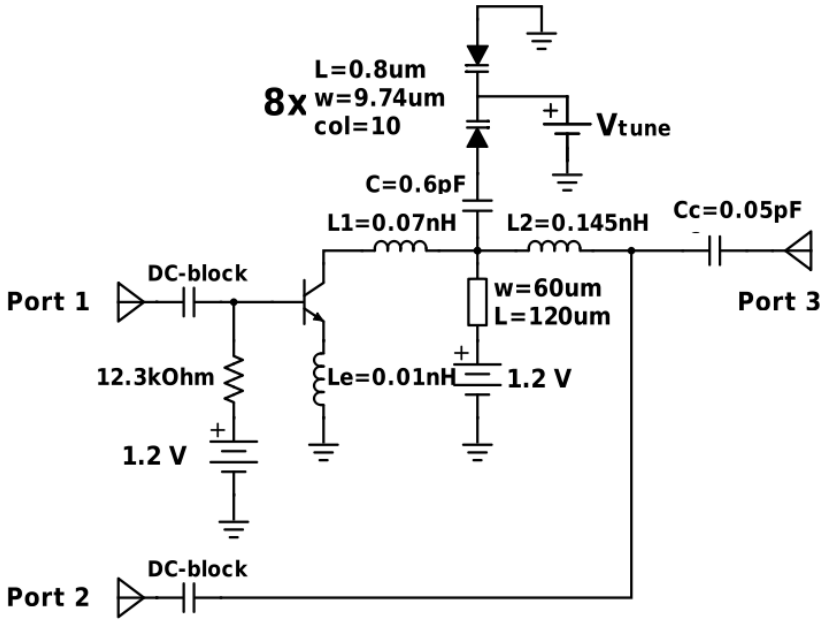


Figure 5.7: Common Emitter with Coupled Parallel Resonator, Nx = 8.

When forming the oscillator the loop is closed and one of the DC-block capacitors in Figure 5.7 is removed.

In Table 5.7 results from the open-loop calculations and Harmonic Balance (HB) simulations are shown, before and after tuning.

The results from the HB simulation before tuning differs a lot from the results found in calculations because no matching has yet been done. The gain margin is higher than expected, which is reflected upon the output power which is also higher. The oscillating frequency is 69 GHz when 61.5 GHz was the goal, this is the result of not considering the frequency shift invoked by the coupling inductors in calculations. By applying eq.2.8 we see that the bode plot is pessimistic by 1.6 dB. This means that the actual GM is 6.6 dB.

After tuning the circuit with only using L_1 and L_2, new results were obtained, (bottom) Table 5.7. The equation for MismatchError now shows us that the bode plot is pessimistic by 0.9 dB which is an improvement in the right direction. Considering this, the actual gain margin is 4.4 dB and is more close to the one predicted of 4.8 dB. The SSB is 7 dB higher than predicted which can be improved when optimizing the oscillator, if chosen to go forward with.

Component values after tuning are shown in Figure 5.7. The total series capacitance, is the 8 parallel varactors in series with the 0.6 pF MIM capacitor.

Setup	SSB	Q_L	Ps(dBm)	GM(dB)	f_0(GHz)	Tune(GHz)	ME(dB)
Calculations	-89.0	3.4	-5.0	4.8	61.5	9.0	–
Before Tuning	-69.5	2.2	0.8	5.0	69	7.0	1.62
After Tuning	-82	3.0	-3.4	3.5	61.5	6.5	0.91

Table 5.7: Results from the Common Emitter with Coupled Parallel Resonator, Nx = 8. "Calculations" are from the open-loop cascade and "Before Tuning" and "After Tuning" are Harmonic Balance simulations.

5.4.2 Common Emitter with Coupled Series Resonator

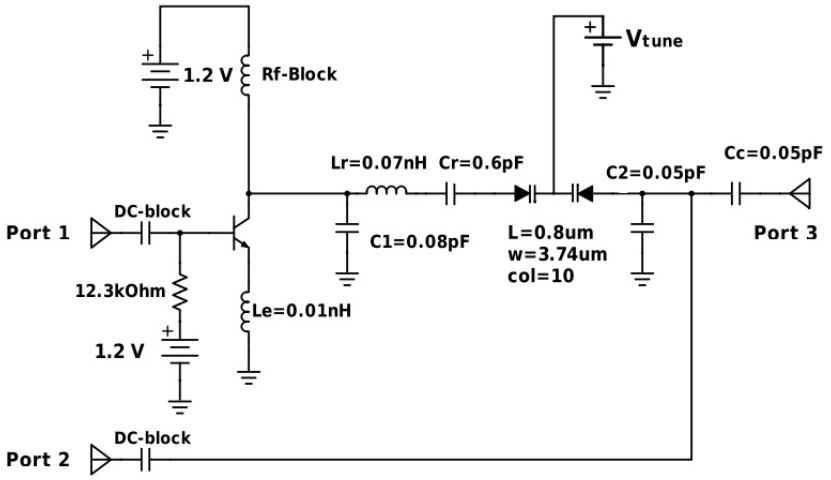


Figure 5.8: Results from the Common Emitter with Coupled Series Resonator, Nx = 8. "Calculations" are from the open-loop cascade and "Before Tuning" and "After Tuning" are Harmonic Balance simulations.

The same procedure as for the parallel resonator was done here and the results are presented in Table 5.8. The simulated circuit in Figure 5.8 is shown with values used after tuning.

Before tuning, the output power is lower than expected as a consequence of the low gain margin. The Q_L is larger then expected which again explains the low gain margin. When Q_L is large it increases the insertion loss, hence the low gain margin. The oscillating frequency is also to high. This indicates that the calculated resonating capacitance is to low and the coupling capacitors to high.

Components values after tuning are shown in Figure 5.8. Gain margin and output power is increased to acceptable values, but the phase noise deviates by 11.7 dB from the calculated values. The main reason for the high phase noise is because we had to decrease the resonating inductance due calculation errors. This increased the gain margin, but decreased Q_L and so the SSB was affected in a negative way. Still it is better than before tuning because of higher output power due to the gain margin.

Setup	SSB	Q_L	Ps(dBm)	GM(dB)	f_{osc}(GHz)	Tune (GHz)	ME(dB)
Calculations	-90.2	4.0	-1.5	4.5	61.5	9.0	–
Before Tuning	-82.4	6.3	-12.0	0.7	63.3	1.5	-0.6
After Tuning	-78.5	4.8	-4.5	3.0	61.5	3.0	0.4

Table 5.8: Results from simulating the CE with CS resonator using component values from calculations (upper part) and after tuning (lower part).

5.5 Summary Choosing Topology

Two oscillators has been made, the Common Emitter With Coupled Parallel Resonator and the Common Emitter With Coupled Series Resonator. They have some similarities such as the sustaining stage and they both use coupling. The parallel resonator shows better results, but the series resonator do not need as many varactors to make a significant impact on the tuning range. Because the resonators are very different in layout and because they have different features, both oscillators will be realized and optimized in the next chapter. This will give a better understanding of what impact non-ideal components have on the performance.

Chapter 6

Layout and Optimizing

This chapter contains two sections. In the first section, layout of both oscillators chosen in the previous chapter are fully realized and results are presented. In the second section the oscillators are optimized.

6.1 Layout

When realizing the oscillators all connections are made of microstrip. Because the resonator also is made of microstrip and drawn on TM2_M1, it is natural to use this layer for the connections to avoid to many vias. As elements are replaced the oscillators will be constantly tuned to make the results as similar to the ones obtained in the previous chapter. All microstrip components are EM-simulated because a lot of the circuitry is made of microstrip. By doing this the results will not deviate so much when a final, more thorough EM-simulation is done later. Also a design rule check (DRC) is used verify the layout. The DRC contains separation rules, maximum/minimum widths etc. for every layer that is used in the design. This is process specification rules and assures that the circuit that has been designed, also can be made on a wafer. This DRC test was made from the documentation that followed the SG13s process. By using Cadence this test is included and is more advanced.

6.1.1 Realizing the Common Emitter (Nx = 8) with Coupled Parallel Resonator

All connections are made using microstrip. The lengths and widths off all microstrip components are given in Figure 6.2 and is drawn on TM2_M1. The 5 kOhm Rppd resistor, F) Figure 6.1, utilizes unsalicided, p-doped gate polysilicon as resistor material. For realizing precision resistors, a line width of 2 µm or higher is recommended by IHP. Looking at resistance versus temperature in the documents for SG13s one can also see that the Rppd is by far the most stable one in therms of temperature. The Le inductor, D) Figure 6.1, has been replaced with microstrip lines with equivalent inductance drawn on TM2_M1, more information on this topic see APPENDIX D. For capacitance the MIM

(Metal5 – insulator – TopMetal1) capacitor is used. The 1.36 pF, C) Figure 6.1, capacitor blocks DC from VCC. The 0.3 pF, A) Figure 6.1, degenerates the capacitive effect from the varactor and at the same time it makes the unloaded Q better when looking at the resonating capacitance as a whole, it also blocks DC signals preventing the varactor from getting forward biased.

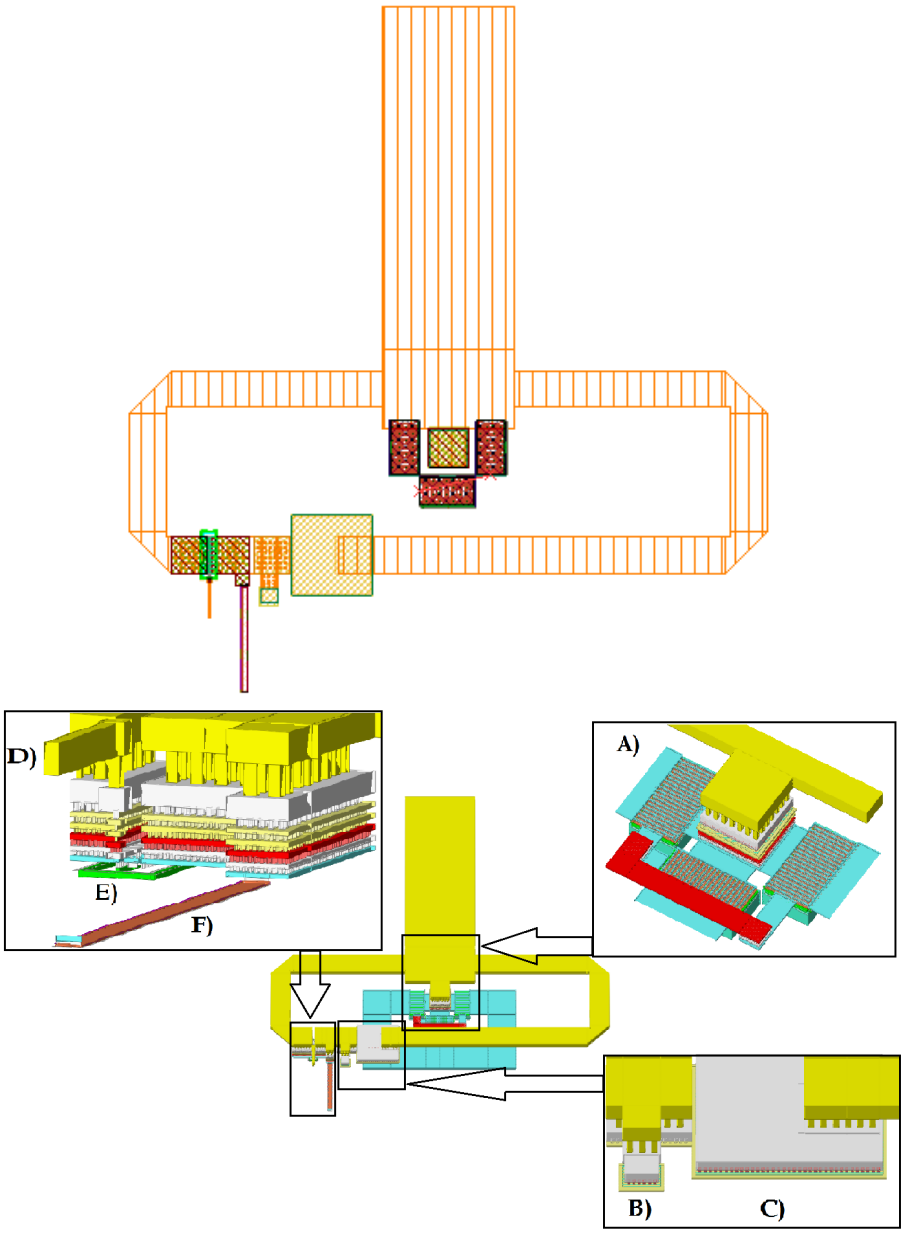


Figure 6.1: Layout, 2D and 3D, of the Common Emitter (Nx = 8) with Coupled Parallel Resonator.

Three varactors, A) Figure 6.1, are placed in parallel to increase the tuning range. The tuning ranges from 59-65.1 GHz with 0 V applied being the lowest frequency and 2 V being the highest. It can also be specified as 3.05 GHz/V, see table 6.1 for results.

For output coupling a 60 fF capacitor, B) Figure 6.1, is connected to a 50 ohm port. The npn13p, E) Figure 6.1, uses 8 emitter fingers. Final results are presented in Table 6.1 and Figure 6.3. Total area usage is approximately 0.051 mm^2.

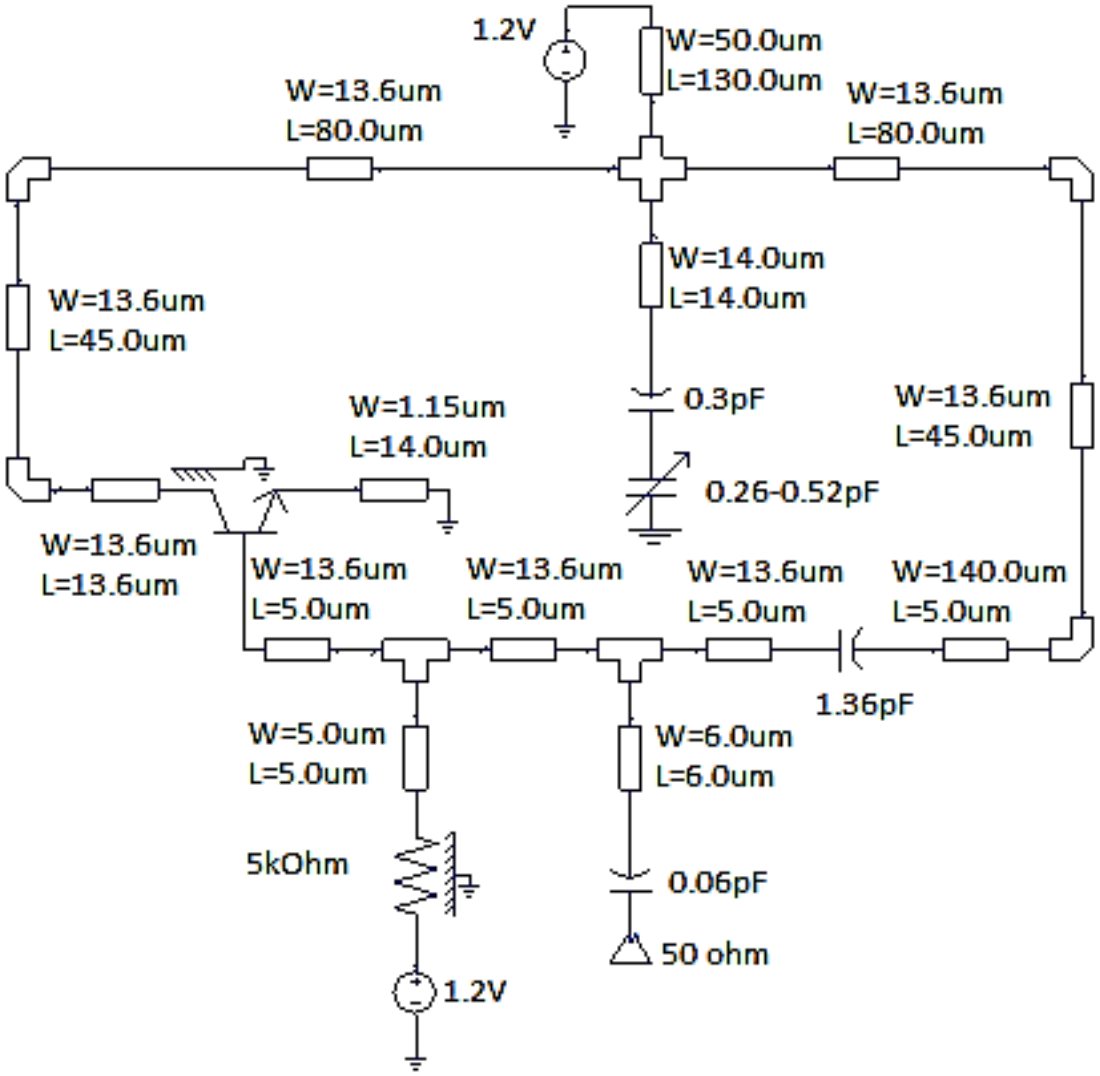


Figure 6.2: Schematic for the Common Emitter (Nx = 8) with Coupled Parallel Resonator.

Looking at Table 6.1 one can see that the SSB decreases as the as the oscillating frequency increases, this is because Q_L increases. The Q_U for the varactor also increases when voltage is applied because the effective capacitance decreases as the reversed bias voltage is increased, APPENDIX B, Table B.4. The gain margin however decreases which can be seen as result of lower output power because insertion loss increases as Q_L increases, eq.2.20. This leads to less compression when nonlinear action occurs and hence less output power.

In Figure 6.3 we can see from the output spectrum and waveform that the harmonic content is rather high. The output power is also a bit to low, but this can be fixed with a

buffer and filter if this oscillator chosen to go forward with. The upper part of the output waveform is approximately 0.24 V and the lower part is approximately -0.12 V. This is the result of an unbalanced input stage which can be fixed with proper biasing, in this case raising V_{BE}.

Varactor Volt	SSB @ 1MHz	SSB @ 10MHz	Ps(dBm)	GM(dB)	f_{osc}(GHz)
0	-64.2	-112	-6.5	3.5	59
0.2	-67.5	-115	-6.9	3.4	59.7
0.4	-71.4	-116	-7.4	3.3	60.7
0.6	-73.7	-118	-7.9	3.1	61.7
0.8	-74.9	-119	-8.3	3	62.5
1.0	-75.6	-120	-8.6	2.9	63.2
1.2	-75.9	-120	-8.9	2.8	63.7
1.4	-76.2	-121	-9.1	2.7	64.2
1.6	-76.3	-121	-9.3	2.6	64.6
1.8	-76.4	-121	-9.4	2.6	64.9
2.0	-76.5	-121	-9.5	2.55	65.1

Table 6.1: Results after realizing the Common Emitter (Nx = 8) with Coupled Parallel Resonator.

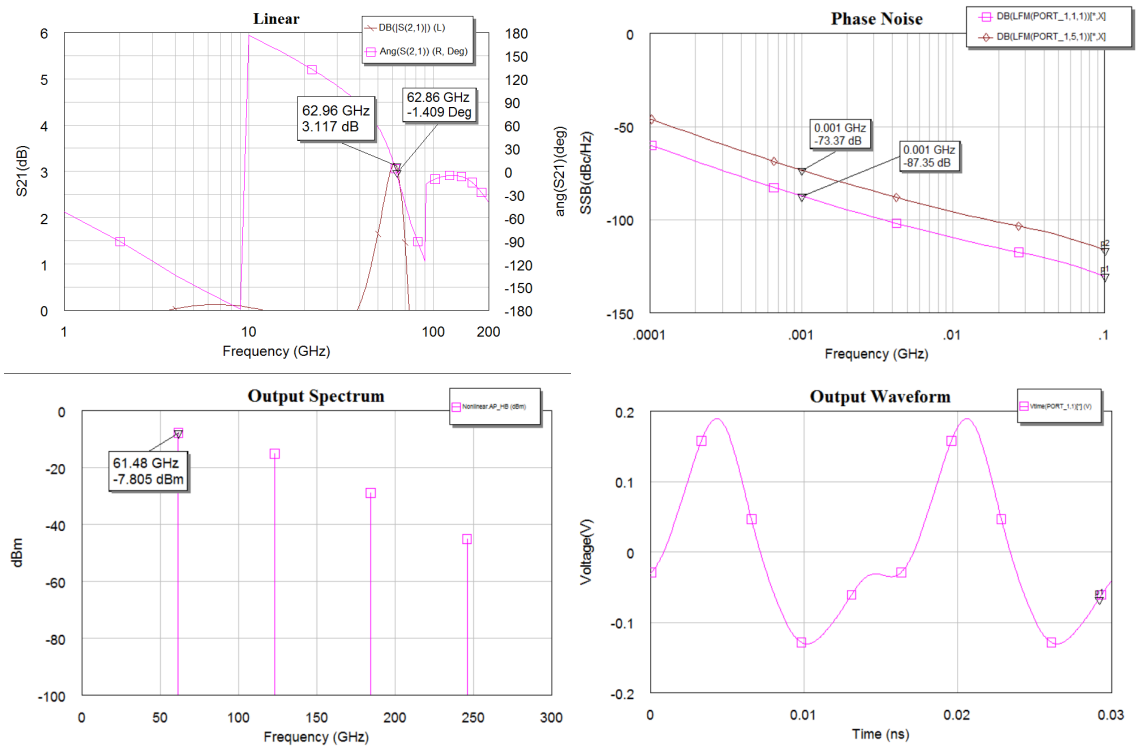


Figure 6.3: Simulation plots at 61.5 GHz after realizing the Common Emitter (Nx = 8) with Coupled Parallel Resonator.

6.1.2 Realizing Common Emitter (Nx = 8) with Coupled Series Resonator

As for the parallel resonator all connections where made using microstrip, layer TM2_M1 Figure 6.46.5.

In Figure 6.5 a 2D and 3D layout is shown. The meander inductor A) was mainly realized in TM2_M1, but for the bridge TM1_M1 was used. The large Rf-block inductor B) has been replaced with a thin long microstrip line. The npn13p is placed at C) and is the bias resistor at D). The DC-block MIM capacitor at E) and the output coupling MIM capacitor at F). The two shunt coupling capacitors are actually different in size, but are represented by one figure G). The varactor is placed at H).

The layout in Figure 6.5 area usage is approximately 0.038 mm^2.

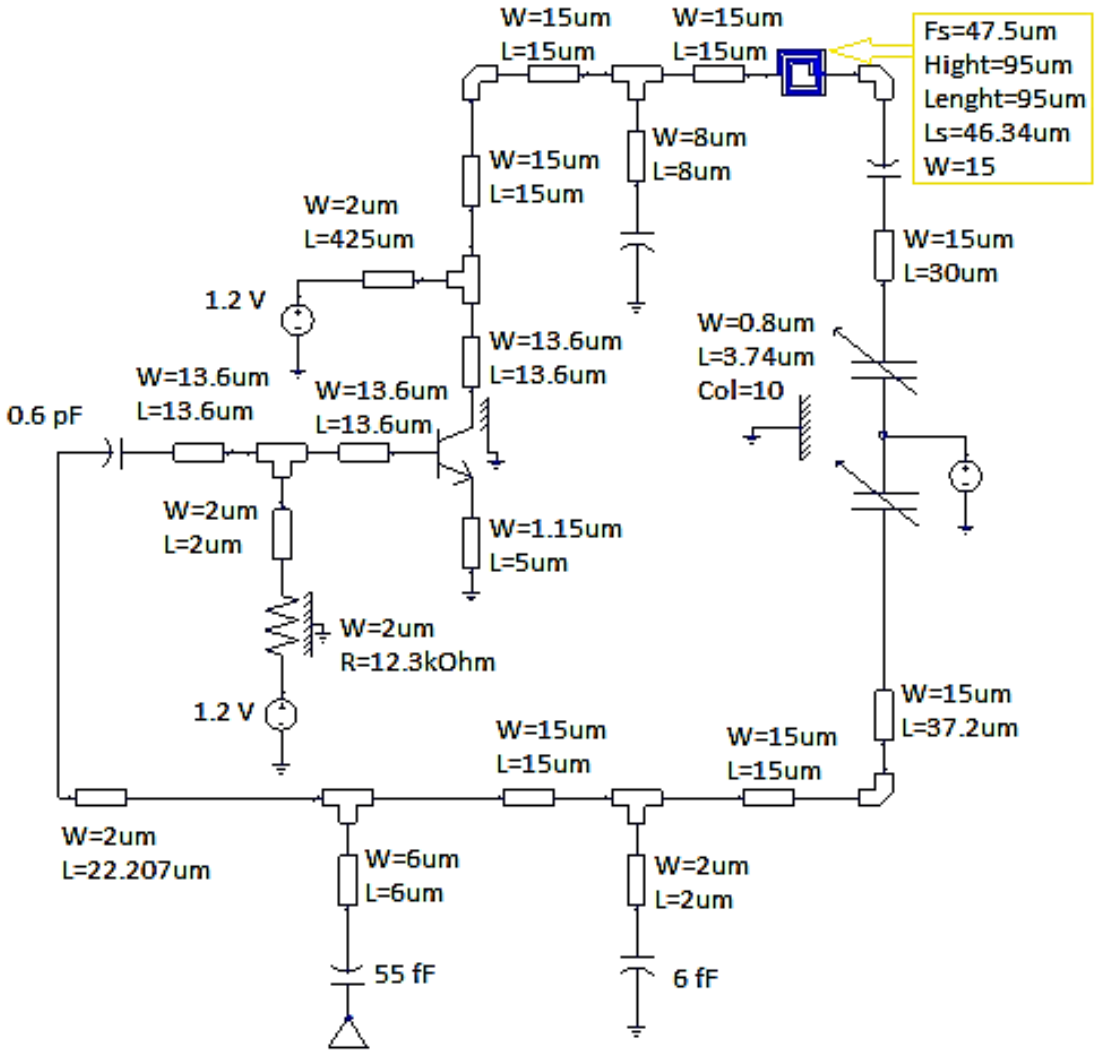


Figure 6.4: Common Emitter (Nx = 8) with Coupled Series Resonator.

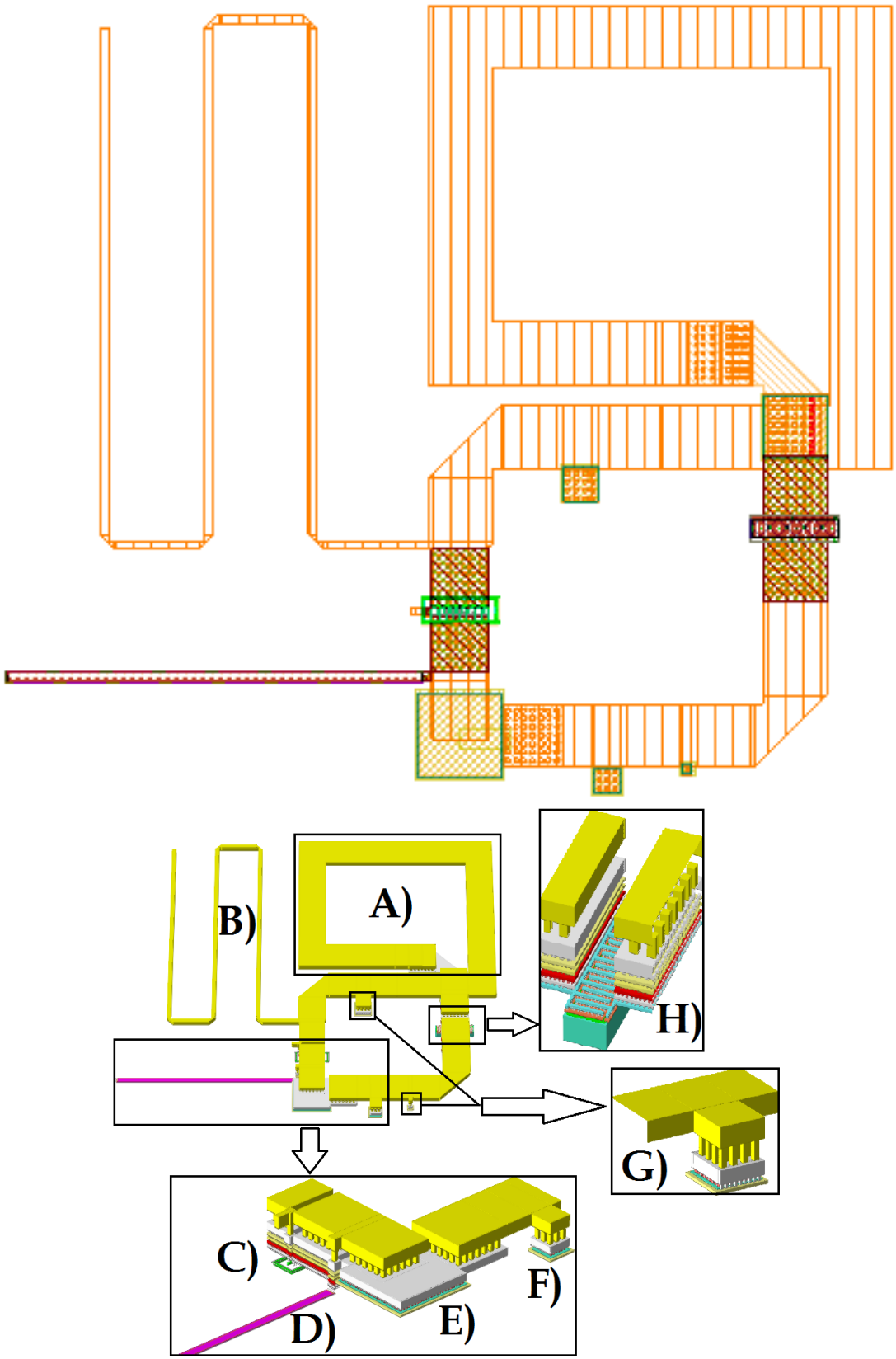


Figure 6.5: Layout, 2D and 3D, of the Common Emitter (Nx = 8) with Coupled Series Resonator.

In the output spectrum of Figure 6.6 the 2.Harmonic is approximately -17 dBm lower than the carrier. Phase noise is quite similar to the parallel resonator. The output waveform is a bit unbalanced and the gain margin in the Linear plot is within reason.

When changing the ideal Rf-block inductor with a microstrip line, it was not possible to produce adequate inductance with several nH. Because of this, a new gain peak was created at 12 GHz. This is quite clear when looking at the Linear plot Figure 6.6 at approximately 12 GHz.

This type of open-loop bode plot response is not recommended [20].

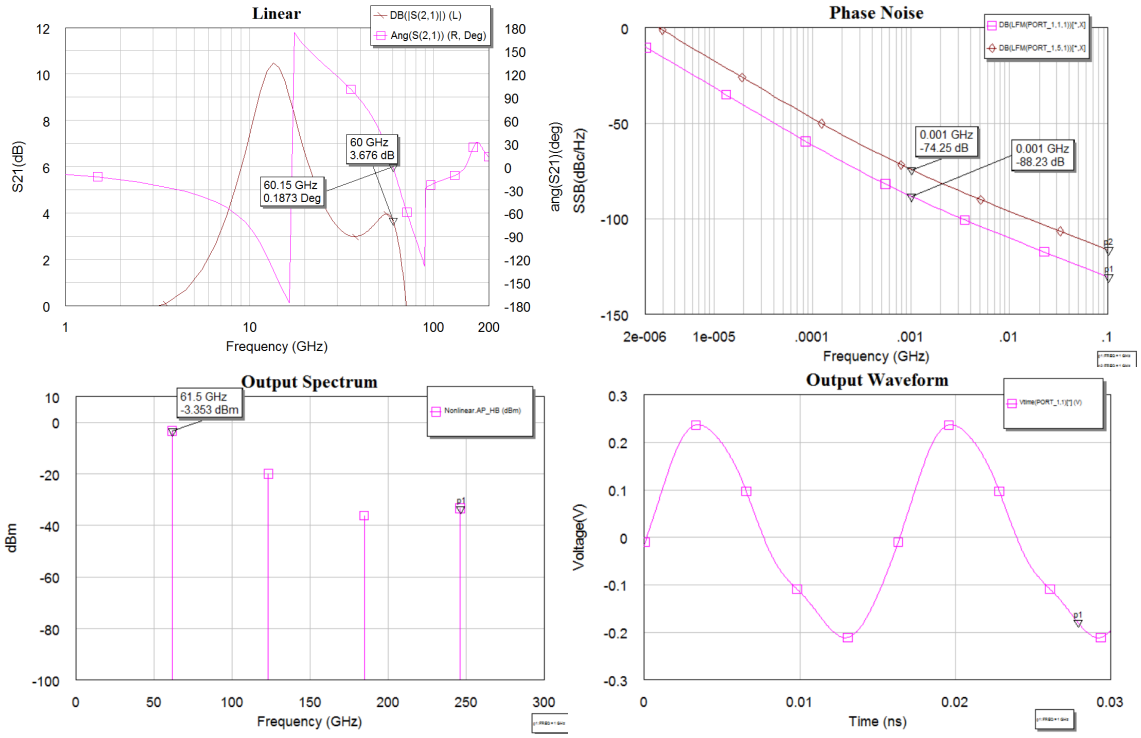


Figure 6.6: Simulation results at 61.5 GHz for the Common Emitter (Nx = 8) with Coupled Series Resonator.

6.2 Optimizing

When optimizing the oscillators lengths and widths of all microstrip lines will be considered for matching and optimal loaded and unloaded Q. The number of emitter fingers will be explored with HB simulations and the varactor MIM capacitor setup will be adjusted to get sufficient tuning.

The series resonator was discarded and will not be optimized. This is because of issues related to a Rf-block inductor shown in the previous section.

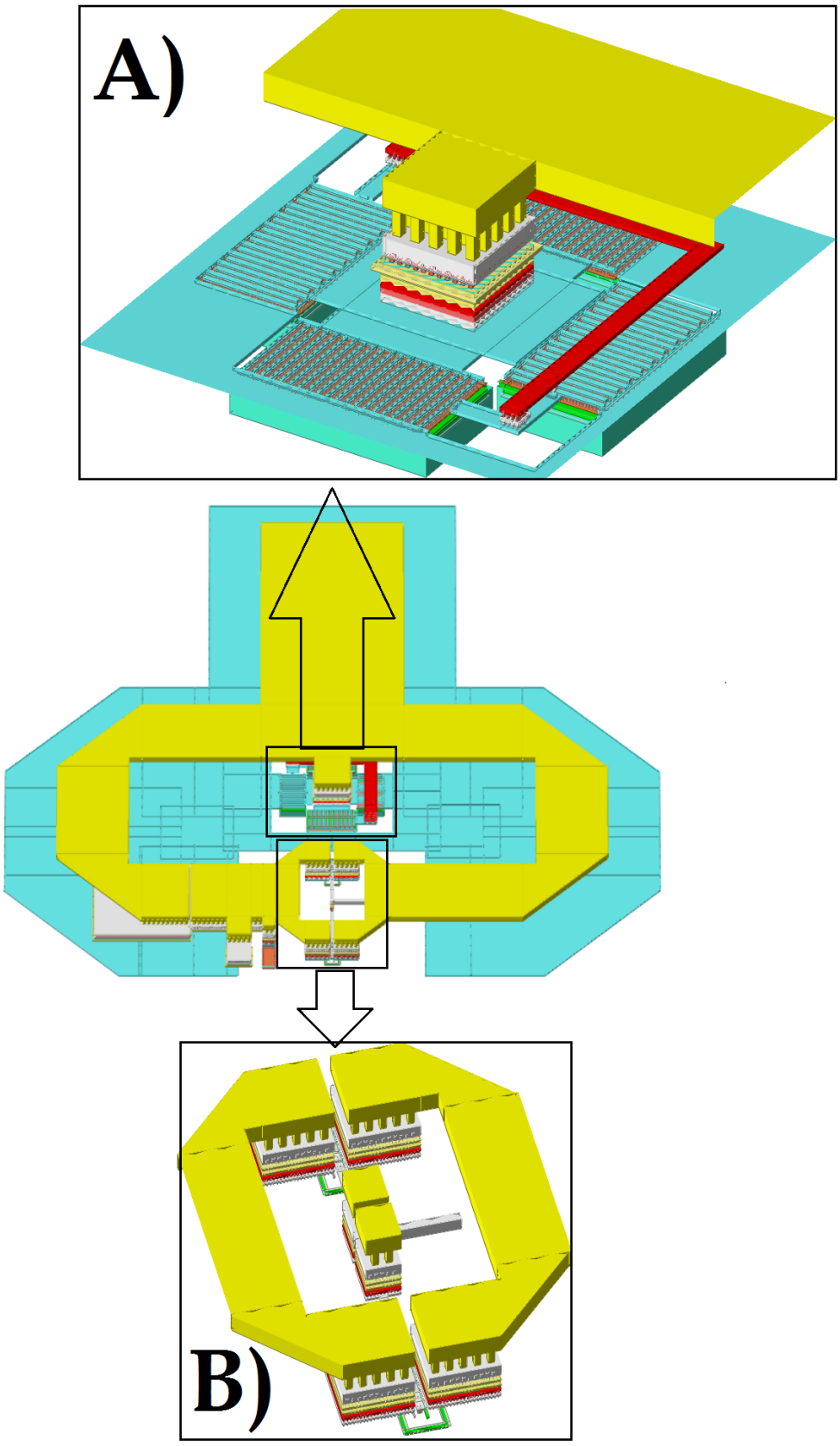


Figure 6.7: Optimized layout,3D, for the Common Emitter (Nx = 12) with Coupled Parallel Resonator.

6.2.1 Optimizing the Common Emitter with Coupled Parallel Resonator

Because the output power was not sufficient the number of emitter fingers was increased to 12 Figure 6.9. The transistors had to be split up in to two columns with 6 fingers in each because the maximum fingers allowed in one column is 8 fingers, B) Figure 6.7. This however gave a more symmetrical layout, Figure 6.7 and 6.8. The microstrip connections widths were increased from 13.6 μm to 30 μm. This gave better matching, less insertion loss and higher unloaded Q. The length from the cross to the base collector determines the inductor coupling. This had to be chosen carefully so that matching, loaded Q and gain margin was within boundaries. Because of the symmetrical design, the length from the cross to the base and collector terminals was equal and approximately 170 μm, including the bends. Both transistor pulls a total of 18.6 mA at $V_{CC} = 1$ V and so the DC power consumption is 18.6 mW. The number of varactors was increased from 3 to 4 for better tuning range. They are placed in parallel around the series MIM capacitor to get a nice symmetrical structure, A) Figure 6.7. The reason for considering symmetry is because if they are effected by their surroundings at least they are effected in the same way. The total area usage is approximately 0.055 mm^2.

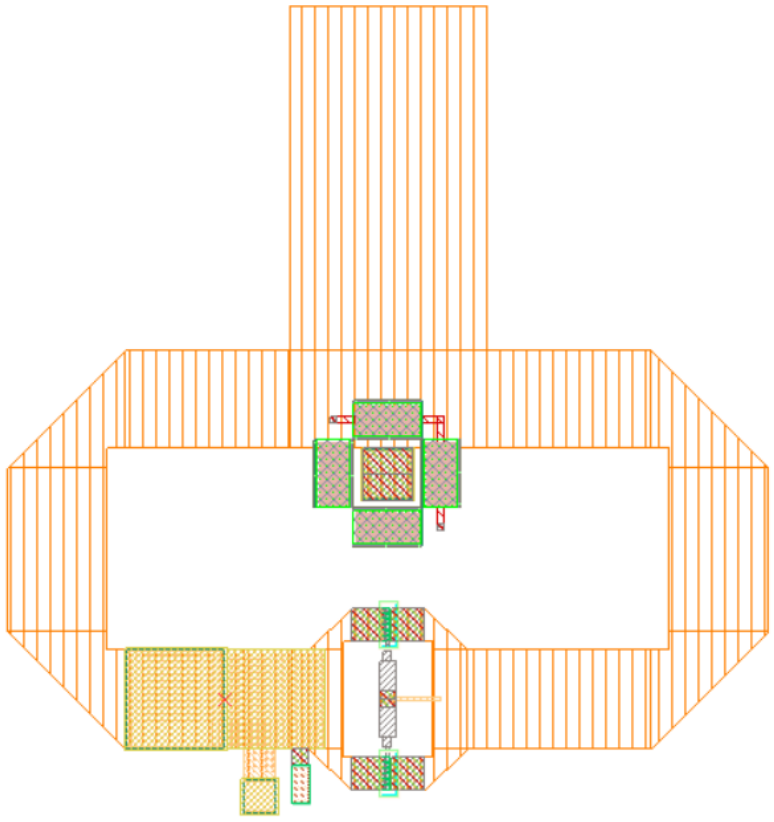


Figure 6.8: Optimized layout, 2D, for the Common Emitter (Nx = 12) with Coupled Parallel Resonator.

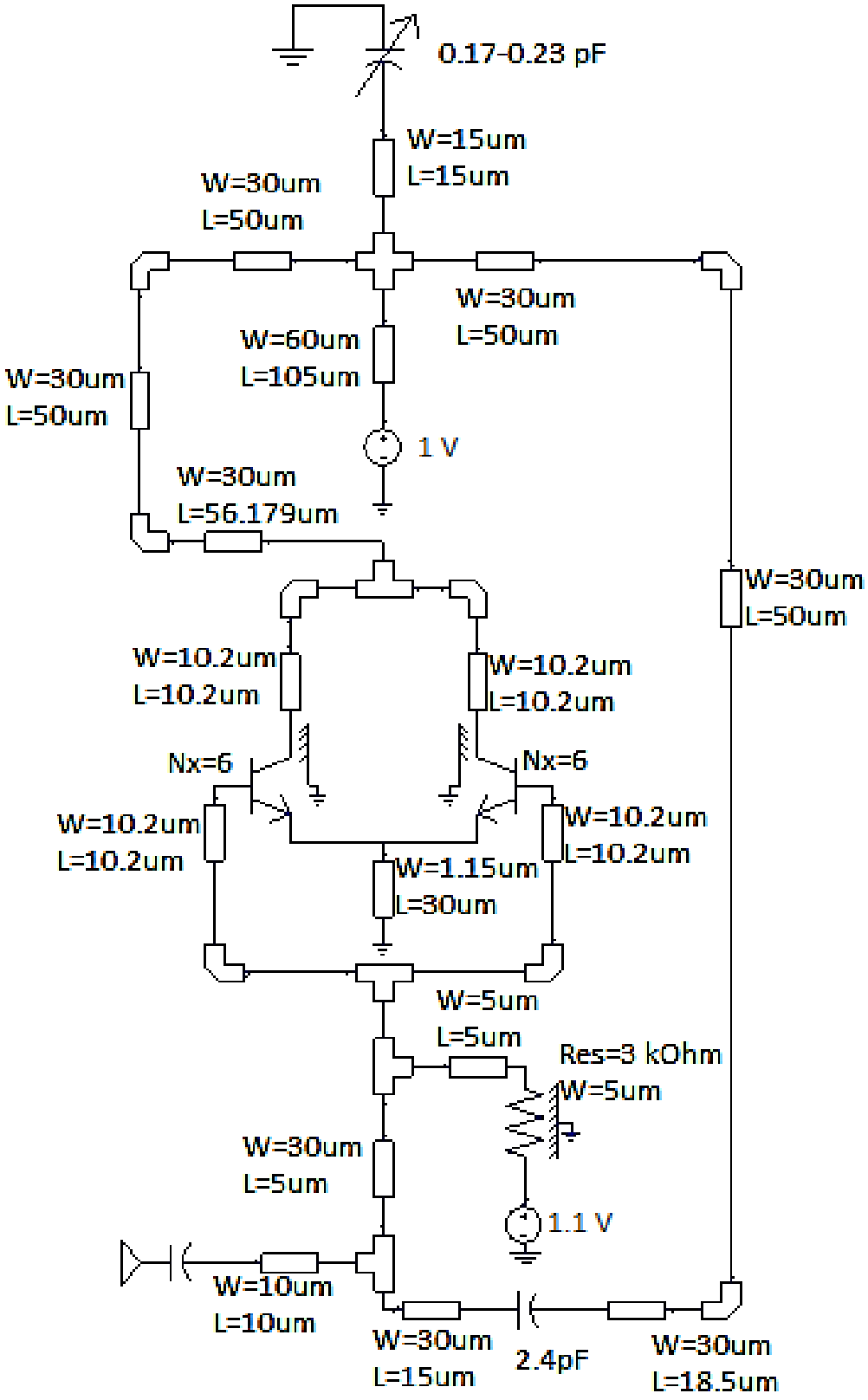


Figure 6.9: Optimized schematic for the Common Emitter (Nx = 12) with Coupled Parallel Resonator.

The results are as expected with a drop in gain margin and better phase noise characteristics, Table 6.2. The phase noise is quite stable over the whole tuning range of 58.8-64.2 GHz which gives us 2.7 GHz/V tuning capabilities. Because the gain margin is lesser, the forward gain from the active device is not as heavily compressed and so the harmonic content is more suppressed. The output power is very much the same and is a trade off with the phase noise. At the top left of Figure 6.10 the Bode-plot shows that the phase only crosses the phase-zero one time which was one of the goals presented in Chapter 2.

A buffer and filter will also be considered if this circuit is realized.

Varactor Volt	SSB @ 1MHz	SSB @ 10MHz	Ps(dBm)	GM(dB)	f_{osc}(GHz)
0	-78.4	-119.9	-5.1	2.1	58.8
0.2	-78.5	-119.8	-5.6	2.1	59.5
0.4	-78.7	-119.8	-6.1	2.1	60.5
0.6	-78.6	-119.6	-6.6	2.1	61.4
0.8	-78.5	-119.3	-7.1	2.0	62.0
1.0	-78.0	-118.8	-7.4	2.0	62.6
1.2	-78.8	-119.6	-7.7	1.9	63.1
1.4	-78.2	-119.0	-8.0	1.9	63.5
1.6	-77.9	-118.7	-8.2	1.9	63.8
1.8	-77.8	-118.6	-8.4	1.8	64.1
2.0	-77.8	-118.5	-8.5	1.8	64.2

Table 6.2: Results from the optimized Common Emitter (Nx = 12) with Coupled Parallel Resonator.

6.3 Summary

By choosing a oscillator setup for optimizing, new and improved results where obtained. The oscillator that was chosen is the Common Emitter (Nx = 12) with Coupled Parallel Resonator. The resonator can be classified as a **Hybrid Microstrip Resonator** because it is realized with the combination of both microstrip elements and library components [20].

Nx = 12 emitter fingers shows the best results in terms of phase noise and harmonic compression. SSB is quite stable at -78 dBc/Hz at 1 MHz Offset for the whole tuning range, 58.8-54.2 GHz. This is 7 dB more noise than the initial goal of -85 dBc/Hz at 1 MHz Offset, but 18 dB lower than the maximum noise requirement for the modulator, -60 dBc/Hz at 1 MHz Offset. The output power is -6.7 dBm which is only 1.7 dBm lower than the initial goal of -5 dBm.

In the next chapter the Hybrid Microstrip Resonator will be verified with EM-simulations and corner analysis.

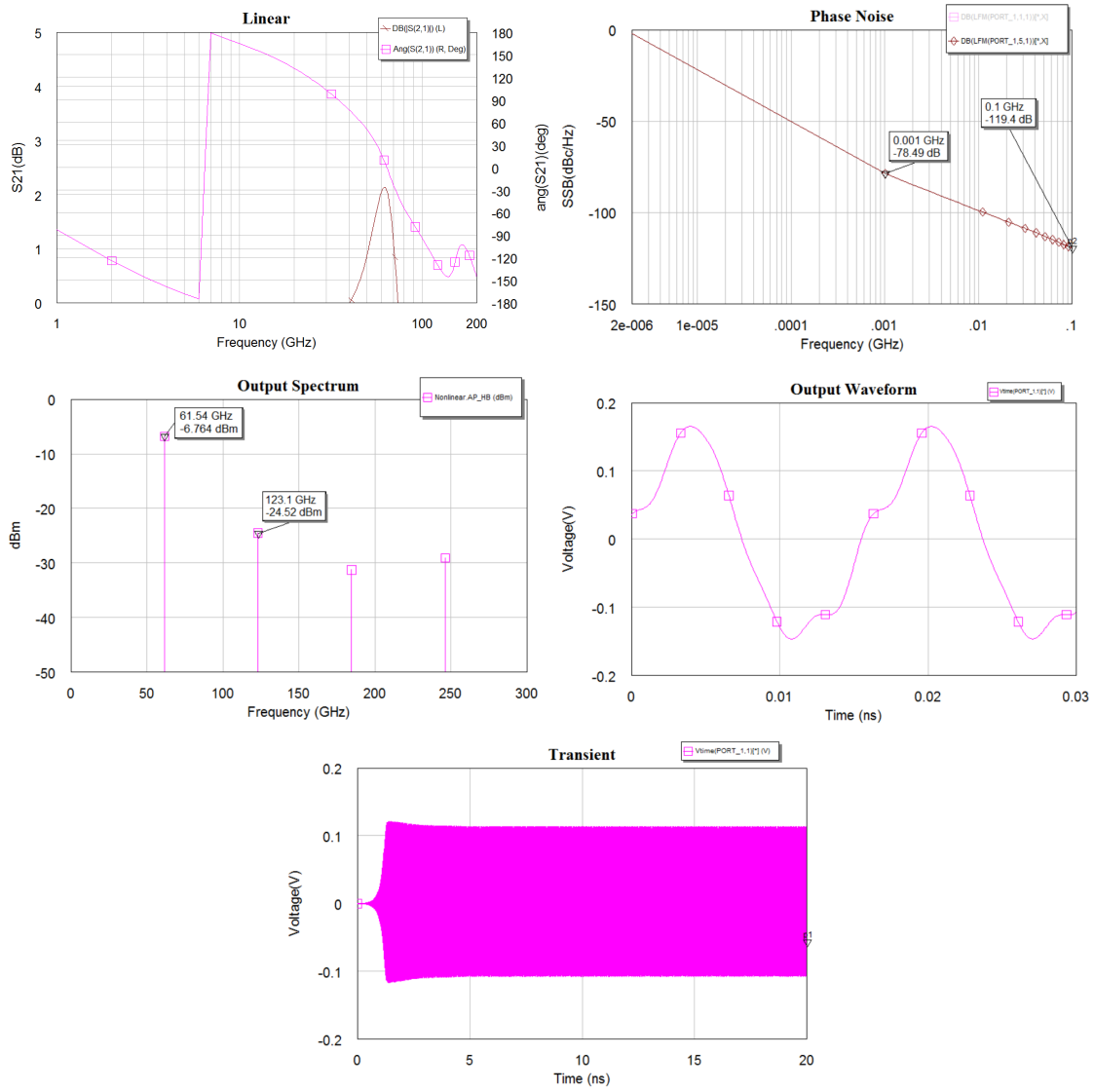


Figure 6.10: Results from HB simulations at 61.5 GHz for the optimized Common Emitter (Nx = 12) with Coupled Parallel Resonator.

Chapter 7

Verification

As of now there are 3 critical parts on the oscillator that has not been sufficiently tested, The 4 varactors in parallel which are connected to a MIM capacitor in series, C) Figure 7.1, the DC-block capacitor in the feedback path, B) Figure 7.1 and the microstrip line in the emitter which acts as an inductor, A) Figure 7.1.

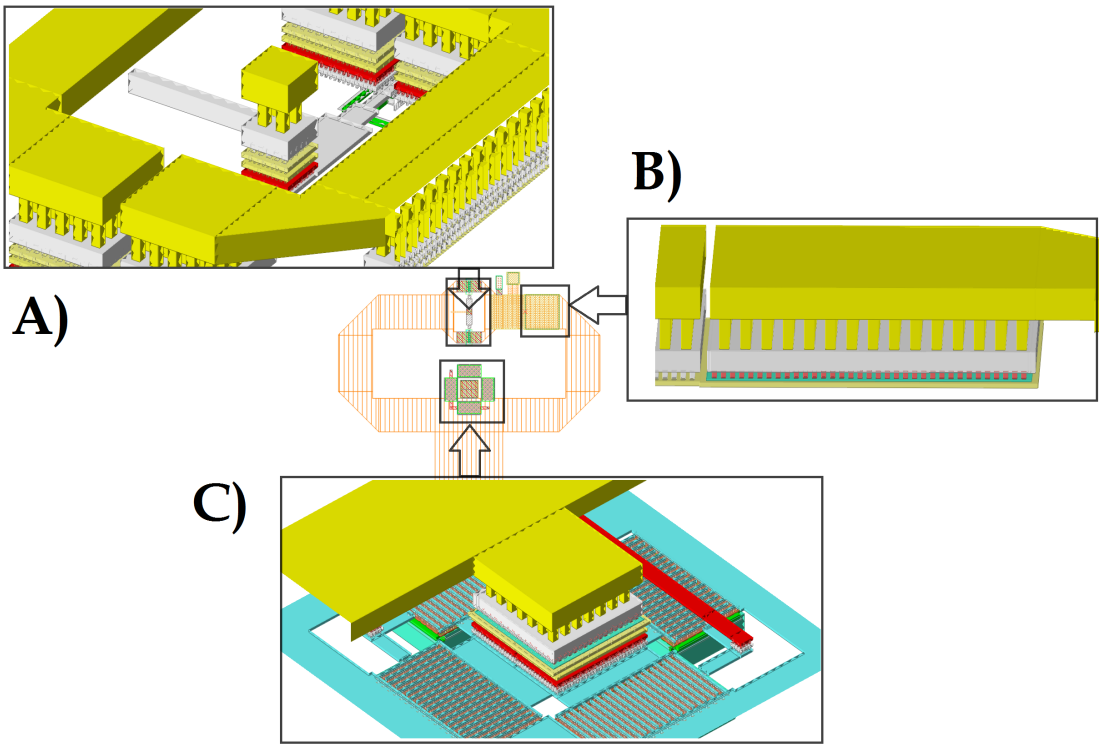


Figure 7.1: Critical components that needs to be verified.

7.1 EM Simulation

For these simulations the electromagnetic solver AXIEM has been used, provided by MWO. AXIEM uses conductor shapes in the x-y plane and defines a mesh on the surface of the conductors as a basis for the solution. It then uses a Method of Moments solver that solves for the currents on conductors. The surface currents modeled by AXIEM include all x, y and z components. But the z component is referred to as thickness and is optional.

When executing EM-simulation we choose which part of the circuit we want to look at and create a mesh. It is important that the mesh has enough resolution or else we can get the wrong results. A rule of thumb is 10% of the smallest length/width, referring to the AWR training guide. The reason for preforming EM-simulations is explained in subsection 3.0.3.

7.1.1 EM simulation of emitter microstrip

In Figure 7.2 the mesh for the emitter microstrip is shown, this is nice mesh and if we look up closely to the right in the figure we can see that there is almost a thin line that follows the edges. Referring to AWR's learning videos this is good thing and they say that by experience this gives good results.

There are 3 ports and so now we simulate the structure using AXIEM and then we use these results as a replacement for the modeled microstrip.

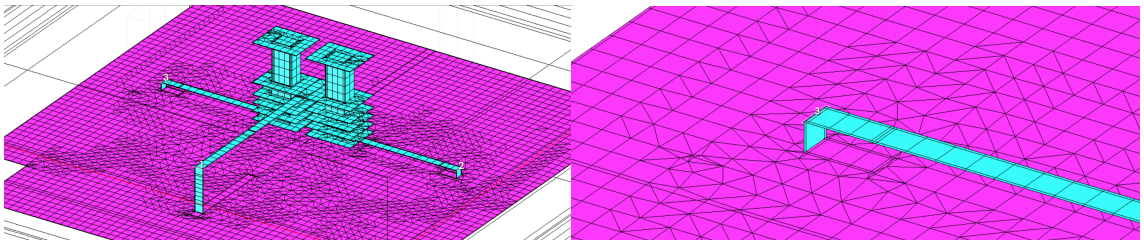


Figure 7.2: Meshing structure of emitter microstrip.

7.1.2 EM simulation of Varactor Connection

The structure in Figure 7.3 is more complex in the sense that it has 5 ports. Four of them has to be connected to metal1 and the fifth to metal5 which is the bottom of the MIM capacitor. The varactors are placed in parallel right beneath the capacitor one on each side creating a symmetric square pattern so that the path from the capacitor to each varactor has the same length.

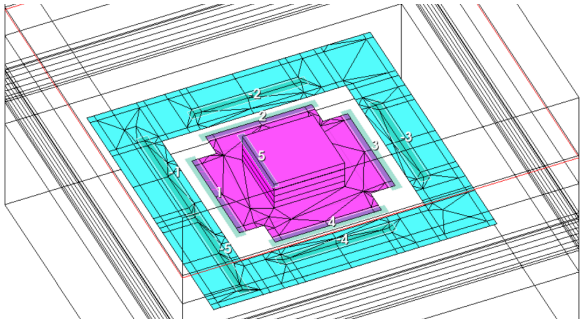


Figure 7.3: EM simulation of varactor connection.

7.1.3 EM simulation of MIM Capacitors

The series MIM capacitor connecting the cross to the varactor is one of the main parts in the resonator. Looking at Figure 7.4 one can see that the capacitance is not frequency independent as the model from the library would imply. It acts as a combination of capacitor and transmission line at high frequencies. At lower frequencies the capacitance matches the model for the $15x15\mu m^2$ MIM capacitor, but when increasing the frequency the capacitance increases to 1.2 pF at 61.5 GHz and then resonates at approximately 70 GHz. The area was reduced to a $10x10\mu m^2$ and the MIM capacitor got a higher resonance frequency, but it will still have the same response. The increase in capacitance with frequency will impact the tuning range in a negatively way. This is because when tuning for higher frequencies the MIM capacitor will counteract with a increase in capacitance, eq2.11.

The DC-block capacitance is reduced from $30x30\mu m^2$ to $30x10\mu m^2$ because it has to low resonance and becomes inductive at frequencies above 40 GHz. The coupling capacitor Cc remains unchanged.

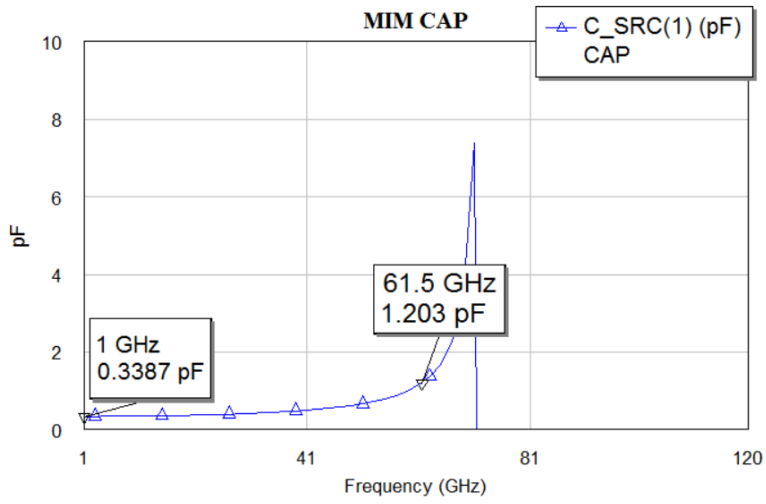


Figure 7.4: Resonance of MIM capacitance

7.1.4 Compering Results before and after EM-simulation

In Table 7.1 a list of component values before and after the EM-simulation is listed, this list corresponds to Figure 7.5. TM6 is the transmission line used to connect the cross to the series capacitor and had to be reduced to fit. TM10 and TM11 also had to be changed in length to fit the design, but had no special impact on the performance. TM15 is also referred to as the emitter microstrip and had to be built like a T-junction, Figure 7.2. The series Cap and C-dc had to be reduced because of increase in capacitance with frequency.

Component	Before	After
Nx	12	12
TM1/TM2/TM16/TM17	L=10.2μm , W=10.2μm	The same as before
TM3	L=56.2μm , W=30μm	The same as before
TM4/TM5/TM8/TM9	L=50μm , W=30μm	The same as before
TM6	L=15μm , W=15μm	L=10μm , W=10μm
TM7	L=105μm , W=60μm	The same as before
TM10	L=18.5μm , W=30μm	L=30μm , W=30μm
TM11	L=15μm , W=30μm	L=5μm , W=30μm
TM12	L=10μm , W=10μm	The same as before
TM13	L=5μm , W=30μm	The same as before
TM14	L=5μm , W=5μm	The same as before
TM15	L=30μm , W=1.15μm	L=16μm , W=1.15-5μm
Cc	WxL=10x10μm^2	The same as before
Varactor	4x(L=0.8μm , W=9.74μm , col=10)	The same as before
Series Cap	WxL=15x15μm^2	WxL=10x10μm^2
C-dc	WxL=30x30μm^2	WxL=30x10μm^2
Rbias	3 kOhm	The same as before

Table 7.1: Component values before and after EM-simulation.

The tuning range has been reduced from 5.4 GHz to 2.8 GHz leaving us with 1.4 GHz/V, Table 7.2. The main reason for this is the MIM capacitors increase in capacitance with frequency which counteracts the varactors when tuning for higher resonance frequency, Figure 7.4. The phase noise characteristic has not changed substantially when compering Table 6.2 and 7.2. The output power Ps has decreased with approximately 4-5 dBm and the gain margin is almost the same. The transient analysis shows that the oscillator is balanced Figure 7.6. When EM-structures where used for the C-dc we got multiple phase-zero crossings, Linear plot Figure 7.6, but there are more crossing with a negative phase-slope so the Barkhausen's criterion are fulfilled, Chapter 2.

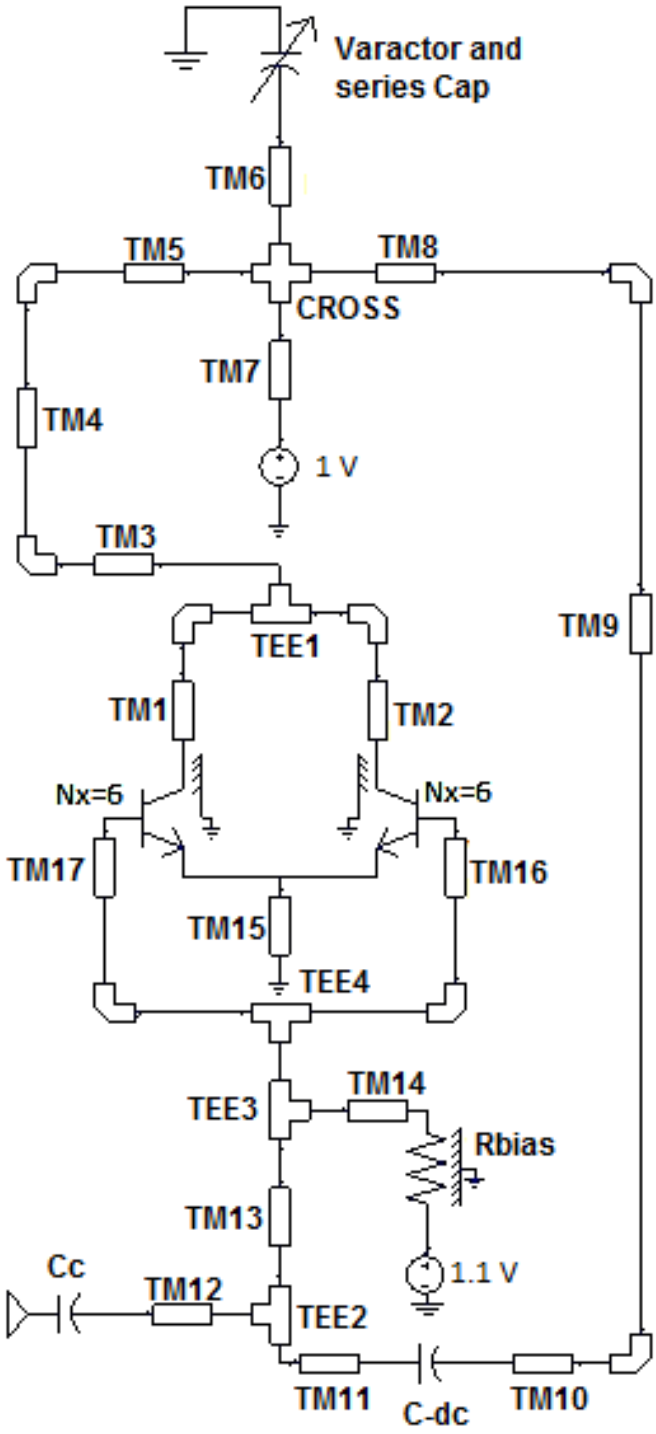


Figure 7.5: Schematic for the Hybrid Microstrip Resonator before and after EM simulation. Component values are found in Table 7.1.

Varactor Volt	SSB @ 1MHz	SSB @ 100MHz	Ps(dBm)	GM(dB)	f_{osc}(GHz)
0	-79.3	-119.2	-8.8	2.2	59.9
0.2	-79.3	-119.2	-9.0	2.2	60.1
0.4	-79.3	-119.2	-9.2	2.2	60.4
0.6	-79.1	-119.1	-9.5	2.1	60.7
0.8	-79.1	-119.1	-9.7	2.0	60.9
1.0	-79.0	-119.0	-9.9	2.0	61.2
1.2	-79.0	-119.1	-10.1	2.0	61.5
1.4	-78.8	-118.8	-10.3	1.9	61.8
1.6	-78.7	-118.8	-10.6	1.9	62.1
1.8	-78.7	-118.8	-10.8	1.8	62.4
2.0	-78.5	-118.6	-10.9	1.8	62.6

Table 7.2: Results after EM-simulation

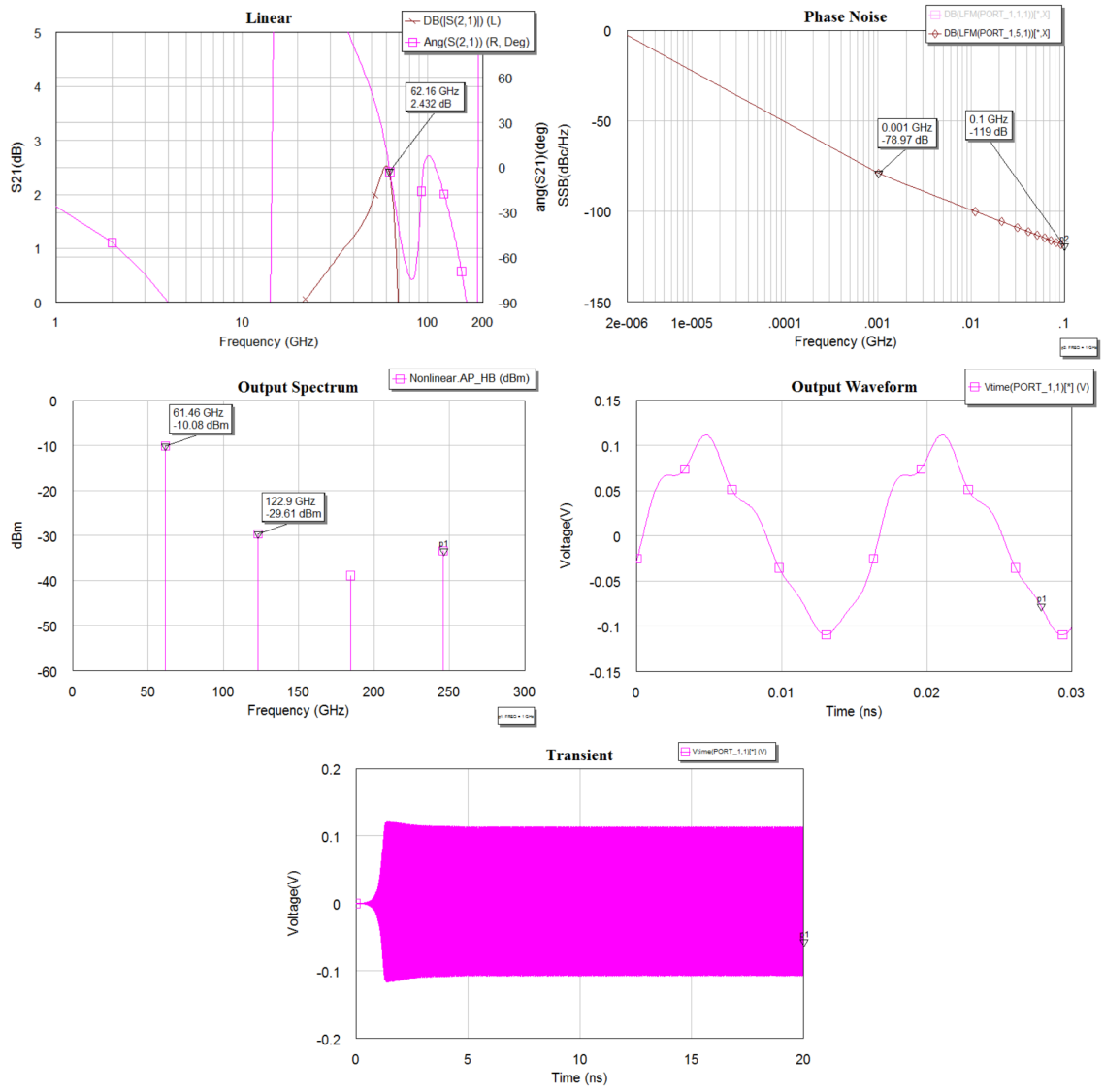


Figure 7.6: Results after EM-simulation.

7.2 Corner Analysis

To predict the variations on a wafer corner analysis must be done. In this analysis WCS (worst case), TYP (typical) and BCS (best case) are simulated versus temperature and supply voltage variations.

In Figure 7.8 the results are presented in terms of SSB, Output Power and frequency shifts. The nominal supply voltage value is 1.1 V for both V_{BB} and V_{CC}. To adjust the temperature a secondary parameter called the "_TEMP" has to be inserted. This parameter controls temperature in all of IHP_SG13 library components which are temperature dependent, when disabled the temperature is nominally 27°C or 300 K. In Figure 7.7 the parameters that are varied is illustrated.

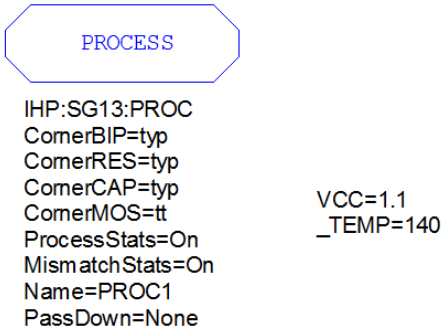


Figure 7.7: Parameters used that are used for corner analysis.

Phase Noise and Output Power are one of the main parameters in which determines the quality and efficiency of the oscillator and are therefor used to represent the different corners. The phase noise varies approximately from -63 to -80 dB/Hz at 1MHz offset, Figure 7.8. Both the WCS, TYP and BCS scenarios has supply voltage values which has -75 dB/Hz or lower below 100°C and so the results can be controlled at some degree with using supply voltage.

The nominal resonating frequency was chosen to be 61.5 GHz, with process variations this changes from 61.2-63.0 GHz, (bottom) Figure 7.8. The second harmonic component is approximately -20 dBc at all corners. The output power varies a from -8 dBm to -17 dBm in the temperature range $0 - 140°C$ respectively. From 100°C and down towards 0°C the output power is -14 dBm or higher. The two figures shows a clear trade-off relationship between output power and phase noise. For WCS the gain margin is higher then the gain margin for TYP and BCS resulting in higher output power, but also higher harmonic content which increases the phase noise.

All in all the output power is to low and needs to be amplified. A active filter has been designed in the next section without any special effort, just to show that it is possible to recover a nice sinusoidal signal from the oscillator with adequate output power. But first we will take a look at Pushing Induced Noise.

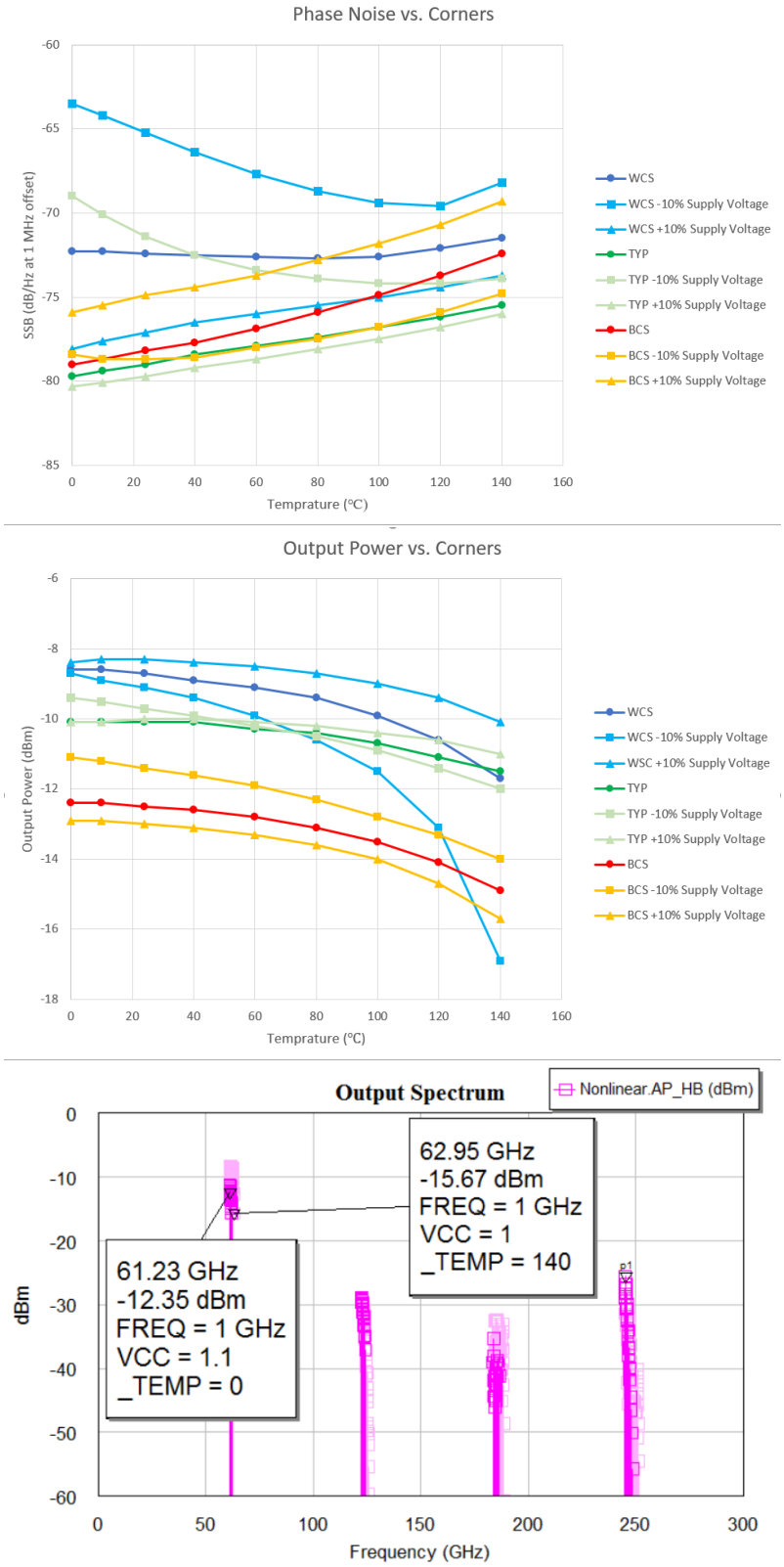


Figure 7.8: Results from corner analysis i therms of SSB (top), Output Power (middel) and output spectrum (bottom).

7.2.1 Pushing Induced Noise

A change in the supply voltage changes the bias and transfer characteristic of an amplifier. A change in transmission phase results in oscillator frequency shift and is therefore transferred in to phase noise. The same goes for the varactor that is tuned by a external voltage source. To simulate this, three white noise voltage sources are placed in series with voltage source VBB, VCC and Vtune, each source was set to 1 $nV/\sqrt{Hz}$. A 50 ohm source has 0.8949 $nV/\sqrt{Hz}$. Because the loaded Q was rather poor, typical 4-5, the bandwidth was approximately 30 GHz. To calculate the rms value added to the sources $\sqrt{\triangle f}$ is multiplied with 1 nV. This results in 0.17 mVrms of white noise and the phase noise is plotted in Figure 7.9.

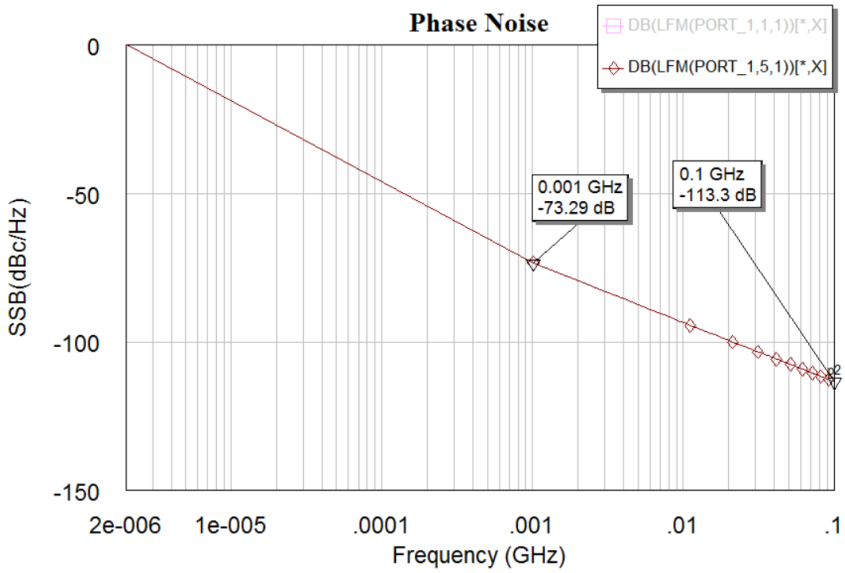


Figure 7.9: Simulating Pushing Induced Noise and the effect it has on phase noise.

7.3 Active Filter

An example of a active filter has been made to amplify and filter the output signal, Figure 7.11.

In Figure 7.10 the results from applying the active low-pass filter is shown. The second harmonic component is -44 dBm below the carrier which is at -6.2 dBm and we now see a clean and nice sinusoidal output waveform. DC-power consumption is 8.6 mW and the SSB is -79.2 dBc/Hz at 1 MHz Offset. The noise floor is raised to -90.5 dBc.

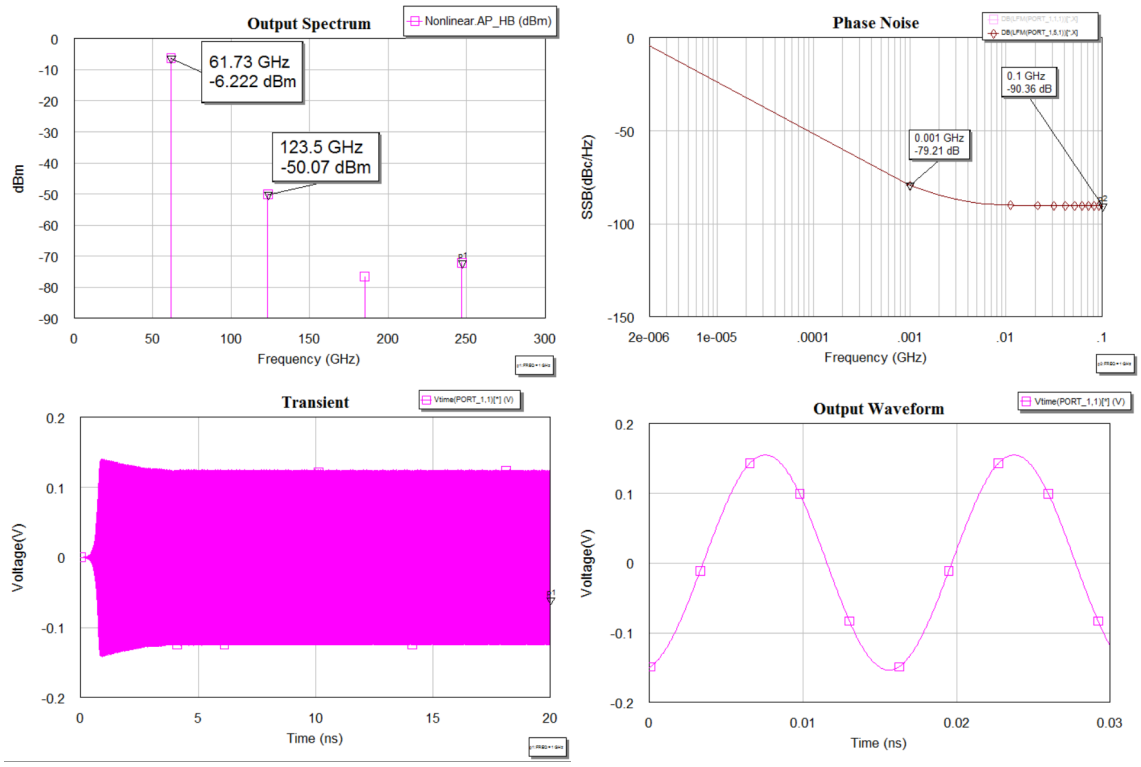


Figure 7.10: Results after applying active filter to the Hybrid Microstrip Resonator.

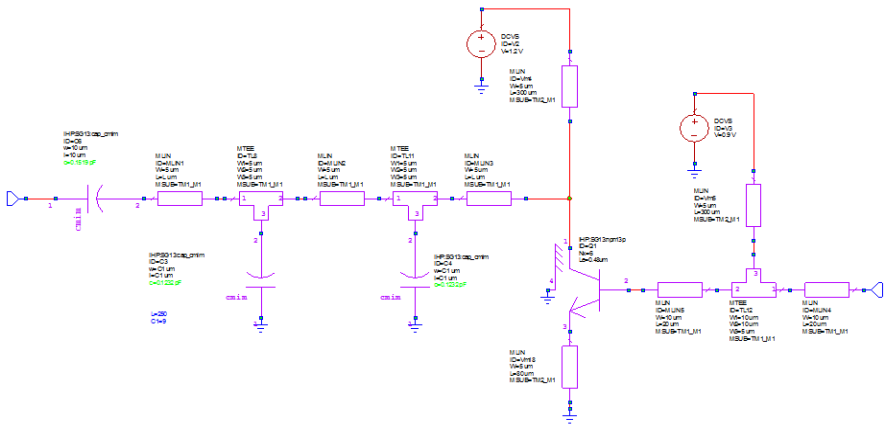


Figure 7.11: Schematic for the active filter.

Chapter 8

Discussion and Conclusion

A 61.5 GHz Hybrid Microstrip Resonator VCO has been designed and verified using simulation tools provided by AWR and design methodology from the book [20]. To our knowledge this oscillator has never been design at frequencies these high..

Compared to other oscillators, section 4.1, the Hybrid Microstrip Resonator VCO has a low power consumption, **19.5 mW**, and a low total area usage, **0.055** $\boldsymbol{mm^2}$. The SSB is approximately stable at **-79 dBc/Hz at 1 MHz Offset** over the whole tuning range of **59.9-62.2 GHz**. The output power is **-10 dBm** and it has a 2.Harmonic suppression of **-20 dBc**. This is well within boundaries of what is required by the OOK Modulator, Chapter 4 except for the output power. A solution to this is applying a active filter, section 7.3, which can easily produce a nice sinusoidal output with **-5 dBm** and **-44 dBc** 2.Harmonic suppression.

The corner analysis in Chapter 7 shows that the phase noise can be controlled to a certain degree using the supply voltage. This makes it possible to keep the phase noise below -75 dBc/Hz at 1 MHz Offset, at all corners for temperatures below 100°C . In (bottom) Figure 7.8 we see that the fundamental resonating frequency drift from 61.2-63 GHz in different process corners. Given the tuning range from 59.9-62.2 GHz using the varactor there should be no problem compensating for this drift.

8.1 Improvements

When designing the oscillator for the first time, varactor and EM-structures were not considered. Because the results from the EM-structures had a big an impact on the performance of the oscillator a second iteration had to be done, starting with the open-loop cascade analysis. The second iteration included EM-structures of the components in the resonator, except for the MIM capacitor. This gave a more accurate prediction of how the resonator behaved in closed-loop. The IHP SG13s library included a model for the MIM capacitor, for this reason we did not include EM-structures for this particular component

at this point.

Later we discovered that the model for the MIM-capacitor did not change with frequency, which was not expected. We had good reasons to believe that the MIM capacitor should act as a transmission line as well as a capacitor, because of the simple fact the signal needs to propagate though the plates of the capacitor. The model did not even change in behavior when keeping the capacitance constant and increasing the electrical length of the capacitor. Because of this EM-structures were made and simulated.

This was somewhat troublesome in beginning when the capacitance did not concur with the model. It turned out that the thickness in the material properties ThinAluminum2_5 was set to 450 nm when it should have been 490 nm. This made a significant impact on the capacitance and changing it made the results similar to the model at lower frequencies, Figure 7.4. However, the response from the MIM capacitor showed that the capacitance increased with frequency to a certain point where it became inductive. This is exactly as predicted, the MIM capacitor acted as a transmission line as well as a capacitor. This counteracted the tuning capabilities of the varactor and made the tuning less efficient since the effective capacitance of the MIM capacitor increased, which will lower the frequency.

If this had been spotted earlier, efforts could have been made so that this type of response would have been considered when doing a resonator analysis in Chapter 5. We have good reasons to believe that this could have increased the tuning range as well as the output power.

8.1.1 Other design methods

When looking at earlier designs, referring to Table 4.1, the most common way to design MMW oscillators on integrated circuits is by using a push-push oscillator. The push-push oscillator can be realized by using of negative resistance or negative conductance. To quote [6], "The inherent physical symmetry of the balanced oscillator circuits makes them very attractive in applications where two balanced out-of-phase outputs are required. Due to the excellent amplitude and phase balance as well as better noise performance compared with a single-ended configuration, they are widely used in balanced mixers, phase lock loops or synthesizers where out-of-phase signals from local oscillators are needed." But because the high f_t of npn13p, as explained in sec.2.6, this approach was disregarded. A possible way to solve this problem could be to design a 120 GHz oscillator and than use a frequency divider.

8.2 Future Work

We have good reasons to believe that improving the resonator by analyzing it more thoroughly with EM-structure will decrease phase noise, increase tuning range and output power. If higher output power for some reason is not obtainable the active filter needs to

be validated and optimized. Another possibility is designing a 120 GHz negative resistance push-push VCO, or explore the differential amplifier as a sustaining stage by using the the 2-port method. Antennas needs to be designed with high gain and low area usage. This will insure a compact design which is capable relative high transmission line. A set of integrated horn antennas has been made earlier with 14.6 dBi [15].

Abbreviations

ASK Amplitude Shift Keying

BCS Best Case Scenario

BER Biterror Rate

CB Common Base

CC Common Collector

CE Common Emitter

CMOS Complementary Metal Oxide Semiconductor

CMRR Common Mode Rejection Ratio

DRC Design Rule Check

EM Electromagnetic

ESTI European Telecommunications Standards Institute

FOM Figure Of Merit

HBT Heterojunction Bipolar Transistors

HB Harmonic Balance

HD High Definition

IC Intergrated Circuit

IEEE Institute of Electrical and Electronics Engineers

IHP Innovations for High Performance Technology

LNA Low Noise Amplifier

LOS Line Of Sight

LO Local Oscillator

M1 Metal 1

MIMO Multiple-Input Multiple-Output

MIM Metal-Insulator-Metal

MMW Millimetre Wave

MWO Microwave Office

OOK On-Off Keying

OQPSK Offset Quadrature Phase-Shift Keying

PA Power Amplifier

PLL Phase Locked Loop

RF Radio Frequency

SiGe Silicon Germanium

SSB Single Sideband Phase Noise

TM2 Top Metal 2

TPD Total Power Dissipation

TYP Typical

UiB University in Bergen

VBB Base Voltage Supply

VCC Collector Voltage Supply

VCO Voltage Controlled Oscillator

WCS Worst Case Scenario

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Appendix A

Analysis results for amplifiers that are not used.

A.1 Common Base (CB)

With 9 emitters the $NF = 3.5$dB, $G = 3.8$ and $\phi = -38°$. The Colpitt and Hartley resonator is commonly used with the CB because they provide matching between the high output and low input. Another possibility is the Coupled Series resonator using coils as coupling or Coupled Parallel resonator using capacitors as coupling given that they provide maximum negative phase slope at positive angle compensating for the negative angle of the CB stage.

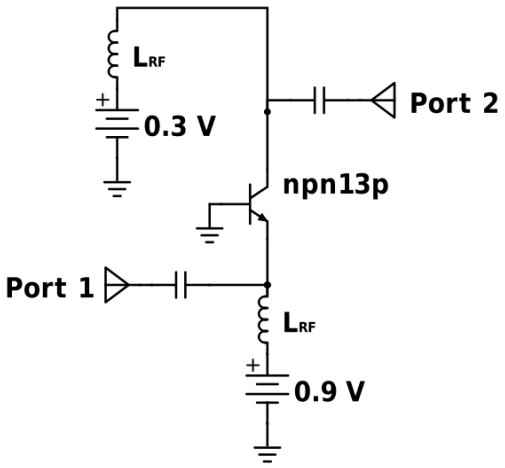

Figure A.1: Common Base Amplifier.

A.2 Common Collector (CC)

With 8 emitters the $NF = 2.3$dB, $G = 3.7$ and $\phi = -28°$. The Colpitt and Hartley resonator is commonly used with the CC for the same reasons as for the CB.

Emitters Nx	$\phi(degrees)$	R_{in}	R_{out}	$NF(dB)$	$G(dB)$	$f_t(GHz)$	$I_C(mA)$
1	-26	75	770	8	-1.8	-	1.2
2	-26	38	422	5.9	1.2	122	2.4
3	-28	26	298	4.9	2.4	173	3.6
4	-29	20	232	4.4	3.1	195	4.8
5	-31	16	191	4	3.5	205	6
6	-33	14	163	3.8	3.7	207	7.2
7	-34	12	142	3.7	3.8	206	8.4
8	-36	11	127	3.6	3.9	202	9.6
9	-38	10	111	3.5	3.8	181	10.8
10	-40	9	100	3.5	3.8	168	12
11	-42	8	92	3.5	3.7	158	13.2
12	-44	7.5	85	3.5	3.6	149	14.4
13	-45	7	79	3.5	3.5	141	15.6

Table A.1: Analysis of the Common Base stage with different number of emitters.

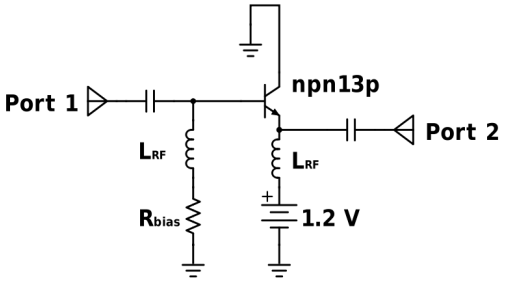

Figure A.2: Common Collector Amplifier.

A.3 Cascode

With 7 emitters the $NF = 3.9$dB and $G = 13.5$ and $\phi = 69°$. Coupled Series resonator using capacitors as coupling or Coupled Parallel resonator using coils as coupling is a choice for this sustaining stage given that they provide maximum negative phase slope at negative angle compensating for the positive angle of the Cascode stage. The Cascode can also use a shunt feedback from the collector output to the base input decreasing excessive gain, stabilizing but also increasing noise.

Emitters Nx	R_{in}	R_{out}	$\phi(degrees)$	$NF(dB)$	$G(dB)$	$f_t(GHz)$	$I_C(mA)$
1	440	77	-19	6	-1.9	-	1.2
2	277	42	20	3.7	1	101	2.4
3	215	31	-21	3	2.2	139	3.6
4	180	25	-22	2.7	2.8	154	4.8
5	157	22	-24	2.5	3.2	160	6
6	140	20	-25	2.4	3.4	160	7.2
7	127	18	-26	2.4	3.6	158	8.4
8	116	17	-28	2.3	3.7	155	9.6
9	108	16	-29	2.3	3.7	152	10.8
10	100	15.5	-30	2.3	3.7	148	12
11	94	15	-32	2.3	3.6	144	13.2
12	88	14.5	-33	2.3	3.6	139	14.4
13	33	14	-34	2.4	3.6	135	15.6

Table A.2: Analysis of the Common Collector stage with different number of emitters.

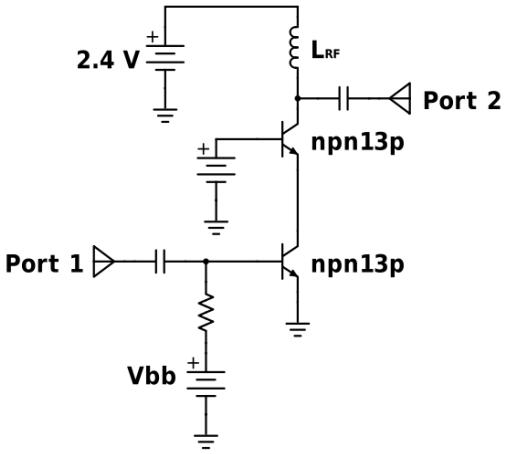

Figure A.3: Cascode.

Emitters Nx	R_{in}	R_{out}	$\phi(degrees)$	$NF(dB)$	$G(dB)$	$f_t(GHz)$	$I_C(mA)$
1	250	1058	116	8	2.1	106	1.2
2	124	542	105	5.9	7.2	193	2.4
3	82	366	96	5	9.8	226	3.6
4	62	276	88	4.5	11.4	240	4.8
5	49	222	81	4.2	12.4	245	6
6	40	186	75	4	13	247	7.2
7	34	160	69	3.9	13.5	247	8.4

Table A.3: Analysis of the Cascode stage with different number of emitters

Appendix B

Unloaded Q simulations for components that are used in resonators.

B.1 Unloaded Q for the microstrip inductance.

Width	Length	Inductance pH	Unloaded Q-EM	Capacitance(pF)tune from 57-66 GHz
60	50	8	22.8	0.98-0.73
60	60	9	22.7	0.87-0.65
60	70	11	23	0.71-0.53
60	80	13	23.2	0.60-0.45
60	90	14	23.3	0.56-0.42
60	100	16	23.1	0.49-0.36
60	110	18	23	0.43-0.32
60	120	20	23	0.39-0.29
60	130	21	22.9	0.37-0.28
60	140	23	22.0	0.34-0.25
60	150	25	22.0	0.31-0.23
60	160	27	21.9	0.29-0.21
60	170	29	21.7	0.27-0.20
60	180	31	21.5	0.25-0.19
60	190	33	21.3	0.24-0.18

Table B.1: Unloaded Q for the microstrip inductance.

B.2 Unloaded Q for TL Cap

Cap Value pF	Unloaded Q
0.1	474
0.2	237
0.3	157
0.4	118
0.5	95
0.6	78
0.7	67
0.8	59
0.9	52
1	47

Table B.2: Unloaded Q for TL Cap.

B.3 Unloaded Q for MIM

Cap Value pF	Unloaded Q
0.1	474
0.2	237
0.3	157
0.4	118
0.5	95
0.6	78
0.7	67
0.8	59
0.9	52
1	47

Table B.3: Unloaded Q for MIM.

B.4 Unloaded Q for Varctor

Colums	Width	Length	Cap Value pF	Unloaded Q
1	3.74	0.3	0.0043	12
2	3.74	0.3	0.0086	5.5
3	3.74	0.3	0.0120	3.6
4	3.74	0.3	0.0145	3.2
5	3.74	0.3	0.0165	3.4
6	3.74	0.3	0.0185	3.8
7	3.74	0.3	0.0207	4.3
8	3.74	0.3	0.0230	4.9
9	3.74	0.3	0.0255	5.4
10	3.74	0.3	0.0280	5.9
1	3.74	0.8	0.010	4.5
2	3.74	0.8	0.017	2.7
3	3.74	0.8	0.022	2.6
4	3.74	0.8	0.026	3.1
5	3.74	0.8	0.030	3.7
6	3.74	0.8	0.035	4.3
7	3.74	0.8	0.040	4.9
8	3.74	0.8	0.046	5.5
9	3.74	0.8	0.051	6.2
10	3.74	0.8	0.057	7
1	9.74	0.3	0.0086	5.3
2	9.74	0.3	0.016	3.3
3	9.74	0.3	0.022	2.9
4	9.74	0.3	0.027	3
5	9.74	0.3	0.032	3.2
6	9.74	0.3	0.037	3.4
7	9.74	0.3	0.042	3.6
8	9.74	0.3	0.047	3.8
9	9.74	0.3	0.052	4
10	9.74	0.3	0.057	4.1
1	9.74	0.8	0.018	2.6
2	9.74	0.8	0.030	2.4
3	9.74	0.8	0.040	2.8
4	9.74	0.8	0.051	3.1
5	9.74	0.8	0.062	3.4
6	9.74	0.8	0.073	3.7
7	9.74	0.8	0.084	4
8	9.74	0.8	0.095	4.4
9	9.74	0.8	0.107	4.9
10	9.74	0.8	0.118	5.6

Table B.4: Varctor unloaded Q.

Appendix C

Results from corners analysis in tables.

temp/corner	wcs SSB -10% supp.volt.	wcs SSB Nom supp.volt.	wcs SSB +10% supp.volt.
0	-63.5	-72.3	-78.1
10	-64.2	-72.3	-77.6
24	-65.2	-72.4	-77.1
40	-66.4	-72.5	-76.5
60	-67.7	-72.6	-76.0
80	-68.7	-72.7	-75.5
100	-69.4	-72.6	-75.0
120	-69.6	-72.1	-74.4
140	-68.2	-71.5	-73.7
temp/corner	wcs Ps -10% supp.volt.	wcs Ps Nom supp.volt.	wcs Ps +10% supp.volt.
0	-8.7	-8.6	-8.4
10	-8.9	-8.6	-8.3
24	-9.1	-8.7	-8.3
40	-9.4	-8.9	-8.4
60	-9.9	-9.1	-8.5
80	-10.6	-9.4	-8.7
100	-11.5	-9.9	-9.0
120	-13.1	-10.6	-9.4
140	-16.9	-11.7	-10.1

Table C.1: Worst case scenario.

temp/corner	Typ SSB -10% supp.volt.	Typ SSB Nom supp.volt.	Typ SSB +10% supp.volt.
0	-69.0	-79.7	-80.3
10	-70.1	-79.4	-80.1
24	-71.4	-79.0	-79.7
40	-72.5	-78.4	-79.2
60	-73.4	-77.9	-78.7
80	-73.9	-77.4	-78.1
100	-74.2	-76.8	-77.5
120	-74.2	-76.2	-76.8
140	-73.9	-75.5	-76.0
temp/corner	Typ Ps -10% supp.volt.	Typ Ps Nom supp.volt.	Typ Ps +10% supp.volt.
0	-9.4	-10.1	-10.1
10	-9.5	-10.1	-10.1
24	-9.7	-10.1	-10.0
40	-9.9	-10.1	-10.0
60	-10.2	-10.3	-10.1
80	-10.5	-10.4	-10.2
100	-10.9	-10.7	-10.4
120	-11.4	-11.1	-10.6
140	-12.0	-11.5	-11.0

Table C.2: Typically.

temp/corner	BCS SSB -10% supp.volt.	BCS SSB Nom supp.volt.	BCS SSB +10% supp.volt.
0	-78.4	-79.0	-75.9
10	-78.7	-78.7	-75.5
24	-78.7	-78.2	-74.9
40	-78.6	-77.7	-74.4
60	-78.0	-76.9	-73.7
80	-77.5	-75.9	-72.8
100	-76.8	-74.9	-71.8
120	-75.9	-73.7	-70.7
140	-74.8	-72.4	-69.3
temp/corner	BCS Ps -10% supp.volt.	BCS Ps Nom supp.volt.	BCS Ps +10% supp.volt.
0	-11.1	-12.4	-12.9
10	-11.2	-12.4	-12.9
24	-11.4	-12.5	-13.0
40	-11.6	-12.6	-13.1
60	-11.9	-12.8	-13.3
80	-12.3	-13.1	-13.6
100	-12.8	-13.5	-14.0
120	-13.3	-14.1	-14.7
140	-14.0	-14.9	-15.7

Table C.3: Best case scenario.

Appendix D

This section will not delve in transmission line theory because it is a rather big subject, but it will try to give a basic understanding of transmission lines, how to make equivalent lumped models and how to read smith charts and S-paramters.

D.0.1 Transmission Lines

The main difference between normal circuit analysis and transmission line analysis is the electrical length. In normal analysis it is assumed the wavelength of the signal that is applied to the circuit is much larger then the circuit. In transmission line theory the signals wavelength is shorter then the circuit. In this way the signal can propagate through the circuit, varying in voltage, magnitude and phase over the length of the line. The characteristic impedance of a transmission line can be represented by series resistance (R), series inductance (L), shunt capacitance (C) and shunt conductance (G). R and G represent loss. These are familiar therms and basically any wire can be represented by this. The characteristic impedance is given by eq.D.1

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{D.1}$$

The ratio between the voltage and current of a traveling wave down a line with characteristic impedance of Z_0 is equal to $Z_0 = \frac{V_0^+}{I_0^+}$ *or* $\frac{-V_0^-}{I_0^-}$ depending on which direction the wave is traveling.

When the signal propagates through a wire and into load with different impedance then Z_0, Z_L the ratio between voltage and current must equal Z_L and so a reflected wave V_0^- must be generated. Imagine if the traveling wave had a voltage of 5 V and a current of 0.1 A right before terminating in $Z_L = 100$ and $Z_0 = 50$. Now where should the excessive power go? 5 V and 0.1 A has to equal 100 ohms.

The relationship between the reflected voltage wave and the incident voltage wave is given by eq.D.2.

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{D.2}$$

The incident and reflected signal causes standing waves and a standing wave ra-

tio, SWR shown the relationship between the top of the standing wave and the bottom, eq.D.3.

$$SWR = \frac{V_{max}}{V_{min}} = \frac{\left|V_0^+\right|(1+|\Gamma|)}{\left|V_0^+\right|(1-|\Gamma|)} = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{D.3}$$

D.0.2 S-parameters and Smith Chart

At high frequencies it is easier to measure incident and reflected voltages rather then currents and voltages, but because the smith chart is based the impedance and admittance matrix the relationship between them will shown. We will focus on the reflected parameters S_{11} and S_{22} because they are the main contributors to mismatch in the open-loop cascade analysis. The relation ship between the impedance and linear port s-parameter is given by eq.D.4, the magnitude and VSWR at given port eq.D.5 and the magnitude of the s-parameter in term of the reflection parameter at given port eq.D.6D.7. Examples of this is used in smith chart is shown in sec.2.1.5.

$$Z_n = Z_0 \frac{1+S_{nn}}{1-S_{nn}} \tag{D.4}$$

$$VSWR_n = \frac{1+|S_{nn}|}{1-|S_{nn}|} \tag{D.5}$$

$$|S_{nn}|\,(dB) = 20log\,|\Gamma_n| \tag{D.6}$$

$$\Gamma_n = \frac{VSWR-1}{VSWR+1} \tag{D.7}$$

D.0.3 Lumped equivalent models

Current which flows in a transmission line creates a magnetic field that impedes the current flow thus creating a series inductance, fig.D.1. The conductor possesses capacitance to the ground. The value for the inductor and capacitance is

$$L_1 = L_2 = \frac{Z_0 tan\frac{\theta}{2}}{\omega} \tag{D.8}$$

$$C_1 = \frac{sin\theta}{\omega Z_0} \tag{D.9}$$

θ is the electrical length of the transmission line and Z_0 is the characteristic impedance. For TL2 and TL3 in fig.D.2 value for C1 and L1 is given by

$$C_1 = \frac{tan\theta}{\omega Z_0} \tag{D.10}$$

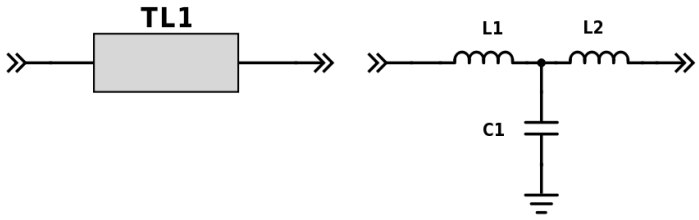

Figure D.1: Equivalent circuit for a transmission line.

$$L_1 = \frac{Z_0 tan\theta}{\omega} \tag{D.11}$$

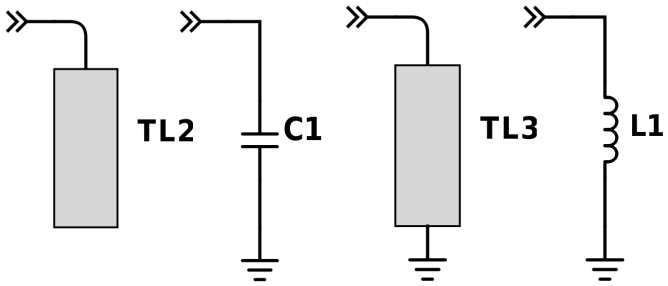

Figure D.2: Equivalent circuit for a open transmission line (left) and shunt transmission line (right).