Proton computed tomography readout testing and detector design

A thesis by

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Abstract

Proton computed tomography is a way of using protons instead of x-rays to make a three dimensional image of a scanned object. This will result in more accurate predictions for proton treatments and less radiation in the surrounding tissue. This will be realized through the use of an array of particle detector chips developed at for the ALICE ITS upgrade at CERN.

This thesis covers work done in chips testing and detector design specification, the most important of which is how the test code work and what the results tell us. This is then considered to give the minimum and basic specifications for the detector and its readout electronics.

Understanding the ALPIDE is of major importance to the PCT project and is one of the reasons for this thesis. Therefore test were done with the ALPIDE test software to get data from the chip. The software was also used to do tests with radiation sources which gives good insight into what particle hits look like.

Acknowledgment

I will start this thesis with a thank you to the university and professor Kjetil Ullaland and associate professor Johan Alme for giving me the chance at a master degree. A huge thanks to my wife for getting me up in the morning. It has been hard work and lots of frustration getting this thesis done, but I am glad I did. Starting this I did not know where it would end up or how to get there but I have learned a lot. I chose this task because it was interesting and something new and visionary. As this thesis is part of a cancer treatment project it is something that is going to positively affect the future and that is something I find meaningful to do.

I would also like to thank Simon Voigt Nesbø, Ganesh Jagannath Tambave and Felix Reidt for their help and expertise.

Contents

Acronyms

ALICE	A Large Ion Collider Experiment
ALPIDE	ALICE Pixel Detector
CERN	"Conseil Européen pour la Recherche Nucléaire" European Council for Nuclear Research
CMOS	Complimentary Metal Oxide Semiconductor
CT	Computed Tomography
DAC	Digital Analog Converter
DAQ	Data acquisition
ECC	Empty Core Cluster. A doughnut shaped particle hit
FIFO	First In First Out, Usually used to describe how a buffer/memory holds and transfers data
FPGA	Field Programmable Gate Array
IB	Inner barrel, This is one of the staves that the ALPIDE chips are assembled into for the ALICE project IC Integrated circuit
ITS	Inner Tracking System
LET	Linear Energy Transfer
LHC	Large Hadron Collider
MAPS	Monolithic Active Pixels Sensor
MDM	Module Data Management
OB	Outer barrel, This is one of the staves or modules that the ALPIDE chips are assembled into for the ALICE project
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCT	Proton computed tomography
RRU	Region Readout Unit
USB	Universal Serial Bus. A common bus used for communication between computers and peripheries.
Vbb	Voltage Back Bias. An important setting for the ALPIDE.

Glossary

Threshold Since it is threshold and not sensitivity that is used in the ALPIDE documentation the use has been continued here.

8b/10b A way of encoding 8 bits to 10 bits for the purpose of error correction

Bragg peak The region where particles stop in tissue and therefore an area of high radiation dose

IP core Intellectual property core. A proprietary part or code in an IC.

NWELL A negative doped part of a semiconductor used to make diodes and transistor.

Xb X is the number of bits, hence the b. eks. 8b

XB X is the number of bytes, hence the B. eks. 8B

Multiplexer A multiplexer takes many data inputs and converts it to one output.

Firmware A piece of code inside a chip.

ROOT Software for processing data and make plots.

1 Introduction

1.1 Background and motivation

The reason for the project this thesis is a part of is to improve cancer therapy. High energy photons has been the most common radiation therapy for treating cancer but lately charged particles has made an entry. The main benefits of charged particles is the area surrounding the tumor receives less radiation [8].This results in a reduction in radiation induced secondary cancers. To improve the accuracy of the proton treatment it would be beneficial to know what the object or person looks like from a protons perspective. Therefor it is proposed to make a CT image with protons.

1.2 About this thesis

The purpose of the thesis is to gain knowledge about the ALPIDE chip and how it works and from this make a set of specifications and requirements for the PCT detector and readout electronics. The ALPIDE is a Monolithic Active Pixel Sensor detector chip developed for use in the ALICE ITS upgrade at CERN. The PCT detector will be made of layers of these chips, all of which will be connected to FPGAs for the data readout.

The tests of the ALPIDE were done with the software provided by the ALICE ITS upgrade team. A lot of time went into figuring out how this software worked and looking at the code to understand what the tests do as there was little to none documentation when the project started. The reason for this being that the ALICE upgrade was also in progress and therefore complete documentation had yet to be written. This resulted in good understanding of how to run the tests and what to make of the output.

The test results show how the chip responds to stimuli and are very helpful for understanding what the chip does. Many of the tests give important information for calibrating the chips. "Luckily" there were some defects in the chips which shows how the chip can fail and what to look for if this happens.

Tests were done with radioactive sources, these give great insight in what to expect from a particle hit.

For the readout electronics it makes the most sense to use FPGAs. Therefore some work was done to determine the requirements and necessary specifications of the FPGAs. Since there will be hundreds of chips, all of which requires high speed communication, only the newest and best FPGAs are up to the task. The most important feature for the FPGAs is high speed LVDS communication and lots of I/O ports. The reason for the LVDS requirement is that due to the number of chips it is necessary to use the regular I/O of FPGAs as none of them come with enough high speed transceivers.

References that are listed in the end of a chapter or sub chapter may be refer to the whole section.

1.3 Thesis outline

An overview of the chapters

Chapter 2: Proton computed tomography is explaining radiation therapy and the benefits of using protons instead of photons. This chapter also goes through the concept of proton computed tomography

Chapter 3: The ALPIDE This chapter describes the ALPIDE and the ALICE ITS upgrade. Since the ALPIDE chip is developed for the ALICE ITS upgrade there will be a lot of overlap between the detector designs and the testing and verification of the chips. Therefore the knowledge from ALICE is very valuable and a natural starting point for the thesis as it gives a good understanding of the ALPIDE.

Chapter 4: The test setup This chapter describes the ALPIDE test setup and the accessories needed to preform tests and verification of the chips.

Chapter 5: The tests This chapter describes the test written for the ALPIDE and what they are testing

Chapter 6: Test results This chapter goes through the result from the different tests and analyses the data.

Chapter 7: Detector design ideas This chapter brings all the previous ones together and defines a set of specifications and requirements for the PCT detector.

Chapter 8: Discussion and conclusion This chapter summarizes the work and discusses what needs to be done for further testing and completion of the project.

Appendices Extra information.

2 Proton therapy and Proton computed tomography

To understand way PCT has advantages over CT using photons it is important to know the difference between protons and other charged particles, and photons. This chapter will go through that and how this makes PCT superior in some cases. Proton therapy has been on the rise lately and as of 2015 more then 137 000 patients have been treated with charged particle therapy.
[10]

2.1 Radiation

PCT and conventional CT work by irradiating an object or patient and detecting the shadow cast by the obstruction. Therefore it is important to have at least a basic understanding of radiation. There are many types of radiation some natural and some man made. Natural sources of radiation comes from radioactive nuclei and cosmic radiation, which we call background radiation. Examples of man made radiation is X-ray tubes and particle accelerators.

Another way to characterize radiation is ionizing and non-ionizing. Ionizing radiation has enough energy to rip electrons from atoms turning them into ions, hens the name ionizing radiation. Because of this ionizing radiation can be very destructive, which in a medical setting can be both good and bad depending on the procedure. Charged particles like protons, alpha- and beta-particles can directly ionize an atom due to the way they directly interfere with it. Uncharged particles are indirectly ionizing, these include photons and neutrons.
[7][11]

2.2 Photons interaction with matter

Photons interact with matter in three main ways. The first is the photoelectric effect, which is when a photon is absorbed by a orbital electron with equal or greater binding energy. This will either excite the atom or ionize it. The second is Compton scattering, which is an elastic collision with an outer shell electron. Due to the photon having such a high energy it will knock the electron out of orbit, lose some energy and change direction. The electron will gain the energy lost by the photon and move in an angle proportional to the photons loss in energy. The third is pair production, which is when the photon converts into a positron/electron pair. But for this to happen the energy of the photon must be equal to or greater then to electron masses.

Photons are attenuated as they travel through matter, due to this the photon beam will have the highest intensity where it enters an object and lose intensity the further it travels. [7]

2.3 Proton beam interaction with matter and proton therapy

The main mechanism of energy loss for a proton beam in matter is the protons colliding with orbital electrons. As the proton, or in general any heavy charged particle, moves through matter it will interact with the orbital electrons through inelastic scattering. A proton will slow down through collisions with electrons and eventually stop. The amount of energy deposited along the protons path is dependent on the distance to electrons and the time it spends near them. Another term used to describe this is specific ionization as it is focused on the energy lost by the radiation. To measure the energy loss we use the linear energy transfer (LET).

$$LET = \frac{dE_L}{dl} \tag{1}$$

In equation 1 the term dE_lrefers to the energy transferred to the absorbing object over the distance dl. This term is more interesting from the radiation therapy point of view, as the energy deposited in the patient is more important when considering radiation therapy or the side effects of radiation.

As the proton slows down, the deposited energy increases. The area where the protons stop is where the largest amount of energy is deposited and corresponds to the Bragg peak. The Bragg peak, see figure 1, is an important feature of proton therapy, the reason being that after it there is almost no more radiation, and the largest radiation dose is delivered here. Photons on the other hand deliver the most energy where they enter the object, this is because a photon beam is only reduced in intensity as it travels through matter. Due to the Bragg peak, as illustrated in figure 2, the radiation of surrounding tissue is greatly reduced compared to X-rays.

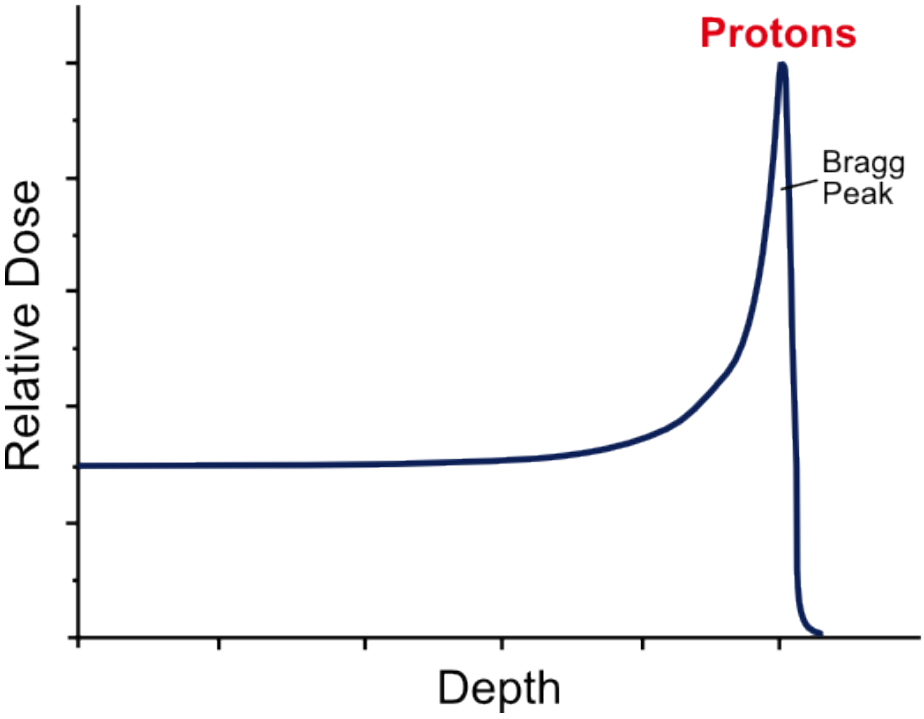

Figure 1: The Bragg peak. As shown here the relative dose is far greater in the Bragg peak and negligible after it. [14]

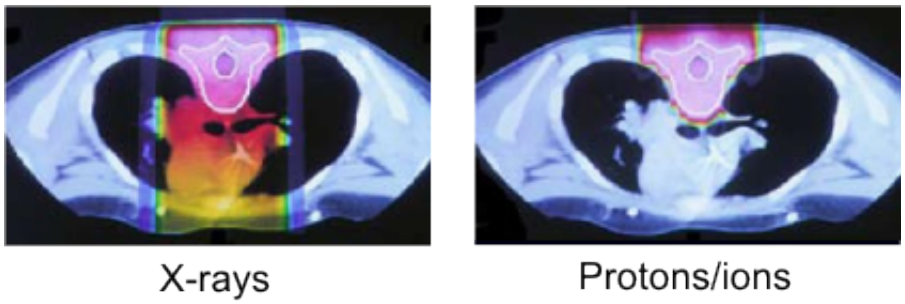

Figure 2: Photons vs Protons in tissue[14]

As seen in figure 2 the area behind where the radiation therapy is supposed to hit receives less to none of the radiation compared to photons.
[7][10]

2.4 PCT

Proton Computed Tomography (PCT) is CT using protons instead of x-rays to scan an object or a patient to make a 3D model. This results in a more accurate picture of how protons behave in the body and takes the estimation from x-ray CT out of the equation in the case of proton therapy planning. Although x-rays have a higher resolution, the accuracy of knowing more precisely how protons behaves makes up for this. The PCT scan gives a map of the relative stopping power of the object being scanned. Because protons mainly lose energy through collision, they will slow down as they move though matter. Therefore matter stops the protons and this is measured in relative stopping power. [7] [10]

To use protons for CT they need to pass through the object being scanned. As opposed to X-rays which are attenuated, all protons go through and simply analyzing the "shadow" is no good as this will produce an image. One must therefore find the energy the proton has after going through the object. Using only the energy after penetration is a possible way of doing PCT but this method has shown limitations. The limitations being spatial resolution and edge artifacts[9]. An alternative to this is proton tracking. With this method every proton is tracked and their energy after penetration measured. This method has been used with position sensitive detectors and either calorimeters or scintillators, but has the limitation that only one proton can be tracked at once. This method has been used by several PCT projects including one at Loma Linda University[15] and the Italian project PRIMA[9].

The PCT prototype being developed at the Department of Physics and Technology at the University of Bergen is trying to address some of these problems. The proton detection and measurement is done with high-granularity silicon particle detectors. These detectors are chips consisting of 1024*512 pixels each of which can detect particles going through them. The full detector design will have several layers of these chips. The proton hitting the detector will then leave a path of activated pixels corresponding to its path. The dept of penetration, the amount of layers it goes through, is corresponding to its energy. This will therefore find both the proton path and the energy in one detector. Another huge benefit of this is that because of the high resolution several protons can be tracked at once. [10]

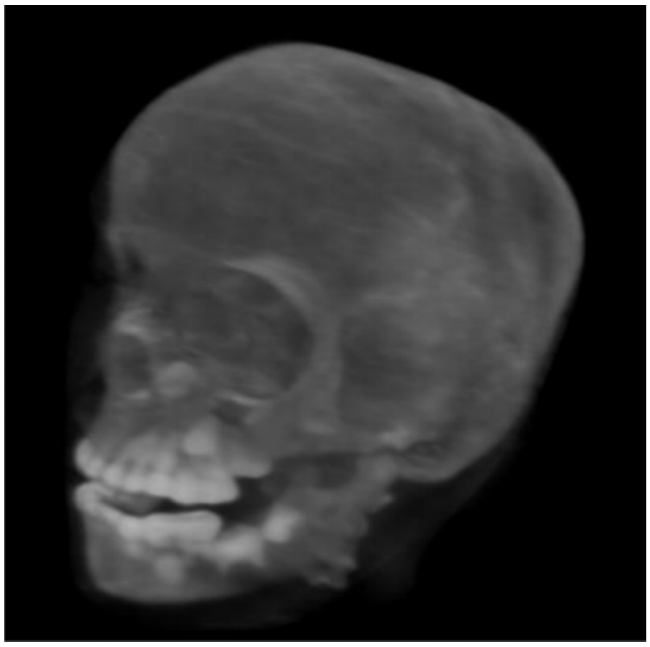

Figure 3: PCT of head phantom[20]

Figure 3 shows a head phantom scanned with a PCT prototype. The image shows the relative stopping power of the head phantom. [20]

As a side note I have found that visualizing the PCT detector as a pinscreen helps with understanding what the detected "image" looks like. Here the protons are the pins. Though this is not an entirely good analogy, it works to some extent.

3 The ALPIDE

The ALPIDE is a particle detector chip designed to be used at CERN for the ALICE ITS upgrade. It is based on Monolithic Active Pixels Sensor (MAPS) And implemented using 180 nm CMOS technology for image sensors.
[1]

3.1 The ALICE ITS upgrade

ALICE is an experiment at CERN and is one of the four large detectors stationed around the LHC. The ITS part of ALICE, the inner tracking system, is scheduled for an upgrade in 2019-2020. This is what the ALPIDE is developed to do. The ITS is made up of ALPIDEs surrounding the particle beam, see Figure 4. The ALPIDEs are arranged into seven layers. The three inner layers will use inner barrel mode and are made up of inner barrel staves. The middle two layers will use chips in outer barrel mode arranged into outer barrel staves in middle layer modules. The two outer layers are chips in outer barrel mode arranged in outer barrel staves in outer barrel modules. The differences of inner/outer barrel modes are explained later in this chapter. Inner barrel staves are 1x9 chips each with their own high speed connection. Outer barrel staves are 2x7 chips

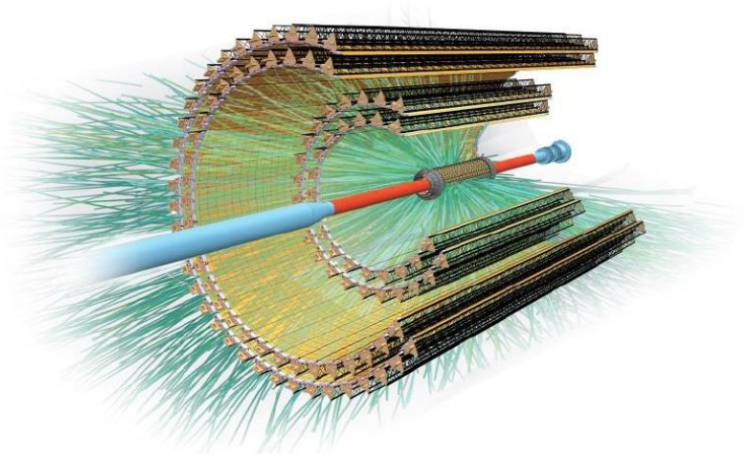

Figure 4: ALICE ITS, a sketch of the new detector to be built at ALICE. [13]

3.2 The ALPIDE

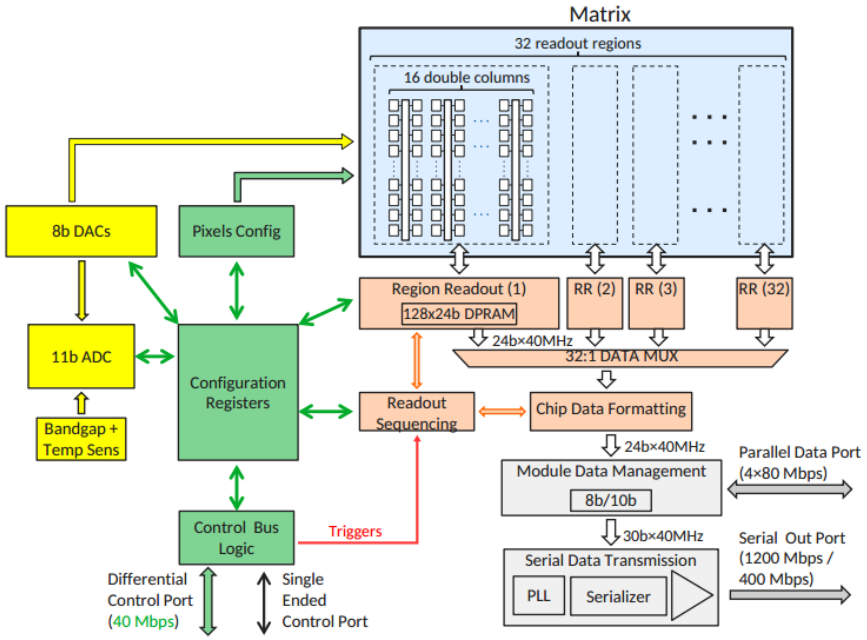

Figure 5: ALPIDE chip block diagram[1]

Table 1: ALPIDE specification

Size:	1,5 cm * 3 cm (1,2mm*30mm periphery circuit region)
Thickness:	50 µm - 450 µm
Pixel size:	29,4*26,88 µm
Pixel arrangement:	512 x 1024
Supply voltage:	1,8 V
Process:	180 nm
Power:	40 mW/cm2
Data rate:	400, 600 or 1200 Mb/s

The ALPIDE is a matrix of 512 by 1024 detectors, or as described in the ALPIDE manual, pixels [1]. These pixels are grouped into double columns, so it can be viewed as 512 by 512 double columns. This is important to remember when decoding the data as a raw data value that seems to be on the edge of the chip might be in the middle of it. These double columns are grouped together in regions, each containing 16 double columns, for a total of 32 regions. Each region has a Region Readout Unit (RRU), which read out the double columns

sequentially. The RRUs are sent trough a multiplexer before being encoded in 8b/10b encoding and sent out from the chip.

The chip can be configured in three different modes, inner barrel, outer barrel master and outer barrel slave.

The pixel have a diode in reverse bias, which is the detector, an amplifier and a digital section. When the diode is hit by a particle it produces a voltage drop which is then amplified and sent to the digital section as a hit if it reaches a set threshold.

3.3 The pixel

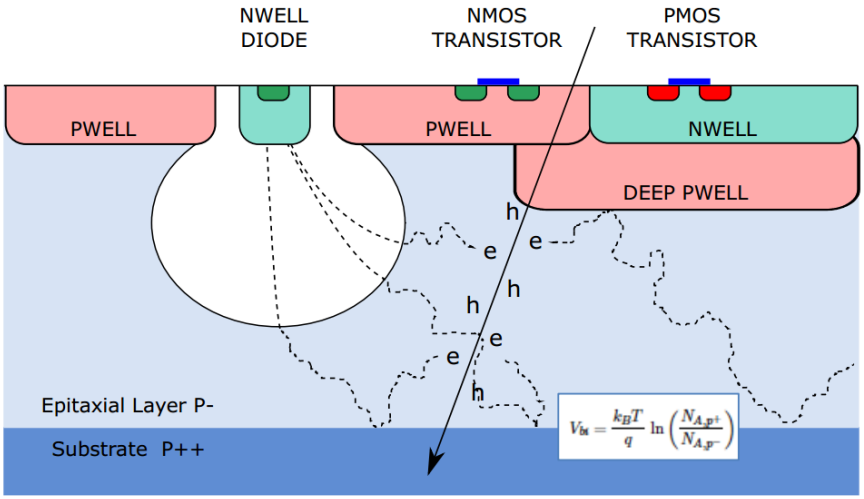

Figure 6: The pixel cell[13]

Figure 6 shows how the pixels work. If a particle hits the pixel it creates a lot of charge. This charge results in a voltage drop over the collection diode, the NWELL DIODE in figure 6.

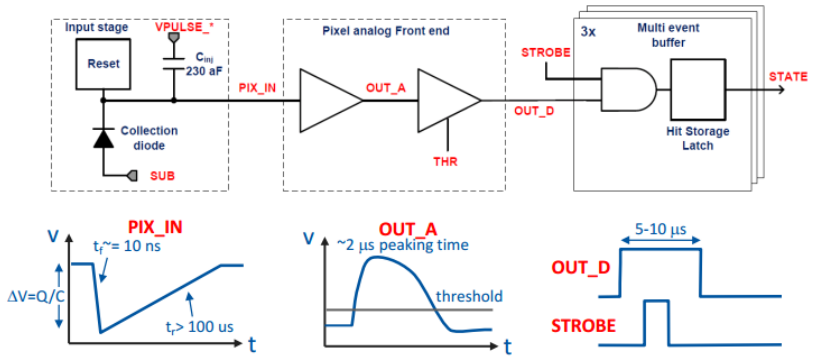

Figure 1.2: Block diagram of the ALPIDE pixel cell.

Figure 7: Block diagram of singel pixel and readout[1]

Figure 7 shows a block diagram of the pixel cell and the individual pixel readout electronics. It also shows what the signals look like in the different part during a particle hit event. As explained earlier, a particle event will create a voltage drop over the collection diode. This voltage drop is amplified and measured against a threshold in the pixel analog front end. If the signal is above the threshold and a strobe signal is present the signal will be sent through to the next part of the read out, the RRU.

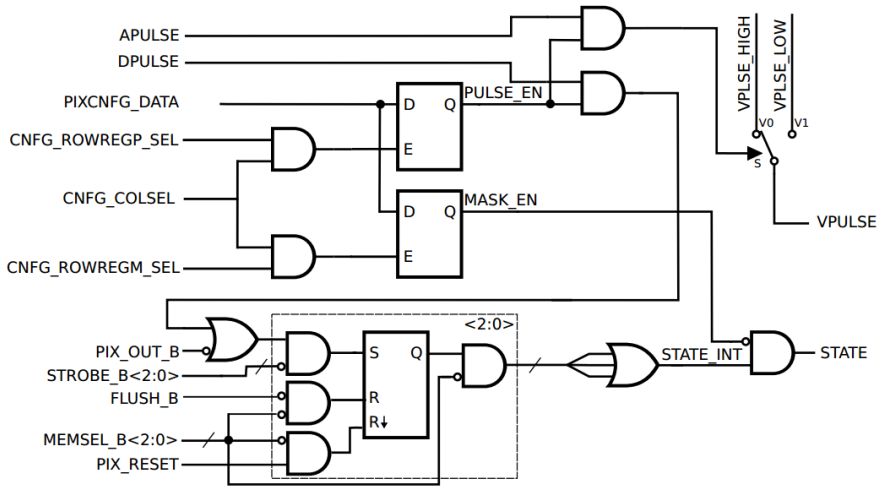

Figure 8: Block diagram of pixel logic

[1]

The pixels can all be turned on and of trough the pixel mask settings. Because of this it is possible to turn on and of individual pixels. This is done through the ROWREGP_SEL, COLSEL and ROWREGM_SEL registers. The logic of this can be seen in figure 8. The ROWREGP_SEL enables the pulse from the pixels trough to the readout, this is a per row setting. The COLSEL enables a column of pixels. The ROWREGM_SEL enables the pixel to be read out. Together these form a pixel mask setting.

3.3.1 The pixel amp

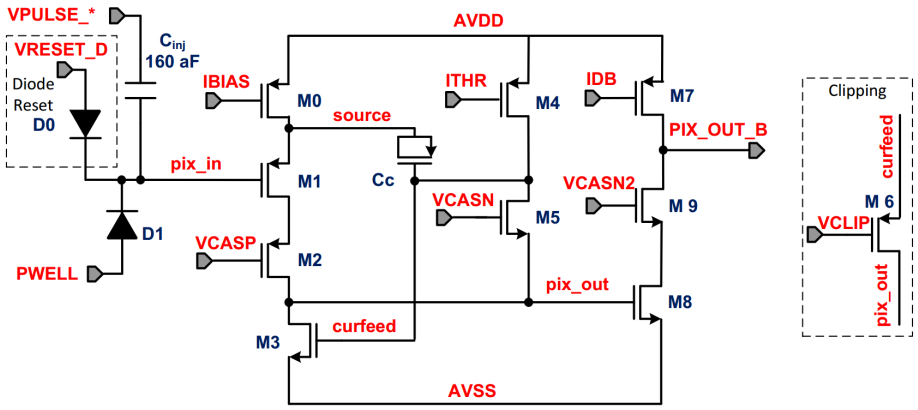

Figure 9: Schematic of the pixel amp [1]

The pixel amp or analog front-end as it is described in the ALPIDE operations manual [1] is amplifying the particle hit and compares it to a threshold value to make a hit/no hit binary output. A hit will cause the node pix_in to fall by a few tens of mV. This will cause the source node to drop as well due to the lowering of the current in M3 and raising the pix_out node by hundreds of mV. This will force the PIX_OUT_B low if the charge from the particle is high enough to overcome the current setting IDB on M7 which will cause M8 to drive PIX_OUT_B to 0. The charge threshold is set with ITHR, VCASN, and IDB, this is further explained in the chapter about pixel amp settings. [1]

3.4 The Regional Readout Unit

The RRU is the next part of the readout. It is connected to the double columns and is responsible for collecting the data from one region, that is 16 double columns. This is done sequentially for the different columns. The double columns themselves have a priority encoder and zero suppression. In the RRU there is also a pixel buffer in form of a 128*24b FIFO. There are 32 RRUs in

total, one for each region. After the RRUs the data is multiplexed together to make it a serial data stream before global readout. [1]

3.5 ALPIDE communication

The ALPIDE has two ways to send out data, one high speed serial out and one parallel output. They are intended for different purposes, and are both important for this project. The high speed serial output is intended to be used for data out to a common readout unit. For the inner barrel configuration every chip has it own high speed line, this is due to the high flux environment they are in. The outer barrel master chips also has a high speed connection to a common readout unit. The parallel output is used to send the data from the outer barrel slave chips to the outer barrel master chips. Due to the parallel communication only being used in outer barrel mode it is disabled for inner barrel mode. This is important to remember when switching between modes for testing purposes.

3.5.1 The control ports

MLCK_P, MCLK_N: Clock forwarding input port, used for clock sharing in the outer barrel application
RST_N: Global reset, active low.
POR_DIS_N: Disabling the power on reset feature, active low.
DCTRL_P, DCTRL_N: Differential bidirectional control port. Intended to implement the control bus between the control electronics and the IB and OB master chips. Half duplex.
DCLK_P, DCLK_N: Main clock input and forwarded clock output.
CTRL: Single ended, bidirectional control port. To be used for local control between the OB master and OB slave.
BUSY: Single ended port. To be used to communicate the busy state of OB slaves and OB master.
DACMONV: Analog pin. Used to monitor the different DAC voltages or override the internal DACs. The override can only be done for one DAC at a time.
DACMONI: Analog pin. Used to monitor the different DAC currents, override the internal DACs or override the reference current. It is possible to override one DAC at a time or the range of all of them by overriding the reference current.
CHIPID[6:0]: Chip address and mode selection. The address is intended to give the position on the stave and the mode of the chip.

[1]

3.5.2 The data ports

HSDATA_P, HSDATA_N: High speed serial differential data output port. This port is used for the communication between readout electronics and chips configured in IB and OB master mode. The data rate on this port is 1,2 Gb/s

(default), 600 Mb/s or 400 Mb/s in IB mode and 400 Mb/s in OB master mode. This data stream is 8b/10b encoded.
DATA[7:0]: CMOS bidirectional data port. This is the parallel data port between the OB slave and OB master.

[1]

3.5.3 Inner barrel and outer barrel differences

The difference between the inner barrel and outer barrel communication with the readout electronics is the speed and if all the chips are directly connected to the readout electronics. For the IB chips, every chip has a high speed connection to the readout electronics. For the OB chips only the master chips have a high speed connection to the readout electronics. The slave chips send their data to the master over the parallel data port and the master forwards it to the readout electronics over the high speed serial port.

The main difference between the settings IB and OB is the readout speed and the readout port. For the purposes here both are necessary. The parallel port, and therefore outerbarrel

3.6 Why choose the ALPIDE

The ALPIDE is designed to detect particles for the ALICE experiment at CERN. It is a state of the art particle detector chip. One of the important features is the small pixels which makes it easier to accurately determine the path of the particle. Another important feature is the high data rate the ALPIDE can sustain. This is important for making the scan time for PCT as short as possible.

3.7 Setting up the ALPIDE for testing and particle detection

For the ALPIDE to work it is important to set a handful of parameters to within the optimal range for particle detection. Most of these are internal DACs that set voltages and currents in the pixel amplifier and an external p-well voltage, labeled Vbb from here on.

3.7.1 The DACs, Settings of the pixel amp.

The pixel amp can be seen as a fully adjustable amplifier as all of the bias voltages and currents can be adjusted through the DACs settings. The values in table 2 are the ones normally used [16]. These values are a good starting point and can be used for testing. The values are given for a few different values of Vbb.

Table 2: DAC settings that are normally used.

DAC	**Vbb= 0V**	**Vbb= -3V**	**Vbb= -6V**	**Info**
ITHR	50			Increasing this increases threshold and makes the response shorter
VCASN2	67	117	147	VCASN2 = VCASN + 12
VCASN	50	105	135	Increasing this lowers the threshold
VCLIP	0	60	100	
VRESETD	147	170	170	
IDB	29			Fixed for all values of Vbb
VCASP	86			Fixed for all values of Vbb
IBIAS	64			Fixed for all values of Vbb
VPULSEH	170			Fixed for all values of Vbb

The important values here are ITHR, VCASN and VCASN2. These are the DACs that govern the threshold. To change the threshold it is best to use ITHR, the reason for this will be given in chapter 6.4.

4 The test setup

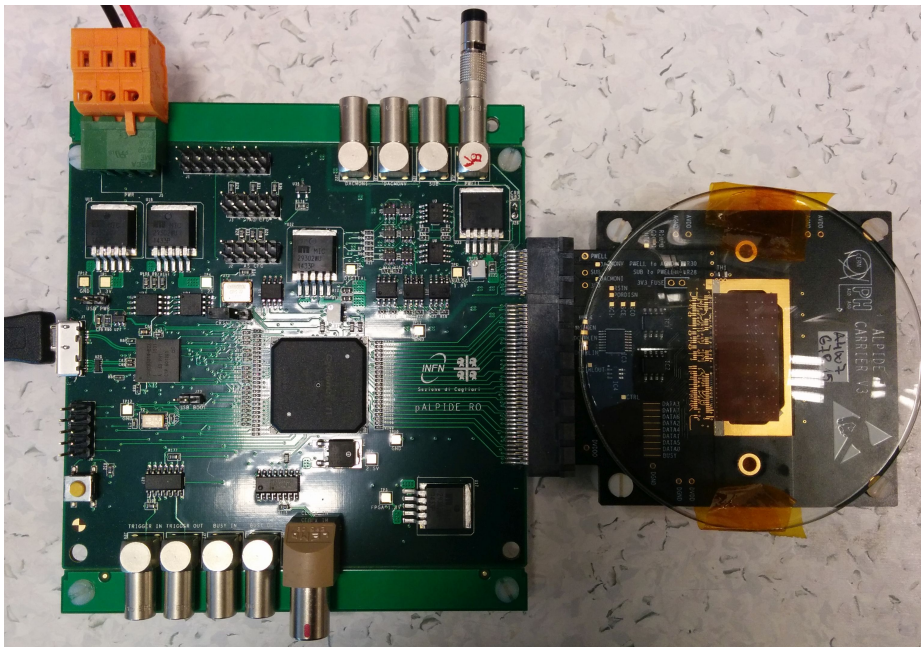

Figure 10: ALPIDE test setup with DAQ (left) board and ALPIDE carrier card

Figure 10shows the test setup. In the upper left corner of the DAQ board it is connected to a 5 V power supply. In the upper right corner of the DAQ board a short circuit is made to set the back bias of the detector diode to 0 V. A voltage can be supplied here for the back bias, but if this is nor done it has to be shorted. A USB connector can be seen on the left side of the DAQ board, this is used for communication with a computer. The ALPIDE carrier card is connected on the right side of the DAQ board through a PCI connector. The carrier card is covered with a glass plate to protect the chip from damage.

4.1 The readout board

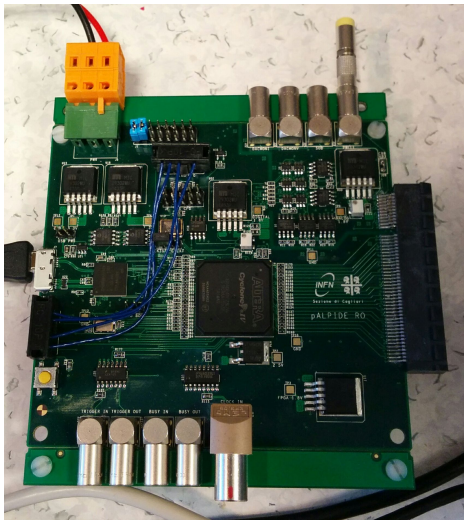

Figure 11: Picture of DAQ board

The readout board is from the ALICE ITS upgrade team and is referred to as the DAQ board. It is designed for testing and verifying the ALPIDEs during development, as it can only test one chip at a time. The DAQ board can only use the parallel out of the ALPIDE. Because of this the chip must be in OB mode.

Because the DAQ board only uses the parallel out of the ALPIDE and can only be used with the ALPIDE carrier card, testing more then one chip at once is highly impractical. The DAQ board is good for learning about the ALPIDE and for understanding the tests but becomes obsolete for system testing.

Before the DAQ board can be used the USB FX3 chip has to be configured. To do this a supplied firmware has to be uploaded to it. This has to be doe every time the DAQ board is powered on as the setting does not persist through restarts. It is therefore advised when testing, as it can lead to many restarts, to run this in the terminal "watch -n 1 ./download_fx3 -t RAM -i SlaveFifoSync.img" [16]. This will automatically check for a newly connected DAQ board and then load the FX3 firmware every second.

[3]

4.2 ALPIDE carrier card

Figure 12: The ALPIDE carrier card

This is a card containing the ALPIDE chip. It uses a PCI connection to connect to the readout board. To do tests with sources, the glass cover must be removed. It is possible to place the source under the carrier card but than some of the chip is masked by the PCB. The CHIPID can be changed by shorting or connecting the resistors R2-R8, R8 being the most significant bit. For using the DAQ board the CHIPID must be 16, which corresponds to R6 being shorted.

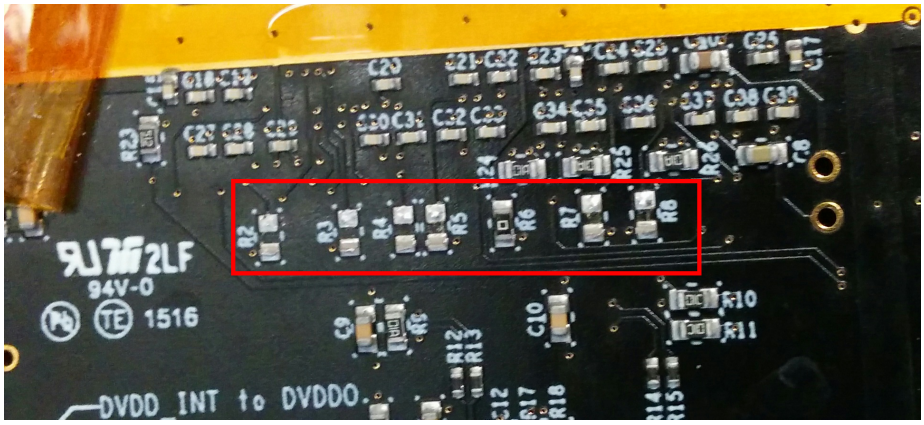

Figure 13: The CHIPID resistors

4.3 The full setup

The full setup can be seen in figure 14 as a simple sketch and a picture of the setup can be seen in figure10.

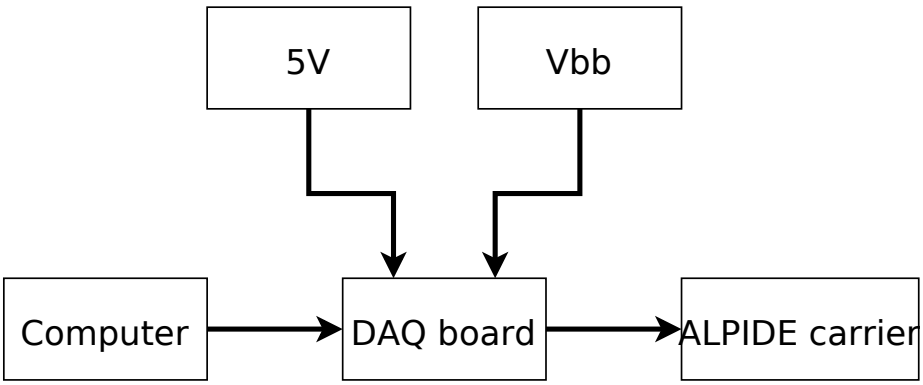

Figure 14: Simple sketch of test setup

The ALPIDE carrier is connected to the DAQ trough a PCI port which supplies it with all necessary voltages and data/control lines. The DAQ board is connected to a computer trough USB and communicates with the software provided by the ALICE ITS upgrade team. The main power supply is 5V. The Vbb is the back bias for the detection diode, this can be between 0-6 volts but is usually 0, 3 or 6 volts, This have to be shorted if no voltage is supplied resulting in 0V.

4.4 The test code

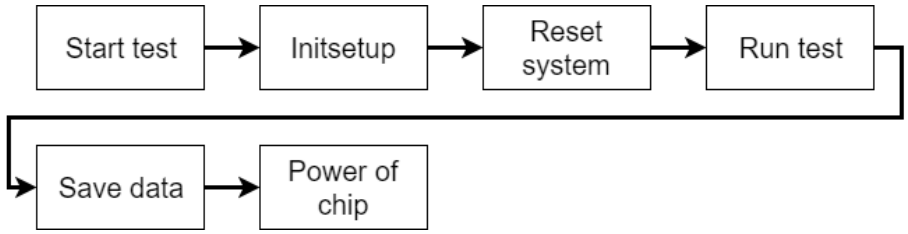

Figure 15: General overview of the code execution

The code from CERN helps a lot when trying to understand how to talk to the ALPIDE and daq board. Most of the code is very useful for testing. The different tests help with characterizing the different values. A very important file is the config.cfg which contains the DAC settings and readout settings, further explanation will be given in chapter 4.4.1. For many of the tests there exists a ROOT script to make graphs of the data.

All the tests start out with the same procedure which is to search for readout boards and adding them to a vector.

4.4.1 The config file

The config file is where the main parameters of the and readout boards are set. The DEVICE value has to specified to "CHIP" for the purposes of the testing done here as only single chip testing has been done. Other options are; OBHIC, IBHIC, TELESCOPE, CHIPMOSAIC and HALFSTAVE. These will not be further discussed.

The next thing is scan parameters. Since testing the whole pixel array at once is not possible, one must set a number of masks to be used. The mask sets the number of enabled pixels per region. There are 32 regions and on the each containing 16384 pixels. Therefore it follows that the maximum number of masks is 16384. This is set by the "NMASKSTAGES parameter. It is possible to scan up to 32 pixels per region at a time, this is set in the "PIXPERREGION" parameter. This results in $\frac{16384}{32} = 512$ masks. When the readout board allows 32 pixels per region it should be used as it reduces run time for the test significantly. For the DAQ board the value of PIXPERREGION should be 4, this is limited by the memory on the DAQ board[16]. It is also possible to change the charge parameters of the threshold test from here, but they will be discussed later in chapter 5.3.

the last thing is the chip settings. Here we find the DAC settings, the setting of these are covered in chapter 3.7.1.

4.4.2 DACscan test

Scans all the dacs. Writes all possible values to the dacs then reads them from the dacmonv/i interfaces. This tests finds any faults in the DACs, many of which will render the chip useless. The 0x600 register controls whats sent to the dacmonv/i pins. The values are controlled through their own registers 0x601-0x60E. Tables 3.23-26 from operations manual are useful.[4]

4.4.3 FIFO test

Tests the pixel fifo. Writes patterns to the pixel buffers and reads it back to check for memory errors. The pattern tested are 0x0, 0xff and 0x55. This is a quick test and confirms that communication with the chip works and of course that the memory works. The test is for the Memory in the 32 RRU. [4]

4.4.4 Digital scan

This is a test of the chip from after the analog front end, that is, only the digital part of the chip. This test sets every pixel high 50 times then reads them back. To do this the pixels are masked and scanned systematically. Then the DPULSE, see figure8, is set high. This will then produce a hit to be sent to the

RRU and through to the DAQ board. After the test is done a bitmap of the can be produced through a ROOT script.[4]

4.4.5 Noise occupancy

Scans for data, for a given time and saves the data to a file. Nice graphs can be made with a ROOT script. This scan will show problematic pixels which makes false hits. This scan can also be used for testing with a radiation source. [4]

4.4.6 Threshold

The threshold test is scanning the threshold values for the ALPIDE. This test is modifying the VPULSEL (LOW) value to make larger and larger voltage drops over the detection diode. These results show the signal level, or electron charges, needed to trigger an event. The root script for this test also approximates the noise from this data.

[4]

5 The tests

For the initial chip testing the main thing to do is to replicate the results seen from CERN and find potential flaws in the chip. As seen further down in this chapter our new chip has some broken pixels and the first chip has a broken DAC. This is a good thing as it gives us knowledge on how a chip may be bad and if it matters for detection at all. The matter of the bad chip will be further discussed in chapter 6.8.

5.1 Communication

When the chip is connected and powered up it is good to run some communication test to establish that you are indeed connected to the ALPIDE. This is especially true when connecting to a chip for the first time as other tests are useless if there is no communication. To test the connection one should run the FIFO test described in section 4.4 or the dacscan, as both of these are quick . The FIFO test checks the pixel memory for errors by writing and then reading patterns from it. [12]

5.2 DACscan

The DACscan test is checking that all the DACs in the pixel amplifier works. The test works by writing all the possible values (0-255, corresponding to 0V - 1,8V or 0nA - 10 µA) to a DAC and reading them back through the DACMONV or DACMONI ports on the chip. The main value of this test is to check that the DACs are in working condition. [12]

5.3 Threshold

The threshold scan is checking the threshold of all the pixels. It does this by simulating increasingly larger particle hits. The hits are simulated by creating a pulse that looks like a particle hit on the pixel amplifier input. This is implemented with the VPULSEH and VPULSEL DACs. The size of the pulse is determined by the difference in these two values. The pulse is made by switching from VPULSEH to VPULSEL which creates a falling edge signal on the input. To change the amplitude of the pulse the VPULSEH value is manipulated. In the test as it is implemented the pulse goes from a small value to a large value. Therefore the threshold is found when the pixel starts detecting the pulse. This is done for all pixels and gives a pixel map of the chip where the color is the threshold value (see figure 19). The root script for the this test also produces a threshold distribution which is more important for chip calibration and a noise distribution. The threshold distribution is the value that can be adjusted by changing the DAC values that affect threshold, these being VCASN, VCASN2 and ITHR. This is due to the threshold being a global setting, as it is set by aforementioned DACs, these being global. The test also finds dead pixels as these will not give a response to the pulse. [12]

Before running a full threshold scan one should run a limited one. That is because this is a time consuming test and especially for the DAQ board which take several hours to completes the test.

5.4 Simulation of hits

There are two ways of simulating hits, digital and analog. The analog test is basically the same as the threshold test but with a fixed value for the pulse amplitude, so there has been no testing of analog simulation as it would give the same or less knowledge as the threshold test. Therefore only the digital test will be talked about here. The digital test is testing the pixels without simulating a particle hit but by setting the pixel out high. That is, only the readout part of the pixels and the chip is tested and the front end is bypassed. The value being set high is the DPULSE value in figure 8. This test will highlight flaws in the readout of the pixel, as opposed to the threshold test that will also show error in the front end of the pixel. [12]

5.5 Noise testing

The noise occupancy test is simply reading out data for some period of time and report the events that occurred. This measures the noise of the chip as a perfect chip should not give any hits when it is not radiated. Background radiation will look like genuine hits and can be distinguished from chip noise quite easily when looking at the pixel map that is produced after the test. This is because a genuine hit will most likely activate several pixels and the pixels will only fire once. A noisy pixel which more then likely will have fired several times during a test.[12]

5.6 Radiation testing

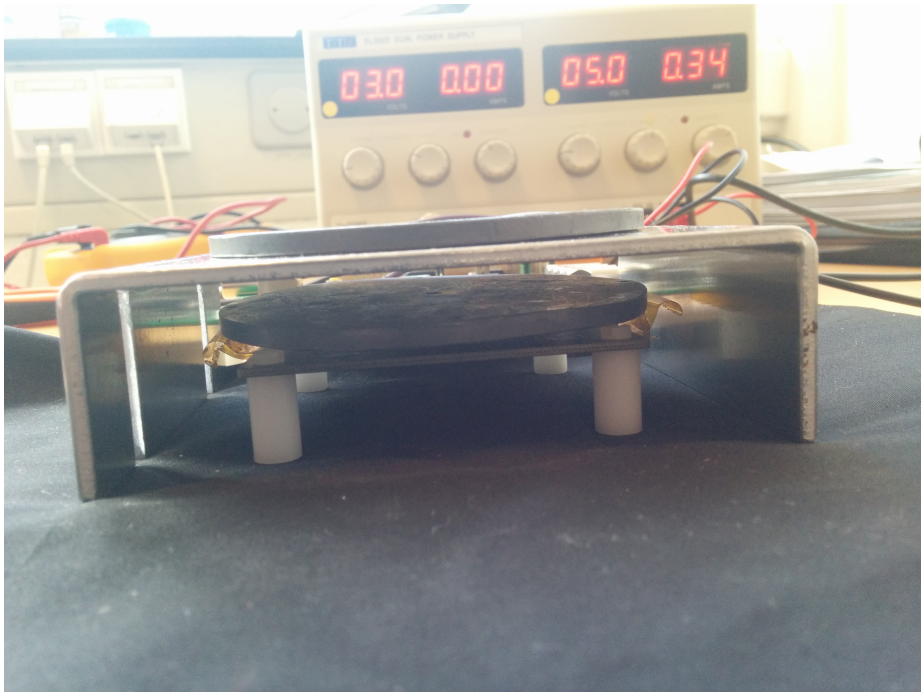

Figure 16: Radiation test setup. From the bottom up: ALPIDE carrier card, lead plate with hole to focus radiation, aluminium stand, lead plate to hold the source.

To test the chip with actual radiation or particle hits a radiation source is needed. The tests that were done was simple but gave good results. The test where done by running the noise scan and then radiating the chip. This was a simple way of running radiation tests without writing new code for it. Some of the tests where done with a lead plate with a hole in it to focus the radiation.

6 Results

6.1 Communication

When the chip is connected and powered up it is good to run some communication test to establish that you are indeed connected to the ALPIDE. This is especially true when connecting to a chip for the first time as other tests are useless if no communication is possible. To test the connection one should run the FIFO test described in section 4.4 or the dacscan, as both of these are fast.

6.2 DACs

When communication is established the next thing to do should be the DACscan 4.4, if the DAC scan was not used for communication test. The DACs in the ALPIDE set voltages and currents in the pixel amplifier and if they do not work the amplifier will most likely not work either. All the voltage DACs should behave linearly from 0V or 0,4V to 1,8V and the current DACs from 0nA to 10µA.

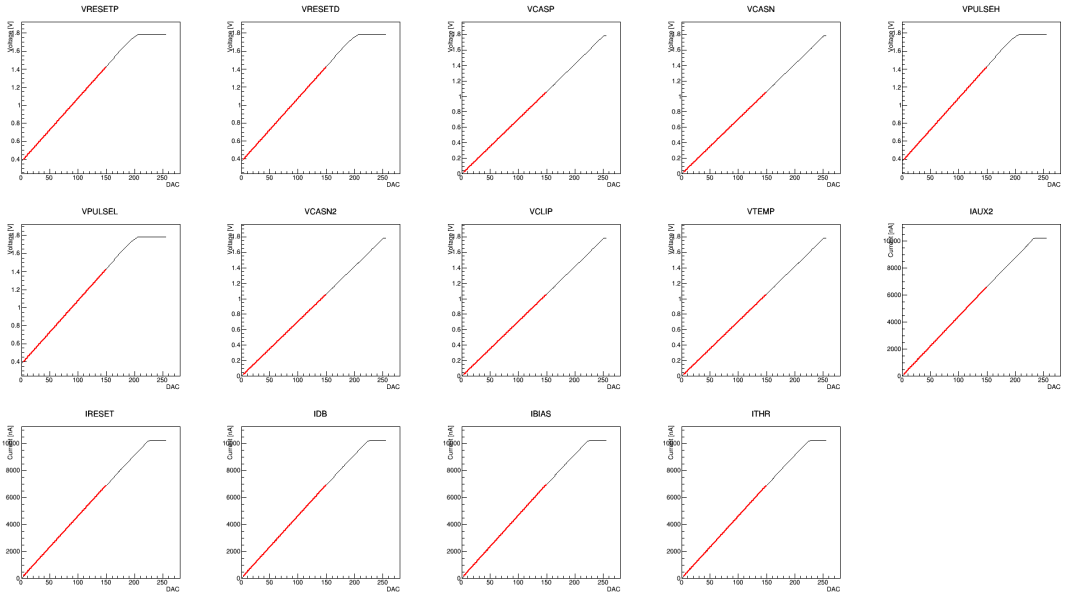

Figure 17: Graphs of a DAC scan made with ROOT

Figure 17 shows the output of the DAC test. The red lines are the ideal values and as one can see the measured values correspond very well to these. The values in figure 17 are from the new chip. The old chip showed an error in one of the DACs. As can be seen from the results, the DACs are supposed to give a linear output based on the 8-bit input but this was not the case for VPULSEH of the first chip. This can be seen in figure 18.

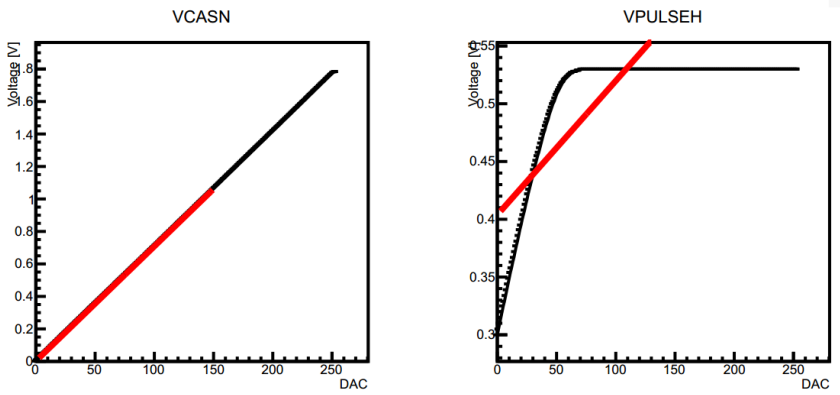

Figure 18: Bad DAC with a good one for comparison. Bad on the right.

The main issue with this is that without this DAC, testing the chips threshold is not possible. It is not critical for the operation of the chip so other tests and operations can be done if no other flaw is present, although the chip can not be calibrated which may be of concern for the detector.

It is impossible to tell if this is a common defect from my testing of two chips but it should never the less be on the list of things to check while testing chips in the future.

6.3 Threshold/sensitivity testing

This test find the threshold values in number of electron charges for the pixels to register a hit. Threshold is the inverse of sensitivity, due to threshold being the measurement and wording used in the test software it will also be used here. The threshold is found for every pixel. The importance of this test is crucial as its results are needed to properly set the threshold for each chip. In figure 19 the threshold is plotted in a color scale to visualize the different values over the chip. There are a few noteworthy things here, The white line which is dead pixels (the possible error is discussed in the chapter 6.5), and The darker squares which corresponds to the bonding points on the chip. This suggests a slightly higher threshold where the bonding points are. This might be because the bonding points contain a lot more metal then other parts of the chip, and this can cause the charge to dissipate faster or not build up sufficiently at all since the charge will spread across the metal. This will make it so that a higher charge from the particle hit is necessary for the charge in the pixel to reach the threshold level. The threshold distribution is plotted in figure 20. This plot is more interesting because it provides the information needed to adjust the calibration. Changing the parameters VCASN and ITHR in the pixel amp changes where the mean value is.

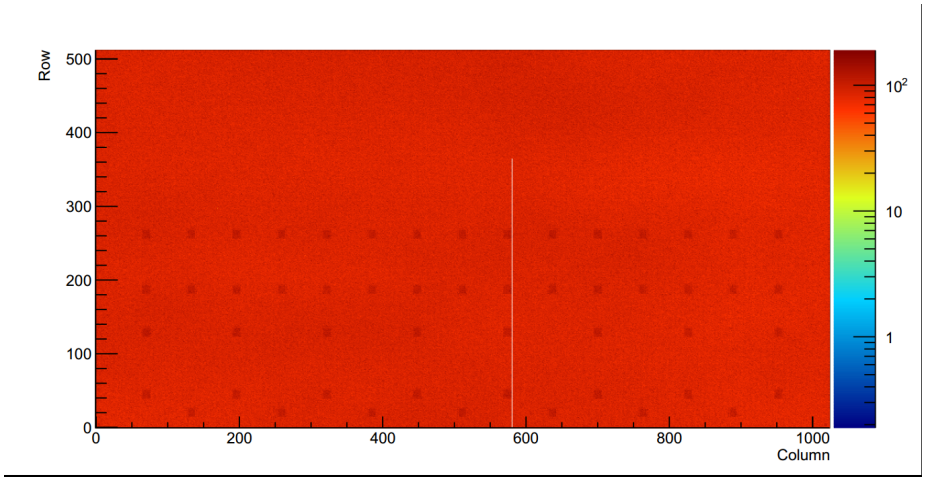

Figure 19: Bitmap of full threshold scan

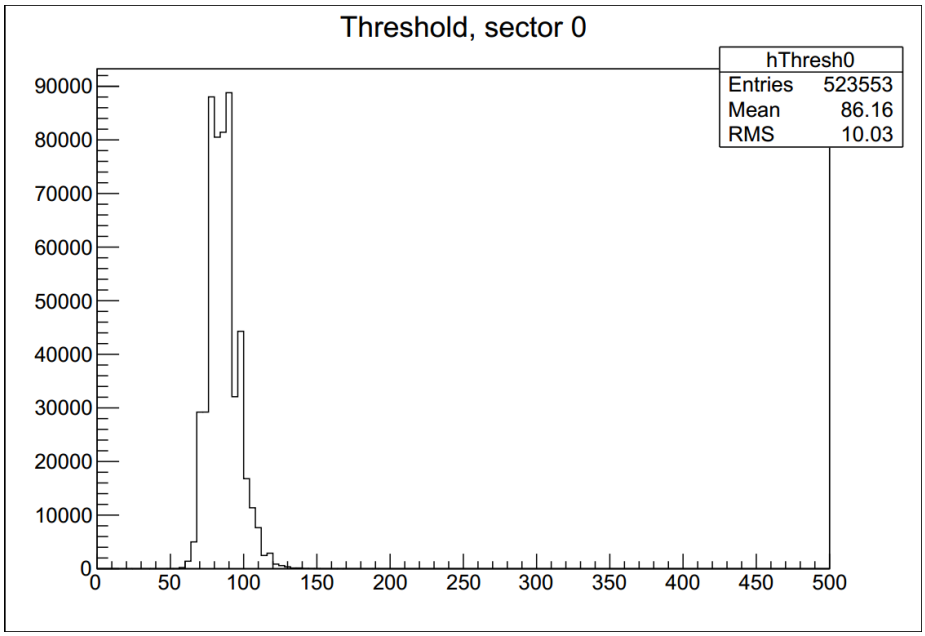

Figure 20: Threshold distribution.

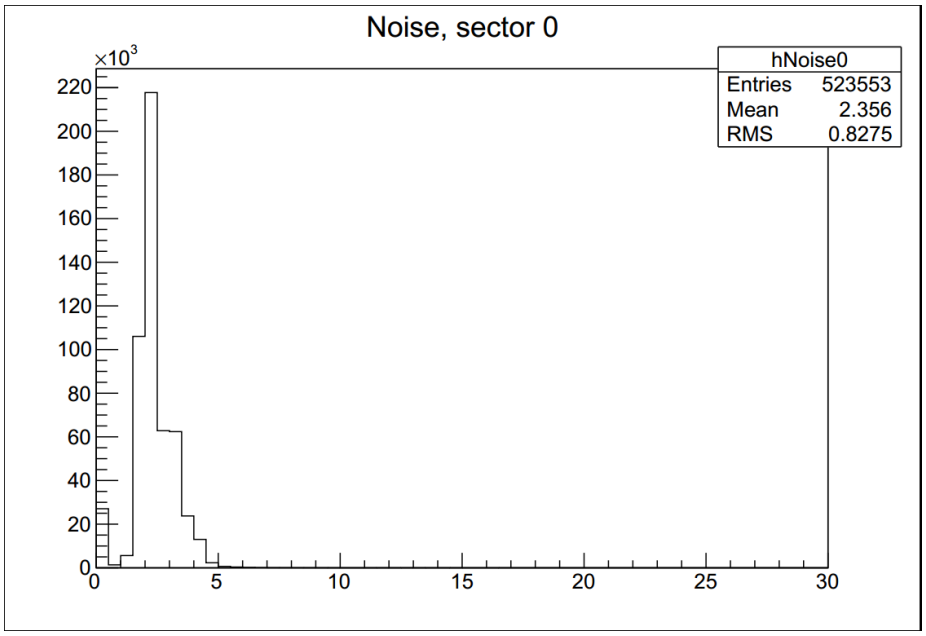

Figure 21: Noise distribution for threshold

Table 3 shows the relationship between Vbb and noise, the important thing to take from this is that higher values of Vbb reduces nosie.

Table 3: Noise vs Vbb

Vbb	Mean noise (e^-)	ITHR	Threshold
0	4.985	111	50
3	2.343	111,6	62
6	1.918	112,3	60

6.4 Effect of VCASN and ITHR on threshold

Here is how the main DACs affect the threshold.

Table 4: Threshold for different VCASN. ITHR is constant at 50

Threshold				Noise	
mean	RMS	Pixels activated	VCASN	mean	RMS
463,5	12,06	35	95	3,05	1,15
438	26,68	1381	96	2,8	0,91
377,8	37,05	2495	97	2,72	0,91
307,8	32,77	2557	98	2,59	0,9
209,5	21,92	2559	100	2,37	0,87
88,42	10,19	2559	105	2,27	0,86
49,7	8,38	2559	110	2,45	0,81
26,94	6,76	2325	120	2,69	0,81

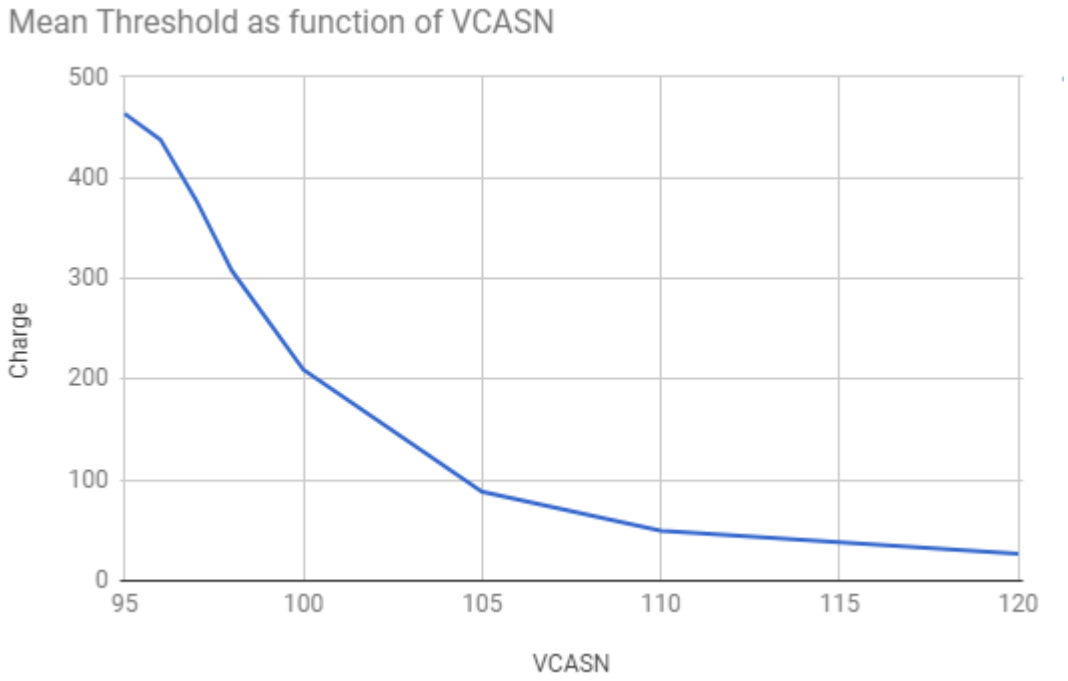

Figure 22: Threshold as charge vs VCASN

Table 5: Threshold for different ITHR. VCASN kept constant at 105

Threshold				Noise	
mean	RMS	Pixels activated	ITHR	mean	RMS
49,9	8,7	2558	30	2,25	0,81
69,24	9,42	2559	40	2,25	0,86
88,42	10,19	2559	50	2,27	0,86
107,3	11,19	2559	60	2,28	0,85
145,8	13,35	2559	80	2,39	0,84
184,9	15,85	2559	100	2,49	0,84

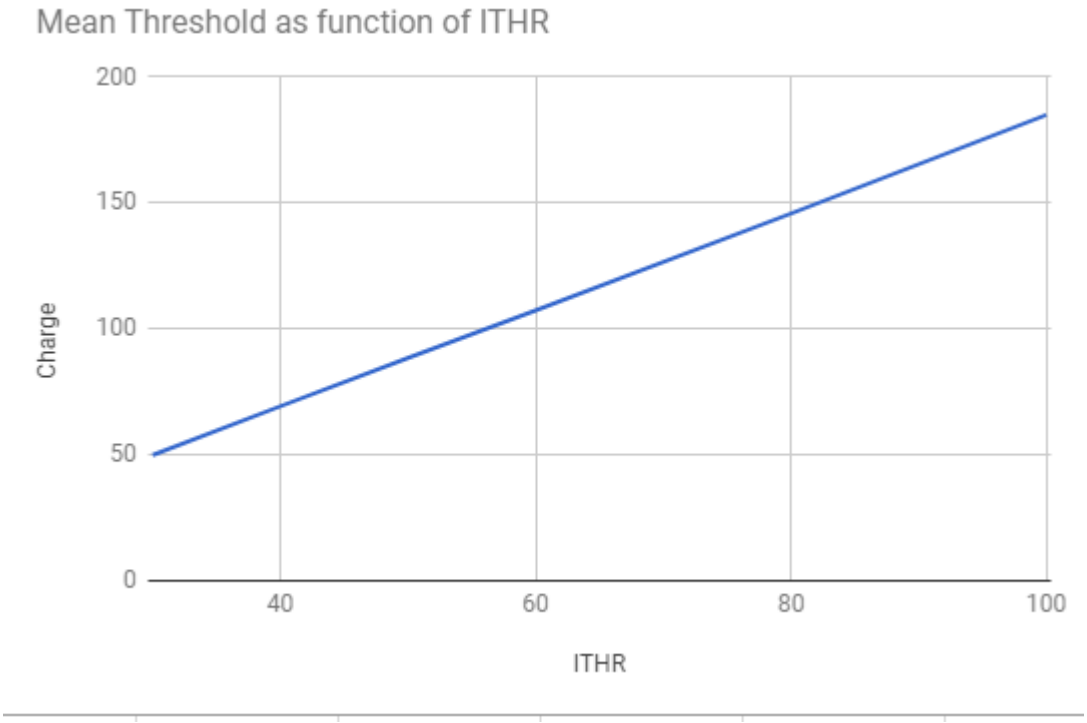

Figure 23: Threshold as charge vs ITHR

From this we can see that ITHR has a linear response to the DAC input value, and a large area of usable values. For this reason ITHR should be the value to change to adjust the threshold. Looking at VCASN it has a very small list of usable values, see figure 24, and a small change in VCASN makes huge changes in the threshold. For this reason alone it should be left at the recommended values and ITHR should be used to adjust the threshold.

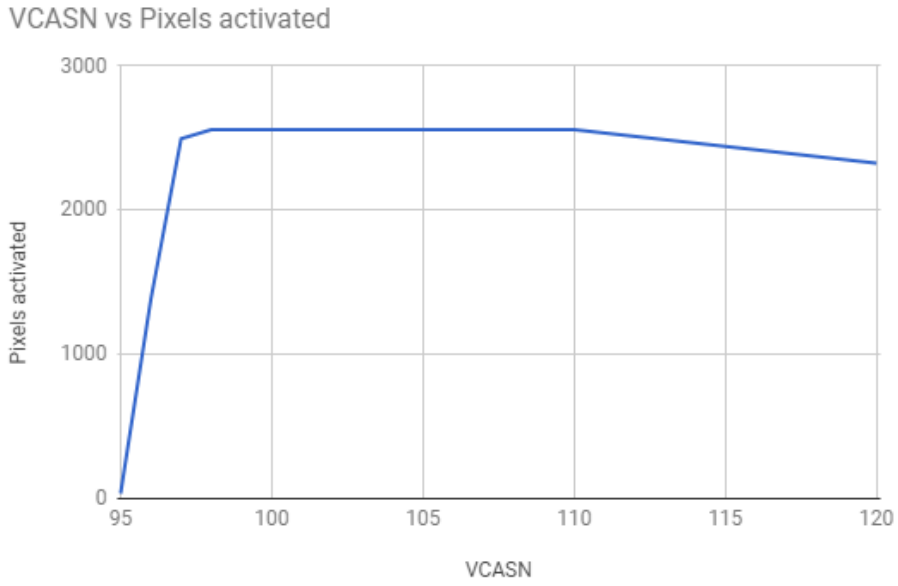

Figure 24: VCASN vs pixels activated. This corresponds to the usable values of VCASN, the recommended one being 105 for Vbb = 3V[16].

As can be seen in figure 24, The VCASN has a very small usable area. The graph shows how many pixels that was activated for a given value of VCASN. The number of pixels that should be activated in the test is the peak of the graph. The number being 2559 and not 524288, is because of not testing the whole chip. This shows how sensitive this value is as small changes can make pixels stop working.

6.5 Simulation of hits

There are to ways of simulating hits, analog and digital. The analog test makes a voltage drop in the detector diode similar to a particle hit, this is the same mechanism used by the threshold test only with a fixed voltage drop. As this is the only difference the subject of analog simulation will not be further explained here. The digital test sets the pixel register of a given pixel high and then reads it out. In figure 25 the output from the digitalscan test is shown. In this test every pixel is tested 50 times and a perfect chip should therefore give 50 hits for all pixels. Here this is not the case as can be seen from the column of pixels in blue. These pixels do not read back the full 50 hits and are therefore faulty. Since the error shows up here in the digital test it suggests that the fault is in the digital part of the chip, and is the same column that dose not give any hits in the threshold testing.

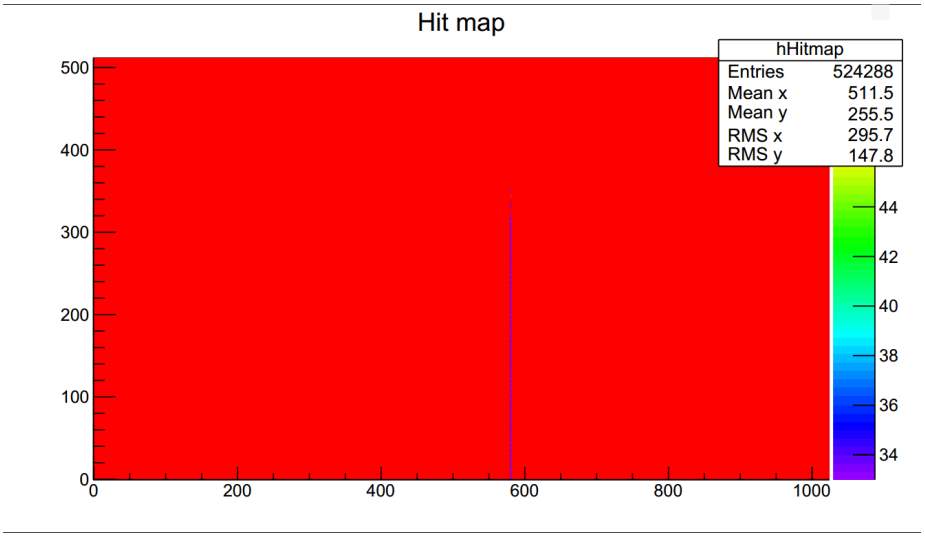

Figure 25: Digital simulation of hits

6.6 Noise results

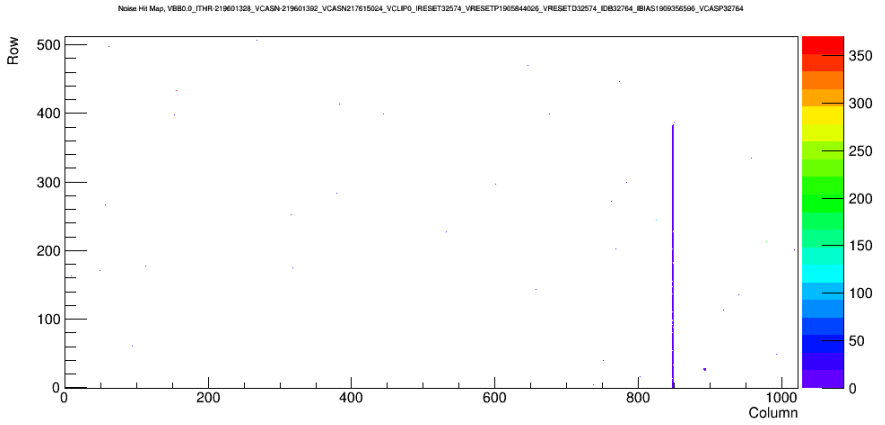

Figure 26: Noise scan of the ALPIDE. Threshold set very low to make it noisier.

The noise test seen in figure 26 is done at a very low threshold to make the noisy parts stand out in a shorter test. The numbers are therefore not representative of the chip noise but it shows which pixels or columns that are problematic but this can be found in appendix . This gives a good result and indicates which pixels need to be masked out for this specific chip.

6.7 Radiation testing

The radiation tests where run with a crude improvised setup of an anluminium stand and lead plates, but in the end they worked fine and produced expected and repeatable results. In all Particle tests the noisy double column shows up. It was intentionally left on, as it is possible to turn it of, to see the effects of radiation on it.

6.7.1 Alpha particle test

The alpha test gave the most surprising results. Where the alpha particle hit it produced a circular hit that looked like a doughnut, see figure 28. This did not happen with higher back bias which is something worth looking in to in the future. The doughnut shaped hit has been explained by trigger timing. It is called ECC (Empty Core Cluster) and happens because the charge in the pixels has dissipated before the trigger is sent. A close up of the doughnut hits can be seen in figure 28[19][18]. Figure 27shows a bitmap of the alpha test and is a good example of what hits look like from heavy charged particles.

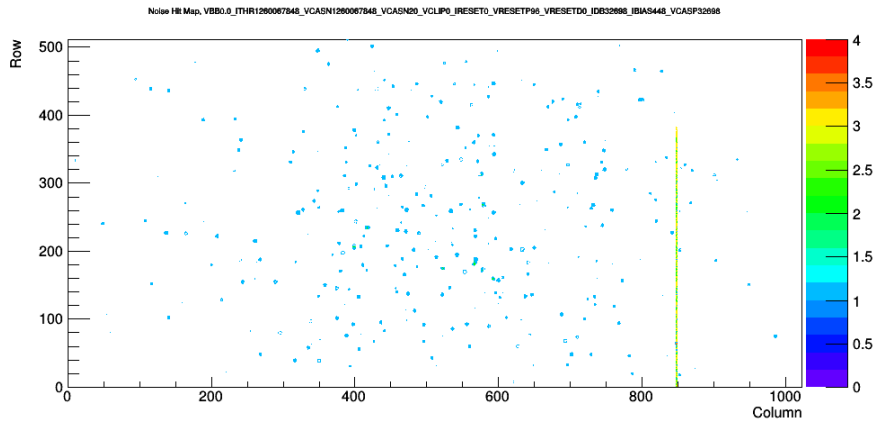

Figure 27: Bitmap of test with alpha source. am247

Figure 28: Example of the doughnut shaped hit.

6.7.2 X-ray test

This was just done because of curiosity of what the chip would give as output when exposed to X-rays. The results look like random noise on the chip.

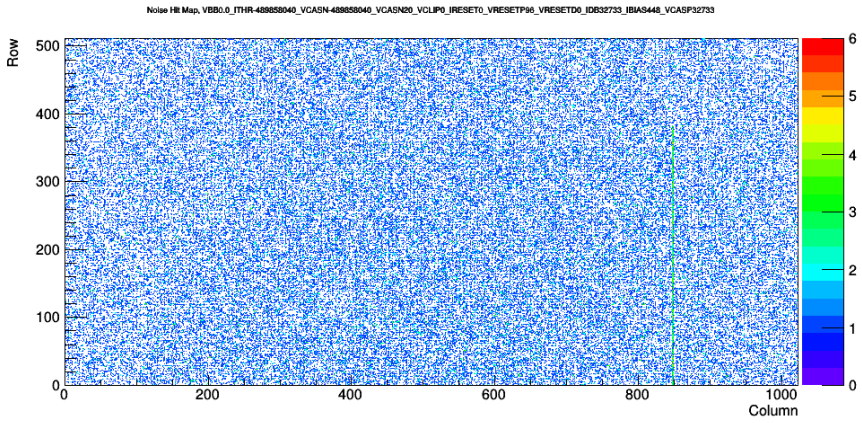

Figure 29: Test done with 5,9 KeV photons

6.7.3 Beta particle test

The beta particle test was done with a more active source and therefore produced more solid pictures compared to the alpha test in the exposure time used.

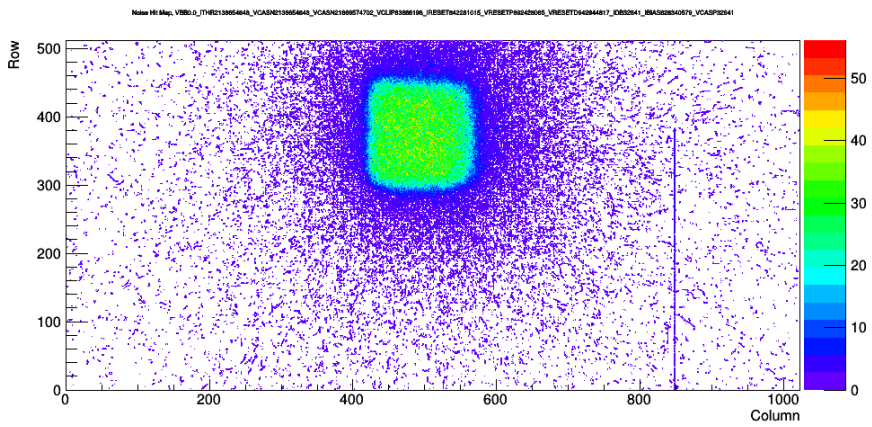

Figure 30: Bitmap of test with beta source.

This test was run for a longer time and with a lead shield with a square hole. This can easily be seen from the picture above. There seems to be a lot of scattering going on as pixels that are shielded gets hits as well. Some of the hits that seem to be around the square seems like particle tracks parallel to the chip plane. This can be caused by Bremsstrahlung, as that would explain the change in direction [7][17].

6.7.4 Proton test

The test do not include protons as there was no proton source available at the time of writing this.

6.8 Discussion

6.8.1 Errors in the output data

When the first tests of the ALPIDE where run, it responded fine to communication tests but the pixel tests did not work. The fifo test ran fine and the dac test ran, but showed us that one of the DACs were faulty. After further testing showed no signs of progress we went to CERN to get help with our test setup. It turns out that there were a fault in the firmware of the readout board which made the output to the computer full of errors. After reprogramming the DAQ board this error was gone. The faulty DAC was still a problem for our testing. Therefore we got a new ALPIDE and then proceeded to run the tests without more errors from the hardware.

6.8.2 The faulty double columns

There are two faulty double columns in this chip. They highlight different errors and the chip is most likely usable with these columns disabled. The error that

shows up during noise testing is false hits in double column 424 or columns 848 and 849 when looking at plots. The error that shows up in threshold and digital testing is different and since it does indeed show up in tests for the digital part of the pixel it suggests that the fault lies here or later in the signal path. As it is only the Priority encoder that sits between the pixel output and the RRU it suggests an error here. To strengthen this idea a fault in the priority encoder is likely as an entire, or most on one, double column can be affected by an error here. And it seems highly unlikely that so many individual pixel in the the same double column has errors. Because of this it would be a good idea to test for errors in the priority encoder, if this is possible, in the future.

7 Detector design ideas

7.1 Wanted specifications and requirements

At first there where no specifications given other than that the ALPIDE chip was to be used. As previously mentioned in chapter 2 the ALPIDE as planed used by CERN comes in two different stave configuration, inner barrel and outer barrel. After looking into which of these to use for the PCT purpose it was soon clear that the inner barrel one was the one needed for PCT.

A square detector is wanted that is 30-40 layer thick [17]. Assuming that we use the inner barrel staves from CERN, which are 9 chips long, this will require 18 staves as demonstrated later in this chapter. In this configuration each layer would end up with, as seen in the formula,

$$9\,\frac{chips}{stave} * 18\,\frac{staves}{layer} = 162\,\frac{chips}{layer} \tag{2}$$

162 chips. This is an important factor to consider when selecting the FPGA for the readout unit, as this FPGA will need to supply 162 LVDS lines for the data output. The following formula shows the total number of ALPIDEs needed for the detector assuming 40 layers.

$$162\,\frac{chips}{layer} * 40\,layers = 6480\,chips \tag{3}$$

As previously mentioned, one FPGA per layer is a requirement, this results in the need for a total of 40 FPGAs for the full detector. The further requirements for the FPGAs will be discussed in 7.3.

7.1.1 Proton flux and expected data rates

to determine buffer size and speed requirements for the readout unit it is important to know the proton flux in the detector. The proton flux is said to be 10^9 [17]. This will result in a per chip flux of:

$$\frac{10^9\,\frac{protons}{s}}{162\,chips} = 6,17 * 10^6\,\frac{protons}{chip * s} \tag{4}$$

To determine if this is possible we must consider the maximum flux the ALPIDEs can handle, which can be done with the following two equations, 5 for data long and 6 for data short:

$$1,2\frac{Gb}{s} * \frac{8}{30} = 3,2 * 10^8\frac{Pixel}{s} \tag{5}$$

$$1,2\frac{Gb}{s} * \frac{1}{20} = 0,6 * 10^8\frac{Pixel}{s} \tag{6}$$

One more consideration is necessary, and that is the fact that protons will activate more then one pixel each. As of writing this the only data available

is the alpha test, which shows that an alpha particle can activate 20-30 pixels. This gives the upper bound of:

$$6,17 * 10^6 \frac{protons}{chip * s} * 30 \frac{pixels\,activated}{proton} = 1,85 * 10^8 \frac{pixels\,activated}{chip * s} \quad (7)$$

As this is an estimate, lets call that half of available detection rate. Protons are of course smaller and have a charge of one e, not two and a mass of 1u, not 4u. This gives rise to the reasonable assumption that this number is most likely to big. Never the less it is smaller then the theoretical limit of the ALPIDE and therefore not of great concern. It should be noted though that if there is a lot of data short transmissions, the ALPIDE may be bandwidth starved.

Continuing with equation 7 to find the number of protons per strobe with the strobe frequency of 100kHz:

$$1,85 * 10^8 \frac{pixels\,activated}{chip * s} * 10^{-5} \frac{s}{strobe} = 1850 \frac{pixels\,activated}{chip * strobe} \quad (8)$$

This is 0,35% of the chips pixels and therefore there should not be a problem of samples overlapping.

7.2 Using existing staves from ALICE project

To save on developmental costs it is advisable to use the same staves that ALICE uses. The problem then reduces to making only the support structure for the staves and not the staves themselves. A more important point is that if the existing staves are used they already have a connector and PCB, and this PCB is very thin and will have minimal effect on the protons compared to other solutions. Since proton CT, as discussed previously, is a high flux, high data rate application the inner barrel module is the one that is needed. The reason for this is that only the inner barrel modules provide the high speed connection to all individual chips that is required for the high flux of protons.

7.3 FPGA

Going in to this with some previous knowledge about FPGA the first assumption was made that it was required to use trancievers to get the requierd speed. Going down that direction it was soon clear that only the biggest chips from the biggest manufacturers was going to do, and as it reqired several chips per detector layer it would become to expensive. After more datasheet reading the impressive 1,6 GHz LVDS specification stood out as a promising candidate. The LVDSs having this speed rating was unexpected but a welcome surprise. This meant that it would be possible to put an entire layer of the detector in to one chip. After further consultation with the professors this was chosen as the most promising solution.

Candidates from both Altera and Xilinx was considered. Given my previous bias towards Altera their Arria and Stratix series was what I looked into first.

This was later abandoned as Xilinx chips handle radiation better. The first proposed solution was 10 IB staves per FPGA, this was considered because the smallest Arria 10 (GX160[2]) could handle this, the assumption here being that no frame buffer was required or that the memory available on the FPGA was enough. The system evolved through a few versions, mostly guided by the capabilities of the FPGAs and the amount of staves one could support. After consultation with the professors it was decided to go for one FPGA per layer if possible and a square detector and with this the 18 stave per layer configuration was settled upon. Table 6 shows some of the immediate specifications that come from this decision.

Table 6: Table of requirements for FPGA

LVDS channels for ALPIDE	198	162 data, 18 ctrl, 18 clk
Pins for EEC DDR4 SDRAM	2*152	Dual channel
100G ethernet transceivers	4	
Minimum number of I/O needed	708	

From this and looking at the specifications of FPGAs it is clear that the Virtex Ultrascale or Ultrascale plus is the best choice. Since the main issue is number of I/O pins the recommended FPGAs become either the VU080 or VU5P[6].

7.4 Buffer/Memory

Looking for the best solution to temporarily store the data before transferring, it was clear form simple calculations that the memory had to be both fast and high capacity.

$$155\frac{Gb}{s} * 1s \Rightarrow 19,38GB \tag{9}$$

$$2133MHz * 64bit = 127\frac{Gb}{s} = 15,88\frac{GB}{s} \tag{10}$$

equation 9 shows the total amount of data from 1 s of full blast (this is only theoretical and is highly unlikely to every occur) and equaition 10 shows the bandwith of singel channel DDR4 at standard speed. From this we see that dual channel memory might be necessary and due to the possible amount of data is desirable anyway.

The highest capacity chips as of writing this are 256GB [5].

7.5 Transfer protocol

To get the data from the readout card to a computer some form of transfer protocol is needed. The first thing to consider is the amount of data to be transferred, the maximum acceptable transfer time if real time readout is not an option. Following is a list of more clarified assumptions:

- The maximum data rate if all data buses from all the ALPIDEs are saturated; 9 x 18 x 1,2Gb/s * 0,8 = 155,52Gb/s per layer. Bursts of this speed might have to be considered, but this is dependent on the proton flux.
- 40 layers will be a total data rate of 155,52Gb/s*40=6220,8Gb/s.
- Assuming a 10% occupancy this is still 622Gb/s.

7.5.1 Data format

To process the data after collection it is necessary to add an unique ID to each chip. The chips already have a chip ID, the board must then add a stave ID and board ID to the transmission. This is easiest done with a (board,stave,chip) coordinate system.

- 9 chips per stave requires 4 bits.
- 18 staves per layer requires 5 bits.
- 40 layers requires 6 bit.

for a total length of 15 bits.

This leaves room for a parity bit in the transmission if wanted. The chips already have a 4 bit ID value hardwired to them. The readout board must have addresses for the staves and add its own address value, or its ID, to the address value.

Table 7: Proposed data format for chip ID

	parity	Board address	stave address	chip address
value	0	000000	00000	0000
bit	0	15-10	9-5	4-1

As seen in table 7 the address or id of the chip can be easily decoded and can be assigned with minimum overhead. It is based on 16 bits, the reasoning for this being that transmissions is byte sized and therefore it is no point in not using a full transmission and 13 bits is needed to count all the chips anyway. The format is also easy to debug and read from just the binary value. The parity bit is a possibility to consider or this bit can be used for some other purpose if needed.

7.6 The detector Picutred

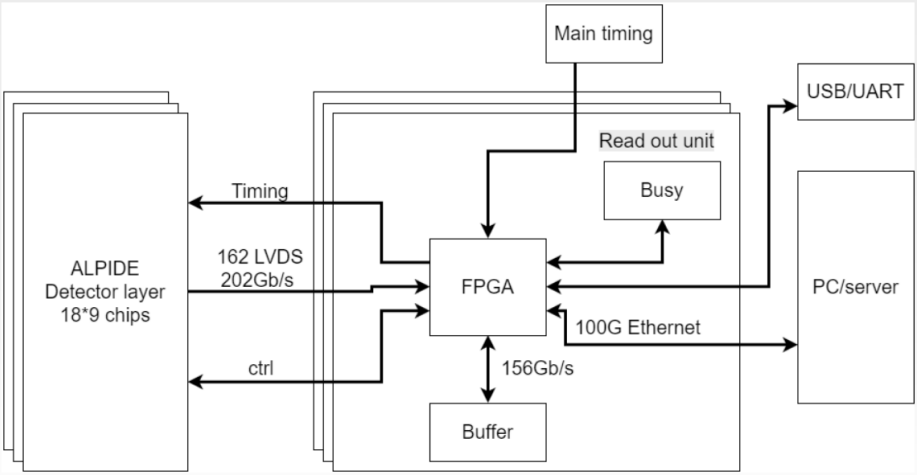

Figure 31: Sketch of the detector system

Figure 31 is a sketch of the system as envisioned.

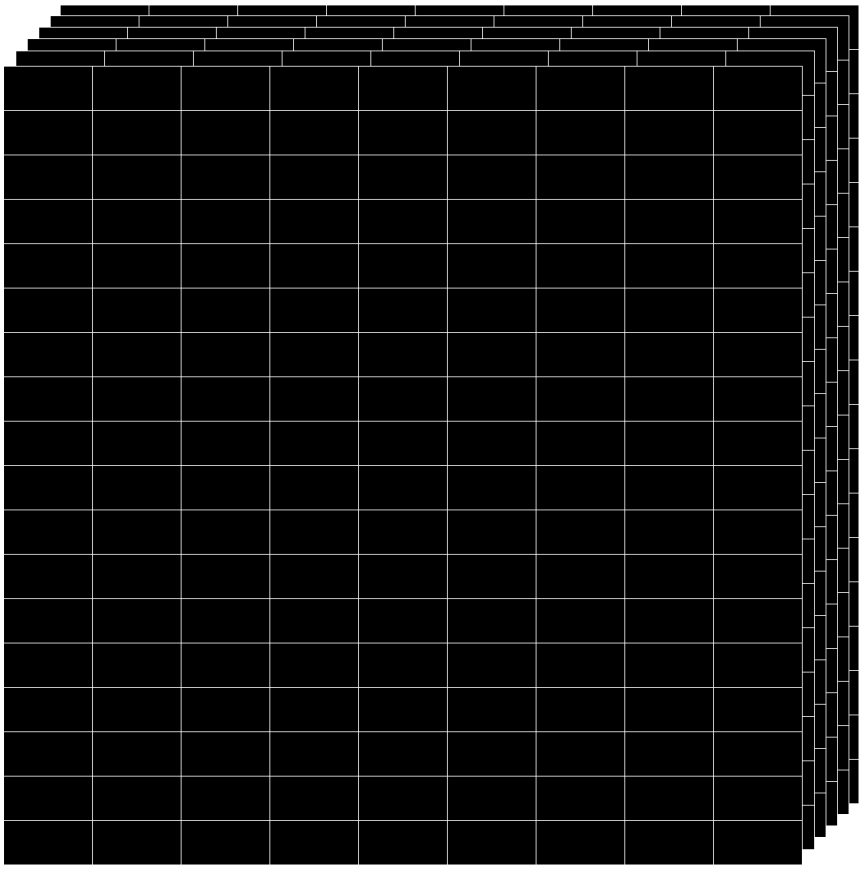

Figure 32: crude sketch of detector layers

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A Noise scan

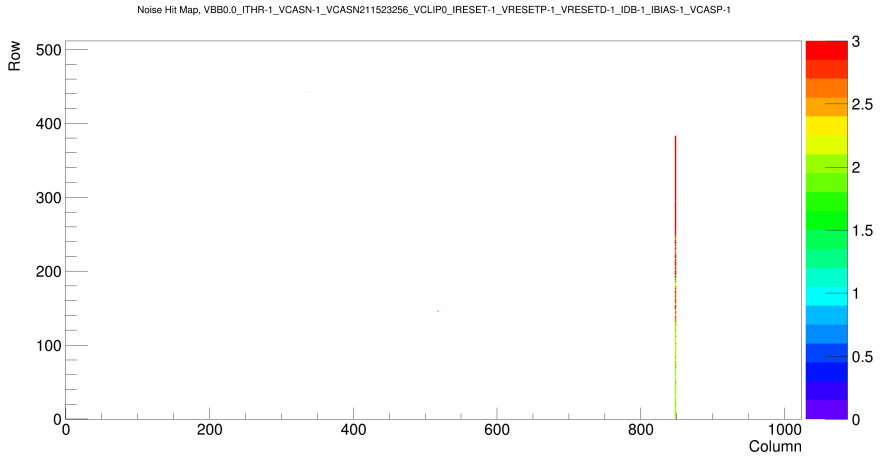

Figure 33: Noise scan

Figure 33 is a noise scan of the ALPIDE.