Design, implementation and testing of SRAM based neutron detectors

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Preface

The work of this thesis has been carried out within the Microelectronics and Nuclear Physics Research Group at the University of Bergen between May 2010 and May 2011.

I would like to thank my supervisors Kjetil Ullaland and Dieter Röhrich for guidance and support throughout the work of this thesis.

Further I would like to thank Eivind Larsen and Kristian Ytre-Hauge for great cooperation throughout this work.

A great thanks needs to go to Ketil Røed and Markus Brugger for letting us come and test together with them at PTB and CERF and for their guidance and support resulting in usable data.

A special thanks goes to Odd Harald Odland for support, and for letting us frequently use the cyclotron at HUS for testing of the equipment throughout this work. This has greatly contributed to the results. Thanks to Jan Salbu for assisting us on testing at the cyclotron at HUS.

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Abstract

Neutrons of thermal and high energies can change the value of a bit stored in a Static Random Access Memory (SRAM) memory chip. The effect is non destructive and linearly dependent on the amount of incoming particles, which makes it exploitable for use as a neutron detector. Detection is done by writing a known pattern to the memory and continuously reading it back checking for wrong values. As the SRAM memory is immune to gamma radiation it is ideal for use in for instance medical linear accelerators for detection of neutron dose to a patient.

The intention of this work has been twofold: (1) Testing of different SRAM devices of different bit-sizes, manufacturers, feature sizes and voltages for their sensitivity to neutrons of different energies from thermal to high energies. (2) Design and implement detector hardware, firmware and its accompanying readout system for successful use in irradiation testing.

The work has been done in close collaboration with Eivind Larsen, whose main contributions has been related to the nuclear physics aspect of the work in addition to arrangements in regard to beam setup and experimentation.

Testing have been done at the Physikalisch-Technische Bundesanstalt (PTB) facility in Braunschweig Germany in a quasi-monochromatic neutron beam of 5.8 MeV, 8.5 MeV and 14.8 MeV, finding a dependence of the sensitivity on the energy. In addition there have been testing conducted in the high energy hadron field at CERF at CERN, finding that by using the results from the other experiments an estimated range of the saturation cross section could be determined. Testing was also conducted at two occasions in the 29 MeV proton beam at Oslo Cyclotron Laboratory (OCL) in Oslo Norway, where it was found that the detector could be used as a reference detector for beam monitoring and for beam profile characterization. The cross sections of the detectors were found to be comparable to the 14.8 MeV cross section found at PTB. Thermal neutron testing of the devices was done in the thermal neutron field of the nuclear reactor at Institute for Energy Technology (IFE) at Kjeller Norway. All the devices were found to be sensitive to the field.

Detector electronics, adapted to the different devices, has been built which can withstand the same radiation as the memory device without malfunctioning. There has been a focus on using Commercial Off The Shelf (COTS) components for reducing the total cost of the detector to about 100–200$US. The use of COTS SRAM memory devices also simplifies the reproducibility and availability of spares.

The detector currently uses a two way communication between the detector and

the readout computer over two pair of cables reducing the amount of cabling needed for experiments. The detectors can be connected to the communication link in a bus fashion, currently enabling a total of 14 detectors to be tested simultaneously from 100 m away, over the same cable.

Single Event Latch-up (SEL) and problems with irregular count rate of SRAMs created in the 90 nm fabrication node has created problems during testing. Some solutions and techniques to mitigate these in hardware and firmware are presented in this work.

Contents

Acronyms

ADC	Analog to Digital Converter
API	Application Programming Interface
a.u.	Arbitrary Units
C-RAM	Chalcogenide RAM
CCD	Charge-Coupled Device
CERF	CERN-EU High Energy Reference Field
CERN	Conseil Européen pour la Recherche Nucléaire
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
DAQ	Data Acquisition
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
EEPROM	Electrically Erasable Programmable Read-Only Memory
EPROM	Electrically Programmable Read-Only Memory
FBGA	Fine-Pitch Ball Grid Array
FC	Faraday Cup
FIFO	First-In, First-Out
FPGA	Field Programmable Gate Array
FRAM	Ferroelectric RAM
GSI	Gesellschaft fur Schwerionenforschnung
HEH	High Energy Hadrons

IFE	Institute for Energy Technology
IGBT	Insulated Gate Bipolar Transistor
LED	Light-emitting diode
LET	Linear Energy Transfer
LHC	Large Hadron Collider
MBU	Multi-Bit Upset
MCU	Multi-Cell Upset
MOS	Metal Oxide Semiconductor
MRAM	Magnetoresistive RAM
NM	New Monitor
OCL	Oslo Cyclotron Laboratory
OSI	Open Systems Interconnection model
PCB	Printed Circuit Board
PCRAM	Phase-Change RAM
PIC	Precision Ionization Chamber
PLC	Precision Long Counter
p.o.t.	Particles On Target
PTB	Physikalisch-Technische Bundesanstalt
RadMon	Radiation Monitor
RAM	Random Access Memory
SDRAM	Synchronous DRAM
SEB	Single Event Burnout
SECDED	Single Error Correction, Double Error Detection
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture

SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SPS	Super Proton Synchrotron
SRAM	Static Random Access Memory
SSRAM	Synchronous SRAM
TFBC	Thin Film Breakdown Counter
TID	Total Ionized Dose
TMR	Triple Modular Redundancy
TQFP	Thin Quad Flat Pack
TSOP1	Thin Small-Outline Package 1
TSOP2	Thin Small-Outline Package 2
TSOP	Thin Small-Outline Package
USB	Universal Serial Bus
VFBGA	Very Fine-Pitch Ball Grid Array
VHDL	VHSIC Hardware Description Language

Chapter 1

Introduction

Ionizing radiation has an impact on everything around us. This also applies to electronics, where a single particle can cause the malfunction of a complete system by corrupting data or by altering functions. The problem is growing for every new generation of chips as the size of the integrated transistor is rapidly shrinking, reducing the charge needed from the incoming particle to affect the transistor's operation.

Electronic memory is vulnerable to Single Event Upsets (SEUs) which are caused by an ionizing particle depositing enough charge in the silicon to flip a bit in the memory from zero to one or from one to zero. The bit flips are non destructive and the data can be restored by rewriting the bit. The probability of an upset is random in time and it is linearly correlated with the amount of incoming particles. Knowing this, it is possible to make a radiation detector by writing a known pattern to the memory and continuously reading it back, checking for alterations from the original pattern.

Neutrons are not ionizing themselves, but have the ability to create secondary particles through nuclear interactions which are ionizing and which in turn can create SEUs in memory.

One of the many benefits of using electronic memory as a neutron detector is that they do not produce SEUs in response to gamma or beta radiation, which is often present in radiation environments where neutrons are present.Another benefit is that COTS memory can be bought cheaply, pushing the cost of a complete detector down to a 100–200$US.

1.1 Existing applications

Some neutron detectors based on COTS SRAM are already in use today for various applications. This section gives an example of two of the possible uses or these detectors.

1.1.1 RadMon Radiation Monitoring System for the LHC and the experimental caverns at CERN

In the Large Hadron Collider (LHC), a large amount of electronics is needed to control everything from bending magnets to cooling systems. In a harsh radiation environment like this, electronics will start to fail much more rapidly than it would under normal circumstances. Failing electronics can cause damage to other electronics when it breaks down which can lead to long unwanted beam stops needed to fix the damaged electronics. To combat this, nearly 300 RadMon radiation monitoring devices have been mounted on strategic places to give an early warning of when radiation levels have reached a critical level and the equipment needs to be exchanged. The RadMons are connected together in a network providing on-line measuring of the amount of radiation at any given time.

The RadMon is equipped with two Radfets for measurement of the Total Ionized Dose (TID), three PIN photodiodes for measurement of the 1 MeV neutron fluence and four 4 Mb SRAM devices for detection of SEUs caused by high energy hadrons above 20 MeV [1].

1.1.2 NEUTOR - Neutrons Monitor for Radiotherapy

During radiation treatment by the use of a medical linear accelerators (linacs), commonly used for treatment of cancer, the dose received from the secondary particles produced by the shaping of the beam can increase the risk of secondary tumors in the patient. The NEUTOR is a device that can actively monitor the neutron dose around the linac and is thus able to determine the neutron dose received by the patient. Due to the pulsed nature of the beam and the large amount of scattered photons, other forms of active neutron detectors are not suitable for use in this environment.

The NEUTOR is equipped with eight boards, each having 16 SRAM devices of 512 kb for a total of 64 Mb [2]. The SRAMs were particularly chosen for their higher content of ^{10}B, which have a large capture cross section for thermal neutrons.

1.2 Primary objective and main contributions

The main purpose of this thesis has been to investigate the applicability of various SRAM devices for use as an active neutron detector. For this to be done, the devices need to be tested in neutron beams at different energies where the flux of the beam is known for which the device can then be calibrated against. The sensitivity of the device for neutrons of a certain energy can then be found. This sensitivity is referred to as the single event upset cross section, σ_{SEU}. When the sensitivity of a device to a range of energies have been found, an energy dependent spectrum can be created. By knowing the radiation environment where the device should be used, the flux at the position of use can be determined.

To be able to test a wide range of SRAM devices during accelerated irradiation testing with high stability and predictability, an in situ electronic readout that can be adapted to all the different devices without much reconfiguration is needed. An in situ detector removes the uncertainty, due to packet loss or bad connections, which comes by the use of a communication link for direct readout of the memory. It also adds the possibility of using more than one memory device on the same detector, and testing more than one detector at the same time.

A focus in this thesis has been to use Commercial Off The Shelf (COTS) components, both for cost reasons and to make the detector easily reproducible. This enables the detector to be produced at the cost of one tenth of the price of other commercial neutron detectors.

For the detector to be characterized as an active detector, some form of readout communication and software is still needed. The readout software enables the user to monitor the amount of Single Event Upsets (SEUs) in real time and also any errors reported in addition to other information available from the detector.

All these aspects have been treated in this thesis, and the main contributions are listed below.

- Investigation into SRAM and other memory devices' applicability as a neutron detector is presented in chapter 3.
- Development of firmware and hardware for testing of nine different SRAM detectors is presented in chapter 4.
- Development of firmware and hardware for testing of two Synchronous DRAMs (SDRAMs) was completed in the early stages of development. Only minor testing was done on them with the cyclotron at Haukeland University Hospital where they were compared to three other SRAMs. Only one upset was detected on one of them compared to more than 1000 on each of the SRAMs and they were thus deemed not suitable. This development will not be further discussed in this thesis as the radiation environment at the cyclotron is not sufficiently known and a proper cross section could not be determined for the SDRAMs.
- Development of hardware, firmware and software for communicating with the detectors is presented in chapter 4.
- Accelerated beam testing at PTB in Braunschweig Germany in 5.8 MeV, 8.5 MeV and 14.8 MeV neutron beams. This is presented in section 6.1 and this part of the work was done in collaboration with Eivind Larsen [3].
- Testing in a high energy hadron field at the CERN-EU High Energy Reference Field (CERF) at CERN. The results are presented in section 6.3 and were done in collaboration with Eivind Larsen.
- Two accelerated beam tests at the OCL in a 29 MeV proton beam. The results are presented in section 6.2 and were done in collaboration with Eivind Larsen.

- Calibration and beam profiling for two ASIC tests at OCL in addition to repurposing of the detector hardware and development of new firmware for SEU in one of the ASICs. This will be further discussed by Magnus Lode Roscoe [4].
- Testing of the detectors in a thermal neutron field at the IFE at Kjeller. The results are presented in section 6.4 and were done in collaboration with Eivind Larsen.
- Testing the detectors ability to detect the neutron field in a linear accelerator (linac) at the Haukeland University Hospital. The linac produces secondary thermal and high energy neutrons when used with photon energies above 7 MeV to 8 MeV. This happens through interaction of the photons from the linac with the tungsten/lead collimators. The detectors were found to be sensitive to the field and the results will be further discussed by Eivind Larsen [3].
- Testing of the detectors applicability as a detector for the neutron dose in carbon ion treatment of cancer. This was done at GSI in Germany in a 400 MeV carbon beam on a human tissue equivalent phantom. The work was done in collaboration with Eivind Larsen and Kristian Ytre-Hauge. The results will be further discussed by Larsen [3].

1.3 Outline

This thesis is divided into seven chapters including the current one. In order to understand the behavior of electronics exposed to radiation, some knowledge is needed on how these effects occur. Chapter 2 gives a brief overview of the interaction of radiation with matter and continues with an introduction to the single event effects relevant to memory devices. As there currently are many memory devices available today that may be potentially used as radiation detectors, a look at what separates them from each other and how effective they could be as a radiation detector is needed. Chapter 3 reviews the functionality and behavior of mostly all the different types of memory devices commercially available today. An examination of their susceptibility to the different single event effects is included and is followed by a discussion on their applicability as a neutron detector. The second part of this thesis addresses the development of a neutron detector and the testing needed for calibration. Chapter 4 presents the design and implementation of a neutron detector. In chapter 5 the irradiation test setup is introduced for all the different test cites and setups, an added focus is given to the monitoring and calibration of the beam at each test cite. Chapter 6 presents the results for the irradiation tests and lastly the thesis is summarized and concluded in chapter 7.

Chapter 2

Radiation effects in semiconductor devices

Radiation effects are present in all types of electronic devices. As the industry moves to smaller feature sizes, lower voltages and higher densities, these problems will probably escalate. This chapter presents some of the more common radiation effects in electronics and how they effect memory based electronics. The information is mostly based on Knoll [5] and Nicolaidis [6] if not otherwise noted.

2.1 Radiation interaction with matter

To be able to detect or measure any type of radiation, we need to make it interact with matter in some way and then analyze the resulting change in the matter's properties. As all particles carry some energy with them, either in the form of charge or momentum, they are capable of interacting with matter in the form of particle interactions.

We distinguish between two main groups of particle interactions, charged particle interactions and neutral particle interactions. Alpha particles, beta particles, heavy ions and protons are charged particles while neutrons and photons (gamma rays, X-rays) are neutral.

We also differentiate between ionizing and non-ionizing radiation. Ionization is the process of removing an electron from an atom resulting in charged particles, a negatively charged electron and a positively charged ion. For this effect to occur the particle hitting the atom needs to have an energy above the electrons binding energy, typically a few eV. Non-ionizing particles are thus particles that don't have enough energy to displace these electrons.

2.1.1 Interaction of charged particles with matter

Charged particles can be divided between heavy and light charged particles. Ions, protons and alpha particles are considered heavy charged particles, while beta particles are considered light.

Charged particles moving through a material mainly interacts with the negative electrons through the Coulomb forces. As a result they continuously lose energy through

each interaction and will finally stop after tens of thousands of collisions.

Beta particles which are three orders of magnitude lighter than a proton, may lose all their energy in a single collision with an atomic electron as it involves a collision between two particles of the same mass. They may also scatter to large angles and end up with a zig-zag trajectory. In contrast to heavy charged particles which lose a small amount of energy in each collision and end up with a more or less straight trajectory.

Charged particles can interact with the nuclei of the target material leading to the particle being deflected through elastic scattering or fragmented through inelastic scattering. Depending on the target material and projectile energy, the secondary fragment created can be a proton, neutron or a heavier particle.

The rate at which a charged particle moving through matter lose energy is generally referred to as the *stopping power* of the material. It is defined as the amount of energy lost per unit length of the material being transversed and is given in MeV/cm. Charged particles can have either nuclear or Coulomb interactions and the total stopping power is then the sum of these.

$$S_{total} = -\frac{\mathrm{d}E}{\mathrm{d}x} \tag{2.1a}$$

$$-\frac{\mathrm{d}E}{\mathrm{d}x} = S_{col} + S_{nuc} \tag{2.1b}$$

The amount of energy absorbed by the matter through Coulomb interactions is referred to as the Linear Energy Transfer (LET) and is equivalent to the stopping power of Coulomb interactions but with an opposite sign. The LET is usually denoted in respect to the density (ρ) of the material being traversed and is so given in MeV/mg/cm^2.

The stopping power is described by the *Bethe formula*, see for instance [5].

$$-\frac{\mathrm{d}E}{\mathrm{d}x} = \frac{4\pi e^4 z^2}{m_0 v^2} NB \tag{2.2}$$

where

$$B = Z\left[\ln\frac{2m_0v^2}{I} - \ln\left(1-\frac{v^2}{c^2}\right) - \frac{v^2}{c^2}\right] \tag{2.3}$$

Symbol	Definition
e	Electron charge
z	Charge of primary particle
m_0	Electron rest mass
v	Velocity of primary particle
N	Number density of target material
Z	Atomic number of target material
I	Mean excitation potential for the target material
c	Speed of light

As long as the primary particle is non-relativistic ($v \ll c$) only the first term in B is significant. It can then be seen that the stopping power for a given non-relativistic particle varies with $1/v^2$, or inversely with the particle energy. For different particles of the same velocity the stopping power is mainly depended on z^2, which means heavier particles, like an alpha, will lose energy at a greater rate than for instance a proton.

As a charged particle nears the end of its track it starts interacting more with the surrounding matter and will start to lose energy faster, resulting in a maximum energy loss at the end of the track. This is illustrated by the *Bragg curve* in figure 2.1 showing the specific energy loss of a charged particle traversing a matter. The peak of the energy loss is referred to as the *Bragg peak*. After the Bragg peak the energy loss of the particle falls off sharply due to electron pickup.

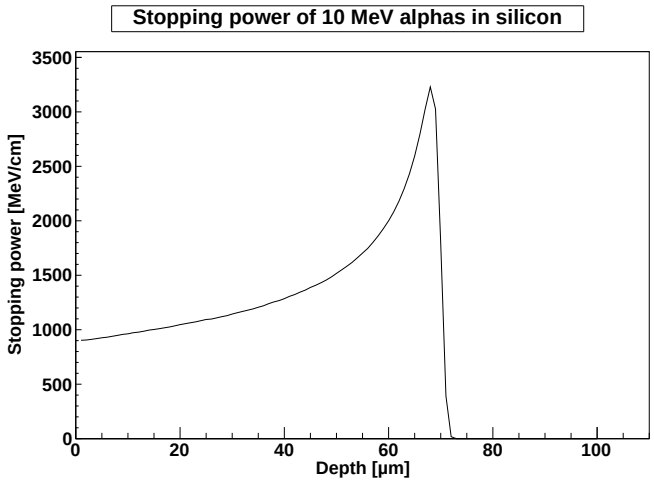


Figure 2.1: *As an example of the Bragg curve, the stopping power of 10 MeV alphas in ^{28}Si is shown here as simulated by the SRIM code [7].*

2.1.2 Interaction of neutral particles with matter

Two types of neutral particles are neutrons and photons. As none of them have any charge they do not interact with the Coulomb force.

Interaction of photons with matter

Photons, which can be gamma rays, X-rays, UV etc., are an example of electromagnetic radiation. They travel at the speed of light and have zero rest mass and charge. They interact with matter mainly in three ways: photo electric absorption, Compton scattering and pair production. In photo electric absorption the photon interacts and gets absorbed by an atom which emits an energetic photo-electron from one of its bound shells. In Compton scattering the photon interacts with a weakly bound electron in the absorbing material. In the process the photon direction is deflected and some of its energy is

transfered to the electron. In pair production the energy of the photon is absorbed and used to create an electron-positron pair.

Interaction of neutrons with matter

Neutrons interact with nuclei only through the strong nuclear force. For this to happen the neutron has to pass very close to the nucleus and since the distance between the nuclei in normal dense matter is large, the neutron has a deep penetration depth in matter. The ways the neutron interacts with the nuclei can be divided into scattering and absorption as seen in figure 2.2. In scattering reactions the neutron interacts with the nucleus, but both particles reappear after the reaction though with a different direction and energy. In absorption the neutron disappears, but one or more heavy charged particles will appear after the reaction. The total probability that a reaction will occur is depends on the cross section, σ_t.The cross section is strongly depended upon the energy of the neutron and the atomic number of the target nucleus.

Neutrons can be classified according to their energy and for our practical purpose can be divided into thermal neutrons and fast neutrons. Thermal neutrons have an energy below 0.5 eV which also is the energy of which an abrupt drop can be seen in the cross section of cadmium (the cadmium cutoff energy). This property can be utilized to differentiate between thermal and fast neutrons in neutron detection. Due to the small kinetic energy of thermal neutrons, they lose and gain only minor amounts of energy through elastic scattering with the nucleus, but will eventually get absorbed. Fast neutrons have higher energy and can deposit more energy in each interaction with the nucleus.

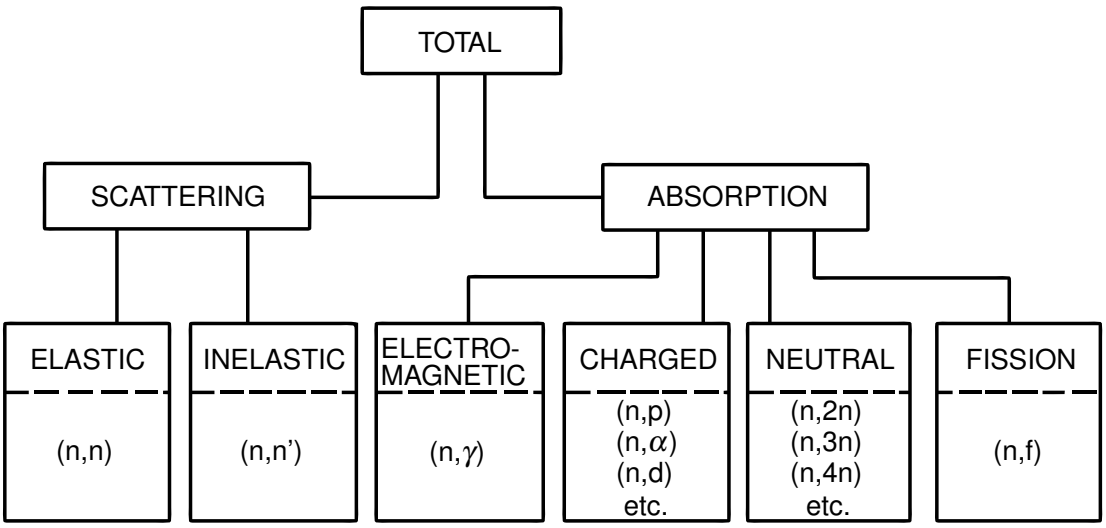


Figure 2.2: *Overview of different neutron interactions. The letters separated by commas in the parentheses show the incoming and outgoing particle [8].*

2.2 The influence of radiation on semiconductor devices

Radiation effects experienced in semiconductor devices can range from displacement of atoms in the structure to corruption of stored data due to charge injection. The different effects are usually classified into two groups, cumulative effects and single-event effects.

2.2.1 Cumulative effects

Cumulative effects are potentially destructive effects that are caused by accumulated dose over time.

Displacement Damage

Displacement damage is the result of nuclear reactions, typically scattering, that can cause changes in the semiconductor lattice altering the crystal's electrical characteristics. Any incident particle or photon capable of imparting an energy of about 25 eV to a silicon atom can dislodge it from the lattice site [9]. The displacement damage is usually measured in neutrons/cm^2, the same as for the neutron fluence.

Total Ionizing Dose

Total Ionizing Dose is the dose accumulated by the device due to ionizing radiation over time and is measured in *Grays* (Gy).As the ionizing particle is creating electron-hole pairs, there is a probability that the electrons and holes will not recombine in the presence of a field due to the slow movement of the holes. This can cause the holes to be trapped in the oxide or the oxide-silicon interface creating a net positive charge.

2.2.2 Single Event Effects

Single Event Effects (SEE) group all effects caused by interaction of a single particle with an electronic component. These effects are usually again grouped into *soft* and *hard* errors. Soft errors are effects that causes some form of corruption of a stored element or glitches in the device's operation. They are non destructive and can be corrected be rewriting the affected element with a correct value, resetting or power cycling the device. These errors concern SEU, Multi-Bit Upset (MBU), Multi-Cell Upset (MCU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI) and SEL.

Hard errors are destructive errors that are non-recoverable. These can be Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR) in power MOS devices, IGBT or power bipolar transistors. These effects are only seen in high voltage/current devices and are not applicable to memory devices.

Single event effects are measured by a cross section. This is analogous to the nuclear cross section and is measured in cm^2. It is given by

$$\sigma = \frac{\text{No. of SEE}}{\varphi \cdot \text{s}} = \frac{\text{No. of SEE}}{\Phi} \tag{2.4}$$

Where σ is the Single Event Upset (SEU) cross section, φ is the flux in number of particles per square cm per second and Φ is the fluence which is the integrated flux.

Single Event Effects (SEE) manifest themselves in different ways in different devices and will therefore be further discussed in chapter 3 for each respective device. This part will give an introduction to the subject.

Single Event Upsets

A Single Event Upset (SEU) occurs when an ionizing particle hits the sensitive area of a storage cell, changing its electrical state and causing the wrong value being presented when the cell is read back. A rewriting of the value will return the storage cell to the correct state. A SEU can occur in any device containing latches or other storage cells.

An increase in SEUs can be seen over time for a device in a radiation environment due to increased TID creating leakage currents lowering the required charge to upset the node [10].

SEUs can experimentally be studied by writing a known pattern to the storage cells and continuously reading the pattern back during irradiation to look for changes.

Multi Bit Upsets/Multi Cell Upsets

When an ionizing particle causes more than one bit flip to occur, it is referred to as a Multi-Cell Upset (MCU). If the bit flips occur in a single word it is referred to as a Multi-Bit Upset (MBU). Multiple errors can occur if a particle crosses between two sensitive zones of different cells or if the free carriers from the ionizing strike can be collected by different junctions of transistors. The amount of multiple upsets increases with more lateral angles of the impinging ionizing particle and is the lowest at a 90° angle from the plane [11].

In resent devices the words are interleaved, ensuring that cells belonging to the same word are physically apart and in so reducing the possibility of a MBUs occurring [12].

If the cell layout of a device is not known it can be hard to determine if two upsets detected are an MCU or two separate SEUs. But if the flux is relatively low and the readout speed is high the probability of two ionizing particles hitting within the specified time-window is low.

$$P(MCU/MBU) = (T_{readout} \cdot \varphi \cdot \sigma \cdot \text{No. of bits})^2 \tag{2.5}$$

Where $T_{readout}$ is the time to read through a whole device, φ is the particle flux and σ is the cross section per bit.

Single Event Transients

Single Event Transients (SETs) are momentary voltage or current pulses created from an ionizing particle disturbing combinational logic. An SET may propagate from the output of a gate throughout the circuit and can in the end cause an SEU. For this to happen some criteria must be met [6].

- The particle strike must generate a transient capable of propagating through a circuit.
- There must be an open logic path through which the SET can propagate to reach the latch or memory element.
- The SET must have a sufficient amplitude and duration to change the state of the latch or memory element.
- Depending on the operation of the device, the SET must arrive at the latch during the latching edge of the clock for a synchronous device, or during a read or write command for an asynchronous device.

The probability of an upset increases linearly with the clock or access frequency of the device as the time between the time-windows for latching of data decreases.

Determining if a device is suffering from SET effects in a device containing memory elements can be hard as it will be difficult to separate them from regular SEUs, but if the device is seen to have an increased SEU rate at higher frequencies this could indicate the presence of a SET effect.

Single Event Latchups

SELs are originating from the interaction of an ionizing particle with a parasitic PNP and NPN transistor structure in bulk CMOS. As seen in figure 2.3, they are combined into a PNPN thyristor structure where if a large enough current is induced in to the circuit to turn on the thyristor, it will remain on until the power is cycled. The point where the thyristor starts to turn on is referred to as the knee point, the voltage to keep the thyristor turned on is called the holding voltage as illustrated in figure 2.4. The ion can strike at any position in the structure, including regions far away from I/O terminals which are normally immune to electrical induced latchups [13]. The effectiveness of the heavy ion to create a SEL depends on the position of the strike in the n-well.

Triggering of the SEL can be separated into four steps [13]:

1. A transient current is induced by a heavy ion within the well-substrate junction. This current flows from the well contact to the substrate contact and produces a voltage drop within the well. The voltage drop depends on the distance from the strike to the well contact and a strike closer to the well contact will produce a smaller voltage drop and will not induce a SEL.

2. If the voltage drop is sufficiently large the vertical transistor (Q1) will be forward biased, producing a much larger current which will flow from the emitter of the vertical transistor to the substrate.

3. A voltage drop in the substrate from the higher current in step 2 will forward bias the lateral transistor (Q2) causing it to turn on as well starting the regenerative process.

4. The regenerative condition causes both transistors to saturate and allows the structure to remain latched after the triggering occurred.

The Vdd supply voltage needed for the holding voltage is the sum of the three forward voltage of the PNPN structure, where the middle one is reverse biased, plus the voltage over the substrate/well resistor. This would amount to about 1.0 V to 1.5 V, but it implies that the two transistors are in saturation, which is not always the case. One transistor in active mode will increase the absolute value of the reverse biased junction giving a higher holding voltage.

By lowering the main supply voltage for the device it is possible to reduce the probability of an SEL occurring [14]. As the device supply voltage gets lower for newer devices, SEL will eventually disappear.

A SEL is commonly accompanied by a SEU, but it might also trigger SEUs in several bit-arrays. This is believed to be because a short circuit between the Vdd contact or the p-source occurs so that the Vdd line in a large region of the chip is brought down below the voltage needed to retain the memory content [10].

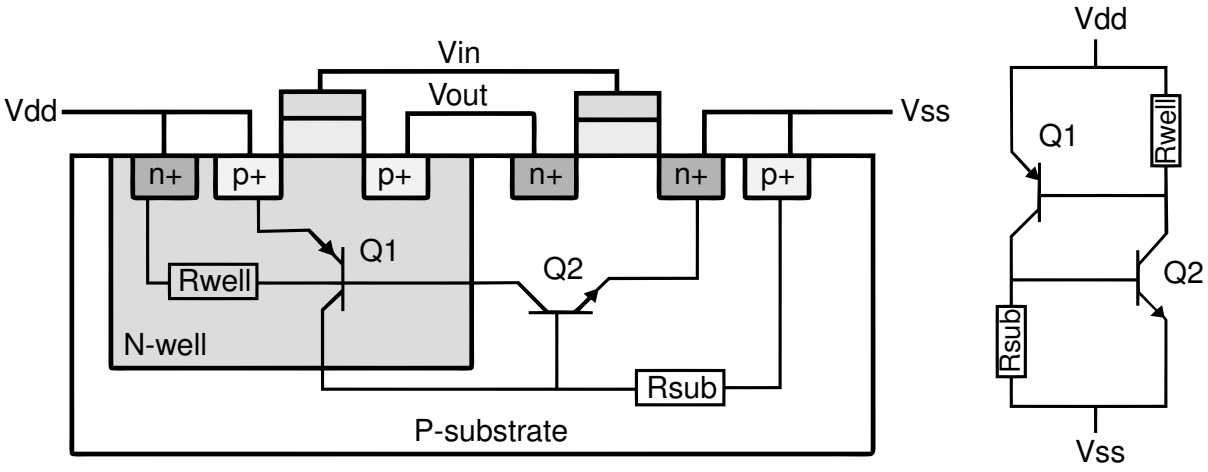


Figure 2.3: *PNPN parasitic structure in an N-well bulk CMOS inverter structure [6].*

Single Event Functional Interrupts

A Single Event Functional Interrupt (SEFI) is the result of a SEU or SET creating an upset that alters the operation of the device. This is usually present in more advanced

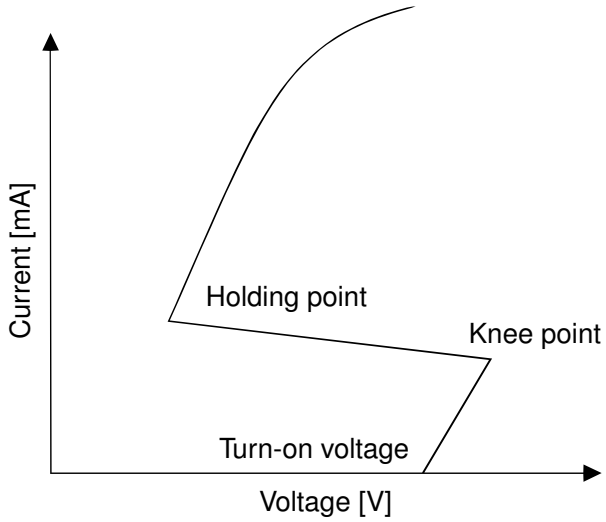


Figure 2.4: *The latchup I-V characteristic [15].*

devices where an upset can make the device go into reset, change into a test mode or other mode that alters the device's functionality.

To experimentally detect SEFI it is possible to continuously run an operation on the device that creates a predictable output and then look for alterations in the output and restarting the device if an error occurs. An error from a SEFI can usually be distinguished from a SEL by monitoring the current of the device during the experiment. An abrupt increase in current indicates a SEL.

Chapter 3

Memory based semiconductor devices

Different techniques exists for storing a bit in a CMOS structure. The most common today are flash, SRAM, DRAM and EEPROM, but new technologies like PCRAM, FRAM and MRAM are emerging. This chapter gives an overview of the different technologies and their SEE susceptibility and applicability as a neutron detector.

3.1 Static RAM

A SRAM cell has the ability to store one bit in a latched structure created by two inverters in a loop. The data does not need to be refreshed and is retained as long as the power is retained, if the power is lost the data will be corrupted. This is referred to as the device being *volatile*.

The cell structure can be built from either four transistors or six transistors, referred to as 4T and 6T cells, see figure 3.1 for example of a 6T cell. The 4T cell uses two poly-silicon resistors in the giga-ohm range for pull-up instead of the two p-type transistors. The advantage of using a 4T structure is the lower area consumption, but it has the disadvantage of having a higher power consumption due to the current constantly flowing through the pull-up resistors. The devices used in this thesis contain only 6T cells.

To read from the 6T cell both the bit (B) and $\overline{\text{bit}}$ ($\overline{\text{B}}$) line must be pre-charged to a high value. The wordline (W) is then pulled high enabling the access transistors (N3 and N4) causing the bit line connected with the node of the cell having 0 volt to be pulled low. A sense amplifier detects the voltage change and propagates the value to the outside.

Writing to the cell is done by forcing a high on one bit line and a low on the other while enabling the wordline overpowering the p-type transistor and changing the state of the cell.

SRAMs come in different configuration, there is asynchronous, synchronous, special types and non-volatile.

- The asynchronous is managed by three control signals. Chip enable (CE) or chip select (CS) selects or de-selects a chip. When the chip is de-selected it sets the

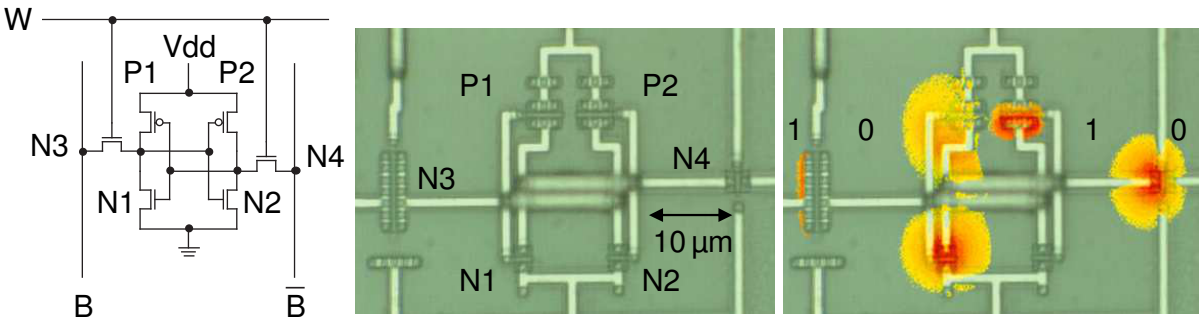


Figure 3.1: *Image on left shows a standard 6T SRAM cell [16]. Center shows the same cell laid out in a 0.8 µm AMS BiCMOS technology, the spacing between transistors are exaggerated for testing purposes. Image on right shows the sensitive areas as mapped by a pulsed laser with energy from 10 pJ to 1193 pJ, darker color indicates higher sensitivity [17].*

output pins in high impedance and stops responding to input signals. The write enable (WE) pin enables writing to the device. The output enable (OE) pin enables outputting of data from the selected address. As there is no clock source to control the device, a constant minimum-delay is needed between each command to the device. Typical speeds are from 10 MHz to 100 MHz.

- The synchronous device (SSRAM) has its read and write cycles synchronized with a clock from the readout device, this enables it to work with high-speed devices, typically hundreds of MHz.

- Special SRAMs are First-In, First-Out (FIFO) or serial SRAM, where the addressing is controlled by the SRAM itself, and dual-port SRAM which provide the ability to write and read from the device at the same time by an extra set of access transistors.

- Non-volatile SRAM either contain a battery for retaining memory or it uses flash memory in parallel with the SRAM memory.

The special SRAMs and the battery backed SRAMs share much of the same principal architecture as the asynchronous or synchronous SRAM.

3.1.1 SEU susceptibility

To flip a bit in an SRAM, the ionizing particle needs to strike either the drain region of the NMOS or PMOS transistor which currently is in the off position. This can be seen in figure 3.1 where the drain of N1 and P2 have a high sensitivity. The access transistor N4 can also be seen to have some sensitivity as it is reverse biased in this case.

Because of the higher mobility of electrons than holes, and since the PMOS transistor is created weaker than its complimentary NMOS transistor, a strike in the drain of

the NMOS transistor will have a higher probability of creating a SEU than if it would hit the PMOS.

The strike on one of the critical nodes will create a transient, which if it reaches the other inverter and has enough charge to turn on the appropriate transistor will lock the new value and the bit will be flipped.

3.1.2 Critical charge

The critical charge needed to flip a bit is depended on the size of the critical node, the voltage of the cell and the feedback time of the cell. This is formulated in the simple model first proposed by Roche et al. [18]

$$Q_{crit} = C_N \cdot VDD + I_{DP} \cdot T_F \tag{3.1}$$

Where C_N is the node capacitance, VDD is the supply voltage, I_{DP} is the max PMOS drain conduction current and T_F is the flipping time of the cell.

From this one can see that lowering the voltage of the device will lower deposited charge needed to be generated from the incoming ion and thus increasing the SEU susceptibility. Moving to a smaller feature size will also increase the SEU susceptibility as it will reduce the size of the node capacitance, but the sensitive area will also be somewhat smaller which counteracts it. Both effects have been found experimentally, see for instance Flament et al. [19].

When reaching certain levels of critical charge new ionizing secondary particles that before had too little initial energy to upset a node can now displace enough energy to flip the bit. This creates a jump in the SEU sensitivity compared to a similar device in the previous feature size. But in recent technologies, the fraction of the effective interactions reaches 90 % and only small changes will be seen in the future [6].

3.1.3 SEFI susceptibility

Asynchronous SRAMs do not normally suffer from SEFIs as there is little control logic embedded in the device. But an upset in the sense amplifiers or the address decoders might enable the readout of a wrong value or the wrong address. This can be avoided by reading out three times from the same address and doing a majority vote on the read data.

Synchronous SRAMs might suffer from other SEFI as it uses registers to store the address and other control bits. An upset in one of these registers might create a wrong value being read.

3.2 Dynamic RAM and Synchronous Dynamic RAM

The Dynamic Random Access Memory (DRAM) stores a bit as a charge on a capacitor. An access transistor is connected to the capacitor and isolates it from the rest of the

Feature size	SRAM property		
	Normalized cell area	Density	Normalized Q_{crit}
[nm]	[a.u.]	[Mb]	[a.u.]
250	7.45	4	12.8
180	3.84	8	6.4
130	2.01	16	3.2
90	1.00	32	1.6
65	0.49	64	0.8
45	0.24	128	0.4
32	0.12	256	0.2
22	0.06	512	0.1

Table 3.1: *Assumed roadmap of scaling in SRAM [20]. The size of a cell in 130nm, 90nm and 65nm is on average 2μm^2, 1μm^2 and 0.5μm^2 respectively [21] and the critical charge of a 90nm has been found from simulation to be 1.4fC [22] so the numbers are within range.*

circuitry as seen in figure 3.2. When the capacitor is not read or written from, this charge will leak off the capacitor due to the sub-threshold leakage current in the access transistor. This causes a need for the cell to be rewritten many times per second.

To read from the cell the bit line is precharged to VDD/2 and when the word line is enabled the charge stored on the capacitor is shared with the bit line causing a change in voltage on the bit line which can be detected by a sense amplifier. A read disturbs the content of the cell and thus it needs to be rewritten after every read.

To write to the cell, the desired value is force on the bit line while the word line is enabled, effectively charging or discharging the capacitor to the new value.

Due to the fewer number of transistors compared to the SRAM, a smaller area is needed per cell. The smaller area enables higher bit density per device and thus is more economic to use when high densities are required, even though the DRAM is inherently slower than SRAM due to the constant need for refreshing.

The Synchronous DRAM (SDRAM) differentiates it self from the DRAM by being a synchronous device, meaning the read and write from the device is synchronized to a clock. The SDRAM also contains all the circuitry needed to refresh a cell inside the device so that only a command is needed to tell it to refresh all the cells.

Other types of DRAM exists, but they mostly inherit their properties from SDRAM and mostly differ in the communication with the readout device.

3.2.1 SEU susceptibility

The primary cause of SEUs in DRAM is due to cell discharge from an ionizing particle. Any disruption of the charge on the device will be latent until a refresh is performed on the cell. To flip the bit, the ionizing particle does not need to fully deplete the capacitor, only enough to lower the charge below the noise margin of the sense amplifier.

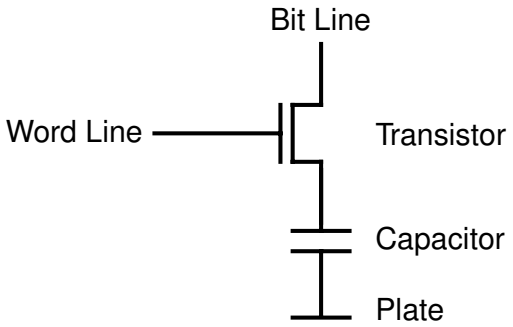


Figure 3.2: *Schematic drawing of 1T DRAM cell [16].*

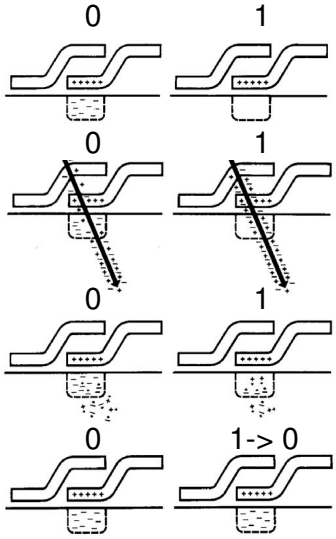


Figure 3.3: *An alpha particle hitting a DRAM can primarily flip a bit from 1 to 0 [23].*

Another upset possibility is if the ionizing particle hits the bit line during a read when the bit line is precharged.

3.2.2 Critical charge

The charge needed to upset a cell is constantly changing due to the leakage, but can generally be expressed as

$$Q_{crit} = C_{cell} \cdot (V_c - V_b) \tag{3.2}$$

Where C_{cell} is the capacitance of the cell, V_c is the voltage currently on the capacitor and V_b is the level at which the bit line is precharged to when reading, usually Vdd/2. V_b can at most be Vdd.

Mueller et al. [24] set the cell voltage at 1.4 V and the cell capacitance to 30 fF for a 90 nm device. This gives a Q_{crit} of 21 fC, an order of magnitude higher than the 1.4 fC for a 90 nm SRAM reported by Naseer et al. [22].

3.2.3 SEFI susceptibility

The SDRAM has both mode registers, address registers and refresh counters embedded, and a SEU in any of these will create a SEFI. There are different results from a SEFI in a SDRAM, hitting the address register might create a read or write to a wrong row or column. A hit in the mode register might put the device into a test mode, preventing read and write until the correct mode is rewritten. A hit in the refresh counter or other places in the mode register might create a SEFI where the device needs to be power cycled to work again.

3.3 Ferroelectric RAM

Ferroelectric RAM (FRAM) is similar in construction with the DRAM but uses a ferroelectric layer instead of a dielectric layer in the capacitor to provide non-volatile storage. There is no leakage from the capacitor and hence it doesn't need to be refreshed. A ferromagnetic material has a nonlinear relationship between the applied electric field and the apparent stored charge which results in a hysteresis curve. When an external electric field is applied over the capacitor, ions in the ferroelectric material shift their position to one of two positions depending on the polarization of the electric field applied. When the electric field is removed, the ions remain polarized in the same position as when the electric field was present [25].

Ferroelectric materials switch only in an electric field and are not affected by magnetic fields.

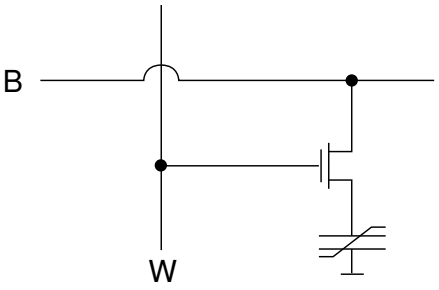


Figure 3.4: *Schematic drawing of 1T FRAM cell [16].*

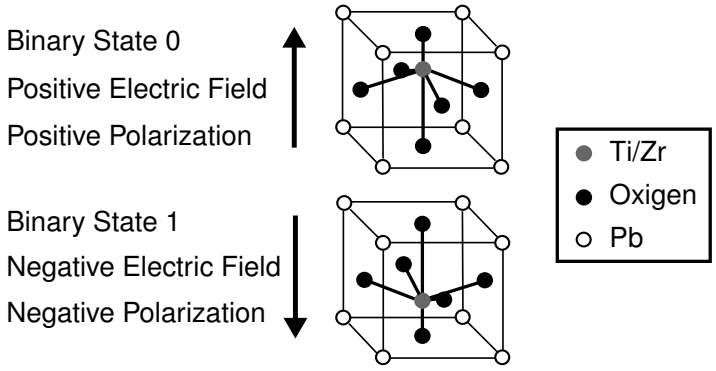


Figure 3.5: *Two stable states in a ferroelectric material [25].*

3.3.1 SEE susceptibility

Since FRAM is a relatively new technology and has only recently become affordable in respect to flash, DRAM and SRAM there has been little interest by the space industry, which are the main main driving force for testing of COTS devices, to investigate SEE susceptibility.

Some testing has been done by Scheick et al. [26] and it has been found that FRAMs are sensitive to SEUs and SELs and should be excluded from use in severe radiation environments.

3.4 Magnetoresistive RAM

Magnetoresistive RAM (MRAM) uses two ferromagnetic plates separated by a thin insulating layer to store its data. One element is a permanent magnet with a fixed magnetic polarization, the other one can be polarized by an external field. When both magnets

have the same polarization they create a low resistance path, when they have opposite polarization they create a high resistance path.

Reading from the cell is accomplished by measuring the current when enabling the word line and setting the bit line high. A high current indicates a '0', a low current indicates a '1'.

Writing is accomplished by passing a current through the bit line (B) and the digit line (DL), which lie perpendicularly to each other, causing an induced magnetic field at the junction where the cell is.

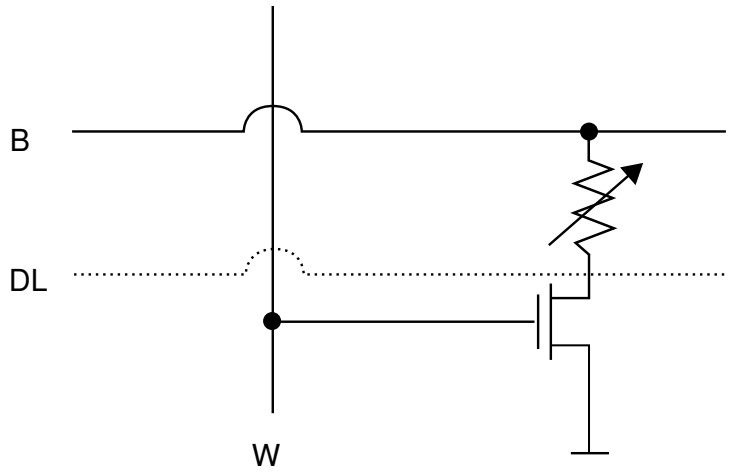


Figure 3.6: *Schematic drawing of 1T MRAM cell.*

3.4.1 SEE susceptibility

The same argument about the low amount of available data for SEE susceptibility of FRAM also apply for MRAM. Since the cells do not rely on charge to store a bit, they should not be vulnerable to SEUs, but the sense amplifiers and the programming circuitry probably are [27]. Resistance against TID effects and SEL effects are found to be rather good in new devices [28].

3.5 Phase Change RAM

Phase-Change RAM (PCRAM), also known as PRAM, Chalcogenide RAM (C-RAM) and Ovonic Unified Memory, employs a chalcogenide material, such as a $Ge_2Sb_2Te_5$ alloy (GST), to store its data. This material has the ability to change between a amorphous and a polycrystalline form when heated and cooled [29]. In the amorphous state, the material features a high resistivity while in the polycrystalline form, it is characterized by a low resistance value.

Figure 3.7 shows the schematic of a PCRAM cell composed of a heater and the GST material. To write a '1' (SET state), the GST material is heated to a temperature between

200 °C to 400 °C which is above the crystallization point, but below the melting point. In this state the material has a low resistance.

To write a '0' (RESET state), the GST is heated to above the melting point of 600 °C. This turns it back into a amorphous, an almost glass like, state which has a high resistance. The time to switch from one state to another is about 100 ns.

Reading the device is done in the same manner as with the MRAM. By putting a voltage over the cell, the amount of current flowing through it can be detected by a sense amplifier. A high current indicates a '1', and a low current indicates a '0'.

As the material is permanently in its present state until reheated, the data will not be lost when powering off the device making it a non-volatile memory.

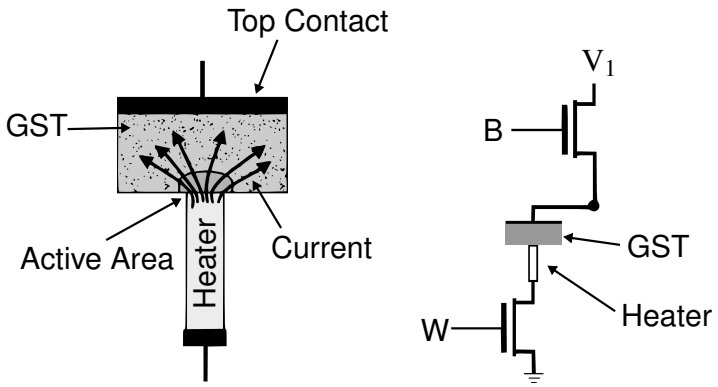


Figure 3.7: *Schematic drawing of a PCRAM cell.*

3.5.1 SEE susceptibility

The PCRAM has only recently become available commercially, but some SEE and TID testing has been done concluding that the only change seen are degradations of the select transistors causing a move in the characteristic current for '1' and '0' [29] [30]. The sensing circuitry was not tested, as it was placed external to the chip on this sample. Since it is based on Complementary Metal Oxide Semiconductor (CMOS) technology it might be sensitive to SET.

3.6 Electrically Erasable Programmable ROM

Electrically Erasable Programmable Read-Only Memorys (EEPROMs) can store a bit with a single transistor. This transistor is equipped with two gates separated by a thin insulating layer where the bottom gate is floating [16]. When applying a high voltage to the top gate and Vdd to the source, some electrons will flow from the channel through to the bottom gate due to the Fowler-Nordheim tunneling effect. Upon turning off the voltage, the electrons will be trapped in the floating gate causing the transistor to have a higher threshold voltage. The cell is now referred to as erased and will be recognized

by the readout circuitry as a '1'. To program the cell and remove the trapped electrons, a high voltage is applied to the source of the transistor with the gate grounded.

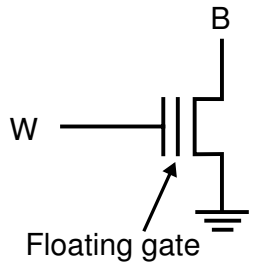


Figure 3.8: *Schematic drawing of a EEPROM cell.*

3.6.1 SEE susceptibility

Due to the construction and size of the floating gate in the EEPROM cell, removal or insertion of charge into a floating gate by an ionizing particle will be difficult. The EEPROM have been found to have a very low SEU cross section while reading and a somewhat higher for writing [31]. Though the readout circuitry is still vulnerable and can cause SEFI with a higher cross section [32].

3.7 Flash memory

Flash memory is similar in many ways to the EEPROM and got its name because it has the ability to erase whole blocks of memory at once instead of just one bit at a time like the EEPROM. The flash cell uses a floating gate transistor, similar to the EEPROM, and is commonly connected together in either a NAND or NOR configuration, as seen in figure 3.9. The NAND construction uses less layout space but is inherently slower as all the transistors are in series.

Due to the use of a more compact cell construction and because it utilizes a block configuration, the flash memory can achieve much higher densities and speeds than the EEPROM and hence it has become the most widely used non-volatile memory today.

3.7.1 SEE susceptibility

Due to the increased density and aggressive scaling of flash memory, the floating gate of the flash memory is becoming more vulnerable to SEUs from lower LET particles [33][34]. A 90 nm 1 Gb NAND flash was found to have a cross section of $10^{-15}\,\mathrm{cm^2\,bit^{-1}}$ at an LET of $10\,\mathrm{MeV\,cm^2\,mg^{-1}}$. SEFIs are also present, but at 3–4 orders of magnitude lower cross section [35].

Recent devices also employ a page buffer for storing a complete block read from the flash memory. This page buffer is constructed from SRAM cells which have a relatively

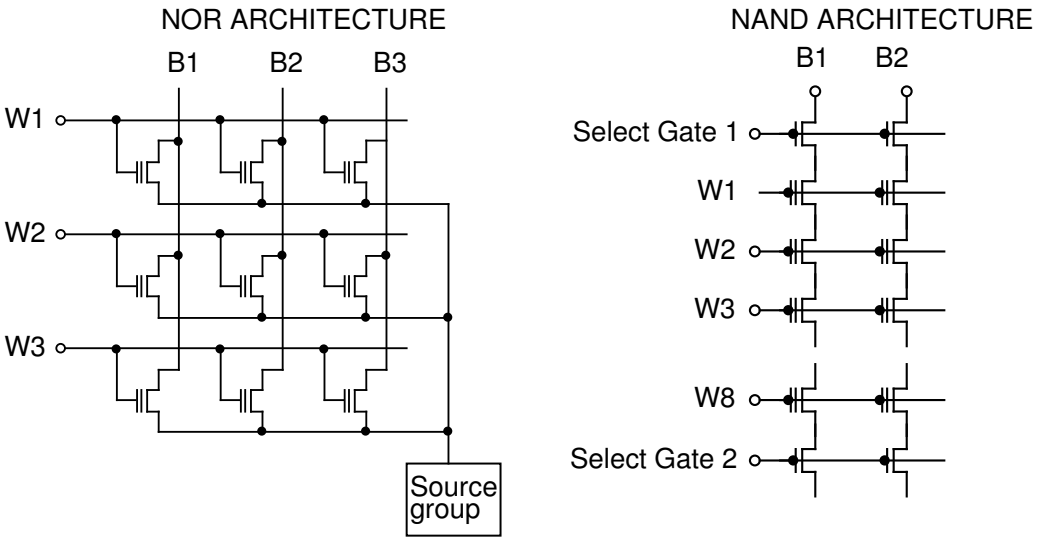


Figure 3.9: *Schematic drawing of the flash NAND and NOR structures [16].*

high cross section per bit. But as the page buffers are small, with a size of some kilobit, the cross section per device becomes relatively small.

3.8 Applicability of different memories as a neutron detector

Some features of the memory is necessary to be present for it to be useful as neutron detector, listed here in descending order:

High SEU cross section
A high SEU cross section per device is needed to get a detector with a high efficiency. To achieve this, the device can have a lower cross section per bit, but be available in a high density, or it should be cheap enough to be bought in quantities large enough to compensate for the low density.

Low amount of unwanted radiation effects
This includes SEL, SEFI, TID, stuck bits and destructive breakdowns. SEL can be mitigated on the hardware level by restarting the device upon a current increase, by using a current limiting device to avoid the latchup structure reaching its holding current or by running at a voltage too low for the latchup to occur, if the device allows it. Stuck bits can be mitigated in the firmware by writing back and re-reading the bit detected to have a SEU, to check if the written value sticks. SEFI can be mitigated by restarting the device upon detecting many errors in a row or other effects particular for the device under test. TID and breakdowns can not be mitigated. All these effects either creates dead-time for the detector or increases the probability of a wrong radiation level readout.

High endurance
Depending on the end use of the device, it might be needed to have a continuous

lifetime of at least a year or two. Two effects factor in here, the TID and normal aging. TID is not normally a concern if the device is not supposed to be used in a high radiation environment, as most devices can withstand an accumulated dose of more than 10 krad. Aging effects depends on the type of memory, but most suffer at least from electromiragtion and thermal damage. Floating gate memories have problems with degradation of the oxide between the floating gate and the channel, causing the cell eventually not to be programmable.

If a device has a readout time for the whole device of 100 ms, it would need an endurance of 6×10^8 to survive two years.

Fast read/write speed

Depending on the end application, having a delay of tens of seconds between a particle hitting the device and a SEU being detected by the readout can be unwanted. The device read-through speed is both dependent of the density and the bit read-write speed of the device.

	FRAM	MRAM	PCRAM	Flash	EPROM	SRAM	DRAM	Ideal
Write Speed	<150 ns	<40 ns	<150 ns	<100 ns	<10 µs	<10 ns	<200 ns	<60 ns
Erase Speed	<150 ns	<40 ns	<150 ns	>10 ms	>10 s	<10 ns	<60 ns	<200 ns
Endurance	10^{12}	10^{15}	10^6	10^6	10^5	10^{15}	10^{15}	10^9
Cost/Bit	High	High	Med	Low	Med	Med	Low	Low
Bits/Dev	10^6	10^6	10^8	10^{10}	10^6	10^7	10^8	10^8
SEU (bit)	No	No	No	Yes	No	Yes	Yes	Yes
SEU (periph)	Yes	Prob.	Yes	Yes	No	Yes	Yes	Yes
SEU σ	10^{-16}	na	na	10^{-17}	na	10^{-14}	10^{-18}	10^{-10}
SEL	Yes	Prob.	Yes	Yes	Yes	Yes	Yes	No
SEFI	Prob.	Prob.	Prob.	Yes	Yes	Yes/No	Yes	No

Table 3.2: *Overview of specifications for different RAM, partly based of Kayali [36]. Cross section of SEU is taken for protons at 50 MeV. 'na' in the table indicates data was not available. Endurance is measured as number of read write cycles before problems arise.*

Table 3.2 summarizes the features of each device. From what has been proposed above as the ideal detector, it can be seen that the MRAM and PCRAM can be dismissed, since they have not currently been found to be sensitive to SEU, testing could be done to determine this further. FRAM is currently available at too low densities and at a too high price to be useful at this time, but could be applicable in the future. Flash suffers from a lot of unwanted radiation effects and has in addition a low endurance. EEPROM are available at too low densities and has even lower endurance. This leaves DRAM and SRAM as viable contenders. The current density of DRAM do not make up for its low SEU cross section compared with the SRAM. A pre-study was done for this thesis, as noted in the section 1.2, with a SDRAM from an older technology node compared to a SRAM and it was found that it had a SEU cross section of at least three orders of magnitude lower than the SRAM.

For this work several different SRAMs have been picked for their various properties. Two synchronous SRAM from two different manufacturers were chosen to test if SEFI would hinder them from being used as a neutron detector. One device was picked for being able to run at voltages as low as 1.0 V, in contrast to 1.5 V as is normal for most of the other devices we have tested. A lower voltage reduces the charge needed to upset a memory cell and thus will increase a device's overall sensitivity. One device was chosen for its fast access speed of 10 ns, in contrast to 55 ns which was common for most of the other devices we tested. Access speed could possibly alter a device's sensitivity through for instance SETs. Another device was chosen for having the largest available bit size for an asynchronous SRAM of 64 Mb. A larger bit size means a larger sensitivity per device if the sensitivity per bit is not exceptionally low. The rest of the devices were chosen from the ultra low power series from Cypress to look for similarities between devices within the same series. The device with the high bit size is also a part of this series.

Chapter 4

Neutron detector implementation

This chapter focuses on the development of the hardware, firmware and software for a neutron detector.

4.1 Detector system overview

To have a setup for actively detecting neutrons, at minimum three things are needed. 1) A sensor to convert the energy deposited by the particle to a readable signal, 2) a preprocessor for detecting the signal and converting it to a signal which can be transmitted to the readout and 3) a device for collecting or reading out the number of counts from the detector. The last device can also be split into two, having a device in between that converts the signal to a readable signal for the device which counts the events from the detector. A general setup can be seen in figure 4.1.

Converting the energy deposited by the particle can be done in many ways, but in electronic memory this energy is converted to a flipped bit. This bit flip can be detected by writing a known pattern to the memory and continuously reading it back checking for alterations to the known pattern. The readout of the sensor can be done with for instance a microprocessor, an Field Programmable Gate Array (FPGA) or by use of basic electronic circuits. The readout device also needs to be able to transmit the number of events detected to the device collecting the events. This gives the device the functionality of a preprocessor of the sensed signal. Accompanying the preprocessor there are commonly also support electronics needed for the operation of the preprocessor and the sensor. This can be for instance power supplies, clock circuits, communication circuits or other sensors for temperature or current.

The device which should convert the signal from the detector to a readable signal by the data processing device is commonly either an Analog to Digital Converter (ADC), a Data Acquisition (DAQ) device or a direct communication link. The data is then fed to a device that post processes the data and stores it for later retrieval or it displays the data directly to the user. This device could be a pulse counter, a computer or a specificly designed hardware.

If we compare the general setup with a scintillator setup, we have the scintillator as

the sensor, the photo multiplier tube in combination with an amplifier as the preprocessor and a pulse shaper in combination with an ADC, inside a counter, as the converter. The signals can then be collected and displayed by a pulse counter.

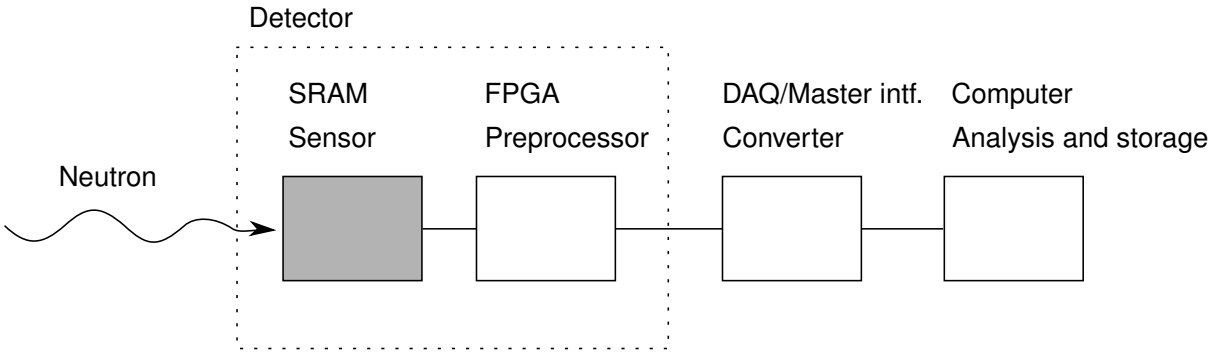


Figure 4.1: *Overview of a detector system.*

4.2 Hardware

An important aspect of creating hardware for a neutron detector is to avoid any additional components besides the SRAMs that suffer from Single Event Effects (SEE). Figuring out if a component is suitable can be determined by looking for radiation testes of the same component already completed by others or by picking suitable components and testing them yourself. COTS components have been used in the space industry for some time due to low availability of high performance semiconductors [37] and a large amount of test data of radiation hardness and SEE susceptibility have been accumulated over time. An example of such a database is the NASA Goddard Space Flight Center Radiation Test Database [38].

A schematic overview of the hardware can be seen in figure 4.2 and a picture of two of the detectors can be seen in figure 4.3.

The hardware exists in two revisions, but with only minor component differences. The first design is composed of a 100 MHz crystal oscillator providing the main clock, an Actel IGLOO nano IGLN250Z flash FPGA for controlling the read out of the SRAM and communicating with the PC, some step down voltage converters, two transistors acting as an inverter for pulsing out SEUs and the SRAM.

The second design adds the possibility of having four SRAMs on two separate buses. As this increases the number of pins beyond the 100 which are available on the Actel IGLOO, the IGLOO is exchanged by an Actel ProASIC3 A3P250 flash FPGA with 208 pins. The inverter is also replaced by a LTC1480 RS485 communication circuit. The inverter circuit can be added back by connecting an add-on board to some spare connections on the board.

The first design was used for testing at PTB and CERF and the second revision for the other tests.

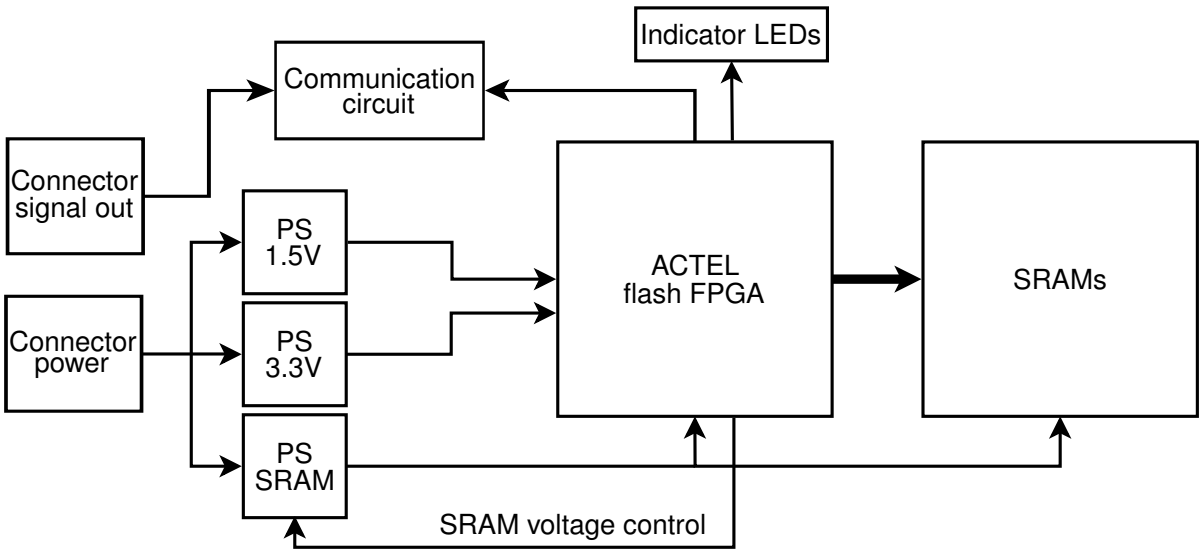


Figure 4.2: *Schematic overview of hardware for the detector.*

4.2.1 SRAM packages

Just as everything else, SRAMs come in different sizes and packages. From a designers point of view this means different placement of address/data-bus and different pin layouts. Most manufacturers adhere to the JEDEC Standard No. 21C [39], which describes the pin layout for many types of RAM devices, packages and sizes. But since not everything is specified in the standard, some qualified guesswork and comparison of different makes and models needs to be done to avoid making hardware modifications when later adding a new type of SRAM to an existing board.

The 2nd revision Printed Circuit Board (PCB) exist in five different designs created for five different packages, Thin Small-Outline Package 2 (TSOP2) 44 pin, Thin Small-Outline Package 1 (TSOP1) 48 pin, Very Fine-Pitch Ball Grid Array (VFBGA) 48 pin, Thin Quad Flat Pack (TQFP) 100 pin and Fine-Pitch Ball Grid Array (FBGA) 165 pin. To avoid some of the problems of pin compatibility, all of the pins that were not ground or power pins on the three first packages mentioned were all routed to the FPGA. The decision of which pins should be connected to what can now be done in firmware at a later stage.

To increase the number of SRAMs to be tested at once on the same board when there is a constrain on the number of pins available on the FPGA, it is possible to utilize a bus structure connecting two or more SRAMs in parallel. This is possible by having a separate connection to the chip enable pin for each SRAM. The chip enable pin makes the SRAM put it's data pins in high impedance mode avoiding interference with the other SRAM circuits. In addition it will also stop responding to write and read signals. The PCBs design for the two TSOP packages and the TQFP package utilizes this bus structure to connect two SRAMs to the FPGA.

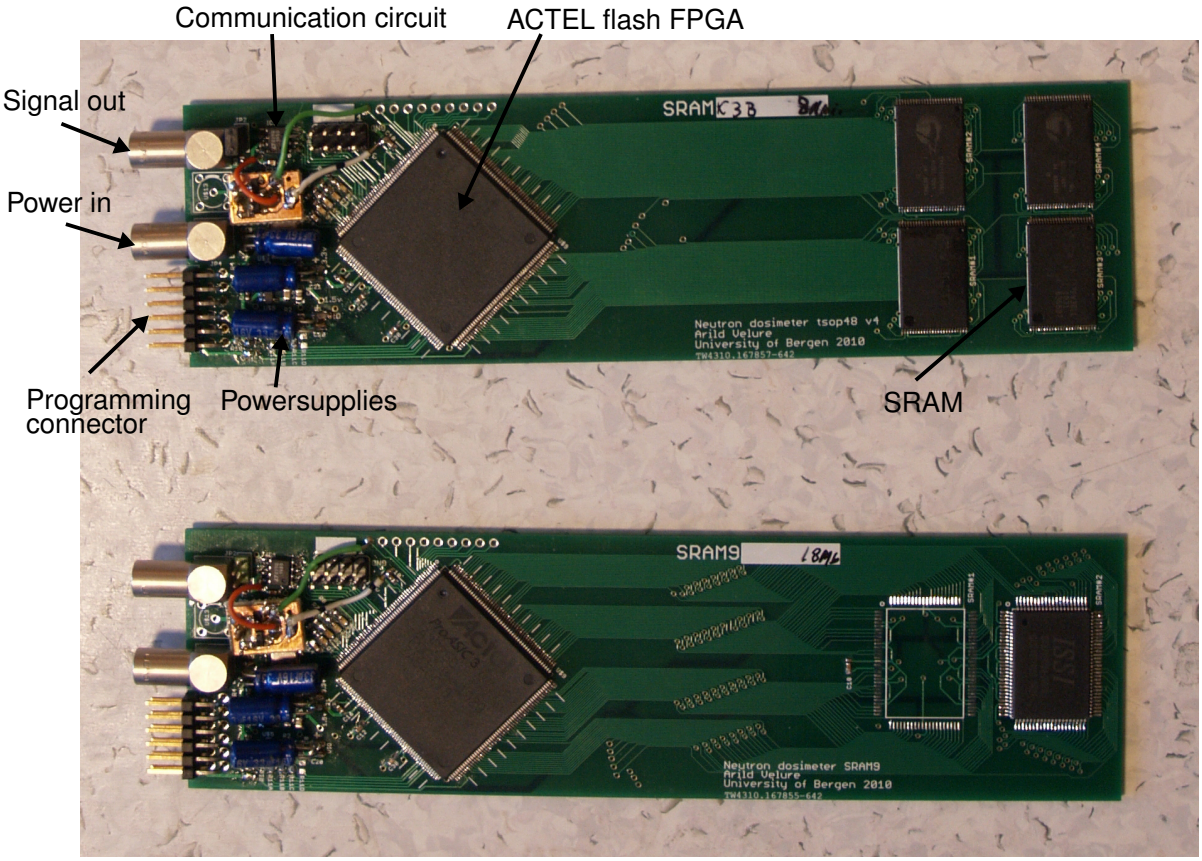


Figure 4.3: *Picture of two of the detectors.*

4.2.2 Voltage control

Different SRAMs are specified to different core voltages and current consumptions. In addition it has previously been found by among others Flament et al. [19] that the cross section for SRAMs are dependent on the core voltage. This calls for a flexible voltage supply design which is handled by adding a variable voltage supply that can be controlled by changing resistor values. These resistors are connected to pins on the FPGA, enabling control of the voltage from the firmware during runtime.

The voltages and currents available are 500 mA down to 1.2 V and 100 mA down to 0.6 V, depending on the voltage controller used.

4.2.3 Communication interface

To be able to monitor the detector from the control room during irradiation, the detector needs some form of hardware for transmitting its data over the communication link. Connecting the communication link directly to the FPGA is possible, but not advisable as a malfunction in the communication link could damage the FPGA directly. Some form of buffer or communication device in between the link and the FPGA is the best

choice.

When choosing communication form, there is a choice between simplex, half-duplex or full-duplex communication. Simplex is the most trivial form, where the data can only flow in one direction. This communication form can be found in many particle detectors like for instance the scintillator, where a pulse is transmitted for every detected particle. In half-duplex communication both the detector and the receiver can communicate with each other over the same link, but only one at a time. The communication circuit would commonly use the same pair of wires for both sending and receiving. In full-duplex communication both detector and receiver can talk to each other at the same time without disturbing the communication.

If testing many device at the same time, a communication protocol which uses half- or full-duplex communication in a bus or ring topology would be the best as this would minimize the amount of cabling needed between the experimental area and the control room.

There are three main iterations in the firmware design for the communication which are described below.

Pulse counter design

The first design used in accelerated irradiation testing at PTB, uses a simplex communication form. The detector sends out a short pulse for every SEU detected in the SRAM. The signal can be connected to a pulse counter to recorded the total amount of SEUs per run. A simple inverter, used as a buffer, is placed in between the FPGA and the communication link on the detector.

This design can be seen to have some drawbacks. Firstly, if more than two device are to be tested at the same time, either a counter able to record more than one input simultaneously or two or more counters are needed.Another drawback is the lack of time-stamping capability. Time-stamping is in principle possible with high-speed data-acquisition, but this has not been implemented.

LabView DAQ design

The second design was used at CERF and OCL and is based around the previous design, but tries to compensate for some of its shortcomings. The pulse-width of the pulses have been increased enough so that the pulses can be picked up by a low-cost DAQ device like the National Instruments USB-6008 or similar. The DAQ provides the possibility of having time-stamping of the incoming pulses on a computer and enables more than one detector to be recorded at the same time through the many inputs on the DAQ.

A drawback of using these low-cost DAQs is that their digital input ports don't have built in hardware sampling and will thus only provide a sampling-rate of about 70 Hz through software sampling, largely depending on the speed and load of the computer used. To be able to accurately detect a pulse, the detector can't have a higher pulse-rate than about 30 Hz, which is quite low. Instead of the digital ports, the analogue channels

need to be used. The analogue channels have a hardware based sampling rate of 10 kS/s divided between all channels used, but at least four times oversampling is needed per channel to get an accurate detection of a pulse.

RS485 communication

As there was a growing request for having a form of two-way communication for changing settings in the firmware during runtime, a new communication interface was designed. This design uses a half-duplex communication over a RS485 link. RS485 is a differential, high speed interface that provides communication between a master and multiple slaves over a single pair of wires in a multi-drop configuration with distances up to 1200 m. The RS485 standard only defines the physical layer (layer 1 in the Open Systems Interconnection model (OSI) layer model) so the communication protocol in the data link layer can be freely chosen.

This design uses a proprietary protocol with two start bits, four address bits (assigned in firmware), 2 address bits (assigned per SRAM), 26 data bits, one even parity bit and one stop bit. The address and data bits are in addition hamming encoded giving a total of 38 bits for the main load. The added parity bit in addition to the hamming bits enables Single Error Correction, Double Error Detection (SECDED) increasing the reliability of the link. The design is fully configurable to other address/data sizes as long as all devices on the same bus uses the same configuration.

The data transmitted back to the master from the slave contains a snapshot of some of the internal registers and counters of the detector, this means that if a packet is lost due to bad communication no data is actually lost, in comparison to the previous designs where a loss of a pulse equaled a loss of a SEU.

The present design uses a communication speed of 2.5 Mb/s which has been tested to work reliably over a 100 m cable as long as the appropriate signal termination is applied at both ends. The amount of termination is dependent on the rated impedance of the communication cable used. A variable termination has been made for easy adaption to different cables.

4.3 Firmware

The firmware for the detector was written in VHDL with robustness against SEUs in mind. The flash FPGA is not sensitive to upsets in the configuration of the blocks, which could lead to SEFIs, but it is still sensitive to upsets in registers and the internal memory [40]. The upset rate for registers is 0.27×10^{-14} cm^2/logic cell [41] which is about an order of magnitude lower than the average cross section per bit for the SRAMs we have tested and on the same order as for a SRAM based FPGAs. The number of available registers in the flash FPGA is though only 6144 [42] which gives the device a cross section per device of three orders of magnitude lower than for the least sensitive device we have tested. The cross section for the internal memory is higher, but it is not

used in this design and therefore not of any concern.

4.3.1 SEU hardening

To prevent any malfunction due to SEUs in registers of the FPGA, the design uses Triple Modular Redundancy (TMR) for all critical single bit registers and hamming encoding for all registers longer than one bit. Both techniques gives the ability to correct one error in the register.

Since the states in a finite state machine also are stored as registers they also need some form of protection not to end up in an illegal state or to jump to a wrong state causing a lock up or a corruption of other registers. The best way to avoid this and in addition maintain a high speed in the finite state machine is to use one-hot encoding of the states. In one-hot encoding only one bit is 1 in the state vector for any given state and the rest is 0, this means that the vector needs to be as long as the number of states represented by the vector. One advantage is that moving from one state to the next can always be done with a distance of two, independent of the length of the state vector. Even though the number of flip flops used are larger than for other encodings like Gray and binary, the majority of states are unused states and so the probability of getting a wrong output is less [43]. The state vector also has a hamming distance of two, meaning that two bits need to be flipped to move to a wrong state. Binary and Gray encoding have a hamming distance of 1 and is therefore inherently less safe.

To avoid getting stuck in an unused state, the state machine is separated into two processes. One describes the combinatorial logic that computes the output values and the next state, and the other is a register that stores the state. By always assigning a valid state to the next state in the combinatorial logic, an exit from all illegal states will always be present, see figure 4.4 for an example.

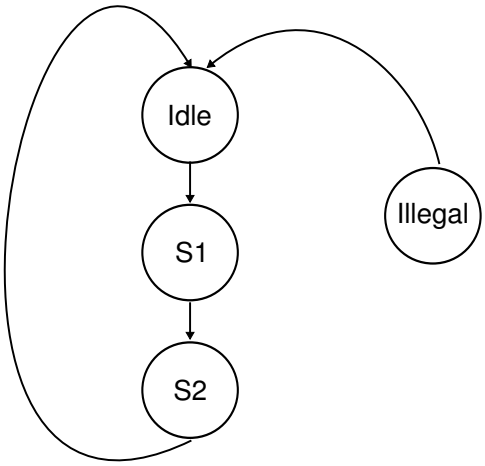


Figure 4.4: *Illustration of a finite state machine with exit from an illegal state. The next state after the illegal state can also be a special error state which can do some damage control before going to the idle state, but this was not needed in this design.*

4.3.2 Hierarchy, regularity, modularity

As stated before the design is supposed to support a wide variety of different SRAM devices and the VHDL code should therefore be made so that recompiling for a different devices can be made with a minimal change of code. The code should also not be separated into different branches for each device, as the maintainability and chance of error and differences in code between devices would increase.

To reach this, the standard structured design strategy with hierarchy, regularity, modularity was used. Hierarchy involves dividing a system into smaller modules and repeating this until you reach a level of comprehensible detail. This means you either reach a level where it can not be divided any more, or you reach a level where there are prebuilt components or modules available. Hierarchy also eases the testing and verification of the design as it can now be done one module at a time which makes fault finding easier. But hierarchy isn't enough, as you in the end may end up with a lot of different sub modules which are really not that different. The best way is to strive to divide the design into similar modules creating a regularity among the modules. To still keep a good overview of the interface between all the submodules and to easily be able to reuse modules later it is important to have well defined interfaces to the modules.

This design uses *generics* to reach the regularity goal. A generic is a constant that can be placed in a higher module in the hierarchy tree which can for instance define the width of a vector. The design has collected all the parameters for all the SRAMs as constants in a separate package. This package also contains information about all the PCBs, which SRAMs is connected to which PCB and how many there are on each PCB. These constants are used as generics throughout the design and in the top entity the PCB, for which the design should be synthesized for, is defined. Some synthesis tools provide the ability to change top entity generics before synthesis so that the code never needs to be modified.

Because there is a wide variety of different SRAMs it is in principle not possible to use the exact same modules for all SRAMs. To integrate the special modules for the odd SRAMs into the main code, the *if [condition] generate* statement is used to choose a certain module instead of the normal one when synthesizing.

The hamming library used in the design is created with the modularity in mind. The functions for decoding, encoding and doing various other tasks uses unconstrained vectors in the interface. This means that the functions can be used on all sizes of vectors even though different lengths of vectors have different number of additional hamming bits depending on the length and thus also different decoding methods. This is possible by using vector attributes like *length* and *range* to get the size of the input vector for deciding how to handle it.

A block diagram of the current design can be seen in figure 4.5. For a description of the listed modules in the block diagram see appendix E.

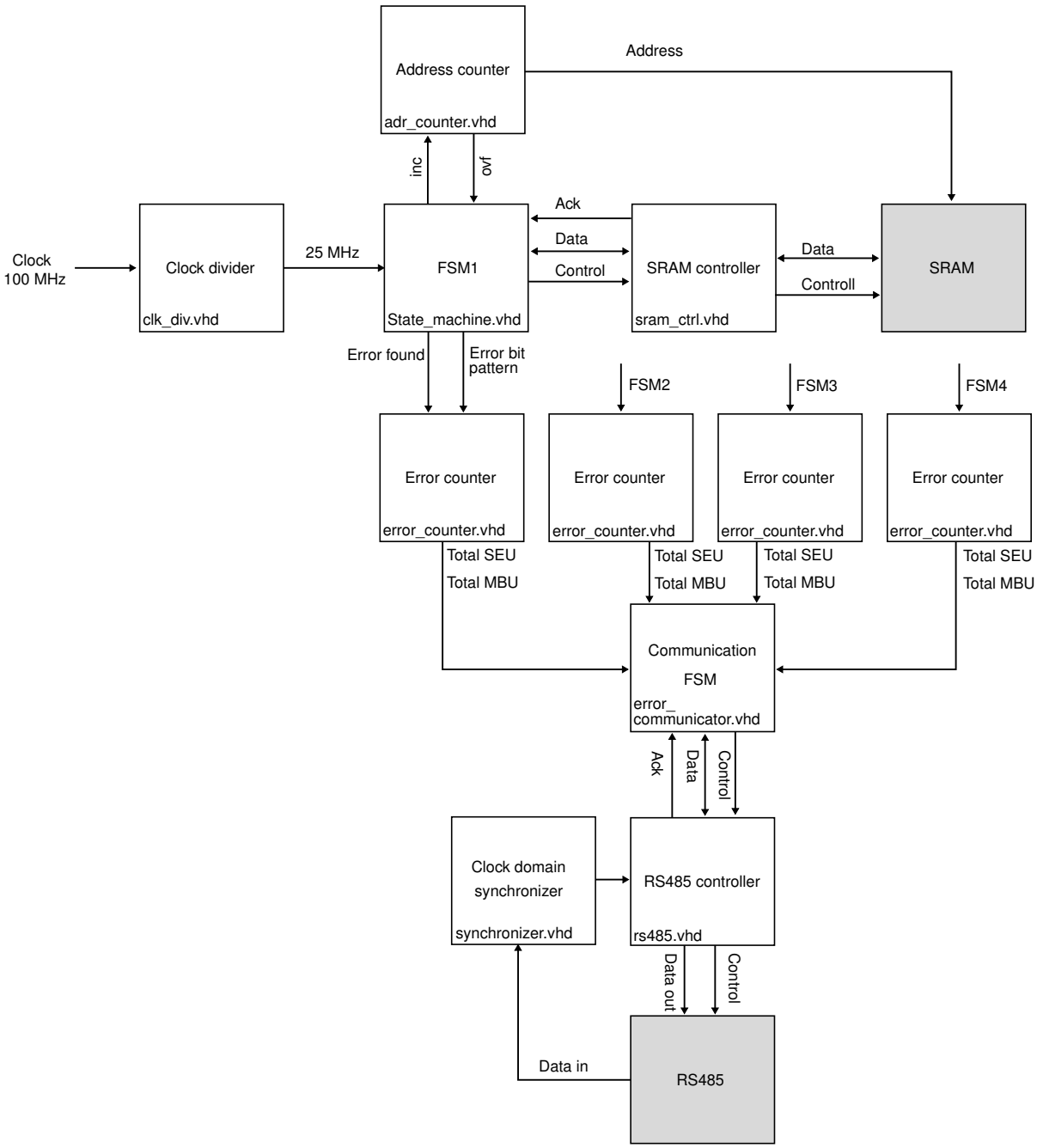


Figure 4.5: *Block diagram of the firmware of the current detector. Boxes in gray are external components. The state diagram of the main finite state machine has the same flow as shown in the flowchart in figure 4.6.*

4.3.3 SEU detection in SRAM

The method of detecting an Single Event Upset (SEU) in a SRAM is rather straight forward, as can be seen in the flow diagram of figure 4.6. There is an initial startup

phase where a known pattern is written to the all the addresses in the SRAM. When the startup phase is done, the value from the first address is read back and compared to a known value by xoring the known value with the read. This will result in a vector containing a 1 for every upset. The correct value is then written back to the address and the system moves on to the next address. When there are two SRAMs present on the same bus they are read out consecutively for each address.

A checkerboard pattern, a pattern of alternating ones and zeros, is used when writing to the memory. To check for stuck bits, the bit pattern is inverted after each read through of the whole address space. Other patterns like all-zero, all-one or walking-one can be used, but changing from one pattern to another has not been implemented. In literature it has been found that the SEU rate is not significantly dependent on the pattern stored in the memory [44].

To reduce the possibility of transient values or temporary errors in the readout of the SRAM which could create false indications of SEUs, the design reads out the data from the same address three times and uses majority voting to choose the correct value.

If the data at an address is found to contain all zeros or all ones when using a checkerboard pattern, it can be determined that the device has malfunctioned in some way. The probability of flipping the exact bits needed to get all ones or zeros is extremely low and the SEUs should thus not be propagated to the SEU counter. Instead a flag is raised which can be read remotely by the computer in the RS485 communication design.

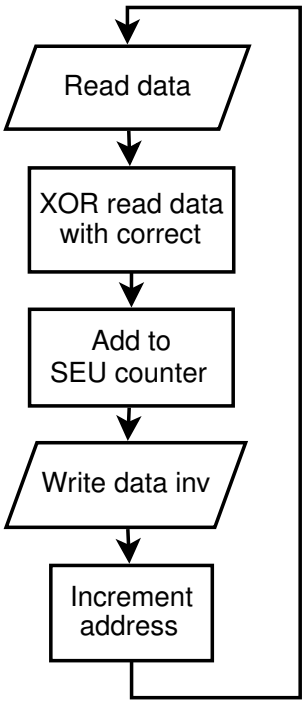


Figure 4.6: *Simplified flowchart for SEU detection*

4.3.4 SEU transmission

Pulse counter design

In the pulse counter design the finite state machine sends out a one clock cycle pulse for all the resulting bits of the xor between the read data and valid data, one bit after another. An extra zero is added in between each bit to get a proper pulse in case there are more than one '1' after another.

The drawback of using this design is that it increases the read-through time due to having to pulse out all the bits before being able to advance to the next address. For a 16 Mb SRAM the read-through time is increased from about 5 s to about 38 s. A long read-through time is a drawback when doing short high-intensity irradiation runs of less than a minute, as you would need to wait for a complete read-through after the beam stops to get all the SEUs.

LabView DAQ design

To be able to use the Labview DAQ boxes and account for their slow sampling rate, the pulsing needs to be moved into a separate finite state machine to not slow down the main finite state machine. This also removes the problem of the previous design with the long read-through time.

The pulse rate and duty cycle can now be set at will in the firmware giving greater flexibility for use with other types of DAQs. To account for SEUs arriving faster than they can be pulsed out, a buffer is added in the form of a hamming encoded counter.

RS485 communication

In addition to the SEU counter from the previous design, this design adds a MBU counter. The counter increases if more than one SEU is detected on the same address. It does not account for MCUs across addresses and is therefore mostly used as an indicator.

The counters can be reset and read remotely over the RS485 interface from the readout computer.

4.3.5 Scintillator counter

For beam flux monitoring during irradiation measurements a scintillator or other pulse generating detectors is sometimes used. The counts will commonly be recorded on a pulse counter or another form of DAQ device provided by the facility. To better coincide the counts from the scintillator with the SEUs from the detector, a separate scintillator input is available on the detector. The counts from the scintillator will now be time stamped together with the SEUs when the detector is read out. The signal from the scintillator needs to be in 3.3 V logic and each pulse needs to be longer than 100 ns for accurate detection.

4.4 Software

For the two last iterations of the design a program designed in LabView is used to collect the data from the detector and store it in a log file.

LabView DAQ design

For the DAQ design the communication line is sampled continuously and the samples are collected in bulk every fifth second. The data is digitally low pass filtered before entering an edge triggered counter for counting the SEUs. A hysteresis is added to the input of the counter to remove problems with a floating input on the DAQ. An open input will float at about 1.4 V to 1.6 V which is in the center of the switching area of 3.3 V. The front panel shown in figure 4.7 contains the accumulated number of SEUs for each device and a graph showing the last collected sample pack for each communication line.

For the second measurement at the OCL a current-monitor was also added by use of an extra DAQ which sampled the voltage over a resistor in series with the main voltage for the detector. The current-monitor can give an indication that a SEL has occurred giving the user an opportunity to stop the irradiation run prematurely to save time or to reboot the detector.

The number of SEUs for each detector, the elapsed time since the start of measurement and the measured current is written to the log file after each bulk of samples is received.

RS485 communication

This design collects the packages from the communication interface, splits the package into address bits, SEU bits, MBU bits and status bits and displays them on indicators on the front panel as seen in figure 4.8. For each packet which is received a line is added to the log file with the current data from all SRAMs and a time stamp. A packet will only be received from the interface if the data in the current package is different from the last. This avoids flooding the log file if nothing has changed.

A configuration bit field for each SRAM is provided which enables the user to reset all internal counters on the detector, set one or both SRAM buses in pause mode, enable the readout of the scintillator counter on a specific SRAM, change the SRAM voltage and to turn off all LEDs to make the analysis of the current measurements easier.

4.5 Master interface

To communicate with the detectors over the RS485 link, a device on the master side is needed which can handle the high speeds of the communication channel. To be able to reuse some of the firmware modules from the detector and to offload all the communication handling from the readout computer a small development board from Opal

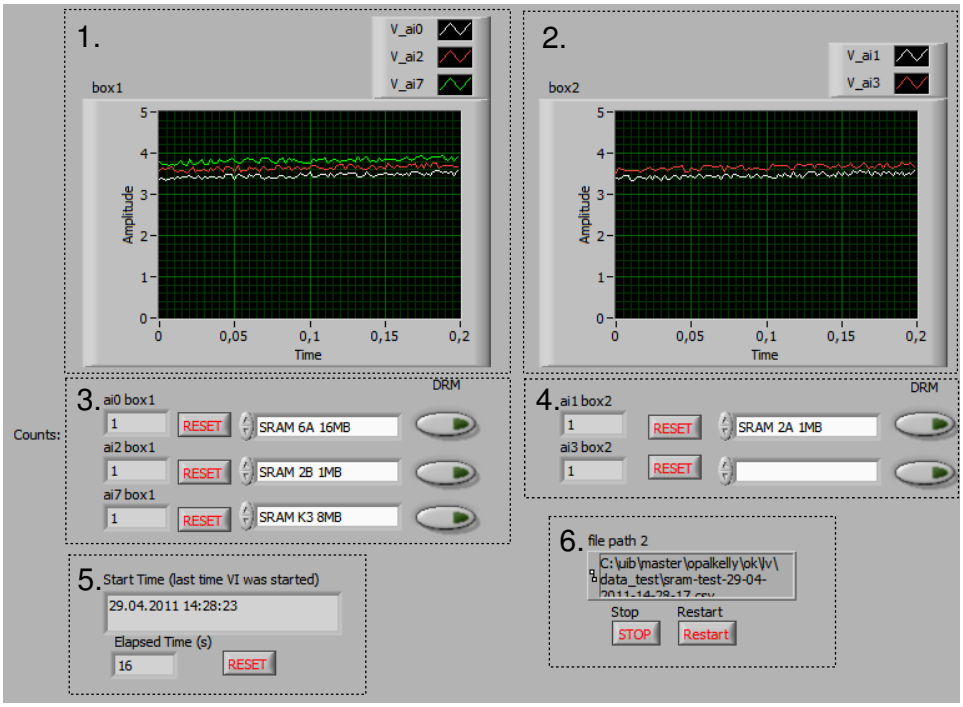


Figure 4.7: *Frontpanel of LabView for DAQ design with added groups for explanation. 1 and 2 is the voltage level of each communication channel on each DAQ, received from the last sample pack. 3 and 4 contains the current number of SEUs, a reset of the current count and an indication of which device is connected to the specific channel. 5 has the start time of the measurement, the elapsed time since the start and a reset of the time. 6 controls the starting and stopping of the measurement and the path to the log file.*

Kelly was used. The XEM3001 features a Xilinx Spartan-3 XC3S400 FPGA and a USB 2.0 high speed interface. The manufacturer provides precompiled VHDL modules for use with the USB interface which relieves the developer from needing to have any interaction with the USB protocol. On the computer side an API is provided which can be used in among others LabView to read data from the development board.

A small add-on board with the RS485 communication chip was added to development board to enable it to communicate with the detector.

4.5.1 Firmware

The development board reuses the RS485, hamming and an input signal synchronizer module, for avoiding metastability, from the detector firmware development. In addition it contains a FIFO for temporarily storing data to be transmitted to the host computer, a buffer containing the last message received from all devices and a local buffer of the control message which is going to be sent to the detector. The last message received buffer is used for comparing a received packet with the previous package to determine if there is a difference. A new package is only sent to the FIFO if it isn't the same as the last package received, this is to avoid flooding the communication link to

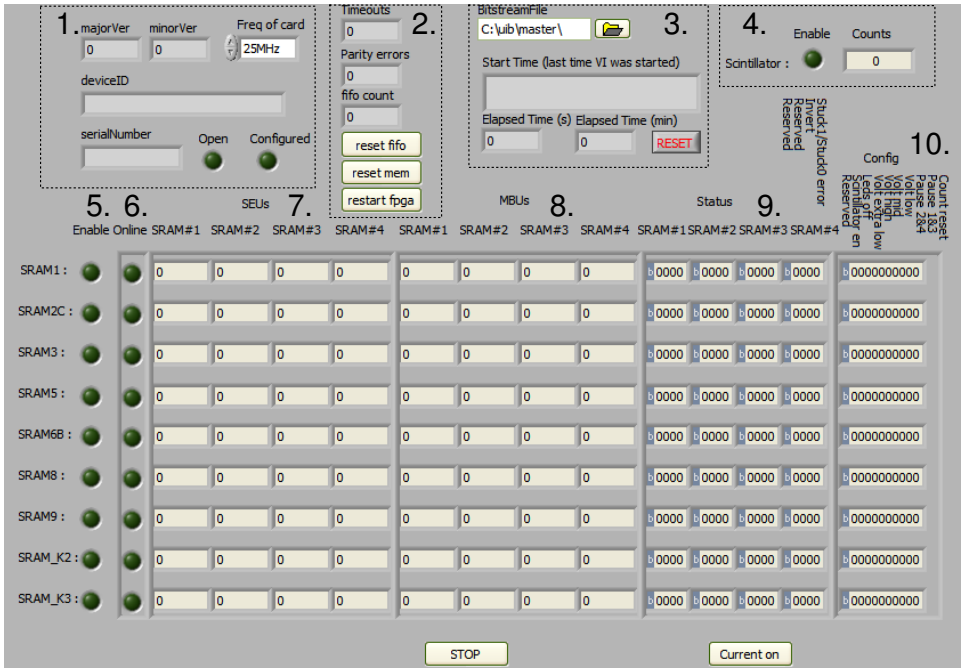


Figure 4.8: *Frontpanel of LabView for RS485 design with added groups for explanation. The current measurement is on a sub screen (not shown). 1 is related to the status of the initial configuration of the master interface. 2 contains counters from the master interface indicating the number of parity errors and lost packets, it also contains resetting of the internal buffers. 3 contains the start and elapsed time for the measurement in addition to the programming file for the master interface. 4 has the enabling of the scintillator and the number of counts. 5 enables communication with a particular SRAM, 6 tells if it answers. 7 lists the number of SEUs and 8 lists the MBUs. 9 has some status information from the detector and 10 contains control bits sent to the detector.*

the computer with unneeded packages.

4.6 Improvements and future outlook

To better pinpoint the occurrence of SELs, study MCU and avoid stuck bits, some changes to the hardware, firmware and software should be done for future work.

4.6.1 MCU detection

To study the occurrence of Multi-Cell Upset (MCU), the address where an SEU was detected and its corresponding data bits needs to be transmitted to the readout computer for logging and later analysis. Since the arrangement of the addresses internally in the SRAM is not known this might not produce any meaningful data and was thus not prioritized for this design. It could potentially be useful for future studies to investigate if any patterns in the data can be found after irradiation and if they can be exploited. It would also be nice for investigation of the anomalies in the upset rate for 90 nm Cypress

SRAMs, further discussed in section 6.2.

4.6.2 Stuck bits mitigation

In connection with SELs stuck bits will sometimes appear. In the normal test flow outlined in figure 4.6 these will be detected as SEUs, creating wrong data in the log file. A manual restart needs to be done to recover from one of these errors meaning the operator needs to constantly monitor the amount of upsets looking for abnormal increases in count rate. In figure 4.9 a new test flow is proposed which should avoid detection of stuck bits as SEUs. Upon detecting a SEU it should write back to and then re-read the same address to check that a SEU isn't detected in the newly written address. But if it is, then one of the bits must be stuck and a power cycle should be applied in order to reinitialize the memory. It would be possible to continue the readout and ignore the stuck bits, as no destructive effects have been seen from the SELs in this work, but as the latchup can increase the SEU susceptibility of the nearby nodes and thus increase the cross section, it would not be advisable.

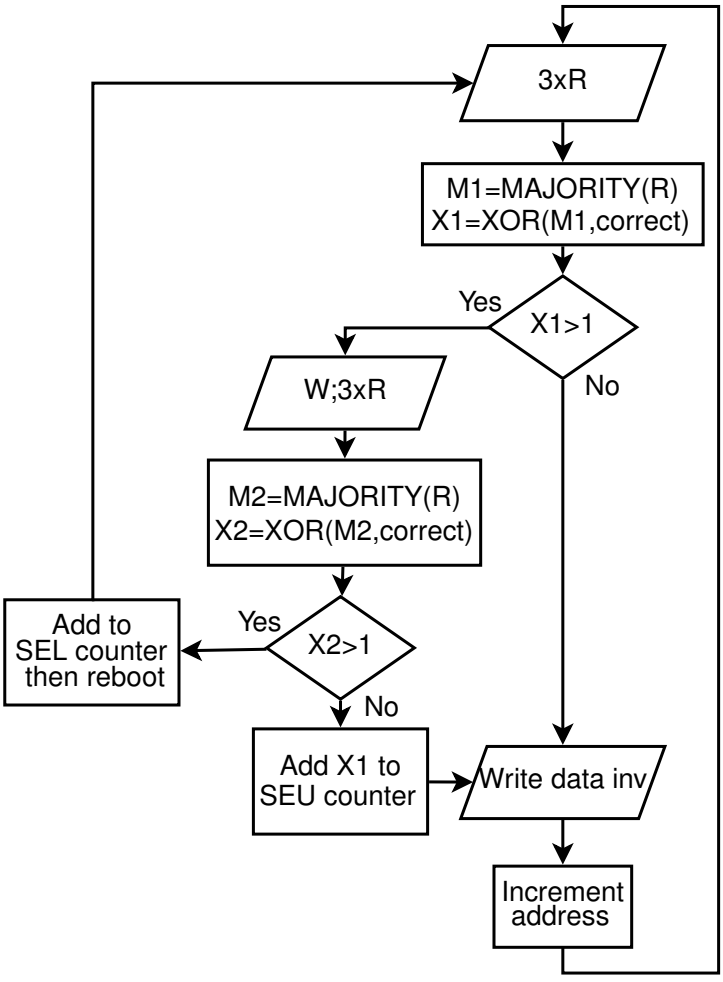


Figure 4.9: *Flowchart for stuck bit mitigation.*

The time currently needed to reinitialize a device is the same time as needed for a complete readthrough of the device. The cycle time is $N(3R + W) = 81\text{ms/Mb}$ where N is the number of bits in the device, R is the time to read an address and W is the time to write an address. To avoid losing too much time after a SEL has occurred the reinitialization time can be reduced by having a separate initialization phase which only writes to the device. The cycle time would then be $N \cdot W = 5\text{ms/Mb}$.

4.6.3 SEL mitigation

The detection of SELs is currently done by monitoring the current of the detector from the computer in the control room. This is not an optimal solution as the current is somewhat fluctuating with the load of the other devices on the detector and detecting small SELs can therefore be hard. A current monitoring circuit on the detector, only connected to the SRAMs, would be the best solution. This could be done for instance by using an AD7401 sigma-delta modulator from Analog Devices which converts an analog input to a high speed pulse-width modulated signal. Current sensors and ADCs with serial communication which stores the value of the input in a SRAM register should be avoided for the obvious reason of SEUs in the data.

A threshold value for the current can now be set in the FPGA, possibly also from the readout computer, which resets the device upon detecting a current above the threshold level.

Another option for mitigating SELs would be to restrain the current to within the normal operating current so that the holding current for a SEL is not reached. For low-power devices this can be done by basically connecting a resistor in the kilo-ohm range in series with the power supply line for the SRAM and having a capacitor connected in between. A sudden high current would increase the voltage drop over the resistor, thus reducing the voltage on the SRAM below the threshold of the holding voltage needed to sustain a SEL. The capacitor will supply the needed current for short current spikes due to change in activity in the SRAM. A voltage comparator can be connected to each side of the resistor to detect the voltage drop and provide a signal to the FPGA notifying it of the occurrence of the SEL. The use of a resistor as a current limiting device is only usable for low current SRAMs in the 100 µA range where a usual latchup at above 10 mA is a change of two orders of magnitude.

For devices needing currents in the 100 mA range a resistor limiter would introduce a too high voltage drop at normal operation and would be hard to detect. A solution is then to us a fold-back current limiter like the one proposed by Henkel [45] which consists of a comparator and a series transistor as seen in figure 4.10. The advantage of this circuit is that it will only create a drop of 200 mV at 100 mA between the supply and the load.

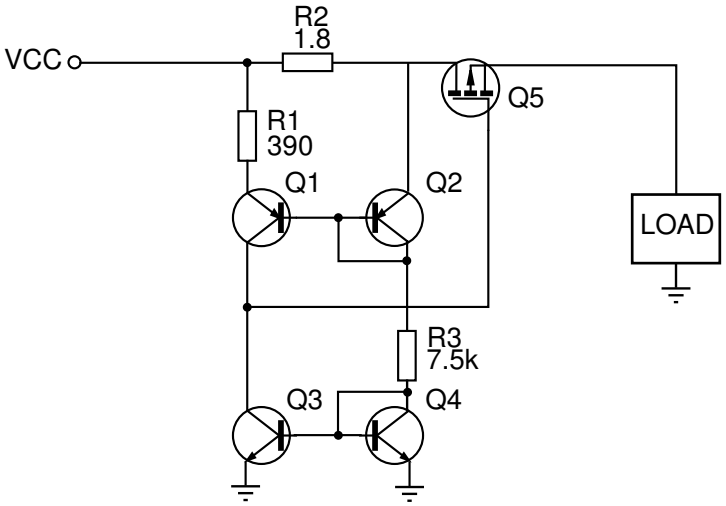


Figure 4.10: *Schematic for a SEL prevention circuit [45]. Recreated for eligibility.*

Chapter 5

Facility description and setup

The SRAMs were tested at PTB in Braunschweig Germany, CERF at CERN, at The Oslo Cyclotron Laboratory and at IFE at Kjeller. This chapter will provide an overview of the different test setups used, with an added focus to the beam line monitoring and calibration.

5.1 Irradiation testing

As there are three main energy regions of interest for a neutron detector, namely thermal neutrons, fast neutrons below 20 MeV and high energy hadrons above 20 MeV, a range of facilities for testing should be used to cover the different types of radiation. A requirement for the facility is that it can provide an accurate characterization of the beam profile, so that the beam is known to be covering all of the sensitive area of the detector, and a calibrated monitoring of the beam during irradiation so that the beam flux can be known.

Careful planing needs to be done in advance to avoid beam time loss. The preparations include acquiring all equipment needed for testing in addition to spares for critical components. It is best to be self sufficient in regards to the equipment as it is not always certain what equipment is available at the irradiation facility. A detailed plan on the arrangement and positioning of the setup should be conducted in advance to detect any difficulties which would require bringing additional equipment not normally used in the setup.

The procedure for testing can be as follows; 1) Install equipment needed for testing. 2) Calibrate and characterize the beam. 3) Mount the device to be tested in the beam. 4) Irradiate device for the wanted amount of time and monitor the device during the irradiation. 5) Change device, settings, voltages etc. and repeat from 3.

5.2 Physikalisch-Technische Bundesanstalt

The Physikalisch-Technische Bundesanstalt (PTB) facility in Braunschweig Germany has the possibility to create quasi-mono-energetic neutron beams of 5.77 MeV and 8.5 MeV from deuteron induced reactions on a gas target $^{2}\mathrm{H(d,n)}^{3}\mathrm{He}$ or 14.8 MeV with a Van-de-Graaff and a tritium target $^{3}\mathrm{H(d,n)}^{4}\mathrm{He}$ [46]. To achieve higher beam intensities the target is wobbled. The experimental hall where the irradiation took place has the dimensions of $\mathrm{V} = 25\,\mathrm{m} \times 30\,\mathrm{m} \times 14\,\mathrm{m}$ and contains a steel grated floor with another level 4.5 m below [47]. Due to it's large size, the scattering from the concrete walls are low.

5.2.1 Purpose of tests

The purpose of the testing at PTB was to :

- Test if the devices are sensitive to fast neutrons at all.
- Investigate the dependency of the cross section on the energy of the incoming neutrons.

5.2.2 Experimental setup

Beam monitoring

For monitoring of the neutron fluence during a run a Precision Long Counter (PLC) was used. The PLC consists of a long BF_3 proportional counter placed inside a large, specially shaped, moderating cylinder made of polyethylene, boron loaded polyethylene, aluminum and cadmium. It is placed at a distance of about 5.5 m from the target, at an angle of 100° [46]. Also available was a New Monitor (NM), a ^{3}He proportional counter and a Geiger-Müller counter. These were not used as they were obstructed by our test device.

To accurately find the neutron spectra for each new run at a new energy, and to calibrate the PLC and the other monitors, a proton recoil proportional counter and proton recoil telescope was used. After calibration they were removed again before the other measurements started. See figure 5.1 for placement.

The number of counts in a PLC is proportional to the neutron fluence per steradian:

$$\Phi_{sr} = N_{PLC} \cdot C_{PLC} \tag{5.1}$$

Where N_{PLC} is the number of counts in the PLC and C_{PLC} is the calibration factor for the PLC at the current run. This can be converted to neutron fluence per cm^2 for a given distance from the definition of the steradian, details are given in appendix B.

$$\Phi(d) = \frac{N_{PLC} \cdot C_{PLC}}{\pi(d \cdot \tan(\theta))^2} \tag{5.2}$$

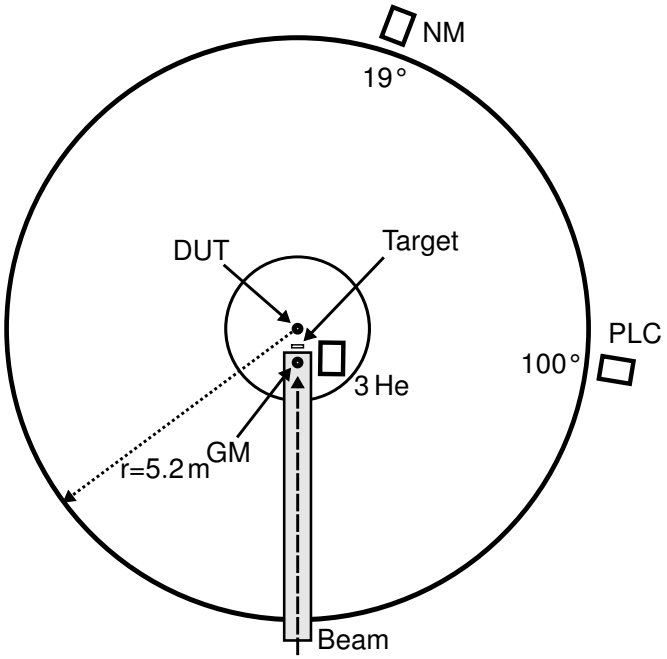


Figure 5.1: *Schematic setup of the different reference detectors.*

Where d is the distance from the target to the Device Under Test (DUT) and θ is a constant.
Below in table 5.1, the calibration data for the 5 runs are summarized. For a complete listing of calibration data see appendix A.

Run #	$\langle E_n \rangle$ [MeV]	Reaction	E_p [MeV]	I [µA]	PLC [1/sr]	ΔPLC [%]
1	8.5	^{2}H(d,n)^{3}He	5.63	1.7	6.888E5	1.03
2	5.77	^{2}H(d,n)^{3}He	2.95	1.5	4.982E5	0.93
3	8.5	^{2}H(d,n)^{3}He	5.61	1.6	5.487E5	0.93
4	5.77	^{2}H(d,n)^{3}He	2.91	1.4	4.732E5	1.11
5	14.5	^{3}H(d,n)^{4}He	0.215	6.2	1.029E5	1.95

Table 5.1: *Summarized calibration data from 5 runs at PTB. E_n is the nominal neutron energy, E_p is the energy of the projectile, I is the ion current, PLC is the amount of counts on the Precision Long Counter and ΔPLC is the uncertainty in the PLC counts.*

Devices Under Test

Two different SRAM devices were tested at PTB, one 16 Mbit and two 1 Mbit, all manufactured by Cypress. Specifications are listed in table 5.2.

The SRAMs were all mounted to the front side of the RadMon boxes [1] from the CERN group, which were tested in parallel with our devices. The CERN group also

provided the mounting stand which could be mounted to the stand provided by PTB.

Nr.	Part number	Date code YYMM	Die rev.	Tech. [nm]	Speed [ns]	Size [Mbit]	Voltage [V]
1a	CY62127DV30LL-55ZXI	0737	D	130	55	1	2.5
1b	CY62127DV30LL-55ZXI	0737	D	130	55	1	2.4
2a	CY62167DV30LL-55ZXI	0825	D	150	55	16	2.6
2b	CY62167DV30LL-55ZXI	1001	D	150	55	16	2.4

Table 5.2: *List of SRAM devices tested at PTB, note that SRAM2b was never tested as it malfunctioned before testing commenced.*

DUT setup

To decide at which position to place the DUT from the exit of the beam pipe, calibration measurements at two downstream positions, 20 cm and 30 cm, and at two angels, 0°/13° and 0°/8° respectively, were completed by the PTB staff before our arrival. As can be seen from table 5.3 a greater uniformity of the beam is found in the most downstream position.

An angle of 8° at 30 cm corresponds to a beam diameter of 84 mm. This is a bit less than the needed minimum distance between the outermost SRAM devices of the RadMon boxes of 90 mm and also for our SRAM devices, but assuming that the die of the SRAMs doesn't extend to the edges of the package and the decrease in beam flux from 84 mm to 90 mm is small, an error of 10% can be considered at this position.

The size of the dies of the SRAMs have later been measured to be 2.0 mm×2.5 mm and 6.3 mm×7.8 mm for the 1 Mb and 16 Mb respectively. A picture of the setup is shown in figure 5.2, the dimension and placement of the SRAM dies and the relative size of the beam spot for 90 mm and 84 mm is shown.

Location	Angle [°]	Radius [cm]	Distance [cm]	Flux [φ] 5 MeV	Flux [φ] 8 MeV	Ratio edge/center 5 MeV	Ratio edge/center 8 MeV
Center	0	0	20	1.1×10^5	3.3×10^5	0.8	0.8
Edge	13	4.6	20	8.7×10^5	2.6×10^5		
Center	0	0	30	4.8×10^4	1.4×10^5	0.9	0.9
Edge	8	4.2	30	4.4×10^4	1.3×10^5		

Table 5.3: *Neutron flux for two downstream positions at two different angels.*

Equipment setup

The main readout functionality of the setup used at PTB has already been presented in chapter 4. A diagram of the setup can be seen in figure 5.3.

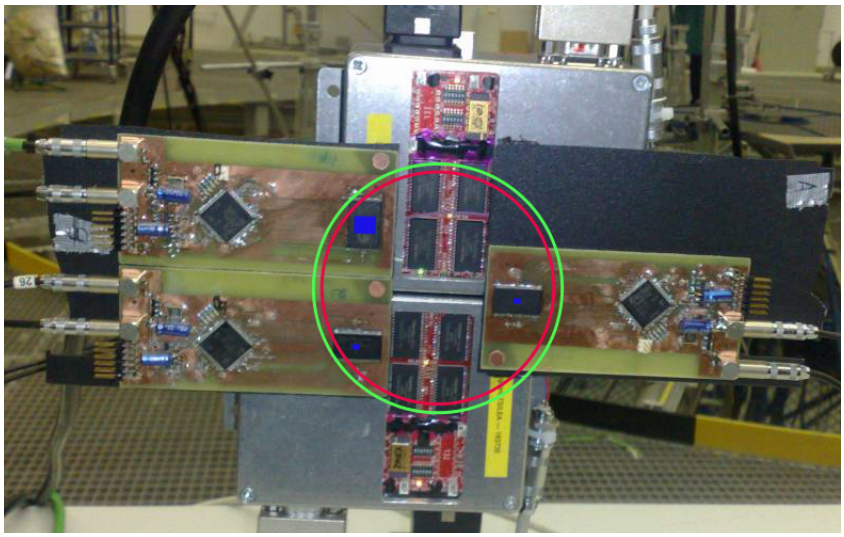


Figure 5.2: *Photograph of the setup of the SRAMs and RadMon boxes. The green circle indicates the 90 mm diameter, the red circle indicates the 84 mm diameter. The blue squares indicate the size and placement of SRAMs' die. Top left is SRAM2b, bottom left is SRAM1a, right is SRAM1b. SRAM2b was exchanged with SRAM2a when doing the irradiation testing. SRAM2a has a circuit board with a narrower width which makes it come closer to the center of the beam.*

The BNC cables for connecting power and telemetry to the DUTs were provided by PTB and part of their existing cabling setup. The cables seemed to have a termination along the way which dropped our signaling from the DUTs from 3.3 V to 1.5 V which is the same as the threshold voltage of the Ortec 973A 3 channel 100 MHz counter [48]. To be on the safe side a level converter was used in between.

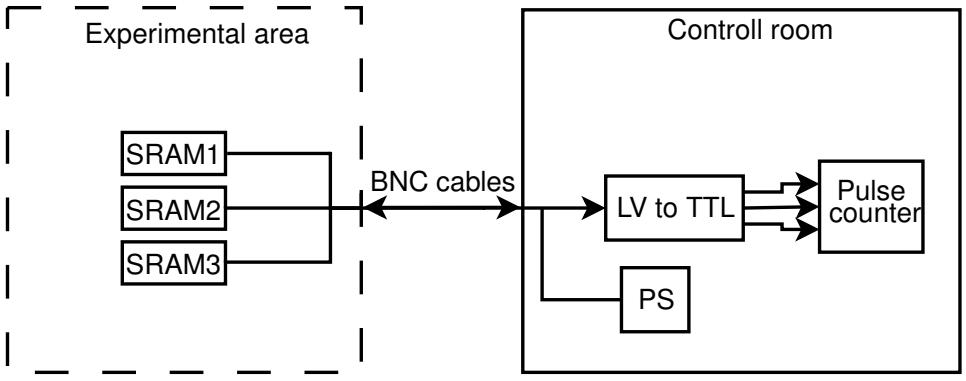


Figure 5.3: *Schematic setup of the the equipment used at PTB.*

5.3 CERN-EU High Energy Reference Field

The CERN-EU High Energy Reference Field (CERF) facility is located on the North Experimental Area on the Prévessin site of CERN in France and is connected to one of

the secondary beam lines (H6) from the Super Proton Synchrotron (SPS).

A positively charged hadron beam (a mixture of protons, kaons and pions) with momentum of 120 GeV/c hits a copper target, 50 cm thick and 7 cm in diameter [49]. This creates a wide energy spectrum from thermal neutron to hadrons of up to 1 GeV. A plot of the neutron energy spectra can be seen in figure 5.5.

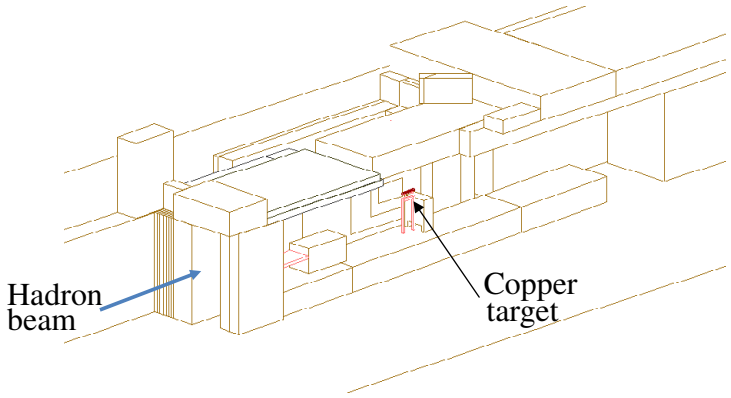


Figure 5.4: *Layout of the experimental bunker at CERF as modeled in FLUKA [50].*

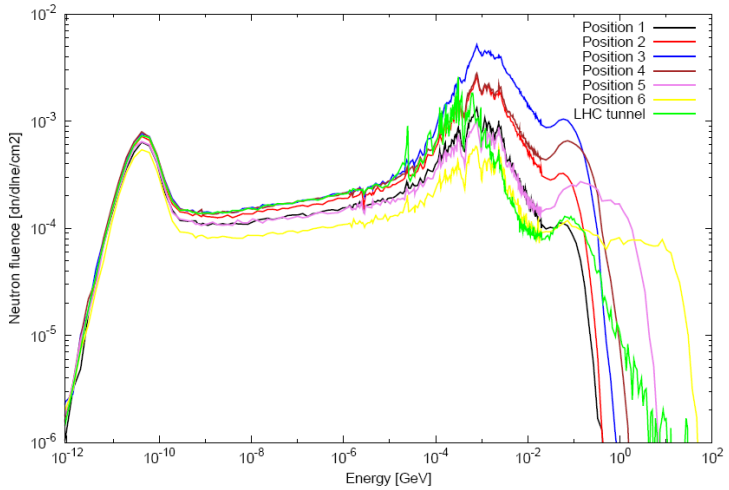


Figure 5.5: *Neutron energy spectra for the experimental bunker at CERF as calulated by FLUKA [50]. The placement of the positions mentioned in the plot can be seen in figure 5.6.*

5.3.1 Purpose of tests

The purpose of the testing at CERF was

- Test the new measurement setup.
- Compare the new SRAM3 device against the other two types.
- Check some anomalies for the data collected for SRAM2 at PTB.
- Try to compare the collected data with data from PTB.

5.3.2 Experimental setup

Beam monitoring

The intensity of the incoming beam is monitored by an air filled Precision Ionization Chamber (PIC) placed upstream, not far from the copper target. A count is scored when the charge created from the ionization of the beam in the volume has reached a certain value. One PIC count represents 22400±10 % particles impinging on the target.

The beam from SPS is pulsed and one pulse is referred to as a spill. During the spill the beam is constant. The spill usually lasts 10 s with a cycle of 48 s, but could be adjusted.

The flux is calculated as p.o.t/s where p.o.t. is Particles On Target = PIC counts * 22400. To find the flux at the position of the DUT a plot from a Monte Carlo simulation with FLUKA of the amount of High Energy Hadrons (HEH) around the copper target normalized to the amount of particles on target was used. See figure 5.6.

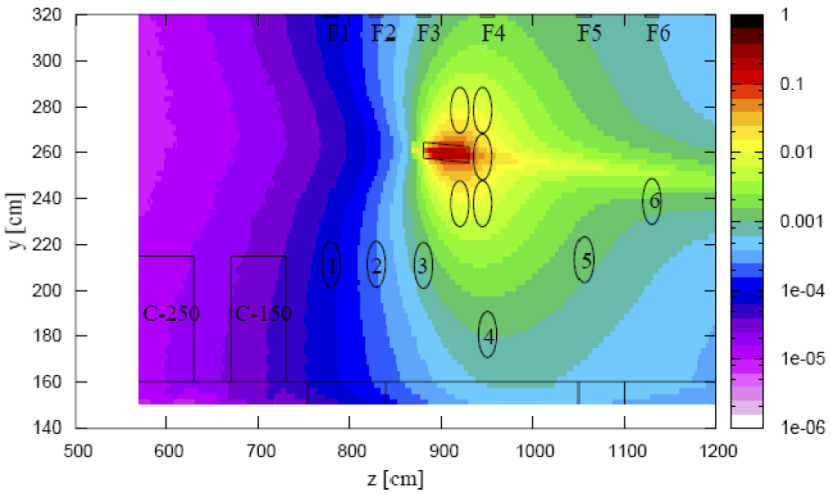


Figure 5.6: *High Energy Hadrons (HEH) fluence normalized per primary particle on target (p.o.t.) at the different mounting positions [50]. The plot is seen from below.*

Devices Under Test

The same SRAMs that were tested at PTB tested at CERF also, in addition there was a new 8 Mb Cypress device and SRAM2b, which was not tested at PTB, had been repaired. Specifications are listed in table 5.4.

DUT setup

The devices were tested at two positions, position F1 and F4 in figure 5.6. As can be seen in figure 5.7, position F4 has a large amount of HEH on the order of 10^{-3} with

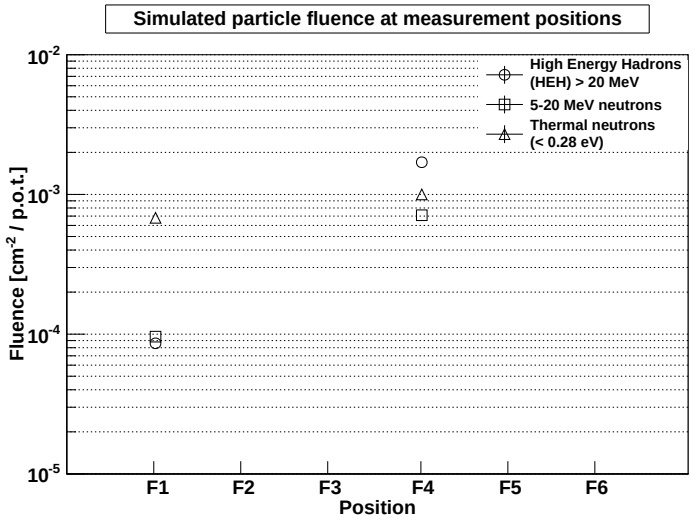


Figure 5.7: *Simulated fluence for wall positions F1 and F4. Numbers by Ketil Røed [51].*

Nr.	Part number	Date code YYMM	Die rev.	Tech. [nm]	Speed [ns]	Size [Mbit]	Voltage [V]
1a	CY62127DV30LL-55ZXI	0737	D	130	55	1	2.5
1b	CY62127DV30LL-55ZXI	0737	D	130	55	1	2.4
2a	CY62167DV30LL-55ZXI	0825	D	150	55	16	2.6
2b	CY62167DV30LL-55ZXI	1001	D	150	55	16	2.4
3a	CY62157EV30LL-45ZXI	1001	F	90	45	8	2.4

Table 5.4: *List of SRAM devices tested at CERF.*

about the same for thermal, while position F1 has an order of magnitude lower amount of HEH with only a bit lower thermal. Since the devices should have a linear response in conjunction with the fluence, a difference in cross section between the two positions for the same device should be less than an order of a magnitude if the devices are sensitive to thermal neutrons.

During the campaign it was decided not to test the two 1 Mb SRAMs (SRAM1) in the thermal position F1 because of the low amount of upsets collected in the HEH position F4. It has also previously been found by Granlund et al. [52] that they should not be sensitive to thermal neutrons.

The SRAMs were mounted to two thin plastic plates to ease the task of moving them between the two positions. The two 1 Mb SRAMs (SRAM1) were positioned on topmost board and the other three on the bottommost. As can be seen in figure 5.8 the cards were mounted with the SRAMs closest to the taped line along the wall. The line indicated the height of where the simulated fluence had been calculated.

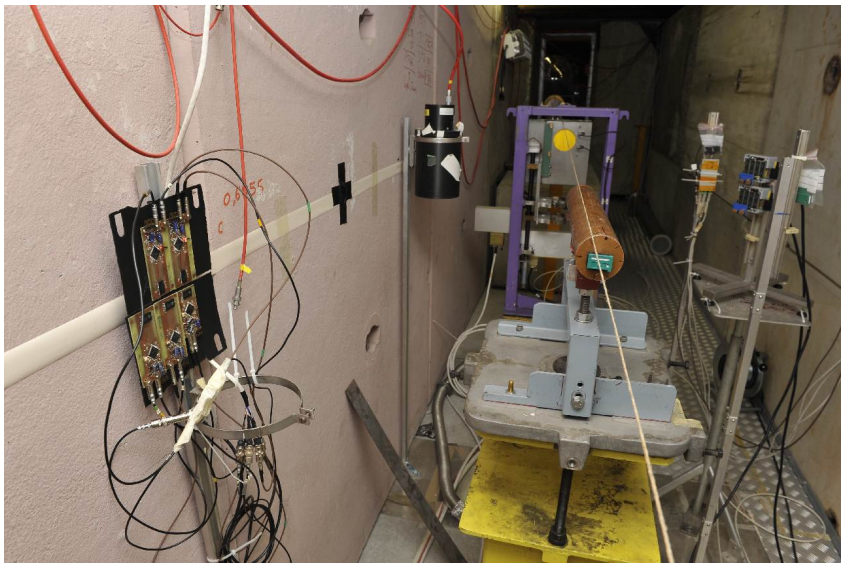


Figure 5.8: *SRAMs mounted at position F4. Cylinder on right is the copper target, thread indicates direction of incoming particles, horizontal tapelines on wall indicates the height of which the simulated fluence had been calculated.*

Equipment setup

The main readout functionality of the setup used at CERF has already been presented in chapter 4. A diagram of the setup can be seen in figure 5.9.

The computer used for readout of the SEUs from the SRAMs was placed in an area right outside the bunker. Due to radiation levels above the normal background level in this area, only physical configurations of the setup was done there. The computer used for readout was controlled from a remote desktop application from the control room further away.

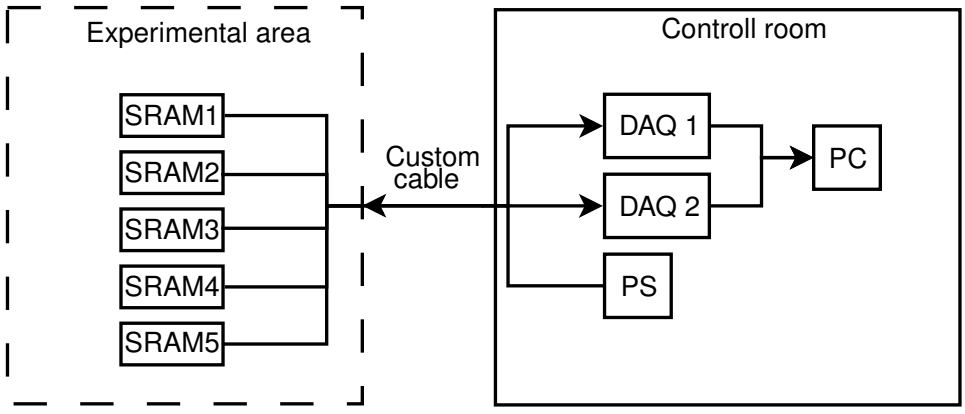


Figure 5.9: *Schematic setup of the the equipment used at CERF.*

5.4 Oslo Cyclotron Laboratory

Oslo Cyclotron Laboratory (OCL) is located at the Department of Physics at the University of Oslo and was built in 1978. The cyclotron is of the type MC-35 and was produced by Scanditronix AB from Sweden. It has the possibility of accelerating protons, ^{2}He, ^{3}He and ^{4}He with up to tens of MeV and intensities of up to 100 nA [53]. For this work a proton beam with an energy of 29 MeV, at the exit of the beam pipe, and an intensity in the order of hundreds of pA was used.

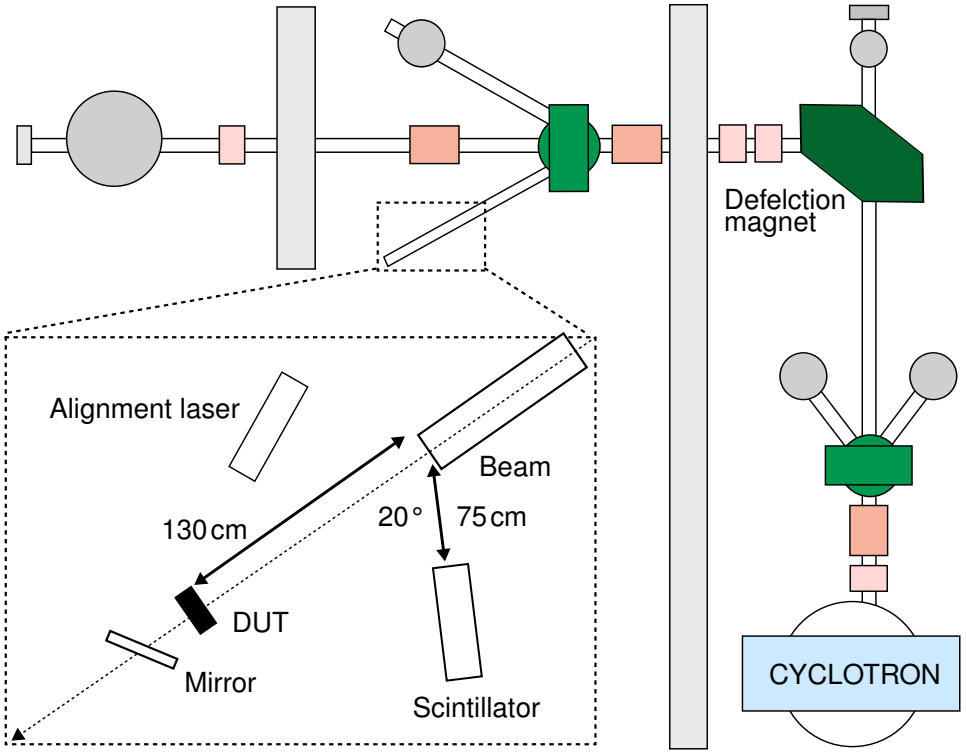


Figure 5.10: *Schematic layout of experimental area at OCL.*

5.4.1 Purpose of tests

The purpose of the testing at OCL was

- To compare the previous measurements for the devices tested at PTB and CERF with these measurements.
- Test the dependence of the cross section on the voltage. All devices were tested at three voltages corresponding to the minimum, typical and maximum operating voltage from the datasheet.
- Some of the devices have what is called data retention mode. To enable this, according to the datasheet, the device needs to be put into idle mode with the chip

enable pulled high and without any activity on its pins. Then the voltage on the device can be reduced by about one volt and the device can still retain its memory. The devices had been tested beforehand to work properly at the data retention voltage level without running in idle mode and without getting any errors. To confirm that the voltage on the SRAM cells are the same at the data retention voltage in idle and normal mode, the devices were tested in both modes and the cross section was compared.

- SEL had been seen to appear at the testing at CERF for all devices and a current monitoring system was created to check for current increases caused by latchups.
- Sudden increases of more than 100 counts in a few seconds had been seen to occur on SRAM3 at CERF. SRAM3 uses a 90 nm technology and as opposed to 130 nm and 150 nm on SRAM1&2. A wider test to check if the increases were related to SEL, readout functionality or the specific technology was done by testing other devices in various technology nodes and adding current measurements. The new PCBs and the upgraded firmware for the new PCBs should change the behavior if it was related to the readout.
- Test the newly created PCBs and accompanying SRAMs.

5.4.2 Experimental setup

Beam setup

The laboratory is divided into three rooms, two experimental areas and one control room. The cyclotron is contained in the innermost experimental area. The layout can be seen in figure 5.10.

The direction and uniformity of the beam can be controlled by moving four collimators, positioned in the vacuum chamber at the end of the beam pipe, through remote control. This vacuum chamber also contains a Faraday Cup (FC) which can be moved into the beamline and effectively stops the beam from exiting to the outer experimental area. This makes it possible to work in the outer experimental area without shutting down the cyclotron completely.

To set up the positioning of the beam at the position of the DUT, a fluorescent ceramic plate is mounted in the position where the DUT should be. The ceramic plate is positioned in the center of the beam by the use of a laser which is positioned so that it hits the center of the beam pipe exit point at approximately 0° horizontal and vertical angle via a mirror positioned on the end of the mounting rail going out from the beam pipe (see figure 5.10). The ceramic plate has a crosshatch in the same position on the back and on the front and is positioned with the laser hitting the center of the crosshatch. By using a CCD camera aimed at the ceramic plate, it is now possible to see the position and physical shape of the beam from the control room.

Due to the weak fluorescence of the ceramic plate at lower intensities, the beam profile could not be determined accurately only from observing the ceramic plate. For

previous radiation tests at OCL by other students from the University of Bergen [54, 55, 56] a Thin Film Breakdown Counter (TFBC) with a known proton sensitivity had been used to find the beam profile. Unfortunately this TFBC was not available for our tests. Instead we chose to use one of the 1 Mb SRAMs (SRAM1) which we previously had calibrated at PTB with 14.8 MeV neutrons for determining the beam profile and for calibrating a scintillator used for beam monitoring during irradiation runs.

The SRAM was first calibrated for 28 MeV protons with the FC as a reference close to the exit of the beam pipe, see appendix C for details of calibration. When the ratio between the number of SEUs in the SRAM and the fluence was known, a scintillator positioned in an angle from the beam exit was calibrated with the SRAM as a reference. The scintillator was then used to measure the fluence during the runs.

To determine the profile of the beam, the 16 Mb SRAM (SRAM2) was mounted in the position of where the DUT should be. The 16 Mb was now used because of its larger memory size which makes the accumulation of SEU counts faster and thus reduces the time needed for each run to collect sufficient statistics. The 16 Mb SRAM was moved in the X- and Y-direction in 2.5 mm steps and at each step the number of SEUs were recorded. From this a plot can then be constructed which gives an indication of were the center of the beam was.

The beam profile had to be determined at the start of each day as the cyclotron was shut down during non working hours.

Beam monitoring

The usual way of monitoring the beam intensity at OCL is to use a 3 cm FC connected to a Keithley 610C amperemeter and mounted behind the DUT. But, due to the low intensity we were running the beam at, a great contribution to the measured current in the FC would come from electrons generated from ionization of the air and from hitting our DUT [54]. This made the stability and uncertainty in the FC measurements too large for practical use. As stated before a scintillator was instead used for online monitoring of the beam.

Devices Under Test

In addition to the detectors previously tested at CERF there were now nine new detectors with devices of different feature sizes, voltages, makes and models. The new detectors all had the 2nd generation of the PCB which adds the possibility of up to 4 SRAMs, but only one was mounted to each PCB as the beam width wasn't big enough to cover more than one SRAM.

Specifications for all devices are listed in table 5.5.

DUT setup

Each PCB containing one SRAM got a cross marked on the backside of the PCB where the center of the SRAM was located on the front-side. Then depending on where the

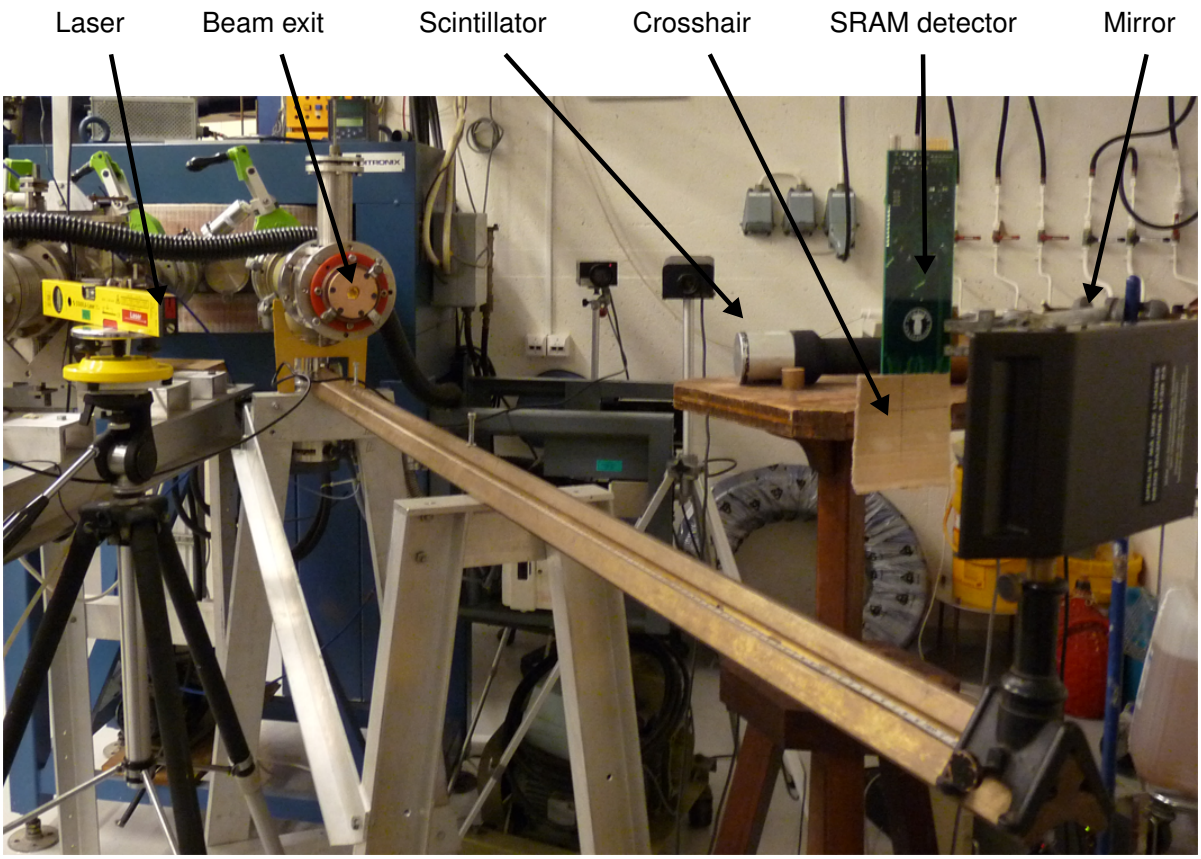


Figure 5.11: *Overview of setup at OCL.*

Nr.	Part number	Date code YYMM	Die rev.	Tech. [nm]	Speed [ns]	Size [Mbit]	Voltage [V]
1a	CY62127DV30LL-55ZXI	0737	D	130	55	1	1.5 2.5 3.3
1b	CY62127DV30LL-55ZXI	0737	D	130	55	1	1.5 2.4 3.3
1c	CY62127DV30LL-55ZXI	0737	D	130	55	1	1.5 2.4 3.4
2b	CY62167DV30LL-55ZXI	1001	D	150	55	16	1.5 2.4 3.3
2c	CY62167DV30LL-55ZXI	1001	D	150	55	16	1.5 2.4 3.4
3b	CY62157EV30LL-45ZXI	1001	F	90	45	8	1.2 2.4 3.4
4	CY62187EV30LL-55BAXI	0925	F	90	55	64	1.5 2.4 3.4
5	BH616UV8010TIG55	0805		na	55	8	1.0 2.4 3.3
6	CY7C1426JV18-300BZXC	0907	Z	90	3.3	36	1.5 1.8 na
7	IS61WV5128BLL-10TL	0948		130	10	4	1.3 2.4 3.3
8	IS61LPS51236A-200TQLI	0937		na	5	18	2.5 3.0 3.4
9	CY62147EV30LL-45ZSXI	1007	F	90	45	4	1.5 2.4 3.4

Table 5.5: *List of SRAM devices tested at OCL. Devices 1a,1b and 2b were used for calibration and beam-profile measurements on the first trip to OCL and were replaced by the equivalent 1c and 2c when doing other tests. The voltage on the SRAM could be changed in three steps, low, normal and high.*

center of the beam was found to be from the beam profile, a new mark was made to the backside indicating the point where the laser should be aimed. The device was positioned in the beam path at about 130 cm by the use of a movable clamp. See figure 5.11 for an overview.

Equipment setup

The main readout functionality of the setup used at OCL has already been presented in chapter 4. A diagram of the setup can be seen in figure 5.12.

The computer used for reading out the SEUs from the SRAM was placed in the experimental area beside the beamline. There was some spare cables available which went to the control room and there was also some spare room in the cable conduits which we could have used for pulling our own cable, but it was deemed more efficient and less error prone to have the computer and equipment permanently in one place inside during the experiment. If more protection for the equipment would be wanted, it could be placed behind a shielding wall a few meters further away. A remote desktop was used for external monitoring during the experiments.

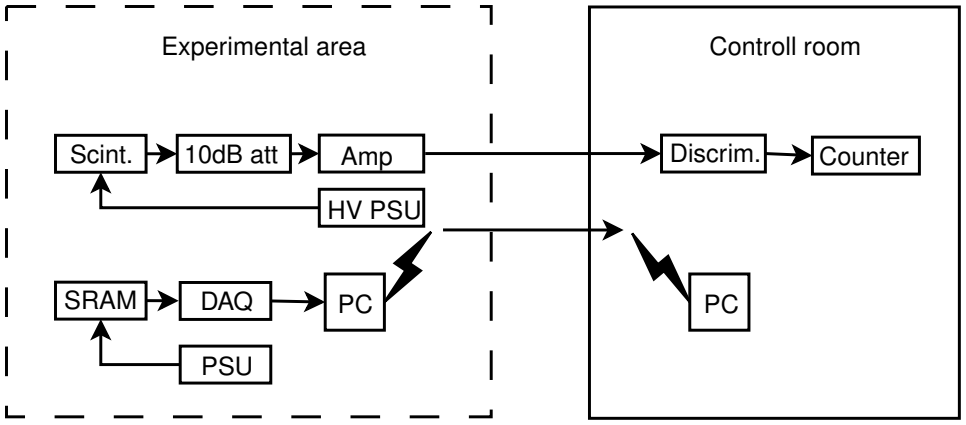


Figure 5.12: *Schematic setup of the the equipment used at OCL.*

The scintillator was placed as seen in figure 5.11. It contains a Harshaw 12S12/3 NaI(Tl) 3" scintillator crystal. The scintillator was connected to the preamplifier through a Telonic 10 dB attenuator. Without the attenuator the preamplifier would go into saturation. The preamp was a Ortec 672 Spectroscopy Amplifier set at lowest gain. This was further connected to a Ortec CF8000 Octal Constant-Fraction Discriminator for setting of the discrimination level. The counts from the scintillator was recorded by a CAEN N145 Quad Scaler and Preset Counter-Timer which also provided a timed stop of the counting. The scintillator was biased from a high voltage power-supply set at 650 V. The schematic of the setup can be seen in figure 5.12.

5.5 Institute for Energy Technology

The research reactor JEEP II at the IFE at Kjeller is a heavy water reactor [57]. It has a power output of 2 MW and uses low-enriched Uranium-235 in the form of uranium dioxide as fuel. The generated heat is transported through a heat exchanger to a secondary water-based central-heating system which heats some of the nearby research buildings. The core is moderated by heavy water and is connected to a pool of normal water through a horizontal tunnel separated by a steel plate. The tunnel begins where the thermal neutron flow is at its highest inside the core providing a relatively high thermal neutron flux in the outer pool.

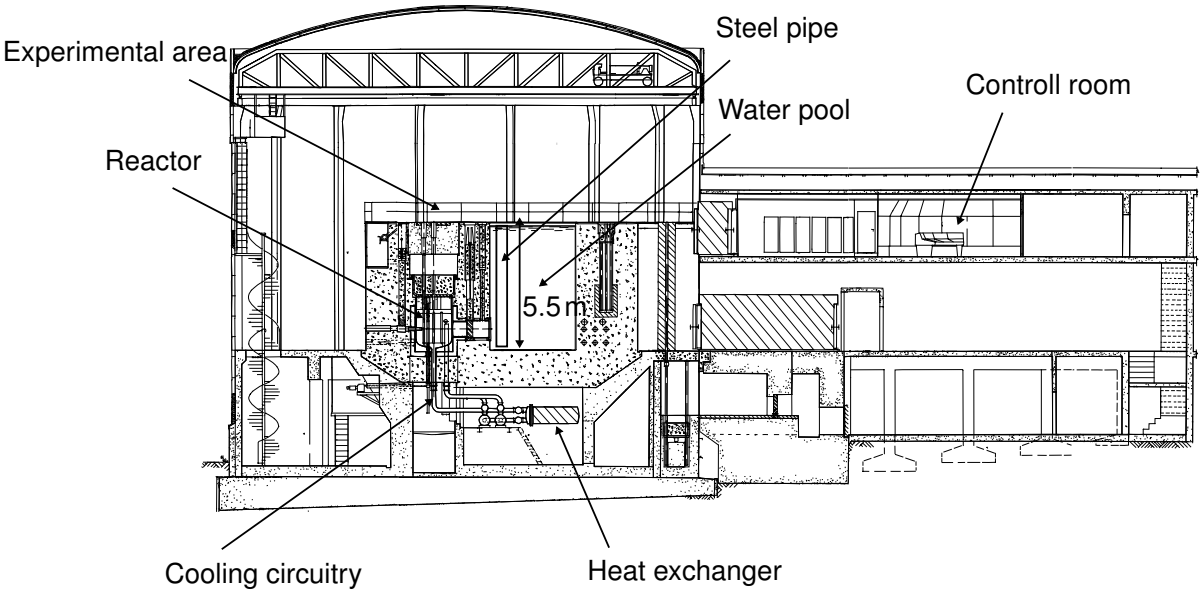


Figure 5.13: *Overview of the JEEP II reactor at IFE [57].*

5.5.1 Purpose of tests

The purpose of the testing at IFE was to

- Determine the thermal cross section for all the devices.
- Check if the cross section for thermal neutrons also have a voltage dependence.
- Investigate if the large jumps in the count rate of the 90 nm devices are also seen at thermal energies.

5.5.2 Experimental setup

Beam monitoring

The flux was measured by gold activation by the staff at IFE at the point where the device was placed. The flux was said to be constant as long as the reactor was running at full operation, also between shutdowns and restarts.

Devices Under Test

Mostly the same devices as tested at OCL was also tested at IFE, specifications are listed in table 5.6. Most of the detectors got fitted with up to 3 extra SRAMs of the same type.

Nr.	SRAM nr.	Part number	Date code YYMM	Die rev.	Tech. [nm]	Speed [ns]	Size [Mbit]	Voltage [V]
1c	1-4	CY62127DV30LL-55ZXI	0737	D	130	55	1	1.5 2.4 3.4
2d	1-4	CY62167DV30LL-55ZXI	1013	D	150	55	16	1.3 1.5 2.4 3.4
3b	1, 3 2, 4	CY62157EV30LL-45ZXI	1031 1001	F	90	45	8	1.3 1.2 2.4 3.4
4	1	CY62187EV30LL-55BAXI	0925	F	90	55	64	1.3 1.5 2.4 3.4
5	1, 2	BH616UV8010TIG55	0805		na	55	8	1.0 2.4 3.3
7	1 2-4	IS61WV5128BLL-10TL	0948 1017		130	10	4	2.4 3.3
8	1	IS61LPS51236A-200TQLI	0937		na	5	18	1.3 2.5 3.0 3.4
9	1 2-4	CY62147EV30LL-45ZSXI	1019 1007	F	90	45	4	1.3 1.5 2.4 3.4

Table 5.6: *List of SRAM devices tested at IFE. The voltage on the SRAMs could be changed in up to four steps, extra low, low, normal and high. Detector 1c, 2d, 3b, 7 and 9 were fitted with three more SRAMs, detector 5 with one more.*

Equipment and DUT setup

A 3" steel pipe, extending almost to the bottom of the pool, was used for the measurements. The pipe was placed 49 cm from the edge of the pool nearest the core and 130 cm from the left edge from the core's perspective. The length of the pipe was about 5.5 m and the detector was placed 5 cm above the bottom on a piece of Styrofoam. The purpose of the Styrofoam was to get the detector to stay in a more or less upright position and to avoid bumping it in the bottom when lowering it down. To avoid short circuiting the detector to the steel pipe, the detector was placed inside an anti-static bag. The direction of which the SRAM was facing, was not always consistent between the test of different detectors, as the detector tended to turn with the twists of the cable when lowered to the bottom of the pipe. A drawing of the set up can be seen in figure 5.14. The readout computer was placed on a table beside the pool.

For two runs with SRAM2d a 1.3 mm cadmium foil was wrapped around the detector to shield it from thermal neutrons below the cadmium cut-off energy of about 0.5 eV.

The difference in count rate would then indicate the detectors sensitivity to pure thermal neutrons and the amount of neutrons in the epi-thermal and higher energy range.

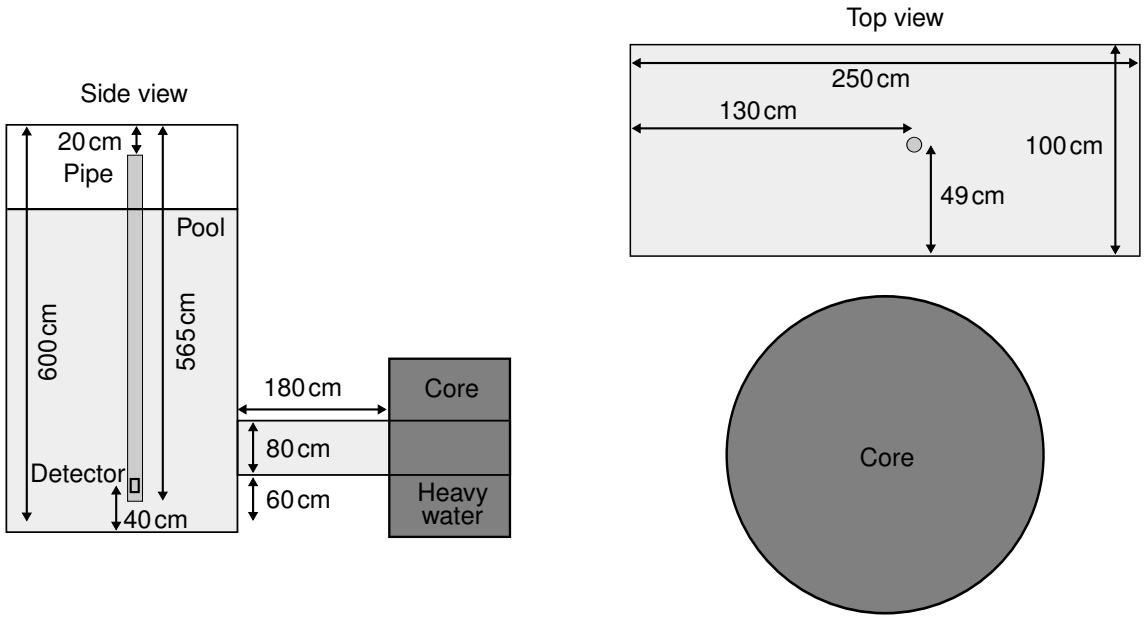


Figure 5.14: *Drawing of the placement of the detector in the pool. Not to scale.*

Chapter 6

Analysis and results

This chapter presents the results from all the irradiation tests outlined in the previous chapter.

6.1 Accelerated neutron-beam testing at PTB

The data was recorded between 14–18 of July 2010. Table 6.1 provides a summarized list of the fluence and SEUs detected for all the runs at PTB. For more details and a complete table, see D.1.

The runs listed with zero fluence for a given detector indicates that the detector was not in place for the specified run. Run 9 was done with the detectors facing in the opposite direction and the beam hitting them from the back.

Run	E_n	SRAM 1a		SRAM 1b		SRAM 2a	
	[MeV]	Φ [n/cm^2]	SEUs	Φ [n/cm^2]	SEUs	Φ [n/cm^2]	SEUs
1	8.5	2.6×10^8	5	2.6×10^8	7	0	0
2	8.5	5.2×10^8	15	5.2×10^8	8	0	0
3	5.7	2.4×10^9	26	0	0	0	0
4	8.5	2.5×10^9	39	2.5×10^9	40	0	0
5	8.5	4.4×10^9	89	4.4×10^9	80	4.4×10^9	65
6	8.5	4.0×10^9	14	4.0×10^9	7	4.0×10^9	4
7	5.7	2.6×10^9	16	2.6×10^9	22	2.6×10^9	9
8	14.8	1.4×10^9	83	1.4×10^9	91	1.4×10^9	54
9	14.8	6.5×10^8	6	6.5×10^8	14	6.5×10^8	8
10	14.8	0	0	0	0	1.2×10^9	57

Table 6.1: *Summary table of data from runs completed at PTB. On run 9 the devices are positioned in the opposite direction.*

6.1.1 Analysis of data

As SRAM1a and SRAM1b are both the same device and from the same production batch, the number of counts for each of them will be added together to get sufficient statistics. The cross section is then determined by weighted mean :

$$\sigma_{\mathrm{n}} = \frac{\sum \frac{1}{\sigma_{\sigma_{\mathrm{i}}}^2} \sigma_{\mathrm{i}}}{\sum \frac{1}{\sigma_{\sigma_{\mathrm{i}}}^2}} \tag{6.1}$$

Where σ_i is the cross section for one run of a device and σ_{σ_i} is the uncertainty in the cross section for that particular run.

Uncertainties

A number of uncertainties are present in the measurement :

- The beam coverage was estimated to have an uncertainty of 10 % (σ_{BU}) as mentioned in 5.2.2. This was also confirmed by further testing from the RadMon people who accompanied us on the measurements [58].
- Since the number of SEUs detected in the device is random in time and linearly dependent on the amount of incoming particles, its uncertainty is given by the Poisson distribution and is $\frac{1}{\sqrt{\mathrm{N_{SEU}}}}$.
- The positioning of the device from the exit of the beam (σ_d) has an uncertainty of 0.5 cm. From the beam-profiles in D.3 this can be seen to introduce a change in intensity of about 5 %.
- The uncertainty in the calibration constant for the PLC ($\mathrm{C_{PLC}}$) is given in the calibration reports listed in appendix A. It varies between 1 % to 2 %.

The uncertainty of the cross section is determined from the propagation of errors :

$$\sigma_\sigma = \sqrt{(\frac{1}{\sqrt{\mathrm{N_{SEU}}}})^2 + \sigma_{\mathrm{BU}}^2 + (\frac{2\sigma_{\mathrm{d}}}{\mathrm{d}})^2 + \sigma_{\mathrm{C}}^2} \tag{6.2}$$

6.1.2 Results

Table 6.2 and table 6.3 lists the SEU cross section per bit and its associated error for each device at three energies tested. Figure 6.1 shows the relationship between the cross section at different energies for both types of devices. A difference of 23 times can be seen between SRAM1a/b and SRAM2a at 14.8 MeV. This has later been found to be caused by a bad firmware on SRAM2a. Four of the address lines were found not to toggle, giving a loss in bit-size of the device of $2^4 = 16$. This is still a bit low compared

to data from OCL. The data is included here for references sake, a final correction factor have not been determined.

Figure 6.2 shows the number of SEUs versus the fluence for SRAM1a and 1b combined at 8.5 MeV. The number of counts is seen to be linearly dependent on the fluence as it is supposed to due to the random nature of the occurrence of SEUs.

The cross section for SRAM1a/b has been found by Granlund et al. [52] to be $3.80 \times 10^{-14}\,\mathrm{cm}^2$/bit in a wide spectrum neutron beam extending from 1 MeV to 400 MeV. Assuming this is the saturation cross section, it is a bit lower than the $5.8 \times 10^{-14}\,\mathrm{cm}^2$/bit that we got at 14.8 MeV, which should be close to the saturation cross section. But given that they tested the device at 3.0 V, in contrast to the 2.5 V we tested it at, which would give them a lower cross section [19] and given the property of their neutron beam, the values can be said to be comparable.

Energy [MeV]	SEU	Φ [n/cm^2]	$\sigma_{SEU,n}$ [cm^2/bit]	σ_σ [cm^2/bit]
5.8	64	3.79×10^9	8.06×10^{-15}	1.3×10^{-15}
8.5	304	8.10×10^9	1.78×10^{-14}	2.1×10^{-15}
14.8	174	1.42×10^9	5.81×10^{-14}	7.5×10^{-15}

Table 6.2: *Measured cross sections at the different energies for SRAM1a and 1b combined.*

Energy [MeV]	SEU	Φ [n/cm^2]	$\sigma_{SEU,n}$ [cm^2/bit]	σ_σ [cm^2/bit]
5.8	9	2.58×10^9	2.08×10^{-16}	7.3×10^{-17}
8.5	69	4.84×10^9	8.50×10^{-16}	1.3×10^{-16}
14.8	111	2.60×10^9	2.54×10^{-15}	3.6×10^{-16}

Table 6.3: *Measured cross sections at the different energies for SRAM2a.*

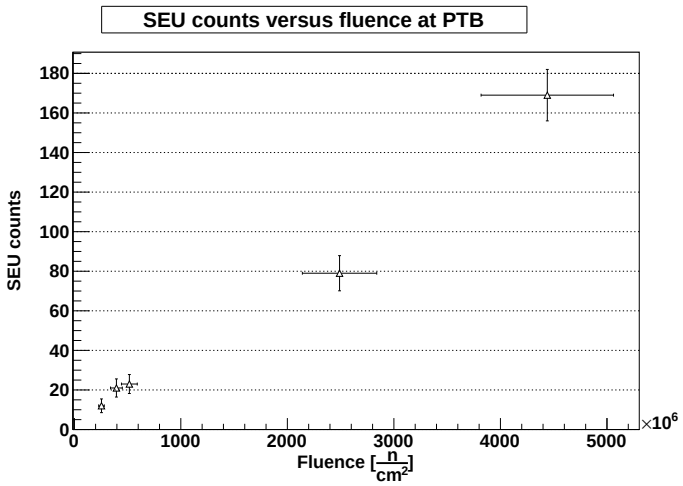


Figure 6.2: *Number of SEUs as a function of fluence at 8.5 MeV for SRAM1 and 2 combined.*

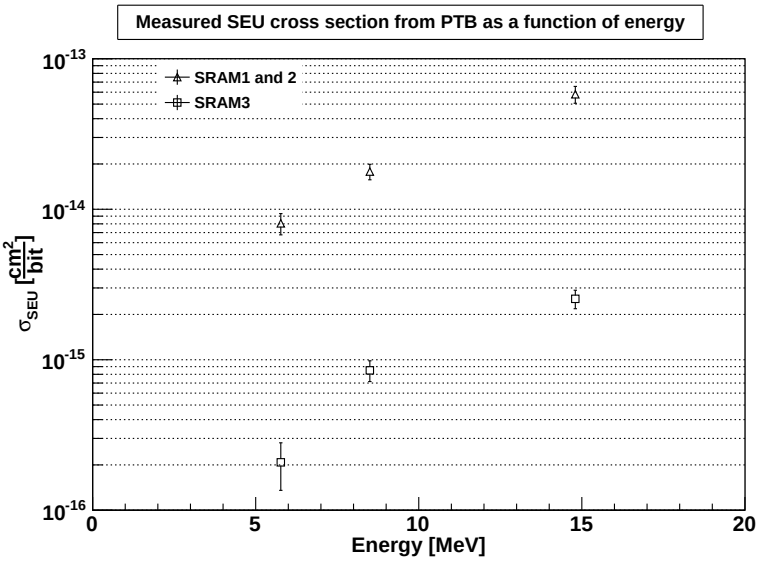


Figure 6.1: *Measured SEU cross section as a function of energy.*

On run number 9 in table 6.1 the devices were tested in the opposite direction. A difference of more than 2 was seen between front and back irradiation as seen in table 6.4. A difference of between 2 and 3 was also seen, with better statistics, by the CERN group who tested in parallel with us [58]. This has also been found by others [44, 19, 59] and can be explained by the oxide passivation layer. This is a layer of glass and silicone nitride put on top of a die after production to protect it from contamination during assembly. According to simulations presented by Wrobel et al. [59] the average recoil energy LET for n+O reactions are higher than n+Si below 50 MeV, at 14 MeV this difference reaches a factor of two. When irradiating from the back the neutrons will pass the sensitive area before interacting with the passivation layer. As the nuclear reactions with SiO_2 are mostly forward peaked, they wont reach the sensitive area and thus not contribute to the cross section.

SRAM	Front σ_{SEU} [cm^2/bit]	Back σ_{SEU} [cm^2/bit]	Ratio front/back
1a+b	$(5.81 \pm 0.75) \times 10^{-14}$	$(2.37 \pm 0.58) \times 10^{-14}$	2.5 ± 0.7
2a	$(2.54 \pm 0.36) \times 10^{-15}$	$(1.19 \pm 0.44) \times 10^{-15}$	2.1 ± 0.8

Table 6.4: *Differences between backside and front side radiation for SRAM1 and 2 at 14.8 MeV.*

6.2 Accelerated proton-beam testing at OCL

The measurements were done at two occasions, 15–18 November and 7–9 December 2010. The devices were placed at about 130 cm upstream from the beam exit. The

beam has an energy of 29 MeV at the exit of the beampipe and 26.3 MeV at the point of interaction with the DUT, as calculated by the LISE++ code [60].

Listed here are only the averaged result of all runs, see D.3 for complete tables.

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
1.5	Normal	8.26×10^{-14}	7.5×10^{-15}
2.4	Normal	5.88×10^{-14}	4.7×10^{-15}
3.4	Normal	6.52×10^{-14}	5.9×10^{-15}
1.5	Idle	6.98×10^{-14}	6.4×10^{-15}

(a) *SRAM1c*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
1.5	Normal	1.14×10^{-13}	1.3×10^{-14}
2.4	Normal	6.82×10^{-14}	7.8×10^{-15}
3.4	Normal	6.79×10^{-14}	7.7×10^{-15}
1.5	Idle	9.31×10^{-14}	1.1×10^{-14}

(b) *SRAM2c*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
3.4	Normal	1.79×10^{-13}	2.0×10^{-14}
2.4	Idle	8.65×10^{-14}	1.8×10^{-14}
3.4	Idle	7.93×10^{-14}	9.1×10^{-15}

(c) *SRAM3b*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
2.4	Normal	6.22×10^{-14}	7.1×10^{-15}
3.5	Normal	7.01×10^{-14}	1.1×10^{-14}
1.5	Idle	4.50×10^{-14}	5.1×10^{-15}
2.4	Idle	4.09×10^{-14}	4.6×10^{-15}

(d) *SRAM4*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
2.4	Normal	3.42×10^{-14}	3.1×10^{-15}
3.3	Normal	3.48×10^{-14}	4.1×10^{-15}
1.1	Idle	7.08×10^{-14}	8.1×10^{-15}
2.4	Idle	3.64×10^{-14}	4.2×10^{-15}
3.3	Idle	3.70×10^{-14}	5.8×10^{-15}

(e) *SRAM5*

Table 6.5: *Average SEU cross sections for a given voltage at OCL.*

6.2.1 Analysis of data

The fluence and cross sections in the table are the weighted mean of all the runs at the specified voltage.

Uncertainties

The uncertainties in the cross section is dependent on

- The uncertainty (σ_{ratio}) resulting from finding the ratio between the number of scintillator counts and the number of SEUs in the calibration SRAM was commonly about 10 %.

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
1.8	Normal	3.43×10^{-14}	3.9×10^{-15}

(f) *SRAM6*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
2.4	Normal	3.75×10^{-14}	3.4×10^{-15}

(g) *SRAM7*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
2.5	Normal	3.47×10^{-14}	4.0×10^{-15}
3.0	Normal	3.53×10^{-14}	4.1×10^{-15}
3.4	Normal	3.43×10^{-14}	3.9×10^{-15}
2.5	Idle	3.41×10^{-14}	5.3×10^{-15}

(h) *SRAM8*

Voltage [V]	Mode	$\sigma_{SEU,p}$ [cm^2/bit]	σ_σ [cm^2/bit]
1.5	Idle	4.02×10^{-13}	4.6×10^{-14}
2.4	Idle	4.62×10^{-13}	5.2×10^{-14}

(i) *SRAM9*

Table 6.5: *Average SEU cross sections for a given voltage at OCL.*

- The uncertainty introduced due to the nonlinear response (σ_{lin}) of the scintillator to the intensity of the beam was estimated to 10 %.
- The positioning of the device in the beam has an estimated uncertainty of 1 mm. From the beam-profile this can be found to result in a 5 % systematic error (σ_{pos}).
- The number of SEUs in the SRAMs and the number of counts in the scintillator have a statistical uncertainty given by the Poisson distribution of $\frac{1}{\sqrt{N_{SEU}}}$ and $\frac{1}{\sqrt{N_{scint}}}$.

The uncertainty of the cross section is determined from the propagation of errors.

6.2.2 Results

Figure 6.3 shows the relationship between the voltage and the cross section in idle and normal mode. The plots of SRAM6 and 7 has been left out as they were only tested in one voltage and mode.

Due to problems with SEL occurring in normal mode, some of the voltage levels could not be successfully tested on the three 90 nm devices, SRAM3b, 4 and 9. These devices are also seen to have a large discrepancy between the cross section in idle and normal mode indicating probable faults caused by SETs or upsets in the address decoding logic. The sharp increases in count rate seen for SRAM3a at CERF could not be detected properly at OCL. The high flux caused the count rate to increase beyond the maximum readout speed of the detector.

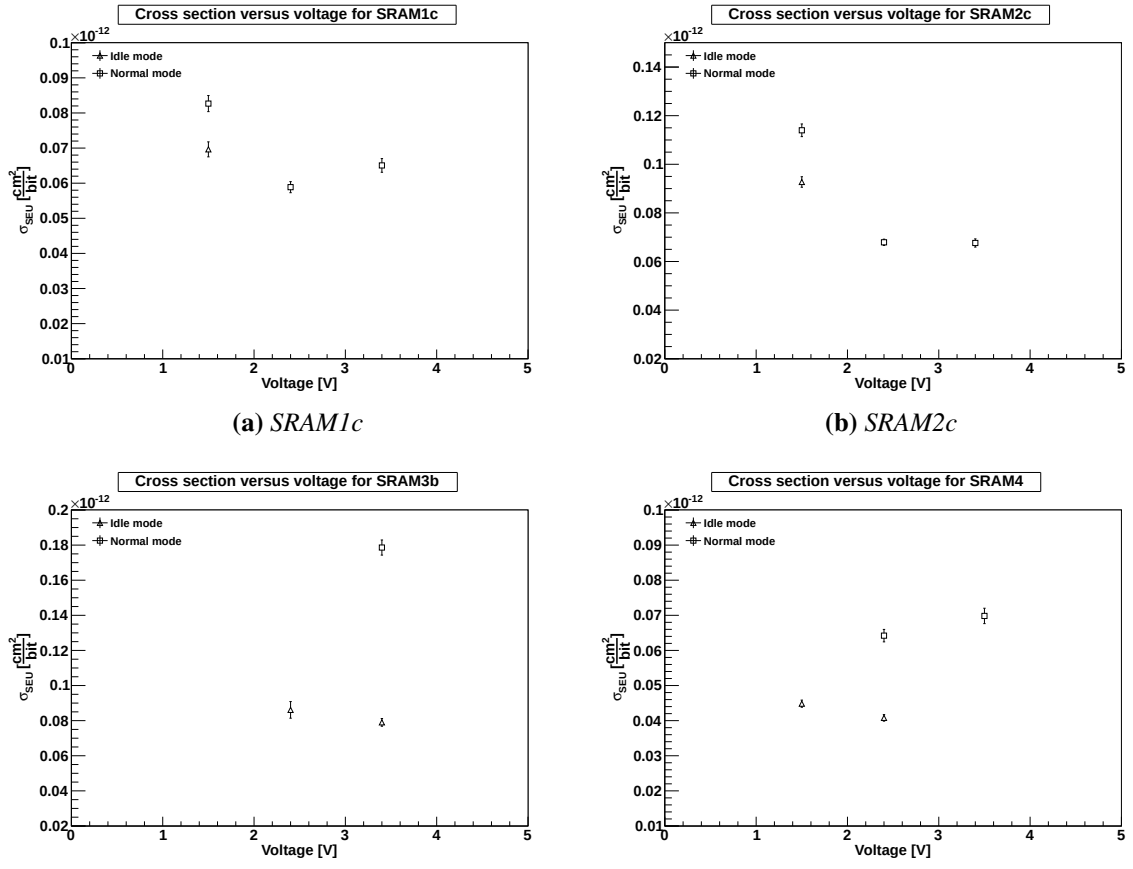
SRAM1c, 2c and 5 exhibit the expected effect of an increase in cross section at lower voltage. In retrospect, SRAM1c and 2c should have been tested in idle mode for the two higher voltages to determine if the small difference in cross section at low voltage also is present at higher voltage to disprove or confirm the presence of a voltage change

in data retention mode. SRAM5 loses its data retention if run in normal mode at low voltage and is thus only tested at idle at this voltage.

Comparison to PTB

If comparing the cross section for the 1 Mb SRAM1a+b from PTB at 14.8 MeV of $(5.81 \pm 0.75) \times 10^{-14}$ with the equivalent SRAM1c from OCL of $(5.89 \pm 0.16) \times 10^{-14}$ we can see that they are equal within the uncertainties given. The approximate equal cross sections at 14.8 MeV neutron and 26.3 MeV can be seen also in proton vs. neutron testing by Dyer et al. [61] and Lambert et al. [62].

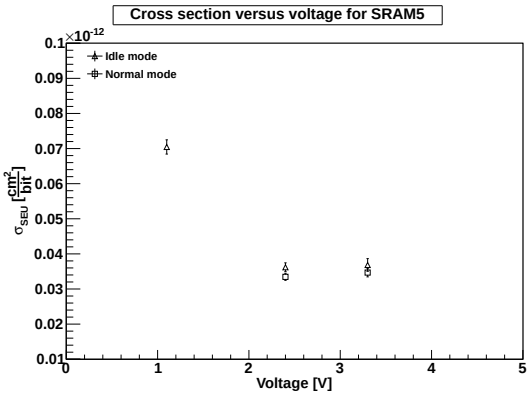
Comparing the 16 Mb SRAM2a from PTB at 14.8 MeV of $(2.54 \pm 0.36) \times 10^{-15}$ with the equivalent SRAM2c from OCL of $(6.79 \pm 0.13) \times 10^{-14}$ we can see that there is a factor 26 between them. Since the cross sections for the 1 Mb are equal within the uncertainties, the 16 Mb should also have been close. This again confirms the wrong measurements of the 16 Mb at PTB.



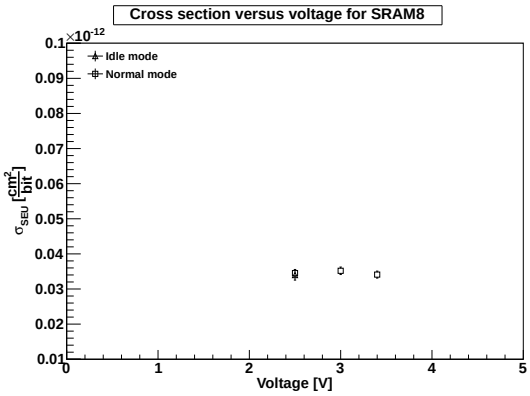
(a) *SRAM1c* **(b)** *SRAM2c*

(c) *SRAM3b* **(d)** *SRAM4*

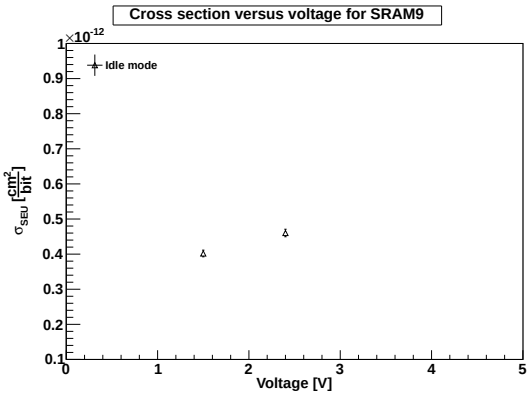
Figure 6.3: *Cross section for different voltages at OCL.*



(e) *SRAM5*



(f) *SRAM8*



(g) *SRAM9*

Figure 6.3: *Cross section for different voltages at OCL.*

6.3 High energy hadron-field testing at CERF

The measurements were done between 1–6 of August 2010. Table 6.6 provides a summarized list of the fluence and detected SEUs for the two positions tested. For more details and a complete table, see D.2.

6.3.1 Analysis of data

The counts from the Precision Ionization Chamber (PIC) has been converted to particles-on-target by multiplying by 22400. From a FLUKA simulation done by Ketil Røed, three conversion factor from particles on target to fluence at the two wall positions F1 and F4 were found. The three conversion factors correspond to the fluence of high energy hadrons (HEH) above 20 MeV, fast neutrons between 5 MeV and 20 MeV and thermal neutrons. Table 6.8 lists these conversion factors and their given uncertainty. Position F1 is seen to be dominated by thermal neutrons by an order of magnitude higher then HEH.

To analyze the response of the detector in a mixed radiation field a fitting function

Nr.	Position	SEUs	p.o.t [1/cm^2]	Φ_{HEH} [1/cm^2]	Φ_{n5-20} [1/cm^2]	Φ_{therm} [1/cm^2]	SEUs/p.o.t./bit [cm^2/bit]	$\sigma_{SEUs/p.o.t./bit}$ [cm^2/bit]
1a	F4	198	1.16×10^{12}	1.97×10^{9}	8.22×10^{8}	1.16×10^{9}	1.63×10^{-16}	2.0×10^{-17}
1b	F4	262	1.14×10^{12}	1.94×10^{9}	8.08×10^{8}	1.14×10^{9}	2.19×10^{-16}	2.6×10^{-17}
2a	F1	84	4.33×10^{11}	3.72×10^{7}	4.15×10^{7}	2.94×10^{8}	1.16×10^{-17}	1.7×10^{-18}
2a	F4	931	2.42×10^{11}	4.12×10^{8}	1.72×10^{8}	2.42×10^{8}	2.29×10^{-16}	2.4×10^{-17}
2b	F1	75	4.33×10^{11}	3.72×10^{7}	4.15×10^{7}	2.94×10^{8}	1.03×10^{-17}	1.6×10^{-18}
2b	F4	1288	3.34×10^{11}	5.68×10^{8}	2.37×10^{8}	3.34×10^{8}	2.30×10^{-16}	2.4×10^{-17}
3a	F1	125	4.33×10^{11}	3.72×10^{7}	4.15×10^{7}	2.94×10^{8}	3.44×10^{-17}	4.6×10^{-18}
3a	F4	6565	7.09×10^{11}	1.21×10^{9}	5.04×10^{8}	7.09×10^{8}	1.10×10^{-15}	1.1×10^{-16}

Table 6.6: *Combined fluences and counts for each device for a given position and its calculated response to the number of particles on target.*

Nr.	Ratio F4/F1 SEUs/p.o.t.	Ratio F4/F1 $\Phi_{\text{HEH}}+\Phi_{\text{fast}}$	Ratio F4/F1 Φ_{HEH}	Ratio F4/F1 Φ_{fast}	Ratio F4/F1 Φ_{therm}	Ratio F4/F1 p.o.t.
2a	19.8 ± 3.8	7.4 ± 0.1	11.1 ± 0.1	4.1 ± 0.1	0.82 ± 0.01	0.56 ± 0.08
2b	22.3 ± 4.1	10.2 ± 0.2	15.3 ± 0.2	5.7 ± 0.1	1.13 ± 0.02	0.77 ± 0.11
3a	32.1 ± 5.9	21.7 ± 0.4	32.4 ± 0.4	12.1 ± 0.2	2.41 ± 0.03	1.64 ± 0.23

Table 6.7: *Ratio between fluences of position F1 and F4 compared to ratio of SEUs/p.o.t.*

is used :

$$\text{SEUs} = (\Phi_{\text{HEH}}\cdot\sigma_{\text{HEH}}) + (\Phi_{\text{fast}}\cdot\sigma_{\text{fast}}) + (\Phi_{\text{therm}}\cdot\sigma_{\text{therm}}) \tag{6.3}$$

Where Φ is the fluence and σ is the calibrated cross section for the specified energy range. Commonly the cross section is seen to saturate at about 50 MeV and above, the high energy hadron cross section can thus be assumed to be the same as the saturation cross section for a device. The thermal cross section is for energies below the cadmium cut-off energy of about 0.4 eV.

Energy	F1		F4	
	Φ [1/(cm^2 pot)]	Unc. [%]	Φ [1/(cm^2 pot)]	Unc. [%]
HEH	8.6×10^{-5}	1.3	1.7×10^{-3}	0.2
5-20 MeV neutrons	9.6×10^{-5}	1.3	7.1×10^{-4}	0.4
Thermal neutrons	6.8×10^{-4}	1.3	1.0×10^{-3}	0.4

Table 6.8: *The fluence per particle on target at wall position F1 and F4 from FLUKA simulations by Ketil Røed [51].*

Uncertainties

The following uncertainties are used in the calculations

- The calibration factor used when converting PIC counts to particles on target has an uncertainty (σ_{PLC}) of 10 %.

- The conversion factors from particles on target to the fluence on the wall have the statistical uncertainties (σ_{HEH}, σ_{fast}, σ_{th}) listed in table 6.8

- The number of SEUs in the SRAMs has a statistical uncertainty given by the Poisson distribution of $\frac{1}{\sqrt{N_{SEU}}}$.

The uncertainty of the response is determined from the propagation of errors.

6.3.2 Results

The response from SRAM1a and b in table 6.6 can be seen to differ by 30 %. The placement of the two detectors were switched midway in the measurement, but the difference didn't move with the position. A difference to this extent can not be seen for the PTB results.

The response of the two SRAM2 detectors can be seen to be equal within the given uncertainty. The response is also comparable to the response of SRAM1 in position F4, indicating a comparable behavior.

SRAM3 is seen to have an order of magnitude higher response for position F4, this is caused by nonlinearity in the response as seen in figure 6.6.

SRAM2a and b had frequent latchups, SRAM1b had one and SRAM3a had two during the measurements.

6.3.3 SRAM1a and b

This device has previously been tested not to be sensitive to thermal neutrons by Granlund et al. [52]. If we ignore the thermal contribution in equation (6.3) we can estimate the range of the high energy hadron cross section by using the cross section for 14.8 MeV and 5.8 MeV neutrons as the cross section for fast neutrons. The HEH cross section can then be found from

$$\sigma_{\mathrm{HEH}} = \frac{(\mathrm{SEUs} - (\Phi_{\mathrm{fast}} \cdot \sigma_{\mathrm{fast}}))}{\Phi_{\mathrm{HEH}}} \tag{6.4}$$

The result is given in table 6.9 and it can be seen that the HEH cross section should be between 1.5 and 1.9 times the cross section found for 14.8 MeV neutrons at PTB.

σ_{fast} [cm^2/bit]	SEUs	Φ_{HEH} [1/cm^2]	Φ_{fast} [1/cm^2]	σ_{HEH} [cm^2/bit]	$\sigma_{\sigma HEH}$ [cm^2/bit]	$\sigma_{HEH}/\sigma_{14.8}$
$\sigma_{n5.8}$	459	3.90×10^9	1.63×10^9	1.09×10^{-13}	1.2×10^{-14}	1.87
$\sigma_{n14.8}$	459	3.90×10^9	1.63×10^9	8.79×10^{-14}	9.7×10^{-15}	1.51

Table 6.9: *Estimated range of HEH cross section for SRAM1.*

SRAM2a and b

Calculating the three unknown cross sections from the two equations taken from the two positions is not possible as this will yield a negative answer. But if we assume that the thermal cross section is zero and use the cross section found for 26 MeV proton at OCL as the upper bound for the cross section of fast neutrons and the same ratio between the upper and lower bound as between the cross section of 14.8 MeV and 5.8 MeV neutrons for SRAM1 we can again try to calculate the range of the cross section for HEH.

σ_{fast} [cm^2/bit]	Position	SEUs	Φ_{HEH} [1/cm^2]	Φ_{fast} [1/cm^2]	Φ_{therm} [cm^2/bit]	σ_{HEH} [cm^2/bit]	$\sigma_{\sigma HEH}$ [cm^2/bit]	$\sigma_{HEH}/\sigma_{p26}$
$\sigma_{p26}/7$	F4	2219	9.80×10^8	4.09×10^8	5.76×10^8	1.31×10^{-13}	1.3×10^{-14}	1.93
σ_{p26}	F4	2219	9.80×10^8	4.09×10^8	5.76×10^8	1.07×10^{-13}	1.1×10^{-14}	1.57
$\sigma_{p26}/7$	F1	159	7.44×10^7	8.31×10^7	5.89×10^8	1.17×10^{-13}	1.5×10^{-14}	1.72
σ_{p26}	F1	159	7.44×10^7	8.31×10^7	5.89×10^8	5.14×10^{-14}	6.6×10^{-15}	0.76

Table 6.10: *Estimated range of HEH cross section for SRAM2.*

It can be seen in table 6.10 that the cross section for HEH at the lower bound of the cross section of fast neutrons has overlapping errors between position F1 and F4 and can thus be seen as a better estimate. The ratio between the HEH cross section and the proton cross section at the lower bound is also comparable to the ratio found for SRAM1.

SRAM3a

The calculations for SRAM3a is done in the same fashion as for SRAM2 and is shown in table 6.11. Due to anomalies in the count-rate of the device, the results are not perfectly clear. During a run the device is seen to have sharp rises in count rate of 10–30 counts in a couple of seconds when the normal count-rate would be 1 every other minute. When looking at table 6.7 it can be seen that the ratio between position F4 and F1 for SEUs/p.o.t. and the ratio of the HEH fluence is equal within the given uncertainties. This could mean that the sharp rises in count rate are primarily caused by HEH. For SRAM2 this relationship seems to be more complex.

σ_{fast} [cm^2/bit]	Position	SEUs	Φ_{HEH} [1/cm^2]	Φ_{fast} [1/cm^2]	Φ_{therm} [cm^2/bit]	σ_{HEH} [cm^2/bit]	$\sigma_{\sigma HEH}$ [cm^2/bit]	$\sigma_{HEH}/\sigma_{p26}$
$\sigma_{p26}/7$	F4	6565	1.21×10^9	5.04×10^8	7.09×10^8	6.39×10^{-13}	6.4×10^{-14}	3.57
σ_{p26}	F4	6565	1.21×10^9	5.04×10^8	7.09×10^8	5.74×10^{-13}	5.8×10^{-14}	3.21
$\sigma_{p26}/7$	F1	125	3.72×10^7	4.15×10^7	2.94×10^8	3.73×10^{-13}	5.0×10^{-14}	2.08
σ_{p26}	F1	125	3.72×10^7	4.15×10^7	2.94×10^8	2.01×10^{-13}	2.7×10^{-14}	1.12

Table 6.11: *Estimated range of HEH cross section for SRAM3a.*

Reproducibility and linearity

Figure 6.4 presents the reproducibility of the devices based on the number of SEUs and the number of particles on target for all the runs of position F4. The uncertainties given are only the statistical uncertainty and the uncertainty in the conversion factor from the PIC counts to particles on target.

SRAM1a and SRAM2a and b is seen to have a good reproducibility and the response is linear. SRAM2b is seen to have a greater dispersion around the mean at lower count-rates than SRAM1a. This could just be due to low statistics, but if we look at the accumulated number of SEUs versus the accumulated number of particles on target in figure 6.5 we can still see that the response is linear for a long run. Looking at the reproducibility from PTB in figure 6.2, the device is there seen to be linear even at low count rates. The difference could thus stem from the mixed radiation field and for such a field it could be argued that the detectors do not present a good reproducibility below 50 SEUs.

When looking at the response of SRAM3 it can be seen that the reproducibility is not good, but by plotting the accumulated response in figure 6.6, the device still seem to show an acceptable linearity. The jumps in the count-rate might be linearly dependent on the amount of incoming particles, but the response of the jumps is too low to be filtered out from the rest of the counts.

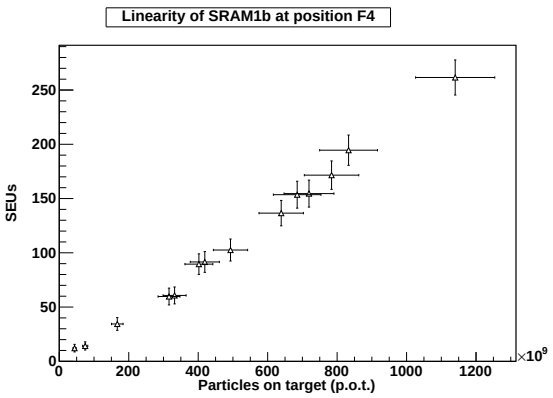


Figure 6.5: *Linearity of SRAM1b at position F4.*

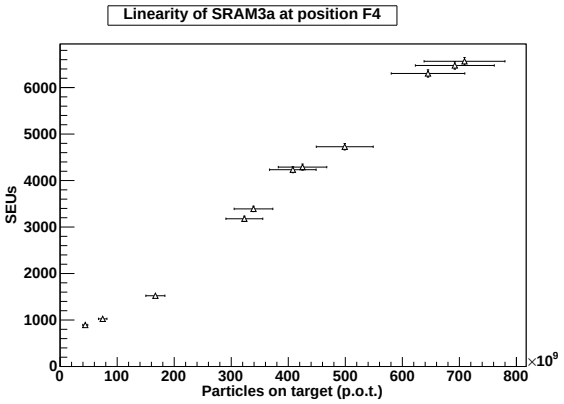
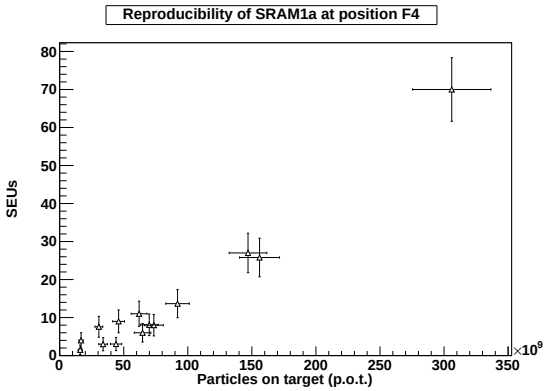


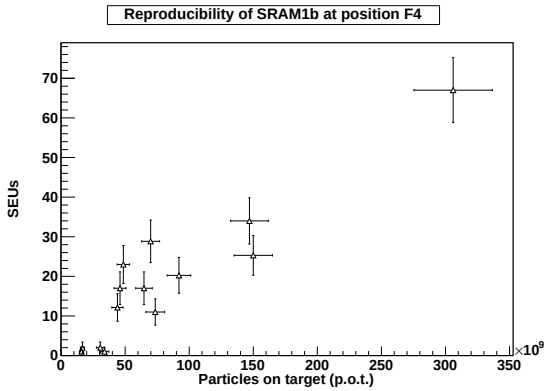
Figure 6.6: *Linearity of SRAM3a at position F4.*

6.4 Thermal neutron testing at IFE

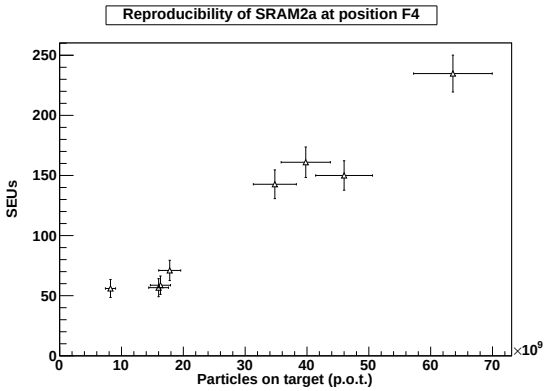
The measurements were done between 10–13 of May 2011. Two gold activation test were conducted to measure the thermal neutron fluence. The fluence and position of measurement can be seen in table 6.12. A test with SRAM2d wrapped in cadmium foil was later done to look at the difference in count rate when the thermal neutron spectra was moderated. As can be seen in table 6.13b the count rate between a run with cadmium and one without at the same voltage shows no difference within the given uncertainties. As there was no other information available on the energy spectrum



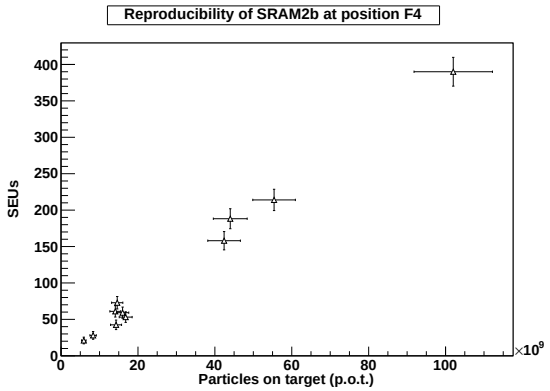
(a) *SRAM1a*



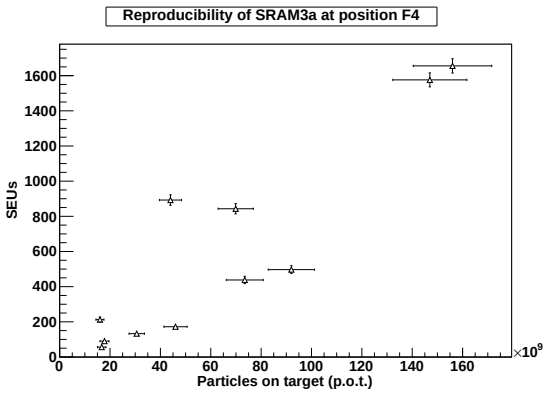
(b) *SRAM1b*



(c) *SRAM2a*



(d) *SRAM2b*



(e) *SRAM3a*

Figure 6.4: *Reproducibility of SRAMs at position F4 at CERF.*

of the neutrons in the pool, the rest of the results will not be based on the fluence measurements. Cross sections based on the fluences can be found in D.4.

Run	Weight [g]	Exposure time [s]	Activity [Bq]	Flux [n/cm^2]	Position
1	0.2883	1860	2630 ± 74	$(5.47 \pm 0.15) \times 10^6$	Bottom of pipe
2	0.2333	2220	3350 ± 90	$(7.22 \pm 0.20) \times 10^6$	Bottom of pipe + 5–10 cm

Table 6.12: *Measured thermal flux by gold activation in pool.*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
1.5	Normal	1.29×10^{-8}	3.0×10^{-9}
2.4	Normal	7.86×10^{-9}	2.0×10^{-9}
3.4	Normal	6.33×10^{-9}	1.6×10^{-9}
1.5	Idle	1.05×10^{-8}	2.6×10^{-9}

(a) *SRAM1c*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
1.5	Normal	1.37×10^{-8}	2.9×10^{-9}
2.4	Normal	7.36×10^{-9}	1.1×10^{-9}
3.4	Normal	7.08×10^{-9}	1.5×10^{-9}
2.4	Idle	8.95×10^{-9}	1.9×10^{-9}
2.4	N + Cd	8.70×10^{-9}	1.8×10^{-9}

(b) *SRAM2d - N + Cd is normal with cadmium*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
1.5	Normal	9.39×10^{-9}	2.0×10^{-9}
2.4	Normal	2.46×10^{-8}	5.1×10^{-9}
3.4	Normal	1.60×10^{-8}	3.3×10^{-9}
1.5	Idle	9.33×10^{-9}	2.0×10^{-9}
2.4	Idle	9.50×10^{-9}	2.0×10^{-9}

(c) *SRAM3b*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
1.3	Normal	3.23×10^{-8}	6.8×10^{-9}
1.5	Normal	1.22×10^{-8}	2.6×10^{-9}
2.4	Normal	1.40×10^{-8}	2.9×10^{-9}
3.4	Normal	1.13×10^{-8}	2.4×10^{-9}
2.4	Idle	1.27×10^{-8}	2.7×10^{-9}

(d) *SRAM4*

Table 6.13: *Average number of SEUs per second for a given voltage at IFE.*

6.4.1 Analysis of data

The fluence and cross sections in the table are the weighted mean of all the runs at the specified voltage.

Uncertainties

The following uncertainties are used in the calculations :

- The time between starting and stopping a measurement has an uncertainty of 2 s for runs where the time was restarted at the same time as the counting was reset. For some of the first runs this was not done properly and has thus a higher uncertainty.
- From the uncertainty in positioning of the device in the pipe an uncertainty of 20 % has been estimated.

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
2.4	Normal	8.46×10^{-9}	1.9×10^{-9}
3.3	Normal	9.74×10^{-9}	2.1×10^{-9}
1.0	Idle	2.85×10^{-8}	6.2×10^{-9}
1.0	Idle	2.44×10^{-8}	5.2×10^{-9}
2.4	Idle	9.25×10^{-9}	2.1×10^{-9}

(e) *SRAM5*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
2.4	Normal	2.50×10^{-8}	5.2×10^{-9}
3.3	Normal	2.48×10^{-8}	5.2×10^{-9}
2.4	Idle	2.79×10^{-8}	5.8×10^{-9}

(f) *SRAM7*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
1.3	Normal	1.29×10^{-8}	2.9×10^{-9}
2.5	Normal	8.49×10^{-9}	1.9×10^{-9}
3.0	Normal	7.63×10^{-9}	1.7×10^{-9}
3.4	Normal	8.80×10^{-9}	2.0×10^{-9}
1.3	Idle	1.43×10^{-8}	3.2×10^{-9}

(g) *SRAM8*

Voltage [V]	Mode	SEU/time/bit [1/(s bit)]	$\sigma_{SEU/time/bit}$ [1/(s bit)]
1.3	Normal	1.89×10^{-8}	4.1×10^{-9}
1.5	Normal	2.24×10^{-8}	4.7×10^{-9}
2.4	Normal	2.02×10^{-8}	4.2×10^{-9}
3.4	Normal	3.50×10^{-8}	7.2×10^{-9}
1.5	Idle	3.35×10^{-8}	6.9×10^{-9}
2.4	Idle	5.07×10^{-8}	1.0×10^{-8}

(h) *SRAM9*

Table 6.13: *Average number of SEUs per second for a given voltage at IFE.*

- The number of SEUs in the SRAMs has a statistical uncertainty given by the Poisson distribution of $\frac{1}{\sqrt{N_{SEU}}}$.

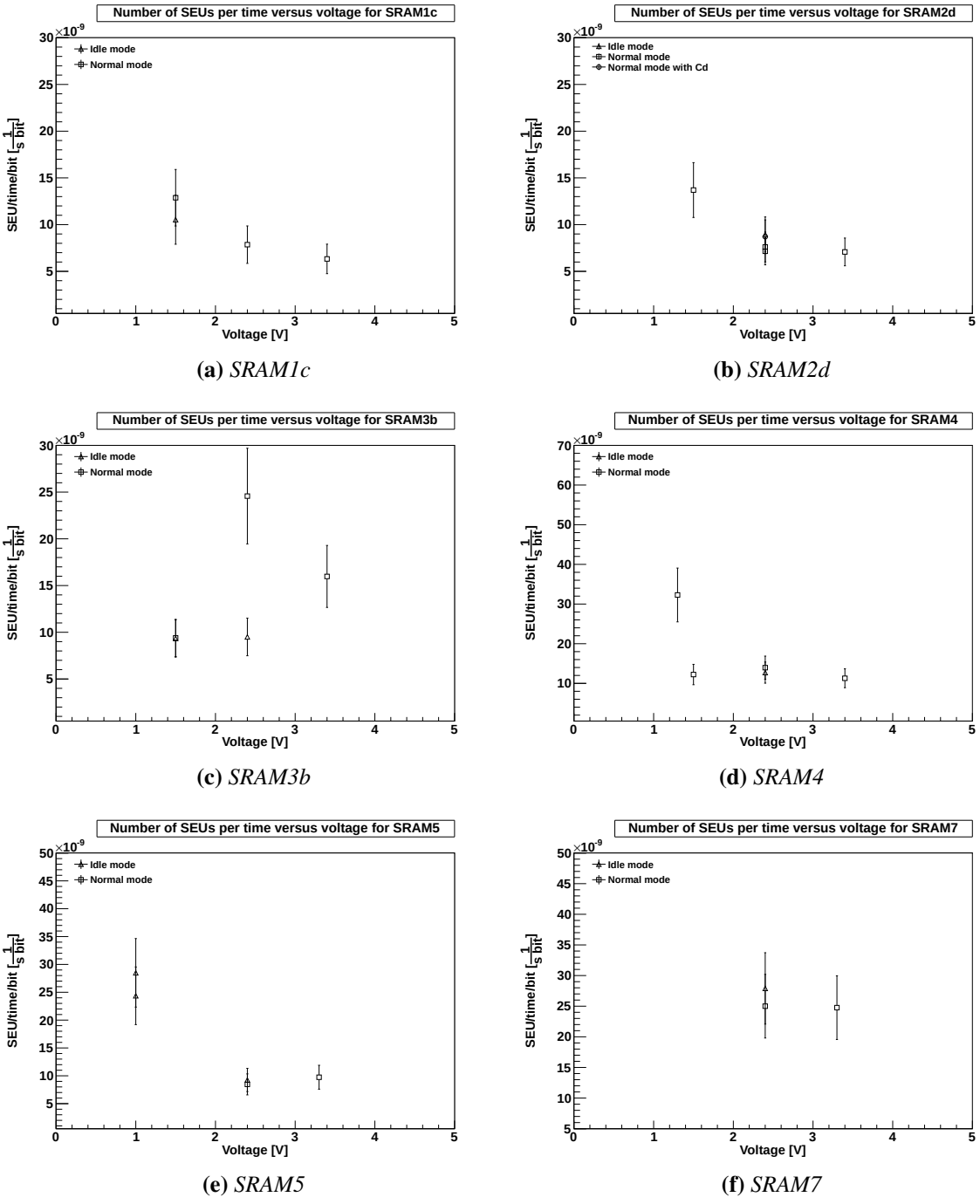
The uncertainty of the number of SEUs per time is determined from the propagation of errors.

6.4.2 Results

Figure 6.7 shows the relationship between the voltage and the cross section in idle and normal mode. The increased sensitivity at lower voltage for SRAM1c, 2d, and 5 is also present here, the same as what was seen at OCL. Additionally for the newly tested lowest voltage setting, an increase can also be seen for SRAM4 and 8.

The sharp increases in count rate for the 90 nm devices are also present here and an example of this is presented in figure 6.8k. These sharp increases are also confirmed by Ketil Røed et.al who were testing SRAM3 in parallel with us but with a different setup. The effects are also seen in a Cypress CY62148EV 4 Mb 90 nm by yet another party [51] proving that the anomalies are not caused by the setup, but is a general problem with the 90 nm device-series by Cypress.

None of the devices latched up for any of the voltages.

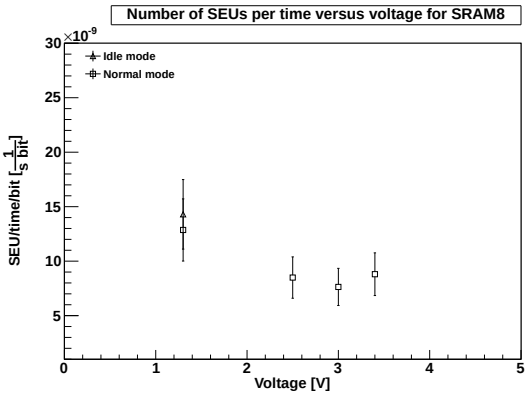


(a) *SRAM1c* **(b)** *SRAM2d*

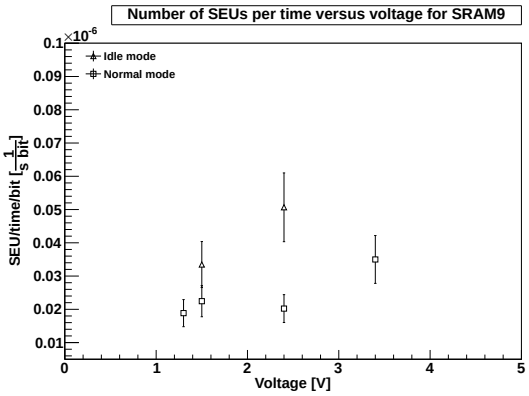
(c) *SRAM3b* **(d)** *SRAM4*

(e) *SRAM5* **(f)** *SRAM7*

Figure 6.7: *Cross section for different voltages at IFE.*

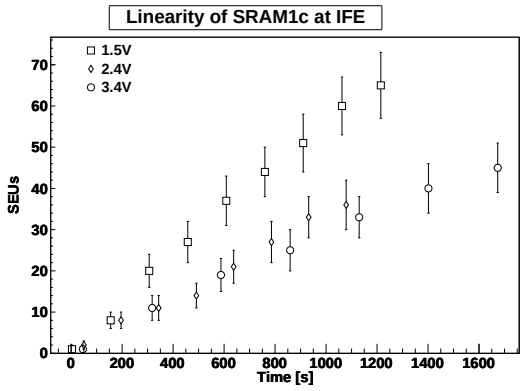


(g) *SRAM8*

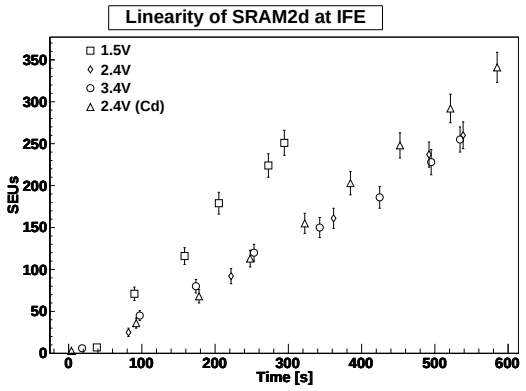


(h) *SRAM9*

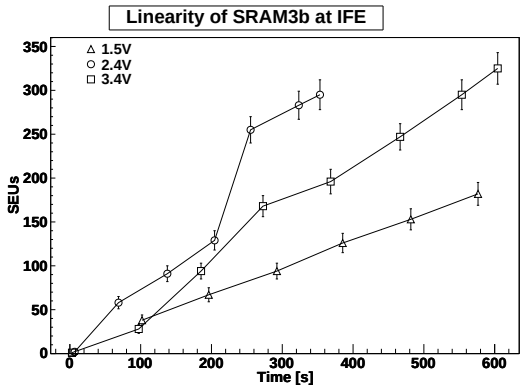
Figure 6.7: *Cross section for different voltages at IFE.*



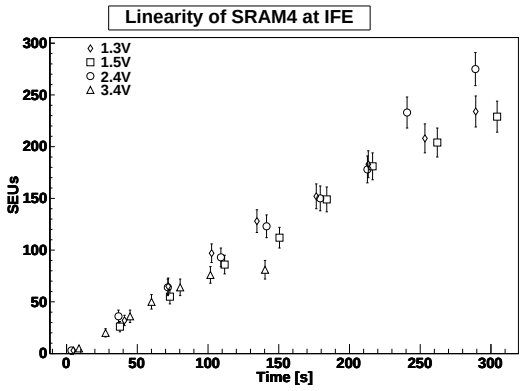
(i) *SRAM1c*



(j) *SRAM2d*



(k) *SRAM3b*

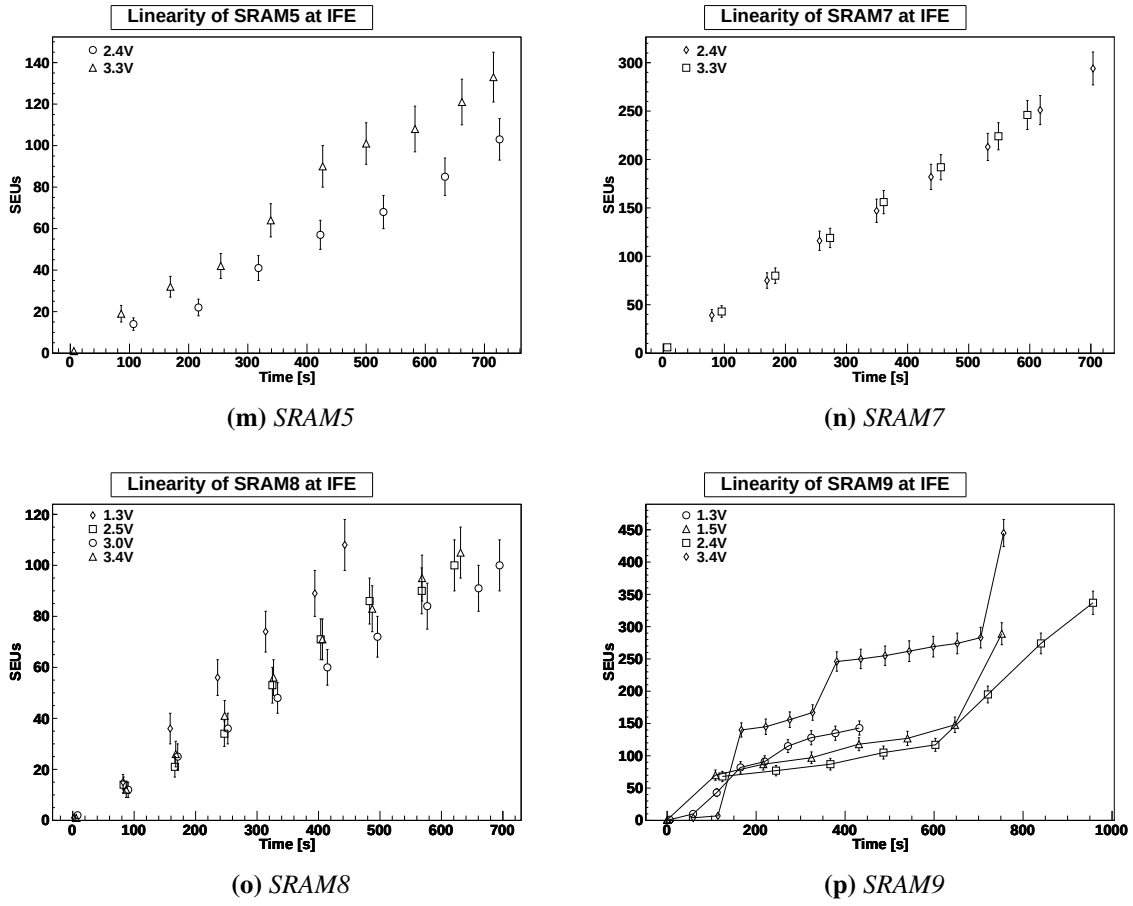


(l) *SRAM4*

Figure 6.8: *Linearity of devices tested at IFE. Lines added for clarity for SRAM3b.*

6.4.3 Linearity

Figure 6.8 shows the linearity of the devices tested at IFE. All devices show a good linearity beside SRAM3b and 9, as has been seen before. The interesting thing to note is that it seems that the sharp increases in count rate of SRAM3b and 9 is less severe at lower voltages, at 1.3 V for SRAM3b it is perfectly linear.



(m) *SRAM5*

(n) *SRAM7*

(o) *SRAM8*

(p) *SRAM9*

Figure 6.8: *Linearity of devices tested at IFE. Lines added for clarity for SRAM3a and 9.*

6.4.4 TID problems

SRAM2c was tested for a total of 108 min in the pool. In the last run the communication was lost and the device stopped working. Further investigation of this showed that the on-board power supplies had dropped to such a low voltage that the FPGA had stopped working. This decrease in voltage was also present on the other detectors and when plotting the voltage of each detector against the amount of time the detector stayed in the pool, as shown in figure 6.9, one can see that power supplies can withstand about 40 min before starting to drop considerably. The detectors that were irradiated between 50 min and 80 min had an oscillating current consumption, but otherwise worked al-

right. The two detectors that were irradiated more than 80 min worked normally after replacing the affected power supplies.

No effects have previously been seen after any of the other irradiation tests which have been commenced for this thesis and so it is assumed that the cause of this failure is due to the Total Ionized Dose (TID) received from the very high amount of gamma radiation present in the pool. For future testing with this detector a lead shielding should be used for the power supplies or they should be replaced by other devices able to withstand higher doses.

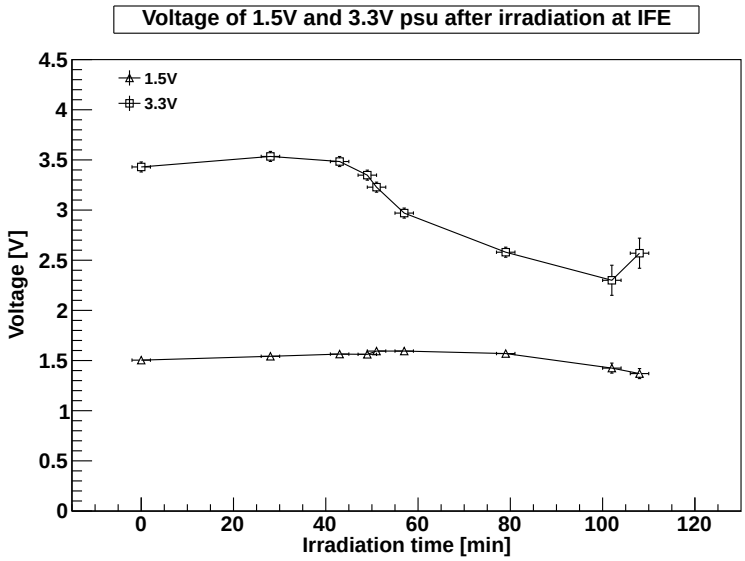


Figure 6.9: *3.3 V and 1.5 V power supply voltage versus irradiation time measured after testing at IFE.*

6.5 Summary

What can be summed up from these measurements is that SRAM2 seems to be the most stable device with the overall highest cross section, but this is also the device with the oldest technology and will most likely go out of production first. This has already happened to SRAM5 during the work with this thesis.

The next best contender is SRAM1 in case of stability and cross section, but as the device only has 1 Mb of memory it needs too much physical space to get the same sensitivity per detector as the other devices.

The next contender in line is SRAM4, which could be used in spite of its 90 nm anomalies. In this device, the sharp rises in count rate are relatively small in contrast to the overall count rate of the device due to the large memory of the device.

SRAM6 and 8 are both viable contenders, but with a low cross section. Their drawback is that they have a current-consumption of 100 mA to 200 mA due to them being Synchronous SRAMs (SSRAMs). In contrast to the current-consumption of the other

devices of about 20 mA, this would limit their possibility of being set up in a large array.

SRAM8 had more problems with latchup at OCL than the other device, but the one cross section found is on the lower level compared to the others.

SRAM3 and 9 both suffer greatly from the 90 nm anomalies and are not great contenders if the problem can not be mitigated.

Looking at the detector hardware and readout it has been seen that it holds up quite well in most radiation environments and the only problems discovered are the dose related damages to the power supplies. No errors have been observed in the operation of the FPGA which proves the reliability of using flash based FPGAs in a radiation environment.

Chapter 7

Conclusion and outlook

7.1 Conclusion

The first objective of this thesis has been to investigation the applicability of various SRAM devices for use as an active neutron detector. This included testing them in both a fast neutron beam and a thermal neutron field. The second objective was to design and implement the detector hardware and firmware in addition to the readout system for the detector, to effectively be able to test the devices properly.

Two devices were tested at the Physikalisch-Technische Bundesanstalt (PTB) facility in Braunschweig, Germany, on a quasi-monochromatic neutron beam of 5.8 MeV, 8.5 MeV and 14.8 MeV energies. A dependency on energy was found for both devices which showed a factor three lower Single Event Upset (SEU) cross section between 14.8 MeV and 8.5 MeV, while a factor seven was found between 14.8 MeV and 5.8 MeV. An indication that the sensitivity is significantly lower when irradiated from the back than the front was also found and should be taken into consideration for later use.

These two devices and one additional device were later tested in a mixed high energy hadron field at CERF at CERN, France. An effort has been made to unfold the spectra from data gathered from the other experiments and get the SEU cross section for high energy hadrons, which should be close to the saturation cross section for the device. But due to low statistics, only an estimated range of the saturation cross section can be determined.

Testing was also conducted with six more devices at two occasions in a 26 MeV proton beam at Oslo Cyclotron Laboratory (OCL) in Oslo, Norway. A cross section was found for all devices and a dependency on the applied voltage of the device was additionally found to be up to a factor two for some. The cross section for 26 MeV protons was also found to be equal to the cross section found for 14.8 MeV neutrons, indicating that the proton beam at OCL, which is easier to get access to, can be used for further SEU of SRAM detectors.

No accurate beam monitoring or characterization was available for the measure-

ments at OCL at low intensities, but a technique has been developed using a scintillator as a reference monitor during irradiation. The scintillator is calibrated against one of the SRAMs previously calibrated at PTB. This SRAM has further been calibrated against a Faraday Cup at a much higher intensity, which a flux can be calculated from. One of the SRAMs has also been used for creating the beam profile needed for determining the position of the center of the beam and its dispersion.

Thermal neutron testing was conducted at the nuclear reactor facility at IFE at Kjeller, Norway. All devices were found to be sensitive to the field, but only one device was tested with cadmium. The device tested with cadmium, which moderates the thermal neutrons below 0.5 eV, showed no significant difference with and without. Further testing of the other devices with cadmium is needed to determine if they have a sensitivity to thermal neutrons.

Of the devices tested in this work, two were active device (SRAM6 and 8), which could be susceptible to Single Event Functional Interrupts (SEFIs), but none were found. This indicates that SEFI is not a severe problem in active devices and they could potentially be used as detectors.

Three of the devices tested were from the currently smallest feature size of 90 nm from Cypress and they all suffer from sudden increases in SEU count rate of between 10–30 counts or more. The problem is not present when the device is tested in idle, and seems to decrease with the applied voltage. The problem has also been verified by others [51] and is thought to be related to SEUs in the control and readout logic of the devices.

As has been mentioned previously, some of the devices tested showed that the sensitivity had a dependence on the voltage. This was both found for 26 MeV protons and for thermal neutrons and, as can be seen in figure 7.1, the relationship is the same within the given uncertainty.

It can be concluded that all the devices which have been tested, besides the devices with a 90 nm feature size, are applicable as neutron detectors.

The system design of the detector tries to be minimalistic to reduce the points of error which could occur due to radiation damage of the components. Additionally this keeps the cost of the detector down to about 100–200$US. To read from the SRAM devices the detector uses a flash based FPGA from Actel which have proven to be reliant and which has not suffered from any noticeable radiation effects. The on board power supplies have though shown to suffer from a gradual drop in voltage related to Total Ionized Dose (TID) when the detector was irradiated in the thermal neutron pool at IFE.

The computer used to read out from the detectors uses two way communication to command up to 14 detectors at the same time over a 100 m cable, on the same pair of wires. The readout speed of the detectors is about 2 Mb/s and the data is read continuously from registers in the detectors.

From starting out with a very simple design, the detector and its setup has evolved to be a versatile and robust detector which has been proved to withstand testing in a wide

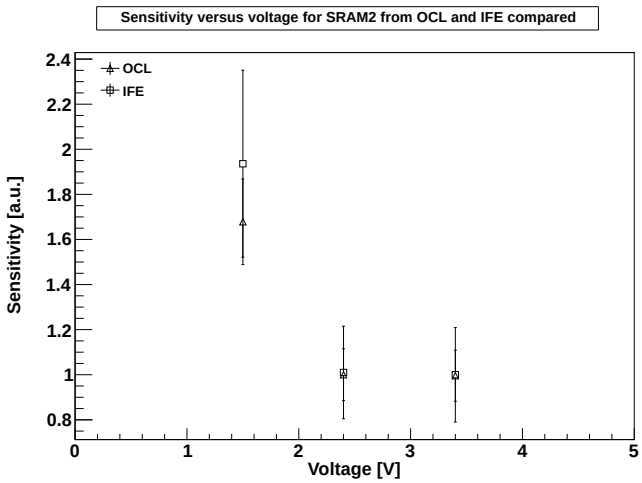


Figure 7.1: *The voltage dependence of the sensitivity compared between OCL and IFE. The numbers have been normalized to 2.4 V and given in Arbitrary Units.*

variety of radiation environments, even though there are still room for improvements as is discussed in the next section.

7.2 Outlook

At the testing at OCL and CERF severe problems of Single Event Latch-up (SEL) were discovered in most of the devices. This should be mitigated on the detector for future testing, and some solutions to how this could be done was presented in section 4.6.3.

As mentioned previously the problem of anomalies in the counting rate of the 90 nm devices should possibly be mitigated in some way also if they are to be further used.

For the beam profile creation at OCL the detector was moved manually resulting in loss of beam time due to having to run back and forth between each run. A x-y table has now been bought and could be used in combination with one of the detectors for future testing at OCL to reduce the time needed to create the beam profile and to increase the accuracy.

Accurate determination of the neutron spectra at IFE and further testing with cadmium on all devices should be done to determine the thermal neutron sensitivity of the devices.

Appendix A

PTB Calibration Data

A.1 PTB calibration report for 1st run

Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin

neutron fluence for 8.5 MeV

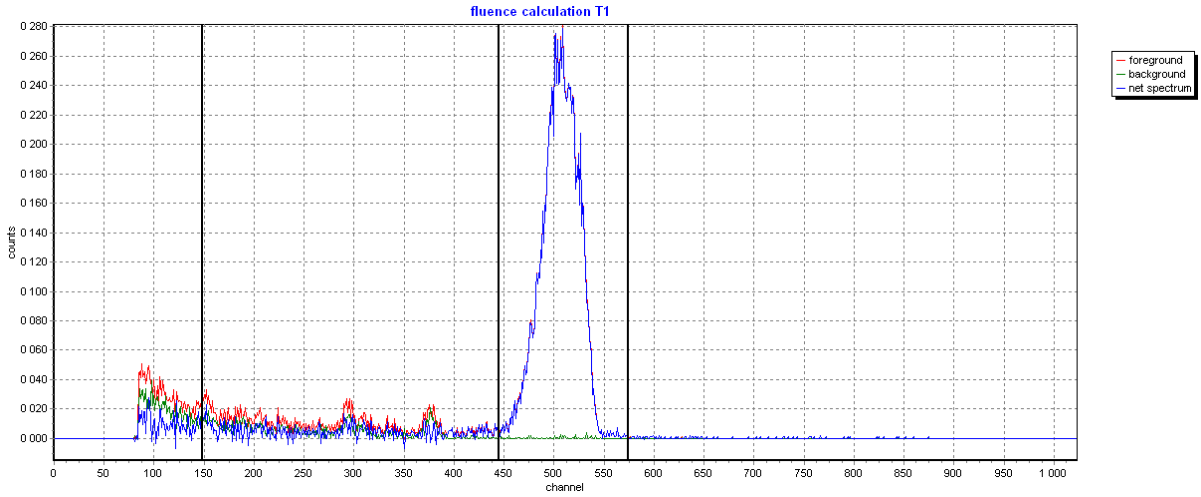
Date of measurement : 14-JUN-2010
Date of evaluation : 30.6.2010
File name : 2010_JUN_14_8_5MeV_T1_FG_1.MPA
Evaluator : S. Löb
Program version : version 1.0

NEUTRON PRODUCTION
Reaction : 2H(d,n)3He
Initial ion energy/MeV : 5.63
Target : Gas D2
Lab. angle/° : 0.0
backing/mm : -
areal mass/(mg/cm²) : -

FLUENCE INSTRUMENT
Radiator : 10.085 mg/cm²tristearine
Radiator↔ Target : 39.1876 cm
wobbling radius/cm : 0.6
beam current : 1.7 µA
gas pressure foreground : 2063.0 mbar gas pressure background : 2022.2 mbar
yield : 2.421E+011 1/sr
yield/Q : 1.198E+008 1/sr µC
phi_c : 1.572E+008 1/cm²

VALUES IN 1m
fluence : 2.406E+007 1/cm² dH*(10)/dt : 30645.8 µSv/h
fluence rate : 2.053E+004 (1/cm²s) dHp(10,0)/dt : 33494.3 µSv/h
fluence/Q : 1.191E+004 (1/cm²µC)

MONITOR CALIBRATION FACTORS
neutron yield / monitor counts
PLC : 6.888E+005 1/sr ±1.03 % PLC/Q : 173.940 counts/µC
HE3 : 8.386E+004 1/sr ±1.02 % HE3/Q : 1428.723 counts/µC
GM : 1.933E+006 1/sr ±1.06 % GM/Q : 61.979 counts/µC
NM : 4.149E+004 1/sr ±1.02 % NM/Q : 2887.922 counts/µC


fluence calculation T1
counts
channel
foreground
background
net spectrum

A.2 PTB calibration report for 2nd run

Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin

neutron fluence for 5.7 MeV

Date of measurement : 14-JUN-2010
Date of evaluation : 1.7.2010
File name : 2010_JUN_15_5_8MeV_T1_FG_1.MPA
Evaluator : S. Löb
Program version : version 1.0

NEUTRON PRODUCTION

Reaction : 2H(d,n)3He
Initial ion energy/MeV : 2.95
Target : Gas D2
Lab. angle/° : 0.0
backing/mm : -
areal mass/(mg/cm²) : -

FLUENCE INSTRUMENT

Radiator : 10.085 mg/cm²tristearine
Radiator↔ Target : 39.1876 cm
wobbling radius/cm : 0.6
beam current : 1.5 µA
gas pressure foreground : 1038.1 mbar gas pressure background : 1028.8 mbar
yield : 2.017E+011 1/sr
yield/Q : 3.996E+007 1/sr µC
phi_c : 1.309E+008 1/cm²

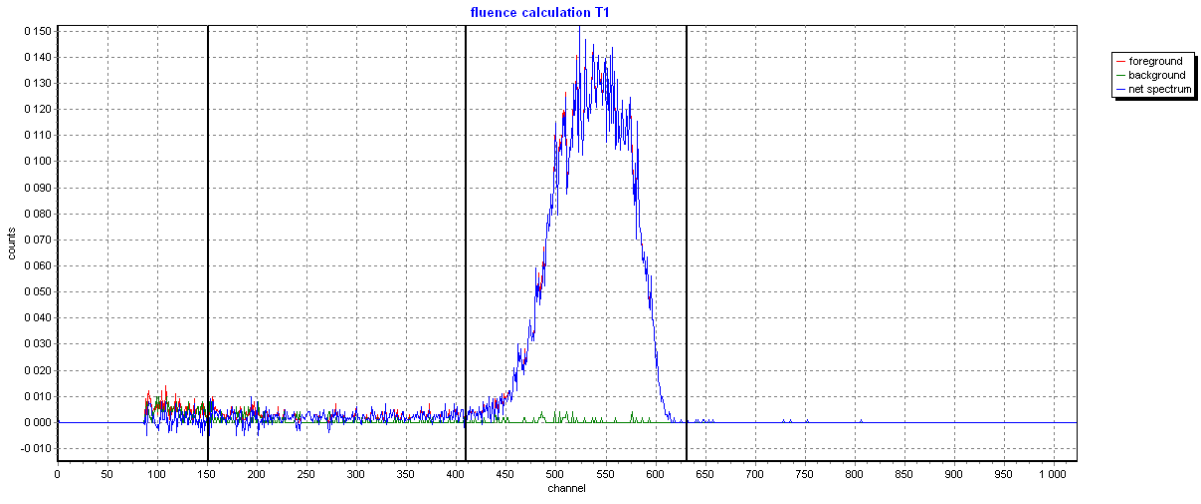
VALUES IN 1m

fluence : 2.002E+007 1/cm² dH*(10)/dt : 8305.3 µSv/h
fluence rate : 5.747E+003 (1/cm²s) dHp(10,0)/dt : 8.7347 µSv/h
fluence/Q : 3.937E+003 (1/cm²µC)

MONITOR CALIBRATION FACTORS

neutron yield / monitor counts

PLC : 4.982E+005 1/sr ±0.93 % PLC/Q : 79.610 counts/µC
HE3 : 6.881E+004 1/sr ±0.92 % HE3/Q : 576.365 counts/µC
GM : 8.495E+006 1/sr ±1.12 % GM/Q : 4.669 counts/µC
NM : 2.957E+004 1/sr ±0.91 % NM/Q : 1341.170 counts/µC



A.3 PTB calibration report for 3rd run

Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin

neutron fluence for 8.5 MeV

Date of measurement : 15-JUN-2010
Date of evaluation : 2.7.2010
File name : 2010_JUN_15_8_5MeV_T1_FG_1.MPA
Evaluator : Dr. R. Nolte
Program version : version 1.0

NEUTRON PRODUCTION

Reaction : 2H(d,n)3He
Initial ion energy/MeV : 5.61
Target : Gas D2
Lab. angle/° : 0.0
backing/mm : -
areal mass/(mg/cm²) : -

FLUENCE INSTRUMENT

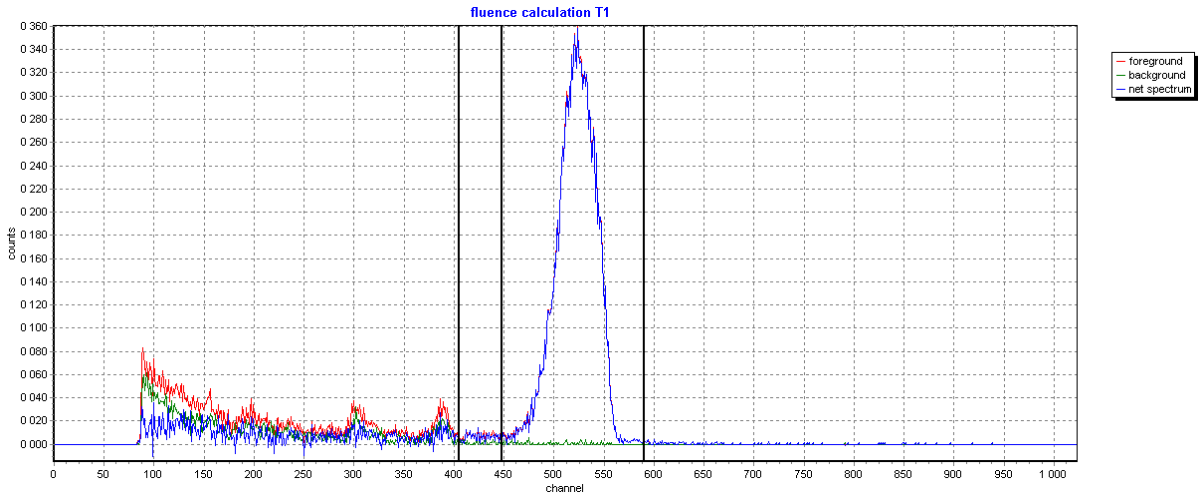
Radiator : 10.085 mg/cm²tristearine
Radiator↔ Target : 39.1876 cm
wobbling radius/cm : 0.6
beam current : 1.6 µA
gas pressure foreground : 1997.0 mbar gas pressure background : 2031.8 mbar
yield : 3.307E+011 1/sr
yield/Q : 1.184E+008 1/sr µC
phi_c : 2.147E+008 1/cm²

VALUES IN 1m

fluence : 3.287E+007 1/cm² dH*(10)/dt : 28628.1 µSv/h
fluence rate : 1.918E+004 (1/cm²s) dHp(10,0)/dt : 31289.1 µSv/h
fluence/Q : 1.177E+004 (1/cm²µC)

MONITOR CALIBRATION FACTORS

neutron yield / monitor counts
PLC : 5.487E+005 1/sr ±0.93 % PLC/Q : 215.719 counts/µC
HE3 : 7.327E+004 1/sr ±0.92 % HE3/Q : 1615.468 counts/µC
GM : 1.238E+006 1/sr ±0.94 % GM/Q : 95.613 counts/µC
NM : 3.771E+004 1/sr ±0.92 % NM/Q : 3138.871 counts/µC



A.4 PTB calibration report for 4th run

Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin

neutron fluence for 5.7 MeV

Date of measurement : 16-JUN-2010
Date of evaluation : 30.6.2010
File name : 2010_JUN_16_5_8MeV_T1_FG_1.MPA
Evaluator : S. Löb
Program version : version 1.0

NEUTRON PRODUCTION

Reaction : 2H(d,n)3He
Initial ion energy/MeV : 2.91
Target : Gas D2
Lab. angle/° : 0.0
backing/mm : -
areal mass/(mg/cm²) : -

FLUENCE INSTRUMENT

Radiator : 10.085 mg/cm²tristearine
Radiator↔ Target : 39.1876 cm
wobbling radius/cm : 0.6
beam current : 1.4 µA
gas pressure foreground : 1032.5 mbar gas pressure background : 1022.6 mbar
yield : 1.383E+011 1/sr
yield/Q : 3.794E+007 1/sr µC
phi_c : 8.975E+007 1/cm²

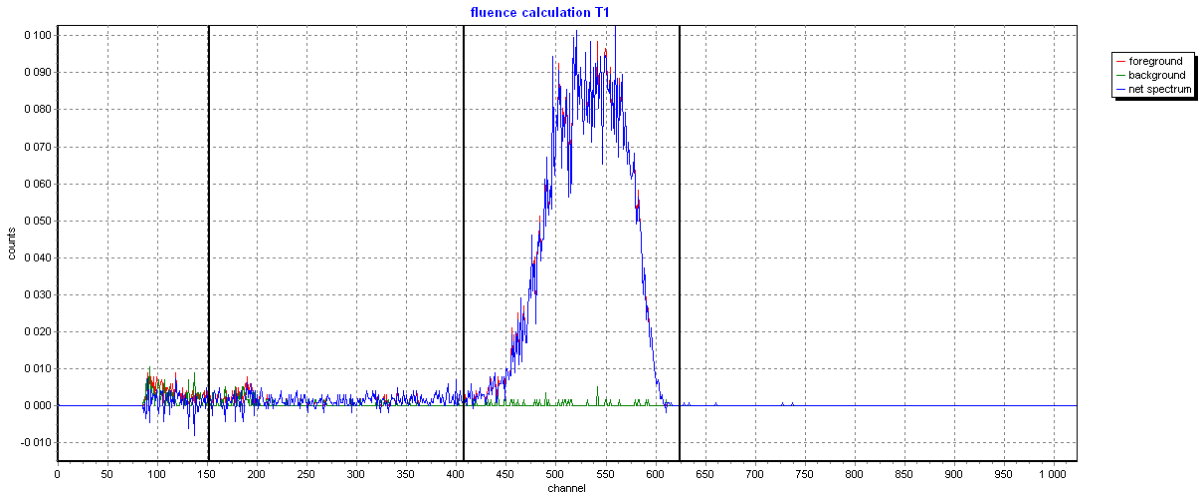
VALUES IN 1m

fluence : 1.372E+007 1/cm² dH*(10)/dt : 7593.7 µSv/h
fluence rate : 5.255E+003 (1/cm²s) dHp(10,0)/dt : 7986.3 µSv/h
fluence/Q : 3.766E+003 (1/cm²µC)

MONITOR CALIBRATION FACTORS

neutron yield / monitor counts

PLC : 4.732E+005 1/sr ±1.11 % PLC/Q : 80.188 counts/µC
HE3 : 6.747E+004 1/sr ±1.09 % HE3/Q : 562.389 counts/µC
GM : 1.011E+007 1/sr ±1.39 % GM/Q : 3.754 counts/µC
NM : 2.935E+004 1/sr ±1.09 % NM/Q : 1292.760 counts/µC



A.5 PTB calibration report for 5th run

Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin

neutron fluence for 14.8 MeV

Date of measurement : 17-JUN-2010
Date of evaluation : 30.6.2010
File name : 2010_JUN_17_14_8MeV_T1_FG_1.MPA
Evaluator : S. Löb
Program version : version 1.0

NEUTRON PRODUCTION

Reaction : 3H(d,n)4He
Initial ion energy/MeV : 0.215
Target : PTB 06
Lab. angle/° : 0.0
backing/mm : 0.5 Ag
areal mass/(mg/cm²) : 1.910

FLUENCE INSTRUMENT

Radiator : 10.085 mg/cm²tristearine
Radiator↔ Target : 37.63 cm
wobbling radius/cm : 0.6
beam current : 6.2 µA

yield : 1.898E+011 1/sr
yield/Q : 1.026E+007 1/sr µC
phi_c : 1.336E+008 1/cm²

VALUES IN 1m

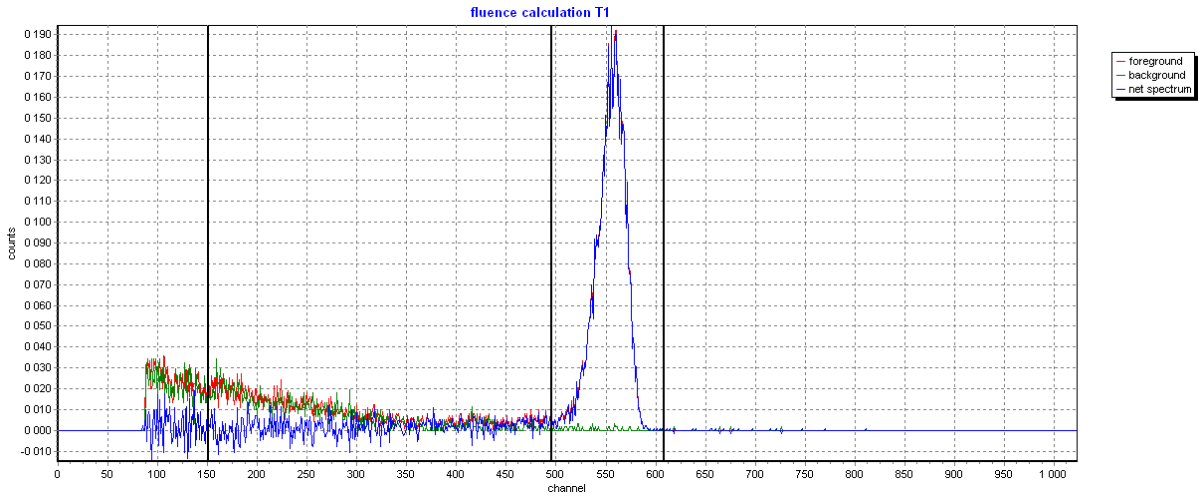
fluence : 1.882E+007 1/cm²
fluence rate : 6.296E+003 (1/cm²s)
fluence/Q : 1.017E+003 (1/cm²µC)
dH*(10)/dt : 12150.7 µSv/h
dHp(10,0)/dt : 12721.8 µSv/h

MONITOR CALIBRATION FACTORS

neutron yield / monitor counts

PLC : 1.029E+005 1/sr ±1.95 %
HE3 : 7.309E+004 1/sr ±1.95 %
GM : 2.100E+006 1/sr ±1.98 %
NM : 2.231E+004 1/sr ±1.95 %

PLC/Q : 99.713 counts/µC
HE3/Q : 140.311 counts/µC
GM/Q : 4.884 counts/µC
NM/Q : 459.723 counts/µC



Appendix B

Definition of steradian

1 steradian is defined as the solid angle that cuts out a surface area of $1\,\mathrm{m}^2$ on a sphere of radius 1 m, see for instance [63].

$$\Omega = \frac{A}{R^2} \tag{B.1a}$$

$$A = R^2 \tag{B.1b}$$

$$\Omega = 1 \tag{B.1c}$$

Where the area A corresponds to the area of a spherical cap, see for instance [64].

$$A = 2\pi Rh \tag{B.2}$$

Combining equation (B.1b) and equation (B.2) gives:

$$R^2 = 2\pi Rh \tag{B.3a}$$

$$\frac{h}{R} = \frac{1}{2\pi} \tag{B.3b}$$

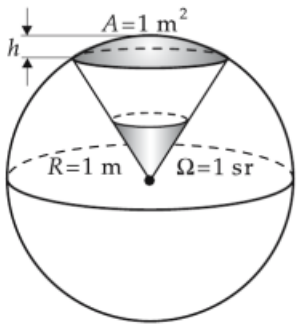


Figure B.1: *Illustration of the principle of a steradian as a unit of solid angle [64].*

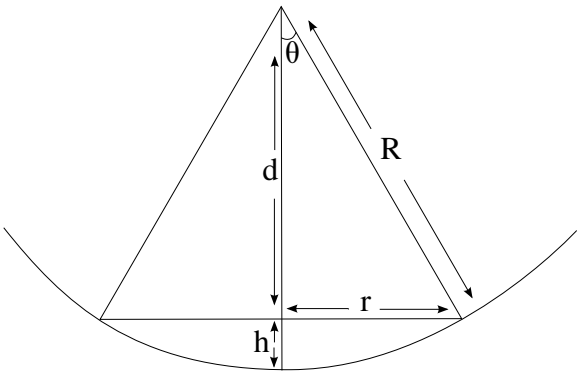


Figure B.2: *Illustration of the definition of the steradian.*

The angle θ in figure B.2 can now be determined:

$$\theta = \cos^{-1}\left(\frac{R-h}{R}\right) = \cos^{-1}\left(1-\frac{h}{R}\right) = \cos^{-1}\left(1-\frac{1}{2\pi}\right) \tag{B.4}$$

The area of the plane at distance d is given by:

$$A_{plane} = \pi r^2 \tag{B.5a}$$

$$A_{plane} = \pi(d\tan(\theta))^2 \tag{B.5b}$$

$$1 = \frac{A_{plane}}{\pi(d\tan(\theta))^2} \tag{B.5c}$$

The relationship between the steradian and the plane at a distance d from the center can now be determined:

$$\frac{\Omega}{A_{plane}} = \frac{1}{\pi(d\tan(\theta))^2} \tag{B.6a}$$

Appendix C

Sram Calibration

To calibrate the 1 Mb a FC was used as a reference. As reported by Røed [54] the FC is unreliable at low beam currents, but is usable at above 0.25 nA. Running at too high intensities would then again likely damage the SRAM, so a beam current of 0.5 nA was used (measured at 28 cm from the beam exit point with the FC).

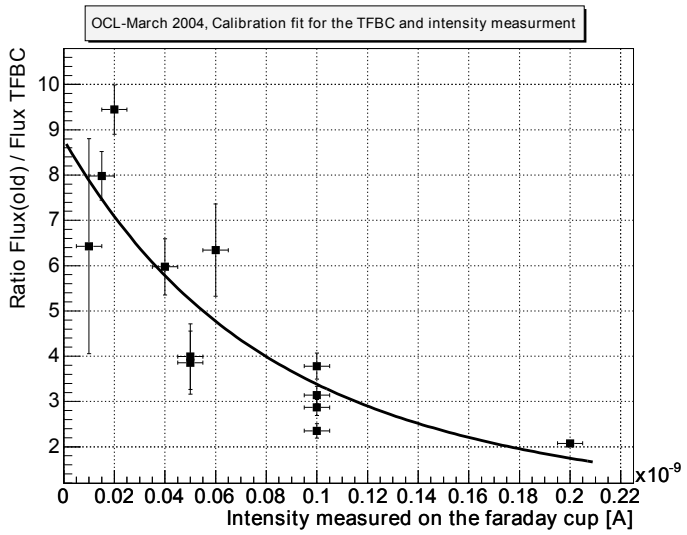


Figure C.1: *A fit of the ratio between the flux measurement using the Faraday cup and the flux measurement using a Thin Film Breakdown Counter (TFBC) [54].*

Nr.	Part number	Tech. [nm]	Size [Mbit]	Voltage [V]	Note
1a	CY62127DV30LL-55ZXI	130	1	1,50	Used for beam profile
1b	CY62127DV30LL-55ZXI	130	1	2,43	Used for calibration

Table C.1: *List of SRAM devices used for calibration at OCL. See table 5.5 for more specifications.*

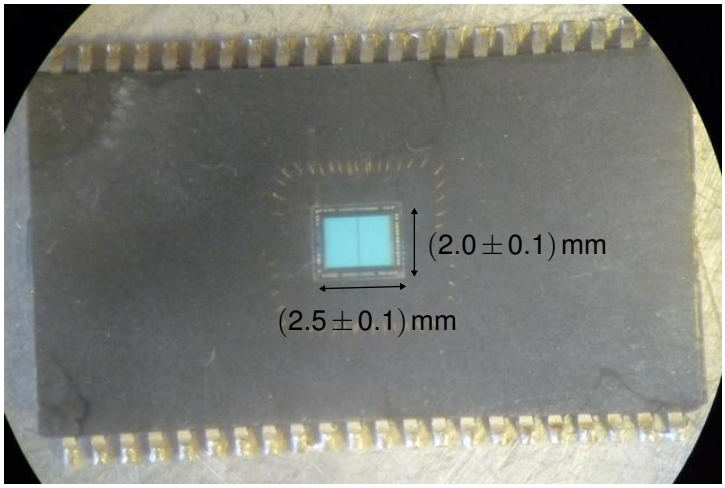


Figure C.2: *The SRAM used for beam profile measurements. The top has been shaved off after irradiation to expose the die. During irradiation the short end was facing downwards.*

The beam-profile was measured in both X and Y direction in 2 mm steps from −6 mm to +6 mm at 53.5 cm from the beam exit. At each step the beam was run for 15 s and the number of SEUs were recorded. To determine the fraction of the beam hitting the silicon wafer of the SRAM, the top was shaved off with a fine grained sandpaper. The silicon wafer was measured with a vernier caliper and found to be (2.00 ± 0.05) mm X (2.50 ± 0.05) mm, see figure C.2. The profile of the beam was assumed Gaussian and a fit was made for each direction, see figure C.3. A two dimensional Gaussian function can be created from

$$f(x,y) = A \cdot e^{-\left(\frac{x^2}{2\cdot\sigma_x^2}+\frac{y^2}{2\cdot\sigma_y^2}\right)} \tag{C.1}$$

Where A is the amplitude of the function (given as *constant* in figure C.3) and σ_x, σ_y is the spread of the peak. The intensity of the beam hitting the silicon wafer is then

$$A_{eff} = \frac{\int_{-1.25}^{1.25}\int_{-1}^{1} f(x,y)\,\mathrm{d}x\,\mathrm{d}y}{\int_{-6}^{6}\int_{-6}^{6} f(x,y)\,\mathrm{d}x\,\mathrm{d}y} = 0.12 \tag{C.2}$$

$$I_{eff} = I_{tot} \cdot A_{eff} = 0.06\,\mathrm{nA} \tag{C.3}$$

Knowing that the proton has the elementary charge of 1.602×10^{-19} C, the conversion from ampere to protons per seconds can be done the following way

$$1\,\mathrm{A} = 1\,\frac{\mathrm{C}}{\mathrm{s}} = 1\,\frac{\mathrm{proton}}{1.602 \times 10^{-19} \cdot \mathrm{s}} \tag{C.4}$$

Combining equation (C.3) and equation (C.4) and dividing by the area of the silicon wafer gives us the flux

$$\varphi = 0.06 \times 10^{-9}\,\frac{\mathrm{proton}}{1.602 \times 10^{-19} \cdot \mathrm{s}} \cdot \frac{1}{0.20\,\mathrm{cm} \cdot 0.25\,\mathrm{cm}} = 7.5 \times 10^{9}\left[\frac{\mathrm{protons}}{\mathrm{s} \cdot \mathrm{cm}^2}\right] \tag{C.5}$$

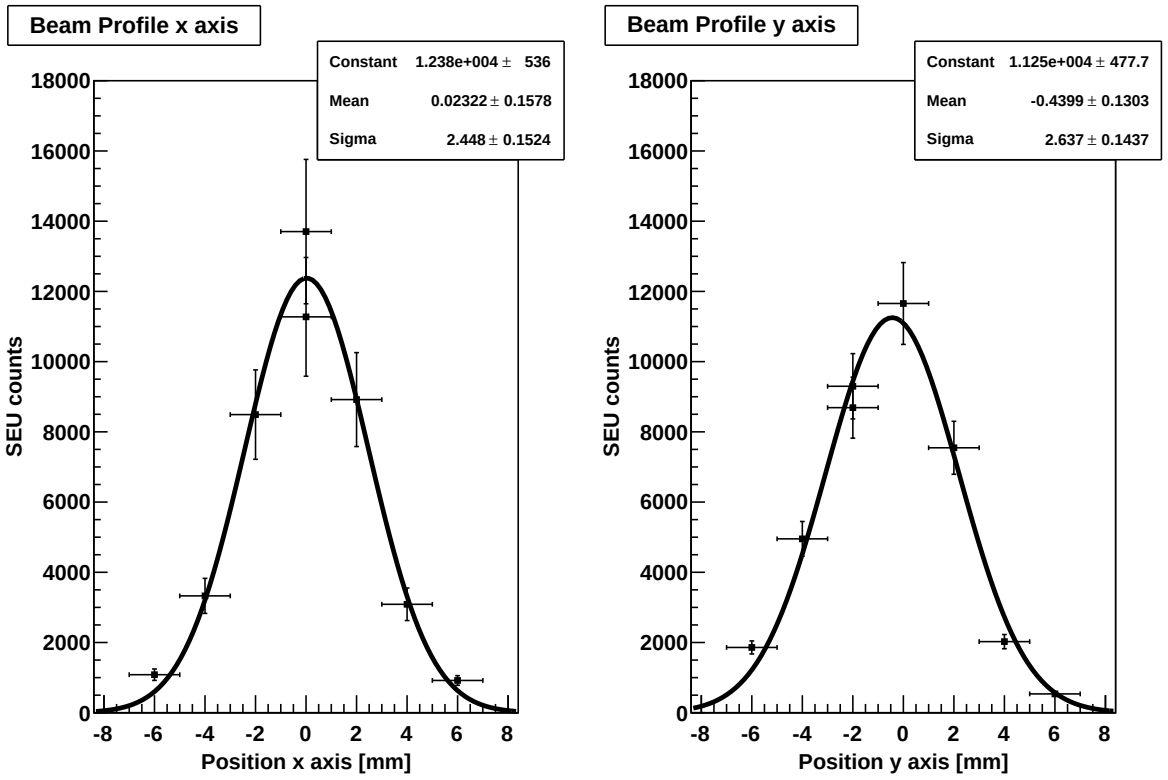


Figure C.3: *The number of SEU counts at each position along the x- and y-axis fitted with a Gaussian fit. The uncertainty in the number of counts comes from fluctuations in the beam of 15 %. The uncertainty in the position is due to the size of the laser point used for positioning. The Gaussian fit was created with ROOT [65].*

The cross section can then be found by dividing the number of SEUs by the fluence

$$\sigma_{SEU} = \frac{\#\text{SEU}}{\text{Time} \cdot \varphi} \tag{C.6}$$

Three runs of 15 s in the center of the beam was done with SRAM1b to calculate the cross section, the fluence was 1.13×10^9.

Run	SEUs	$\sigma_{SEU}\left[\text{SEU}\frac{\text{cm}^2}{\text{p}}\right]$
1	6274	5.65×10^{-8}
2	6010	5.41×10^{-8}
3	6144	5.53×10^{-8}

Table C.2: *Number of counts and resulting cross section for three runs with the 1 Mb SRAM.*

The reason why the number of SEUs are about half in the calibration run compared to the beam-profile is because the SRAM used in the beam-profile measurements was stuck at 1.5 V instead of 2.45 V, see section 6.2 for details about voltage differences

versus sensitivity. The difference doesn't have any impact on the calibration measurement.

Uncertainty

A number of different uncertainties are present in the cross section calculations, but the three most dominant are

- Beam intensity: The intensity was assumed to be stable, but fluctuations of about 15 % could be seen during runs.
- Positioning laser: The laser beam had a resolution of 1 mm. This is indicated in the beam-profile plots. When recalculating the intensity of the beam for a position 1 mm in either direction a difference in 9 % can be seen. This can be considered a systematic error, as the device or laser was not moved between the three measurements. It is thus included after calculating the weighted mean.
- Time taking: The runs were timed by hand with a common stopwatch, this induces an uncertainty of 1 s.
- Statistical: The number of SEUs detected is Poisson distributed and has thus an uncertainty of $\frac{1}{\sqrt{N_{SEU}}}$.

In addition to these uncertainties there are also small errors in fitting of the beam-profile and the difference between the sensitive area of the silicon wafer and the whole silicon wafer. The final uncertainty is therefore estimated to be 20 % random and 9 % systematic.

The weighted mean of these three measurements is then

$$\sigma_{SEU} = (5.52 \pm 0.81) \times 10^{-8}\,\mathrm{SEU}\frac{\mathrm{cm}^2}{\mathrm{p}} \tag{C.7}$$

Scintillator Calibration

During our measurements it was experimented with different placement of the scintillator in reference to the beam-pipe. This section explains the general method of calibrating the scintillator.

The proportional constant between the number of SEUs and the number of scintillator counts was found by placing the calibrated SRAM in the center of the beam and having the scintillator next to the beam path. For each run the proportional number was calculated.

$$\mathrm{Ratio} = \frac{\#\mathrm{SEU}}{N_{Scint}} \tag{C.8}$$

The fluence in a given run can be found from equation (C.6) by rearranging

$$\Phi = \frac{\#\mathrm{SEU}}{\sigma_{SEU}} \tag{C.9}$$

and inserting equation (C.8)

$$\varphi = \frac{\text{Ratio} \cdot N_{Scint}}{\sigma_{SEU}} \tag{C.10}$$

The factor $\frac{\text{Ratio}}{\sigma_{SEU}}$ will be referred to elsewhere in this work as 1/scint and is given in $[1/(\text{N}_{\text{scint}}\,\text{cm}^2)]$.

Appendix D

Complete data tables for irradiation tests

D.1 Accelerated neutron-beam testing at PTB

Table D.1 lists all data for all runs at PTB. The distance d is the distance from the detector to the center of neutron production. For 5.8 MeV and 8.5 MeV this is 31.04 cm which includes 29.44 cm from the surface of the SRAM to the beam pipe exit and 1.6 cm from the beam exit to the center of the gas target. When running at 14.8 MeV the gas target was exchanged with a tritium target and the 1.6 cm does not need to be added. MS is the measurement number as used by the beam control and monitoring system. PLC counts are the counts recorded by the Precision Long Counter (PLC) during a run and is given per steradian. The calibration factor is used to calculate the fluence per steradian from the PLC counts. The average flux is the effective fluence divided by the time.

The PLC counts can be converted to fluence given in neutrons / cm^2, as explained in appendix B

$$\Phi(d) = \frac{N_{PLC} \cdot C_{PLC}}{\pi(d \cdot \tan(\cos^{-1}\left(1 - \frac{1}{2\pi}\right)))^2} \tag{D.1}$$

Run	MS	d [cm]	Energy [MeV]	Sram	SEUs	Time [s]	PLC counts [1/sr]	PLC Calibration	Eff. Φ	Ave. φ	Comment
1	4	31.04	8.5	1	5.00	1500	882370	688800	2.55×10^8	1.70×10^5	
1	4	31.04	8.5	2	7.00	1500	882370	688800	2.55×10^8	1.70×10^5	
1	4	31.04	8.5	3	0.00	1500	882370	688800	0.00	0.00	Not connected
1	5	31.04	8.5	1	15.00	3047	941788	688800	5.17×10^8	1.70×10^5	
1	5	31.04	8.5	2	8.00	3047	941788	688800	5.17×10^8	1.70×10^5	
1	5	31.04	8.5	3	0.00	3047	941788	688800	0.00	0.00	Not connected
2	3-5	31.04	5.7	1	26.00	52576	6090245	498200	2.42×10^9	4.60×10^4	
2	3-5	31.04	5.7	2	0.00	52576	6090245	498200	0.00	0.00	Not connected
2	3-5	31.04	5.7	3	0.00	52576	6090245	498200	0.00	0.00	Not connected
3	3-7	31.04	8.5	1	39.00	17085	5706654	548700	2.50×10^9	1.46×10^5	
3	3-7	31.04	8.5	2	40.00	17085	5706654	548700	2.50×10^9	1.46×10^5	
3	3-7	31.04	8.5	3	0.00	17085	5706654	548700	0.00	0.00	Not connected
3	8-16	31.04	8.5	1	89.00	30330	10160616	548700	4.44×10^9	1.47×10^5	
3	8-16	31.04	8.5	2	80.00	30330	10160616	548700	4.44×10^9	1.47×10^5	
3	8-16	31.04	8.5	3	65.00	30330	10160616	548700	4.44×10^9	1.47×10^5	
3	18	31.04	8.5	1	14.00	2699	904353	548700	3.96×10^8	1.47×10^5	
3	18	31.04	8.5	2	7.00	2699	904353	548700	3.96×10^8	1.47×10^5	
3	18	31.04	8.5	3	4.00	2699	904353	548700	3.96×10^8	1.47×10^5	
4	6-8	31.04	5.7	1	16.00	59778	6835554	473200	2.58×10^9	4.31×10^4	
4	6-8	31.04	5.7	2	22.00	59778	6835554	473200	2.58×10^9	4.31×10^4	
4	6-8	31.04	5.7	3	9.00	59778	6835554	473200	2.58×10^9	4.31×10^4	
5	3-8	29.44	14.8	1	83.00	25655	15645331	102900	1.43×10^9	5.56×10^4	
5	3-8	29.44	14.8	2	91.00	25655	15645331	102900	1.43×10^9	5.56×10^4	
5	3-8	29.44	14.8	3	54.00	25655	15645331	102900	1.43×10^9	5.56×10^4	
5	9-10	29.44	14.8	1	6.00	13734	7168805	102900	6.54×10^8	4.76×10^4	Mounted backwards
5	9-10	29.44	14.8	2	14.00	13734	7168805	102900	6.54×10^8	4.76×10^4	Mounted backwards
5	9-10	29.44	14.8	3	8.00	13734	7168805	102900	6.54×10^8	4.76×10^4	Mounted backwards
5	11-15	29.44	14.8	1	0.00	22605	12890889	102900	0.00	0.00	Not connected
5	11-15	29.44	14.8	2	0.00	22605	12890889	102900	0.00	0.00	Not connected
5	11-15	29.44	14.8	3	57.00	22605	12890889	102900	1.18×10^9	5.20×10^4	

Table D.1: *Complete table of data from runs at PTB.*

D.2 HEH testing at CERF

Table D.2 lists all data for all runs at CERF. The PIC counts can be converted to particles on target by multiplying by 22400. The simulated fluences for the three energy regions is given in table 6.8. Run 11–13 was done at wall position F1 for SRAM2ab and 3a, the other runs were done at position F4 for all devices.

During the measurement there was a problem with the program doing the data processing where the DAQs were not set up to sample continuously causing some sample-loss between each sample capture. The sample loss was later quantified by sampling from a signal generator and comparing with a pulse counter. The loss was found to be 1.2 % for box1 and 51.2 % for box2.

Run 1–5 on SRAM1a, run 6 for SRAM1b and run 1–6 for SRAM2b has been multiplied by 1.512 while run 6 for SRAM1a, run 1–5 for SRAM1b and run 1–6 for SRAM2a and 3a has been multiplied by 1.012.

Run	SRAM1a		SRAM1b		SRAM2a		SRAM2b		SRAM3	
	PIC	SEUs	PIC	SEUs	Pic	SEUs	PIC	SEUs	PIC	SEUs
1	1.96×10^6	3	1.96×10^6	12	0.00	0	1.96×10^6	188	1.96×10^6	893
2	1.37×10^6	8	1.37×10^6	2	7.26×10^5	59	6.51×10^5	73	1.37×10^6	133
3	4.11×10^6	14	4.11×10^6	20	1.55×10^6	143	2.47×10^6	214	4.11×10^6	497
4	6.96×10^6	26	6.69×10^6	25	2.84×10^6	235	7.51×10^5	53	6.96×10^6	1656
5	7.13×10^5	2	7.13×10^5	1	7.13×10^5	57	7.13×10^5	59	7.13×10^5	213
6	3.12×10^6	8	3.12×10^6	29	0.00	0	6.40×10^5	42	3.12×10^6	843
7	7.44×10^5	4	7.44×10^5	2	0.00	0	3.72×10^5	28	7.44×10^5	56
8	3.28×10^6	8	3.28×10^6	11	1.78×10^6	161	6.27×10^5	61	3.28×10^6	438
9	6.55×10^6	27	6.55×10^6	34	3.67×10^5	56	4.56×10^6	390	6.55×10^6	1576
10	2.06×10^6	9	2.06×10^6	17	2.06×10^6	150	1.89×10^6	158	2.06×10^6	172
11	1.51×10^6	3	1.51×10^6	1	7.93×10^5	71	2.64×10^5	21	7.93×10^5	90
12	2.89×10^6	6	2.89×10^6	17	2.89×10^6	5	2.89×10^6	18	2.89×10^6	1
13	2.77×10^6	11	2.17×10^6	23	2.77×10^6	15	2.77×10^6	5	2.77×10^6	21
14	1.37×10^7	70	1.37×10^7	67	1.37×10^7	64	1.37×10^7	52	1.37×10^7	103

Table D.2: *Complete table of data from runs at CERF.*

D.3 Accelerated proton-beam testing at OCL

Table D.3 to table D.11 lists all the data for the given devices. For each day that the devices were tested, a beam profile was created to find the center and the dispersion of the beam. In addition a proportionality constant was found between the calibrated SRAM and the scintillator which was used for converting the scintillator counts to fluence.

D.3.1 Cross section tables

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
08.12	1	2.4	Normal	323	122648	5.53×10^9	5.57×10^{-14}	9.0×10^{-15}
08.12	2	2.4	Normal	361	122771	5.54×10^9	6.22×10^{-14}	1.0×10^{-14}
08.12	3	1.5	Normal	316	86566	3.90×10^9	7.72×10^{-14}	1.2×10^{-14}
08.12	4	1.5	Normal	485	121674	5.49×10^9	8.43×10^{-14}	1.3×10^{-14}
08.12	5	3.4	Normal	407	122853	5.54×10^9	7.01×10^{-14}	1.1×10^{-14}
08.12	6	3.4	Normal	362	120877	5.45×10^9	6.33×10^{-14}	1.0×10^{-14}
08.12	7	1.5	Idle	327	97615	4.40×10^9	7.08×10^{-14}	1.1×10^{-14}
08.12	8	1.5	Idle	384	118182	5.33×10^9	6.87×10^{-14}	1.1×10^{-14}
09.12	1	1.5	Normal	527	134248	5.87×10^9	8.57×10^{-14}	1.3×10^{-14}
09.12	2	1.5	Normal	478	124092	5.42×10^9	8.41×10^{-14}	1.3×10^{-14}
09.12	3	2.4	Normal	356	118731	5.19×10^9	6.54×10^{-14}	1.0×10^{-14}
09.12	4	2.4	Normal	326	125103	5.47×10^9	5.69×10^{-14}	9.2×10^{-15}
09.12	5	3.4	Normal	363	122364	5.35×10^9	6.47×10^{-14}	1.0×10^{-14}
09.12	6	3.4	Normal	328	112632	4.92×10^9	6.36×10^{-14}	1.0×10^{-14}
09.12	7	1.5	Idle	371	108225	4.73×10^9	7.48×10^{-14}	1.2×10^{-14}
09.12	8	1.5	Idle	292	96709	4.23×10^9	6.59×10^{-14}	1.1×10^{-14}

Table D.3: *Complete table of data for SRAM1c at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
18.11	1	2.4	Normal	1803	245370	1.59×10^9	6.8×10^{-14}	1.0×10^{-14}
18.11	2	2.4	Normal	1884	253112	1.64×10^9	6.9×10^{-14}	1.1×10^{-14}
08.12	1	1.5	Normal	4983	58256	2.63×10^9	1.13×10^{-13}	1.7×10^{-14}
08.12	2	1.5	Normal	5310	60541	2.73×10^9	1.16×10^{-13}	1.8×10^{-14}
08.12	3	3.4	Normal	2166	42377	1.91×10^9	6.76×10^{-14}	1.0×10^{-14}
08.12	4	3.4	Normal	3024	58589	2.64×10^9	6.82×10^{-14}	1.0×10^{-14}
08.12	5	1.5	Idle	4271	60749	2.74×10^9	9.29×10^{-14}	1.4×10^{-14}
08.12	6	1.5	Idle	4139	58637	2.64×10^9	9.33×10^{-14}	1.4×10^{-14}

Table D.4: *Complete table of data for SRAM2c at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
09.12	1	3.4	normal	2948	49265	2.15×10^9	1.63×10^{-13}	2.5×10^{-14}
09.12	2	3.4	normal	3550	47662	2.08×10^9	2.03×10^{-13}	3.1×10^{-14}
09.12	3	2.4	idle	1454	47573	2.08×10^9	8.34×10^{-14}	1.3×10^{-14}
09.12	4	2.4	idle	1530	46339	2.02×10^9	9.01×10^{-14}	1.4×10^{-14}
09.12	5	3.4	idle	1400	51227	2.24×10^9	7.46×10^{-14}	1.1×10^{-14}
09.12	6	3.4	idle	1462	46609	2.04×10^9	8.56×10^{-14}	1.3×10^{-14}

Table D.5: *Complete table of data for SRAM3b at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
18.11	1	2.4	Normal	6589	258247	1.67×10^9	5.88×10^{-14}	9.0×10^{-15}
09.12	1	2.4	Normal	8540	43861	1.92×10^9	6.64×10^{-14}	1.0×10^{-14}
09.12	2	3.5	Normal	7357	35773	1.56×10^9	7.01×10^{-14}	1.1×10^{-14}
09.12	3	2.4	Idle	4458	38427	1.68×10^9	3.96×10^{-14}	6.0×10^{-15}
09.12	4	2.4	Idle	5457	43746	1.91×10^9	4.25×10^{-14}	6.5×10^{-15}
09.12	5	1.5	Idle	5534	41471	1.81×10^9	4.55×10^{-14}	6.9×10^{-15}
09.12	6	1.5	Idle	5548	42441	1.85×10^9	4.46×10^{-14}	6.8×10^{-15}

Table D.6: *Complete table of data for SRAM4 at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
18.11	1	2.4	Normal	474	243521	1.57×10^9	3.59×10^{-14}	5.7×10^{-15}
18.11	2	2.4	Normal	495	247408	1.60×10^9	3.69×10^{-14}	5.9×10^{-15}
09.12	1	2.4	Normal	572	47445	2.07×10^9	3.29×10^{-14}	5.2×10^{-15}
09.12	2	2.4	Normal	569	48131	2.10×10^9	3.23×10^{-14}	5.1×10^{-15}
09.12	3	3.3	Normal	624	47089	2.06×10^9	3.62×10^{-14}	5.7×10^{-15}
09.12	4	3.3	Normal	599	48563	2.12×10^9	3.37×10^{-14}	5.3×10^{-15}
09.12	5	1.1	Idle	1208	47385	2.07×10^9	6.96×10^{-14}	1.1×10^{-14}
09.12	6	1.1	Idle	1235	46751	2.04×10^9	7.21×10^{-14}	1.1×10^{-14}
09.12	7	2.4	Idle	647	48207	2.11×10^9	3.66×10^{-14}	5.7×10^{-15}
09.12	8	2.4	Idle	630	47616	2.08×10^9	3.61×10^{-14}	5.7×10^{-15}
09.12	9	3.3	Idle	635	46808	2.05×10^9	3.70×10^{-14}	5.8×10^{-15}

Table D.7: *Complete table of data for SRAM5 at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
09.12	1	1.8	Normal	2684	48929	2.14×10^9	3.33×10^{-14}	5.1×10^{-15}
09.12	2	1.8	Normal	2940	50201	2.19×10^9	3.55×10^{-14}	5.4×10^{-15}

Table D.8: *Complete table of data for SRAM6 at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
18.11	1	2.4	Normal	481	488697	3.16×10^9	3.63×10^{-14}	5.8×10^{-15}
18.11	2	2.4	Normal	517	496047	3.21×10^9	3.84×10^{-14}	6.1×10^{-15}
09.12	1	2.4	Normal	342	49880	2.18×10^9	3.74×10^{-14}	6.0×10^{-15}
09.12	2	2.4	Normal	335	48278	2.11×10^9	3.79×10^{-14}	6.1×10^{-15}

Table D.9: *Complete table of data for SRAM7 at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
09.12	1	3.0	Normal	1006	34802	1.52×10^9	3.50×10^{-14}	5.4×10^{-15}
09.12	2	3.0	Normal	1015	34530	1.51×10^9	3.56×10^{-14}	5.5×10^{-15}
09.12	3	2.5	Normal	1039	36059	1.58×10^9	3.49×10^{-14}	5.4×10^{-15}
09.12	4	2.5	Normal	1020	35937	1.57×10^9	3.44×10^{-14}	5.3×10^{-15}
09.12	5	3.4	Normal	1176	41438	1.81×10^9	3.44×10^{-14}	5.3×10^{-15}
09.12	6	3.4	Normal	1169	41573	1.82×10^9	3.41×10^{-14}	5.3×10^{-15}
09.12	7	2.5	Idle	1093	38855	1.70×10^9	3.41×10^{-14}	5.3×10^{-15}

Table D.10: *Complete table of data for SRAM8 at OCL.*

Date	Run	Voltage [V]	Mode	SEUs	Scint.	Fluence [1/cm^2]	σ [cm^2/bit]	σ_σ [cm^2/bit]
09.12	1	2.4	Idle	3934	49526	2.16×10^9	4.33×10^{-13}	6.6×10^{-14}
09.12	2	2.4	Idle	4326	47227	2.06×10^9	5.00×10^{-13}	7.6×10^{-14}
09.12	3	1.5	Idle	4350	51120	2.23×10^9	4.64×10^{-13}	7.1×10^{-14}
09.12	4	1.5	Idle	3232	48496	2.12×10^9	3.64×10^{-13}	5.5×10^{-14}

Table D.11: *Complete table of data for SRAM9 at OCL.*

D.3.2 18. November 2010

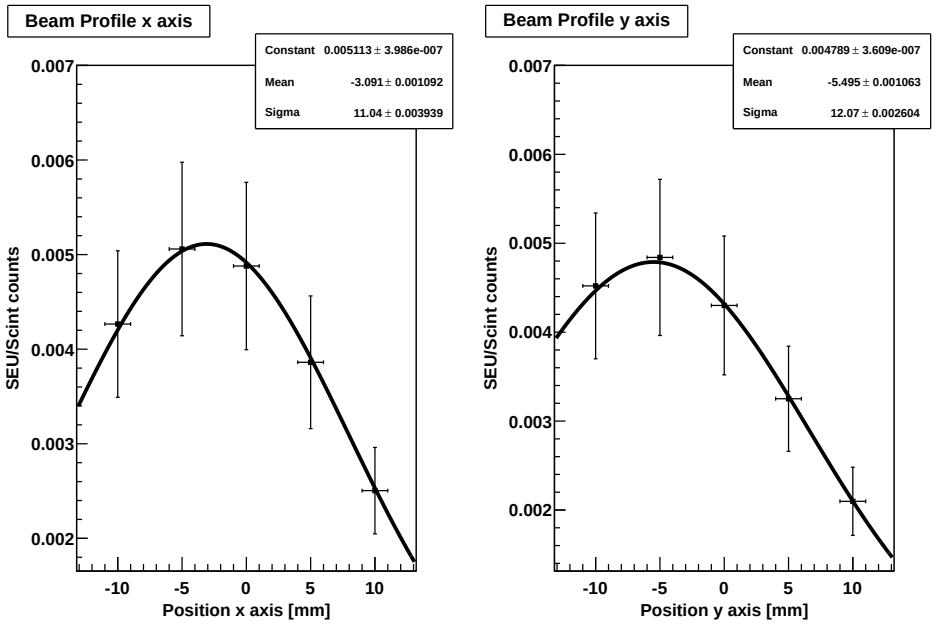


Figure D.1: *Beam profile for 18.11.2010. The Gaussian fit was created with ROOT [65].*

The cross section used for calculating the 1/scint factor is $(5.52 \pm 0.81) \times 10^{-8}\,\mathrm{cm}^2$ found from the first calibration measurements. See appendix C for further details. The device tested this day was placed at position ($-2.5\,$mm, $-2.5\,$mm, $130\,$cm). The scintillator was placed at ($25\,$cm, $0\,$cm, $175\,$cm) which gives an angel of $8°$.

Run	Time [s] [s]	Scint.	SEUs	1/scint [1/(N_{scint} cm^2)]	$\sigma_{1/scint}$ [1/(N_{scint} cm^2)]
1	300	771	2.10×10^6	6.64×10^3	1.2×10^3
2	300	743	2.08×10^6	6.46×10^3	1.2×10^3
3	120	391	1.03×10^6	6.89×10^3	1.3×10^3
4	120	340	1.03×10^6	5.98×10^3	1.1×10^3

Mean	6.46×10^3
STD	5.9×10^2
STD[%]/100	0.10

Table D.12: *Proportionality measurement between scintillator and SRAM1a for 18.11.2010.*

D.3.3 8. December 2010

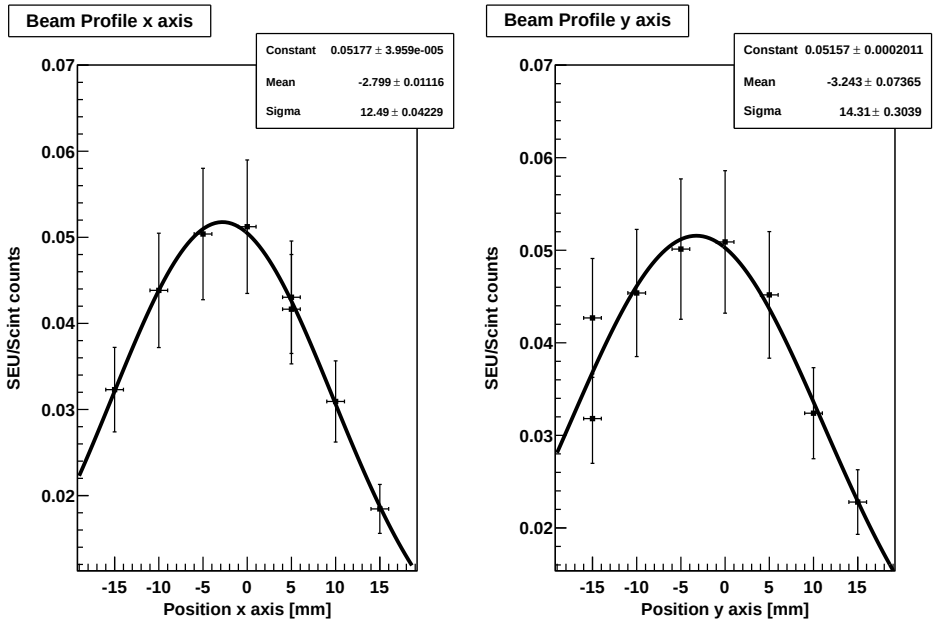


Figure D.2: *Beam profile for 8.12.2010. The Gaussian fit was created with ROOT [65].*

The cross section used for calculating the 1/scint factor is $(1.14 \pm 0.13) \times 10^{-6}\,\mathrm{cm}^2$ and is found by taking the weighted mean of run 1 and 2 of SRAM2c at 18.11.2010. The device tested this day was placed at (0 mm, 0 mm, 130 cm). The scintillator was placed at (25 cm, 75 cm, 27 cm) which gives an angel of 20°.

Run	Scint.	SEUs	1/scint	$\sigma_{1/scint}$
1	43600	2231	4.47×10^4	6.9×10^3
2	36382	1890	4.54×10^4	7.0×10^3
3	46540	2405	4.52×10^4	6.9×10^3

Mean	4.51×10^4
STD.	4.0×10^3
STD[%]/100	0.10

Table D.13: *Proportionality measurement between scintillator and SRAM2c for 8.12.2010.*

D.3.4 9. December 2010

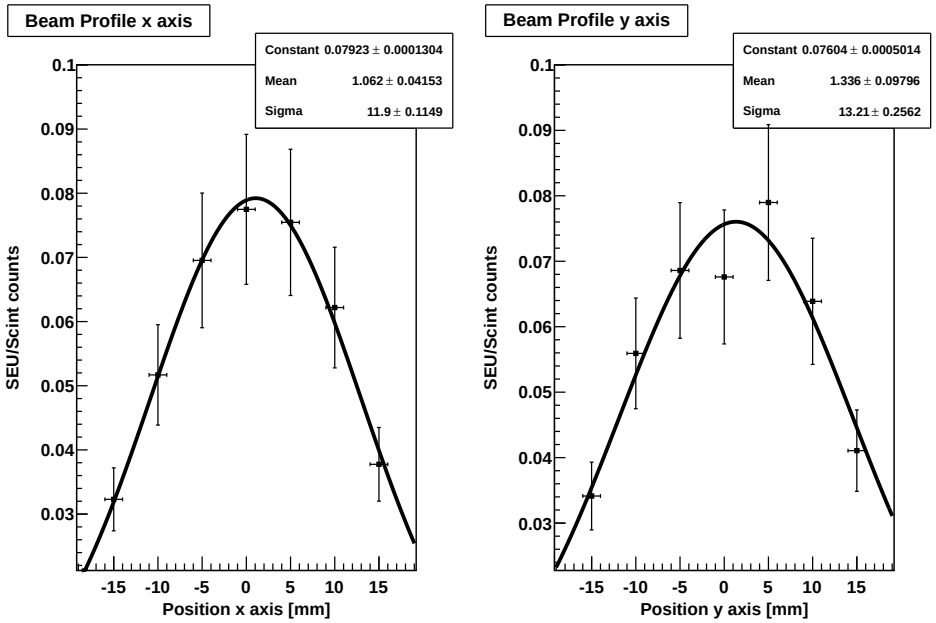


Figure D.3: *Beam profile for 9.12.2010. The Gaussian fit was created with ROOT [65].*

The cross section used for calculating the 1/scint factor is $(1.14 \pm 0.13) \times 10^{-6}\,\mathrm{cm}^2$ and is found by taking the weighted mean of run 1 and 2 of SRAM2c at 18.11.2010. The device tested this day was placed at ($-2.5\,$mm, $-2.5\,$mm, $130\,$cm). The scintillator was placed at ($25\,$cm, $75\,$cm, $27\,$cm) which gives an angel of $20°$.

Run	Scint.	SEUs	1/scint	$\sigma_{1/scint}$
1	46221	2249	4.25×10^4	6.5×10^3
2	47639	2400	4.40×10^4	6.8×10^3
3	47624	2432	4.46×10^4	6.9×10^3

Mean	4.37×10^4
STD.	3.9×10^3
STD[%]/100	0.10

Table D.14: *Proportionality measurement between scintillator and SRAM2c for 9.12.2010.*

D.4 Thermal neutron testing at IFE

Run	SRAM	Size [Mb]	Volt [V]	Mode	Time [s]	σ_{time} [s]	SEU1	SEU2	SEU3	SEU4	Φ [1/cm^2]	σ_Φ [1/cm^2]	σ_{SEU} [cm^2]	$\sigma_{\sigma_{SEU}}$ [cm^2]
2	2d	64	2.4	Normal	515	7	80	61	71	51	2.8×10^{9}	2.8×10^{8}	1.4×10^{-15}	1.6×10^{-16}
3	2d	64	1.5	Normal	273	12	54	76	57	64	1.5×10^{9}	1.6×10^{8}	2.5×10^{-15}	3.2×10^{-16}
4	2d	64	3.4	Normal	539	3	53	64	75	64	2.9×10^{9}	3.0×10^{8}	1.3×10^{-15}	1.5×10^{-16}
5	2d	64	2.4	Idle	428	3	61	73	78	45	2.3×10^{9}	2.3×10^{8}	1.6×10^{-15}	1.9×10^{-16}
7	1c	4	2.4	Normal	1214	2	8	11	11	10	6.6×10^{9}	6.6×10^{8}	1.4×10^{-15}	2.7×10^{-16}
8	1c	4	1.5	Normal	1222	2	15	17	19	15	6.7×10^{9}	6.7×10^{8}	2.4×10^{-15}	3.7×10^{-16}
9	1c	4	3.4	Normal	1695	2	14	12	11	8	9.3×10^{9}	9.3×10^{8}	1.2×10^{-15}	2.1×10^{-16}
10	1c	4	1.5	Idle	1019	2	16	12	10	7	5.6×10^{9}	5.6×10^{8}	1.9×10^{-15}	3.5×10^{-16}
11	7	16	2.4	Normal	751	2	83	72	43	117	4.1×10^{9}	4.1×10^{8}	4.6×10^{-15}	5.2×10^{-16}
12	7	16	3.3	Normal	597	2	58	52	39	99	3.3×10^{9}	3.3×10^{8}	4.5×10^{-15}	5.4×10^{-16}
13	7	16	2.4	Idle	596	2	69	74	46	90	3.3×10^{9}	3.3×10^{8}	5.1×10^{-15}	5.9×10^{-16}
14	5	16	2.4	Normal	726	2	0	52	0	51	4.0×10^{9}	4.0×10^{8}	1.5×10^{-15}	2.2×10^{-16}
15	5	16	3.3	Normal	722	2	0	57	0	61	3.9×10^{9}	4.0×10^{8}	1.8×10^{-15}	2.4×10^{-16}
16	5	16	1.0	Idle	477	2	0	94	0	101	2.6×10^{9}	2.6×10^{8}	4.5×10^{-15}	5.5×10^{-16}
17	5	16	1.0	Idle	318	2	0	74	0	78	1.7×10^{9}	1.7×10^{8}	5.2×10^{-15}	6.7×10^{-16}
18	5	16	2.4	Idle	599	2	0	42	0	51	3.3×10^{9}	3.3×10^{8}	1.7×10^{-15}	2.4×10^{-16}
19	8	18	3.0	Normal	701	2	0	101	0	0	3.8×10^{9}	3.8×10^{8}	1.4×10^{-15}	2.0×10^{-16}
20	8	18	3.4	Normal	632	2	0	105	0	0	3.5×10^{9}	3.5×10^{8}	1.6×10^{-15}	2.2×10^{-16}
21	8	18	2.5	Normal	630	2	0	101	0	0	3.4×10^{9}	3.4×10^{8}	1.6×10^{-15}	2.2×10^{-16}
22	8	18	1.3	Normal	449	2	0	109	0	0	2.5×10^{9}	2.5×10^{8}	2.4×10^{-15}	3.3×10^{-16}
23	8	18	1.3	Idle	378	2	0	102	0	0	2.1×10^{9}	2.1×10^{8}	2.6×10^{-15}	3.7×10^{-16}
24	4	64	2.4	Normal	301	2	0	282	0	0	1.6×10^{9}	1.7×10^{8}	2.6×10^{-15}	3.0×10^{-16}
26	4	64	3.4	Normal	305	2	0	231	0	0	1.7×10^{9}	1.7×10^{8}	2.1×10^{-15}	2.5×10^{-16}
27	4	64	1.5	Normal	301	2	0	247	0	0	1.6×10^{9}	1.7×10^{8}	2.2×10^{-15}	2.7×10^{-16}
28	4	64	1.3	Normal	120	2	0	260	0	0	6.6×10^{8}	6.7×10^{7}	5.9×10^{-15}	7.0×10^{-16}
29	4	64	2.4	Idle	300	2	0	256	0	0	1.6×10^{9}	1.6×10^{8}	2.3×10^{-15}	2.7×10^{-16}
30	2d (Cd)	64	2.4	Normal	601	2	81	80	95	95	3.3×10^{9}	3.3×10^{8}	1.6×10^{-15}	1.8×10^{-16}
32	9	16	2.4	Normal	1008	2	155	88	24	75	5.5×10^{9}	5.5×10^{8}	3.7×10^{-15}	4.2×10^{-16}
33	9	16	1.5	Normal	778	2	131	21	22	119	4.3×10^{9}	4.3×10^{8}	4.1×10^{-15}	4.8×10^{-16}
34	9	16	3.4	Normal	758	2	166	75	177	27	4.1×10^{9}	4.1×10^{8}	6.4×10^{-15}	7.1×10^{-16}
35	9	16	1.3	Normal	471	2	20	22	35	72	2.6×10^{9}	2.6×10^{8}	3.4×10^{-15}	4.5×10^{-16}
36	9	16	1.5	Idle	659	2	103	106	77	84	3.6×10^{9}	3.6×10^{8}	6.1×10^{-15}	6.9×10^{-16}
37	9	16	2.4	Idle	734	2	324	97	85	118	4.0×10^{9}	4.0×10^{8}	9.3×10^{-15}	1.0×10^{-15}
38	3b	32	2.4	Normal	359	2	81	40	83	92	2.0×10^{9}	2.0×10^{8}	4.5×10^{-15}	5.2×10^{-16}
39	3b	32	1.5	Normal	644	2	70	48	41	44	3.5×10^{9}	3.5×10^{8}	1.7×10^{-15}	2.1×10^{-16}
40	3b	32	3.4	Normal	610	2	77	94	66	90	3.3×10^{9}	3.3×10^{8}	2.9×10^{-15}	3.3×10^{-16}
41	3b	32	2.4	Idle	643	2	60	52	55	38	3.5×10^{9}	3.5×10^{8}	1.7×10^{-15}	2.1×10^{-16}
42	3b	32	1.5	Idle	578	2	49	43	34	55	3.2×10^{9}	3.2×10^{8}	1.7×10^{-15}	2.1×10^{-16}
43	2d	48	2.4	Normal	2132	2	0	230	257	280	1.2×10^{10}	1.2×10^{9}	1.3×10^{-15}	1.4×10^{-16}
44	2d (Cd)	48	2.4	Normal	458	2	0	98	112	93	2.5×10^{9}	2.5×10^{8}	2.4×10^{-15}	2.8×10^{-16}

Table D.15: *Complete table of data from runs at IFE.*

Appendix E

VHDL code

Table table E.2 lists the different VHDL files used in the detector. Files are available from http://svn.ift.uib.no/svn/raddet/

File	Description
adr_counter.vhd	Contains the RAM address counter
clk_div.vhd	Divides the clock down from 100 MHz to a specified frequency
debounce.vhd	Debounces an external incoming signal. Used for changing of settings through jumpers on the header mounted on the detector.
error_communicator.vhd	Collects the SEUs and MBUs from the counter in addition to other status information and prepares the next packet to be sent to the computer. Checks every incoming packet if the packet is meant for the particular detector and answers if it is.
error_counter.vhd	Counts the number of SEUs and MBUs detected for one of the SRAMs.
error_transmit.vhd	Used in older design to count the SEUs and pulse them out through the interface.
gen_functions.vhd	Contains some generic functions like counting the number of ones in a bit vector and majority voting. Moved to a package to ease readability of main code.
hamming.vhd	Contains all functionality related to decoding and encoding single error correcting hamming.
interface.vhd	Top level design. Initializes all other modules.
por.vhd	Power on reset functionality to provide a stable reset signal for three consequential clock cycles to initialize the firmware properly.

(a)

Table E.2: *List of VHDL files used in firmware design.*

File	Description
ram_config_pkg.vhd	This file contains parameters for all SRAMs used, values are stored in an array so it's only needed to change one line in the top level design when recompiling for another device.
rs485.vhd	Finite state machine for sending and receiving data over the RS485 interface.
scint_counter.vhd	Basic hamming encoded pulse counter meant for the scintillator input.
sram_ctrl.vhd	Controls the reading and writing to the SRAM.
state_machine.vhd	Main finite state machine. Controls the SRAM controller and the address counter. Analyses the data received from the SRAM and notifies the error counter if any found.
synchronizer.vhd	Used on inputs to combat metastability.

(b)

Table E.2: *List of VHDL files used in firmware design.*

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