Optimum power control of a battery energy storage system

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Acknowledgment

This master thesis is the final step in completing the Energy master program at Western Norway University of Applied Science (HVL). Additionally, at University of Bergen (UiB) the fields of renewable resources and consumption have been completed due to the importance of sustainable mindset in the energy sector. The specialization within electric power engineering can be characterized by subjects including power electronics and control systems. The motivation for this thesis have been significantly impacted by the merging of these focus areas. It has been natural to write about a subject in which I have had the most progress since I became an engineer in 2020. Additionally, it has been meaningful to comprehensively study a subject that have been receiving an increasingly amount of interest in modern times.

This thesis have been completed in the period August 2021 to June 2022. It has posed a great and fun challenge which symbolizes an excellent end to my five years studying electric power engineering at HVL. First of all, I would like to thank both HVL and UiB for providing competent and supportive lectures, in a great learning environment. Secondly, I am specially grateful for the assistance given by associate professor Emil Cimpan, who has been a great teacher and supervisor, providing useful tips, knowledge and support. In addition, I would like to express my gratitude to Eirik Haustveit for providing support and solutions in Simulink. Lastly, I would like to thank my family, which has been a tremendous support and patient throughout the project period. As a final note, I hope that this thesis may represent inspiration, guidance and break the barrier for fellow student successors that wishes to address the relatively unknown territory of self healing power grids.

Abstract

The future power transmission and distribution needs to account for a continuously growing demand. Increasing regulations regarding sustainable and renewable energy provides incentives to increase the research within the field of Power Electronics (PE) and Energy Storage Systems (ESS). The utility networks of today holds large potential towards future automation in order to increase power grid efficiency, stability and reliability. By integrating proper dynamic monitoring in the utility substations and end users, the power grid may achieve intelligent control over a new, modernized smart grid such as microgrids. These modern grids contains centralized control over stationary generators in conjunction with distributed generation (DG) such as Renewable Energy Sources (RES), Photovoltaic (PV) cells, Battery Energy Storage System (BESS) and other ESS services by the means of bidirectional communication between all system components. This enables automatic control of smart grid features, such as Peak Load Shaving (PLS) and Self Healing (SH) microgrids.

The increased interest and progress within battery technologies have paved way for BESS as a suitable DG application. Using Direct Current (DC), a high-efficient Power Conversion Stage (PCS) is required in order to interface the batteries with the utility. Promising PCS such as 3-level Active Neutral Point Clamped (ANPC), Cascaded Full Bridge (CHB) and Modular Multilevel Converters (MMC) are reviewed in detail in order to provide an optimized PCS for a BESS model. Furthermore, optimization of active power control, voltage balancing and Constant Current (CC) charging has been conducted in order to decelerate battery degradation. Controllers have been mathematically modelled in order to provide refined transfer function based tuning through Matlab PID-Tuner Application.

The implemented model consists of Li-ion batteries and Insulated Gate Bipolar Transistors (IGBT), interfaced using a Bidirectional AC (BDAC) CHB converter and a Bidirectional DC (BDC) Phase Shift Full Bridge (PSFB) converter. It has been tested through Simulink simulations upon PLS and SH scenarios. A digital control logic has been designed in order to realize PLS, using two real load cases from Sogn og Fjordane Energi (SFE). Moreover, a SH control design has been proposed and tested in the event of utility disruption for three different load cases, including scenarios of variable change in loads.

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Abbreviations

AMS	Advanced Measurement System
ANPC	Active Neutral Point Clamped
BDAC	Bidirectional AC
BDC	Bidirectional DC
BESS	Battery Energy Storage System
BJT	Bipolar Junction Transistor
BMS	Battery Management System
C-rate	Charge rate
CB	Circuit Breaker
CC	Constant Current
CCM	Continuous Conduction Mode
CHB	Cascaded Full (H) Bridge
CPU	Central Processing Unit
CT	Current Transformer
CV	Constant Voltage
DAB	Dual Active Bridge
DCM	Discontinuous Conduction Mode
DG	Distributed Generation
DOD	Depth of Discharge
DSCC	Dual Star Chopper Cell
DSP	Digital Signal Processor
DST	Dynamic Stress Test
ESS	Energy Storage System
FFT	Fast Fourier Transform
GI	Galvanic Isolation
GTO	Gate Turn-off Thyristor
GUI	Graphical User Interface
HF	High Frequency
HV	High Voltage
IC	Integrated Circuit
ICT	Information and Communication Technology
IGBT	Insulated-Gate Bipolar Transistor
KCL	Kirchhoff's Current Law

KVL	Kirchhoff's Voltage Law
LF	Loop Filter
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	Medium Voltage
NVE	Norwegian Water Resources and Energy Directorate
OS	Overshoot
PCS	Power Conversion Stage
PD	Phase Detector
PE	Power Electronics
PLL	Phase Locked Loop
PLS	Peak Load Shaving
PPU	Power Processing Unit
PS	Phase Shift
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Source
ROGI	Reduced Order Generalized Integrator
RTU	Remote Terminal Unit
SCADA	Supervisory Control And Data Acquisition
SDBC	Single-Delta Bridge Cell
SDG	Sustainable Development Goals
SH	Self Healing
SOC	State of Charge
SRF	Synchronous Reference Frame
SSBC	Single-Star Bridge Cell
THD	Total Harmonic Distortion
UN	United Nations
UPS	Uninterruptible Power Supply
VCO	Voltage Controlled Oscillator
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1 Introduction

1.1 Motivation

The first dc machine was connected for electric power generation distributed in New York city in 1882 [104]. Nikola Tesla showed only a few years later that alternating power systems were more efficient for large distant power transmission, making it significantly more economically feasible. Since then, there has been an enormous development within the field of electric power generation, transmission and distribution. Today, electric power is distributed across the entire world, which is implying a severely increased system complexity. In 2015, the United Nations (UN) presented guidelines in form of Sustainable Development Goals (SDGs) [107]. Additionally, international conventions, such as the Kyoto Protocol and Paris Agreement manifests climate obligations. The essence is to achieve a reduction in emission levels and a responsible consumption of energy and merchandise, all in which may be improved by modernizing the electric power sector.

As electric power demand is continuously increasing, the energy source is of vital importance in order to reach these goals. Figure 1.1 shows the estimated energy consumption in the U.S. in 2016 [58]. It gives an overview of the energy cycle from power source (left) to source of consumption (right). It shows that fossil fuels such as coal and natural gas represents 62.13 % of the total electricity generation. RES including wind, solar, hydro and geothermal generates 13.52 % of the total power consumption. This ratio needs a drastic improvement if the 1.5°C from the Paris Agreement is to be achieved. However, perhaps more interestingly, figure 1.1 shows that there is a significant potential in improving the electric power transmission and distribution efficiency. One way to improve this, is by supporting the grid supplied by fossils or nuclear energy sources. In general, these power stations have a slow reaction time to rapid change in loads and load peaks. It is therefore desired that these are adjusted to supply the rated power, and that load peaks are supplied using more rapid energy power plants (peak plants) such as hydro power [67]. PLS may also be achieved using ESS by storing energy using thermal, electrolytic, compressed air, flywheel or pumped hydroelectric storage [97].

Introducing RES, ESS and modern monitoring composes a future smart grid. A smart grid utilizes Information and Communication Technology (ICT) integrated in conjunction with the traditional components of the grid. It facilitates a two way communication between the generation and consumer to ensure that grid and load conditions can be measured and fed back to the main monitoring system such as SCADA [78]. Implementing attributes from a smart grid results in a more efficient use of the available energy. Additionally, automation function can be added so that safety, reliability and stability is improved compared to a conventional one-way grid [12]. One of these features is shown

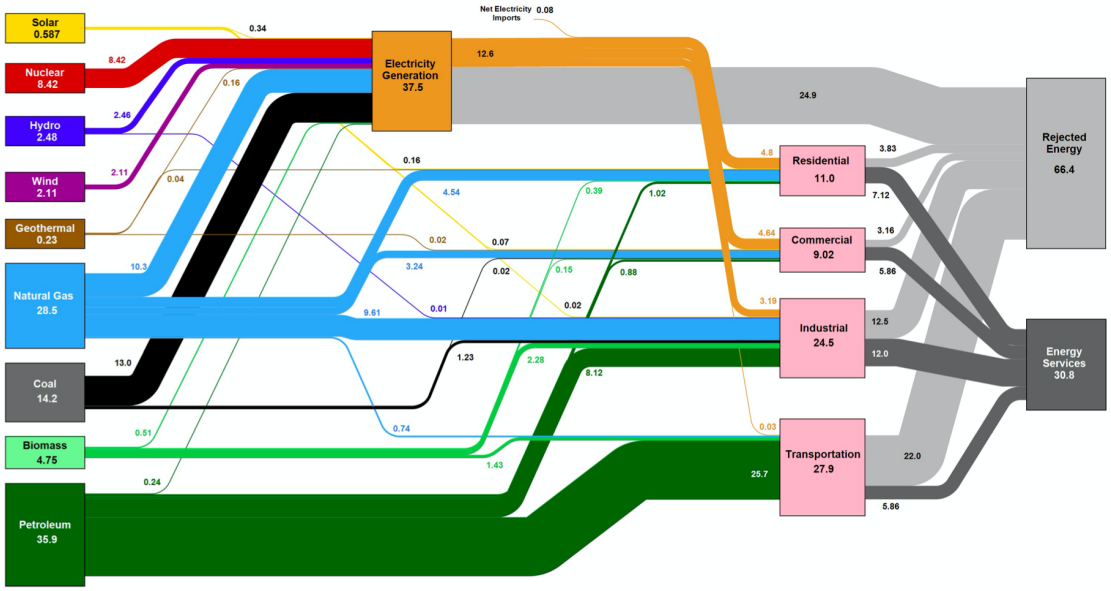


Figure 1.1: Estimated U.S. energy consumption by energy source (2016) [58].

in figure 1.2 which depicts the foundation of SH power grids [12]. When a fault scenario arises, the utility substations monitoring devices detects the fault in which trips the corresponding Circuit Breaker (CB). Fault detection systems may include short circuit and earth fault indicators using current transformers in the substations [81]. Some of these indicators can communicate with impedance protection relays that has the capability of calculating the distance from the substation relay to the fault location, such as [103]. Having proper utilization of these components makes way for self healing algorithms implemented in the Central Processing Units (CPU).

Self healing can be particular useful in combination with ESS. Battery Energy Storage Systems (BESS) have in recent years received increased interest due to the progress made in the field of Power Electronics (PE) and battery technology. Using semiconductor devices such as IGBTs or MOSFETs have paved way for revolutionary control methods of high voltage grid-tied converters. This makes BESS suitable for load leveling and shaving in stead of peaking plants during normal circumstances [2]. In this case, a BESS application functions as an integrated part of the future smart grid. Another positive effect by using BESS is that it can compose as the main part of a microgrid. The key feature of the microgrid is the ability to work independently in island mode, when it is isolated from the utility grid. This is typically of interest during faults or other external disturbances [51].

Electric power in Norway is mainly generated in hydro power plants. In recent years, the

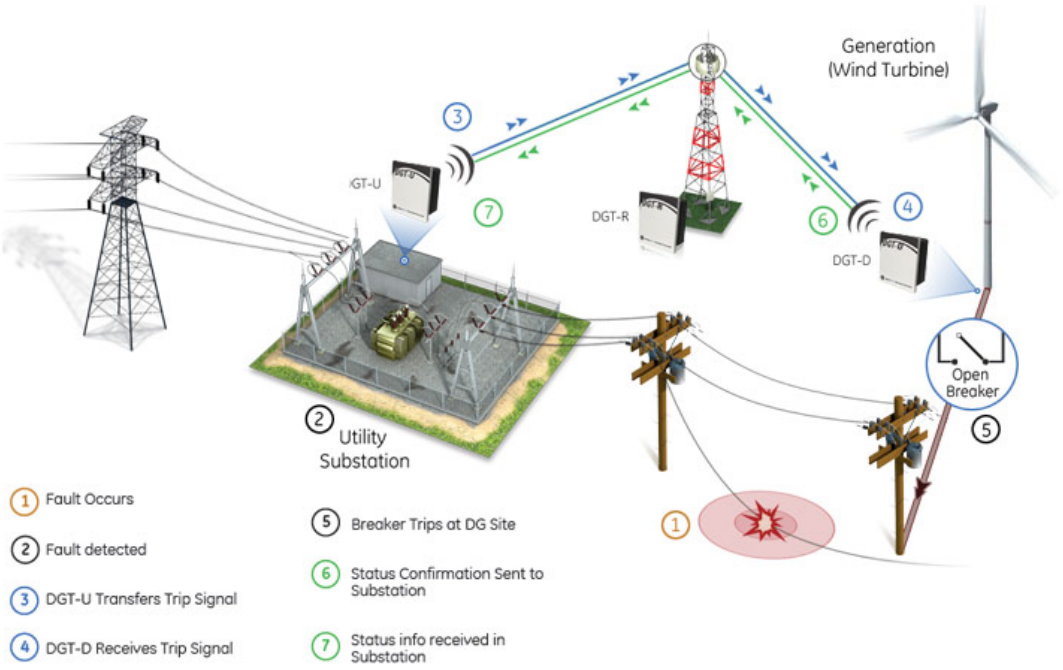


Figure 1.2: Self healing smart grid [12].

grid has become powered by RES in increasing fashion, which is expected to increase even further [93]. Distributing BESS across the distribution grid may lead to many benefits. First of all by improving power quality through PLS. Variable renewables, though powered by power quality controllers, can be the source of power grid instability. On the other side, they can charge distributed batteries at night time. Wind is the movement of heat, so that it tends to increase in strength at nighttime when temperatures are lower [67]. Using this energy to charge BESS would enable an increased amount of water magazine preservation at night. From this point of view, a BESS would represent synergies with the existing and future wind parks. At last, it may provide smart grid features by including SH capabilities. The topology of the power grid is wide spread, having substations in locations that very often are difficult to access. Short circuit or earth faults may be time-consuming to correct. Figure 1.3 shows a statistical overview of fault events across the sub-22kV distribution grids operated by Statnett [61]. It can be seen that the major part of fault in both overhead lines and cables leads to power outages. Typically, these faults are physically caused by downfalls of trees or snow on overhead lines. Physical factors leading to cable faults are typically human activity or frost. Additionally, faults caused by corrosion, aging and water trees penetrating the cable isolation may occur [79]. Furthermore, figure 1.3 shows the number of faults on transformer and component level per 2018. It shows that the number of faults causing power outages on average is much higher than temporary faults. In this regard, the

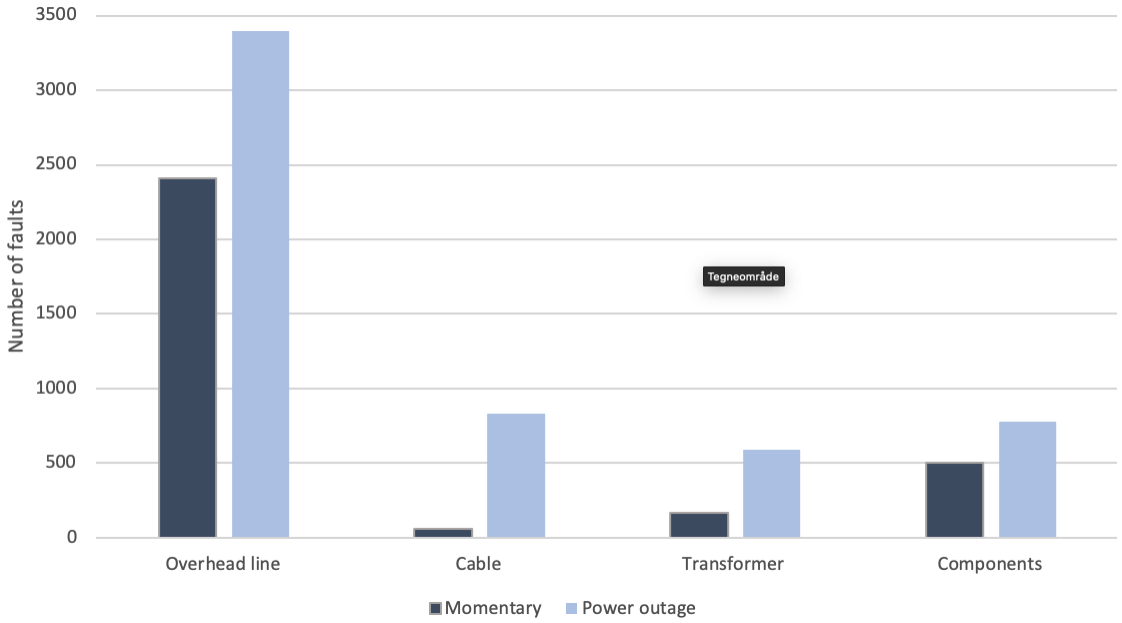


Figure 1.3: Total number of faults in grid powered by Statnett, divided into temporary and permanent faults.

pillars of components represents the total number of faults in CB-equipment and High Voltage (HV) protection gear. In other words, the climate and weather conditions in Norway makes the utility grid prone to faults. This emphasizes the point of arranging for future smart grid technology. Self healing grids will isolate the error, sustaining normal power supply to the majority of the consumers.

1.2 Objective

The main objective of this thesis is to optimize the functionality of a grid-tied BESS through modelling, design and simulation. This optimization process has two main sub-tasks:

- Study, analyze and design an efficient power electronic converter topology for grid-tied BESS applications.
- Study, analyze and design a suitable power control in a PLS and SH oriented BESS in order to test the functionality of the PE design towards future smart grid features.

Choosing a complex power electronic topology for power conversion composes some challenges. Primarily, there are several balancing control strategies that can be applied

for the chosen converters. The focus in this thesis is to balance each individual module capacitor voltage. Secondly, in the complex field of smart grid technology, the project objective is directed towards PLS and SH control.

1.3 Structure

This chapter has introduced the motivation and objective of this thesis. It has provided a general foundation of central terms regarding BESS, and explained the need for an increased focus towards this area. Chapter 2 breaks down the BESS components in detail, and reviews the corresponding theory within the field of power electronics, battery technology and control systems. Chapter 3 is focusing on modelling, design and realization of a $5kW$ BESS model. It represents the work that has been conducted throughout the project period. Chapter 4 presents simulation results of the proposed BESS model. It includes a detailed analysis of controller response, power quality and functionality of the PLS and SH control design. Chapter 5-7 contains model discussions, conclusion and future work respectively. In addition, an Appendix has been added to collect heavy calculations, Simulink design and contributing data.

2 Background

The increasing employment of ESS is characterized by increasing electric power demand and the growing focus towards RES and green energy. ESS can distribute electric power generation all the way to end users through the transmission and distribution network. A financial study regarding the benefits and need for ESS has been conducted in [34]. It summarizes the ESS utility areas in 13 different electricity services, all of which contributes to an increased total grid stability, reliability, socioeconomic growth, and reduced carbon footprint. Figure 2.1 shows an overview of ESS distributed across three subcategories depending on the application [47]. This illustrates the wide area of use regarding both batteries, flywheels and supercapacitors. The scope of this thesis lies withing large scale BESS-applications in the Medium Voltage (MV) grid. BESS consists of three main parts, namely the battery, power conversion and control [52]. In the following sections, these component will be reviewed in detail and selected for design implementation accordingly.

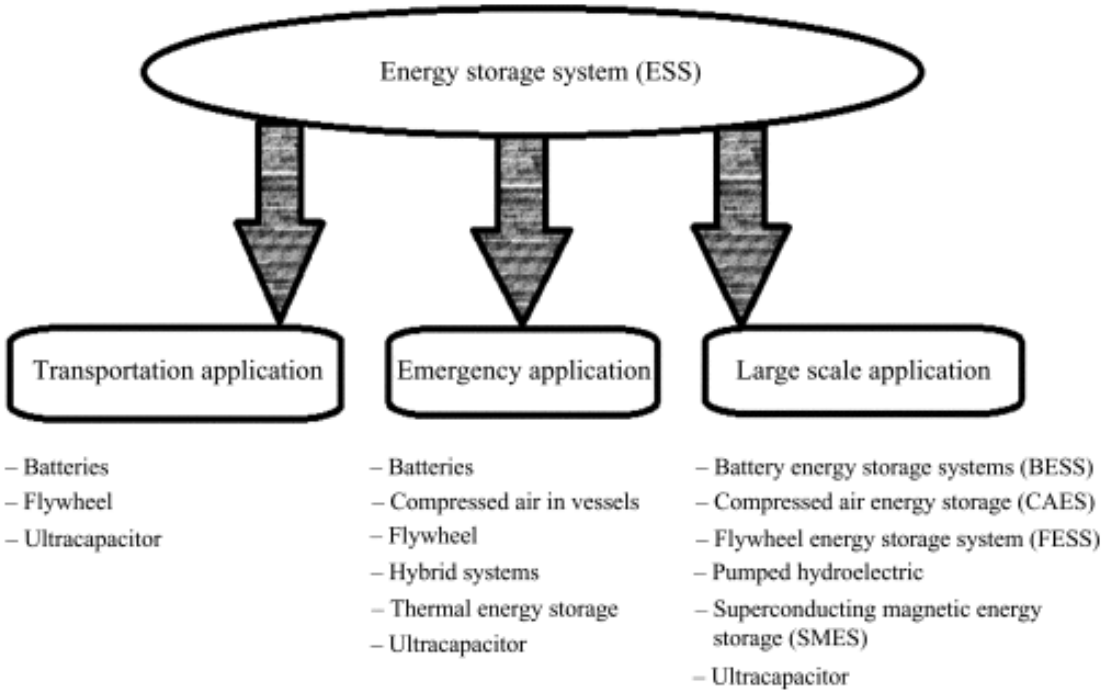
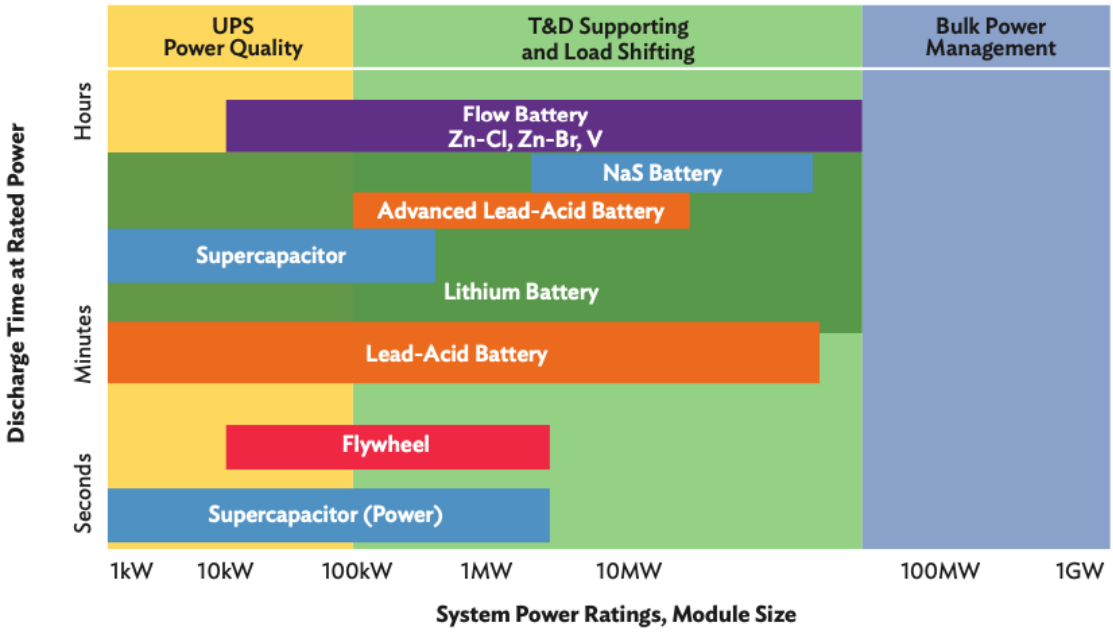


Figure 2.1: Categorization of the different energy storage systems [47].

2.1 Battery

BESS is distinguished from the other ESS services by its rapid response characteristics, high energy density, and wide area of utility [52]. Depending on application, BESS can

be scaled after necessary requirements by connecting batteries in series or parallel across the dc-link nodes. Series connection imposes a wider area of design freedom regarding system voltage, while a parallel connection collects individual battery currents to design a wider range of power output. Figure 2.2a illustrates the span of different battery types in terms of system power ratings and energy density. As previously mentioned, the application spectrum of mechanical flywheels and electric supercapacitors are also wide. However, the inclusion of these in figure 2.2a shows the lack of energy density in these ESS, which means that they have a limited discharge time range compared to batteries. In terms of energy density, the flow batteries are capable of delivering almost its entire range of stored charge due to different battery operating principles, which places them on top in figure 2.2a [49]. However, due to its relatively new technology, they are in early testing stages [53]. As a consequence, they are place third in figure 2.2b in terms of energy density. Li-ion battery technology on the other hand are fully settled considering the integration of its operating principles. They are providing the widest range of both power output and energy density, and scores the highest for round trip efficiency. The technology in this area are still being researched, which has resulted in the arrival of solid state Li-ion batteries [48]. This technology as of today, lacks proper validation so that the market still awaits mass-production. In general, these batteries may provide higher energy density through safer energy storage, due to the absence of liquids. Furthermore, figure 2.2b shows the characterization of the batteries existing on the market per today, using data from 2017 [52]. The results of this summary are consistent with [11], in which emphasizes that Li-ion batteries are the most suited batteries for grid-tied BESS applications. As a result, Li-ion batteries are implemented in the forthcoming model.



(a) Overview of different ESS with reference to power output and discharge rates.

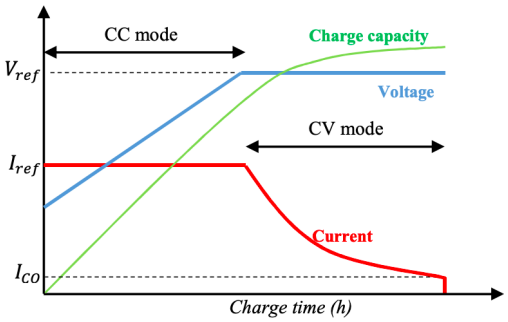
	Energy density (kW/kg)	Round Trip Efficiency (%)	Life Span (years)	Eco-friendliness
Li-ion	1st 150–250	1st 95	1st 10–15	1st Yes
NaS	2nd 125–150	2nd 75–85	2nd 10–15	2nd No
Flow	3rd 60–80	3rd 70–75	4th 5–10	4th No
Ni-Cd	4th 40–60	4th 60–80	3rd 10–15	3rd No
Lead Acid	5th 30–50	5th 60–70	5th 3–6	5th No

(b) Comparison of battery types in BESS.

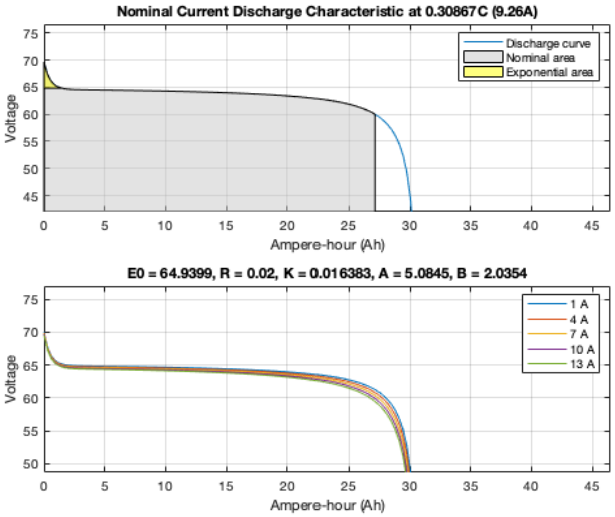
Figure 2.2: Comparison of different ESS technologies towards applications [52].

In terms of battery implementation, the charging and discharging characteristics must be

accounted for. This is shown in figure 2.3, which is illustrating characteristics both for charge and discharge respectively. Figure 2.3a shows the theoretical charging curve for voltage and current split into a constant current (CC) and constant voltage (CV) region [59]. In the initial charging phase, the controls should facilitate CC charge mode in order to preserve battery lifetime. That is, by feeding the battery with a steady current regardless of battery SOC [96]. Moreover, this phase transposes into the CV charge mode once the voltage reaches nominal levels. The CC charging is more efficient than the CV charging due to having uncontrolled currents in CV-mode. These may be excessive which causes temperature surges [65]. Furthermore, figure 2.3b show the discharging characteristics from the model implemented $30Ah$ battery. Details can be found in Appendix C. Here there are no CC or CV regions, which represents that its not necessary to consider them in the control system design [99]. In other words, the implemented model controls will take this into consideration, as explained in detail in chapter 3. The ideal operating area is shown by the grey nominal area in figure 2.3b. The exponential phase marked yellow, is the initial voltage curve when the battery is discharged from 100 % SOC. As explained later in this section, the control system should limit the SOC threshold levels in order to preserve battery lifetime. The bottom plot in figure 2.3b shows the internal voltage of the battery during a discharge of 1-13A with a step difference of 3A up to a total of $30Ah$. As demonstrated, the battery maintains higher levels of voltage during smaller current discharges.



(a) Charging characteristics of Li-ion battery [59].



(b) Discharge characteristics of the implemented battery of $30Ah$ and $I_N = 9.26A$.

Figure 2.3: Li-ion battery charge and discharge characteristics.

Additionally, Battery Management Systems (BMS) are needed in order to maintain safe battery operation and preserve battery lifetime. Battery protection systems may include

physical HV-protection gear in the BESS substation, or protective measures implemented in the control system. One such example can be an integrated circuit (IC) PWM modulator in which can provide voltage protection, current limiting and soft start functionalities [2]. Moreover, faults scenarios may be dealt with by using bypass switches as an integrated part of the PCS. For more advanced PE arrangement such as multilevel converters, this bypass can be implemented towards each individual module [72]. This bypass arrangement has been tested and verified in [8] with promising results. Furthermore, both battery temperatures and SOC measurements should be monitored through the BMS. The battery operating region regarding these parameters are significant with respect to battery degradation. Figure 2.4 is included to demonstrate battery degradation regarding State of Charge (SOC) levels, although similar curves can be represented by degradation as a function of temperature. As shown, the battery lifetime decreases proportional to the amount of depth of discharge (DOD) of each cycle. In addition, figure 2.4 shows improved battery lifetime if the DOD and SOC never reaches 0 % or 100 %. Seeing as the optimum thresholds vary upon each type of Li-ion battery, this model operates with the threshold limits of $35 < SOC < 80$ %.

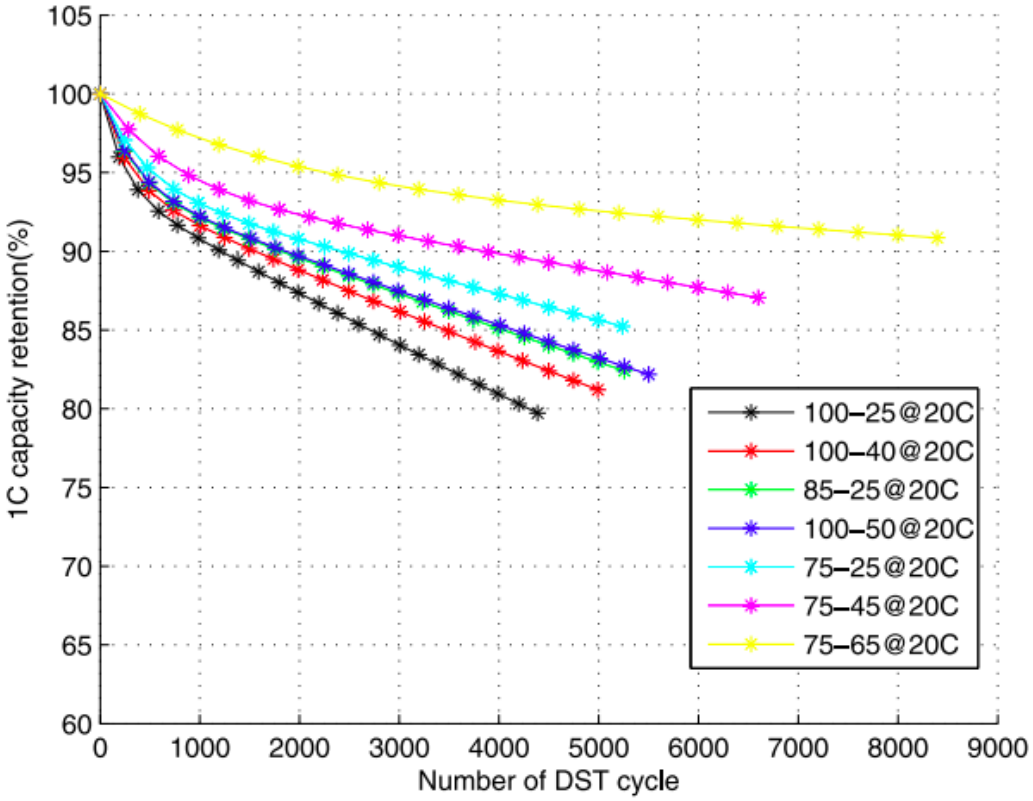
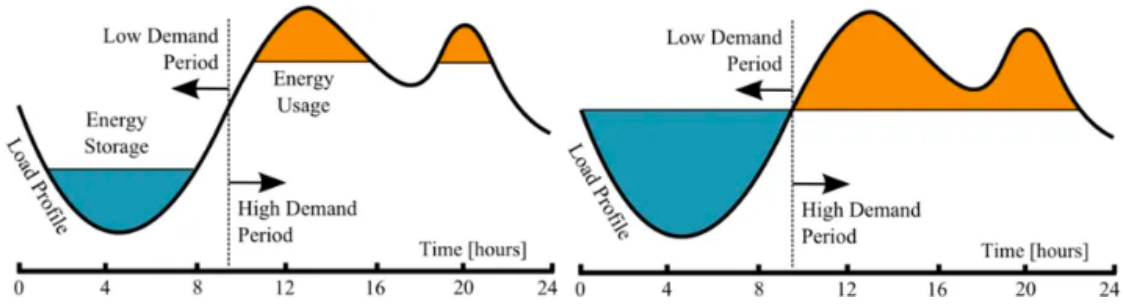


Figure 2.4: Battery degradation curve as a function of Dynamic Stress Testing (DST) at different SOC levels [63].

The desired magnitude of the bidirectional battery currents depends on which battery type that the BESS is using. This is referred to as C-rate, in which offers the optimum charging and discharging current with respect to the nominal battery current. A study of battery deterioration as a function of the applied charging current has been conducted in [57], which has found that the C-rate is consequential with respect to the total battery cycle life. Therefore, technical information about the physical batteries should be carefully studied before physical testing and implementation.

2.2 Future grid technologies

Chapter 1 introduced the concept of smart grid, stating the benefits connected to upgrading the existing grid. This section presents features such as PLS and SH in detail. The PLS concept consists of both load shaving and load leveling. Figure 2.5 introduces the main difference between the two terms. Figure 2.5a refers to shaving the load peaks in order to provide frequency support in the event of heavy load connection or disconnection. Furthermore, these peaks induce surges in the cost of energy, which makes it desirable to reduce their magnitudes [29]. Peak shaving algorithms are mostly directed toward load predictive models in order to optimize the total economic aspect of power flow, such as in [78, 50]. Load leveling on the other hand seeks to maintain the average grid power throughout the day in order to secure a reliable, stable and qualitative power supply. Load prediction models should be implemented in these ESS in order to optimize the desired magnitude and direction of the power to reach this goal. The blue area in figure 2.5 represents the amount of charging power in periods of low demand. In contrast, the orange area represents the desired amount of discharge in order to maintain steady power flow. In the further analysis, both methods are referred to as PLS, where load leveling is designed and tested in simulation.



(a) Peak shaving.

(b) Load leveling.

Figure 2.5: The concept of peak load shaving [41].

Recent development within the smart grid technology has led to the concept of micro-

grids. The main factor separating a microgrid from a smart grid described in 1.1, is its capability of self-sustaining electric power [83]. This is characterized by local influence through a microgrid controller, which results in complete management of the power generation and load distribution. Figure 2.6 illustrates the microgrids independence of the main utility supply.

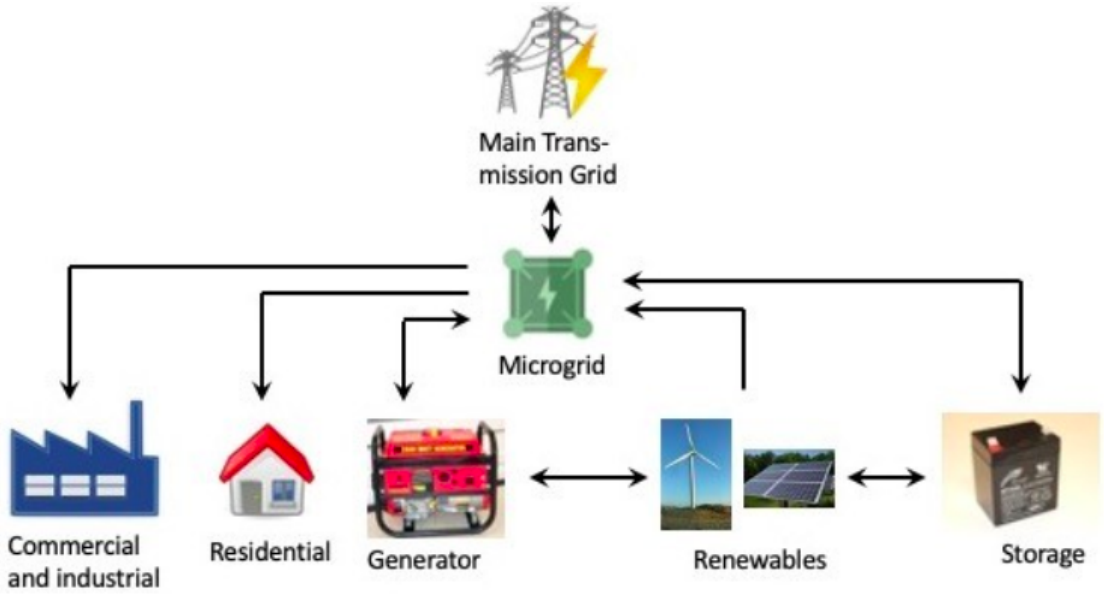


Figure 2.6: Microgrid structure which obtains automatic control of power generation and distribution independent from the utility [89].

Controllers realize smart grid features such as PLS and SH upon a defined area that composes the microgrid. Control of power generation includes power sharing between generators and ESS, and optimalizes power flow between RES and ESS. Depending on the microgrid scale and system rating, the loads may be both industrial or residential, representing cities or neighborhoods. Figure 2.7 shows a one line diagram of a BESS in conjunction with the utility. This microgrid is the foundation of the proposed SH-control design in this project. The assumption is that proper power flow measurement is installed and that the circuit breakers (CB) in each utility substation are remotely controlled. The load power connected to each substation is represented by "$P_{L1} - P_{L6}$".

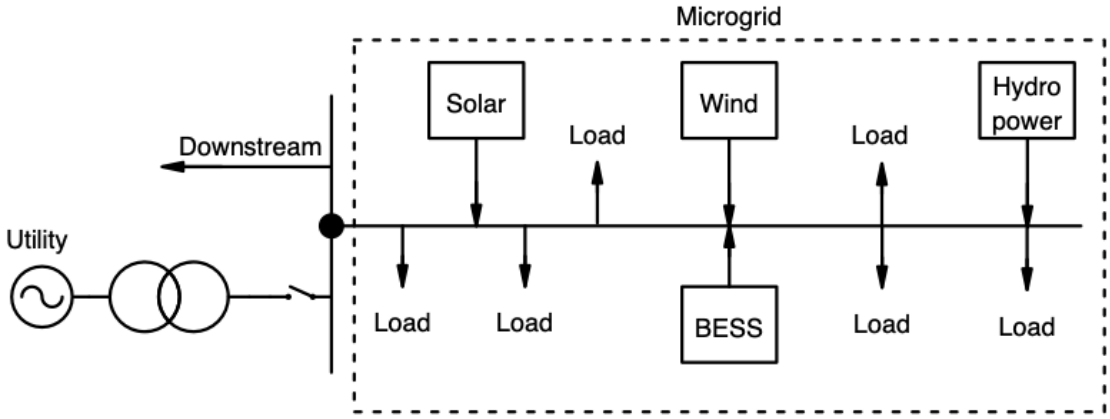
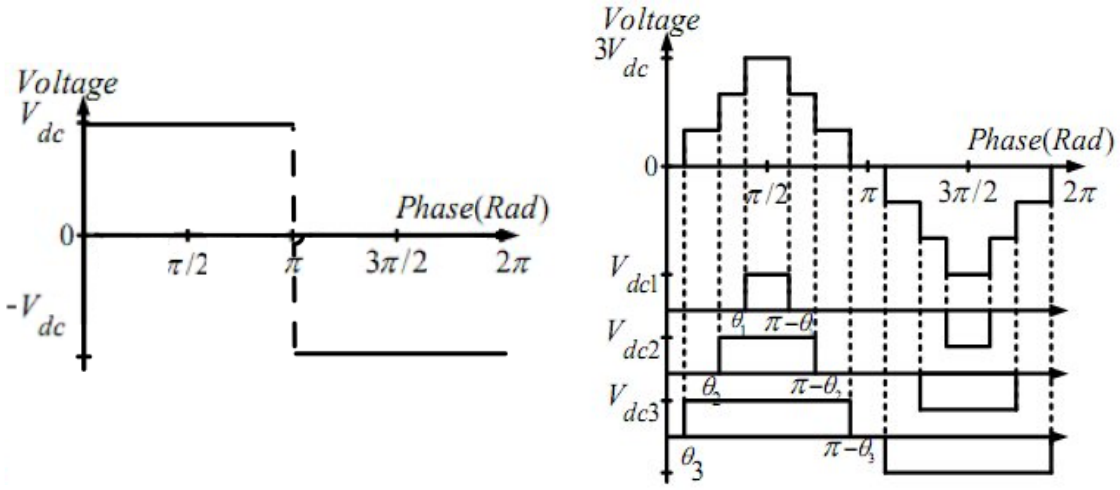


Figure 2.7: One-line diagram illustration of a microgrid.

2.3 Power conversion

2.3.1 BDAC converter topology

The facilitating technology that distributed generation (DG) relies upon, lies within the field of power electronics. The research of sustainability and efficiencies within this field includes the improvement of semiconductor components, new and better power electronic topologies and more profound control system accuracy. There has been innumerable studies concerning efficiencies using different topologies, and several articles have reviewed a selection suitable for utility-scale BESS applications [45, 70, 35]. Converters can be classified by the number of voltage levels at the converter output. The magnitude depends on the bridge topology. A half-bridge that contains two semiconductors is characterized by the operation magnitude of $V_{dc}/2$. 2-level full bridges may operate in the range between $+V_{dc}$ to $-V_{dc}$ as shown in figure 2.8a. 3-level full bridge characteristics are in the range $+V_{dc}$, 0 and $-V_{dc}$. Increasing voltage levels is beneficial with respect to filtering needs and harmonics distortion at the output waveforms. Cascading converters with two or three voltage levels can lead to the waveform shown in figure 2.8b. This is a 7-level converter, where each 2-level converter delivers the voltage connected across its dc-link, and the next bridge is phase-shifted with respect to the previous. This Phase Shift (PS) is reached in the Pulse Width Modulation (PWM) strategy, making PS-PWM exceptionally suited for multilevel converters. Furthermore, this increases the degree of freedom in generating the ac voltages [27]. Additional advantages include smaller filters, improved voltage waveforms and a reduction in the required maximum switching frequency. The latter consequently improves switching losses and conducted Electromagnetic Interference (EMI) [62].

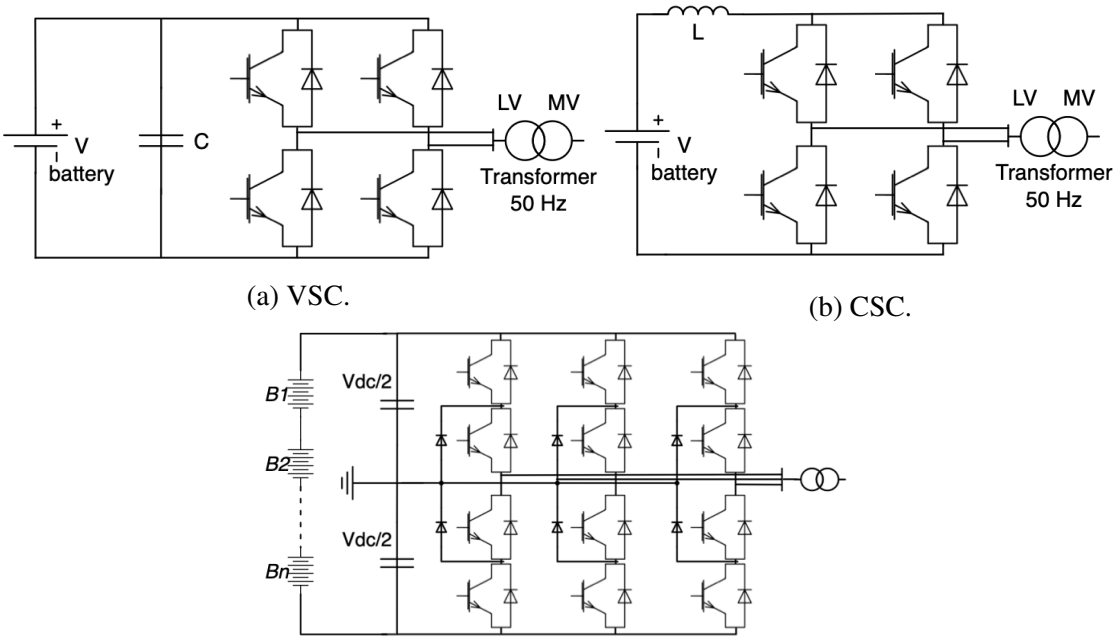


(a) 2-level

(b) 7-level

Figure 2.8: Voltage levels for 2-level and 7-level H-bridge converter [24].

In general, the converters can be divided into two categories, mainly with and without the use of a line-frequency transformer. Conventional 2-level Voltage Source Converters (VSC), as shown in figure 2.9a, requires a transformer in order to boost voltage from battery levels to MV grid levels. Other 2-level converters traditionally used in the ac stage of BESS applications are the Z-Source Converter (ZSC) and Quasi-Z-Source converter (qZSC) [70]. Additionally, there have been experiments regarding the use of current source converters (CSC) in DG-applications [76, 33]. Usually, the VSC is preferred over the CSC in grid-tied converters due to its lower conduction losses in dc-side filtering and semiconductors. Note that the inductor in the link between the BDAC and BDC converter in figure 2.9b makes the nature of the CSI.



(a) VSC.

(b) CSC.

(c) 3-level NPC.

Figure 2.9: Converter topologies where a line-frequency transformer is required.

However, there are some obvious disadvantages with the inclusion of a grid-side transformer. First of all, depending on the power and voltage rating of the grid, there are concerns connected to space and cost. A $50Hz$ transformer is rather bulky, and with higher power rating, the larger and more expensive transformer is needed. Secondly, there are increased power loss entailment linked to the inclusion of a transformer. Other semiconductor arrangements that requires a transformer includes the 3-level Neutral-Point Clamped (NPC) converter. This converter has a multi-level nature in which an anti-parallel diode clamp is used between the semiconductors [87]. A three-phase NPC converter is shown in figure 2.9c. This topology is suggested amongst others as a suitable power stage for BESS [106]. A NPC converter has been validated for PV-cell application in [40] with promising results. However, most such converters requires a grid-side transformer in order to connect the dc side to the grid.

There are several ways to disregard the grid-side transformer. One way is by connecting several battery packs in series or parallel across the dc-link, as shown in figure 2.9c. As batteries are connected in series, the voltage levels rises. The immediate drawbacks to this is the required amount of series connected batteries. Using this arrangement leads to difficulties in monitoring each individual battery. Furthermore, it ceases the possibility of performing individual battery power and SOC control. A better way to neglect the transformer is by series connection of semiconductor devices. One such arrangement is

shown in figure 2.10, using two voltage levels. The main advantage of this arrangement is that the combination of semiconductors leads to a higher capability in blocking the required dc-link voltage compared to one single semiconductor [45].

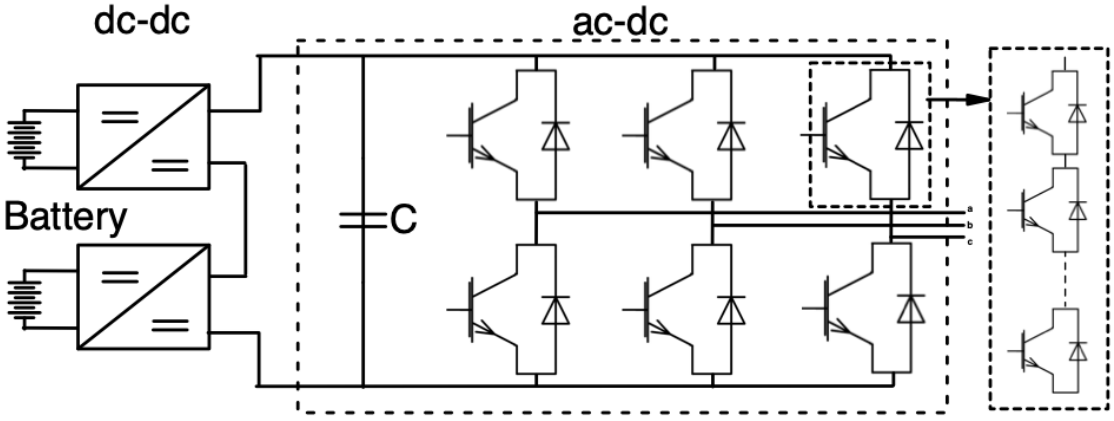


Figure 2.10: Series connection of semiconductors in a three-phase ac-dc converter with dc-dc stage.

Seeing as the general principle behind this topology is convincing, a modification to this arrangement has been proposed in the literature of multilevel converters. The idea is to place battery packs and converter bridges in series connected sub-modules, as shown in figure 2.11. A single sub-module (cell) consists of minimum one distributed battery across the dc-link and either a half-bridge or full bridge (H-bridge) 1-phase converter [35]. The resultant multilevel converters are namely Cascaded H-Bridge (CHB) and Modular Multilevel Converters (MMC). Figure 2.11 shows a CHB converter and battery distributed into submodules. The number of modules in a phase, n_m is related to the voltage level classification n_l of the converter by:

$$n_l = 2n_m \tag{2.1}$$

CHB and MMC differ mainly by the applied bridge structure and neutral connection. CHB as the name implies, consists of full (H) bridges in cascade. The neutral point is usually star-connected (Y), although it may be delta-coupled (Δ). The MMC shown in figure 2.12 consists, on the other hand, of six arms with twice the number of modules. However, using half-bridge converters with two semiconductors leads to an equal number of semiconductors between the two. Designing the output filter for both topologies varies slightly, but the nature of both constellations leads to the same filters, and thus the same total stored energy. The MMC shown in figure requires a higher value of the dc-link capacitance than the CHB [45]. Having twice the number of modules makes this a considerable drawback for the MMC. The reason is due to the six-arm structure,

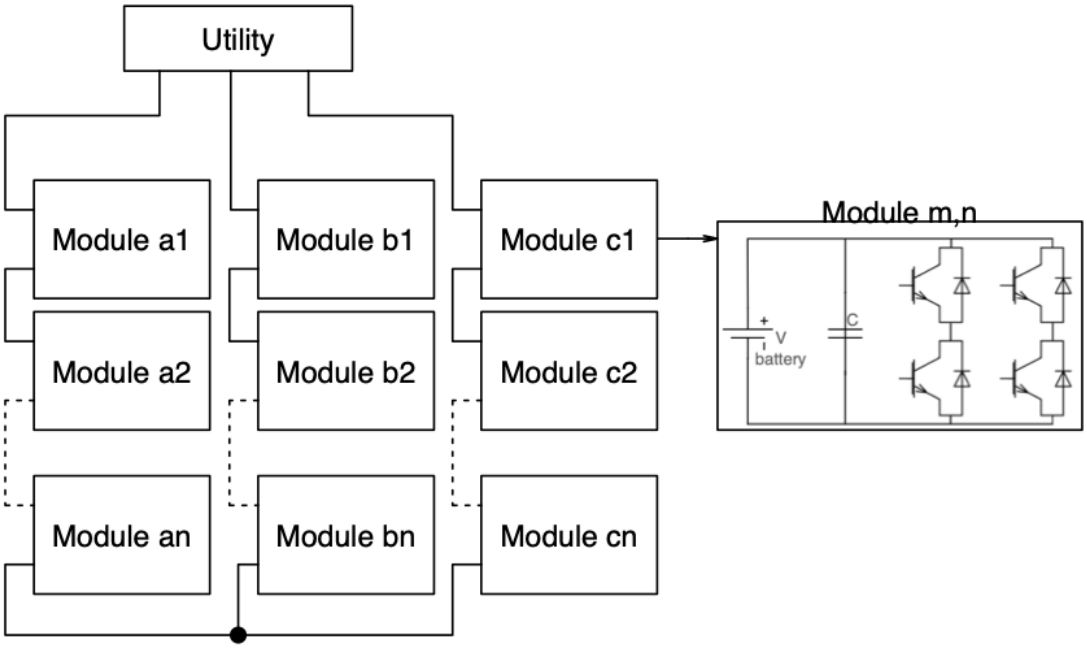
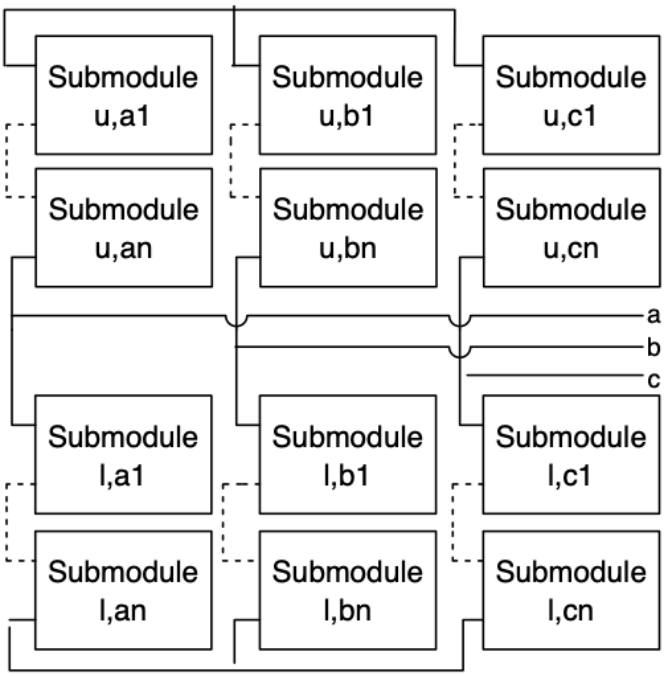


Figure 2.11: H-bridge modules connected in Y-cascade (CHB).

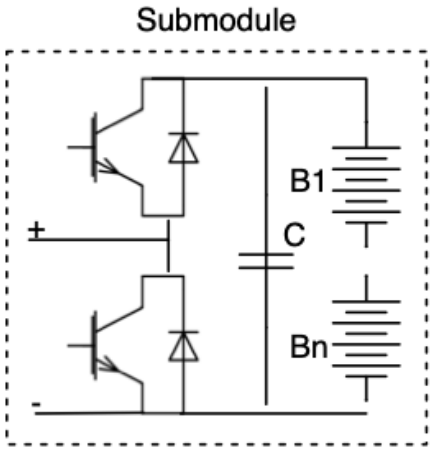
where larger voltage fluctuations occur. Even though [30] has found MMC to be slightly more advantageous over CHB, [35] has concluded that the overall system performance and efficiency favours the CHB converter for BESS applications.

A utility scale BESS may consist of hundreds of battery modules [45]. Having batteries distributed in sub-modules facilitates the possibility of individual cell control over desired controllable parameters such as power system variables or battery variables. Moreover, battery packs are distributed in modules, the resulting number of dc-links and filter capacitors increases proportionally with the number of modules. These however, may be significantly reduced in size across the modules. Additionally, the output filters (details in section 3.1.2) are noteworthy reduced in size and cost. This is shown in figure 2.13 for both CHB and MMC. There has been conducted comparison studies between the different multilevel converters used for BESS applications, such as in [35, 30, 13, 45]. Here it is concluded that CHB and MMC are the two most prominent variants of current converter topologies.

Figure 2.13 shows an overview over both efficiency and cost of the four reviewed topologies in this thesis. Here, (2L+Tx) represents a 2-level converter with grid-connected transformer. The authors of this research have experimentally shown that the MMC is marginally more effective for higher rated power applications. Furthermore, regardless of power rating, it reaches somewhat lower levels of power dissipation in the overall



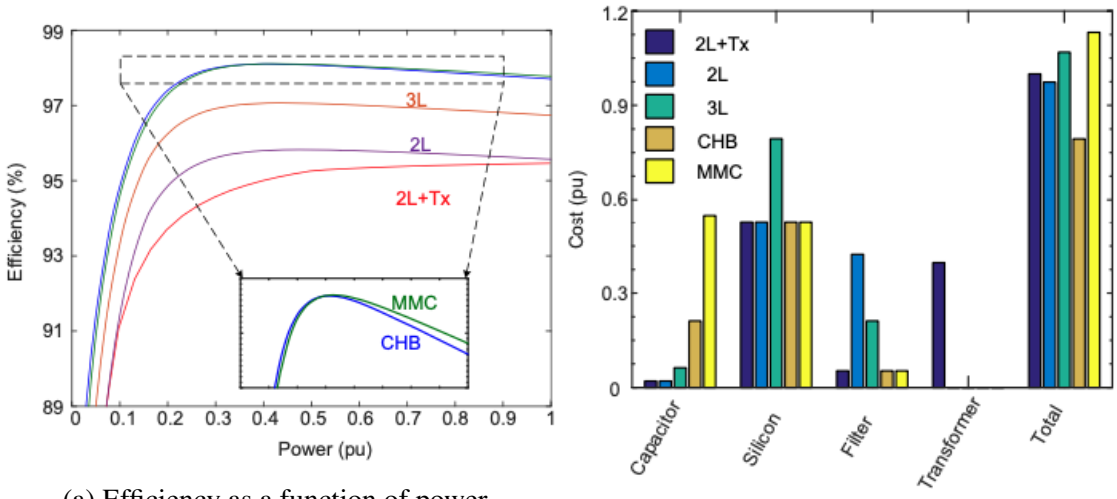
(a) Submodule arrangement



(b) Module using half-bridge converter

Figure 2.12: Modular multilevel converters (MMC) Y-connection. "u" stands for upper, while "l" is lower.

converter during high load conditions. The CHB on the other hand is far better during low consumer demand. Typically for PLS installations, the discharged power will fluctuate between low levels to rated. Taking all of this into consideration, the CHB converter is chosen for this thesis.



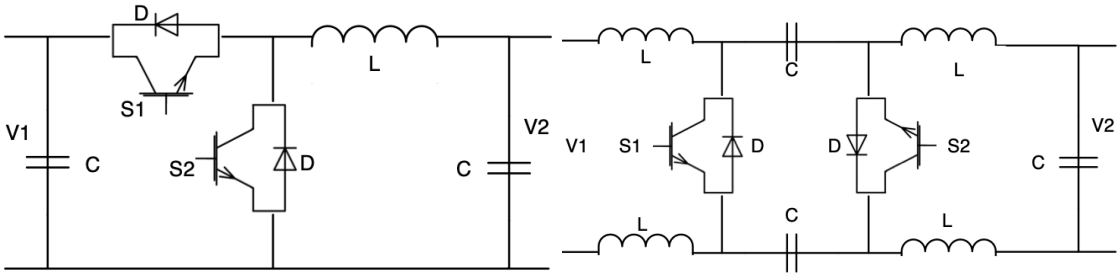
(a) Efficiency as a function of power.

(b) Cost organized by component.

Figure 2.13: Comparison between the four considered converter topologies. Adapted from [45].

2.3.2 BDC converter topology

The need of a dc-dc stage in grid-connected battery applications is discussed in several studies. Experiments have been conducted both with and without the use of dc-dc stage in BESS. Engineers in Japan have suggested CHB converters for BESS applications without a controllable dc-link [17, 6]. This means that the dc link terminal voltage is directly proportional to the battery voltage. Seeing as the internal voltage in the case of a Li-ion battery is a function of the stored charge, it varies in a range between $V_{bat}|_{\%SOC,min} < V_{bat,actual} < V_{bat}|_{\%SOC,max}$. By means of containing dc-link voltage to acceptable values, a voltage control strategy applied upon the modulation signal is employed. Using this topology and control strategy, the number of semiconductors and filtering components are dramatically reduced for CHB converters. However, this means that the range of the modulation index increases as well. As a consequence, there may be higher ac harmonic injections and a decreased converter efficiency [45]. Besides, an uncontrolled dc link means that the semiconductors suffers from over-sizing in terms of dealing with high voltage levels during high SOC. By introducing a dc-dc converter as an interface between the battery and the BDAC converter, may overcome these disadvantages. This stage is crucial to include in some applications. When the degrees of freedom in voltage levels provided by the CHB converter is insufficient, or when the battery voltage levels excessively differs with respect to the grid, this stage should be included. This typically applies for PV-cell applications in order to deal with PV panel leakage currents [23].



(a) Conventional buck-boost converter.

(b) *CÚK* converter.

Figure 2.14: Reviewed bidirectional dc-dc converter topologies.

Figure 2.14 shows two of the investigated BDC topologies. The conventional buck-boost converters in figure 2.14a using two semiconductors in anti-parallel is simple in structure with a moderate efficiency. Although it can be used in conjunction with GI, it is rarely seen in literature for BESS applications. It is therefore excluded in further discussions. Improvements to this topology, including hybrid installments on the other hand are becoming increasingly more interesting. *CÚK* converters and interleaved converters with advantages involving current splitting, cancellation of rippling effects, high power density and overall system efficiency is mentioned in the literature [60].

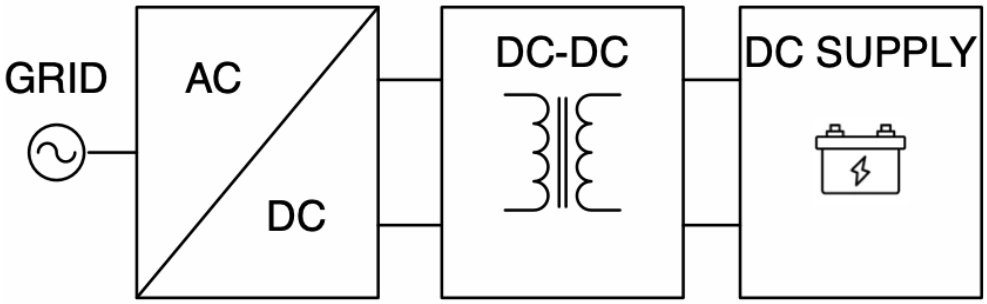


Figure 2.15: Two dc-dc converters separated by a HF transformer.

Another practical feature accompanying the dc-dc stage is the possibility of including Galvanic Isolation (GI), as illustrated in figure 2.15. Here, a dual-bridge topology can be utilized as a dc-dc converter with a High Frequency (HF) transformer separating them. In these topologies, both terminal voltages are almost pure dc-components, while high frequency ac is converted between the two bridges. In doing so, one achieves control over power system variables, such as currents or voltages. Additionally, increasing the frequency of the ac across the isolation transformer leads to a reduction in cost and size of the transformer [2]. Using such a topology into the power electronic structure thereby

reaches the same advantages provided by a grid-side $50Hz$ transformer, while also benefiting the resultant cost, size, efficiency and ease of control [45]. On the other side, a thorough classification over non-isolated dc-dc converters has been conducted in [44]. These converters are attractive in stand-alone applications where size, weight and cost are of utmost importance such as in airplanes or spacecrafts. In grid-tied applications however, loads and grid-tied equipment may be subjected to power surges. Besides, depending on application there are also legislature standards regarding the need of electric isolation (GI). A HF transformer is therefore included in this analysis. [60] suggests that isolated dual half- and full bridge converters are the most suitable for battery applications. Experiments conducted in [4, 21] agrees that the bidirectional H-bridge is the preferred converter. It consists of two legs and four semiconductors and is shown in figure 2.16. Due to this, it is the converter topology chosen in this analysis.

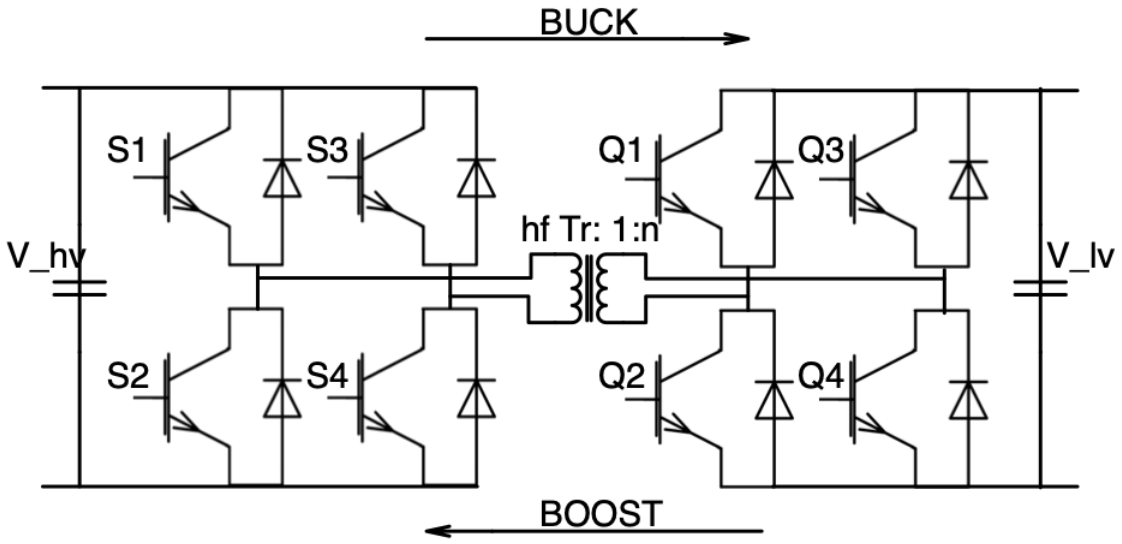


Figure 2.16: Isolated bidirectional H-bridge converter.

The number of modules n_m in cascade are dependant on both maximum arm voltage and module voltage [35]. Therefore, n_m should be selected based on grid parameters. When grid-tied converters is interfaced between an external power source and a high voltage network, it is desirable to increase the voltage in the converter without the use of a bulky line-frequency transformer. For a physical implementation of a battery bank in the distribution grid, the voltage output of the power converter is therefore converted in the range of tens of kV. In this case, the minimum number of modules can be calculated

as [35]:

$$n_{m,min}^{SSBC} = \frac{\sqrt{\frac{2}{2}}V_g \cdot 1.15}{v_{crit}} \tag{2.2}$$

In equation 2.2, n refers to single-star bridge-cell (SSBC), although similar formulas can be applied for SDBC and DSCC [35]. v_{crit} represents the maximum rated semiconductor voltage. However, the focus in this report remains to theoretically investigate a multiple module case using SSBC with an associated control system. This has lead to selecting $n_m = 3$. Here, the general assessment is that $n_m = 2$ comes short of emphasizing the nature of the cascaded structure, while $n_m = 4$ is not necessary for this down-scaled system. As a result of this, the complete topology implemented in this project is shown in figure 2.17.

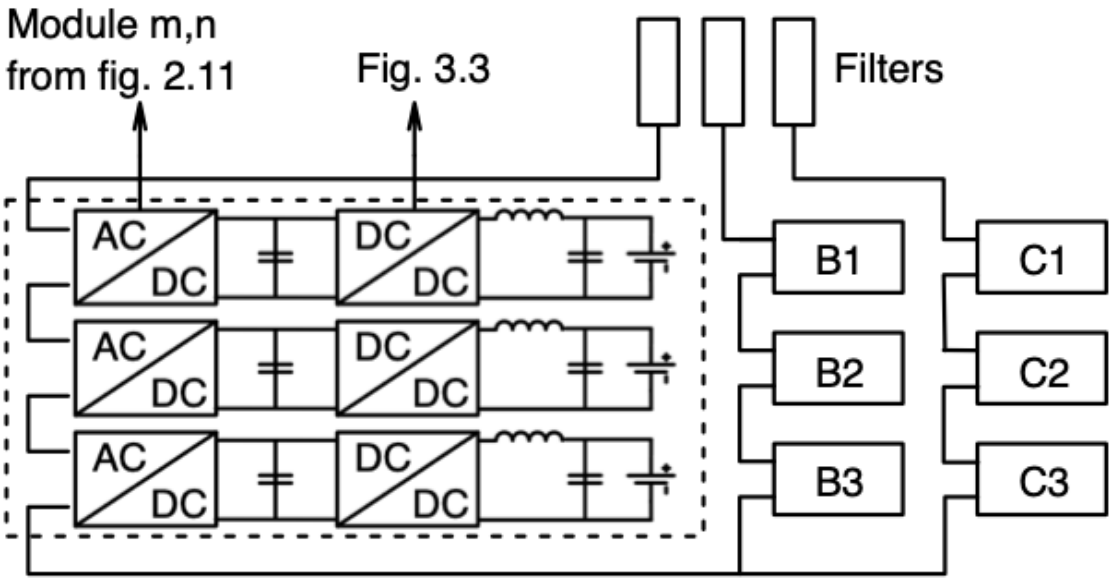


Figure 2.17: Complete overview of the chosen module topology.

2.3.3 Control strategies

The employed control strategy should be reflected by the main objective of the BESS. Direct frequency control can for instance provide fast responsive support to grid-connected RES towards imbalanced conditions or improving the transient stability. Providing direct frequency control to the utility using batteries is shown to have a high value, though it cuts back certain degrees of flexibility [32]. Furthermore, in grids frequently affected

by voltage sags, voltage drops or distortions, a dynamic voltage restorer might be implemented in the control system for BESS, such as in [7]. Voltage droop control may also be implemented to improve the sudden change in voltage sags due to heavy load connections, such as in [31]. PLS-directed applications on the other side, is providing indirect frequency control through the means of supplying the grid power demand. Load measurements can be conducted at consumers using Advanced Measurement Systems (AMS), and fed back to BESS station Remote Terminal Unit (RTU). Here, desired power commands through current or voltage control can achieve great results in terms of PLS control strategy. The recognized variable reference frame is by transforming measured values into $dq0$-frame using Parks [64]. Current and voltage variables are therefore transformed using Parks for ease of control. A common control strategy for active and reactive power control of grid-tied BESS, has been by using decoupled current control [6, 25]. Here, the active and reactive power is fully decoupled, depending on the output filter. Using a single inductance, L_f, the grid voltages are used in proper feed-forward in order to decouple the two terms [88]. LCL-filter possess a resonant characteristic, different to the L-filter. This is discussed in detail in section 3.1.2. Some researchers have designed a Reduced Order Generalized Integrator (ROGI) based decoupled current controller in $\alpha\beta 0$-frame. Such non-$dq0$ method can reach zero steady state error in the tracking of ac-reference signal, resulting in less computational burden [71]. However, it can make matter worse in terms of the current loop capability regarding transient response. In this project, $dq0$-based decoupled current control shown in figure 2.18 has been employed for dual power control.

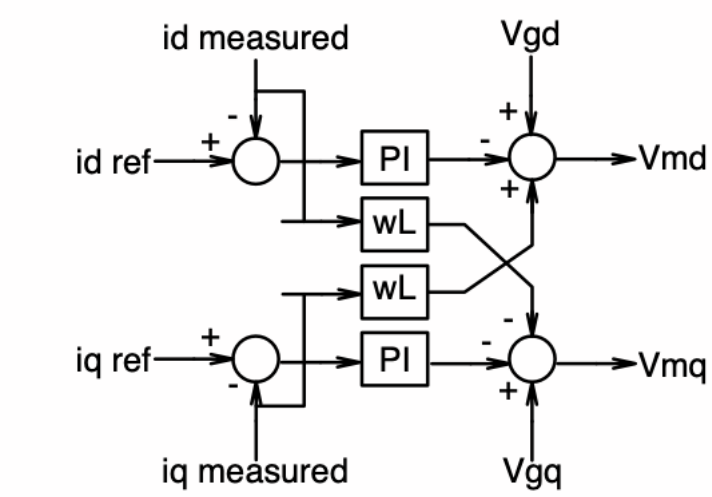


Figure 2.18: Decoupled current control with voltage feed-forward terms.

The dq-components of the current supplied to the active and reactive power control sys-

tem in figure 2.18 can be generated in several ways. Two recognized strategies has been evaluated for this project. [6, 4] have proposed a $i_d^* i_q^*$ generation directly from the desired power commands, while a voltage controller has been implemented in [25, 26, 10, 73]. As explained in section 2.1, the charging operation of a battery should depend on its CC-region to maximize battery cycles and life. A control system should take this into consideration. To achieve this, it is proposed a hybrid between the two i_{dq}- generation methods, in which facilitates the possibility of CC charging. A detailed review of this control strategy follows in section 3.2.

Using multilevel converters requires additional control system, in which adds to the work load complexity and computational needs of the power processors. In MMCs, there are circulating currents which needs to be accounted for [15]. CHB converters have no such needs, but does however, require capacitor voltage balancing for each module individually. Additional balancing controls, such as SOC or individual power control performed on every module can be added. Regardless, SOC-control should be added through the BMS in order to monitor battery conditions. Moreover, SOC-control may secure a balanced SOC between the batteries, all in which increases security and reliability. There are many conventional SOC-control algorithms for CHB proposed in literature, where [68] has proposed a novel technique. Therefore, focusing on capacitor voltage balancing, and take SOC into account for charge and discharge logic should be sufficient for this system. An overview of the complete control strategy is presented in section 3.2.

The leading control strategy regarding switching action of the BDC converter is by employing Dual-Active Bridge (DAB)-control. Having duty on both bridges leads to a higher efficiency compared to a single-active bridge. However, seeing as DAB-converter design is too far from the main objective of this project, the BDC converter implemented are using single-active bridge commands. Furthermore, the BDC converter can be viewed as a single-phase, one-module converter so that it can be modelled and controlled regardless of the cascaded topology considerations.

3 Modelling and design

3.1 Component design

The design of a BESS requires harmony between the selection of nominal values, component sizing and arbitrarily established values. For theoretical investigation, as the one conducted in this project, both HF transformer and IGBTs are considered ideal. Furthermore, the rated battery capacity and grid parameters can be decided arbitrarily. For this model, $30Ah$ batteries are used, although a practical implementation depends on the system rated power and load situation. As will be shown in section 3.1.1, the ideal battery energy capacity is calculated in such an event. An overview of selected an calculated values are collected in table 3.1. These parameters however, should reflect authentic grid conditions so that the system designed provides a beneficial value to the research in this field. The designed system can be scaled after application requirements. Fixed values however, such as duty ratio and switching frequency of both BDAC and BDC converters can be permanently established. Concerning duty cycle, d, a detailed explanation will follow in section 3.4. As of here, the duty cycles for both buck and boost mode of operation in the BDC converter are chosen as $d|_{buck} = 0.45$ and $d|_{boost} = 0.55$ respectively.

Component	Value	Description
Nominal Power	$5kW$	P_N
Battery	$30Ah$	$Bat_{m,n}$
Battery rated current	$9.26A$	$I_{N,bat}$
Grid voltage	$230V$	$V_{g,RMS}$
DC link voltage charge	$153.33V$	V_{dc}
DC link voltage discharge	$108.42V$	V_{dc}
Output filter	$68.4mH$	L_f
Equivalent filter resistance	1.319Ω	R_f
DC capacitor	$0.111mF$	$C_1 = C_2$
DC inductor	$1.686mH$	L
PS-PWM carrier frequency	$5kHz$	$f_{s,BDAC}$
BDC switching frequency	$20kHz$	$f_{s,BDC}$
Duty ratio, buck	0.45	d_{buck}
Duty ratio, boost	0.55	d_{boost}
Nominal modulation index	0.854	M_N
Cascade number	3	n_m

Table 3.1: Summary of all selected and calculated model parameters.

In terms of switching frequency it is desirable to keep it high due to its effects on the resultant waveforms. Depending on application and semiconductor devices, f_s can be selected in the range $f_s < 1kHz$ to $f_s > 100kHz$ [56]. Choosing a high switching frequency on the semiconductor components leads to an attenuation in ripple effects, and thus improving the converter power factor and voltage quality. For this reason, a high valued f_s creates a domino effect upon the filter sizing. The filtering components may be reduced to improve the filter power dissipation and the overall system efficiency. However, selecting f_s too high, results in greater EMI and switching losses, seeing as these losses increase proportionally with f_s [2]. Moreover, [92] have studied the effects of different switching frequencies and its affection on the harmonic distortion and the converter efficiency for a 5-level CHB using PS-PWM. The result shows that the Total Harmonic Distortion (THD) and efficiency are reduced as f_s increases. Hence, there must be a trade-off when selecting f_s. More importantly, f_s depends on the selection of semiconductor device. Using IGBT, f_s may be significantly larger than that of Bipolar Junction Transistors (BJT), power thyristors or Gate Turn-off Thyristors (GTO) due to the low on-state losses. Even though it has lower on-state losses than a Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)-device, the general nature of the IGBT makes it slower so that f_s should be kept moderately high [2].

Finally, selecting f_s is depending on the employed modulation technique. As for the BDAC converter, PS-PWM has a unique characteristic regarding switching frequency and the first harmonic component f_{h1}. The output voltage harmonic move towards higher frequencies in the harmonic spectrum, where the first f_{h1} is given by [54]:

$$f_{h1} = f_s(n_l - 1) \tag{3.1}$$

Here, n_l represents the number of voltage levels in the converter. This effectively make the resultant switching frequency to appear $n_l - 1$ times larger than the actual carrier frequency. This way, f_s can be selected at a relatively low value while reaching lower levels of EMI, power dissipation and harmonic distortion while keeping the overall efficiency high. Taking this into consideration, f_s is chosen to be $5kHz$. This forces the effective f_s and equation 3.1 equal $f_{s,eff} = f_{h1} = 30kHz$, 600 times larger than the fundamental frequency. As for the BDC converter using conventional PWM technique, it is chosen to be $20kHz$. The corresponding GI frequency is chosen equal the BDC switching frequency.

3.1.1 Battery parameters

Power ratings below 5 kW will usually represent a down-scaled system for laboratory purposes only. Although [17] have conducting testing on 10 kW installations, the general consensus is to minimize malfunction consequences during the initial testing phase.

In the event of future testing of the proposed system, the rating should be kept within these limits in order to avoid down-scaling requirements for laboratory action. For that reason, the power rating is selected to be 5 kW, which also should be able to demonstrate the designed system capabilities towards PLS and SH.

The grid voltage V_g is taken equivalent as a wall outlet. That is, $V_g|_{rms} = 230V$ or $V_g|_{ptp} = 230\sqrt{3}V$. As for the battery, it is isolated from the dc-link through the BDC converter as described in section 2.3.2. In order to design a flexible system in which is independent on both grid voltage and battery voltage, the nominal voltage of the battery is selected to differ from the dc-link voltage. Then the BDC converter requires separate modelling and control for both charging and discharging operation. Even though it increases work load and control system complexity, the system reaches the benchmark of being more easily adaptable for different applications. The nominal battery voltage is therefore set to be $60V$, making the BDC converter to operate in buck mode during charging duty. The voltage differs according to SOC-levels, as described in section 2.1.

Having settled the battery voltage rating, the next two parameters of interest is the energy capacity and C-rate, as described in section 2.1. In general, the energy capacity can be determined from the system power and voltage rating. Additionally, SOC limitations mentioned in section 2.1 means reduced availability of the total battery capacity. Having the margins between $35\% - 80\%$ active duty leaves the DOD to be $1-(0.8-0.35) = 0.55$. Then the stored electrical charge (energy capacity) Q_{bat} can be calculated as:

$$Q_{bat} = \frac{W_N}{V_{bat} \cdot DOD} \tag{3.2}$$

W_N is the nominal stored electrical power in Watt-hours. The load profile through 24 hours in Appendix B can be used to calculate the minimum required W_N through equation 3.3:

$$W_{N,min} = P_{load,h_1} + P_{load,h_2} + \cdots + P_{load,h_n} \tag{3.3}$$

Here, h represents the n'th hour. Considering the dynamics of the load, the condition is that equation 3.3 only summarizes adjacent loads of the same polarity. That is, if demand changes from positive to negative from one hour to the next, summation stops to optimize $W_{N,min}$ for PLS applications. The aim is to find the highest value of W_N in order to obtain $W_{N,min}$. From table B.1 in Appendix B, equation 3.3 results in just above $30kWh$. To accommodate for the possibilities for self healing grid during power outage, the power capacity should be in the region above $30kWh$ which represents a normal day. For instance, if the grid were to fall out during the entire day, the total power capacity should be $7.652kW \cdot 24h = 183.648kWh$. There would be no financial justification to

install a battery bank this many degrees above the rated power of $5kW$. Even more so, a power outage of this duration is rare in itself. According to Statnett and the Norweegian Water Resources and Energy Directorate (NVE), the average duration of power blackouts in the distribution and transmission grids are roughly the same across all networks, between 3 to 3.5 hours [69, 77]. Thus, inserting a power outage in 3.5 randomly selected hours, leads to a battery power capacity requirement of $7.652kW \cdot 3.5h = 26.782kWh$ if all the grid loads are to be supplied during the blackout. The outage brings variable disruption upon the battery SOC, depending on the time of impact. Furthermore, a thorough load demand investigation should be conducted in the area in which the battery bank is to be implemented in order to reduce uncertainties concerning demand varieties. Moving forward with this in mind, a battery bank power capacity of $40kWh$ is considered suitable for the loads presented in Appendix B. Distributed across nine batteries, the resulting individual battery power capacity is $W_{N,bat} = \frac{40kWh}{9} = 4.444kWh$. Placing W_{bat} into equation 3.2 leads to an ideal energy capacity of $123.46Ah$.

To estimate the C-rating during max/min operating conditions, the rated battery current $I_{N,bat}$ is needed. Having three batteries per phase, the rated current is given by:

$$I_{N,bat} = \frac{P_N}{3V_{N,bat}} = \frac{5kW}{9 \cdot 60V} = 9.26A \tag{3.4}$$

Then the C-rate is given by:

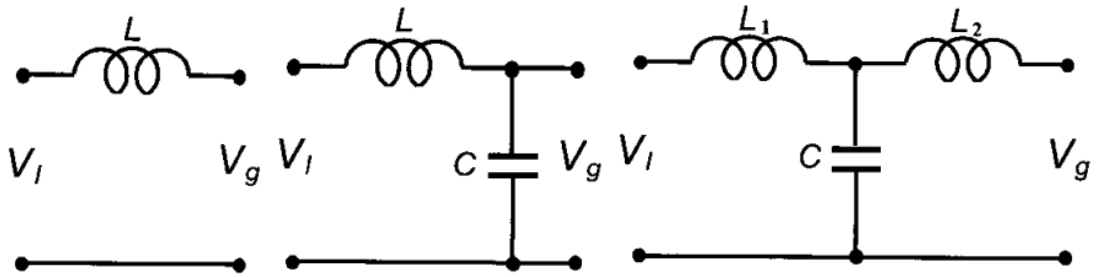
$$C = \frac{I_{N,bat}}{Q_{bat}} = \frac{9.26A}{123.46Ah} = \frac{1}{13.33} \tag{3.5}$$

3.1.2 Output filter

Power electronic equipment can be connected to the grid to serve as an interface between grid and load to prevent power line disturbance from disrupting the loads. However, due to the nature of PE, it can also inject harmonics into the grid and produce Electromagnetic Interference (EMI) when grid-tied. Designing proper filters at the converter output can serve to attenuate the EMI, harmonic current components, switching frequency effects and voltage distortions. Thus, the power factor and voltage quality improves [2]. Furthermore, the output filter impacts on the overall system bandwidth and time constants [3].

In general, there are three different passive filters used by grid-tied converters found in literature [82]. Figure 3.1 shows a one line diagram over filter type L, LC (low-pass) and LCL respectively. There are numerous effects of inserting a L-filter, some of which are mentioned in the section above. Adding a C, or CL element will only serve to moderately improve these effects, although a supplementary shunt capacitor will attenuate

peak-to-peak ripple effects in the output voltage waveform significantly [3]. Moreover, L-filter requires a higher switching frequency than LCL in order to sufficiently suppress the harmonics injected by the converter. The LCL-filter can to a greater extent reduce THD using lower switching frequencies. Due to resonance, the LCL-filter may on the other hand cause input current distortion [3]. Other noticeably drawbacks are concerning practical implementation of LC or LCL filters, such as sizing, losses and financial aspects [2]. Despite the improved effects of adding a shunt capacitive element, the filter chosen for this converter is the L-filter. The reason is threefolded: (1) modelling simplification, (2) maintaining focus on the main objective, that is peak load shaving through the means of CHB converter topology, and (3) research findings in which L-filters are utilized.



(a) L-filter. (b) LC-filter. (c) LCL-filter.

Figure 3.1: Output filter topology. Retrieved from [3].

As will be explained in detail in section 3.3 correct sizing of the output inductor L_f is of vital importance regarding the system dynamics and time constants. In order to estimate a satisfactory L_f, a detailed review of associated converter parameters are needed. The dc-link voltage is required to fulfill the condition in equation 3.6 [2]. Given that there are three modules containing a voltage source each, the second term is modified by a factor of one third.

$$V_{dc} > \hat{V}_g\sqrt{2} \rightarrow V_{dc} > \frac{2V_{rms}}{3} = \frac{2 \cdot 230V}{3} = 153.33V \tag{3.6}$$

However, this system is designed so that the primary voltage of the transformer equals $\hat{V}_g$ divided by the number of modules. In this case that results in $V_1 = 108.42V$. The reasoning behind this is based on employing self healing control, and the ease of using this configuration in order to sum the three phase shifted module voltages into the peak grid voltage $230\sqrt{2}$ when the utility is disconnected. Therefore, using this value for V_1 and setting $n_1 = 1$ leads to the secondary winding equal:

$$a = \frac{n_1}{n_2} \Rightarrow n_2 = \frac{V_2}{V_1 n_1} = \frac{60V}{108.42V} = 0.553 \tag{3.7}$$

This ratio is needed in order to accurately model the BDC converter. Continuing with the output filter, the output current $\hat{I}_{out}$ is needed. It can be calculated by:

$$\hat{I}_{out} = \frac{2P_N}{3\hat{V}_g} = \frac{2 \cdot 5kW}{3 \cdot 230 \cdot \sqrt{2}} = 10.25A \tag{3.8}$$

The relationship between the dc-link voltage and the peak grid voltage can be expressed through the modulation index, M used for PS-PWM. Here, the dc link voltage is set equal to equation 3.6 in order to satisfy the given condition. Then, introducing a term relating V_{dc} with M is given by [10]:

$$V_{g,an} = 3MV_{dc}sin(\omega t - \theta) \tag{3.9}$$

Ignoring the oscillating term and inserting peak grid value $\hat{V}_g$, equation 3.9 can be rearranged with respect to M, so that the minimum modulation index is given by:

$$M_{min} = \frac{\hat{V}_g}{3V_{dc}} = \frac{230V\sqrt{2}}{3 \cdot 153.33V} \approx \frac{1}{\sqrt{2}} \tag{3.10}$$

It can be seen from equation 3.10 that M is well within the linear margins of $0 < M < 1$. In order to calculate filter dimensions, the nominal modulation ratio must be calculated. Ranging between $0.707 < M_{nom} < 1$, results in $M_{nom} = 0.854$. Finally, the filter inductance is given by [10]:

$$L_f = \frac{\sqrt{(3M_{nom}V_{dc})^2 - (\hat{V}_g)^2}}{\omega\hat{I}_g} = \frac{\sqrt{(3 \cdot 0.854 \cdot 153.33V)^2 - (230\sqrt{2})^2}}{2\pi \cdot 50Hz \cdot 10.25A} = 68.4mH \tag{3.11}$$

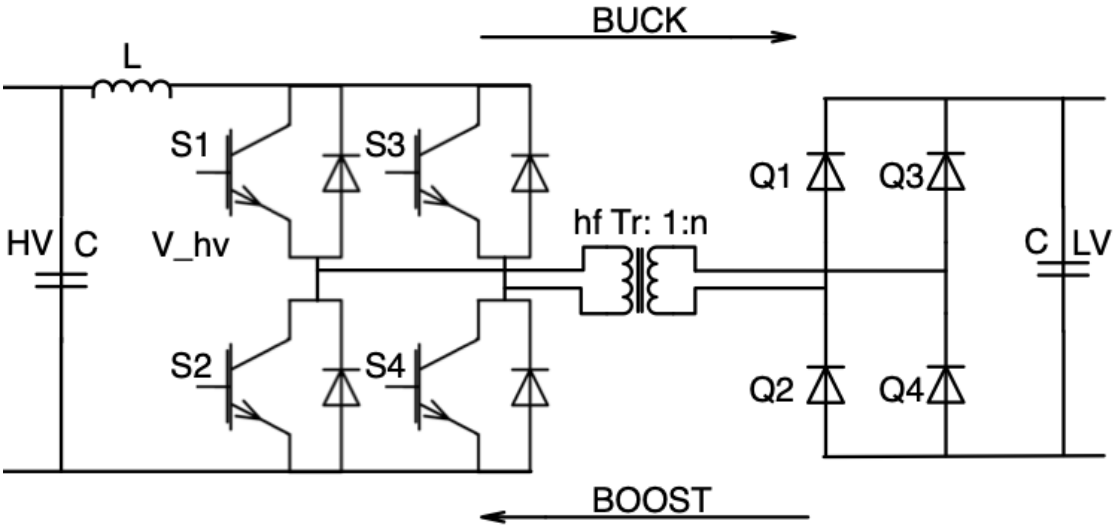
Equivalent filter resistance is given by:

$$X_L = \omega L_f = 2\pi \cdot 50Hz \cdot 68.4mH = 21.49\Omega \tag{3.12}$$

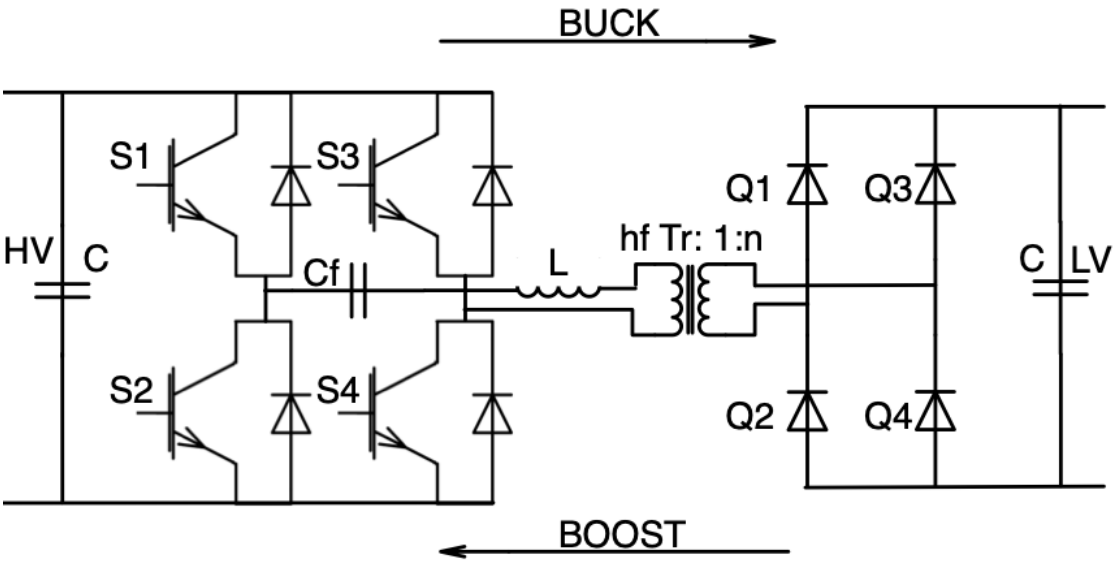
3.1.3 Dc side filter

As explained in section 2.3.2, a dual H-bridge dc-dc converter with isolation is suitable for BESS applications. Regarding the filtering of current and voltage ripple effects within the converter, there are many possible arrangements available. Primarily, filters between single and dual active bridges may be distributed in a similar manner. The simplest filters for both PSFB and DAB includes one dc link inductor and one capacitor at each side of the converter terminals, as shown in figure 3.2a. On top of that, Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS) filters may be added to reach soft switchings, which is shown in figure 3.2b [2]. Having excluded DAB from the discussion in section 2.3.3, figure 3.2 shows two different filter arrangements for

single-active bridge. Switches $Q1 - Q4$ are represented by the IGBT snubber diodes to illustrate the single bridge operation.



(a) PSFB.



(b) Filters enabling ZVS or ZCS.

Figure 3.2: Filter topologies for isolated BDC converter.

The semiconductor devices are expected to transfer the entire current magnitude from the battery to the grid-side load. During the switching operation, the semiconductors are

subjected to high levels of stress in which leads to a high switching power loss. High current transfer leads to higher variations in current and voltage ripples, so that the EMI produced increases [2]. These effects may be suppressed using the filter topology of figure 3.2b in conjunction with modified switching strategies. ZVS or ZCS reaches the soft switching by the means of switching when the voltage across, or current through the semiconductor is zero. Although many filters may be added in order to achieve this to a various degree, it can be seen from figure 3.2b that ZVS or ZCS filters at least consists of a LC arrangement. The nature of LC-elements combined leads to its own resonant characteristics, which is the reason these filters comprises the separate classified converter class, namely resonant converters [2]. Seeing as the work regarding modelling and control of this types of filter falls out of the scope of this analysis, the dc-dc converter is theoretically modelled and controlled by the utilization of the dc-link inductor L_b from figure 3.2a.

The conventional use of the inductance filter is by placing it on the opposite side terminal with respect to the dc-source. Typically, this applies for PV-cell applications. However, when battery is the main dc-source, it is preferred to have the battery connected to the inductance filter side terminals. This way, the waveforms of the dc current supplying the battery during charge mode are substantially improved. Thus, the safety regarding battery supply is increased while battery degradation decelerates [84]. The resulting topology is shown in figure 3.3

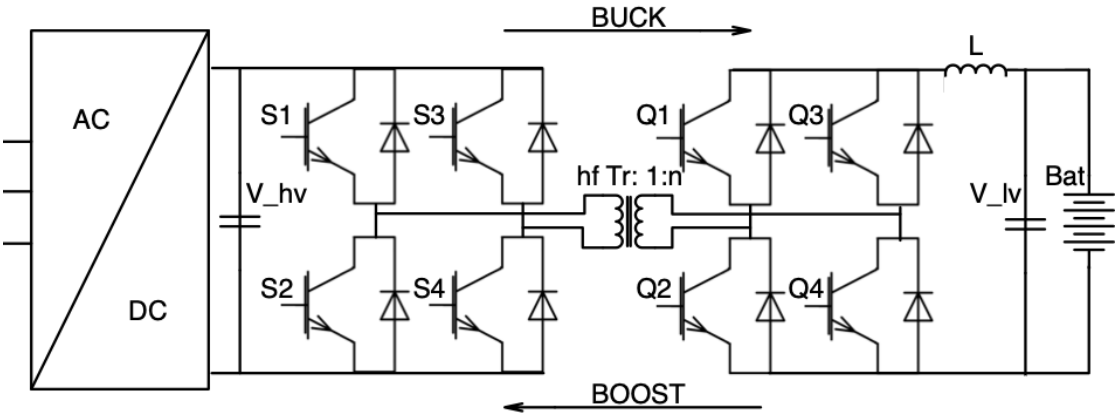


Figure 3.3: Final filter topology of the dc-stage.

The dc-link capacitor C_d serves as an interface between the ripple injected into the dc-link either from the BDC converter when discharging, or from the BDAC converter when charging [2]. It is desirable from a design point of view to keep the dc-link voltage ripple ΔV_{dc} below 1 % of the output voltage [85]. Using a small capacitor relative to

the system may result in too large voltage ripple across the dc-link. This leads to an increased transfer of harmonics to the grid side or the battery. The former represents poor power factor and power quality injection into the grid, while the latter decreases battery lifetime. An oversized capacitor on the other hand fails to be economical justified. Electrolytic capacitors (polarized) are becoming more popular due to its characteristics of effective Farads with respect to size [95]. For this reason, there is a trade off which leads to a reasonable capacitor sizing. The capacitance can be calculated from equation 3.13. Using results from calculations made in section 3.1 and 3.1.2, the capacitance is determined as [36]:

$$C_d = \frac{I_{out} d T_{sw}}{\Delta V_g} = \frac{10.25A \cdot 0.5 \cdot \frac{1}{20kHz}}{0.01 \cdot 230V} = 0.111mF \tag{3.13}$$

In equation 3.13, the ripple voltage ΔV_{dc} is taken to be 1 %. The battery side capacitor C_b serve the same purpose and should be in the region of C_d. As a result, C_b is taken to be equal C_d.

The battery side inductor functions to improve the current ripple ΔI_L. For acceptable ripple currents, ΔI_L should be kept below 20 % [85]. The importance of optimal sizing is vital for control system dynamics, system volume, inductor power loss and battery lifetime. Realizing that the inductor current I_L can be approximately equal to $I_{N,bat}$ from equation 3.4, the inductor value L_b is given by [75, 85, 36]:

$$L_b = \frac{V_{bat} d}{\Delta I_L f_s} = \frac{60V \cdot 0.5}{9.26A \cdot 0.1 \cdot 20kHz} = 1.686mH \tag{3.14}$$

ΔI_L is taken to be 10 % in equation 3.14. When modelling the BDAC converter, the dc side components can be neglected. However, seeing as current flows into the dc-side during charge, the dc-side can be described equivalently in order to design the ac-side controls. Figure 3.4 shows a Thevenin's equivalent of the dc side components in one module.

V_{th} is given by the dc link capacitor voltage during charge. Although this voltage has fluctuations both regarding voltage ripples and SOC, it has been approximated to equal the dc link voltage at $108.42\sqrt{2}$. The corresponding Norton current is found by approximating the dc link current to equal the dc equivalent of the peak grid currents given by:

$$I_N = \frac{I_m}{\sqrt{2}} = \frac{10.25A}{\sqrt{2}} = 7.25A \tag{3.15}$$

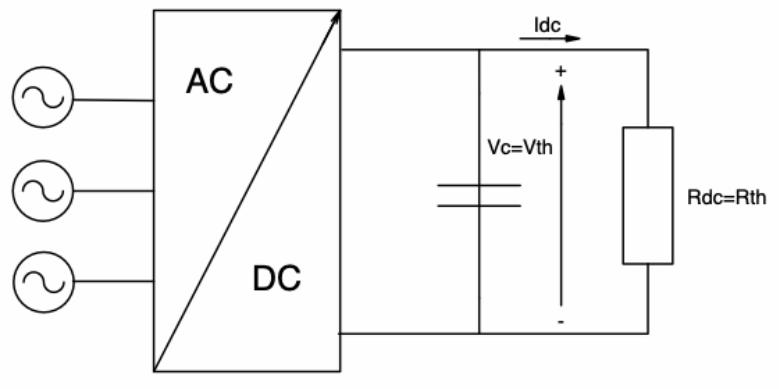


Figure 3.4: Thevenin's equivalent of dc side components.

Then the Thevenin equivalent dc side resistance R_{th} can be calculated as:

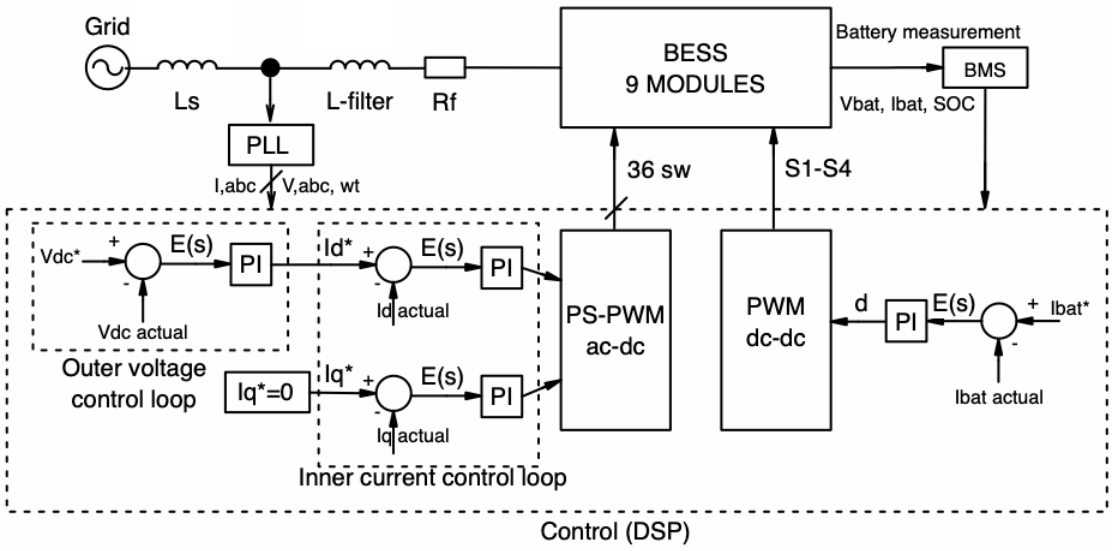
$$R_{th} = \frac{V_{th}}{I_N} = \frac{108.42V\sqrt{2}}{7.25A} = 21.15\Omega \tag{3.16}$$

During discharge, the equivalent resistance of the grid connected load is found using the rated power of the BESS, given by:

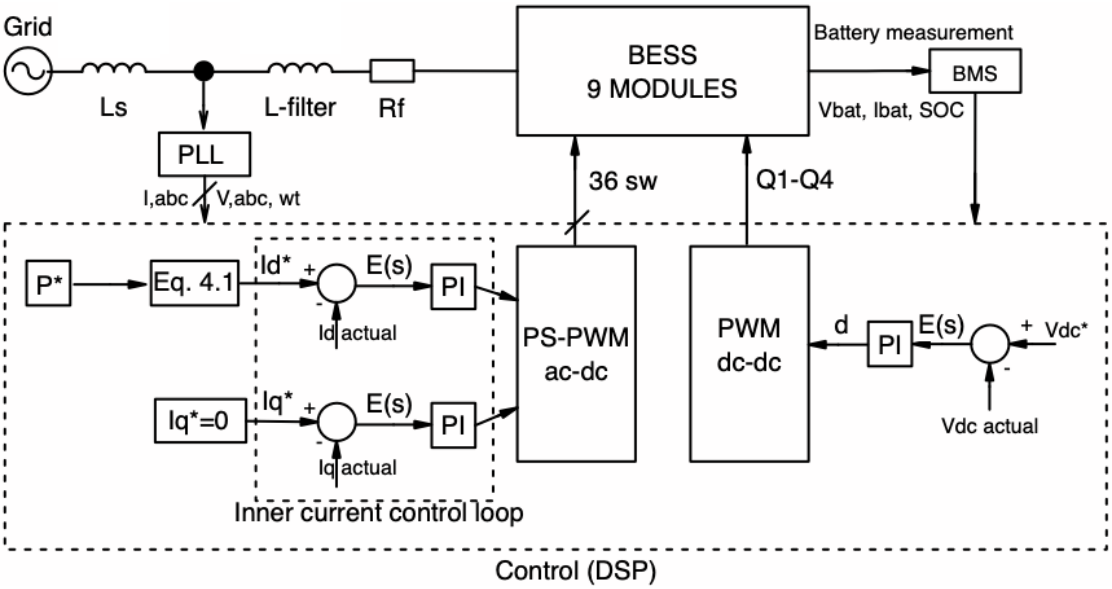
$$R_{dis} = \frac{V_g^2}{P_N} = \frac{230^2}{5kW} = 10.58\Omega \tag{3.17}$$

3.2 System overview

The control strategy is based on a mathematical modelling of the physical coupling of the system components. The model objective is to produce a transfer function describing the physical system, regulated by a PI-controller. The controller tuning is accomplished by the system transfer function representation. It is possible to make a model description of both converters separately by neglecting the influence from the other. The reason is largely due to the high efficiency of the semiconductors and the relatively low switching frequency. In addition, separating the ac and the dc side in the system modelling results in individual converter control.



(a) Buck mode.



(b) Boost mode.

Figure 3.5: One line diagram of simplified control system.

Figure 3.5 shows the resulting control strategy of the converters using variables from the mathematical modelling. Control parameters is converted from *abc*, Rotating Reference Frame (RRF) into Synchronous Reference Frame, $dq0$ in order to ease control and design the PI-regulators [18, 1]. Although there are many system representation methods available, this system is modelled using state space modelling for the BDAC converter, and state space averaging using small signal analysis for BDC converter and

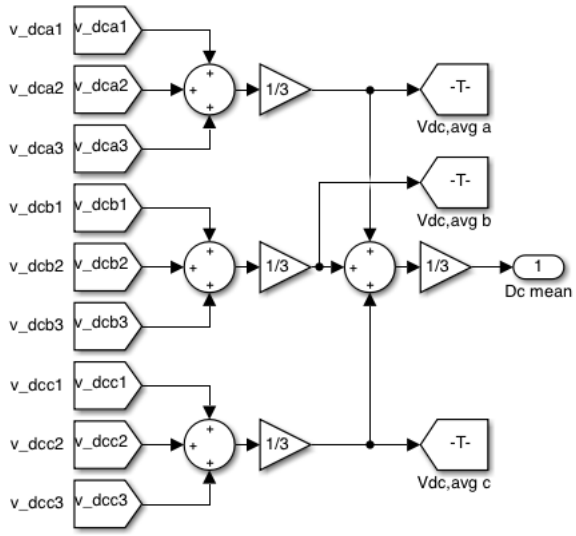


Figure 3.6: Averaging of the measured dc link voltages.

module voltage balancing loop. The target is to achieve CC control for battery charging in addition to dc link voltage control for both direction. As a consequence, the general control overview in figure 3.5 differs slightly depending on the power flow direction. In order to accomplish this, the control strategy is separated into two modes. Consequently, the converters operates differently for charging and discharging operation. Figure 3.5a shows the general control structure for charge, while figure 3.5b overviews the discharge controls. Figure 3.7 shows a detailed control structure. Note that since the BESS consists of nine modules, the actual values are generated by averaging the measured values across the nine modules. Figure 3.6 shows the averaging of the voltage V_{dc}, although the same procedure is performed on both I_{bat} and $SOC_{\%}$.

During charging, the BDC converter regulates the desired battery current, I^*_{bat}. This will accomplish control over the charging current in which realizes CC charging mode. A dc link voltage regulator has been added to the BDAC converter in order to reach dc link voltage control. This controller is designed and described in detail in section 3.3.2. During power supply mode, the voltage controller is disconnected. The dc-link voltage is controlled by the BDC converter. The desired current input to the power control of the BDAC converter is calculated based on the desired amount of active power P. Design details are provided in the forthcoming sections.

3.3 BDAC converter

The objective of the BDAC control system is to achieve desired levels of active and reactive power flow between the battery and the grid. The control structure consists of

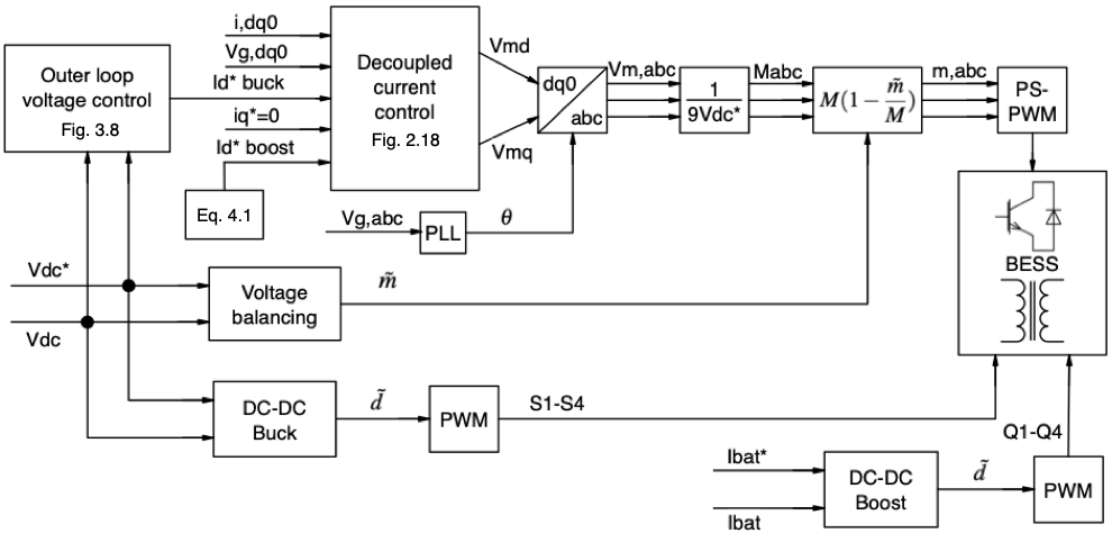


Figure 3.7: Detailed control structure.

an inner current control loop and an outer voltage control loop, as seen from figure 3.8. The main task of the outer voltage loop is to generate a reference for the active power which is fed to the input of the inner loop current controller. The method in doing that, is by keeping all the module dc-link voltages at a desired reference value, serving as the voltage controller input. The outer loop feedback signal is measured by averaging all nine dc-link voltages across the dc-link capacitors and sent back to compare with the desired dc-link values. Averaging the dc-link voltages ensures that the active power reference is correct with respect to the desired value. However, it does not consider unbalanced voltage conditions for each module individually. A voltage balancing controller is designed in section 3.3.3 to address this issue. Voltage controller is modelled and designed in section 3.3.2.

The current controller regulates power flow into or from the grid by controlling the phase voltages, $V_{m,abc}$, across the modules $m_{a1,a2\cdots c3}$. Here, the current controller output is converted from controlled SRF into rotational values, *abc*, and transferred into control voltage used as semiconductor switching signals in PS-PWM. A detailed design procedure is presented in section 3.3.1.

The active and reactive power output of the converter can be controlled through current and voltage control loops shown in figure 3.8. The desired power is generated through various modes, depending on charging, discharging PLS-mode or SH-mode, as presented later in this chapter. These systems is transferring the desired power commands to the system controllers. The power output of the converter in $dq0$-reference frame is given in terms of output phase module voltage $V_{m,dq}$ and output phase module current

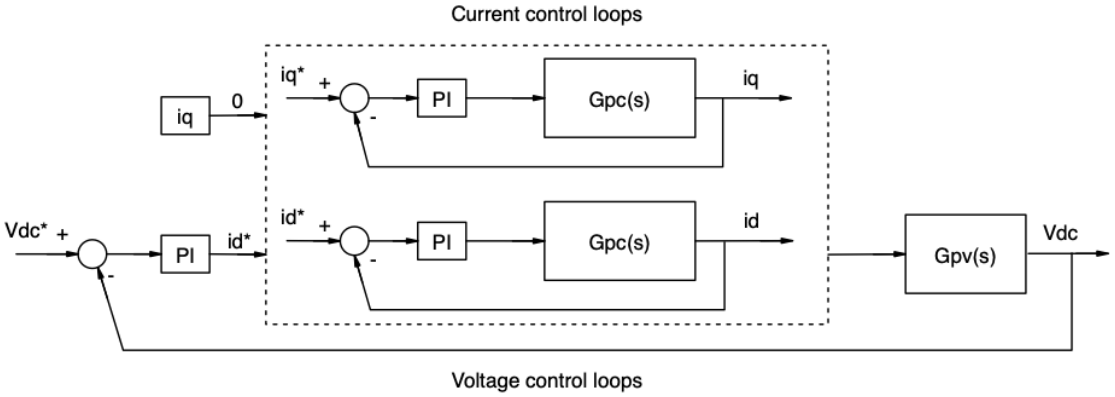


Figure 3.8: Outer and inner control loops.

I_{dq} as [100]:

$$\begin{pmatrix} P_g \\ Q_g \end{pmatrix} = \frac{3}{2} \begin{pmatrix} V_{md} & V_{mq} \\ V_{mq} & -V_{md} \end{pmatrix} \begin{pmatrix} I_d \\ I_q \end{pmatrix} + I_0 \begin{pmatrix} 2 \cdot V_{m0} \\ 0 \end{pmatrix} \tag{3.18}$$

Seeing as the voltage across the modules, V_{md} and V_{mq}, strictly is dictated by the grid voltage, the aim is to control the magnitude and direction of the converter current. Solving equation 3.18 with respect to the current and replacing actual values by desired values for power and current leads to:

$$\begin{pmatrix} I_d^* \\ I_q^* \end{pmatrix} = \frac{2}{3} \begin{pmatrix} P^* \\ Q^* \end{pmatrix} \begin{pmatrix} V_{md} & V_{mq} \\ V_{mq} & -V_{md} \end{pmatrix}^{-1} - I_0 \begin{pmatrix} 2 \cdot V_{m0} \\ 0 \end{pmatrix} \tag{3.19}$$

For balanced conditions, the zero sequence components is equal to zero. The terms involving V_{mq} becomes zero because the SRF used by the controllers are obtained when the grid voltage vector, $\vec{V}_g$, is aligned with the d-axis [15]. Equation 3.19 is therefore rewritten for balanced conditions as:

$$\begin{pmatrix} i_d^* \\ i_q^* \end{pmatrix} = v_{md}^{-1} \begin{pmatrix} P^* \\ Q^* \end{pmatrix} \tag{3.20}$$

Given that there is no desire to deliver or draw reactive power from the grid, the reference current for the q-axis, i_q^* should remain at zero in order to maintain a unity power factor $\cos\phi = 1$[6].

3.3.1 Modelling of current control loops

The BDAC converter structure consists of four main elements, namely the grid, output filter, semiconductors, and batteries. A common strategy regarding converter modelling, is to neglect RC-elements in the semiconductor devices, such as switching losses and

parasitic capacitance. That is, threat them as ideal. Power loss in the semiconductors is relatively small compared to the load and filter impedance. Further simplifications are made by separating the ac and dc side components, leaving the dc-side to be modelled for the voltage control loop in section 3.3.2. Utilizing per phase analysis and the simplifications above leads to the system shown in figure 3.9).

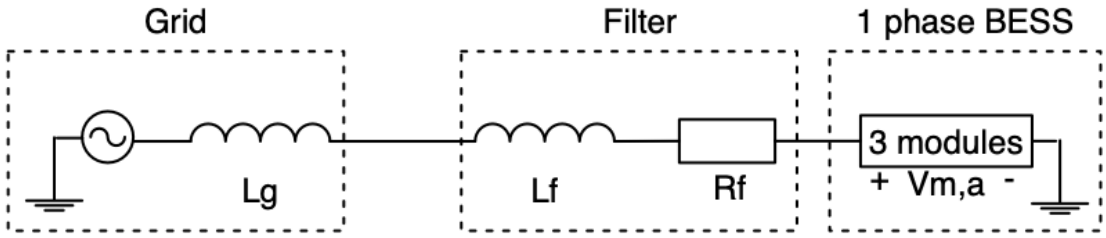


Figure 3.9: Simplified physical system from converter output, through L-filter to grid.

The aim is to create a state space model of the system presented in figure 3.9. An expression for the sets of voltages can be determined using Kirchhoff's Voltage Law (KVL), so that:

$$L_s \frac{d(I_g)}{dt} = V_g - I_g R_f - V_m \tag{3.21}$$

Here, $L_s = L_g + L_f$ where $L_g = 0$ in further discussion. This is a first order system, choosing I_g as state variable. In order to achieve independent control of active and reactive power, the state variable can be expanded into three phase currents, I_a, I_b and I_c. Furthermore, by expanding equation 3.21 into 3-phase, the parameters could be transformed into SRF in order to reach the output variables I_d and I_q from equation 3.20. Making equation 3.21 valid for three phases:

$$L_f \frac{d}{dt} \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} = \begin{pmatrix} V_{ga} - V_{ma} - R_f I_a \\ V_{gb} - V_{mb} - R_f I_b \\ V_{gc} - V_{mc} - R_f I_c \end{pmatrix} \tag{3.22}$$

The left hand side term of equation 3.22 is a table-transform from abc to $dq0$ which can be found in [98]. Therefore, performing Parks-transform leads to:

$$\begin{pmatrix} L_f \frac{d}{dt} & -\omega L_f \\ \omega L_f & L_f \frac{d}{dt} \end{pmatrix} \begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} V_{gd} - v_{md} - R_f i_d \\ V_{gq} - v_{mq} - R_f i_q \end{pmatrix} \tag{3.23}$$

Equation 3.23 is consistent with the literature of decoupled current control [6]. Solving

equation 3.23 with respect to state variables i_d and i_q leads to:

$$x'(t) = \frac{d}{dt}\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \frac{V_{gd} - v_{md} - R_f i_d + \omega L_f i_q}{L_f} \\ \frac{V_{gq} - v_{mq} - R_f i_q - \omega L_f i_q}{L_f} \end{pmatrix} \tag{3.24}$$

This is a state equation containing the state space model output expression, v_{md} and v_{mq}. The output is of no interest in a state equation, meaning that $v_{m-d,q}$ must be substituted [46]. Using equation 3.23, $v_{m-d,q}$ can be expressed as:

$$\begin{pmatrix} v_{md} \\ v_{mq} \end{pmatrix} = \begin{pmatrix} V_{gd} - R_f i_d - L_f \frac{d(i_d)}{dt} + \omega L_f i_q \\ V_{gq} - R_f i_q - L_f \frac{d(i_q)}{dt} - \omega L_{id} \end{pmatrix} \tag{3.25}$$

In order to extract controllable signals, the real and imaginary parts must be separated [25]. This is done by collecting d-axis and q-axis terms affecting the state variable. Equation 3.25 can be rewritten as:

$$\begin{pmatrix} v_{md} \\ v_{mq} \end{pmatrix} = \begin{pmatrix} V_{gd} + \omega L_f i_q - u_1(t) \\ V_{gq} - \omega L_f i_d - u_2(t) \end{pmatrix} \tag{3.26}$$

where:

$$\begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix} = \begin{pmatrix} L_f \frac{d(i_d)}{dt} + R_f i_d \\ L_f \frac{d(i_q)}{dt} + R_f i_q \end{pmatrix} \tag{3.27}$$

Note that v_{md} and v_{mq} are the output voltage of the power converter. By having separated dq-components, equation 3.27 is expressed with respect to the system input, u_1 and u_2, representing the input control signal to the state space model. This means that the input of the system is the output of the PI-controller and can be rewritten as:

$$\begin{pmatrix} u_{PI,d}(t) \\ u_{PI,q}(t) \end{pmatrix} = \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix} \tag{3.28}$$

Substituting equation 3.26 into equation 3.24, we get the state equation:

$$x'(t) = Ax'(t) + Bu(t) \Rightarrow \frac{d}{dt}\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \frac{R_f}{R_f} & 0 \\ 0 & -\frac{R_f}{L_f} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{1}{L_f}\begin{pmatrix} u_{PI,d}(t) \\ u_{PI,q}(t) \end{pmatrix} \tag{3.29}$$

Output equation is given by rearranging equation 3.26 on state space form:

$$y(t) = Cx(t) + Du(t) \Rightarrow \begin{pmatrix} v_{md} \\ v_{mq} \end{pmatrix} = \begin{pmatrix} V_{gd} \\ V_{gq} \end{pmatrix} + \begin{pmatrix} 0 & \omega L_f \\ -\omega L_f & 0 \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} - \begin{pmatrix} u_{PI,d}(t) \\ u_{PI,q}(t) \end{pmatrix} \tag{3.30}$$

Equation 3.29 and 3.30 represents the state equation and output equation of the state space model. A block diagram of the equations is drawn in figure D.1 in Appendix

D. In can be redrawn as shown in figure 2.18 in section 2.3.3. Figure 3.10 shows the implemented power control in Simulink. Here, the d-axis error $i_d^* - i_d^{actual}$ and the corresponding q-axis error is added as input to the PI-controllers. Note that this represents a fully decoupled control system, separating active and reactive power commands through i_d and i_q.

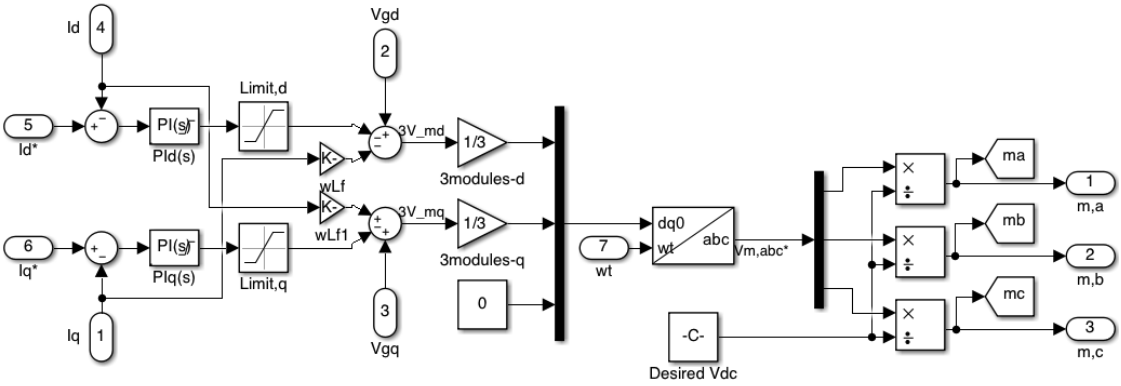


Figure 3.10: Implementation of decoupled current control.

Although the active and reactive components are decoupled, as stated in section 3.3.1, they have the same dynamics [105]. That means that both PI-controllers from figure 3.10 can be tuned based on the same system transfer function. Equation 3.27 emphasizes this point, since the controller output is depending on the same filter, hence, the same system. By isolating the two current loops from figure 3.10, focus can be directed on the d-axis current loop, i_d alone, as seen from figure fig 3.11:

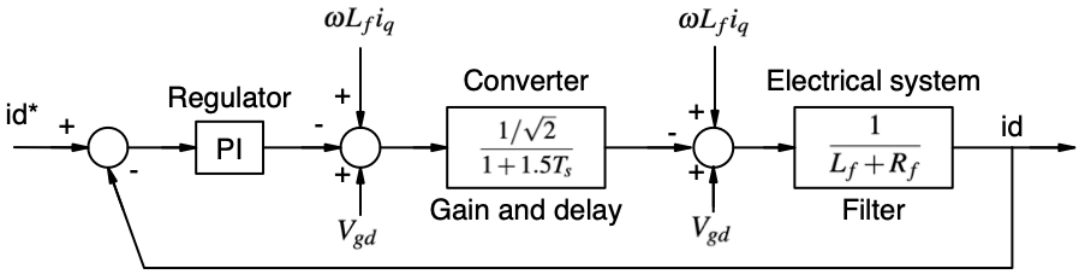


Figure 3.11: D-axis current control loop.

The current loops consist of a PI-controller, the converter delay and the filter process respectively. Some literature operates with a converter gain and delay, $G_{delay}(s) \approx 1$ such as in [6]. However, to model a resemblance of the physical system as accurately

as possible requires laboratory action as shown in [55]. Seeing as this falls out of the scope of this thesis, a generalized transfer function of the converter delay is presented in [105]. This transfer function is implemented into this project, in which completes the transfer functions of the three blocks in figure 3.11, given by [105]:

$$G_{PI}(s) = \frac{k_p(1+T_{is}s)}{T_{is}s} \tag{3.31}$$

$$G_{delay}(s) = \frac{k_{pwm}}{1+1.5T_s s} \tag{3.32}$$

$$G_f(s) = \frac{1}{L_f s + R_f} \tag{3.33}$$

T_s is the sampling time calculated in section 4 and k_{pwm} is the converter gain. Recall that the PI-controller output is expressed by equation 3.27, and that $G_f(s)$ is the filter described by that same equation. Equation 3.33 is the Laplace-domain representation of equation 3.27. An s-plane continuation finding the closed loop transfer function $G_{pc,cl}$ follows:

$$G_{pc,ol}(s) = G_{PI}(s)G_{delay}(s)G_f(s) = \frac{k_p(1+T_{is}s)}{T_{is}s}\frac{1}{1+1.5T_s s}\frac{1}{L_f s + R_f} \tag{3.34}$$

Based on equation 3.34, closed loop transfer function is given by:

$$G_{pc,cl}(s) = \frac{G_{pc,ol}}{1+G_{pc,ol}} = \frac{k_p\frac{L_f s}{R}(1+T_{is}s)}{T_{is}sL_f s(1+1.5T_s s)(1+\frac{L_f s}{R}) + k_p\frac{L_f s}{R}(1+T_{is}s)} \tag{3.35}$$

Equation 3.35 can be simplified so that it resembles a standard second order characteristic equation $s^2 + 2\zeta\omega_n s + \omega_n^2$. The proportional and integral gains of the controller can be found through two sets of equations. Here, the controller damping ratio ζ must be selected at an optimum value. There is inconsistency in literature weather to keep this ratio at critically damped, $\zeta = 1$, or under-damped, $\zeta < 1$. However, it is found that systems with the inclusion of a converter delay, $G_{delay}(s)$, are using $\zeta = \frac{1}{\sqrt{2}}$, such as in [25, 15]. In order to obtain as good results as possible, ζ is taken to equal $\frac{1}{\sqrt{2}}$, which will lead to a converter gain of $\sqrt{2}$ [105]. This must be accounted for when generating the reference values, as shown in table 3.3 in section 3.5. Proceeding with transfer function extraction, the aspect of time constants are of great importance. The speed of the current control loop is related to the current saturation of the output L-filter [10]. Furthermore, it is important for the system dynamics that the zero in the controller transfer function, $G_{PI}(s)$, is cancelling the largest time constant in the system [15]. In this system, that is

the filter time constant $T_f = L_f/R_f$. Using the assumption that $T_{is}s = T_f$ in addition to standard zero-pole cancellation on equation 3.35, we get:

$$G_{pc,cl}(s) = \frac{k_p}{L_f s(1+1.5T_s s)+kp} \tag{3.36}$$

Expressed on standard form, where the denominator of equation 3.36 resembles the second order characteristic equation standard form mentioned earlier, leads to:

$$\frac{\frac{k_p}{1.5T_s L_f}}{s^2 + \frac{s}{1.5T_s} + \frac{k_p}{1.5T_s L}} \tag{3.37}$$

Recognizing that $\omega_n^2 = \frac{k_p}{1.5T_s L_f}$ and $2\zeta\omega_n = \frac{1}{1.5T_s}$ and using values from table 3.1 results in [105]:

$$k_p = \frac{L_f}{3T_s} = 140 \tag{3.38}$$

$$k_i = \frac{R_f}{3T_s} = 43966.67 \tag{3.39}$$

3.3.2 Modelling and design of voltage control loop

The voltage controller has been adopted from [10]. However, a more detailed explanation follows in this section. The outer voltage loop in figure 3.8 is generating the reference current i_d^* sent to the previous described d-axis current controller. The q-axis reference should remain fixed at $i_q^* = 0$, as described in section 3.3. The reference current for the d-axis current-regulator should be controlled in such a manner that it reaches control over the dc-link voltage in each individual module while drawing or delivering a desired amount of active power, P^*. Equation 3.20, derived in section 3.3, can be used to reach this goal by expressing it with respect to the active power only, as $P^* = V_{gd} i_d^*$. Modelling proceeds by simplifying the configuration into a single module, as shown in figure 3.12:

The objective is to control the voltage across the dc-link capacitor. Figure 3.12 is drawn under the assumption that the dc-dc converter is neglected, meaning that the battery current is equal to the dc-link current. Here, the battery is replaced with an equivalent resistance, R_b, mentioned in section 3.1.3. Kirchhoff's Current Law (KCL) can therefore be applied for one module in the circuit in figure 3.12, leading to:

$$i_{grid} = i_c + i_{R_{th}} \tag{3.40}$$

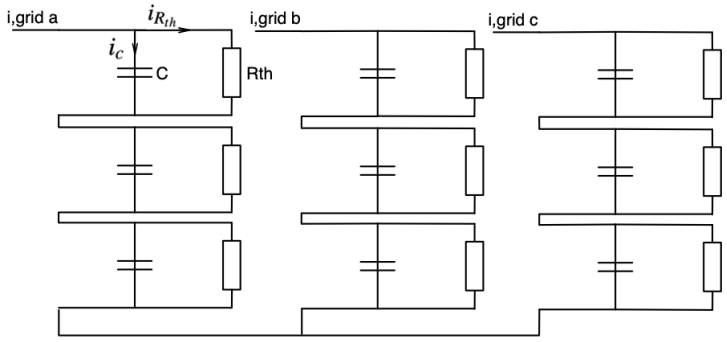


Figure 3.12: Simplified KCL circuit for voltage loop control.

Expressing equation 3.40 with respect to active power on both grid-side and dc-side leads to:

$$v_{gd} i_{gd} = v_c i_c + v_c i_{R_{th}} \tag{3.41}$$

Here, the left hand side term can be substituted with the grid-side active power, $P =_{gd} i_d$ from equation 3.20. Additionally, equation 3.41 must be expanded so that the voltage control loop is valid for nine modules, as shown in figure 3.12. Further rearrangements are needed in order to extract controllable signals. Substituting $i_c = C\frac{d(v_c)}{dt}$ and $v_c i_{R_{th}} = \frac{v_c^2}{R_{th}}$ in equation 3.41 leads to:

$$9 v_{gd} i_d = v_c C \frac{d(v_c)}{dt} + \frac{v_c^2}{R_{th}} \tag{3.42}$$

Applying Laplace-transform leads to:

$$\mathscr{L}\{P\} = 9 v_{gd} i_d = v_c^2 C s + \frac{v_c^2}{R_{th}} \tag{3.43}$$

The target is to control the dc-link voltage, v_c. Solving equation 3.42 with respect to the transfer function $G_{v,ol}(s) = \frac{v_c}{i_d}$ leads to:

$$9 v_{gd} i_d = v_c (v_c C s + \frac{v_c}{R_{th}}) \tag{3.44}$$

And the open loop transfer function $G_{v,ol}(s)$ is obtained using table 3.1 as:

$$G_{v,ol}(s) = \frac{v_{dc}}{i_d} = \frac{v_{gd}}{9 v_{dc}(Cs + \frac{1}{R_{th}})} = \frac{325}{18.68s + 65.25} \tag{3.45}$$

While the speed of the current loop should depend on the output filter current saturation, the voltage loop speed should be limited by the output current magnitude [10].

One way to reach this goal is to make sure that the inner current loop is much faster than the voltage loop. In general, the variables controlled in an arbitrary power circuit is the capacitor voltage or the inductor current. Inductor current is normally the faster variable, which in turn makes a current control loop the natural choice to design as the inner, faster loop [42]. This effectively make the system dynamics of figure 3.8 approximately equal to the voltage control loop. With this in mind, figure 3.8 can be simplified into figure 3.13.

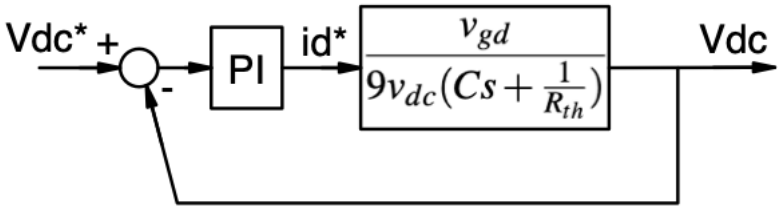


Figure 3.13: Power control loop simplified into outer voltage control loop.

3.3.3 Module dc-link voltage balancing control

The dc link capacitor voltage balancing is modelled by small signal model analysis, inspired from [94]. There is, however, made some changes for system adaption. The dc link voltage balancing can be reached by modifying the modulation index in the PS-PWM so that the small deviations in the dc link voltages across the nine modules are corrected. This means that it is sufficient to direct focus towards the BDAC converter conditions and the dc link capacitor. Then the battery and BDC converter is taken as a load connected to the dc link terminal, such as in section 3.3.2. Using figure 3.4 to apply KCL, leads to:

$$i_c = i_{in} - i_{out}. \tag{3.46}$$

The input current is the current flowing from the BDC converter into the dc link. The ac-side current i_{out} can be described by rearranging equation 3.9 so that it is described by both the modulation index and the capacitor voltage. Note that i_{out} is a dc-current, and under the assumption that $cos\theta \approx 1$, it can be written as:

$$i_{out} = \frac{3mv_c}{R_{th}} \tag{3.47}$$

Note that the BDC converter components is neglected so that R_{th} from section 3.1.3 is applied. Substituting values for i_c and i_{out} in equation 3.46 leads to:

$$\frac{d(v_c)}{dt} = \frac{i_{in}}{C} - \frac{3mv_c}{R_{th}} \tag{3.48}$$

Equation 3.48 can be introduced to small perturbing signals for the three variables, given by:

$$\begin{cases} v_c = V_c + \tilde{v}_c \\ m = M + \tilde{m} \\ i_{in} = I_{in} + \tilde{i}_{in} \end{cases} \tag{3.49}$$

The perturbing terms denoted by " $\sim$ " are small signal representation of oscillation in the dc link, modulation index and input current respectively. Uppercase letters represents the steady state dc-value. Seeing as the interesting terms are given by the small signal variables, they can be written using equation 3.49 into equation 3.48 so that:

$$\frac{d(\tilde{v}_c)}{dt} = \frac{\tilde{i}_{in}}{C} - \frac{3\tilde{m}V_c}{R_{th}C} - \frac{3M\tilde{v}_c}{R_{th}C}. \tag{3.50}$$

In steady state, the small signal input current is equal to zero [94]. Additionally, by applying Laplace on equation 3.50 results in:

$$\tilde{v}_c s = -\frac{3\tilde{m}V_c}{R_{th}C} - \frac{3M\tilde{v}_c}{R_{th}C} \tag{3.51}$$

Terms containing $\tilde{v}_c$ can be collected so that $\tilde{v}_c$ can be factorized, leading to:

$$\tilde{v}_c(s + \frac{3M}{R_{th}C}) = -\frac{3\tilde{m}V_c}{R_{th}C} \tag{3.52}$$

Now, the process transfer function $\frac{\tilde{v}_c}{\tilde{m}}$ can be calculated by dividing on both $\tilde{m}$ and the left hand side bracket term. Furthermore, second order terms can be neglected [94]. $G_{v,bal}(s)$ is therefore given by:

$$G_{v,bal} = \frac{\tilde{v}_c}{\tilde{m}} = -\frac{3V_c}{RCs + 3M} = -\frac{459.99}{0.29s + 2.562} \tag{3.53}$$

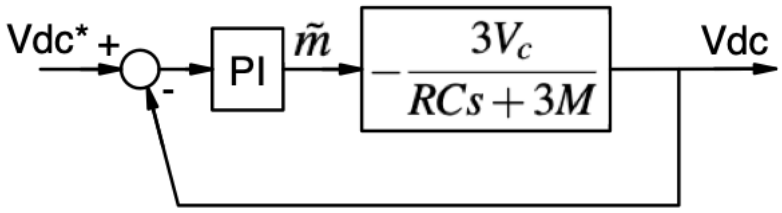


Figure 3.14: Voltage balancing control loop.

The modified modulation index $\tilde{m}$ is connected to the initial modulation index M provided by the current controllers $u_{pi,d}$ and $u_{pi,q}$ through:

$$m = (M - \tilde{m}) \tag{3.54}$$

It should be noted that since M is a sine wave between $0.677 < M < 1$ and $\tilde{m}$ only serves as a correction to its magnitude, they must be multiplied as depicted in figure 3.15. This can be realized in Simulink by factorizing M outside the brackets so that both M and $\tilde{m}$ can be merged in the model [10]. The practical model implementation of the voltage balancing controllers for nine individual modules are shown in figure 3.15. The nine output tags $Ma1, Ma2, \cdots, Mc3$ are multiplied with the modulation index m for their respective phase, keeping consistence with equation 3.54. Here, the controller input reference value is the same as the outer loop voltage controller V_{dc}^{*}.

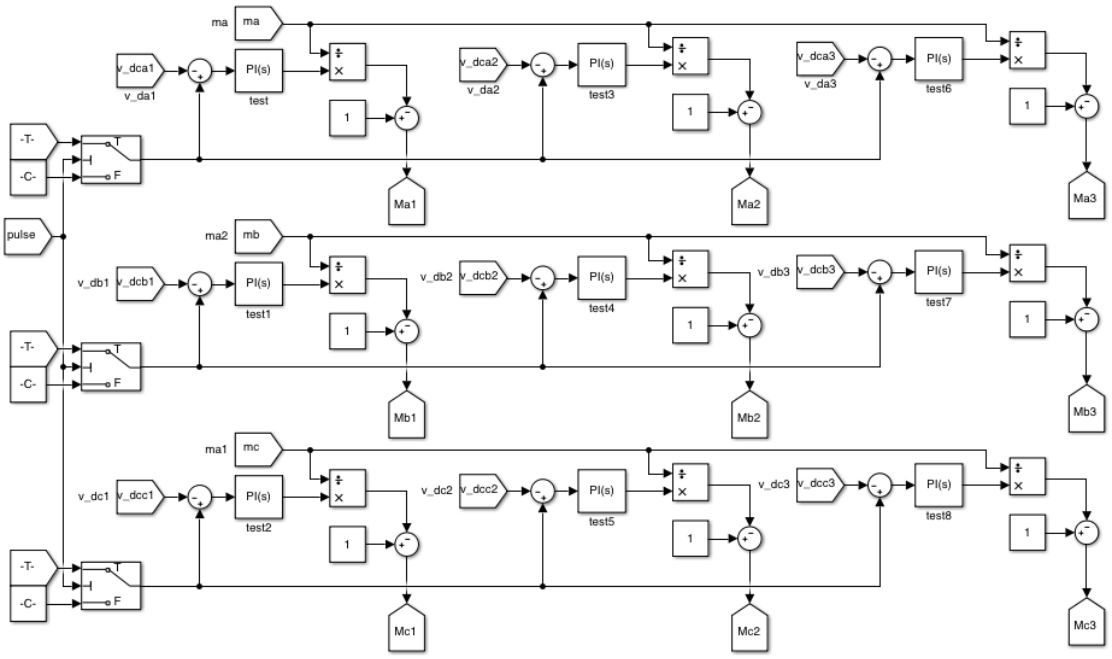


Figure 3.15: Simulink implementation of individual module voltage balancing.

A similar arrangement can be applied as phase balancing controls, meaning that three balancing controllers is added to the capacitor balancing arrangement. Using the same controllers as for the individual modules, the only difference is that the error the controllers serve to correct is given by $V_{dc}^{*} - V_{phase,avg}$. Furthermore, it corrects the phase modulation signals M_{abc} instead of individual module modulation signals $M_{a_1}, M_{a_2} \cdots M_{c_3}$. Additionally, it should be noted that when charging pulse turns active, a simple start-up control logic should be applied, as shown in figure 3.16. The reason is that when the system enables charge from either off-mode or discharge-mode, the outer loop voltage controller increases the dc link voltage from $108.42V$ to $108.42\sqrt{2}$. During the rise time, the reference deviation is significantly larger than the steady state error. In these situations, a controller integral windup may occur [43]. In order to deal with this,

the reference voltage set point for the nine individual balancing controllers is given by the average of the dc link voltages across the corresponding phases. As for the three phase balancing controllers, the input reference is set to be the average of all the nine modules. This is shifted to V_{dc}^{*} after the delay period which is settled to equal to the outer voltage controller settling time.

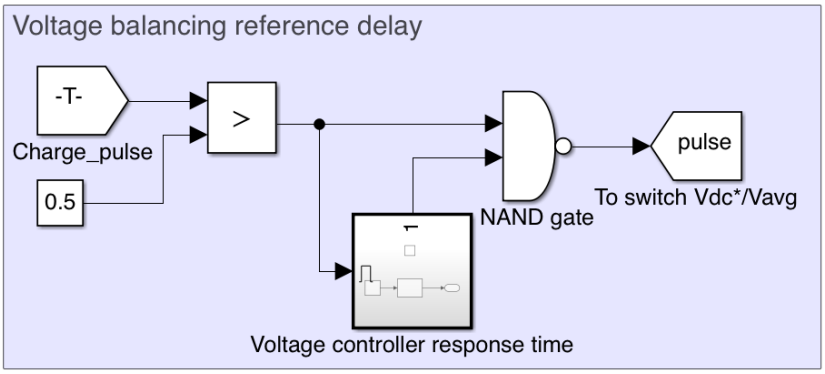


Figure 3.16: Implemented reference delay logic.

3.3.4 PS-PWM

The module reference voltage $V_{m,abc}^{*}$ generated in the BDAC converter is used as control signal, $v_{control}$, for modulation of the semiconductor gates. This signal operates at the fundamental frequency of $50Hz$ in which dictates the output frequency of the voltages and currents. First, the reference signal must be modified before it is used for PWM action. Modification of $V_{m,abc}^{*}$ is necessary in order to produce the control voltage used to modulate the switch duty ratio [2]. Seeing as there are three modules per phase, the module reference voltage should be divided by three, as seen from equation 3.55. For a single phase bipolar full-bridge ac-dc converter, the control voltage magnitude is given by:

$$\hat{v}_{control} = \frac{\hat{V}_{out}}{v_d} = \frac{\hat{V}_{m,abc}}{3v_{dc}}, \tag{3.55}$$

Furthermore, the reference voltage magnitude over a single module is, with small deviations, approximately equal to the dc-link voltage, V_{dc}. Therefore, the resulting control voltage magnitude given by equation 3.55, is close to 1. The control voltage is compared to a carrier signal, v_{tri}. The resulting signal gives the switching pulses which is sent to the IGBT gates. v_{tri} represents the carrier signal in which is a repetitive triangular waveform with a peak amplitude of $\hat{v}_{tri} = 1$ at the switching frequency $f_{sw} = 5kHz$. As a result, the carrier frequency dictates the switching frequency of the BDAC switches,

while the frequency of the control voltage controls the fundamental frequency of the converter output. The ratio between $\hat{v}_{control}$ and $\hat{v}_{tri}$ indicates the amplitude modulation ratio m_a, given by [2]:

$$m_a = \frac{\hat{v}_{control}}{\hat{v}_{tri}} \tag{3.56}$$

Although $\hat{v}_{tri}$ is kept constant, $\hat{v}_{control}$ varies along with P^*, which in turn varies the modulation index m_a. If $m_a > 1$, that is if $V^*_{m,abc} > 3V_{dc}$, then the converter will operate in overmodulation mode. In general, this is an undesired mode of operation due to non-linear disruption in the harmonics spectrum [2]. To ensure $m_a \leq 1$ during both charging and discharging operations, a limit-block is implemented before modulation action takes part in the control system. This way the condition presented in equation 3.57 is fulfilled.

$$\hat{v}_{control} \leq \hat{v}_{tri} \tag{3.57}$$

PS-PWM is a multi-carrier modulation technique. In order to apply PS-PWM technique for switching signals, the required number of carriers is given by the level order, n_l of the converter. Given that the BDAC converter used in this analysis is 7-leveled, the required number of carriers, n_c is given by equation 3.58:

$$n_c = n_l - 1 = 6 \tag{3.58}$$

There are $4 \cdot 3$ semiconductors per phase operating in the BDAC converter. That means that each carrier is designated to two switches, both in the same leg. The six triangular carriers have the same amplitude and frequency, but there is a phase shift with respect to the previous carrier, as described in table 3.2. The phase shift angle, ϕ_c is given by:

$$\phi_c = \frac{360°}{n_c} = 60° \tag{3.59}$$

The carriers are arranged in such a manner that the two legs in one converter is phase shifted 180°[54]. An overview of the arrangement is showed in table 3.2.

Module	**Leg 1**	**Phase shift**	**Leg 2**	**Phase shift**
1	Carrier 1	0°	Carrier 4	180°
2	Carrier 2	60°	Carrier 5	240°
3	Carrier 3	120°	Carrier 6	300°

Table 3.2: One phase carrier arrangement.

The reasoning derived above for single-phase phase shift is valid regardless of phase sequence [54]. In other words, the carriers used for phase a are reused for the corresponding switches in phase b and c. The reference module voltage, $V^*_{m,abc}$ provides the

needed 120° shift between the three output phases. Figure 3.18 illustrates how this is solved in the actual control system. The switching signals in figure 3.18 are redirected through tags containing the specific gate address on the form ϕmn. Here, ϕ represents phase, m gives the module number based on table 3.2, and n gives the exact IGBT component based on figure 3.17.

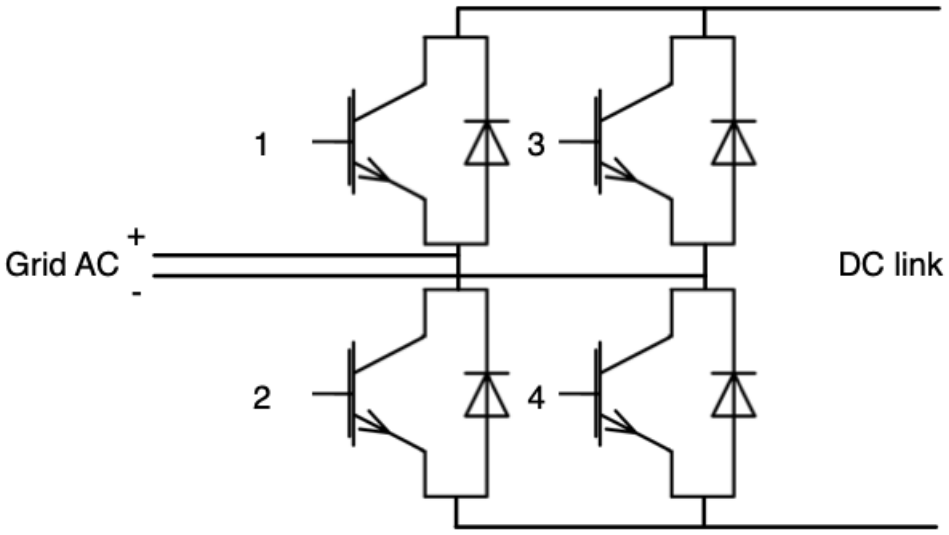


Figure 3.17: IGBT numbering in each individual module. Leg 1 contains IGBT 1-2 and leg 2 contains IGBT 3-4.

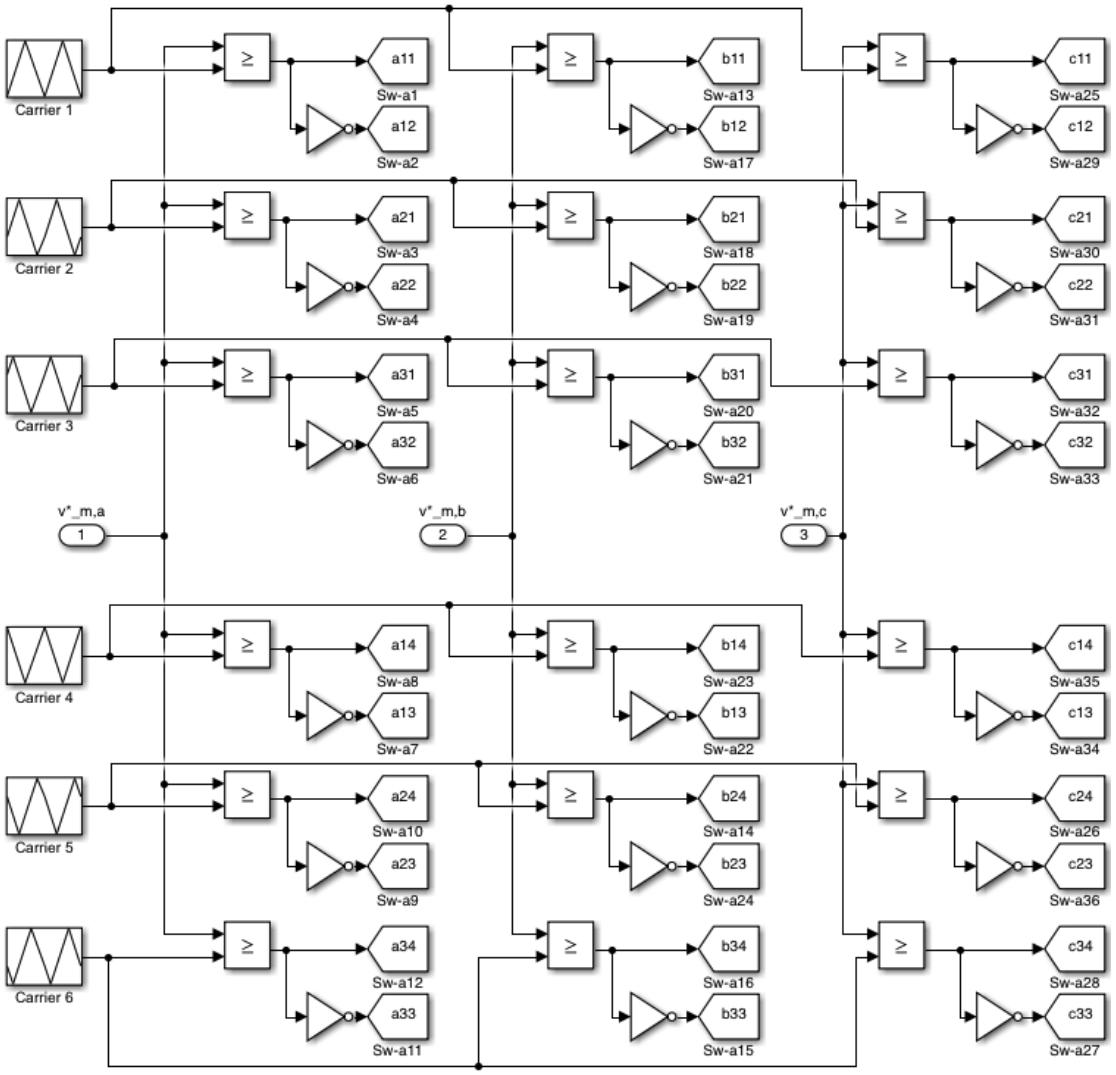
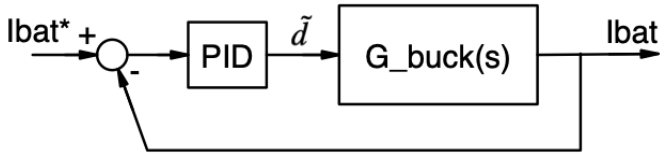


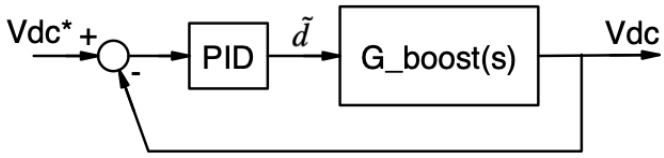
Figure 3.18: Switching signals directed to 36 gates.

3.4 BDC converter

Section 2.3.2 presented the dc-dc converter topology in brief discussion. This section is giving a detailed dive into the design strategy. The objective of the dc-dc converter is threefold. Firstly, the converter manages power flow between the dc-link and the battery. Secondly, it separates the dc-link and the battery so that the dc-link voltage can be controlled in a desired manner. Thirdly, it provides galvanic isolation through a high frequency isolation transformer, described in section 2.3.2. An outline of the control strategy is covered in section 3.2. Figure 3.19 shows the aim of the BDC modelling in order to obtain a process transfer function for controller tuning.



(a) Buck mode.



(b) Boost mode.

Figure 3.19: BDC converter control loop for both charge and discharge.

The modelling of the BDC-converter is performed using a state space model representation. Linearization of the power stage is done through the four-step methodology described in [2]. The first objective is to describe each circuit state through a state space representation. However, due to the voltage difference between the input and output side of the converter, the modelling must be divided into buck mode and boost mode of operation. The grid is connected to the HV-side, and the battery to the LV-side. That is, when the battery is charging, the converter is operating in buck mode. Discharging process requires boost mode of operation respectively. Although the converter isolated speaking is operating as a buck-boost converter, each H-bridge only has one mode of operation.

In general, there are two modes of operation for a PSFB dc-dc converter: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) [2]. The characteristics of each mode is notably different from each other, so that each mode should be taken into consideration during converter design. However, the design strategy of this PSFB BDC converter have been to make two simplifications: (1) small signal model is

obtained during CCM, following the recipe from [2], and (2) using switching waveform and equivalent circuits obtained from [19]. Furthermore, the modulation technique used for base signals must be considered before a model transfer function is derived. This converter is controlled by a PID-controller which outputs an adjusted duty ratio, d, sent to the IGBT gates. As explained in section 3.2, the goal is to control the battery output current I_{bat}, during the charging process, and the dc-link voltage, V_{dc}, during discharging mode of operation. Accordingly, the target for buck mode and boost mode is the small perturbing signals $G_{buck}(s) = \frac{\tilde{i_{bat}}}{\tilde{d}}$ and $G_{boost}(s) = \frac{\tilde{v_{dc}}}{\tilde{d}}$ respectively. A detailed design for boost mode follows in section 3.4. Buck-mode modelling is designed in a similar fashion, so that this is conducted in Appendix A.2.

Boost mode of operation

Figure 3.20 shows the gate pulse signals for boost mode of operation. Note that the duty ratio, d, describes the ratio of the period in which the switch is conducting with respect to the total switching cycle, as $d = \frac{t_{on}}{T_s}$. An analysis of the full switching cycle, T_s, must be applied in circuits containing two semiconductors in order to cover both on/off states, as in [2]. Regarding the different circuit states of a H-bridge, it is sufficient to analyze half the switching cycle, $\frac{T_s}{2}$, of the four switches. For boost mode, the two states is the (1) conduction of both leg L1 and L2 during dT_s, and (2) when only one pair, S1, S4 or S2, S3 are conducting. This is during the time interval $(1-d)T_s$. Reduction into half a switching cycle for state (1) leads to [19]:

$$\frac{T_s}{2} = (d - \frac{1}{2}) \tag{3.60}$$

For state (2), the time interval is:

$$\frac{T_s}{2} = (1 - d) \tag{3.61}$$

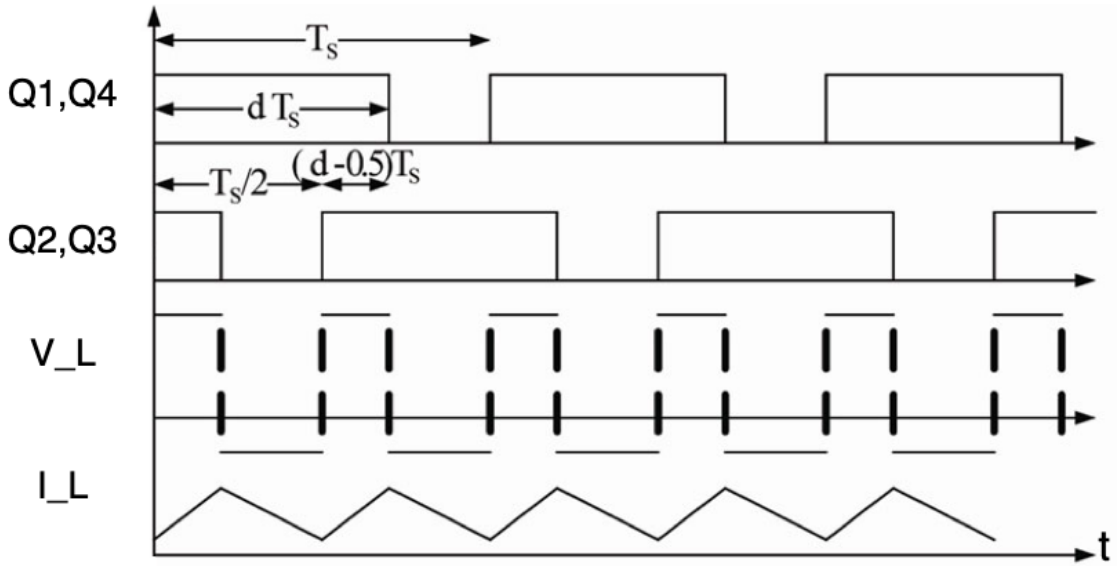


Figure 3.20: Switching waveforms for boost mode. Adapted from [19].

For boost mode, the battery is delivering power into the grid. That means that switches Q1-Q4 is active, while switches S1-S4 is open. The free-wheeling diode in parallel with the IGBT S1-S4 on the HV-side is conducting, working in rectifier mode as shown in figure 3.21. A study regarding the inclusion of switching losses and parasitic elements in the semiconductors have been conducted in [5]. Due to the load, R_L being significantly larger than the equivalent of these elements, $R_L >> R_{eq}$, these are neglected in this analysis. The high frequency transformer is also beyond the reach of this thesis, meaning that they are treated as ideal.

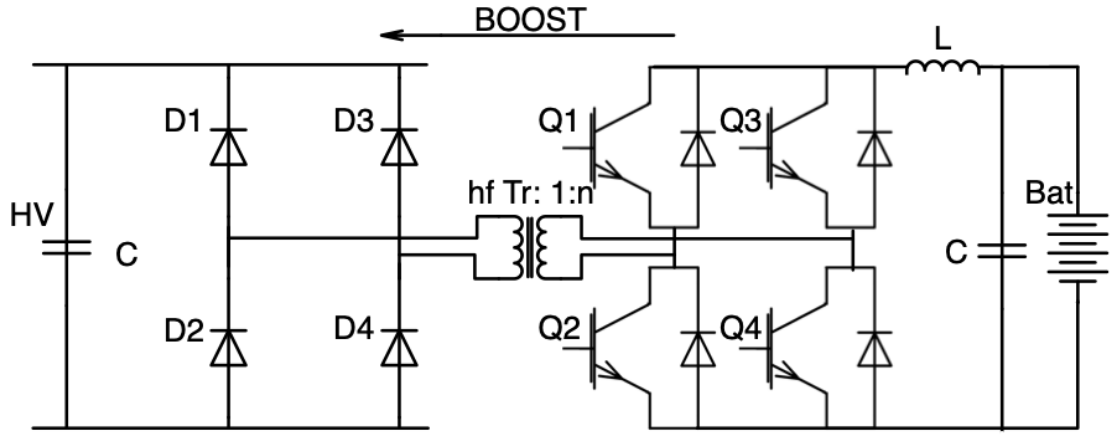


Figure 3.21: BDC converter during boost, where Q1-Q4 switches are active.

During the time all switches conduct, the inductor current, i_L, increases, while the dc-link capacitor discharges stored power into the grid. The battery voltage, V_{bat} is therefore equal to the inductor voltage, v_L. Seeing as all four switches in theory is active, and thus can be treated as the main source shorting the primary transformer side of the circuit, the two transformer sides can be viewed separately. Therefore, the equivalent circuit shown in figure 3.22 can be drawn [19].

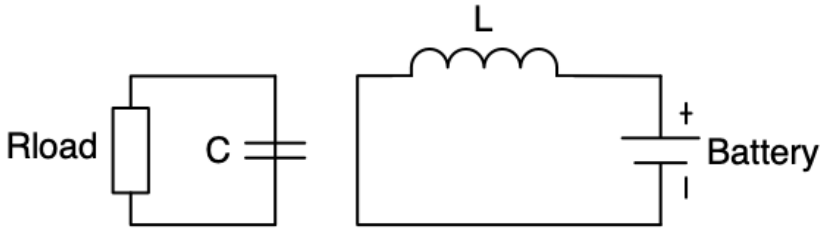


Figure 3.22: Four-switch equivalent circuit of BDC converter during boost mode.

Applying KVL on the LV battery-side in figure 3.22 leads to:

$$V_{bat} = L\frac{d(i_L)}{dt} \tag{3.62}$$

Applying KCL on the HV-side leads to:

$$\frac{v_c}{R_L} = -C\frac{d(v_c)}{dt} \tag{3.63}$$

Rearranging equation 3.62 and 3.63 with respect to the state variables $x_1'(t) = i_L'(t)$ and $x_2'(t) = v_c'(t)$ results in:

$$\frac{d(x_1)}{dt}|_{state(1)} = \frac{d}{dt}\begin{pmatrix} i_L \\ v_c \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix}\begin{pmatrix} i_L \\ v_c \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_{bat} \tag{3.64}$$

Equation 3.64 represents the state equation $x'(t) = A_1x + B_1u$ of the first circuit state. During boost mode, the desired variable to control is the dc-link voltage, $V_{dc} = v_c$. The output equation is therefore given by:

$$y_{0,1} = C_1x + D_1u = \begin{pmatrix} 0 & 1 \end{pmatrix}\begin{pmatrix} i_L \\ v_c \end{pmatrix} + 0u \tag{3.65}$$

The second state is during two-switch conduction, either by pair S1, S4 or S2, S3. During this state, the stored energy in the inductor dissipates through the transformer winding and into the HV-side diodes. When the transformer transfers energy from the battery, the transformer ratio $1 : n$ must be included [19]. Consequently, the equivalent circuit of state (1) is modified for state (2) as shown in figure 3.23.

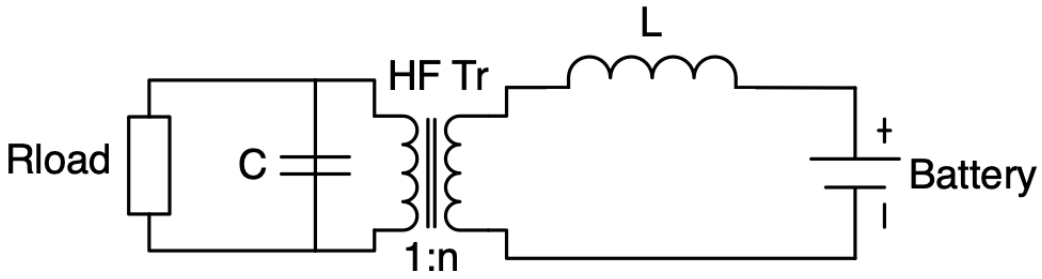


Figure 3.23: Two-switch equivalent circuit of BDC converter during boost mode.

Applying KVL upon the circuit in figure 3.23 results in:

$$v_{bat} - v_L - \frac{v_c}{n} = 0 \Rightarrow \frac{d(i_L)}{dt} = \frac{V_{bat}}{L} - \frac{v_c}{nL} \tag{3.66}$$

Obtaining the second state variable, v_c, through KCL results in:

$$i_L - ni_c - ni_{Load} = 0 \Rightarrow \frac{d(v_c)}{dt} = \frac{i_L}{nC} - \frac{v_c}{CR} \tag{3.67}$$

The circuit state equation during state 2 is found by rearranging equation 3.66 and 3.67 as follows:

$$\frac{d(x_2)}{dt}|_{state(2)} = \frac{d}{dt}\begin{pmatrix} i_L \\ v_c \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{nL} \\ \frac{1}{nC} & -\frac{1}{RC} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_{bat} \tag{3.68}$$

The output, v_c, is the same for both states, meaning that the output matrix $C_1 = C_2$. The same observation can be made for matrix $B_1 = B_2$. This is of importance when averaging the circuit over one switching period. The state- and output equation averaging can be reached by adding the equation from state 1 and 2, and multiply them with their corresponding active duty period, given by equation 3.60 and 3.61 [2]. This can be expressed mathematically for state equation and output equation respectively as:

$$\frac{d(x)}{dt} = [A_1 d + A_2(1-d)]x(t) + [B_1 d + B_2(1-d)]u(t) \tag{3.69}$$

$$y_o = [C_1 d + C_2(1-d)]x(t) \tag{3.70}$$

The two state equations 3.64 and 3.68 has been derived across half the switching period, $\frac{T_s}{2}$. Equation 3.70 results in an average description of the two states across the total switching period. Multiplying equation 3.60 and 3.61 by two brings the circuit descriptions into one full switching period, T_s. This results in $T_s|_{state(1)} = 2d - 1$ and

$T_s|_{state(2)} = 2(1-d)$. This is inserted as the time aspect of the switching states in equation 3.70, replacing d and $(1-d)$. Inserting the state equations and the output matrix into equation 3.69 and 3.70 results in the averaging matrix:

$$A = \begin{pmatrix} 0 & \frac{2(d-1)}{nL} \\ \frac{2(1-d)}{nC} & -\frac{1}{RC} \end{pmatrix} \tag{3.71}$$

$$B = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} \tag{3.72}$$

$$y_o = \begin{pmatrix} 0 & 1 \end{pmatrix} \tag{3.73}$$

The state variables, represented by $x(t) = (i_L, v_c)$, as well as the duty ratio d all represents the total quantity of the variable. It can be separated into dc and ac quantities. Given that these are dc circuits, the majority consist of a dc value, only varied by a small ac perturbation. Introducing small ac perturbations to the dc quantity leads to:

$$\begin{cases} x = & X + \tilde{x} \\ d = & D + \tilde{d} \\ v_{bat} = & V_{bat} + \tilde{v}_{bat} \end{cases} \tag{3.74}$$

Uppercase letters represents dc components, and small ac perturbation is represented by the symbol " $\sim$ ". For simplicity, the small ac perturbation $\tilde{v}_{bat}$ is neglected, so that $v_{bat} = V_{bat}$, as in [2]. Obtaining a small signal steady state transfer function requires a substantial amount of calculation over several expressions. As a consequence, this is realized in Appendix A.1. Continuing here, it is sufficient to clarify the procedure to reach the goal $\frac{\tilde{v}_c}{\tilde{d}}$. Having found the averaging state variable expression by including the duty ratio, an equivalent expression of the small signal, $\tilde{x}'(t)$, can be derived. This is given by equation 3.75:

$$\frac{d(\tilde{x})}{dt} = AX + BV_{bat} + A\tilde{x} + [(A_1 - A2)X + (B_1 - B_2)V_{bat}]\tilde{d} \tag{3.75}$$

In steady state, the small perturbing terms an their derivatives equals zero. That means that the two firs terms $AX + BV_{bat}$ equals zero, and[2]:

$$\frac{d(\tilde{x})}{dt} = A\tilde{x} + [(A_1 - A_2)X + (B_1 - B2)V_{bat}]\tilde{d} \tag{3.76}$$

Similarly, the same can be applied to the output equation 3.70. This leads to [2]]:

$$\tilde{v}_c = C\tilde{x} + [(C_1 - C_2)X]\tilde{d} \tag{3.77}$$

Equation 3.76 and 3.77 must be transformed into the frequency domain through Laplace transform. Applying Laplace to the two previous mentioned equations and rearranging

so that they are solved in terms of $\tilde{v}_c$ and $\tilde{d}$ respectively, leads to the system transfer function of the BDC converter[2]:

$$G_{bdc}(s) = \frac{\tilde{v}_c}{\tilde{d}} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)Vbat] + (C_1 - C_2)X \tag{3.78}$$

From Appendix A.1, the transfer function $G_{bdc}(s)$ can be written as:

$$\begin{aligned} \frac{\tilde{v}_c}{d} &= \frac{-I_L nRLs + RV_c(2-2d)}{n^2RLCs^2 + n^2Ls + R(4d^2 - 8d + 4)} \\ &= \frac{-0.01s + 1147.08}{8.69 \cdot 10^{-5}s^2 + 6.07 \cdot 10^{-4}s + 10.58} \end{aligned} \tag{3.79}$$

3.4.1 PWM

The BDC converters are using conventional PWM technique by regulating the desired duty ratio, d^* through a PI-regulator. The algorithm is shown in figure 3.24 and is adopted from [85]. The duty ratio signal resembles a phase signal, $wt = 2\pi ft$, much similar to a PLL-output. However, the phase signal output from a PLL is almost a completely linear slope, only increasing by t. Here, as d^* changes, so does the gradient slope of the phase signal.

```
function [pwm2, pwm1] = fcn(time, f, phase)
T_sw = (1/f);
pwm1 = 0; pwm2 = 0;
x = mod(time, T_sw);
if x < T_sw*0.55
    pwm1 = 1;
end
t_fi = T_sw*phase/360;
y = mod(time+t_fi, T_sw);
if y<T_sw*0.55
    pwm2=1;
end
```

(a) Charge.

```
function [pwm2, pwm1] = fcn(time, f, phase)
T_sw = (1/f);
pwm1 = 0; pwm2 = 0;
x = mod(time, T_sw);
if x < T_sw*0.45
    pwm1 = 1;
end
t_fi = T_sw*phase/360;
y = mod(time+t_fi, T_sw);
if y<T_sw*0.45
    pwm2=1;
end
```

(b) Discharge.

Figure 3.24: PWM algorithm for BDC gate pulses, representing the Matlab function blocks "Discharge 1-3" in figure 3.25. Adapted from [85].

As described in section 3.4, the waveform concerning the duty ratio for both buck and boost mode of operation differ from each other. For charging duty, the effective duty ratio, $d_{effective}$ is set to 0.55 for optimum results. For discharging duty, the effective duty ratio $d_{effective} = 0.45$. As seen from the first line in figure 3.24, the math function block has three inputs. Along with the PI-controller output, it also receives an internal system

clock time and switching frequency f_s. The former represents simulation time counter, while the latter provides the desired converter f_s at $20kHz$ as explained in section 3.1. Although the switching frequency may vary in some applications, it is kept constant in PWM control [2].

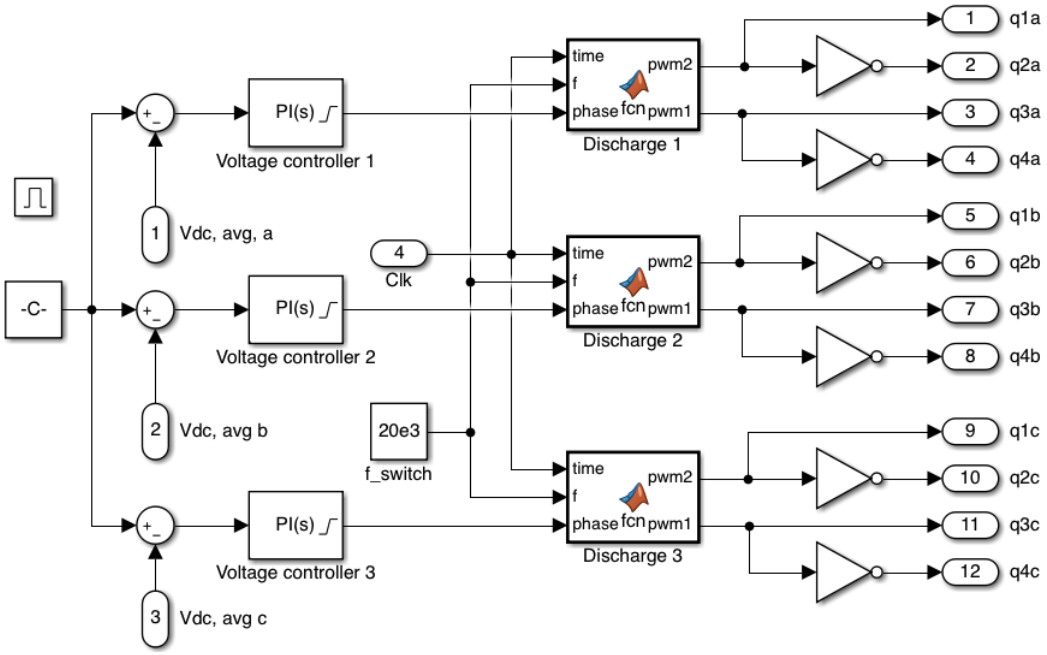


Figure 3.25: PWM for BDC converter implemented in Simulink. This figure represents discharge, while the charging controls is designed in a similar manner.

Figure 3.25 shows the switching signals for the BDC converter. Although this generates switching signals for discharge mode, the charging signals are generated in the same way. The only difference is the Matlab function block described in figure 3.24 and the controllers. The controllers for discharge mode controls the desired dc link voltage. For three modules per phase, the reference voltage is taken to be $3 \cdot 108.42V$, while the actual values is the average dc link voltages of each phase. As a result, the switching signals are separated into three phases, as shown in figure 3.25. The switching signals are generated in a enabled subsystem so that only one bridge is active at the time. The enabling controls are described in section 3.6. An important note is that the controls must ensure that there are no constant gating pulse when the activation from one bridge to another is enabled. This will lead to a semiconductor short circuit, which will bypass the current past the intended diode pathway. This may lead to a negative domino effect of voltage drop across the gate-junction, thus a higher power dissipation leading to local temperature rise in the silicon wafer of the IGBT [2]. This has been avoided by passing a constant zero as gate signal whenever the corresponding subsystem is disabled.

3.5 Converter synchronization

Grid-tied BESS needs to be synchronized to the utility before connection. Phase-Locked Loop (PLL) is a useful tool which detects the phase of the grid voltage and feeds the corresponding phase angle to the control system [14]. The PLL consist of three main building blocks, namely a Phase Detector (PD), Voltage Controlled Oscillator (VCO) and a Loop Filter (LF) [39]. Using the grid voltage as the reference input, the PD detects the phase, and feeds the error between the grid-phase and the VCO output to the LP. The error is processed in the LP, in which is generating the input signal to the VCO. The reference angle at the VCO output is sent both to the control system, and back to the phase detector, completing the loop as shown in figure 3.26. Suitable designs are mentioned in [14]. However, the three-phase PLL integrated in the Matlab Library is used in this model in order to release computational burden.

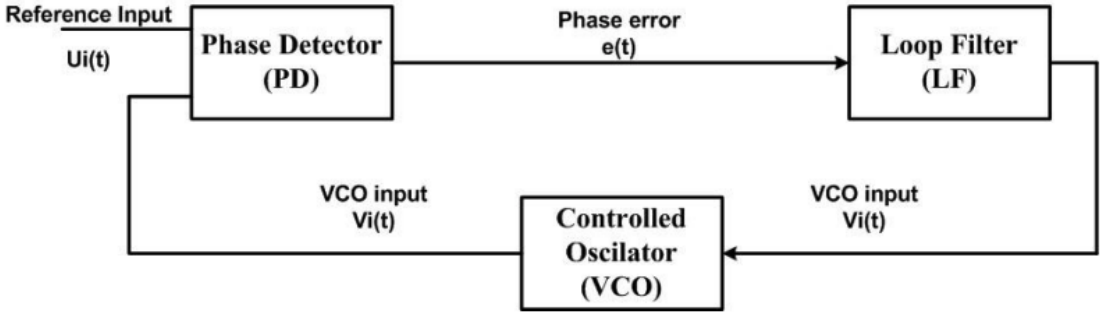


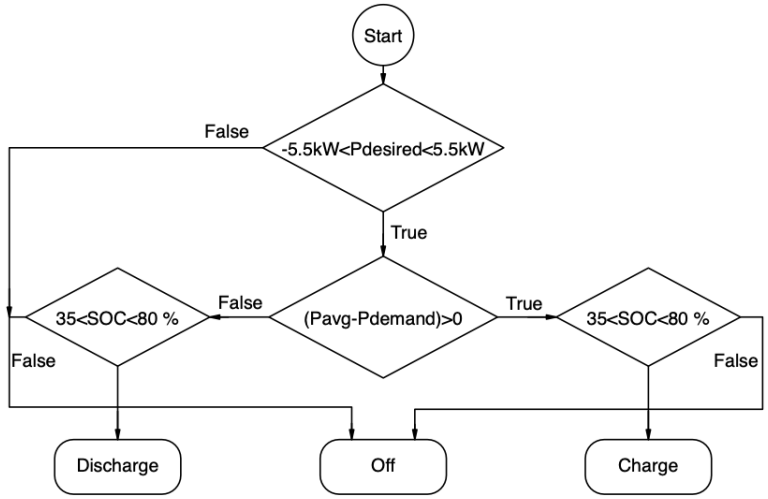
Figure 3.26: The three building blocks composing a Phase Locked Loop (PLL) [14].

Additionally, there must be an internal synchronization between the BDAC and BDC converters. The currents needs to be synchronized in order to release the same amount of power from both converters. Having the back-end converter releasing more power than the front-end converter transfers, will result in a power dissipation in the filter components and IGBTs, leading to major component stress, temperature rise and low efficiency. On the other side, if the front-end converter tries to transfer more power than available, the conducted EMI and harmonics injected into the terminal load will increase significantly. A notable difference between P_{BDC} and P_{BDAC} will result in a non-functioning system and, in worst case, temperature surges and component failure. To deal with this issue, the reference values used for all outer-loop regulators must be calculated based on the total system dynamics. The results are listed in table 3.3.

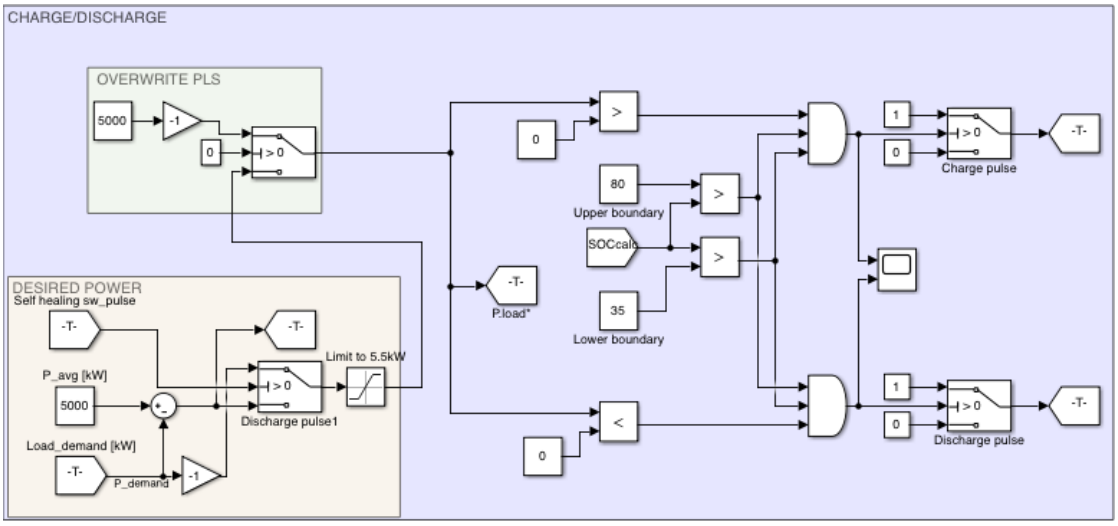
	Charge	Discharge
BDAC	$V_{dc}^{*} = v_{n_1}\sqrt{2}$ (equation 3.6)	$i_d^{*} = \frac{P_{avg}-P_{demand}}{\sqrt{2}v_{gd}} = \frac{P^{*}}{v_{gd}}$
BDC	$i_{bat}^{*} = \frac{v_{gd}i_d}{3} = \frac{\sqrt{3}P^{*}}{9v_{n_1}}$	$V_{dc}^{*} = 3v_{n_1}$

Table 3.3: Calculation of desired values.

3.6 Peak load shaving strategy



(a) General PLS flowchart.



(b) Simulink control logic.

Figure 3.27: Control logic for charging and discharging operation.

The control software has been implemented using logic blocks. Using PSFB dc-dc converter requires control regarding which bridge to activate. Additionally, there are safety and reliability conditions that needs to be fulfilled. Figure 3.27 gives an overview of the general PLS control.

Figure 3.27 contains three conditions, listed in equation 3.80-3.82. The first condition calculates whether to charge or discharge the batteries in order to maintain the grid power at P_{avg}. If the flowchart finds this condition to be true, then the battery charging circuits are activated. Otherwise, the BESS will discharge. This condition is the main contributor to achieve PLS. The second condition directly limits the power output to $\pm 5kW$. The consequence of surpassing this limit is that the BESS is not capable to maintain the grid power at P_{avg}. Having said that, this is when the BESS is delivering or drawing max rated power, in which will have significantly improved the peak loads nevertheless. Additionally, the third condition is that the batteries SOC-state is within acceptable limits. These conditions can be written more specifically as:

$$1. \quad P_{avg} - P_{demand} > 0 \tag{3.80}$$

$$3. \quad -5.5kW < P_{desired} < 5.5kW \tag{3.81}$$

$$2. \quad 35 < SOC_{\%} < 80 \tag{3.82}$$

Figure 3.27a shows the flowchart implemented in Simulink. Here, the desired power generation from the first condition in equation 3.80 is generated in the yellow box. The switch turns active if the grid supply is disconnected, meaning that the self healing logic takes over active power calculation. Details regarding this is found in section 3.7. Further, it should be noted that the terms in equation 3.80 to 3.82 are only related to the PLS system in order to maintain $P_g = P_{avg}$. Situations or events in which the load forecast is known to be higher than usual, these conditions should be overwritten through a Graphical User Interface (GUI). These situations may include holidays, planned events or week days in particular which from experience has higher demand. Seeing as this project is focusing on Simulink controls, it is implemented a pin connection for system overwriting so that the batteries can be fully charged before heavy load. The green box in figure 3.27b contains this pin, where user action can manually seize control over the desired amount of charged or discharged power, regardless of P_{avg}. The blue area in figure 3.27b enables either the charging bridge or the discharging bridge in the BDC converter, depending on whether equation 3.80 to 3.82 is fulfilled. This enabling signal is also used to activate the corresponding voltage, current and power control strategy respectively.

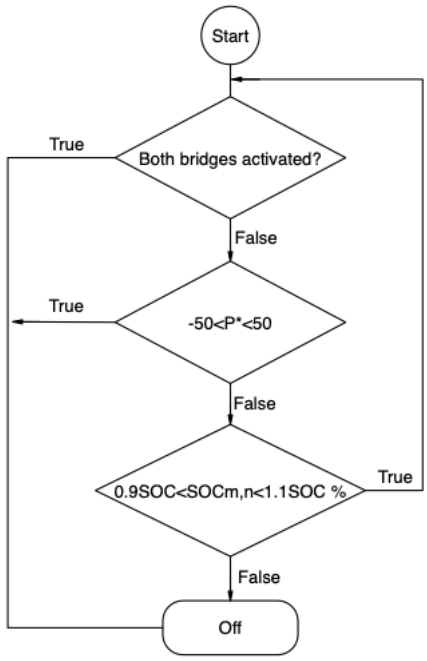
Having implemented this, there are several factors that may go astray. Figure 3.28a provides a flowchart of situations leading to a grid disconnection and BESS turn-off. This protection system is added for safety concerns, and to add stability, reliability and redundancy to the control system. These considerations include:

1. If the SOC levels are lower than the minimum threshold limit (35%) and the grid requires battery discharge duty, the BESS will turn off. Similarly, if the SOC is higher than the threshold (80%) and condition (1) in equation 3.80 is fulfilled, the BESS will automatically turn off. The red box in figure 3.28b represents this condition. This condition is also consistent with the second term mentioned in the section above, in which includes it in the flowchart of figure 3.27a

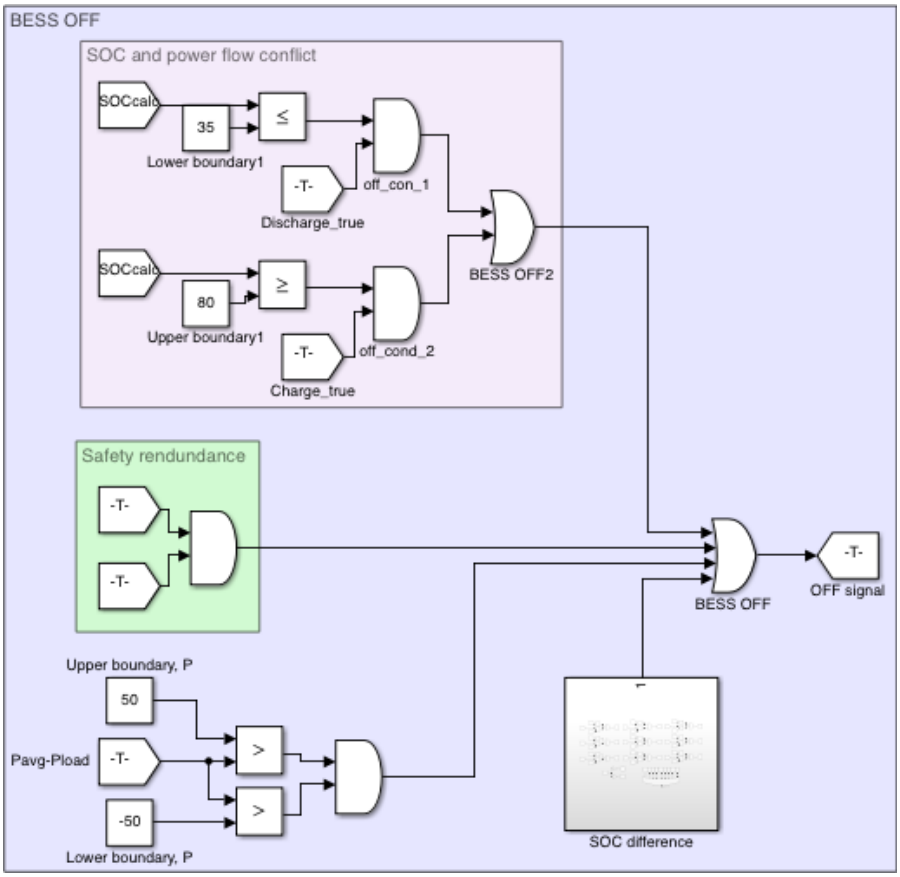
2. Situations in which the logic block diagram activates both bridges in the dc-dc converter should be avoided. This system is design so that this situation never will arise. However, such a situation may lead to a catastrophe since the control system loses current and voltage control. For that reason, a redundancy layer is added so that the BESS will turn off in this situation. The green box in figure 3.28b represents this condition.

3. In cases where $-50 < P^* < 50$, the BESS will turn off. These situation arises when the actual load is almost equal to the average. Due to small power fluctuations, the desired power may oscillate between positive and negative, which leads to an undesirable rapid switching between charging and discharging mode. Seeing as this will increase battery stress and contribute to more transients due to the system controllers, the BESS will turn off in such events. The logic in the blue area in figure 3.28b fulfills this condition

4. If one of the batteries contain a SOC that is between the threshold limits $SOC_{m,n} < 0.9SOC_{avg}$ or $SOC_{m,n} > 1.1SOC_{avg}$, the BESS will disconnect. Such a situation may imply faulty battery cell or other component failure which leads to a difference in SOC levels. Moreover, it leads to an unbalanced power distribution across the modules and phases. In either case, this is a BESS turn-off situation. This stage can be employed for both temperature and battery voltage control using the exact same design procedure. For that reason, only SOC unbalances are addressed. The subsystem "SOC difference" in figure 3.28b represents this condition. It consists of comparing all the individual module SOC with the upper and lower threshold values. If any of the nine comparisons break the condition, the output of the subsystem block is true, and the BESS turns off. The Simulink implementation for the SOC-difference logic is found in Appendix E



(a) Flowchart for PLS safety operation.



(b) System diagram.

Figure 3.28: BESS turn-off conditions.

3.7 Self healing strategy

Figure 3.29 shows an overview of the SH block diagram implemented in the control system. It is composed by logical gates and system I/Os. The control system during normal operation depends on measured values of grid voltage and current. However, if the grid supply disconnects, the control system requires a replacement of these parameters. The red box in figure 3.29 serves this purpose. It can be seen that the self healing logic is activated if the grid power is below $50W$ for a certain time period. The "threshold time limit" subsystem specifies this time limit, and can be adjusted depending on nominal grid parameters in which the BESS is implemented [20]. In this simulation, the minimum threshold time is set to 50 ms. The "restoring fictitious grid" subsystem consists of three digital sine wave generators with an amplitude of $230\sqrt{2}$, phase shifted 120°and a frequency of $50Hz$. Seeing as there is 50 ms delay from the time the grid drops until the self healing mode is activated, a new synchronization with respect to the new fictitious grid is needed. The phase angle used in Parks-transform is therefore changed in this subsystem respectively. When the utility restores, the SH-mode is deactivated in the red box in figure 3.29 because the grid power exceeds the minimum $50W$ SH-threshold. That means that the grid sets a new synchronization for the BESS PLL to tune in, and a new BESS-to-grid synchronization takes place.

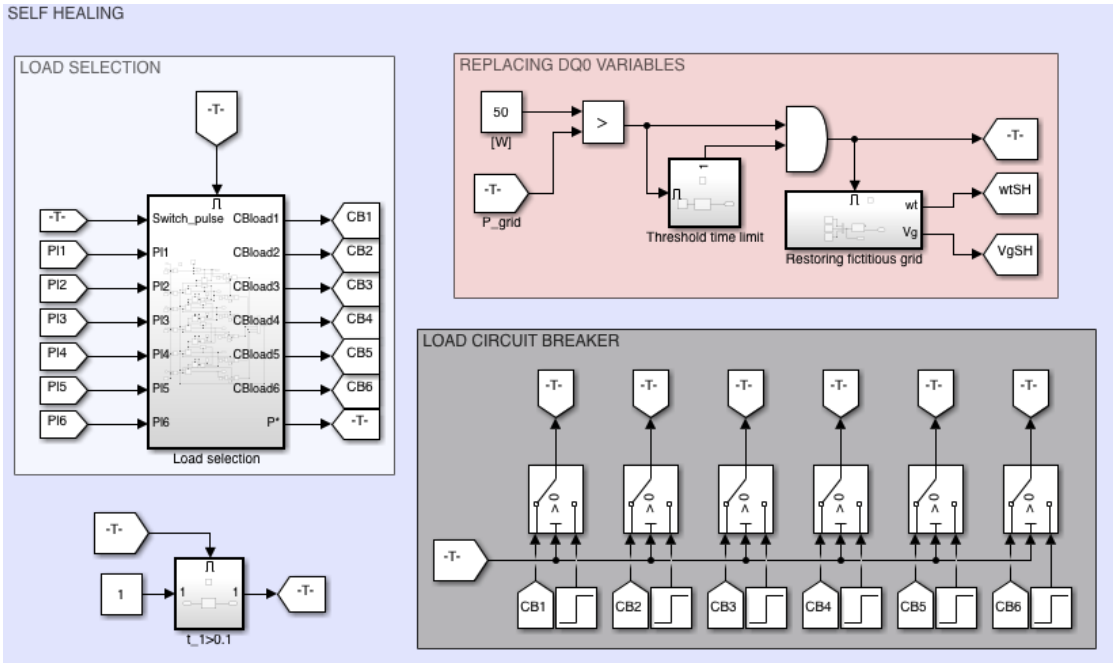


Figure 3.29: Overview of the implemented self healing control.

As mentioned in section 3.6, the desired power generated from PLS flowchart is overwritten by the "Load selection" subsystem inside the white box in figure 3.29 when self

healing is activated. This is necessary because the average grid power P_{avg} is no longer supplied by the utility. That means that the battery bank is designated to take over total power supply, which in most cases surpasses the designed power rating. Therefore, it is proposed a load selection diagram which is designed in this subsystem. The final SH-system design is valid for both mesh grids or line radials. Moreover, there may be several configurations of BESS to grid connections. Figure 2.7 from section 2.2 shows a one line diagram of a microgrid, which is a typical representation of a BESS-to-grid integration in a microgrid. This figure is expanded into figure 3.30, which is the system used for SH-mode testing. This figure is used as a flexible example of grid topologies in which this proposed SH-design can be implemented in, although the SH-logic can be applied on both radials and other mesh grid topologies. The initial assumption is that the grid power supply disrupts at an arbitrary point outside the microgrid, that is, between the power transformer and the bus in figure 3.30. Naturally, if a fault occurs within the microgrid, the CB and HV-protection relays in the corresponding substation will trip so that this particular feeder is disconnected from the rest of the microgrid.

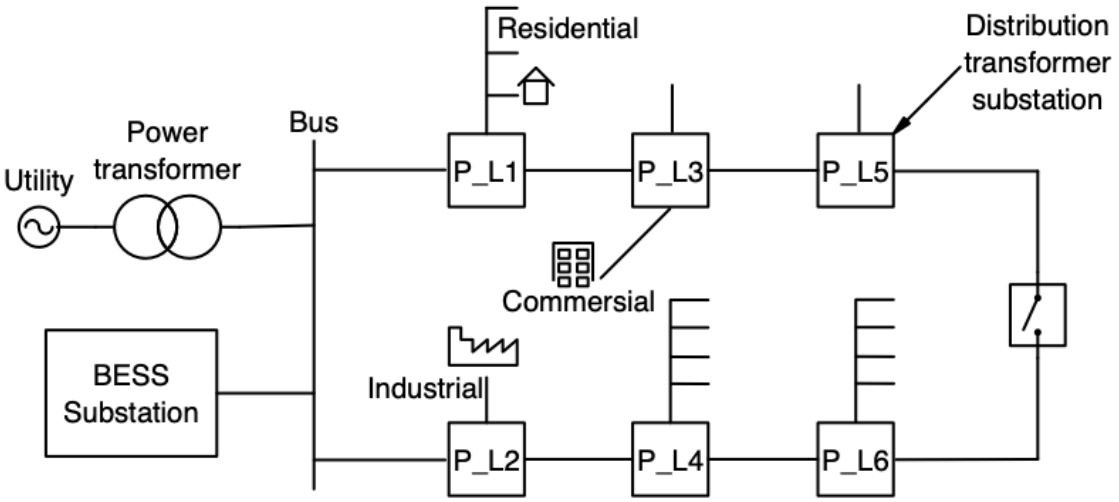


Figure 3.30: Example of grid topology in which the proposes SH-control system can be implemented in. SH-controls are tested based on this figure, using various values of $P_{L_1} - P_{L_6}$ in section 4.

Before a load is connected, the main condition checked is given by equation 3.83 as:

$$P_{L_1} < P_N - P_{activated} \tag{3.83}$$

where:

$$P_{activated} = \sum_{i=1}^{n} = P_{L_i} \tag{3.84}$$

The concept encircling this proposed method is that one load at the time is checked up with the condition in equation 3.83. If that condition is true, then the corresponding CB will reconnect. As this happens, $P_{activated}$ is iterated by the power connected to that CB, and the next load is allowed to be assessed by the condition presented in equation 3.83. This process will continue looping until every load that satisfies the main condition is connected. In the event that one load is to large so that the main condition is false, the control logic still needs to check if other loads can be connected. For this to happen, it has been added a block that activates the next load investigation action regardless of the previous load turned out false. In order to check one load at the time, a time delay of 100 ms has been added in between checking terms. The reason this is needed are two-folded: (1) if every load is compared with the main condition simultaneously, then every load will first be connected before a rapid disconnection, and (2) connection of a load should be conducted during system steady state operation, as a premature load re-connection will interrupt with the system stability. The first consequence mentioned, will repeat in a oscillatory fashion and is characterized as greatly undesirable. The second is important for the transient stability of the system. 100 ms is chosen due to the time constant of the current controller. In section 4, response details will be provided to justify this time delay.

Figure 3.31 shows the proposed flowchart for n loads on the BESS side of the feeder in figure 3.31. The flowchart has been simulated for six substations with different loads connected. The "Load selection" subsystem within the white box in figure 3.29 can therefore be expanded into figure F.1 in appendix F. The black box is constructed so that PLS may be simulated during nominal grid supply. The CB signals are pre-adjusted through the step blocks within this box. If at any point the grid drops to zero, then the pulse activating the self healing controls also serves to give CB control to the load selection system. The last function for the self healing logic diagram is provided in the blue area of figure 3.29. It is meant to delay the actual power drawn by the grid past the transient phase so that the desired active power discharge may be generated based on steady state values. In the delay period, the desired discharged power is represented by a constant, given by the amount of power that was previously connected to the substation.

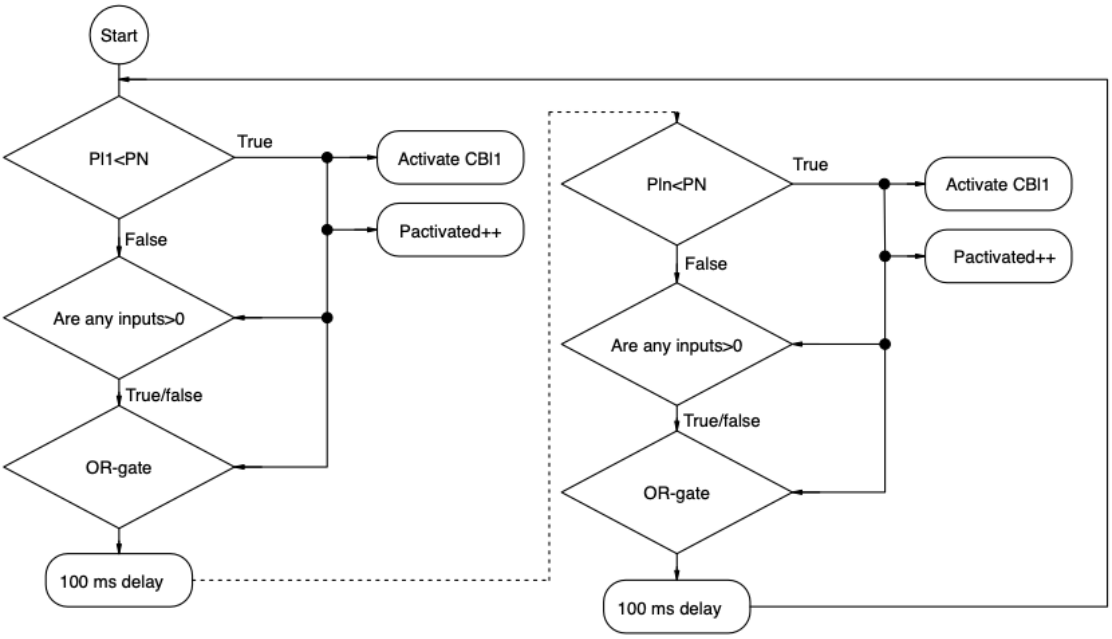


Figure 3.31: SH flowchart for load selection from first to n^{th} load.

After the load selection logic has searched through all the loads, the SH-logic enters a load preservation mode. This is needed in order to account for critical loads L_{crit} in which may break the load selection criteria after CB trip. In detail, the reason is that the load selection chart is based upon the assumption given in equation 3.83. However, this may only be valid during the load selection phase, because if a load is considered suppliable by the BESS search algorithm, the corresponding CB will trip, leading to an increment in the total $P_{activated}$. Without load preservation controls, the load selection will find that the re-connection of the first critical load $P_{L_{crit}}$ breaks the condition $P_N - P_{activated} - P_{L_{crit}} > 0$. The proposed solution to this issue is represented in figure 3.32. Here, whenever the load selection trips a circuit breaker, the SH-criteria presented in equation 3.83 is modified so that $P_{L_n} = 0$.

Figure 3.32: Boolean feedback to switch. If the load is reconnected, the output of the "SH-criteria" is true, which trips the switch to zero.

This means that whenever the load selection has reconnected a load, it naturally never considers to reconnect it again. This arrangement however, induces required measures in order to account for variable load. Two main steps are considered:

1. If a load increases so that the total power output of the BESS surpasses its rating.
2. If a load decreases in favour of another loads.

The first step is critical in nature, in which has been resolved by reactivating the load selection process. The second step is more useful from a self healing perspective. If the demand of a load that already has been reconnected decreases, then other loads which has been disregarded earlier by the load selection controls may be reconnected. However, in order to avoid oscillating CB trip, the desired power output of the BESS cannot surpass 4800W. The reason is that the desired power output is a constant provided by the SH-logic, while the actual power feedback may fluctuate. An example of this is provided in section 4.6.

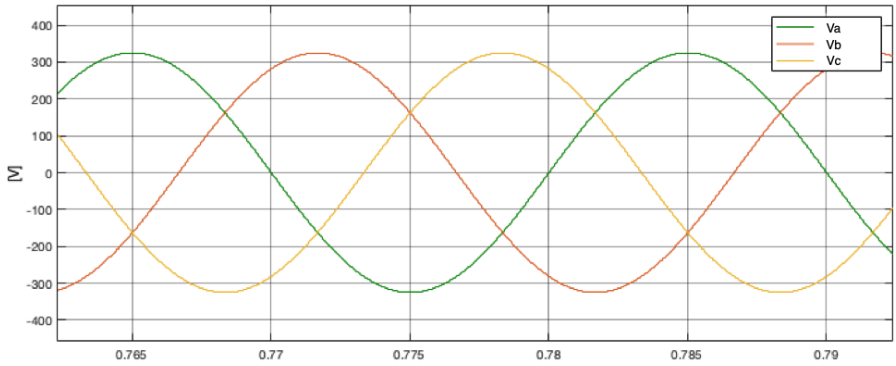
4 Results

This chapter contains simulation results of the proposed design. The author has utilized Matlab solver ode23t for its capability of solving singular mass matrixes (differential-algebraic equations) [102]. Discrete simulation settings are used where the sampling frequency must be manually settled. Having $f_{s,BDC}$ to be the largest system frequency, the minimum sampling frequency Simulink requires is $2 \cdot 20kHz$ since there are two cycles per wavelength [101]. By adding some margin for best possible accuracy, the sampling time inserted into the Simulink model was $10\mu s$.

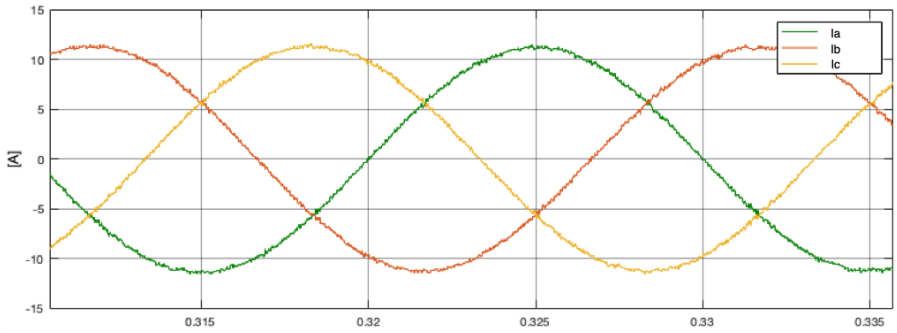
4.1 Power quality assessment

The power quality provided by the designed BESS can be illustrated by the output waveform distortion. Figure 4.1 is indicating that the output waveform distortion is generated by the currents alone. However, the grid power quality is dependant on the voltage quality, since the grid has no specific control over the individual currents that is drawn by each load [16]. Figure 4.1a shows the voltage measured at the output node of the BESS. It is equal to the grid voltage generator implemented in Simulink and remains unchanged for both buck and boost mode. However, seeing as the power control implemented in the BESS is controlling the output currents, the power quality is directly proportional to the periodic distortion of the output current sine wave. Figure 4.1b and 4.1c is showing the input and output current respectively. It should be noted that the magnitude of the currents at $10.25A$ at $5kW$ is consistent with the results in equation 3.8.

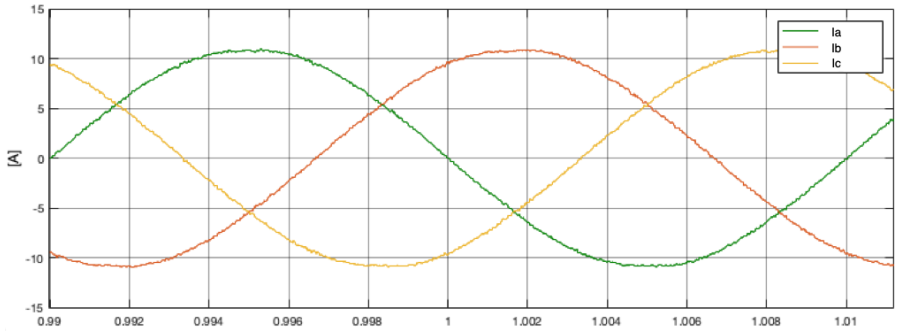
In buck mode, as shown in figure 4.1b, the charging current contains visibly more harmonics than in boost mode. This can be explained through the outer loop voltage controller and the voltage balancing controllers, which will receive more attention in section 4.3. In order to assess the THD of the currents in figure 4.1, a Fast Fourier Transform (FFT) analysis provided by internal tools in Simulink has been conducted. The results given in figure 4.2 shows the THD for $5kW$ charge and discharge currents of the BESS.



(a) Measured voltage at BESS output.

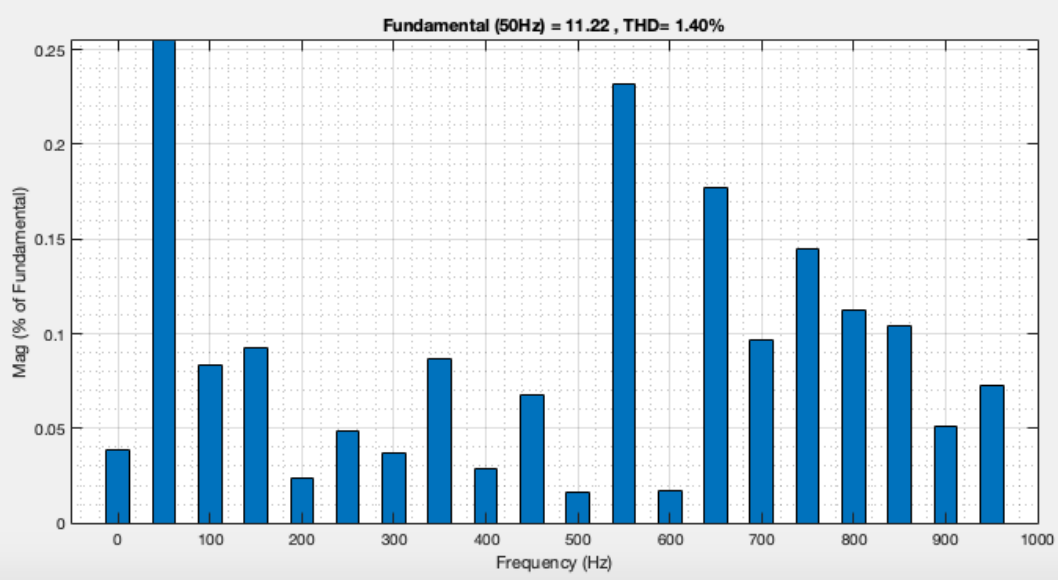


(b) Measured grid charging current at $5kW$.

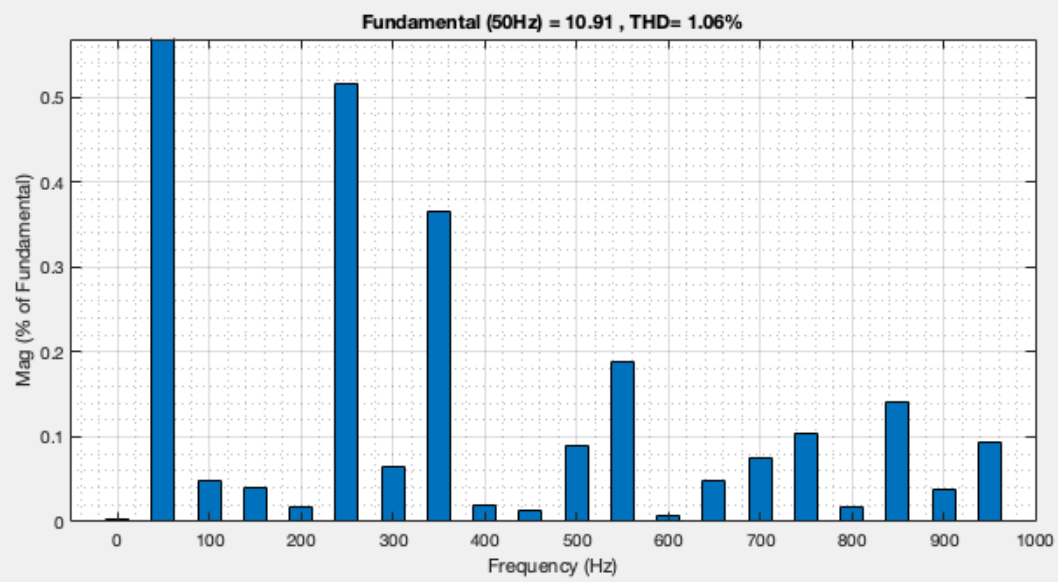


(c) Measured grid discharging current at $5kW$.

Figure 4.1: BESS current and voltage measured at the grid-side of the output L-filter.



(a) $1kHz$ spectrum for charging current.

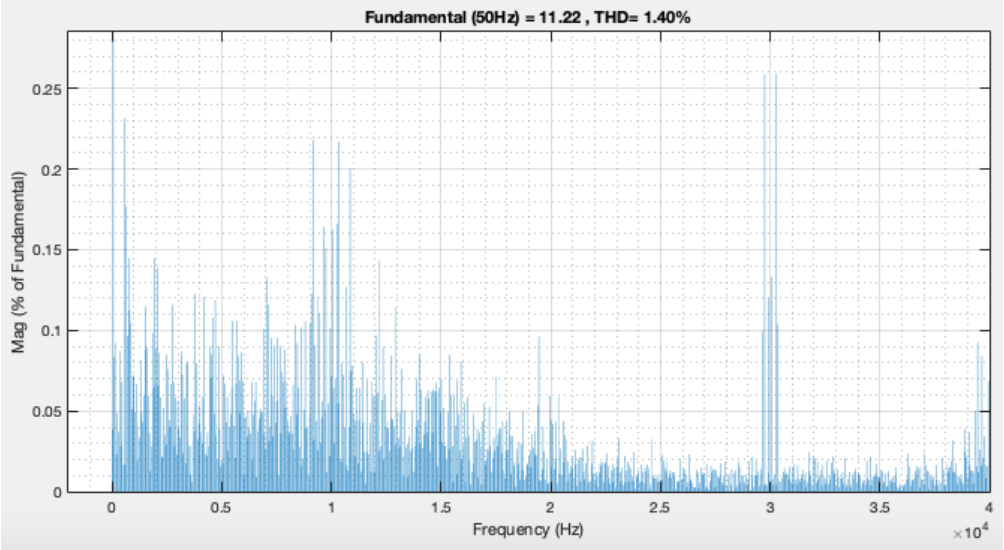


(b) $1kHz$ spectrum for discharging current.

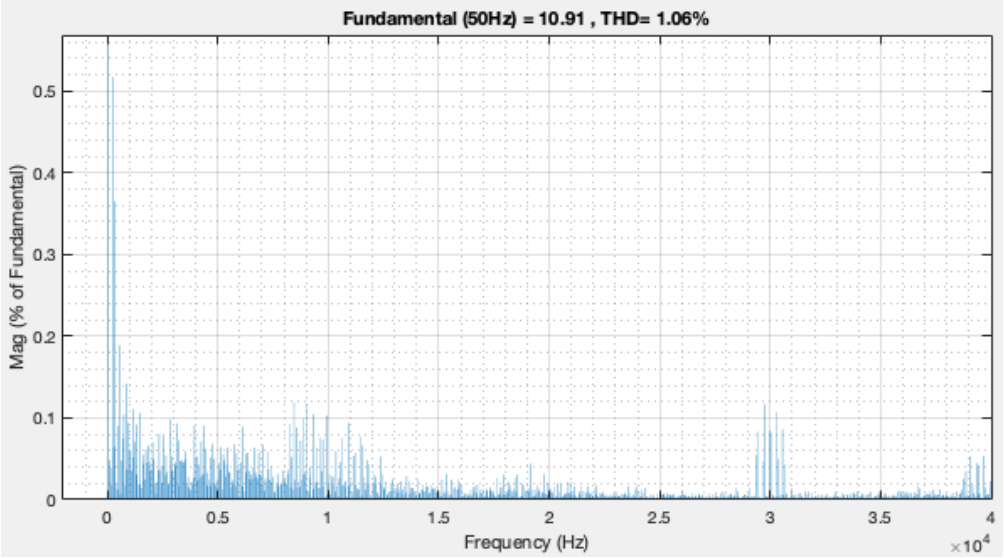
Figure 4.2: Current frequency spectrum providing THD using FFT analysis. Both output and input currents represent $5kW$.

For voltages below $1kV$, the maximum individual harmonic is 5 %. Correspondingly, the THD should not surpass 8 % [28]. As figure 4.2 shows, the THD for both power directions are comfortably within these limits. Figure 4.2a shows a total harmonic distortion of 1.40 %, while figure 4.2b shows a THD of 1.06 % for discharge. The discharging

THD is slightly lower than the charging current, as depicted in figure 4.1. Additionally, figure 4.3 is included to demonstrate the harmonic shift towards higher frequencies for CHB-converters, as mentioned in section 3.1. Figure 4.3a and 4.3b shows the harmonic tendency at $40kHz$, in which illustrates that harmonics has been shifted towards $30kHz$, which is consistent with the calculation provided in section 3.1.



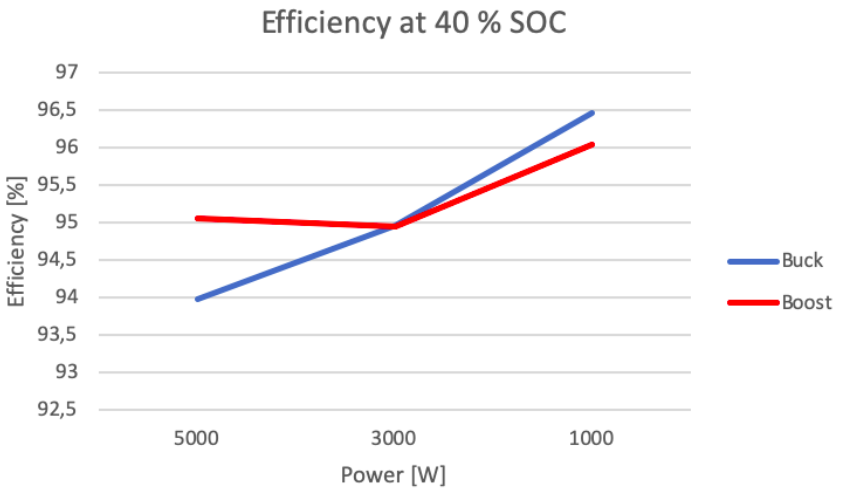
(a) $40kHz$ spectrum for charging current.



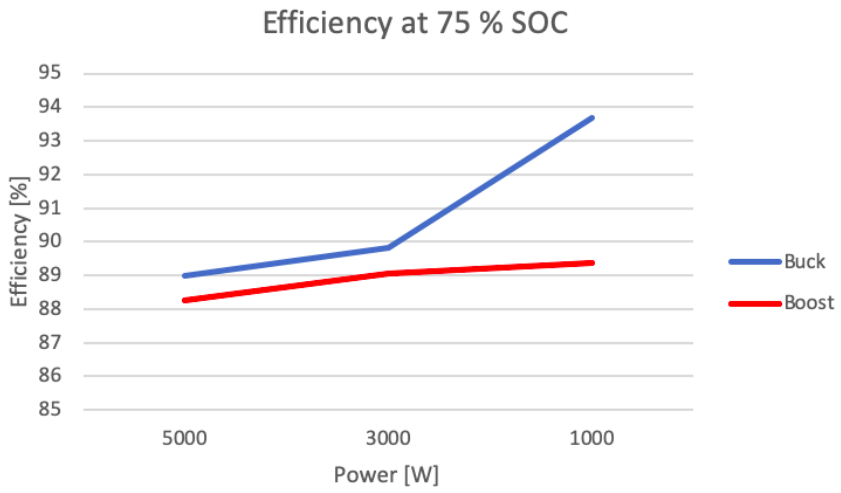
(b) $40kHz$ spectrum for discharging current.

Figure 4.3: $40kHz$ frequency spectrum of the output currents. Both output and input currents represent $5kW$.

The designed PCS is validated by the overall system efficiency. Figure 4.4 shows the efficiency plot from the BESS output to the power supplied by the nine batteries (boost), and during charge (buck). The batteries SOC levels were preset at $\pm 5\%$ from the upper and lower SOC-thresholds of 35% and 80%. This is shown in figure 4.4a and 4.4b respectively. The general assessment is that buck mode of operation results in a high efficiency. Boost mode, although quite high, transfers power with a slight reduction in efficiency levels. As load decreases, the efficiency levels for all modes increases.



(a) Results at 40 % SOC.



(b) Results at 75 % SOC.

Figure 4.4: Efficiency charts for the proposed model using $5kW$, $3kW$ and $1kW$ power respectively.

Additionally, there is considerations that must be made regarding start-up procedures. This may include a starting resistor across the BESS output filter in which suppresses the disturbances delivered by the converter in the initial transient phase of grid connection. Additionally, the inrush currents in the filtering components on the dc-side are quite substantial in the start-up phase, seeing as they are close to being short-circuited in the instantaneous start-up phase. Here, the inrush currents from each battery reaches magnitudes of above $1kA$. In practice, this can be solved by pre-charging the converter filters [86]. The latter start-up method has been implemented into this model, although a starting resistor in parallel with the output filter should be considered in practice. Figure 4.5 shows the improved battery inrush current when the dc-link capacitor is pre-charged to $108\,V$, battery side capacitor to $65\,V$ and the inductance filter to $100\,mA$ in the positive direction towards the battery. In a physical system, an additional control system should be added to measure the nine batteries SOC-levels in order to correctly pre-charge the individual capacitors before activation.

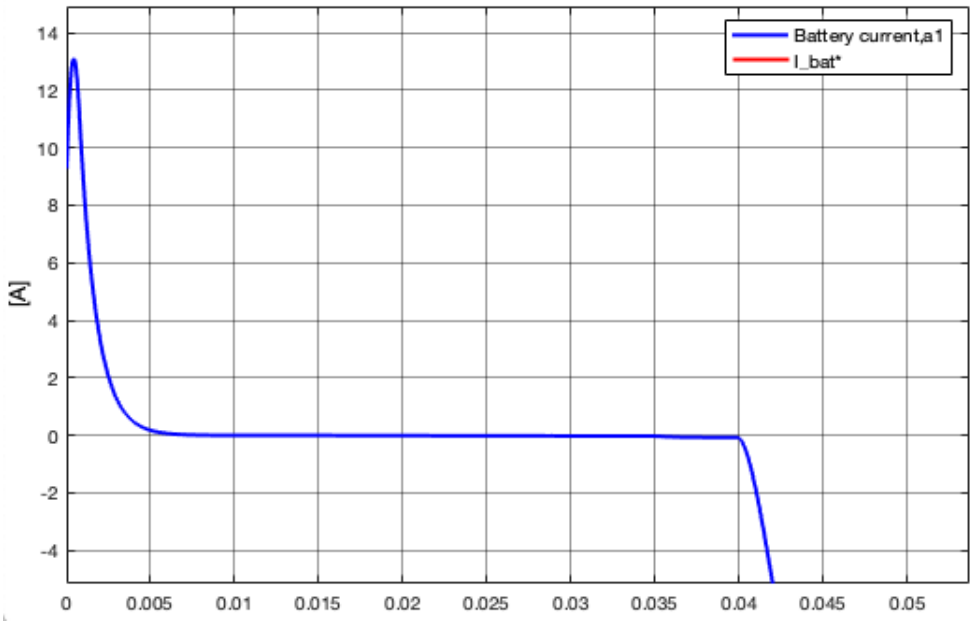


Figure 4.5: Optimized pre-charging of filter components in order to reduce the input surge current.

4.2 Analysis of active power response

The dq-current reference is generated from two separate systems, depending on charge or discharge power flow. As explained in chapter 3, i_d^* is generated through the voltage controller, shown in the left hand side box in figure 4.6. The voltage regulator should be disconnected from the control system during discharge, because of windup issues

when the desired current shifts 180°. When the desired power turns negative, the switch between the two systems in figure 4.6 is activated so that i_d^* can be generated by:

$$i_d^* = \frac{P^*}{V_{gd}\sqrt{2}} \tag{4.1}$$

As explained in section 3.3.1, the converter gain of $\sqrt{2}$ needs to be accounted for. This gain has been included so that equation 3.20 is modified to equation 4.1. Moreover, the desired active power is different during self healing circumstances. Whenever SH is necessary, the switch within the blue box on the right side of figure 4.6 activates, using a new P^*, described in section 3.7.

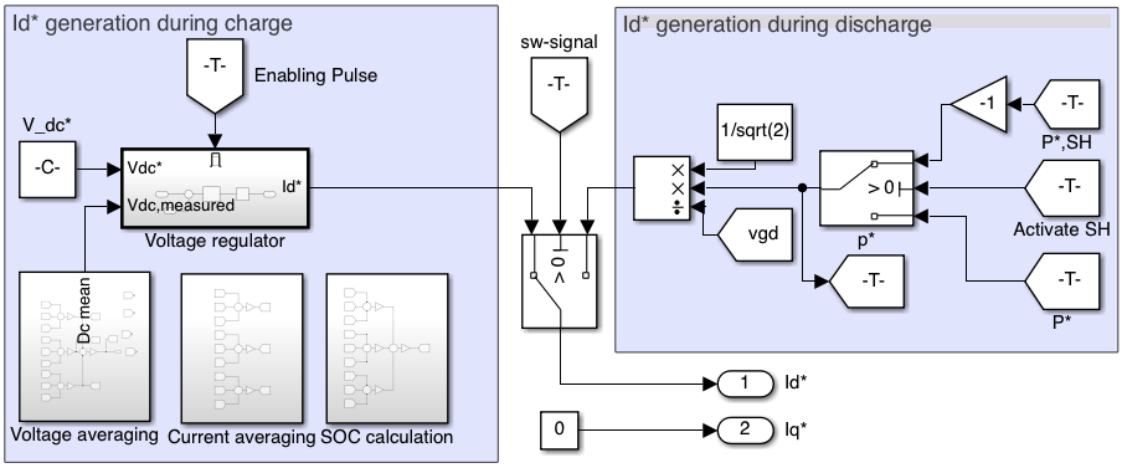
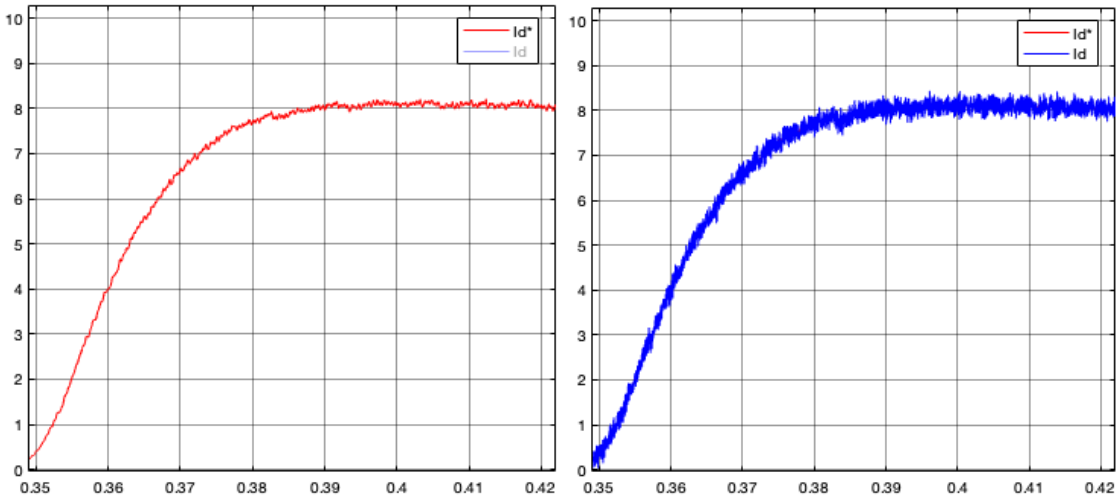


Figure 4.6: Signal diagram of the generated dq control currents.

The receiving end of the output signals generated in figure 4.6 is the inner loop current controllers. Figure 4.7 shows the reference tracking of the d-axis current controller to a $3.5kW$ charging signal. Seeing as charging mode is activated, the reference value is generated by the outer loop voltage controller, shown in figure 4.7a. Figure 4.7b shows the d-axis controller response.

However, when the current controllers are independent from the outer loop voltage controllers, the step response is found in figure 4.8. Here, the referenced power is set to $P^* = -5kW$ discharge. It can be seen that the controller has a 5 ms response time with a somewhat long "tail". The controller settles at 30-35 ms. This should be the fastest controller in the current control loop, making 5 ms the reference when tuning both the outer loop voltage controller and the capacitor balancing controllers. The overshoot is $OS|_{\%,max} = 15.3\%$.



(a) i_d^*. (b) i_d.

Figure 4.7: Reference tracking of PI_d current controller.

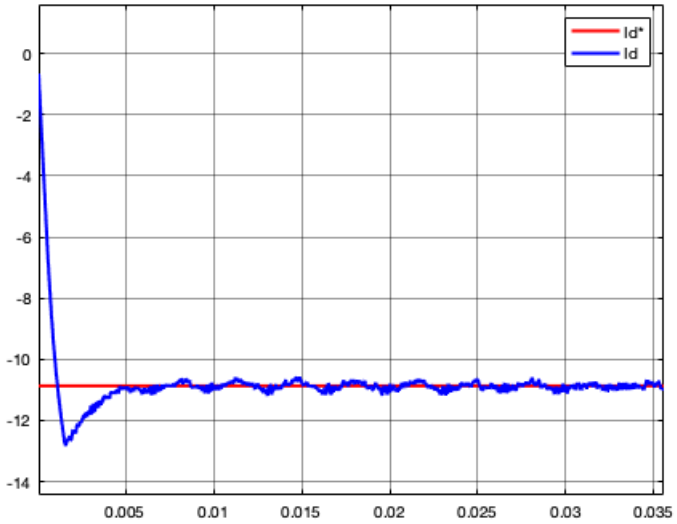


Figure 4.8: Step response for PI_d current controller using $5kW$ load.

4.3 Analysis of BDAC voltage control

Figure 4.9 shows the voltage controller response from the primary transformer winding voltage of $108.42V$ to $108.42\sqrt{2}$ presented in equation 3.6. Module a_1 is used as an example. It is designed so that the $OS|_{\%,max} = 0$ because an overshoot will directly affect the power drawn by the BDAC converter, as shown in figure 4.10. Settling time is reached after 170 ms which is significantly slower than the current controllers, as re-

quired. However, tuning the controller to be faster will lead to an undesirable overshoot in the dc link voltage, and thus the power waveform. Having no load as shown before 300 ms, the voltage tracks the exact reference value. After 300 ms in figure 4.9, the BDC converter converts power from the dc link to the battery, where the voltage ripple starts. It should be noted that the dc link voltage balancing controllers are disconnected in figure 4.9 in order to emphasize the outer loop voltage controller response.

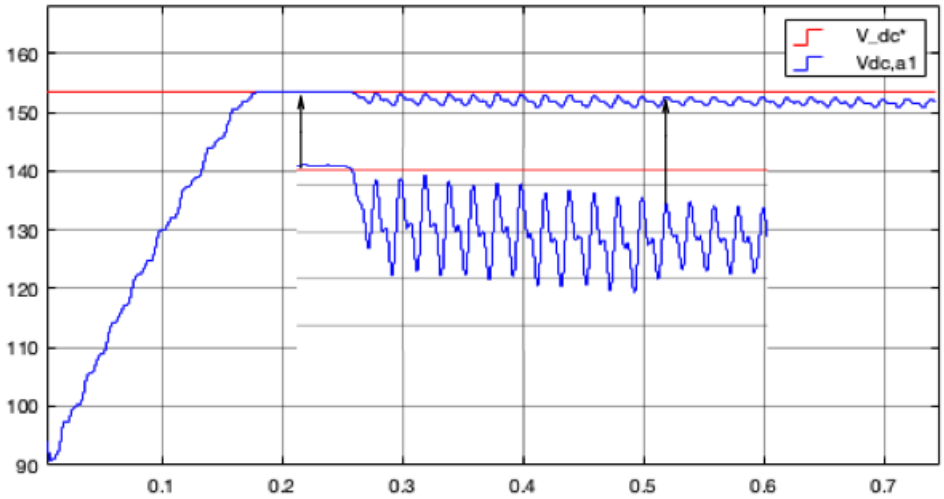


Figure 4.9: Voltage controller step response from $108.42V$ to $108.42\sqrt{2}$.

Figure 4.10 is included to illustrate the voltage controllers in terms of the power converted in the BDAC stage. At 250 ms, the BDC converter charges the battery with $5kW$. The voltage controller increases the power from $0-5kW$ in 60 ms. Additionally, at 0.5 seconds, the power is changed to $3.5kW$ in order to illustrate the response to a change in load. As can be seen in figure 4.9, the change in load has no effect on the dc-link voltage other than a small reduction in the voltage ripple. As explained in section 3.1.3, this ripple should be kept below 1 %. Additionally, the larges voltage ripple is found while charging at $5kW$. Using this arrangement without balancing controllers, the dc link voltage ripple is approximately 2.03 at maximum load which is above the maximum limit of $\Delta V_{dc} < 1.53V$.

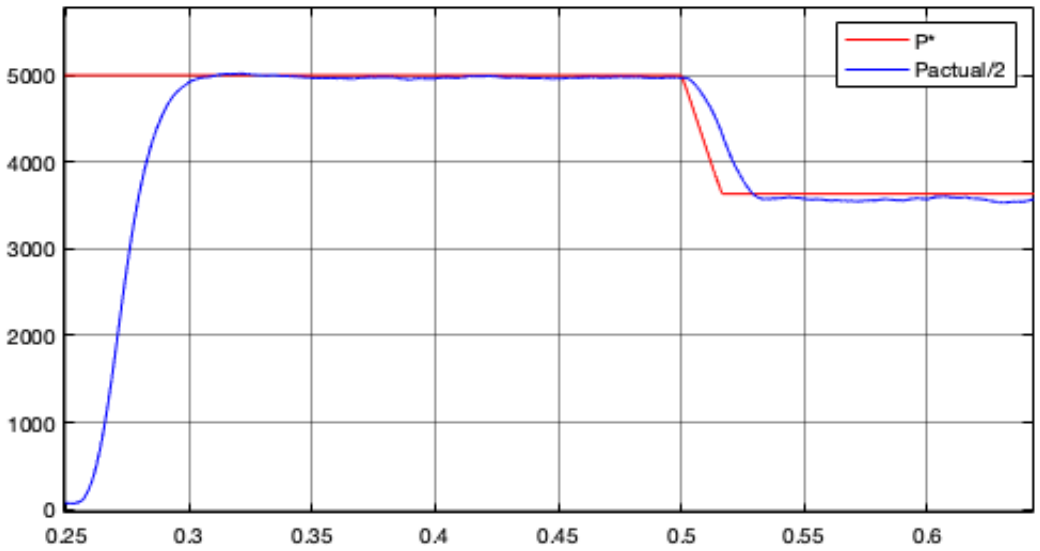
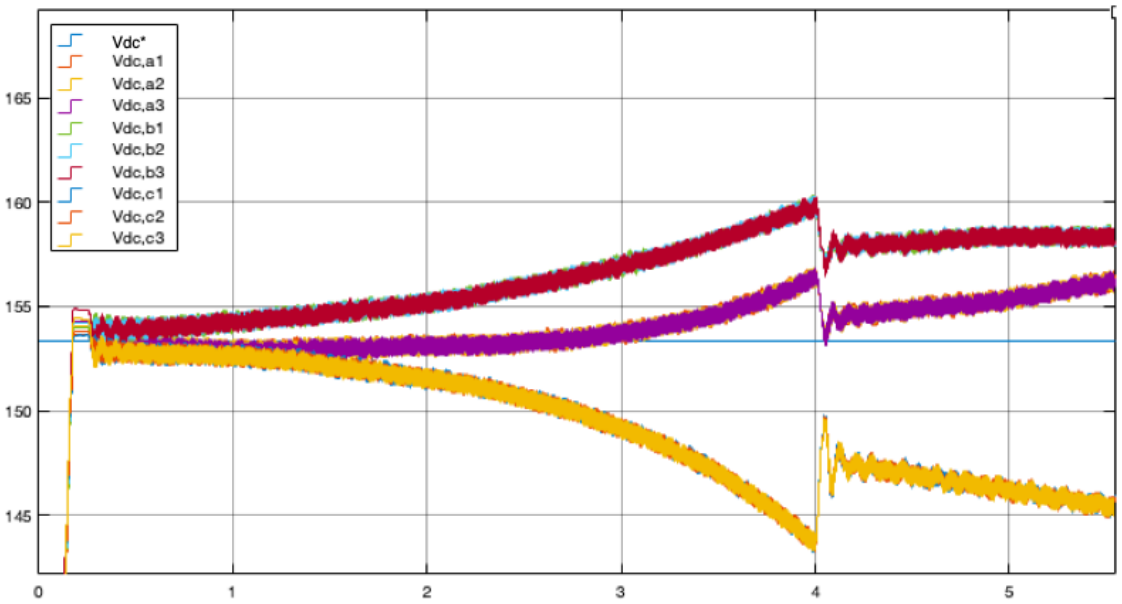
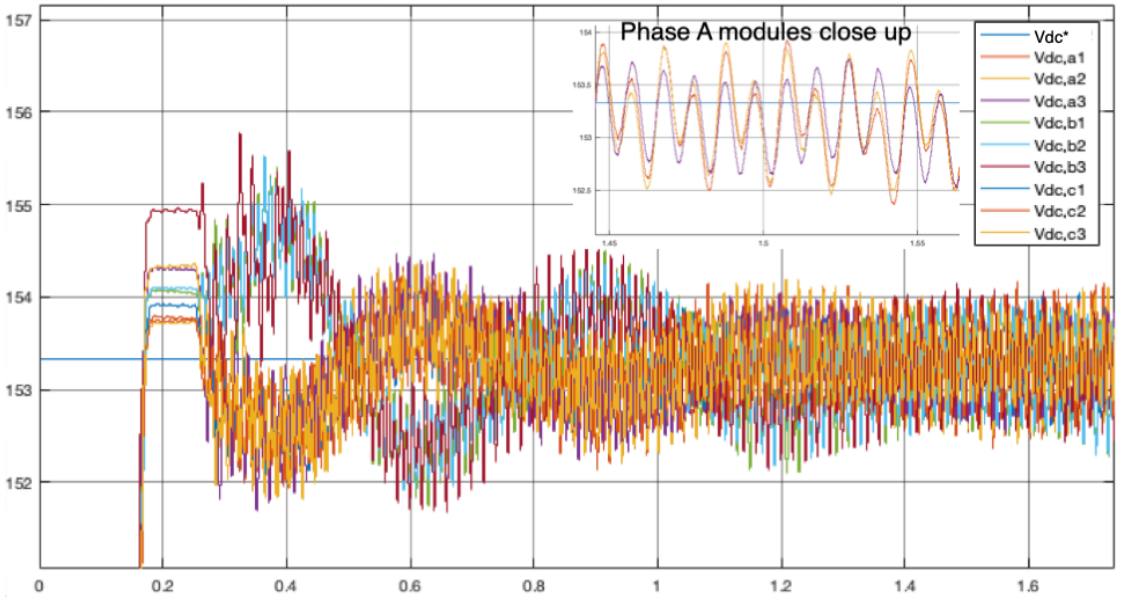


Figure 4.10: Power step response from $5kW$ to $3.5kW$ charging power.

Figure 4.11 shows a comparison between an uncontrolled dc link voltage and controlled using the balancing controllers designed in section 3.3.3. Figure 4.11a illustrates how the nine module dc voltages deviates from the reference value. Although each module corresponds with its respective phase, the phases becomes increasingly more unbalanced. This can lead to instability if the voltage deviation gets too large, as shown after approximately four seconds in figure 4.11a. The voltage balancing controllers are designed so that the module voltages are balanced, both with respect to the corresponding phase modules, and the other phases. Connecting them has additionally improved the dc link voltage ripple, as can be seen from figure 4.11b. The close up shows that the voltage ripple has been reduced to $\Delta V_{dc} \approx 1.4$. There may be several factors that influences this ripple. However, seeing as the ripple period is at 10 ms which corresponds to a ripple frequency of $100Hz$, it proves that it originates from the grid side power fluctuations [38]. It is present in both the battery side inductor filter and the dc link capacitor. The phenomenon is practically inevitable, although it can be shifted between the inductor as current ripple, or the capacitor as voltage ripple by proper filter tuning [37]. The controllers have been tuned to reach settling time at approximately 175 ms, which is marginally slower than the outer loop voltage controller. The tuned overshoot is estimated to be 21 %, although figure 4.11b shows a notably lower simulation result of $OS|_{\%,max} \approx 1\%$.



(a) Uncontrolled dc link voltage as a result of disconnected balancing controllers

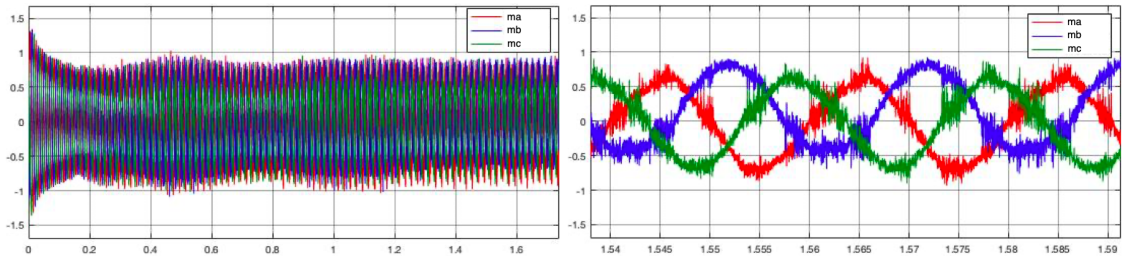


(b) Balanced dc link voltage as a result of connected balancing controllers.

Figure 4.11: Dc link voltage with dc link voltage balancing controllers both connected and disconnected.

The output of the outer voltage control loop is the modulating signal used in PS-PWM. In simulink this is the output of the inner current control loops as shown in figure 3.11 in section 3.2. Figure 4.12 shows the modulating signal for a $5kW$ charging power when

the voltage balancing controls are activated. Figure 4.12a illustrates that the modulating signal is in the linear region, $M < 1$, for max rated power after voltage balancing correction. Figure 4.12b shows a close-up extracted from an arbitrarily point in 4.12a. It indicates control signal noise due to semiconductor switching and voltage balancing corrections. Moreover, during startup, the modulation index starts above 1. Startup procedures such as a starting resistor or pre-charge of filter elements can be implemented in order to reach a soft-start state. Both these issues were addressed in section 4.1. The peak difference is a consequence of the voltage balancing corrections inflicted upon M.

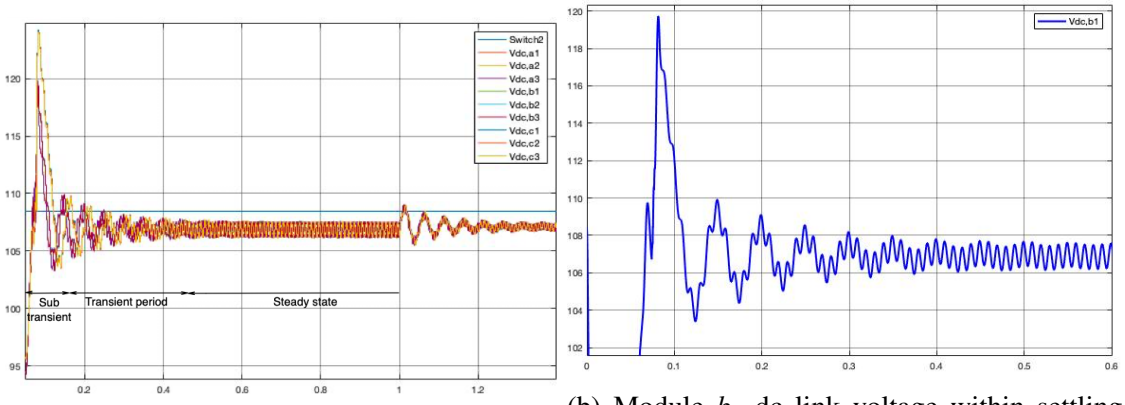


(a) Overview of the modulation index in the interval $-1 < m < 1$.

(b) Modulation index at an arbitrary time period shows balancing corrections.

Figure 4.12: Maximum modulation index balancing correction during $5kW$ charging power. Power output is balanced due to the influence of the balancing controllers.

4.4 BDC control



(a) Dc link voltage nine modules.

(b) Module b_1 dc link voltage within settling time interval.

Figure 4.13: Dc link voltage controlled by the BDC converter.

During discharge, the dc link voltage reference is at $\hat{V}_g/3 = 108.42V$. This is controlled by the boost converter. Figure 4.13 shows the dc link voltage at $5kW$ between $0 < t < 2$

seconds. The discharging power is reduced to $2.5kW$ after two seconds, in which illustrates that the dc link voltage ripple is reduced during lighter loads. Figure 4.13a shows all nine module dc link voltages in which is balanced and stable in steady state. However, the sub-transient and transient periods as shown in figure 4.13b is quite high, lasting for approximately 80 ms and 600 ms respectively. The controller tuning of the transfer function extracted in section 3.4 has been optimized so that the transient stability has been somewhat increased. Nevertheless, this under-damped characterization of the response has proven itself difficult to calibrate by controller tuning. Additionally, there is a steady state error present of approximately $1.4V$ corresponding to 1.31 %. There may be several reasons for this such as modelling imperfections or excessive simplifications. In order to investigate this, the presumed steady state error e_{ss} from the transfer function $G_{BDC,boost}(s)$ can be calculated. The input to the voltage controller is a step input, so that e_{ss} is given by [46]:

$$e_{ss} = \frac{A}{1+K_p} \tag{4.2}$$

Where:

$$K_p = \lim_{s\to 0} G_{BDC,boost}(s) \tag{4.3}$$

Recall that $G_{BDC,boost}(s)$ was derived in section 3.4, given by equation 3.78. A is the magnitude of the unit step input. Note that the dc link voltage reference is a constant, which only is changed if the power flow direction is. This means that in all cases, the step input for the BDC voltage controller is the absolute value of $|108.42 - 108.42\sqrt{2}| = 44.91$. K_p is therefore:

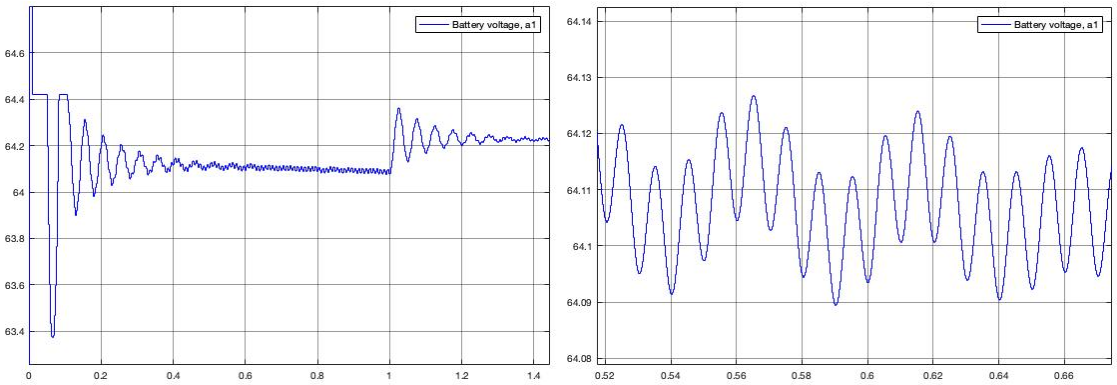
$$K_p = \lim_{s\to 0} \frac{0 + RV_c(2-2d)}{0+0+R(4d^2-8d+4)} = V_c = 108.42 \tag{4.4}$$

The value for the duty ratio $d = 0.5$ has been inserted into equation 4.4, while R gets cancelled. Substituting K_p into equation 4.2 results in:

$$e_{ss} = \frac{44.91}{1+108.42} = 0.914\% \tag{4.5}$$

Comparing this with the actual steady state error of 1.31 %, the difference may be explained through neglected semiconductors and transformers treated as ideal. The maximum voltage ripple during steady state operation is found to be $1.3V$ which is just above the boundary of the maximum ac component of $1.08V$. At half the rated power on the other hand, the voltage ripple magnitude is approximately $0.7V$, or 0.65 % compared to 1.25 % at rated load. However, the ripples of significance are across the battery side capacitor. A large voltage ripple here implies a large ripple across the battery nodes. Although it contains the same under-damped characterization, it is considerably smaller

compared to the dc-link, as shown in figure 4.14. Figure 4.14a shows the BESS discharging $5kW$, until it is changed to $2.5kW$ at 1 second. Figure 4.14b shows a close-up on the battery voltage during rated power discharge. The $100Hz$ voltage ripple has been reduced to $24mV$, which is excellent considering battery lifetime. Additionally, there is a small fluctuation pulsating at $20Hz$ in steady state operation. This ripples at $37mV$ peak to peak, leading to a total $\Delta V_{bat}|_{ptp} = 0.058\%$ of the battery voltage. Boost mode controller is tuned to an overshoot of 13.5 %, reaching settling time at 12.5 ms. The theoretical simulation, however, shows a moderate deviation from this. Controller tuning of $G_{BDC,boost}(s)$ results in an unstable system in most cases. Utilizing a PID controller for this system did resolve this, although with deviating results. This is further discussed in chapter 5.



(a) Module a_1 battery voltage.

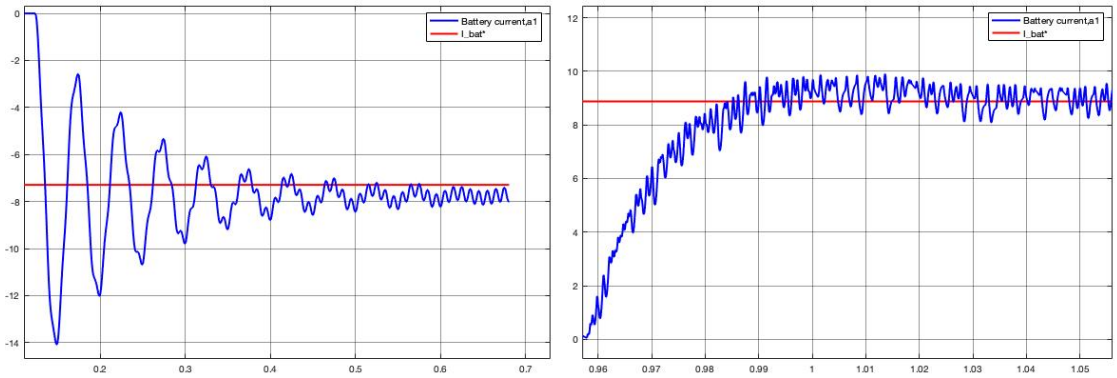
(b) Steady state close up at $5kW$.

Figure 4.14: Module a_1 battery voltage for $5kW$ to $2.5kW$ discharging.

Similarly as the voltage ripple, the battery current should be without a ripple ac component. However, the voltage ripple dictates the current ripple. That leads to a larger stern of the voltage ripple requirement than the current [22]. Figure 4.15 shows the battery current at both charge and discharge. In boost mode, the BDC converter controls the dc link voltage, resulting in a battery current shown in figure 4.15a. It illustrates that the dc link ripple and steady state error is reflected in the battery current. In steady state, this ripple is approximately 12.2% for rated power, which is a good margin below 20 %.

As for buck mode, the BDC converter is controlling the battery current directly, depending on the desired charging power. Figure 4.15b shows the step response from zero to rated power. The controller damping is just below one, resulting in a significantly better transient response than during boost mode. However, higher frequency harmonics and switching noise takes presence compared to the boost mode current. Additionally, the current ripple is slightly higher than the discharging current, peaking at 13.3 %. The controller is tuned at 0% OS at 25.6 ms. T_s from zero to rated is approximately twice

that, as shown in figure 4.15b.



(a) Battery discharging current at $4kW$. (b) Battery charging current at $5kW$.

Figure 4.15: Module a_1 battery current for a $5kW$ charge and discharge current at $4kW$.

Figure 4.16 shows the transition between figure 4.15a and figure 4.15b. This is included to illustrate the drawbacks of an unequal dc-link voltage. The consequence is that while the outer loop voltage regulator increases the dc-link voltage, it outputs a higher i_d^* than rated. Saturation limit corresponding to rated power has therefore been implemented in the voltage controllers. The issue during the voltage build-up period, is that the synchronization between the BDAC and BDC converter is lost. Hence, the BDC converter does not transfer current to or from the batteries. The BDAC converter on the other hand is bypassing power, all in which gets dissipated in the power stage components. When the dc link reaches the desired value, the voltage controller outputs close to zero due to the absence of BDC power transfer. This time period allows for converter synchronization, which has a response time of approximately 110 ms. The total delay period T_{delay} indicated by the reference deviation in figure 4.16, is in the region of 250 ms. Naturally, this is an undesirable feature which has induced further debate in chapter 5. It should be noted that since the desired current is depending on the measured utility power, the current reference marked with the red line in figure 4.16 dips due to the voltage regulator influence towards the grid power dynamic.

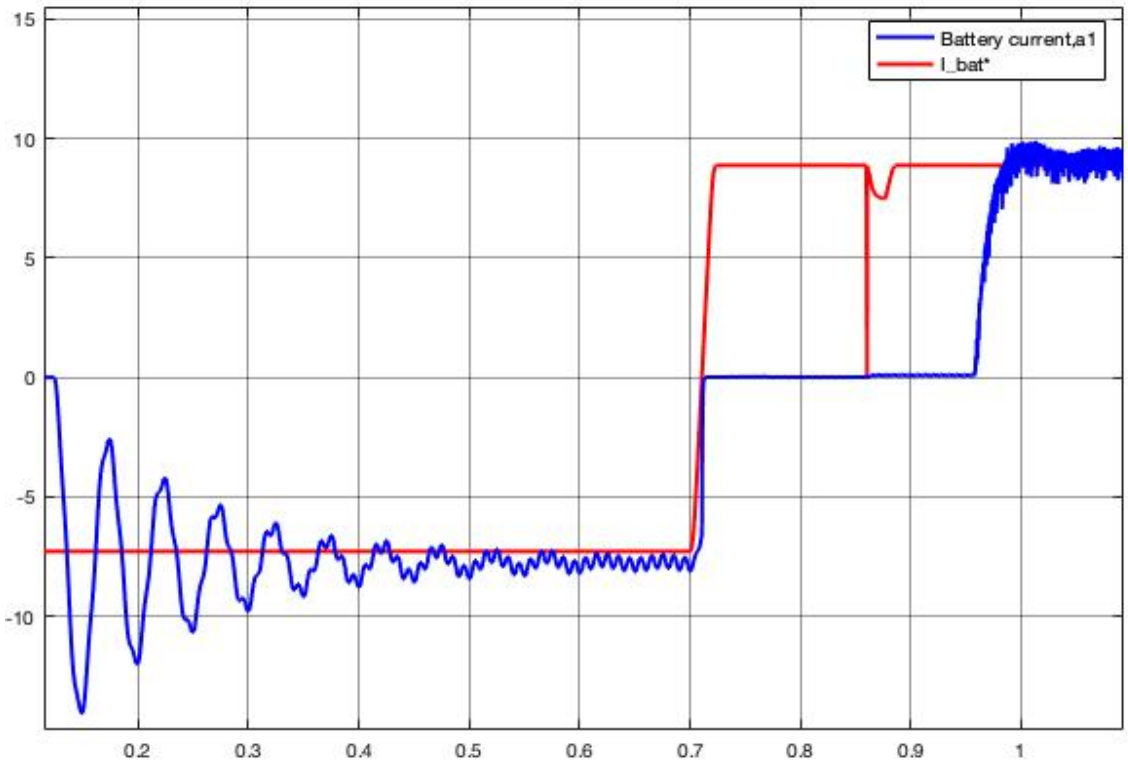


Figure 4.16: Battery current during the transition from discharging-mode to charging-mode.

Figure 4.17 is included to demonstrate the BDC converter current response when the dc link has reached its steady state value. It represents a fragment of the desired and actual battery current during PLS-simulation. Here, the corresponding load from $t_1 = 1.75s$ to $t_2 = 2.03s$ is $5kW$ charge, while $t_2 - t_3$ and $t_3 - t_4$ are $3.3kW$ and $0.75kW$ respectively. It shows a fast dynamic response compared with the start-up transition presented in figure 4.16

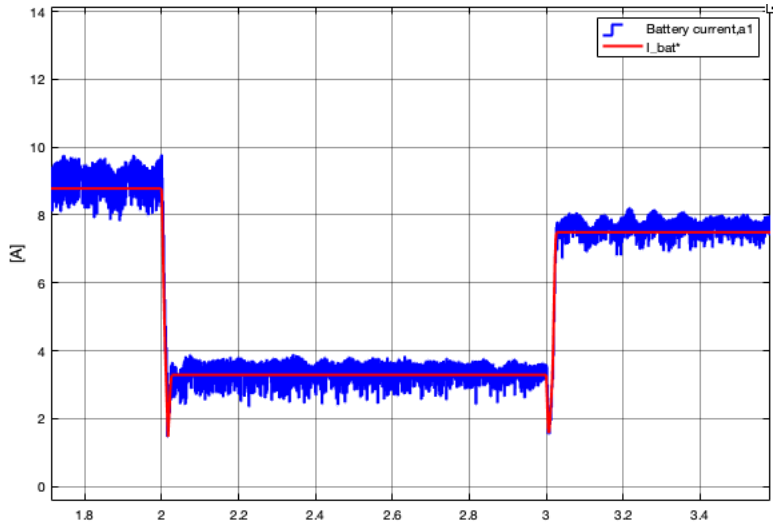
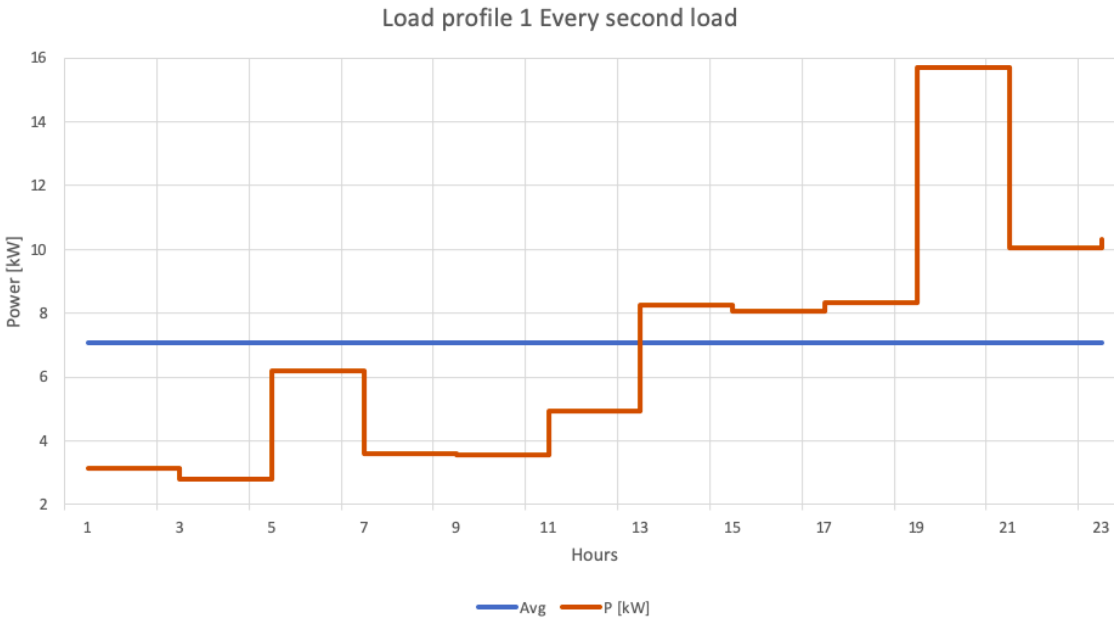


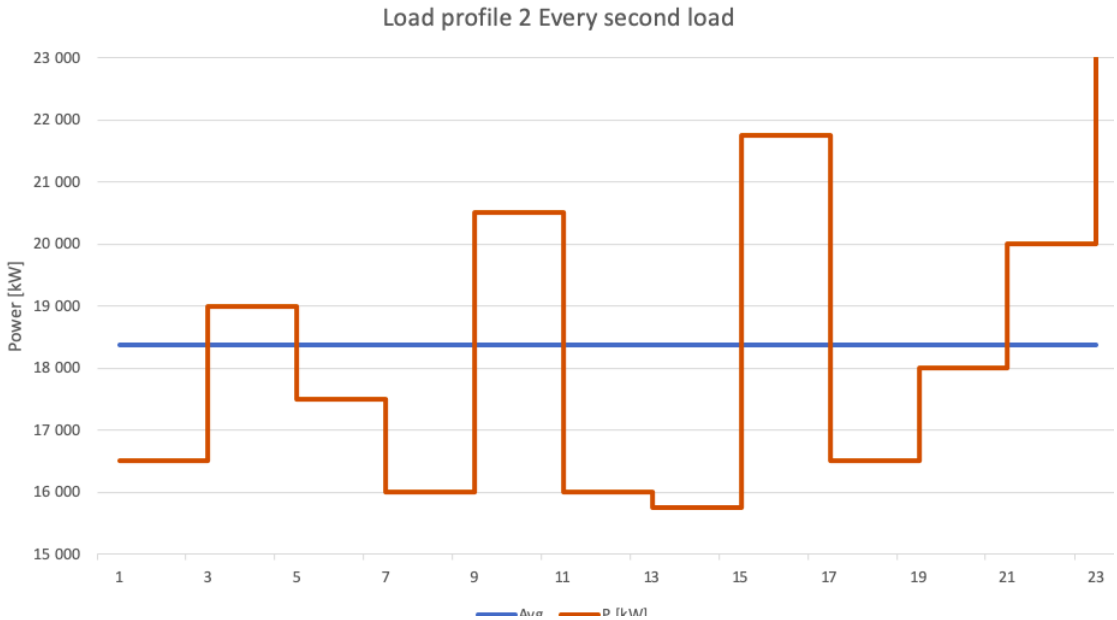
Figure 4.17: Battery current step response when the voltage regulator has reached desired levels, resulting in controlled system steady state operation.

4.5 Peak load shaving

The PLS system has been tested using two load profiles from customers provided by Sogn og Fjordane Energi (SFE). The load data has been adopted from a previous master project at UiB. The project aimed to investigate the use of BESS to achieve PLS, and can be found in [74]. The two load profiles were chosen out of 45 different households. The author justified the choice of load profile by testing the BESS performance on one customer that represents a continuous transition across P_{avg}, and one that had a steady demand shift. The first load profile is included in appendix B, in which gives the hourly power demand for 24 hours. However, it is sufficient to demonstrate the PLS performance upon 12 different sets of loads. The data presented in the forthcoming simulation is using every second hour of the load profile so that roughly the whole day is accounted for. As a result, the simulated loads are shown in figure 4.18.



(a) Load profile 1.



(b) Load profile 2.

Figure 4.18: Load profiles applied for the BESS during PLS control testing.

4.5.1 Load profile 1

Hour	$P[kW]$	$\Delta P[kW]$
1	3.15	3.93
3	2.8	4.28
5	6.2	0.88
7	3.6	3.48
9	3.55	3.53
11	4.95	2.13
13	8.25	-1.17
15	8.05	-0.98
17	8.35	-1.27
19	15.7	-8.62
21	10.05	-2.97
23	10.3	-3.22

Table 4.1: Every second hour of the power demand in profile 1. The average power demand is $P_{avg} = 7.08kW$, and the column represented by "ΔP" is the desired amount of BESS power [74].

Load profile 1 has been scaled according to the BESS rating. The resultant average demand is $P_{avg} = 7kW$ in order to demonstrate the model performance. Table 4.1 illustrates the desired power of the BESS. It is found by using the statement $P_{avg} - P_{demand}$ in equation 3.80. This way, the BESS supplies the deviation of the average grid power. Figure 4.19 shows the simulation results of the loads provided in table 4.1.

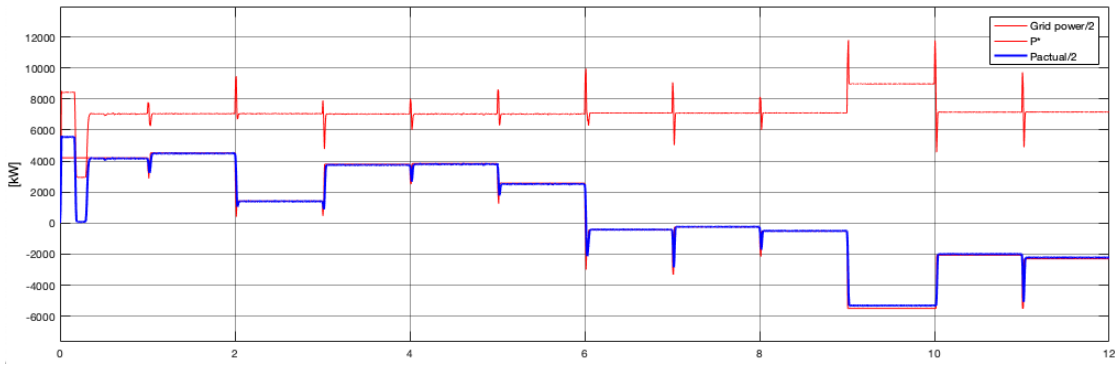


Figure 4.19: Simulation results of load profile 1.

This demonstration shows that the BESS is able to maintain the grid P_{avg} with two

exceptions. The first exception encircles the voltage controller, which previously mentioned is increasing the dc link voltage to desired levels. During this phase, which is approximately in the region $0 < t < 300ms$ of figure 4.19, the BESS is unable to supply the desired amount. The second exception is explained through the load demand at the 19th hour. In order to supply the grid average, the BESS will need to discharge approximately $8.6kW$, which is above the system rating. However, it can be seen that the BESS is delivering the maximum rated power, which is consistent with the designed procedures in these scenarios. Additionally, SOC levels for battery B_{a_1} is included in figure 4.20. Presentation of the second profile results include SOC levels for all batteries.

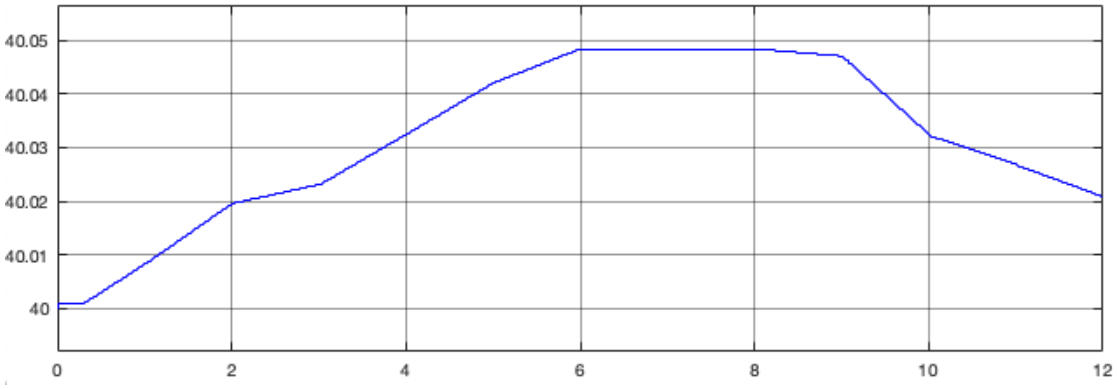


Figure 4.20: Variation of SOC levels for battery B_{a_1} loaded with profile 1 loads.

4.5.2 Load profile 2

Hour	$P[kW]$	$\Delta P[kW]$
1	16.500	1.875
3	19.000	-0.625
5	17.500	0.875
7	16.000	2.375
9	20.500	-2.125
11	16.000	2.375
13	15.750	2.625
15	21.750	-3.375
17	16.500	1.875
19	18.000	0.375
21	20.000	-1.625
23	23.000	-4.625

Table 4.2: Every second hour of the power demand in profile 2. The average power demand is $P_{avg} = 18.375kW$, and "ΔP" gives the desired amount of BESS power.

The loads provided in profile 2 are rapidly fluctuating across the grid average. Table 4.2 shows the power demand for every second hour that day. The column represented by ΔP is included to clarify the desired magnitude and direction of the BESS power. The loads has been scaled by a factor of 10 compared to [74] in order to fill the rated power spectrum of $-5kW < P_{rated} < 5kW$. Using significantly larger loads than the previous case, the average grid power at profile 2 is $P_{avg} = 18.375kW$. Figure 4.21 shows the simulation results of the second load profile.

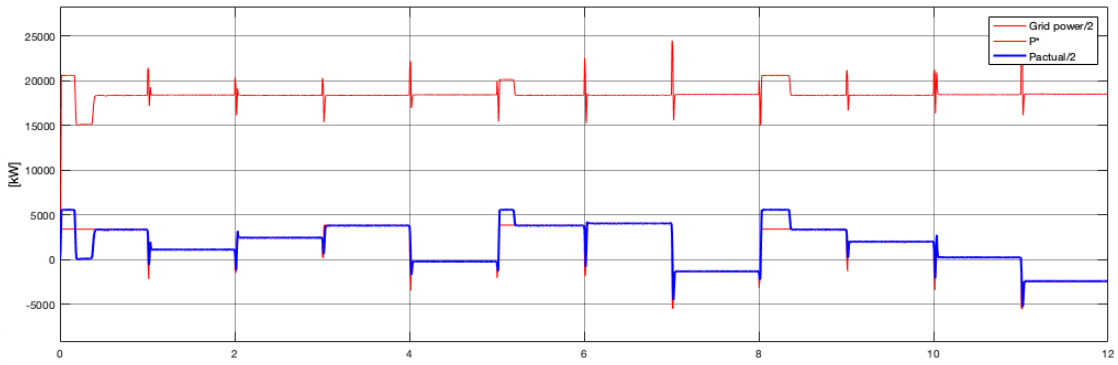
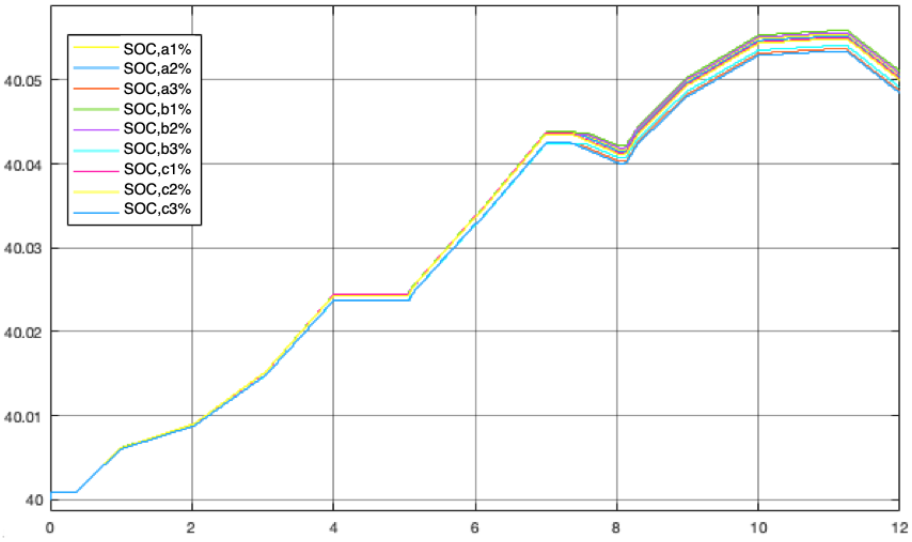


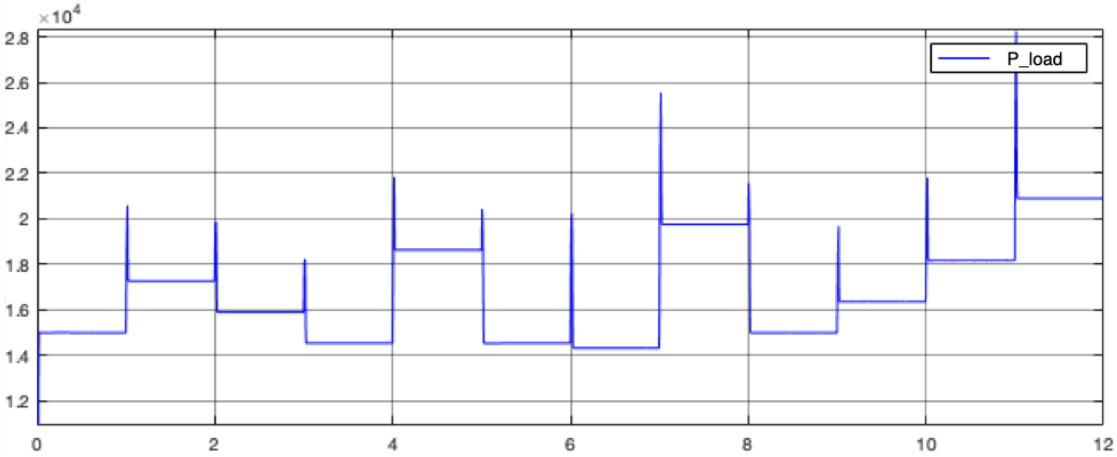
Figure 4.21: Simulation results of the BESS loaded with load profile 2.

This demonstration shows that the BESS is able to supply the load peaks of the grid. The transitions from discharge to charge can be seen as temporary periods in figure

4.21 in which the BESS draws max rated power. The duration of these anomalies is proportional to the voltage controller response time, which is addressed in detail in the previous section. Furthermore, figure 4.22 details regarding both sides of the power conversion stage. Figure 4.22a shows the SOC levels for all nine batteries. During PLS simulations, the 12 voltage balancing controllers has been disconnected in order to release computational burden. This has resulted in the increasing deviation of SOC levels during the simulation, as depicted. Figure 4.22b shows the actual drawn power by the utility loads, which is a simulated visualization of table 4.2.



(a) Variation of SOC for all nine batteries loaded with load profile 2.



(b) Utility load consumption.

Figure 4.22: Supplementary details of PLS-testing during BESS loaded with load profile 2.

4.6 Self healing

The SH logic proposed in section 3.7 is simulated for three different load cases. Table 4.3 shows an overview of the load connected to the algorithm search order 1-6 respectively. It has been tested for three scenarios (Case 1-3), where each of the cases represents a different load dynamic. The results are presented through these three cases to emphasize that the loads satisfying the maximum power condition is reconnected momentarily, regardless of the condition in the previous load. As mentioned in section 3.7, there has been made an assumption regarding the power measurement of the loads. Ideally, the actual power drawn by the load should be fed back to the control system in order to account for the dynamics of changing loads. However, during start-up, it is zero power drawn by the loads due to the utility supply being interrupted. In order to address this, it is assumed that the power drawn by the loads in the moment of utility disconnection is known. In practice, this may be realized through Current Transformers (CT) in the utility substation or other real-time power flow monitoring, such as conducted in [66]. In this analysis, the load power P_{L_n} is known so that it is emulated by a constant. In case 3, as stated in table 4.3, a load change at an arbitrary feeder is included in order to illustrate the dynamics of the proposed logic.

Load order	Load case 1 [kW]	Load case 2 [kW]	Load case 3 [kW]
P_{L_1}	0.75	9	1.25
P_{L_2}	1.5	1	0.75
P_{L_3}	1	6	1.5 (changes to 0.8 kW at 1 sec)
P_{L_4}	3	10	2
P_{L_5}	9	2	4.5
P_{L_6}	10	1.5	7

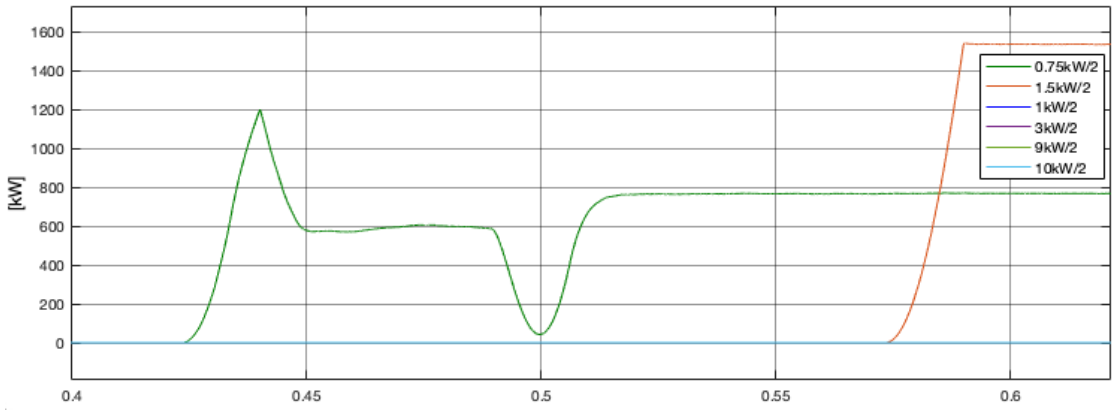
Table 4.3: Overview of load power during different load cases for self healing.

4.6.1 Case 1

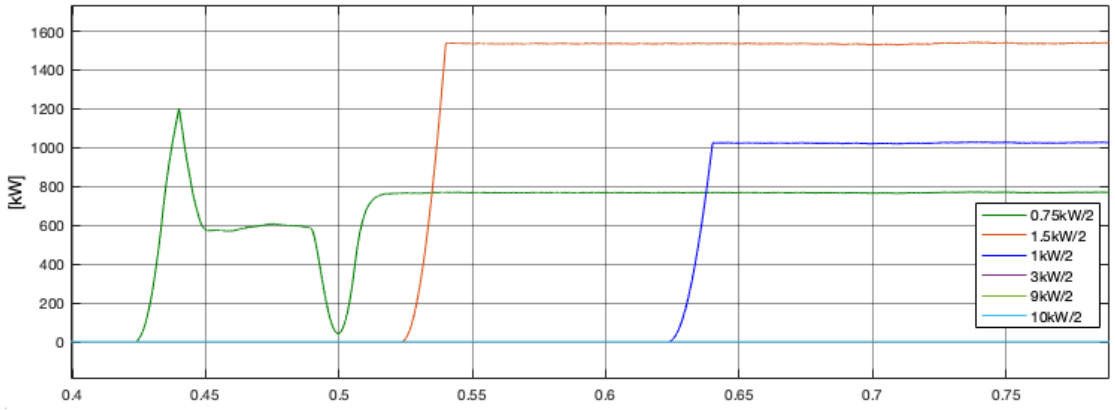
The loads represented in case 1 are predetermined to demonstrate that the loads are reconnected in turn. An additional purpose of this load constellation is to shown that no other feeders are reconnected if the outcome will exceed the maximum power limit of the BESS. Figure 4.23 shows a load re-connection for a grid outage set at 0.4 seconds. The BESS were at $5kW$ charge as preset condition to figure 4.23. For every 100 ms, the next load is compared with both the rated power and the loads that already has been reconnected. After the grid is disconnected and the first load is reconnected, there is a transient phase between 425-515 ms. Note that this precondition were settled when the BESS went from charge to discharge when SH-logic was activated. The unstable phase is due to the shift in dc-link voltage, that is, when the dc-link voltage control

switched from the BDAC converter voltage controller to the BDC voltage controller. For instance, if the BESS originally were in discharge mode previous to the grid disruption, this unstable phase would only depend on the current controller start-up. This will be demonstrated shortly. Here, the steady state power output is reached after approximately $t = 515ms$. Figure 4.23a shows a 150 ms delay between load selection. Seeing as steady state output was reached at 80-90 ms, figure 4.23b shows the same conditions, only with a 100 ms selection delay.

Figure 4.23b shows the re-connection of $0.75kW$, $1.5kW$ and $1kW$ respectively. The signal explanation box in the bottom right corner of figure 4.23b gives the load selection order. If the next load, that is, $3kW$ were to fulfill $P_N - P_{L_1} - P_{L_2} - P_{L_3} > 0$, then it would reconnect at 725 ms.



(a) 150 ms delay between load inspection. Steady state operation is reached after 520 ms.



(b) Load inspection time reduced to 100 ms delay.

Figure 4.23: Simulation results of case 1 where the three first loads are reconnected. The green line represents the $0.75kW$ load and shows start-up instability due to the influence of the current controllers.

Figure 4.24 shows the BESS power output for for the same scenario. Seeing as no loads are connected to the grid in this case, the BESS power is charging with $5kW$ which is the only load that is supplied by the grid. At $t = 0.4$ seconds, the grid power drops, as indicated by the green line. When SH-mode is activated, as indicated by the shift in P^*, the load selection finds that the first load at $0.75kW$ can be reconnected. The next two loads are reconnected the following 200 ms. As figure 4.24 shows, the remaining loads are all to large for the BESS to supply.

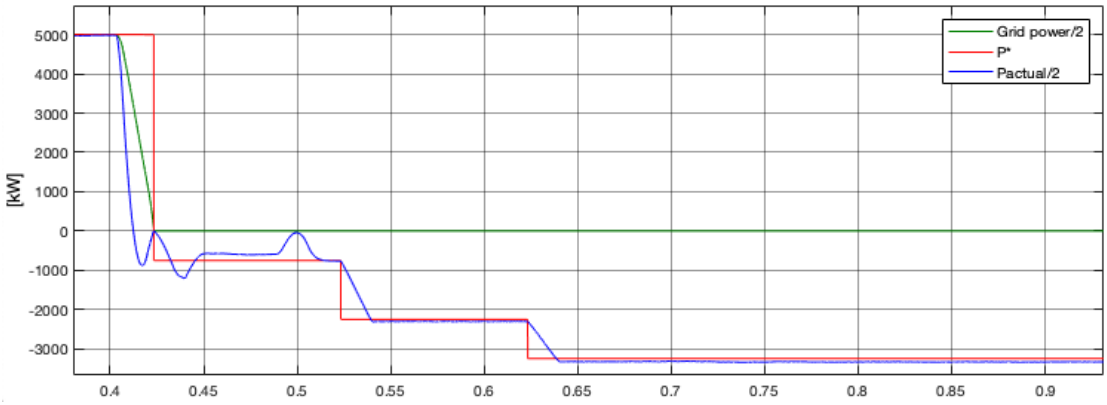
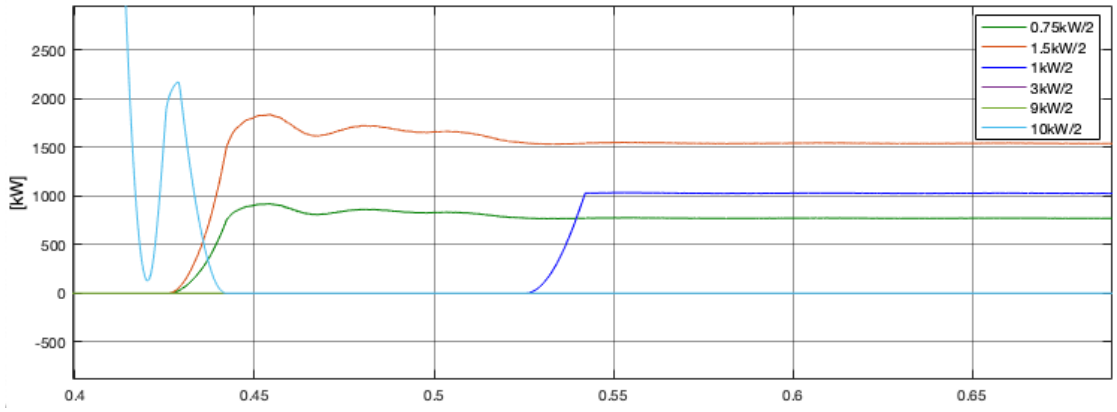


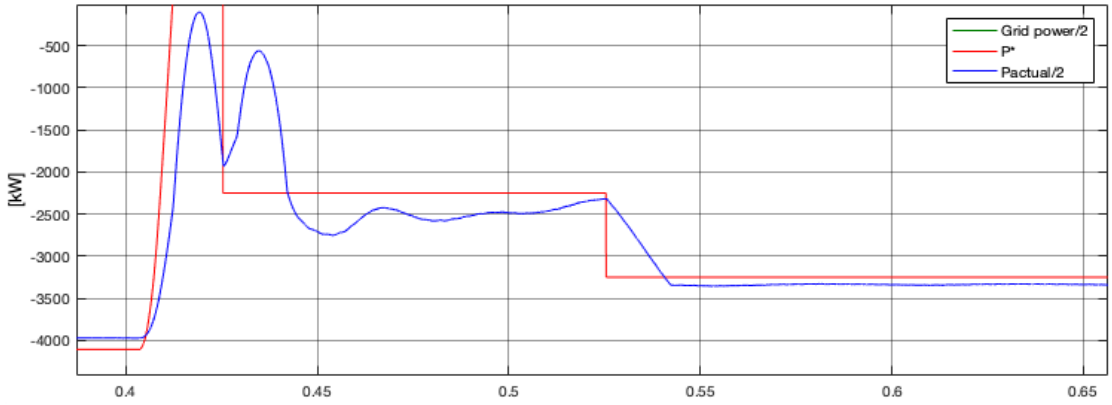
Figure 4.24: BESS power output when dynamics change from $5kW$ charging power at 400 ms to SH-mode. The plot shows an incremental amount of discharged power due to loads being reconnected, and settles when the remaining loads are to large.

Next, the case 1 loads are applied for different starting conditions. Although the time of grid disruption is the same as in figure 4.23 and 4.24, figure 4.25 shows the activation of SH-mode when the BESS originally discharged $4kW$ into the grid. Additionally, a $10kW$ load were connected, as indicated by the light blue line. As the grid-supply is disrupted, the BESS cannot supply the load as stand-alone. This is shown by the power surge in the $10kW$ load moments before SH-mode is activated. This is disconnected by the SH logic. Seeing as the V_{dc}-reference is the same for both discharge mode and SH-mode, the transient instability caused by the change in dc link voltage is significantly improved under these initial conditions. This is depicted in figure 4.25, where the two first loads are reconnected. Since the second load at $1.5kW$ is reconnected 100 ms faster than in the previous initial conditions, the third load of $1kW$ is reconnected 100 ms faster accordingly.

Figure 4.25b shows the simultaneous BESS power output. It illustrates that the start-up instability is still present, although under these initial conditions, it only depends on the current controllers. As the power output reaches steady state, the next load is reconnected by the load selection logic.



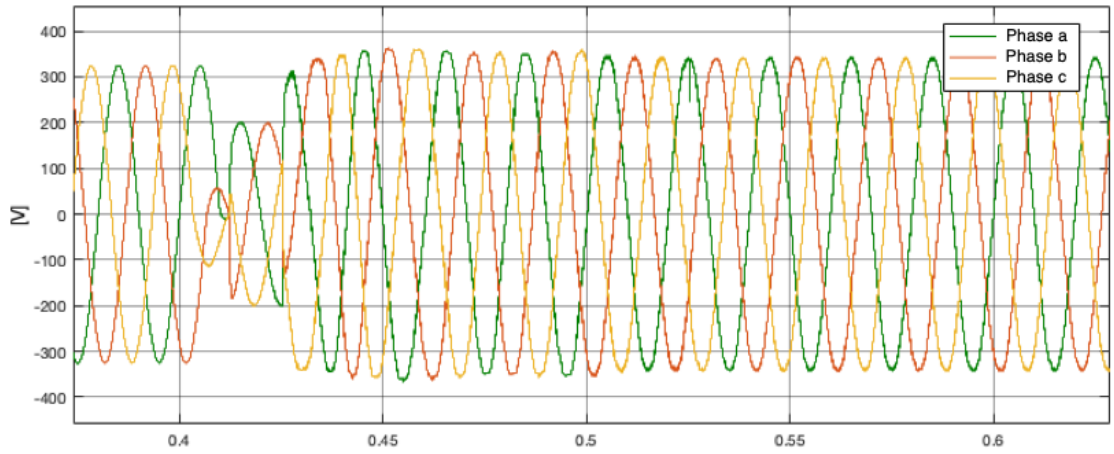
(a) Individual load power.



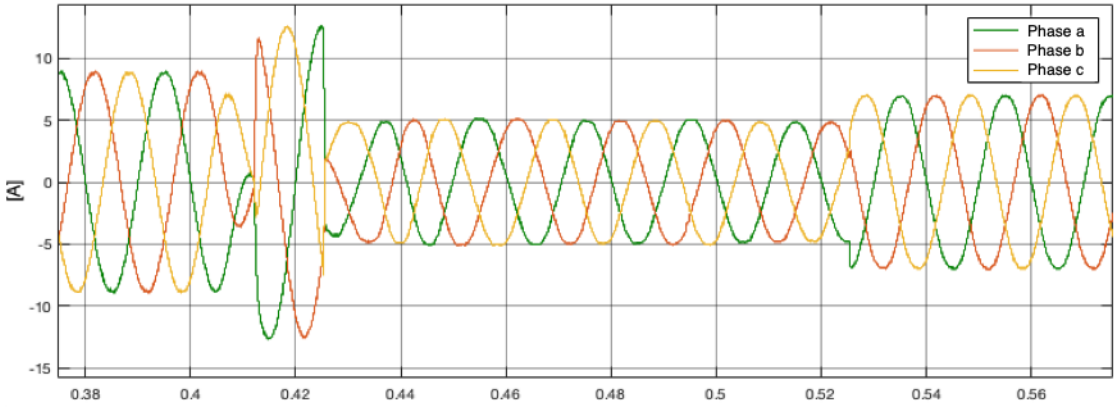
(b) BESS power output.

Figure 4.25: Case 1 load simulation from $4kW$ discharge starting condition. Grid disruption at 0.4 seconds.

Figure 4.26 shows waveforms of the voltage and current output during the same circumstances. Since the BESS is already in discharge-mode, the voltage suffers a significant drop when the grid disconnects, as shown in figure 4.26a. The reason is that it is trying to supply $10kW$ to grid-connected loads alone. As a consequence, the current output increases to compensate for the delivered power, as shown in figure 4.26b. If the BESS was charging at the time of disruption, the currents and voltage would drop to zero from the time the grid disconnected and to the SH-system gets activated. When the third load of $1kW$ is reconnected at approximately 525 ms, it can be shown that the voltage stays constantly at $230\sqrt{2}$, while the current increases to meet the power demand. Additionally, it should also be remarked that the grid retrieves a new synchronization that resembles the internal fictitious SH-grid.



(a) Output voltage waveforms during SH-activation at 0.4 seconds.



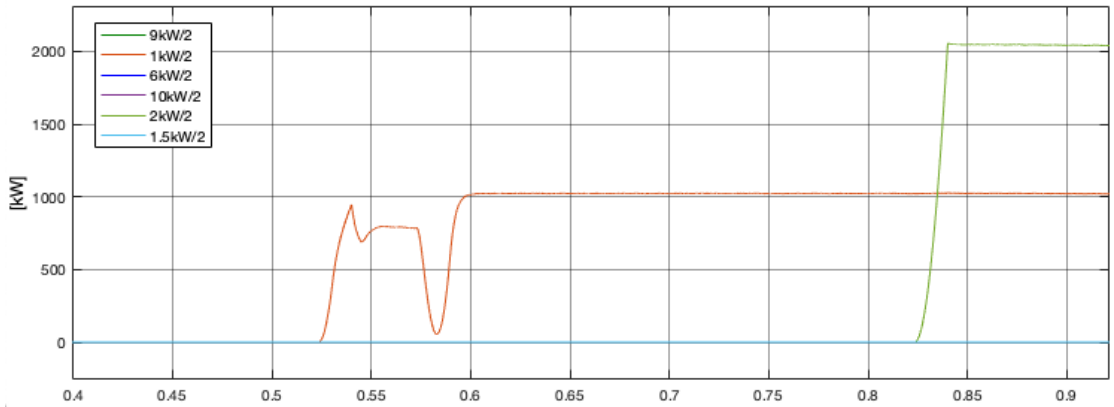
(b) Output current waveforms during disruption at 0.4 seconds.

Figure 4.26: BESS current and voltage output during case 1 load simulation. Starting condition is grid disruption at 0.4 seconds when the BESS was discharging $4kW$.

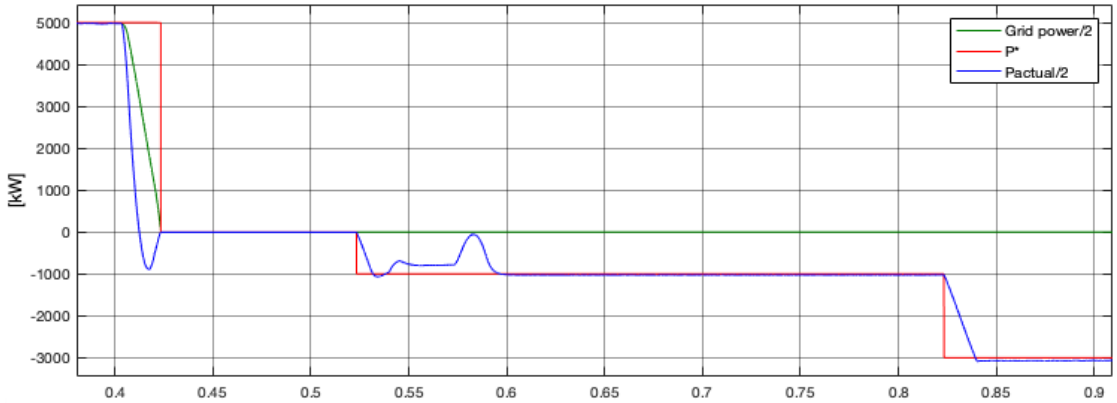
4.6.2 Case 2

In this section, simulation results from the case 2 loads from table 4.3 are provided. Figure 4.27 shows the individual load power and the BESS power output respectively. It is simulated under the circumstance that the BESS is charging $5kW$ and that the grid is disconnected at 0.4 seconds. The signal explanation box in the top left corner in figure 4.27a provides the selection inspection order. Seeing as the there is larger loads connected to the utility in this case, the BESS cannot reconnect the majority of them. As the load selection logic searches through the loads, it finds that it is capable of reconnecting $P_{L_2} = 1kW$ at 525 ms and $P_{L_5} = 2kW$ at 8.25 ms. This is both consistent with the power capabilities of the BESS, and the intended selection design.

Figure 4.27b shows the power output of the BESS. This demonstrates that the BESS power output in the instantaneous moment of grid disruption drops negative, peaking at approximately $-950W$. This happens due to the sudden disappearance of the charging power flowing towards the batteries. The dc-link filters are releasing stored electric charge towards the utility side, which leads to such a temporary discharge. The output power of the batteries are zero until the selection logic finds a suppliable load. As the first load is reconnected at 525 ms, figure 4.27b shows the start-up instability previously mentioned. However, as the controllers reaches its desired levels, the system achieves steady state operation. This is demonstrated by the re-connection of load five at 825 ms. If the load configuration where to consist of several smaller loads, they would be reconnected under the same dynamic terms as for the fifth load.



(a) Case 2 individual load power.

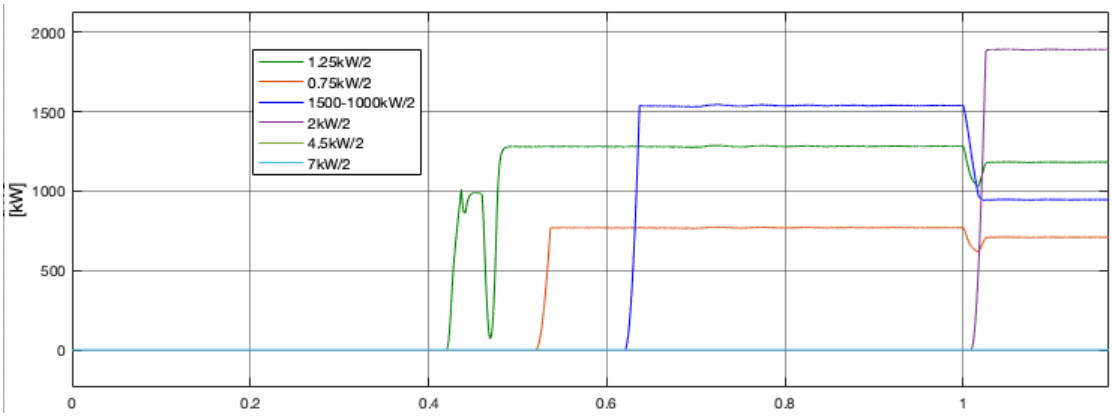


(b) Case 2 BESS power output.

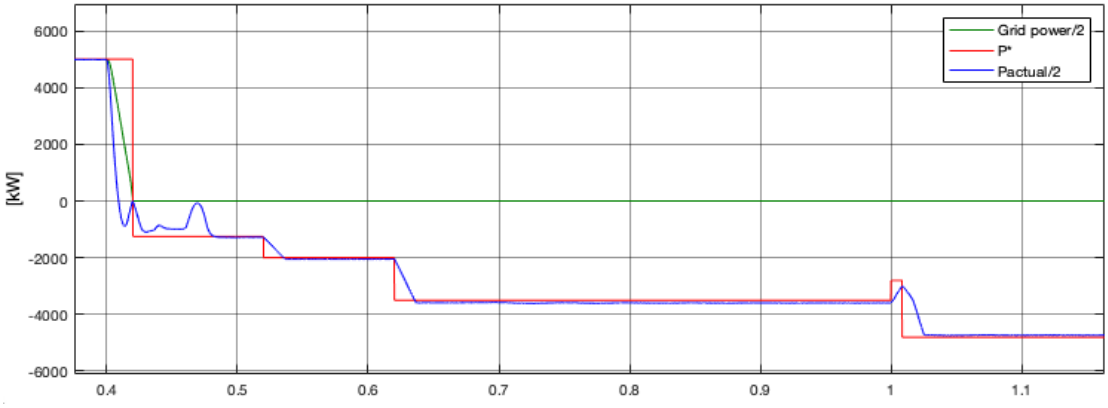
Figure 4.27: Simulation results for case 2. Initial conditions is set to be $5kW$ charge when a grid disruption occurs at 0.4 seconds.

4.6.3 Case 3

The purpose of the loads presented in case 3 is to demonstrate the effects of variable loads upon the SH-controls. This is included to demonstrate the SH-selection logic towards dynamic load scenarios, as grid loads are in constant change throughout the day. As presented in table 4.3, P_{L_3} shifts from $1.5kW$ to $0.8kW$ after 1 second. At this point, every load has been searched by the load selection control. Figure 4.28 shows the simulation results for the loads in this case. As figure 4.28a shows, the three first load colored green, red and blue respectively, are reconnected within roughly 200 ms after the grid disruption. These three loads sum to a total of $3.5kW$, which means that no of the remaining loads are suited for re-connection. Figure 4.28b shows the total power output of the BESS, which is consistent with the drawn power. Additionally, it can be seen that no other loads are reconnected in the time period $t_1 = 625ms$ to $t_2 = 1s$. At 1 second, the third load changes to $P_{L_3} = 0.8kW$, as indicated by the blue line in figure 4.28a. Simultaneously, the power output of the BESS drops accordingly as shown in figure 4.28b, until the load selection finds the SH-condition presented in equation 3.83 true for P_{L_4}. When CB_{L_4} trips, load four is reconnected as indicated by the purple line in figure 4.28a. The period between the change in load three and load four re-connection is indicated by the red line P^* in figure 4.28b, which is dependant of the load disconnection magnitude and the amount of power that is about to be reconnected.



(a) Case 3 individual load power. Load three, represented by blue line is changed from $1.5kW$ to $0.8kW$. This enables load four at $2kW$ to reconnect, as indicated by the purple line.



(b) Case 3 BESS power output.

Figure 4.28: Simulation results for case 3. Initial conditions is set to be $5kW$ charge when a grid disruption occurs at 0.4 seconds.

Figure 4.28a shows that the response of the reconnected load four at approximately 1 second is the same as for the previous loads. This is because the response is dictated by the inner loop current controllers of the BDAC converter. However, as mentioned in section 3.7, this load can only be reconnected during load preservation mode. Figure 4.29 shows case 3 without load preservation controls implemented under the same circumstances as in figure 4.28. It depicts the undesired oscillations due to repeatedly true/false statements of the SH-condition of the load selection mode.

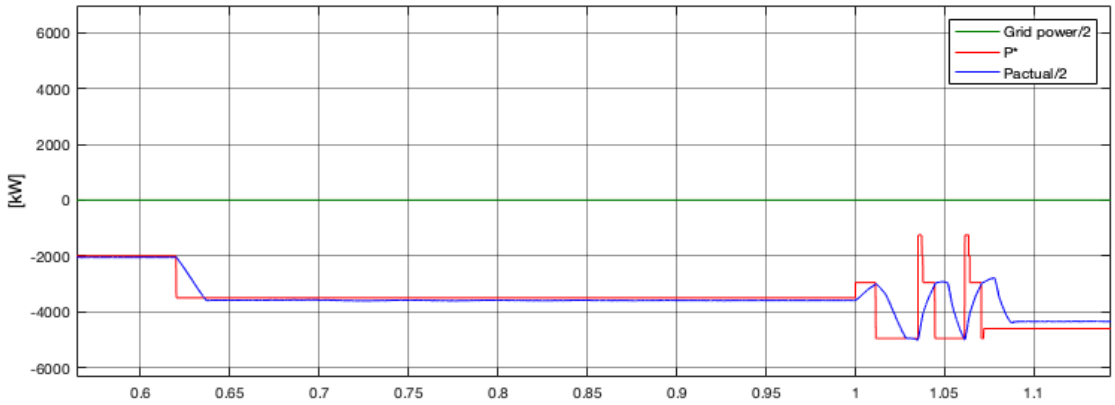


Figure 4.29: Undesired fluctuating CB trip during load change resulting in a repetitive re-connection of a large load. This is the consequence without load preservation controls.

5 Discussion

5.1 Functionality

The designed power conversion and control system has provided successful validation for both PLS and SH scenarios. The controllers provide fast responses to changing demand. Furthermore, the BESS interaction with the utility is characterized by small disturbance levels, which has been shown by the THD analysis in section 4.1. As a result, the average THD at both discharge and charge at rated power is 1.23 %, in which is approximately 15.38 % of the maximum THD limitations provided by IEEE-519 standards. This has led to expected efficiency levels of above 90 %. Although this model is rated $5kW$ using $30Ah$ batteries, it can be scaled towards different utilities of higher system rating. The reason is that this system includes controller transfer functions that are easily changed by inserting parameters for the different applications at hand.

However, a start-up procedure is needed in order to verify this model in laboratory testing. This can, on the other hand, be resolved by the means mentioned in section 4.1. Moreover, a slight down-scaling in the power ratings would be needed in order to verify the model. Here, a system power in the region of $100 - 500W$ would be sufficient. This can be adapted in an effortlessly fashion, as previously stated. Additionally, a suitable battery pack would be needed. The discharge controls were tested upon $9Ah$ batteries when the same filtering components were attached, seeing as this corresponds to a C-rate of approximately 1C. The controller tuning remained unchanged. It showed a reduction in the BDC-converter controlled oscillations of the battery currents and the dc link voltage. This may indicate that it still remains some refined tuning of both controllers and filters. This has been a direct consequence of the complexity of the chosen power electronic topology, which requires additional attention of time in all stages of system building blocks.

5.2 Power electronics

The chosen CHB converters has been delivering consistent results considering the expectations acquired from previous literature in the field of multilevel converters. The choice of arranging the power conversion stage in multilevel modules was made due to its high efficiency, and its impact of battery lifetime. With the increasing demand of electric power, the goal is to deliver it as efficiently as possible. As figure 1.1 indicated in the introduction, there is still a significant amount of improvement that can be made in order to decrease transmission and distribution power dissipation. Considering the relatively new arrival of multilevel converters, it is up to present time much research left in order to push the boundaries of efficiency levels of these converter topologies. Given high efficiency levels at one hand, it still induces discussion regarding the sus-

tainability of the high number of semiconductor devices. In this model, there has been implemented 108 IGBTs. This is the case, despite the fact that it is only distributed across three modules per phase. In MV grids, the number of modules is expected to increase drastically with respect to the three implemented in this project. Considering the on-going integrated circuit (IC) shortage caused by the pandemic SARS-CoV-2, including chips for IGBT manufacturing, it has illustrated the substantial necessity of these components.

On the other hand, a multilevel arrangement results in improved battery state control to a much larger degree than for conventional converter topologies. That is, by decreasing the amount of batteries in series between the dc link nodes results in better SOC, temperature and voltage control of each individual battery, which leads to increased battery life span. Nowadays, batteries are mostly manufactured in countries using fossils such as coal for main electric power source [108]. Seeing as Li-ion battery production requires a significant amount of added energy, the manufacturing process is far from optimized. This means that each battery life-cycle have a certain amount of carbon footprint. Increasing this life cycle through an optimized power conversion stage may contribute to several benefits. First of all, the socioeconomic relations are improved, which paves way for larger incentives towards climate research. Second of all, the increased battery life time results in a smaller net emission of the total battery life cycle. This has a positive impact of the overall climate situation, which in turn directly affects the production of semiconductor devices. For instance, a severe drought period occurred in Taiwan in 2021, which produces approximately 50 % of all silicon wafer in the world [80]. The wafer is used in semiconductor devices, and requires water in the manufacturing process. Moreover, a similar incident happened in the U.S., where severe weather caused the closing of a semiconductor factory [90]. In order to reduce the incidents of extreme weather conditions, the future technology industry needs to be climate-oriented. If this perspective were to have dominated earlier, the extreme weather conditions seen at certain locations today might not have happened. Consequently, the ICs and wafer shortage would not be happening as of today, and the high number of semiconductors in multilevel converters would not have been necessary to justify.

On another note, the PSFB dc-dc converter implemented in this project has provided a functioning BDC stage, which has enabled the simulation of PLS and SH using CHB-converters. However, designing soft switching filters were neglected since it requires a significant amount of work load beyond the aim of this project. This is, nevertheless, the desired course of action if such a system were to be implemented in MV-grid. This is explained by the reduction in IGBT power loss when the switching frequency is increased, as explained in section 3.1.1. Moreover, the topology of the BDC-converter can be used in DAB-mode, leading to added advantages as stated in section 2.3.2. Another filter to

consider is the output L-filter. As explained in section 3.1.2, this was chosen to provide simplifications to the modelling, where the use of an L-filter would provide satisfactory results in demonstrating CHB-converters in PLS and SH applications. However, in a practical system implementation, it is suggested to apply LCL-filters at the BESS output in order to reduce switching noise. Despite this fact, the model delivers very promising results, considering the low THD levels and high efficiency.

5.3 Control strategy

The control strategy has been to investigate to what degree an uneven dc-link voltage affects charging and discharging operation of the BESS. The hypothesis was that this arrangement would ease the system transition into SH-mode. As a consequence of the dc-link voltage shift, the implemented winding ratio of the dc-dc stage HF transformer was chosen with respect to the voltages at each side, where the primary voltage was set to be $\frac{230\sqrt{2}\,V}{3\,modules}$. However, the simulation results has shown that the magnitude of the voltage step from $108.42V$ to $108.42\sqrt{2}V$ is perhaps a too big leap for the outer loop voltage controller to handle. The resultant output power is directly affected by the controller gain and saturation, which is notably depicted in section 4.3. This drawback to the proposed model is noticed in the cases where the BESS transposes from discharge to charge, or during immediate charge start-up. The data presented in section 4.3 is a result of refined controller tuning, in which a faster controller would be unable to increase the dc-link voltage from $108.42V$. Tuning the controller slower on the other hand would result in a slower system response. In light of this, the initial hypothesis proves to be true regarding smooth transition from grid disruption to SH-mode activation, although false during normal operation. Additionally, it is expected that PLS-mode is more active than SH-mode in a physical MV-grid implementation. Therefore, a proposition to resolve this issue might be to disregard the initial hypothesis for this modelled system. Hence, maintaining an equal dc-link voltage at $108.42\sqrt{2}\,V$ to keep consistency with equation 3.6. This way, during the initial phase of a power outage, the voltage can be regulated by the faster BDC-converter voltage controller to desired levels of $108.42\,V$ in order to maintain $V_{rms} = 230\,V$.

Even though the dc-link voltage has been operated at different levels for buck and boost mode, the control strategy of sharing the dc-link voltage between the outer loop BDAC controller and the BDC voltage controller has been successful. This has facilitated the possibilities of constant charging current mode, which may be realized by overwriting the PLS-mode, as described in section 3.7. This way, the current can be controlled in a desired fashion corresponding to the implemented battery C-rate levels.

Regarding the controls of module balancing, the voltage balancing controllers has proven

its capability to balance the dc-link voltages. Thus, the BESS power output provides balanced three-phase power into the utility. On the other hand, section 2.3.3 addresses other methods of module balancing, such as individual module power control or individual SOC-control. The former can be implemented in grids in which constantly suffers from imbalanced power distribution across the phases. The latter involves direct SOC-control of individual battery, in which is a major advantage of using multilevel converters. As initially explained in section 2.3.3, the balancing technique applied for this model was chosen to be voltage balancing.

The balancing controllers were modelled in reverse direction in order to produce a stable process transfer function. Otherwise would impose a negative term in the characteristic equation, which would naturally affect the corresponding controller tuning negatively. However, by resolving the modelling in the conducted manner would still leave a true system description for controller tuning. The results of the balancing controllers have been successful. Although there are slight noise and overshoots across the reference value, the resultant dc link voltage ripples are reduced by including the balancing controllers.

5.4 Peak load shaving

The results of the PLS controls has demonstrated a robust control logic upon load shaving. The BESS supplies with the intended amount of power, and within the threshold limits of the rated power. Furthermore, rapid and repetitive interchanging between charge and discharge is an undesired scenario of Li-ion batteries. The proposed solution to this problem is to restrict the BESS operating region, so that it would be deactivated in the region of $-50W < P^* < 50W$. Depending on the application rating, utility rating, and the statistical magnitude of load fluctuation, this can be suitably and dynamically adjusted. Additionally, a proposed overwrite function has been added so that a grid operator can decide which peaks to reduce. This was listed in section 3.6 as scenarios in which the load forecast is predicted in advance of heavy load hours.

5.5 Self healing

The proposed SH-control shows promising results regarding the re-connection of grid loads after the utility supply drops. In an orderly fashion, it reconnects one load at the time while it makes sure that the BESS is capable of supplying the desired power levels. Furthermore, the SH-logic has been applied upon loads of a random magnitude through the three cases presented in section 4.6. It demonstrates that the control system is able to loop through the loads continuously, so that the dynamics of the utility loads are accounted for. In this regard, the proposed self healing control system is robust and reliable. The first assumptions made beforehand is that every substation circuit breaker

is remotely controlled. The second assumption is that the power flow is properly monitored in the substation. Section 1.1 addressed methods and components in which may realize this in practice.

One drawback with the proposed SH-design is when the last load connected that satisfies the main condition in equation 3.83 results in a smaller power output than the maximum possible. The point being that there is no logic accounting for the additional condition that $P_N - P_{activated}$ should be as low as possible. For instance, seeing as the loads are checked in turn randomly, there may be cases where a small load is checked by the load selection before a larger load. This in disadvantage for the larger, valid load. In this scenario, the resulting BESS power output would be lower than if the larger load was checked first. One way to go about this in this design, is by arranging the loads in a fixed order so that the loads from experience giving the best result are checked first. Here, it can be resolved by choosing the correct pin-connection in the "load selection" subsystem. Similarly, priority may be given to critical loads in this way.

Another issue that might arise with the proposed SH-logic lies within the load preservation controls. In the event of variable loads which increases the total power output passed the rated power limit, the solution provided in this model is to reactivate the load selection logic. If it is a high amount of small loads connected to a large capacity BESS, then the load searching delay of 100 ms might be too large. However, system optimization including start-up circuits, controller fine-tuning and system modification including V_{dc}^* corrections might resolve this so that the load selection restart only is noticed in practice as a blink in the light bulbs.

5.6 Contribution

The power plants across Norway mainly consists of hydro power turbine and generators. The frequency control in these plant constellations are exceedingly more rapid in response than for instance nuclear or coal plants [67, 2]. That makes the Norwegian grid more robust in dealing with significant load changes. However, the increasing electric power demand on world basis has resulted in the intercontinental connection of grids, including Norway with the rest of Europe. Power flows in both direction in the seven cables installed per 2022 [91]. Additionally, several overhead lines connect Norway to Finland and Sweden. On top of that, there is an increasing integration of RES, where wind is especially suited for Norway. In order to secure a steady power flow in the interconnected grid, both HV-BESS and MV-BESS can contribute to maintain the robustness of both transmission and distribution grid. Additionally, as mentioned in section 1.1, installing BESS in conjunction with the continuous power producing wind parks may leave the charging process in large proportions to the wind parks at night,

while conserving the water magazine reserves.

Another point is that SH has been tested in conjunction with PLS, while both smart-grid features are utilizing the fairly recent arrival of multilevel converters. Smaller BESS-applications can be applied as both Uninterruptible Power Supplies (UPS), and to sustain a collection of customers to complete a micro-grid. The former is important seeing as of to day, critical loads are using fossils such as diesel aggregates in high share. The latter represents the socioeconomic aspect of maintaining an uninterruptible, reliable power supply to the residents. This is the core of the incentive-based concept regarding the fee that falls upon the power grid supplier in the event of power outages (KILE) [9]. Finally, the impact of achieving PLS and SH using CHB is quite significant, due to its high efficiency and battery life span conservation through careful condition monitoring. Multilevel inverters are in this regard gradually replacing conventional power conversion topologies to meet the future efficiency power conversion demand.

6 Conclusion

The analysis conducted in thesis addresses the possibility of implementing smart grid features such as PLS and SH in conjunction with BESS applications. The final model indicates a successful composition of proposed design steps.

Utilizing decoupled current control have resulted in a rapid and precise control system response for active and reactive power commands. The outer loop voltage controller is tuned marginally slower to keep consistency with literature. The resulting voltage controller provides accurate reference tracking with inconsequential affection towards the output power quality of the BESS.

The PSFB BDC converter has been added in order to achieve a controlled dc link and to interface the batteries to the grid through GI. Separating the control strategy for buck-mode and boost-mode respectively have resulted in the model feature of CC-charging mode, which is considered to be beneficial with respect to battery lifetime.

Buck-mode controllers provides satisfactory results regarding the transient response, both in terms of settling time, reference tracking and desirable damping. The resulting battery current ripple is well within the limits found in literature.

Boost-mode controllers maintain the dc link voltage at desirable levels. These controllers are to some extent slower than the remaining active controllers, although providing satisfactory results when the system have reached steady state operation. The resulting quality of the power output have been analyzed and concluded to be excellent, having marginally better power quality than buck-mode controllers in terms of THD and battery current ripple. Moreover, boost mode of operation affects the battery voltage ripple to a minimum.

Using FFT, the harmonic analysis have uncovered that the average THD for both charging-mode and discharging-mode is 1.23 %. Considering the upper boundaries for THD in corresponding applications, this is a promising result.

In terms of efficiency, the average of both buck, boost and for all power magnitudes is in the region of 90-95 %. It is assumed that the majority of power losses are dissipated across the dc side filters. Considering that the BDC converter topology are in place in order to realize dual active bridge control, few steps to the control system may pave way to a significant increment in the net efficiency of the power stage.

The PCS consists of CHB-converters in order to optimize the system efficiency and power quality. The complexity of the chosen PE topology have resulted in the design

of individual module voltage balancing controllers. Analysis shows that there is a decisive need of these, and results indicates that the nine module voltages are controlled in a desirable manner. The voltages are corrected by modifying the modulation index, in which is in the linear region during the entire correction operation.

The initial hypothesis regarding uneven dc-link voltage for both modes of operation was made in order to maintain the correct HF transformer winding ratio during SH-mode. This way, the voltage controllers duty were to maintain steady dc link voltage across all the modules and to rapidly suppress voltage disturbances during heavy load connection or disconnection. Despite the fact that it affects the transition from discharging mode to charging mode to some degree, it shows that the change between desired levels of charging power, and the transition back to discharging mode is untroubled, with a fast dynamic response.

Model simulation in PLS-mode shows that load leveling is achieved and that safe operating areas are accounted for. In this regard, the PLS control is successful in demonstrating the capabilities of the proposed control system.

The SH-logic has been design and verified through three loading cases. The results have shown that the proposed SH-control manages to reconnect the desired loads after grid disruption. Furthermore, it demonstrates a scenario in which accounts for variable loads. Consequently, it accomplishes to continuously asses whether to connect the remaining loads that previously has been too large for the rated BESS power. In that note, the results produced by model simulation are consistent with the intended design.

7 Future work

There is a few steps needed in order to realize the proposed model in a MV-network. These include:

- Finalize start-up procedures such as starting resistor and optimize an inrush battery current control.
- Adding a LC-filter at the BESS output in order to optimize the resultant power quality.
- Consider to add DAB control.
- Consider to change the concept of uneven dc-link voltage by changing the HF transformer ratio and redo controller tuning using the same system transfer functions.
- Laboratory testing and model validation where component, battery, Digital Signal Processor (DSP) and Power Processing Unit (PPU) selection is needed.
- Write algorithms composing a predictive model for load forecasting directed towards PLS optimization.

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Appendices

A BDC transfer function calculation

A.1 Boost

Rewriting equation 3.78:

$$G_{bdc}(s) = \frac{\tilde{v}_c}{\tilde{d}} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)Vbat] + (C_1 - C_2)X$$

In order to solve equation 3.78, these terms needs to be calculated:

$$(A_1 - A_2) = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix} - \begin{pmatrix} 0 & -\frac{1}{nL} \\ \frac{1}{nC} & -\frac{1}{RC} \end{pmatrix} = \begin{pmatrix} 0 & \frac{1}{nL} \\ -\frac{1}{nC} & 0 \end{pmatrix} \tag{A.1}$$

$$(B_1 - B_2) = (C_1 - C_2) = 0; \tag{A.2}$$

$$(sI - A) = \begin{pmatrix} s & 0 \\ 0 & s \end{pmatrix} - \begin{pmatrix} 0 & \frac{2(d-1)}{nL} \\ \frac{2(1-d)}{nC} & -\frac{1}{RC} \end{pmatrix} = \begin{pmatrix} s & \frac{-2d+2}{nL} \\ \frac{-2+2d}{nC} & s + \frac{1}{RC} \end{pmatrix} \tag{A.3}$$

$$(sI - A)^{-1} \Rightarrow \frac{1}{Det(sI - A)} \cdot \begin{pmatrix} s + \frac{1}{RC} & \frac{2d-2}{nL} \\ \frac{2-2d}{nC} & s \end{pmatrix} \tag{A.4}$$

where,

$$Det(sI - A) = |D| = s^2 + \frac{s}{RC} + \frac{4d^2 - 8d + 4}{n^2 LC} \tag{A.5}$$

$$C(sI - A)^{-1} = \begin{pmatrix} 0 & 1 \end{pmatrix} \begin{pmatrix} s + \frac{1}{RC} & \frac{2d-2}{nL} \\ \frac{2-2d}{nC} & s \end{pmatrix} = \begin{pmatrix} \frac{2-2d}{nC} & s \end{pmatrix} \tag{A.6}$$

$$C(sI - A)^{-1}(A_1 - A_2) = \begin{pmatrix} \frac{2-2d}{nC} & s \end{pmatrix} \begin{pmatrix} 0 & \frac{1}{nL} \\ -\frac{1}{nC} & 0 \end{pmatrix} = \begin{pmatrix} \frac{-s}{nC} & \frac{2-2d}{n^2 LC} \end{pmatrix} \tag{A.7}$$

$$C(sI - A)^{-1}(A_1 - A_2)X = \begin{pmatrix} \frac{-s}{nC} & \frac{2-2d}{n^2 LC} \end{pmatrix} \begin{pmatrix} I_L \\ V_c \end{pmatrix} = -\frac{I_L s}{nC} + \frac{V_c(2 - 2d}{n^2 LC} \tag{A.8}$$

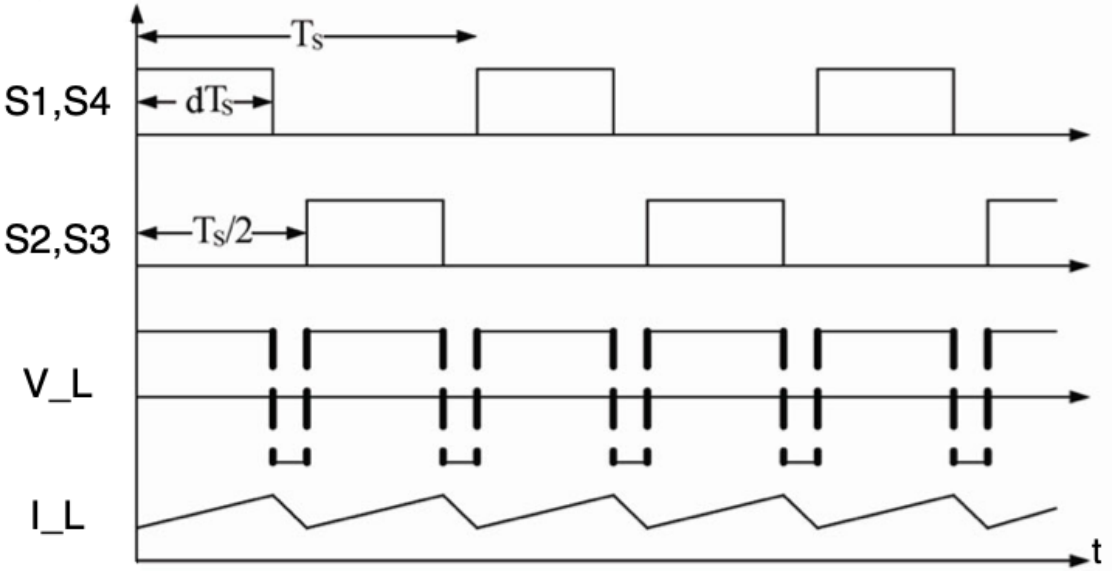
Finally,

$$\frac{1}{|D|}\cdot C(sI-A)^{-1}(A_1-A_2)X = \frac{-\frac{I_L s}{nC}+\frac{V_c(2-2d)}{n^2LC}}{s^2+\frac{s}{RC}+\frac{4d^2-8d+4}{n^2LC}} \qquad |\cdot(n^2RLC) \tag{A.9}$$

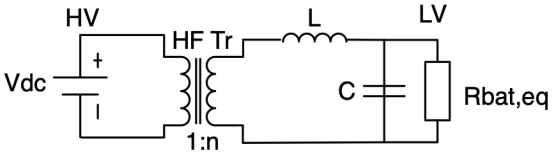
$$= G_{BDC,boost}(s) = \frac{\tilde{v}_{dc}}{\tilde{d}} = \frac{-I_L snRL + V_c R(2-2d)}{n^2RLCs^2 + n^2Ls + R(4d^2-8d+4)}$$

A.2 Buck

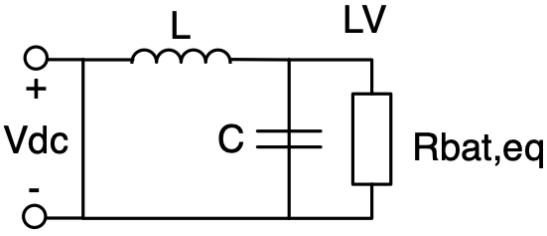
Similarly as boost mode, the buck mode waveforms and equivalent circuit is shown in figure A.1



(a) V_L, I_L and switching waveforms corresponding to buck mode [19].



(b) Equivalent circuit state 1.



(c) Equivalent circuit state 2.

Figure A.1: Circuit state and equivalents valid for BDC buck mode of operation.

Applying KVL upon the circuit in figure A.1b:

$$\frac{V_{dc}}{n} = v_L + v_c = L\frac{d(i_L)}{dt} + v_c \Rightarrow \frac{d(i_L)}{dt} = \frac{v_{dc}}{nL} - \frac{V_c}{L} \tag{A.10}$$

KCL:

$$i_L = i_c + i_R = c\frac{d(v_c)}{dt} + \frac{v_c}{R} \Rightarrow \frac{d(v_c)}{dt} = \frac{i_L}{C} - \frac{v_c}{RC} \tag{A.11}$$

$$\frac{d(x_1)}{dt}|_{state(1)} = \frac{d}{dt}\begin{pmatrix} i_L \\ v_c \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}\begin{pmatrix} I_L \\ V_c \end{pmatrix} + \begin{pmatrix} \frac{1}{nL} \\ 0 \end{pmatrix} V_{dc}$$

$$y_o = \begin{pmatrix} 0 & 1 \end{pmatrix} x(t) \tag{A.12}$$

Applying KVL upon the circuit in figure A.1c:

$$V_{dc} = v_L + v_c = L\frac{d(i_L)}{dt} + v_c \Rightarrow \frac{d(i_L)}{dt} = \frac{V_{dc}}{L} - \frac{v_c}{L} \tag{A.13}$$

KCL:

$$i_L = i_c + i_R = c\frac{d(v_c)}{dt} + \frac{v_c}{R} \Rightarrow \frac{d(v_c)}{dt} = \frac{i_L}{C} - \frac{v_c}{RC} \tag{A.14}$$

$$\frac{d(x_2)}{dt}|_{state(2)} = \frac{d}{dt}\begin{pmatrix} i_L \\ v_c \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}\begin{pmatrix} I_L \\ V_c \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_{dc}$$

$$y_o|_{state(2)} = \begin{pmatrix} 0 & 1 \end{pmatrix} x(t) \tag{A.15}$$

Introducing perturbating terms:

$$\begin{cases} x = & X + \tilde{x} \\ d = & D + \tilde{d} \\ v_{dc} = V_{dc} + \tilde{v}_{dc} \end{cases} \tag{A.16}$$

Rewriting equation 3.78:

$$G_{bdc}(s) = \frac{\tilde{v}_c}{\tilde{d}} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)Vbat] + (C_1 - C_2)X$$

In order to solve equation 3.78, these terms needs to be calculated:

$$A_{avg} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} 2d + \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}(1-2d) = \begin{pmatrix} 0 & -\frac{2d}{L} \\ \frac{2d}{C} & -\frac{2d}{RC} \end{pmatrix}\begin{pmatrix} 0 & -\frac{(1-2d)}{L} \\ \frac{(1-2d)}{C} & -\frac{(1-2d)}{RC} \end{pmatrix} \tag{A.17}$$

$$= \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}$$

$$C_{avg} = C = \begin{pmatrix} 0 & 1 \end{pmatrix} \tag{A.18}$$

$$(A_1 - A_2) = (C_1 - C_2) = 0 \tag{A.19}$$

$$(B_1 - B_2) = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} - \begin{pmatrix} \frac{1}{nL} \\ 0 \end{pmatrix} = \begin{pmatrix} \frac{n-1}{nL} \\ 0 \end{pmatrix} \tag{A.20}$$

$$(sI - A) = \begin{pmatrix} s & 0 \\ 0 & s \end{pmatrix} - \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} = \begin{pmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{1}{RC} \end{pmatrix} = \begin{pmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & \frac{RCs+1}{RC} \end{pmatrix} \tag{A.21}$$

$$(sI - A)^{-1} \Rightarrow \frac{1}{Det(sI - A)} \cdot \begin{pmatrix} \frac{RCs+1}{RC} & -\frac{1}{L} \\ \frac{1}{C} & s \end{pmatrix} \tag{A.22}$$

Where:

$$Det(sI - A) = |D| = \frac{RCs + 1}{RC} + \frac{1}{LC} \tag{A.23}$$

$$C(sI - A)^{-1} = \begin{pmatrix} 0 & 1 \end{pmatrix} \begin{pmatrix} \frac{RCs+1}{RC} & -\frac{1}{L} \\ \frac{1}{C} & s \end{pmatrix} = \begin{pmatrix} \frac{1}{C} & s \end{pmatrix} \tag{A.24}$$

$$C(sI - A)^{-1}(B_1 - B_2) = \begin{pmatrix} \frac{1}{C} & s \end{pmatrix} \begin{pmatrix} \frac{n-1}{nL} \\ 0 \end{pmatrix} = \frac{n-1}{nLC} \tag{A.25}$$

$$C(sI - A)^{-1}(B_1 - B_2)V_{dc} = \frac{V_{dc}(n-1)}{nLC} \tag{A.26}$$

Finally, $G_{BDC,buck}$ can be obtained. However, using [2] results in the transfer function $\frac{\tilde{v}_{bat}}{\tilde{d}}$. The control strategy has been to control $\tilde{i}_{bat}$. Using the equivalent circuits in figure A.1b and figure A.1c, it can be noted that $i_{Rbat,eq} = \frac{v_{bat}}{R_{bat,eq}}$. For that reason, $G_{BDC,buck}$ can be written as:

$$G_{BDC,buck} = \frac{\tilde{i_{bat}}}{\tilde{d}} = \frac{1}{|D|R}[C(sI - A)^{-1}(B_1 - B_2)V_{dc}] \tag{A.27}$$

$$= \frac{V_{dc}(n-1)}{nRLC(\frac{RCs^2+s}{RC} + \frac{1}{LC})} = \frac{V_{dc}(n-1)}{nRLCs^2 + nLs + Rn} = \frac{61.33}{2.9 \cdot 10^{-4}s^2 + 1.01 \cdot 10^{-3}s + 12.69}$$

B 24h load data profile 1

Hour	$P\ [kW]$	$\Delta P\ [kW]$	$W\ [kWh]$
1	8.2	0.55	0.55
2	3.15	-4.502	-4.502
3	2.8	-4.852	-9.354
4	3.6	-4.052	-13.406
5	6.2	-1.452	-14.858
6	5.65	-2.002	-16.860
7	3.6	-4.052	-20.913
8	3.3	-4.352	-25.265
9	3.55	-4.102	-29.367
10	7.3	-0.352	-29.719
11	4.95	-2.702	-32.421
12	8.6	0.948	0.948
13	8.25	0.598	1.546
14	14.2	6.548	8.094
15	8.05	0.398	8.492
16	7.9	0.248	8.740
17	8.35	0.698	9.438
18	10.1	2.448	11.885
19	15.7	8.048	19.933
20	10.5	2.848	22.781
21	10.05	2.398	25.179
22	10.25	2.598	27.777
23	10.3	2.648	30.425
24	9.1	1.448	31.873
	$P_{avg} = 7.652$		

Table B.1: 24 hour load profile corresponding to load profile 1. Scaled by a factor of 5 from previous project [74].

C Simulink battery model

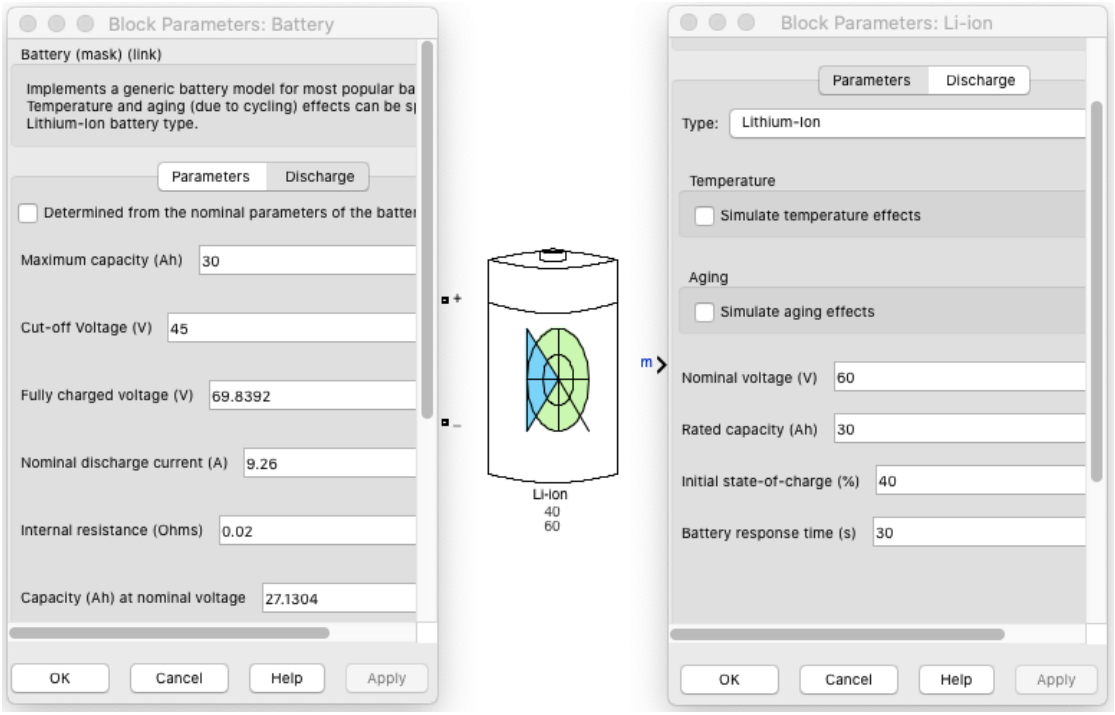


Figure C.1: Simulink model of Li-ion battery with inserted values.

D Block diagram of current loops

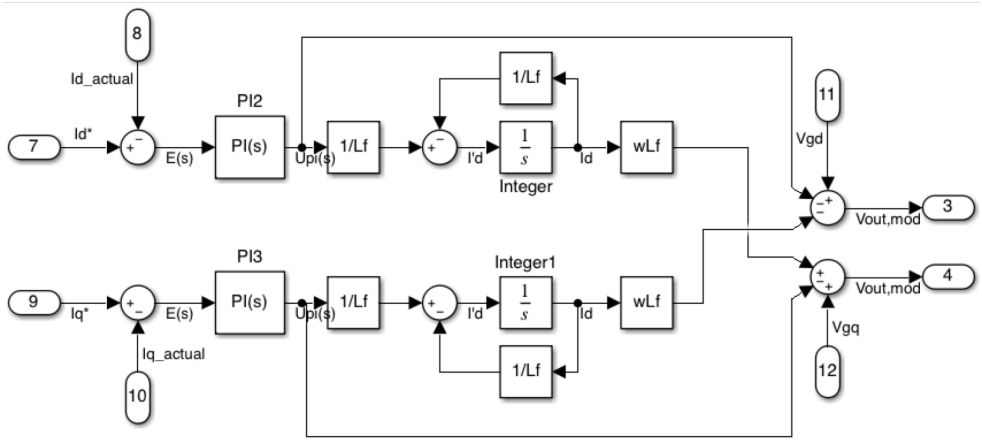


Figure D.1: Block diagram of state space model drawn from equation 3.29 and 3.30.

E Simulink SOC calculation

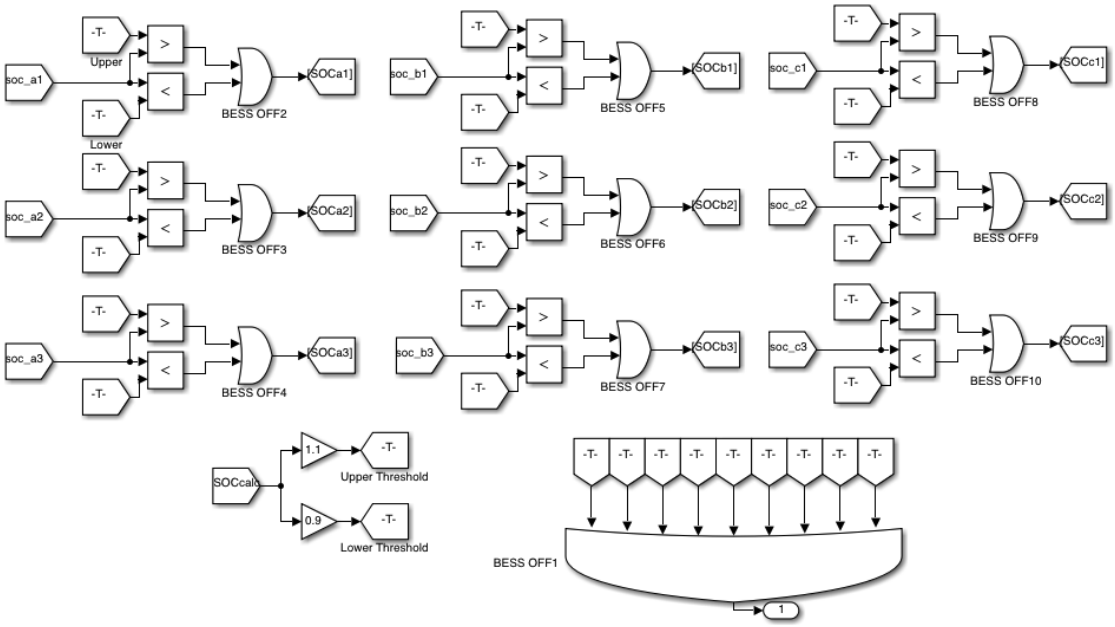


Figure E.1: Simulink implementation of SOC difference logic. The same control logic can be applied for temperature control.

F SH-logic implementation

F.1 SH overview

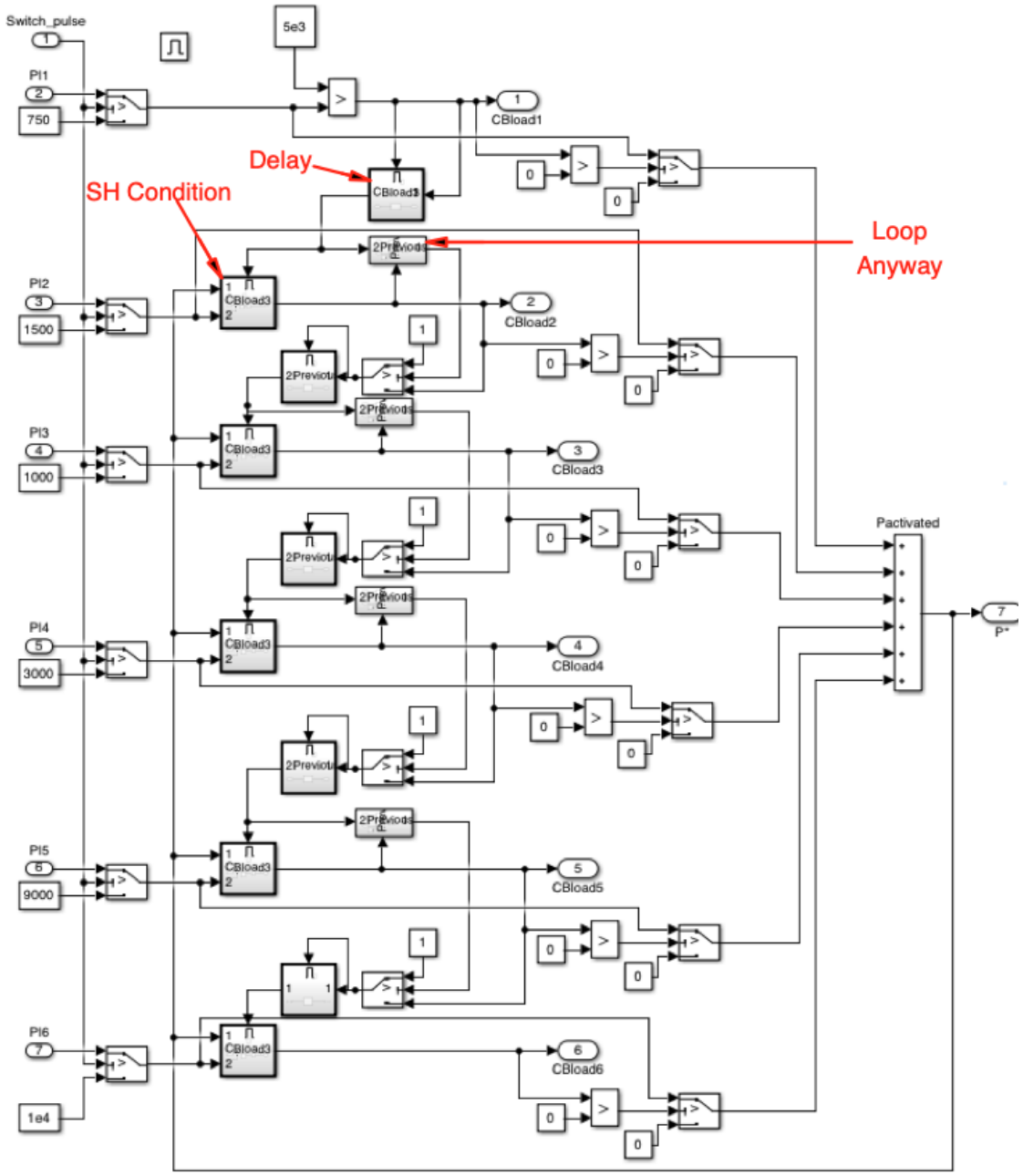


Figure F.1: Six load case selection. The load preservation controls in figure 3.32 are connected across the output and second input of the "SH Condition block".

F.2 Loop anyway

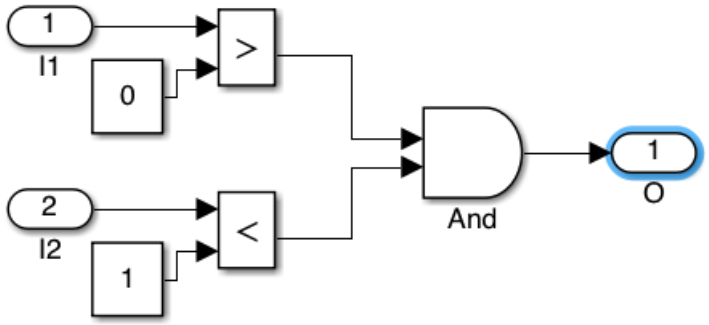


Figure F.2: This block ensures that each individual load are checked for re-connection regardless of the state of the previous load in the loop.