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# Production and integration of the ATLAS Insertable B-Layer

## The ATLAS IBL collaboration

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Abstract: During the shutdown of the CERN Large Hadron Collider in 2013-2014, an additional pixel layer was installed between the existing Pixel detector of the ATLAS experiment and a new, smaller radius beam pipe. The motivation for this new pixel layer, the Insertable B-Layer (IBL), was to maintain or improve the robustness and performance of the ATLAS tracking system, given the higher instantaneous and integrated luminosities realised following the shutdown. Because of the extreme radiation and collision rate environment, several new radiation-tolerant sensor and electronic technologies were utilised for this layer. This paper reports on the IBL construction and integration prior to its operation in the ATLAS detector.

Keywords: Large detector systems for particle and astroparticle physics; Particle tracking detectors (Solid-state detectors)

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## 1 Introduction

The ATLAS [1] general purpose detector is used for the study of proton-proton ($pp$) and heavy-ion collisions at the CERN Large Hadron Collider (LHC) [2]. It successfully collected data at $pp$ collision energies of 7 and 8 TeV in the period of 2010-2012, known as Run 1. Following an LHC shutdown in 2013-2014 (LS1), it has collected data since 2015 at a $pp$ collision energy of 13 TeV (the so-called Run 2).

The ATLAS inner tracking detector (ID) [1, 3] provides charged particle tracking with high efficiency in the pseudorapidity[1] range of $|\eta| < 2.5$. With increasing radial distance from the interaction region, it consists of silicon pixel and micro-strip detectors, followed by a transition radiation tracker (TRT) detector, all surrounded by a superconducting solenoid providing a 2 T magnetic field.

The original ATLAS pixel detector [4, 5], referred to in this paper as the Pixel detector, was the innermost part of the ID during Run 1. It consists of three barrel layers (named the B-Layer, Layer 1 and Layer 2 with increasing radius) and three disks on each side of the interaction region, to guarantee at least three space points over the full tracking $|\eta|$ range. It was designed to operate for the Phase-I period of the LHC, that is with a peak luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an integrated luminosity of approximately 340 $\mathrm{fb}^{-1}$ corresponding to a TID of up to 50 MRad[2] and a fluence of up to $1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ NIEL. However, for luminosities exceeding $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which are now expected during the Phase-I operation, the read-out efficiency of the Pixel layers will deteriorate.

This paper describes the construction and surface integration of an additional pixel layer, the Insertable B-Layer (IBL) [6], installed during the LS1 shutdown between the B-Layer and a new smaller radius beam pipe. The main motivations of the IBL were to maintain the full ID tracking performance and robustness during Phase-I operation, despite read-out bandwidth limitations of the Pixel layers (in particular the B-Layer) at the expected Phase-I peak luminosity, and accumulated radiation damage to the silicon sensors and front-end electronics. The IBL is designed to operate until the end of Phase-I, when a full tracker upgrade is planned [7] for high luminosity LHC (HL-LHC) operation from approximately 2025.

The IBL is a small detector that was constructed on a short timescale using the results from sensor, electronic and mechanical R&D programs, to operate over an extended period in a hostile environment. The emphasis was to construct the detector on time, while identifying and understanding the various production and quality assurance (QA) issues with the R&D groups and industrial partners. Some choices during the IBL construction were consequently influenced by the schedule.

[1] ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the centre of the detector and the $z$-axis along the beam pipe. The $x$-axis points from the IP to the centre of the LHC ring, and the $y$-axis points upward. Cylindrical coordinates $(r, \phi)$ are used in the transverse plane, $\phi$ being the azimuthal angle around the $z$-axis. The pseudorapidity is defined in terms of the polar angle $\theta$ as $\eta = -\ln\tan(\theta/2)$. An ATLAS convention refers to the (-z) side of the detector as the C-side, and the (+z) side of the detector as the A-side.

[2] The Total Ionising Dose (TID) in silicon is a measure of the radiation dose for the front-end electronics. For silicon sensors, a more relevant measure of the radiation dose is the non-ionising energy loss (NIEL), normally expressed as the equivalent damage of a fluence of 1 MeV neutrons ($\mathrm{n_{eq}/cm^2}$).



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The procurement, QA and assembly of the different IBL components into loaded staves were undertaken at the participating institutes. The staves were then transported to CERN, where the final IBL integration and testing was made before installation in the ATLAS experiment.

The motivations and performance of the IBL are briefly described in section 2 together with a brief introduction to the detector layout and the electronic system design. Section 3 describes the production and QA of the individual pixel module components (the sensors, front-end electronics, and module hybrids). This is followed by a discussion of the module assembly and tests to ensure the required electrical and mechanical quality of the modules. The technical specification and fabrication of local support staves and their associated electrical services are discussed in section 4. In section 5 the loading of accepted pixel modules on the staves is described, together with a discussion of the module and stave QA at successive steps in the loading process. Section 6 briefly describes the off-detector services, including the detector control, interlock and power supply systems, and the data acquisition. The integration of the staves and their services around the beam pipe is presented in section 7. Finally, section 8 lists the most critical aspects of the IBL project, together with a short summary of the IBL status following its successful installation in ATLAS.

## 2 Detector overview and physics motivations

### 2.1 Layout overview

The IBL is a new layer of pixel sensors designed to fit between the B-Layer of the existing Pixel detector and a new beam pipe of reduced inner radius of 23.5 mm. It consists of 14 carbon composite staves, providing full azimuthal ($\phi$) hermeticity for high transverse momentum ($p_{\mathrm{T}} > 1$ GeV) particles and longitudinal coverage up to $|\eta|$ of 3. Each stave supports 20 pixel sensor modules together with their electrical services and a cooling pipe. Each module is constructed from a pixel sensor (section 3.1) with each pixel of nominal size $250 \times 50\,\mu\mathrm{m}^2$ electrically bonded (section 3.3.1) to a channel of a read-out chip (the FE-I4B chip described below and in section 3.2). The IBL volume contains the staves and the services in the space between an inner support tube (IST) fixed on the Pixel structure and an inner positioning tube (IPT) with an inner radius of 29 mm. A key feature is that independent radial volumes are installed, allowing for the removal of the beam pipe with respect to the IBL package, or the IBL and beam pipe with respect to the Pixel package.

The ATLAS ID, including the IBL detector and its envelope, is shown in figure 1. The 3-dimensional structure of the IBL detector with its services is shown in figure 2.

The main IBL layout parameters are summarised in table 1 and a comparison between the technical characteristics of the IBL and the Pixel detector is shown in table 2. With a mean sensor radius of 33.5 mm (compared with 50.5 mm for the Pixel B-Layer), the IBL sensors and front-end electronics must cope with a much higher hit rate and radiation doses of $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ NIEL and 250 MRad TID during Phase-I operation. To address these requirements, a new front-end read-out chip, the FE-I4B [8], was developed in 130 nm CMOS technology satisfying the ATLAS requirements of radiation tolerance and read-out efficiency at high luminosity. In addition, the FE-I4B chip has a substantially larger active area compared to the FE-I3 front-end chip [4] of the Pixel detector, and a cell size reduced to $250 \times 50\,\mu\mathrm{m}^2$ from $400 \times 50\,\mu\mathrm{m}^2$, the shorter side being in the transverse plane. The smaller layer radius and the reduced pixel cell length are crucial parameters in defining the performance improvement of the ID, in particular the track-extrapolation resolution.



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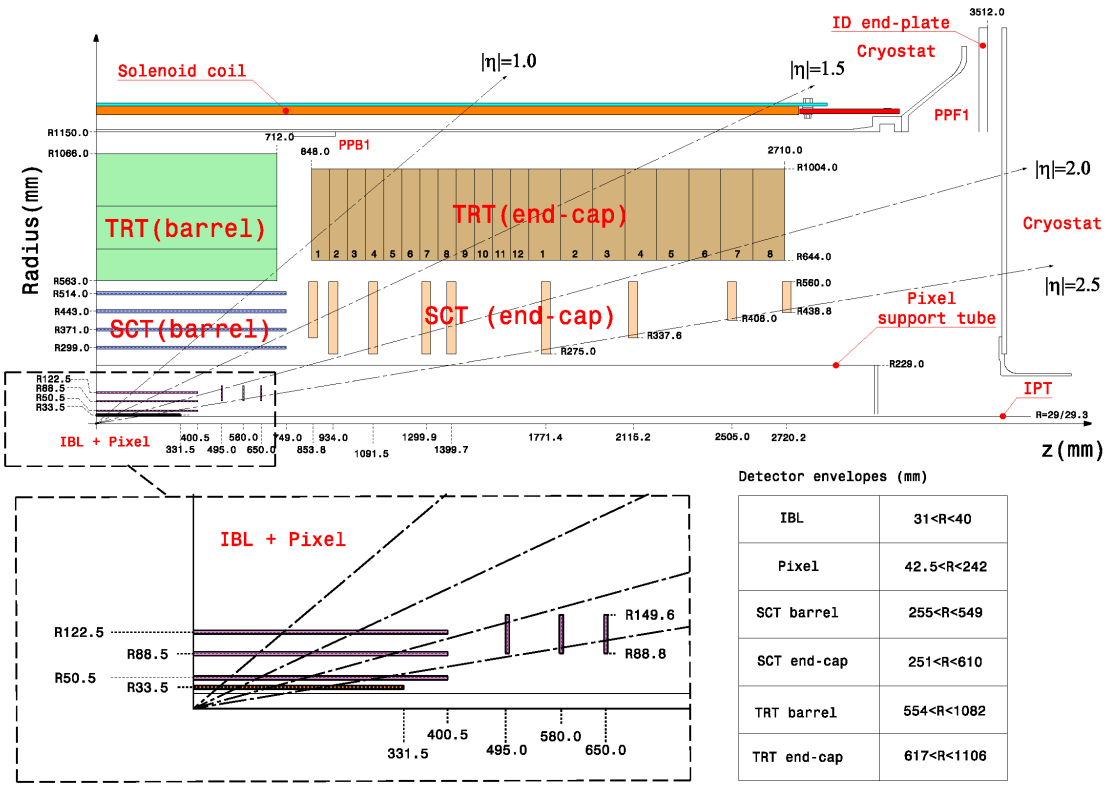


Detector envelopes (mm)

| | |
|---|---|
| IBL | 31<R<40 |
| Pixel | 42.5<R<242 |
| SCT barrel | 255<R<549 |
| SCT end-cap | 251<R<610 |
| TRT barrel | 554<R<1082 |
| TRT end-cap | 617<R<1106 |

**Figure 1.** The layout of the ATLAS inner tracking detector, including the additional IBL detector layer. The inner positioning tube (IPT) supports the IBL staves and separates them from the beam pipe.

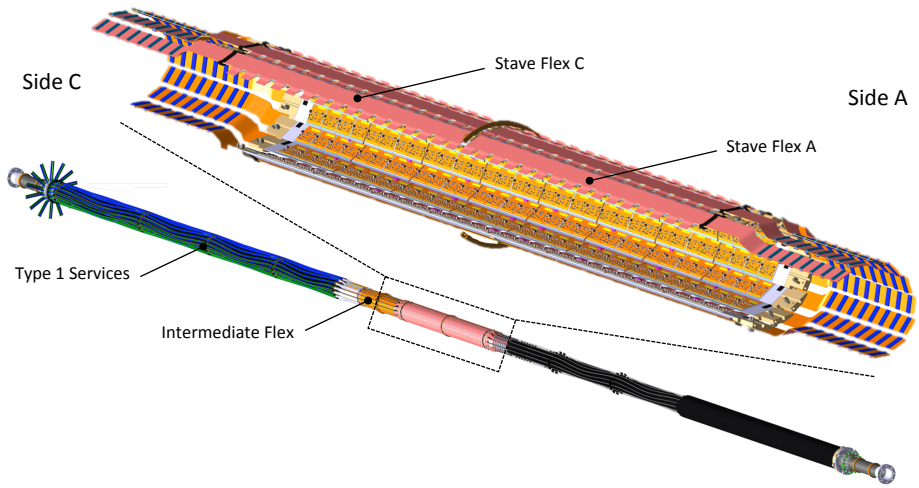


**Figure 2.** Longitudinal view of the IBL detector and its services. The insert shows an enlarged 3-dimensional view of the detector with its modules arranged cylindrically around the beam pipe.

The IBL stave configuration is shown in figure 3. Two module types [9] are installed on each stave. A total of 12 double-chip planar n-in-n sensors similar to those equipping the Pixel detector, each bump-bonded to two FE-I4B read-out chips, populate the central stave region. Four single-chip



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**Table 1.** Main layout parameters for the IBL detector.

| Item | Value |
|---|---|
| Number of staves | 14 |
| Number of physical modules per stave | 20 (12 planar, 8 3D) |
| Number of FEs per stave | 32 |
| Coverage in $\eta$, no vertex spread | $\lvert\eta\rvert < 3.0$ |
| Coverage in $\eta$, $2\sigma$ (122 mm) vertex spread | $\lvert\eta\rvert < 2.58$ |
| Active $\lvert z\rvert$ stave length (mm) | 330.15 |
| Stave tilt in $\phi$ (degree) | 14 |
| Overlap in $\phi$ (degree) | 1.82 |
| Center of the sensor radius (mm) | 33.5 |

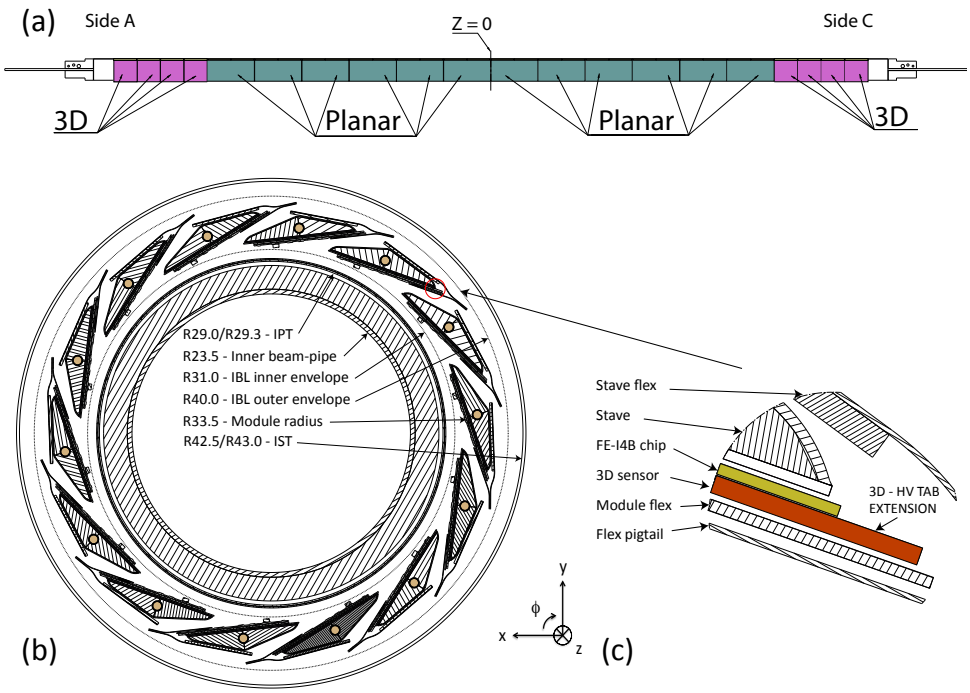


**Figure 3.** IBL detector layout: (a) Longitudinal layout of planar and 3D modules on a stave. (b) An $r-\phi$ section showing the beam pipe, the inner positioning tube (IPT), the staves of the IBL detector and the inner support tube (IST), as viewed from the C-side. (c) An expanded $r-\phi$ view of the corner of a 3D module fixed to the stave.

3D sensors, adopted for the first time in a collider tracking detector and each bump-bonded to one FE-I4B chip, populate each end of the stave. The staves are mounted with the sensors facing the beam pipe and are inclined in azimuth by 14° to achieve an overlap of the active area. This tilt also compensates for the Lorentz angle of drifting charges in the case of planar sensors, and the effect



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of partial column inefficiency for normal incidence tracks in the case of 3D sensors. Owing to space constraints, the sensors are not shingled along the stave (in $z$). To minimise the dead region, modules are glued on the stave with a physical gap of 200 µm.

**Table 2.** Comparison of the main characteristics of the Pixel and IBL detectors.

| Technical characteristic | Pixel | IBL |
|---|---|---|
| Active surface ($m^2$) | 1.73 | 0.15 |
| Number of channels (x $10^6$) | 80.36 | 12.04 |
| Pixel size ($\mu m^2$) | 50×400 | 50×250 |
| Pixel array (columns × rows) | 160×18 | 336×80 |
| Front-end chip size ($mm^2$) | 7.6×10.8 | 20.2×19.0 |
| Active surface fraction (%) | 74 | 89 |
| Analog current (µA/pixel) | 26 | 10 |
| Digital current (µA/pixel) | 17 | 10 |
| Analog voltage (V) | 1.6 | 1.4 |
| Digital voltage (V) | 2.0 | 1.2 |
| Data out transmission (MBit/s) | 40-160 | 160 |
| Sensor type | planar | planar / 3D |
| Sensor thickness (µm) | 250 | 200 / 230 |
| Layer thickness (% $X_0$) | 2.8 | 1.88 |
| Cooling fluid | $C_3F_8$ | $CO_2$ |

Minimising the material budget is very important for the optimisation of the tracking and vertex performance. The IBL radiation length, averaged over azimuth and taking into account the stave tilt and the overlap between staves, is estimated to be 1.88% $X_0$ for tracks produced perpendicular to the beam axis at $z = 0$. This is ~30 % less than that of the Pixel B-Layer.[3] The reduced thickness was achieved by using more advanced technologies as discussed in the following sections. These include: a new low-mass module design; local support structures (staves) made of low density, thermally conductive carbon foam; the use of $CO_2$ evaporative cooling, which is more efficient in terms of mass flow and pipe size; and electrical power services using aluminium conductors. Table 3 reports the main contributions to the IBL material budget. Figure 4 shows the material traversed by a straight track originating in $z = 0$ as a function of $\eta$, smeared over the azimuthal angle.

[3]The as-built IBL radiation length was evaluated using the ATLAS geometry model, as discussed in the IBL TDR [6]. The difference with respect to the value reported in the IBL TDR is mainly due to an initial underestimation of the module material and the addition of the IPT. A recent description of the ATLAS ID material and its comparison with Run 2 collision data is now available [10].



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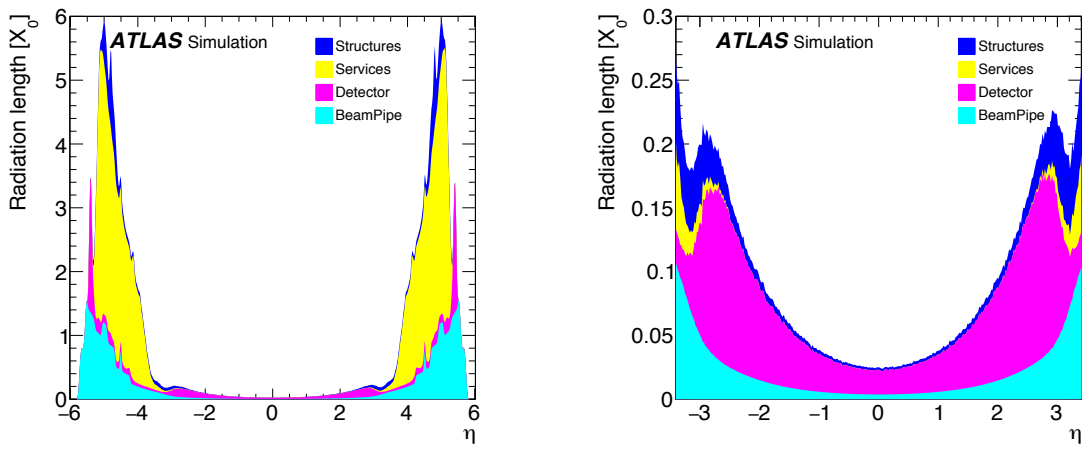
**Table 3.** IBL material budget as a fraction of $X_0$, averaged over the azimuthal angle $\phi$ for straight tracks produced perpendicular to the beam axis at $z = 0$, as implemented in the ATLAS geometry model. The beam pipe material is excluded from the IBL total.

| Item | Value (% $X_0$) |
|---|---|
| Beam pipe | 0.32 |
| IPT | 0.12 |
| Module | 0.76 |
| Stave | 0.60 |
| Services | 0.19 |
| IST | 0.21 |
| IBL total | 1.88 |




(a) (b)

**Figure 4.** Material budget of the IBL detector as a fraction of $X_0$, as implemented in the ATLAS geometry model using straight tracks originating from the nominal beam line at z = 0. Different components are shown: beam pipe, detector (IBL staves, modules, inner positioning tube (IPT)), services (cooling and cables) and structures (stave rings, end-blocks, sealing ring area, inner support tube (IST)). (a) Dependence on $\eta$, averaged over $\phi$. (b) A zoomed view of the central $|\eta|$ region where precise tracking ($|\eta| < 2.5$) is performed.

### 2.2 System overview

The IBL electronic system includes the FE-I4B read-out chip, the off-detector read-out boards (the read-out driver (ROD) [11] and the back-of-crate board (BOC) [12, 13]), the detector control system (DCS) [14], the electronics and sensor power supplies, and all of their associated electrical and optical services.The data acquisition (DAQ) [15] controls the transfer of data to and from the off-detector read-out boards, while the DCS controls the electrical and environmental monitoring of the detector as well as the power distribution to the pixel sensors and FE-I4B chips.



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The electrical service design was driven by physical space constraints, especially in the inner region where all services and connectors must fit into the narrow IBL envelope over a length of approximately 3 m, and by the conflicting requirements of material budget, radiation hardness and electrical performance. Optical transmission is excluded in the IBL envelope because of the high radiation level. Figure 5 shows a block diagram of electrical services for one half-stave (the services are symmetrical, at each end of a stave). Each module of a given half-stave is connected electrically by a stave flex to an end-of-stave (EoS) card. The stave flex transfers the data from the half-stave, as well as control signals from the DAQ and DCS, and the power distribution. In the EoS region the detector services are connected via intermediate flexes to a cable board. The cable board connects the flexes to ~3 m-long extensions (Type 1 cables) that reach the ID end-plate where the first Patch Panel (PP1) is located to allow for electrical and optical connections to the external services after installation in ATLAS. A second break of the electrical services occurs at another Patch Panel (PP2) on the detector periphery that is accessible during a short shut-down.

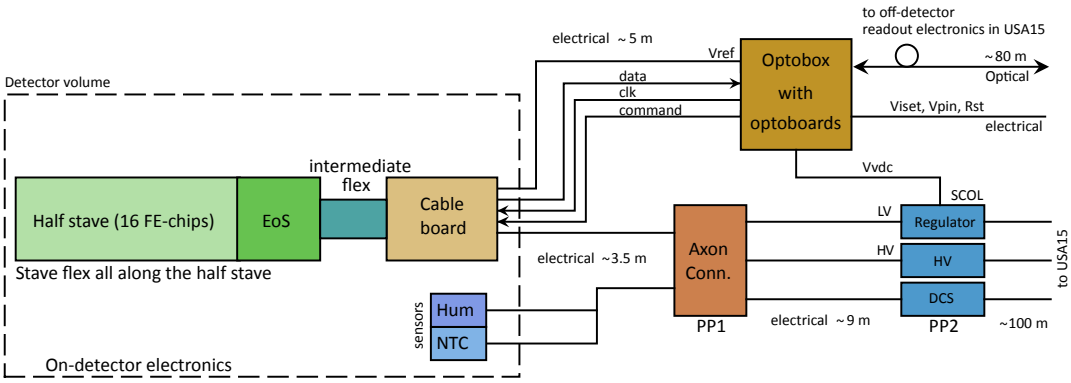


**Figure 5.** Block diagram of on-detector and off-detector electrical services for one half-stave of the IBL detector. The on-detector front-end read-out and services are described in sections 3 and 4. The off-detector services (Type 1 cables) reaching the PP1 patch panel and opto-box are described in section 6.

Details of the FE-I4B chip and the module flex hybrid that connect a module to the stave flex are described in section 3, while those of the stave flexes are described in section 4. The off-detector electronics and power-supplies, as well as the electrical and optical services, are described in section 6.

### 2.3 Tracking and flavour tagging performance

The ATLAS ID provides charged particle tracking with high efficiency in the $|\eta| < 2.5$ range over the full azimuthal range. The pixel layers are crucial for the reconstruction of charged particles trajectories, for their extrapolation to the production point and for the reconstruction of multiple collision and decay vertices which occur in each bunch crossing. The pixels are therefore of crucial importance to the flavour tagging performance. Any inefficiency of the innermost B-Layer would result in a degradation of that performance.

A first assessment of the expected improvements in tracking and vertex reconstruction performance was performed for the IBL Technical Design Report (TDR) [6]. Since then, the ATLAS simulation, digitisation and cluster reconstruction algorithms have been refined and improved.



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The IBL improves the track extrapolation resolution with respect to the Pixel detector of Run 1 by providing an additional high-precision hit closer to the interaction point. This is particularly important for low $p_{\mathrm{T}}$ particles, where it mitigates the effect of multiple scattering in the detector material on the track extrapolation, thus improving the impact parameter resolution in both the transverse ($d_0$) and longitudinal ($z_0$) projections. The smaller pixel pitch of the IBL in the longitudinal direction contributes to improving the resolution in $z_0$ across the full $p_{\mathrm{T}}$ spectrum.

The track reconstruction performance has been evaluated using Monte Carlo simulations of $t\bar{t}$ events, comparing the Run 1 detector geometry to a geometry including the IBL, while keeping all other conditions unchanged. An improvement in the $z_0$ resolution of approximately 2 (1.5) for tracks with $p_{\mathrm{T}}$ of 1 (100) GeV is observed following the addition of the IBL. In the transverse direction, the addition of the IBL improves the $d_0$ resolution by a factor of approximately 2 for tracks with $p_{\mathrm{T}}$ of 1 GeV, with the resolutions for the two geometries converging beyond 10 GeV. These results are confirmed by comparing the track impact parameter resolution measured in Run 1 (2012) data with that in Run 2 (2015) data [16].

In addition to the charged particle track reconstruction, these improvements enhance the primary vertex reconstruction and resolution, the secondary vertex finding, and the flavour tagging performance, hence considerably extending the physics reach of ATLAS analyses.

The IBL also helps to maintain the performance and robustness of the ID track reconstruction when the B-Layer read-out efficiency deteriorates at high peak luminosity, or after a large integrated luminosity (radiation damage to the sensors and front-end electronics as well as possible irreparable failures of its chips and modules).

The flavour tagging performance expected with the addition of the IBL is evaluated using a more realistic simulation of the ATLAS ID based on the final IBL geometry, an updated digitisation model and improved reconstruction algorithms with respect to the IBL TDR. The latter include a refined neural network clustering algorithm [17], a new tracking configuration, which improves the treatment of shared clusters in the core of a dense jet environment [18] and new flavour tagging algorithms. These results supersede those presented in the IBL TDR. Results are based on fully simulated $t\bar{t}$ production events at a collision energy of 13 TeV. The average level of pile-up is approximately 20, reflecting the Run 1 luminosity profile. Jets used for flavour tagging are reconstructed using the anti-$k_t$ algorithm [19] with radius $R = 0.4$. ATLAS combines the discriminating variables obtained from impact parameter, inclusive secondary vertex and multi-vertex reconstruction algorithms. A detailed description of these algorithms can be found in reference [20].

The combination of the input variables obtained from these algorithms is obtained using a boosted decision tree (MV2c20) [21]) that returns a continuum variable peaked around 1 for jets likely to contain a $b$-flavoured hadron and around $-1$ for those likely to originate from light-flavoured quarks. This MV2c20 is an evolution of the neural network algorithm used during Run 1 [20]. In order to perform an useful comparison, the MV2c20 algorithm has been separately re-trained for the $t\bar{t}$ sample generated using the ATLAS Run 1 geometry, without the IBL, and the ATLAS Run 2 geometry, which includes the IBL.

Figure 6 shows the light-jet and $c$-jet rejection as a function of the $b$-jet purity obtained with the two configurations. The addition of the IBL improves the light-jet ($c$-jet) rejection by a factor up to 4 (1.8) for $b$-jet tagging efficiencies up to 85%. Physics analyses will most often profit from the improved performance by re-tuning their $b$-tagging requirements in such a way to keep a



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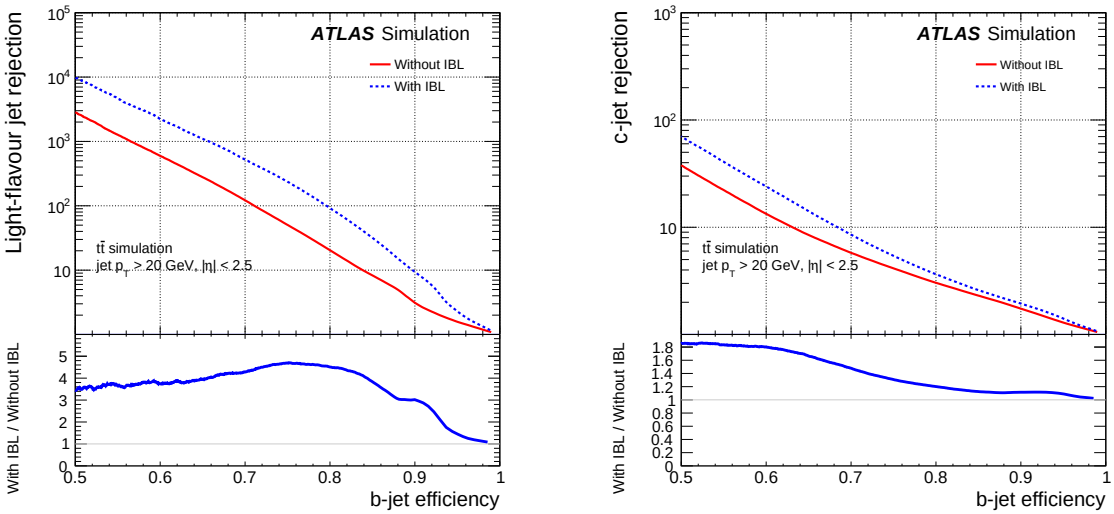


(a) (b)

**Figure 6.** Comparison of (a) light-jet and (b) $c$-jet rejection as a function of $b$-jet tagging efficiency for the Run 1 (without IBL) and Run 2 (with IBL) detector layouts under the same conditions, obtained with the MV2c20 algorithm. The rejection is defined as the reciprocal of the tagging efficiency. Results are derived from jets produced in $t\bar{t}$ events, with jets passing the $p_{\mathrm{T}} > 20\,\mathrm{GeV}$ and $|\eta| < 2.5$ selection.

similar background rejection with an increased signal efficiency. The improvement in performance at constant rejection is summarised in table 4 for different working points.

**Table 4.** Comparison of the $b$-jet tagging efficiency for fixed light- or $c$-jet rejection for the Run 1 (without IBL) and Run 2 (with IBL) detector layouts under the same conditions. Results are obtained for jets in simulated $t\bar{t}$ events satisfying $p_{\mathrm{T}} > 20\,\mathrm{GeV}$ and $|\eta| < 2.5$.

| light-jet rejection | $b$-jet efficiency without IBL (%) | $b$-jet efficiency with IBL (%) |
|---|---|---|
| 1000 | 57 | 65 |
| 100 | 71 | 79 |
| 10 | 84 | 90 |
| $c$-jet rejection | $b$-jet efficiency without IBL (%) | $b$-jet efficiency with IBL (%) |
| 20 | 56 | 62 |
| 10 | 63 | 68 |
| 5 | 72 | 76 |

The $b$-tagging performance as a function of jet $p_{\mathrm{T}}$ is shown in figure 7. The largest improvements are seen at low values of the jet $p_{\mathrm{T}}$ where the proximity of the IBL to the interaction region significantly reduces the impact of multiple scattering in the track reconstruction. The improvement



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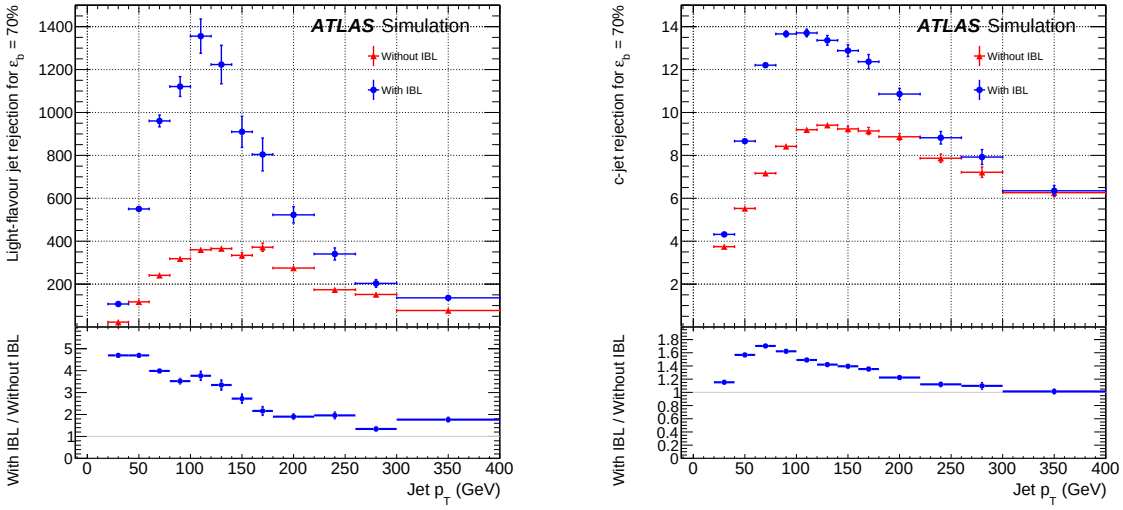
in light-jet ($c$-jet) rejection ranges reaches a factor 4 (1.6) for jet $p_{\mathrm{T}} \lesssim 100$ GeV while at higher $p_{\mathrm{T}}$ the tracking performance gain is limited by shared clusters from collimated tracks produced in the core of high $p_{\mathrm{T}}$ jets.




(a) (b)

**Figure 7.** Comparison of (a) light-jet and (b) $c$-jet rejection as a function of jet transverse momentum, while keeping the $b$-tagging efficiency fixed at 70% in each $p_T$ bin for the Run 1 (without IBL) and Run 2 (with IBL) detector layouts under the same conditions, obtained with the MV2c20 algorithm. The rejection is defined as the reciprocal of the tagging efficiency. Results are derived using jets produced in $t\bar{t}$ events and passing the $p_{\mathrm{T}} > 20$ GeV and $|\eta| < 2.5$ selection.

## 3 Modules

The basic building block of the IBL detector is the module. For each beam crossing an FE-I4B read-out chip records, digitises and locally stores the data from a silicon sensor that is connected to it. Two sensor technologies are used: planar and 3D. A planar silicon wafer contains four sensor tiles, each of nominal dimension 41 340 µm × 18 600 µm (41 315 µm × 18 585 µm in the production process after dicing). A 3D silicon wafer contains eight sensor tiles, each of dimension 20 400 µm × 18 700 µm. There are consequently two module types, planar and 3D:

- A planar module consists of a planar sensor tile connected to two FE-I4B chips. Each chip consists 26880 pixel cells having analog and digital circuitry arranged in a matrix of 80 columns of 250 µm pitch and 336 rows of 50 µm pitch. Each FE-I4B cell is bonded using Sn/Ag bumps to a corresponding cell of the planar tile;

- A 3D module consists of a 3D sensor tile connected to a single FE-I4B chip with each cell of the FE-I4B chip bonded to a corresponding cell of the 3D tile;

- A double-sided, flexible printed circuit (the module flex hybrid) connects the module to external electrical services.



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The sensor design, production and yield is discussed in section 3.1. This is followed by a discussion of the FE-I4B production and yield in section 3.2. The module hybridisation, that is the bump-bonding of the FE-I4B chip(s) and a wafer to produce a bare module, is made industrially. A module flex hybrid is then attached at module production sites to the bare module, prior to detailed performance studies of the final (dressed) module. The module hybridisation, the module flex hybrid connectivity and the final performance are described in sections 3.3 and 3.4. Finally, the overall module production yield is summarised in section 3.5.

### 3.1 Sensors

Two sensor technologies are used for IBL modules. The planar sensor is a development of the Pixel detector sensor design, with several improvements. Most notably, since the limited IBL clearance precludes sensor shingling along the staves (as in the Pixel detector), the inactive sensor edges are substantially reduced to minimise efficiency losses. The 3D sensor design [22] is a new technology developed for increased radiation hardness, and relies on columnar electrodes penetrating the substrate, reducing the drift path with respect to the planar approach while keeping a similar thickness and thus signal size. As discussed in detail in reference [9], both sensor types show satisfactory test-beam performance in terms of noise, hit efficiency and hit uniformity for a fluence of up to $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$. An effective inactive edge width of 215 µm (175 µm) was measured for planar (3D) sensors.

The planar $n^+$-in-n sensors have proven their excellent performance during the Run 1 operation of the Pixel detector and are a well-developed technology. Nevertheless, the 3D sensors have a potentially important advantage in terms of power consumption after high radiation because of their lower operating voltage.

Double-chip planar sensor modules cover the central region of the detector, 75 % of the active area, while the high $\eta$ regions are populated by single-chip 3D sensor modules. This mitigates the reduced efficiency measured for normal incidence in the region of the 3D sensor electrodes.

#### 3.1.1 Planar design

The design of the planar IBL sensor is an evolution of the Pixel detector sensor [4] with $n^+$-in-n pixels. The n-side segmentation matches in size the FE-I4B read-out electronics connected via bump-bonds; a guard-ring structure is placed on the p-side. The planar IBL double-chip sensors are produced at CiS,[4] using n-type wafers of 100 mm diameter and 200 µm thickness, with resistivity in the range 2 – 5 kΩ cm and a <111> crystal orientation. Each wafer contains four sensor tiles of mean dimension 41 315 µm × 18 585 µm after dicing. Details of the sensor design can be found in reference [23]. Key features include slim edges achieved by stretching the edge pixel size opposite to the guard-rings to 500 µm, possible in $n^+$-in-n sensors because of the double-sided process; this option was implemented after extensive studies of the sensor efficiency in the peripheral area [24]. The number of guard-rings was optimised based on a complementary study, which evaluated the breakdown behaviour after partial guard-ring removal [25]. Compared to the Pixel detector sensor, the number of guard-rings has been reduced from 16 to 13 and the cutting edge has been moved

[4] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt (Germany).



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closer to them, as indicated in figure 8 where the overall reduction of the inactive edge (from 1100 to 200 µm) is shown.

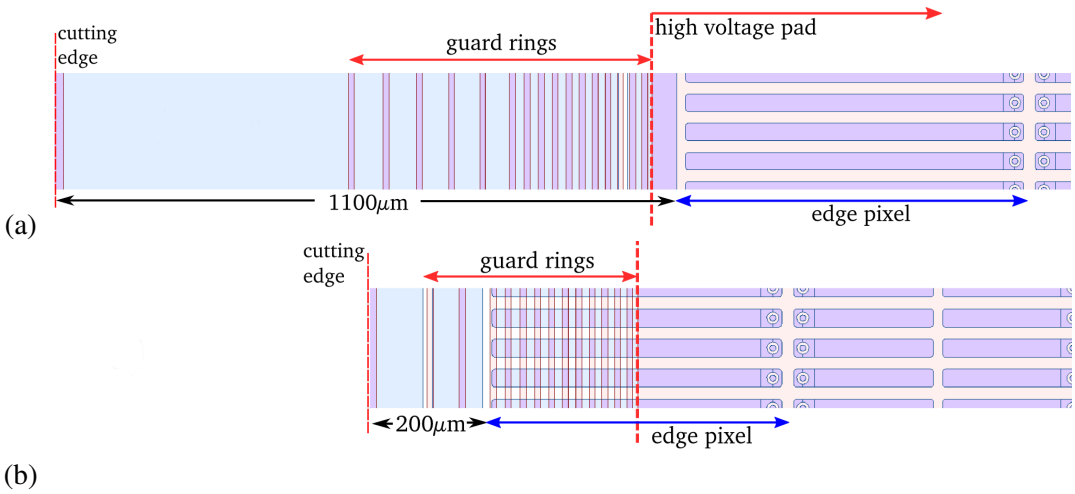


**Figure 8.** Comparison of the edge designs of (a) the ATLAS Pixel detector sensor and (b) the planar IBL pixel sensor. The inactive edge has been reduced from 1100 to 200 µm. Blue shades represent the n-implantation on the front-side of the sensor. Purple shades represent the blue n-implantation on the front-side of the sensor superimposed with red shading for the p-implantation on the back-side. The HV backplane area is metalised and is indicated by a dashed red line and arrow.

The nominal pixel size is 250 µm by 50 µm pitch, matched to that of the FE-I4B chip. The two central columns of these double-chip sensors are extended to 450 µm rather than 250 µm to cover the gap between the two adjacent FE-I4B chips.

### 3.1.2 3D design

In 3D pixel sensors, the columnar electrodes penetrate the substrate instead of being implanted on the wafer surface. The depletion electric field is therefore parallel to the wafer surface. The position and doping of the ~10 µm wide columns define the pixel configuration; the distance between electrodes can be typically fives times smaller than the ~230 µm sensor thickness, thereby dramatically reducing the charge-collection distance and depletion voltage. Although the fabrication process of 3D sensors is more complex, significant advantages can potentially be realised by independently controlling the drift distance and the sensor thickness. Because of the low depletion voltage, the power dissipation per unit leakage current is reduced. The cooling requirements are therefore less demanding. The signal size is determined by the sensor thickness, independently of the small drift distance. Furthermore, the drift perpendicular to the track direction results in fast signals, which are robust against charge trapping caused by heavy radiation damage [22].

The IBL 3D sensors were fabricated at FBK[5] and CNM[6] with a double-sided technology [26, 27]. Starting from p-type Float Zone wafers of 100 mm diameter and 230 µm thickness, with high-resistivity (10 to 30 kΩ cm) crystalline silicon and <100> orientation, columnar electrodes of 12 µm

[5]Fondazione Bruno Kessler, Povo di Trento (Italy).
[6]Centro Nacional de Microelectronica, Barcelona (Spain).



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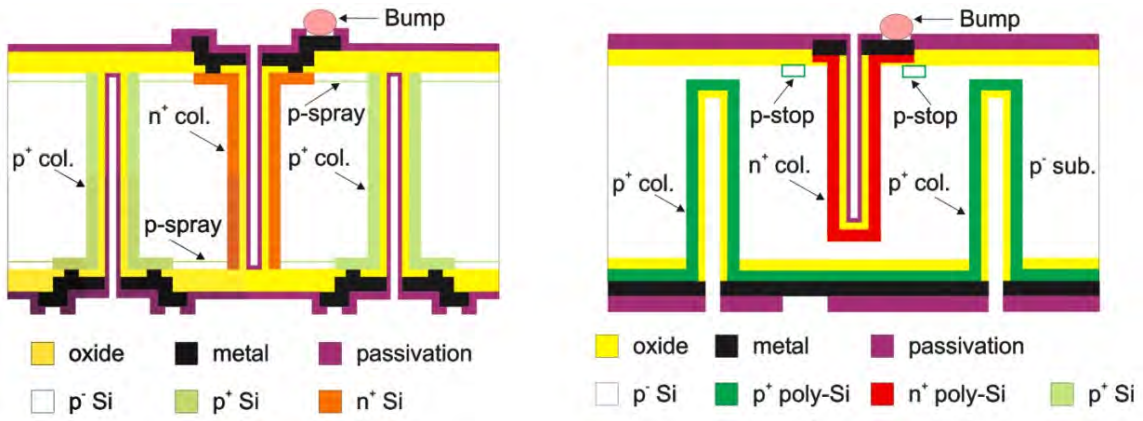
diameter were obtained by Deep Reactive Ion Etching (DRIE) and dopant diffusion from both wafer sides, without the presence of supporting wafers. By doing so, the substrate bias can be applied from the back side ($p^+$), as in planar devices. Figure 9 shows details of the 3D column layout.




(a) (b)

**Figure 9.** Design of the columns of (a) FBK and (b) CNM 3D sensors. This sketch is for illustration only and is not to scale.

Each pixel contains two read-out ($n^+$) columns (two-electrode configuration), with an inter-electrode spacing between $n^+$ and $p^+$ columns of ≈67 µm. In order to maintain a reasonable yield, each wafer contains eight sensor tiles of dimension 20.4 mm × 18.7 mm, rather than the four larger sensor tiles of the planar design. A 200 µm wide region separates the active pixel area from the physical edge of the tile.

The main differences between FBK and CNM 3D sensors are the following:

- FBK sensors have pass-through columnar electrodes [28]; in CNM sensors, on the other hand, electrode etching is stopped ~20 µm before reaching the opposite side [29];
- in FBK sensors, the surface isolation between $n^+$ electrodes is obtained by a p-spray layer on both wafer sides, whereas in CNM sensors, p-stops are used on the front side ($n^+$) only;
- the edge isolation in FBK sensors is based on multiple rows of ohmic columns stopping the lateral spread of the depletion region [30], whereas in CNM sensors a 3D guard-ring, surrounded by a double row of ohmic columns, is used to sink the edge leakage current.

Table 5 summarises the main parameters of the IBL sensors.

### 3.1.3 Sensor production and quality assessment

The electrical quality of the sensors was evaluated from the measurement of the current-voltage (I-V) dependence, as this is sensitive to bulk and surface defects. Tiles satisfying the selection criteria described below were chosen for hybridisation (connection between the sensor and the FE-I4B read-out electronics).



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**Table 5.** Summary of the main design specifications for the planar and 3D sensors of the IBL detector.

| Parameter | Planar | 3D FBK | 3D CNM |
|---|---|---|---|
| Tile dimension [$\mu m^2$] | $41315 \times 18585$ | $20450 \times 18745$ | $20450 \times 18745$ |
| Sensor thickness [μm] | 200 | 230 | 230 |
| Sensor resistivity [kΩ cm] | 2 – 5 | 10 – 30 | 10 – 30 |
| Pixel size (normal) [$\mu m^2$] | $250 \times 50$ | $250 \times 50$ | $250 \times 50$ |
| Pixel size (tile edge) [$\mu m^2$] | $500 \times 50$ | $250 \times 50$ | $250 \times 50$ |
| Pixel size (tile middle) [$\mu m^2$] | $450 \times 50$ | — | — |
| Edge isolation | Guard-rings | Fences | 3D guard-ring, fences |
| Pixel isolation | p-spray | p-spray | p-stop on n-side |
| Nominal operating bias voltage [V] (non-irradiated / $5 \times 10^{15}$ $n_{eq}/cm^2$) | −80 / −1000 | −20 / −160 | −20 / −160 |
| Maximum operational power [mW $cm^{-2}$] (−15 °C and $5 \times 10^{15}$ $n_{eq}/cm^2$) | 90 | 15 | 15 |

The planar design includes a grid structure that allows biasing of the entire sensor by means of a punch-through technique [31]. This bias grid was used to evaluate the quality of the tiles before the sensors were connected to the read-out electronics with the bump-bonding process. After bump-bonding the pixels were biased through the FE-I4B chip while the bias grid, connected to ground via a special bump in the periphery of the pixelated region, was not in operation.

The leakage current of the planar tile, evaluated at an operating voltage ($V_{op}$) 30 V below the depletion voltage ($V_{dp}$), was required to be $I(V_{op}) < 1$ μA, and the slope of the I-V curve was limited to $I(V_{dp} - 30\,V)/I(V_{dp}) < 1.6$. Wafers with two or more planar tiles that satisfied this requirement were sent for under-bump metallisation (UBM) and dicing at IZM.[7] The yield of the planar production (the percentage of planar tiles satisfying the above criteria) before under-bump metallisation and dicing was 90.6 %.

Due to the difficulty of implementing a bias grid structure compatible with the 3D design, alternative evaluation methods were developed for 3D sensors:

- FBK sensors include a metal grid connecting all pixels in each column to a pad located in the periphery of the active region. By measuring the I-V curves of the 80 columns with a specially designed probe card, the quality of each sensor on the wafer can be evaluated. The metal layer was removed by chemical etching after the I-V measurement and the wafers with three or more selected tiles were sent to IZM for UBM and dicing. The sensors that passed the selection criteria were bump-bonded to read-out chips. The sensors were required to have a breakdown voltage $V_{bd} < -25$ V, $V_{dp} > -15$ V and $I(V_{op}) < 2$ μA where $V_{op} = V_{dp} - 10$ V. The slope of the I-V curve was also constrained to satisfy $I(V_{op})/I(V_{dp} + 5\,V) < 2$. The sensor yield of the FBK production on the selected wafers was 57 %.

[7] Fraunhofer IZM, Gustav-Meyer-Allee 25, 13355 Berlin, Germany.



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- The CNM sensor selection criteria were initially based on the leakage current measured through the 3D guard ring structure surrounding the pixelated area. While the p-side of the wafer was biased, the 3D guard ring was connected to ground via a dedicated pad, and the I-V curve was measured for each sensor before the wafer dicing. After hybridization, the 3D guard ring was connected to ground through two special bumps of the FE-I4B chip. The CNM sensors were required to satisfy $V_{bd} < -25$ V, $V_{dp} > -15$ V and $I_{GR}(V_{op}) < 200$ nA with $V_{op} = V_{dp} - 10$ V. $I_{GR}$ is the leakage current measured on the 3D guard ring. The slope of the I-V curve was required to satisfy $I(V_{op})/I(V_{dp} + 5\,V) < 2$. Wafers with at least three sensors passing the selection criteria were sent to IZM for UBM and dicing. Initial studies indicated a good correlation between $V_{bd}$ measured through the 3D guard ring structure and that after detector assembly [9]. However, during module assembly, the correlation proved to be poor, with several CNM 3D modules showing a low $V_{bd}$. This was because of defects located in the central volume of the sensor that do not affect the region probed by the 3D guard ring.Once this lack of correlation was established, all CNM sensors that were not assembled were re-tested on a probe station. The n-side of the sensor was placed in contact with a grounded chuck via the under-bump metallisation (section 3.3.1), while the p-side was connected to the bias potential. Those sensors satisfying $V_{bd} < -25$ V were selected for hybridisation. The sensor yield of the CNM production on the selected wafers, as measured with the 3D guard ring method, was 72 %. However, after re-testing, the final CNM production yield was similar to that for FBK wafers.

The typical sensor I-V behaviour of prototype sensors was previously detailed before and after radiation [9, 23]. Typical I-V curves for each sensor type are shown after module assembly in section 3.4.1.

## 3.2 On-detector electronics

### 3.2.1 The FE-I4 front-end chip

The FE-I4B front-end chip was developed for the IBL read-out. A first version, the FE-I4A [8, 32], was fabricated in 2010 and used to develop and validate the IBL module design [9]. The FE-I4A was not intended for the final detector and the pixel matrix was non-uniform to allow performance comparisons between various analog circuit design choices. The FE-I4B chip was first fabricated in 2011 [33, 34] and tailored to fully meet the IBL requirements. In addition to selecting the analog design and making the pixel matrix uniform, specific powering choices were made and data acquisition features added.

The FE-I4A and FE-I4B both contain read-out circuitry for 26 880 hybrid pixels arranged in 80 columns of 250 µm pitch by 336 rows of 50 µm pitch. Each FE-I4 pixel contains a free running clock-based amplification stage with adjustable shaping, followed by a discriminator with an independently adjustable threshold. The chip keeps track of the time stamp for each discriminator as well as the 4-bit Time over Threshold (ToT).[8] Information from all firing discriminators is kept in the chip for a latency interval programmable up to 255 LHC clock cycles of 25 ns, and is retrieved if a trigger is supplied within this latency. The IBL data output is a serial Low Voltage Differential

[8]The Time over Threshold is defined as the time the amplifier output signal stays above threshold, measured in units of the LHC clock (25 ns). This quantity is related to the collected charge.



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Signal (LVDS), 8b/10b encoded at a rate of 160 MBit/s. The chip has many configurable settings that are stored in triple-redundant registers providing the required radiation hardness to single event upsets (SEU) [35].

Because of space and material limitations, the IBL FE-I4B chips are powered from a single DC supply over long cables providing a resistive load. The single voltage feeds two Shunt-LDO[9] voltage regulators [36, 37] drawing a minimum standing current of 270 mA even when the chip is neither clocked nor configured. This limits the amplitude of voltage transients resulting from current changes on the resistive supply lines, particularly important since the difference between the nominal and maximum input voltage ratings is small. The regulators and attendant voltage references have an input voltage limit of 2.5 V, compared with nominal operation at 1.8 V. Once the chips are configured and clocked, and their internal current draw exceeds 270 mA, the regulator shunt elements shut off and draw no additional current. The chip operates internally with two voltage rails generated by the regulators, nominally 1.4 V for the analog circuitry and 1.2 V for the digital circuitry. Both voltages are adjustable with a hard-wired maximum around 1.5 V (which varies slightly from chip to chip). The voltage references use a combination of a programmable current reference (feeding a poly-silicon resistor) and a fixed voltage reference. This combination was chosen to allow reliable start-up at low temperature (as low as −40 °C), as well as excellent stability (< ±2 %) up to high radiation dose (250 MRad).

Several features important for IBL operation were introduced in the FE-I4B design following experience with prototype FE-I4A modules. Some details of the analog bias distribution and charge injection were changed to correct for degradations observed in the FE-I4A after the expected IBL lifetime dose, particularly at low temperatures. A programmable event-size limit was introduced to avoid data acquisition time-outs from occasional pathologically large events. Bunch crossing and trigger counters were increased to respectively 13 and 12 bits, to avoid ambiguities in tracking the state of each chip. Improved diagnostics were implemented to count and report any skipped triggers (the chip will skip any triggers received when the 16-bit trigger buffer is full).

#### 3.2.2 FE-I4B production and quality assessment

For the IBL production, 3060 FE-I4B chips on fifty-one 200 mm diameter wafers were tested. The data acquisition and handling were performed with a custom read-out system [4, 38]. A custom PCB was used to interface the read-out system hardware with a probe card, establishing electrical contact with 108 FE-I4B pads. All 60 chips of a wafer were probed with an average measurement time of 2.5 days. The goal was to identify FE-I4B chips that were suitable for the IBL and to measure their calibration constants. For chip calibrations it was necessary to make contact with dedicated FE-I4B pads not wire-bonded on the IBL read-out circuit. The chip calibrations were therefore only possible at wafer level. Two calibration constants of the internal charge injection circuit are shown in figure 10. The circuit distributes a voltage step to injection capacitors present in each pixel and is needed to tune the FE-I4B chips during IBL operation. On average for the accepted chips, the injected charge changes with the value (VDAC) of the injection circuit digital-to-analog converter (DAC) setting approximately as

$$\frac{\Delta Q}{\mathrm{VDAC}} = 6.05\,\mathrm{fF} \cdot 1.45\,\frac{\mathrm{mV}}{\mathrm{VDAC}} = 55\,\frac{\mathrm{e}}{\mathrm{VDAC}}$$

to provide a transfer function between the value of the DAC setting and the signal.

[9] A shunt combined with a **L**ow-**D**rop-**O**ut regulator.



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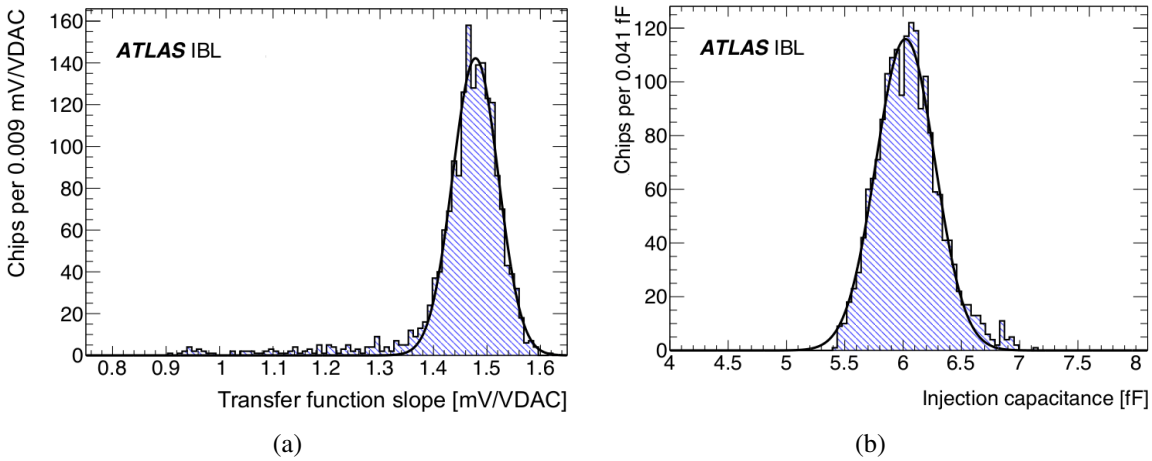


(a) (b)

**Figure 10.** Calibration constants of the internal charge injection circuit for accepted FE-I4B chips. The circuit distributes a voltage step to injection capacitors on board each pixel. The superimposed curves are Gaussian fits. (a) The slope of the transfer function between the signal voltage and the value VDAC of the DAC setting. (b) The measured injection capacitance.

More than 50 tests were used to evaluate the chip response to charge injection, the functionality of digital hit processing, the chip configurability, and the power consumption. Approximately 18000 values were recorded per wafer. A custom made software designed for wafer and module tests of the IBL production was used to automatically determine the chip status. The selection criteria were defined after the distributions of the first ten wafers were studied. A detailed description of the tests and selection criteria is available elsewhere [39].

Test results of 2814 fully probed chips are listed in figure 11. In addition, 246 chips (8 % of all chips) were not fully probed because of an anomalous high current at start-up (dead-shorts). Additional IDDQ,[10] Scan chain and Shmoo plot[11] tests were made by an external company for the first ~20 wafers, but the failure rate was low (less than 0.5 %). In total, 1821 chips (59.5 %) were qualified for IBL module assembly.

Since the powering scheme was not finalised at the time of wafer testing, the on-chip power regulators of the FE-I4B chips were only tested after the module assembly (section 3.4).

### 3.3 Module assembly

#### 3.3.1 Hybridisation of the FE-I4B chip and the sensor

The connection between sensor and electronics was achieved using fine-pitch bump-bonding and flip-chip technology. This was already used with a 50 µm pitch for the construction of the Pixel detector modules [4]. The IBL modules use a similar electroplated (SnAg) bumping process provided by IZM. The bumping process is divided into three steps: under-bump metallisation (UBM) on the sensor and FE-I4B wafers; solder bump deposition on the FE-I4B wafers; and a flip-chip of the diced FE-I4B chips and sensors. The UBM is necessary due to the non-solderable aluminium pads on the sensors and FE-I4B chips; the UBM metal stack consists of electro-deposited Cu on top of a sputtered Ti/W adhesion layer. Solder bumps are then deposited on the FE-I4B

[10] Measurement of the supply current (Idd) in the quiescent state.

[11] A plot showing the range of conditions (voltages, temperatures and inputs) in which the chip operates.



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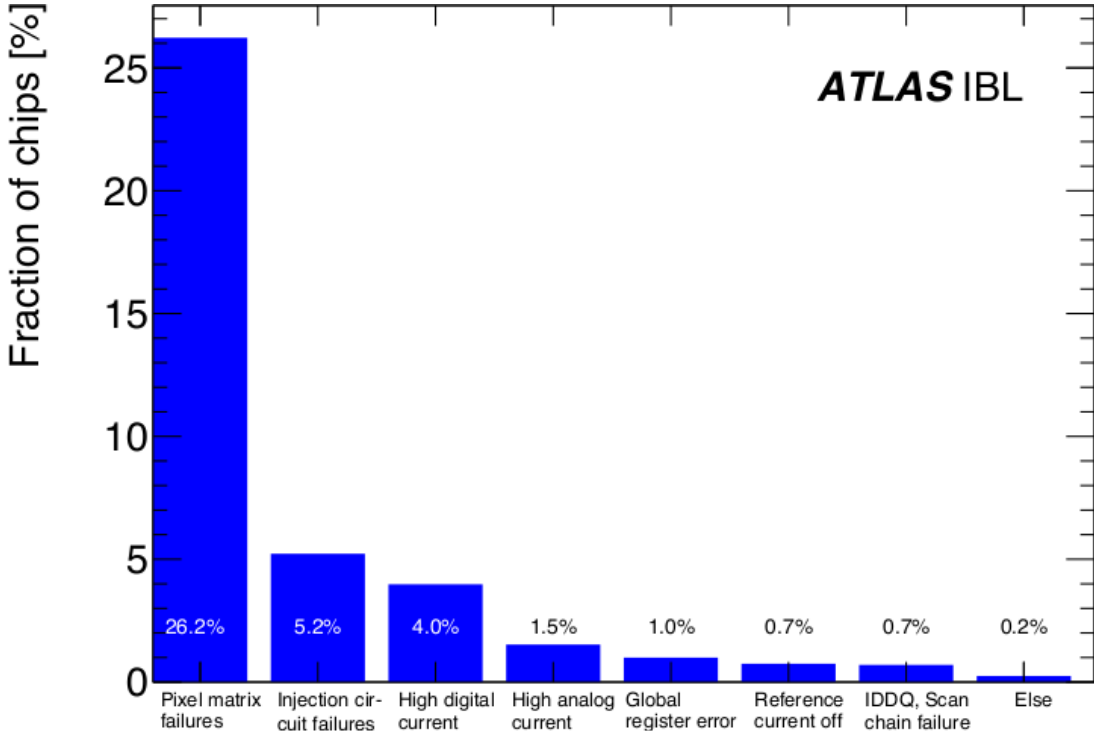


**Figure 11.** Failure modes leading to a rejection of FE-I4B chips before module assembly for 2814 fully probed chips. The bin *Pixel matrix failures* groups chips where the number of bad pixels were too high (>0.2 % failing pixels or >20 pixels per column). The bin *Injection circuit failures* groups failures (e.g. low maximum voltage, a non-configurable injection delay) that prevent using the charge injection for calibration during IBL operation. The bins *High analog/digital current* combine current measurements in different chip states (un-configured, configured, high digital activity). The remaining bins list the rate for chips failing the global register tests, the reference current generation tests and the Scan chain tests, respectively. All failure modes that are not explicitly mentioned contribute only 0.2 % and are included in the bin *Else* The failures are non-exclusive and are evaluated as a percentage of the probed chips.

wafers using electroplating only. The flip-chip operation follows the dicing of the sensor wafers. The FE-I4B chip is placed on the sensor substrate with high accuracy and the assembly is soldered to form the electrical and mechanical interconnection in a reflow soldering process. The sensor bonded to the FE-I4B chip(s) is commonly referred to as a bare module.

The procedure was modified with respect to that for Pixel detector modules, to suit the dimensions of the IBL module components. The FE-I4B chip covers an area of $20.27 \times 19.20\,\mathrm{mm}^2$ and was thinned to 150 µm before bump-bonding. Unconstrained, the thinned FE-I4B would undergo a distortion exceeding 40 µm during the high temperature reflow soldering phase, which would result in unconnected bumps especially in the outer areas of the assemblies. To avoid this, a temporary 500 µm-thick sapphire glass handle wafer was bonded to the FE-I4B chip before UBM. A polyimide bonding technique allowed a laser-induced debonding of the glass carrier at room temperature after dicing and flip-chipping. This debonding process used an UV excimer laser with a wavelength of 248 nm traversing the glass carrier to the bonding interface. The glass carrier was optimised to ensure that the laser light was fully absorbed in the polyimide bonding layer, thus releasing the FE-I4B chips.



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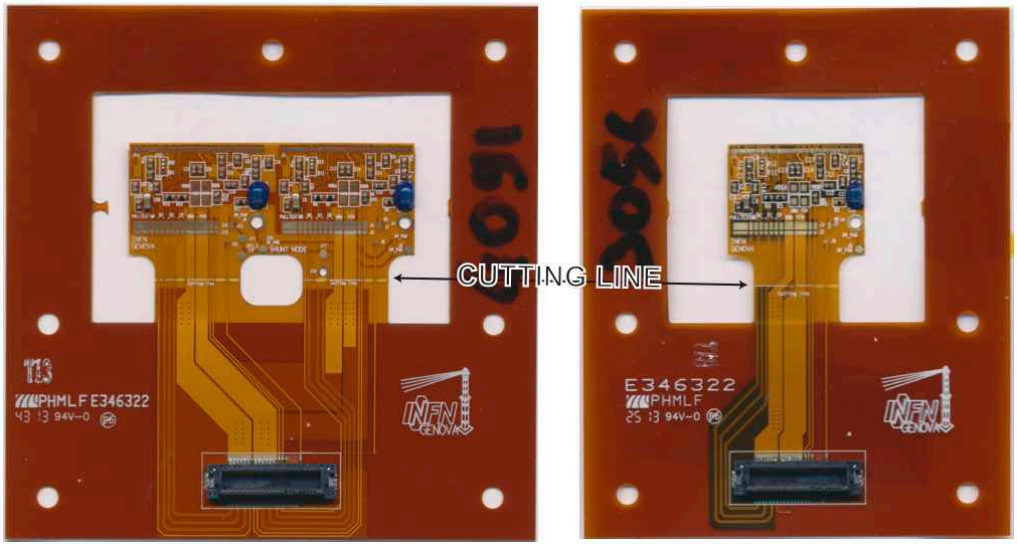
Only 2 mm of the chip length is dedicated to End-of-Column (EoC) logic outside the active pixel matrix. The size is determined by the need to wire bond the I/O and power pads to the read-out chip with the bump bonded sensor in place. The chip-level logic and global configuration occupy less than 20 % of the periphery. Once bonded, most of the EoC part extends beyond the sensor area so that the wire bonding pads at the output of the EoC logic are still accessible to connect the read-out chip via aluminium-wire wedge bonding.

### 3.3.2 Module flex hybrid

The module flex hybrid is a double-sided, flexible printed circuit board which routes the signal and power lines between the stave flex hybrid and the FE-I4B chips, holds the required passive components, and routes the bias voltage to the sensor via Cu traces. Figure 12 shows a photograph of the module flex hybrids for single-chip and double-chip modules. The envelope of the module flex hybrid is defined by the sensor dimensions and it is slightly narrower than the sensor width.




(a) (b)

**Figure 12.** Photographs of (a) a double-chip and (b) a single-chip module flex hybrid. The frame and flex extensions allow testing of the module before stave loading. The hybrid cutting line (see text) is visible as a white trace slightly outside the module envelope.

The module flex hybrids are glued to the back side of the sensor and connected to the longitudinal stave flex, which is located at the back side of the stave, via thin transversal wings, one per read-out chip (section 4.2). The 130 µm-thick flex stack consists of two 18 µm-thick copper layers embedded in dielectric polyimide sheets, glued with acrylic adhesive. Passive components are soldered on the module flex hybrid for the FE-I4B chip decoupling, power supply and HV filtering, and for terminations of the signal traces. The module temperature monitoring and interlock is made via a Negative Temperature Coefficient thermistor (NTC) mounted on the module flex hybrid. All passive components are soldered on the top layer of the module flex hybrid. Special emphasis is given to HV routing and filtering since the flex hybrid must be functional up to 1000 V. To avoid



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HV discharges, wider spacing between the HV traces and the data and LV traces is introduced. The HV capacitor is encapsulated with a polyurethane resin and 27 µm thick Kapton®[12] cover layers are used on the top and bottom of the flex hybrid.

All signal and power traces of the module flex hybrid are routed to a connector on a frame outside the module area that is used during the module production QA. A temporary wire bond connection is necessary to connect all signal and power lines from the flex to the connector on the frame. Prior to the loading of the module to a stave the connector area is cut away. The cutting line is approximately 1.5 mm from the sensor.

The module flex hybrids were produced by Phoenix S.r.l.[13] and the surface mount component loading and encapsulation was made by Mipot S.p.A.[14] Basic QA operations such as testing of line integrity for open and shorted connections were made by the vendors and were followed by more detailed tests at the two module assembly sites. These procedures included HV standoff tests at 1.5 kV, visual inspection and dedicated cleaning to allow for high-quality wire bonding.

### 3.3.3 Final module assembly

The final (dressed) module assembly was made at two module production sites in the period 2012 to 2014, following four assembly steps described below.

A detailed visual inspection of the module flex hybrid was initially made, together with electrical tests of the line and pad integrity, and the hybrid components. To ensure a good wire bonding performance, the flex hybrid was then cleaned in an ultrasonic bath, rinsed with distilled water, and dried. The visual inspection was then repeated.

A visual inspection of the bare module was made to identify scratches or other damage. For planar double-chip modules a re-measurement of the I-V was made to check the sensor quality. Thirteen planar modules (3.2 %) and eight 3D modules (2.9 %) were rejected.

The key assembly step is the alignment and attachment of the bare module and the module flex hybrid. The module flex is glued on the sensor back-side. For this reason, it is necessary to visually access the sensor alignment marks, and to be able to wire-bond to both the FE-I4 chip and the flex wings. An alignment precision of order 100 µm is required. The alignment and gluing procedure differed slightly between the production sites, and the detailed jig designs were developed autonomously. Separate alignment jigs were developed for the planar double-chip and 3D single-chip modules. Several jig sets were made to ensure production capacity, but the module assembly rate was in fact determined by the component supply. Both the module flex and the bare module were initially aligned on separate jigs using alignment marks, and fixed in place via vacuum. The module flex was then removed with a special jig, maintaining the alignment position but allowing access for the deposition of glue. The jig was designed to protect the hybrid components. Glue patterns were then deposited on the flex hybrid: a double tape strip (PPI RD-577F[15] or ARclad[16]) was placed

[12] Kapton® is a Dupont Corp. trademark for polyimide films, see http://www.dupont.com.
[13] Phoenix S.r.l., Via Burolo 22, 10015 Ivrea (Torino), Italy.
[14] Mipot S.p.A., Via Corona 5, 34071 Cormons (Udine), Italy.
[15] PPI RD-577F®, PPI Adhesive Products GmbH, see www.ppi-germany.de.
[16] ARclad®, Adhesives Research Corp., see www.adhesivesresearch.com.



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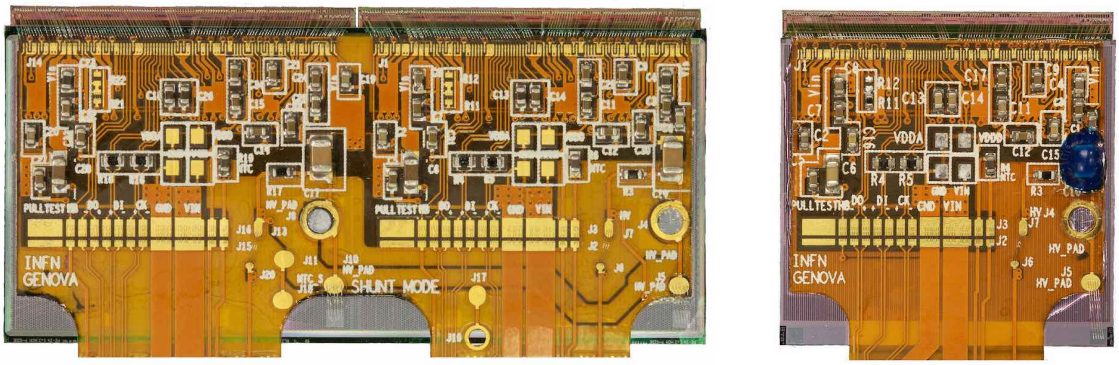
underneath the FE-I4B wire bond pads, and epoxy glue patterns (UHU EF 300[17] or Araldite 2011[18]) were placed under the remainder of the module flex hybrid, especially under the wire bond bridge area and the HV connection pads. The jigs were then aligned and brought into contact. Pressure was applied on the assembly, and in particular around the critical wire bond regions, during curing.

The final step was the wire bonding of the FE-I4B chip and sensor to the module flex hybrid and of the wire bond bridge to the test connector (section 3.3.2), using 25 µm-thick aluminium wire (at least three wire bonds were applied to the low- and high-voltage pads for redundancy and safety). Wire bond pull tests were consistently recorded to ensure the bond integrity.

At each stage of the assembly, details of the module components, as well as metrology and bonding information, were recorded. No site dependence of the module quality was identified.

Fully dressed planar (double-chip) and 3D (single-chip) modules are shown in figure 13. Table 6 summarizes the material budget (units of radiation length for normal incidence) of the IBL modules; the contributions of the different components are averaged over the active module area.

A total of 688 fully dressed modules (410 planar, 162 3D CNM and 116 3D FBK) were delivered for module testing, tuning and characterisation.




(a) (b)

**Figure 13.** Photographs of (a) an IBL planar module and (b) an IBL 3D module after the removal of the module handling frames. The HV encapsulation step is not yet made on the planar module.

### 3.4 Module performance and quality assurance

Prior to the loading of modules onto a stave, each module was tested to ensure its mechanical and electrical functionality, its tolerance to environmental stress, and its electrical performance. The performance validation identified both module-level failures and pixel-level failures. Modules were selected for stave loading on the basis of this validation and only modules passing all tests were selected. At the pixel level, any pixel that failed at least one electrical test was recorded and modules with a bad pixel count of more than 1 % were rejected. The bad pixel category also included bad pixels resulting from nonconformities such as re-work, sensor scratches or the chipping of electronic components.

[17]UHU EF 300®, UHU GmbH, see www.uhu.com.

[18]Araldite® is a trademark of Huntsman Advanced Materials, see http://www.huntsman.com/advanced_materials/a/Home.



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**Table 6.** Material budget of the IBL module components in units of radiation length ($X/X_0$) for normal incidence. The contributions of the different components are averaged over the active module area. Sub-components are shown in a separate column.

| | | $X/X_0$(%) |
|---|---|---|
| Total FE-I4B + bumps | | 0.21 |
| FE-I4B chip | 0.20 | |
| Bump-bonds | $\lesssim$0.01 | |
| Planar (3D) sensor | | 0.24 (0.27) |
| Total module flex hybrid | | 0.13 |
| Cu traces | 0.076 | |
| Polyimide/epoxy | 0.028 | |
| SMD components | 0.025 | |
| Total planar (3D) module | | 0.58 (0.61) |

An initial electrical verification, including the sequential room-temperature tests labelled Q in table 7, was performed after the module assembly. Modules accepted by this initial test were then subjected to an environmental stress test of 10 thermal cycles between −40 °C and 40 °C. The modules were not powered during the thermal cycles. Seventy-three modules (10.6 % of those delivered) were rejected at this stage because of major mechanical or electrical failure, a large fraction being due to a defective on-chip power regulator on the FE-I4B chips. As noted in section 3.2.2, the power regulators were not tested at the wafer level.

An extensive validation stage was then made for each module at both the module and individual pixel level. This included the sequential tests labelled F in table 7. The different measurements are described in sections 3.4.1 through 3.4.5.

A measurement of the sensor I-V was initially made at room temperature with a requirement on the breakdown voltage ($V_{bd}$) depending on the module type. Modules failing the $V_{bd}$ requirement were rejected. A detailed electrical calibration and characterisation was then made at the foreseen detector operation temperature of −15 °C. This included the module timing and threshold calibration and validations of the operational range (for example the low threshold operability). Finally, pixel-level failures, for example threshold tuning failures, bump-bond failures and noisy pixels, were identified and recorded. Forty-one modules (6 % of the delivered modules) were rejected following this detailed electronic validation. Accepted modules were ranked according to their quality, and as discussed in section 5.3, an additional penalty was applied to a module in case of mechanical rework or any other problems in the production and testing procedure.

### 3.4.1 Module I-V characteristics

The leakage current was measured as a function of the sensor bias voltage (I-V characteristic) during both the initial room-temperature electrical test and the full performance test. The breakdown



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**Table 7.** Test flow of the initial electrical test after module assembly (Q) and the intense module functionality and performance validation test (F). The tests labelled Q are made at room temperature.

| Test Name | Test Purpose | Test stage |
|---|---|---|
| Sensor current vs. applied bias voltage | Sensor operability and reference characteristics measurement | Q, F |
| Power-up test | Chip supply voltage and current test | Q, F |
| Shunt-LDO I/V scan | Shunt-LDO warm/cold calibration and functionality test | Q, F |
| Generic ADC test | Generic ADC warm/cold calibration and Shunt-LDO calibration verification | Q, F |
| Sensor bias ON | Ramp-up of sensor depletion bias | Q, F |
| Digital test (high threshold) | Pixel read-out chain functionality | Q, F |
| Module tuning | Multi-step threshold and feedback current adjustment (global and pixel level) | Q, F |
| Digital test (operation threshold) | Pixel digital read-out chain functionality | Q, F |
| Analog test (operation threshold) | Pixel analog read-out chain functionality | Q, F |
| Threshold and noise measurement | Threshold and noise (ENC) measurement | Q, F |
| ToT verification at the charge of 16 000 $e^-$ (MIP) | Charge measurement verification | Q, F |
| Crosstalk test | High analog charge injection for inter-pixel crosstalk test | Q, F |
| $t_0$-tuning | Injection timing fine adjustment | F |
| In-time threshold measurement | Threshold for hit detection within single bunch crossing measurement | F |
| ToT calibration | Full range ToT to charge calibration | F |
| Noise occupancy measurement | Noise hit probability at operation threshold and noisy pixel masking | F |
| Source scan | $^{241}$Am high statistics source scan for bump connectivity test | F |
| Low threshold operability test | Noise occupancy as function of threshold measurement | F |
| Sensor bias OFF | Ramp-down of sensor depletion bias | Q, F |
| Threshold and noise measurement | Threshold and noise (ENC) measurement with undepleted sensor to detect defective bumps | Q, F |

voltage ($V_{bd}$) was used as an acceptance criterion for the modules. Example I-V curves for ten randomly chosen modules of each module type are shown in figure 14a. From these curves, $V_{bd}$ can be determined. The I-V behaviour was measured with the FE-I4B chip unpowered and at approximately 20 °C. A current limit of −10 µA was used to protect the modules.



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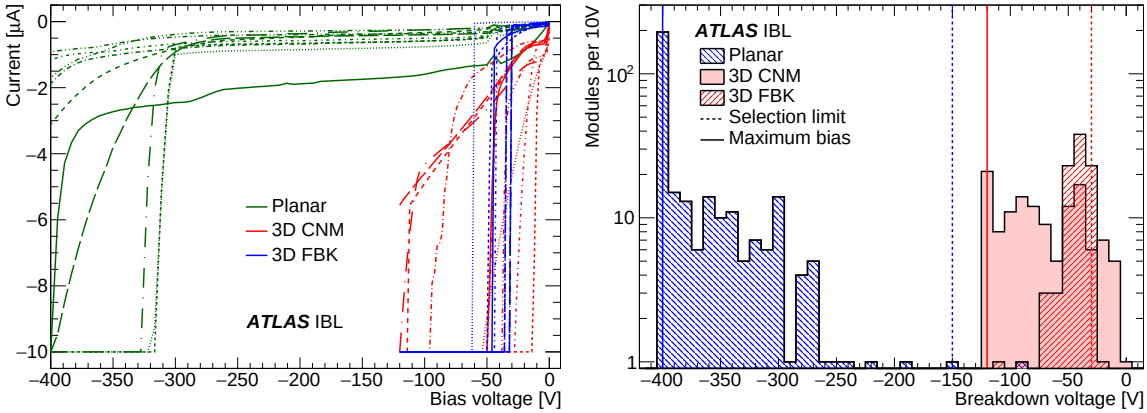


(a) (b)

**Figure 14.** (a) The I-V characteristics of ten randomly chosen modules of each sensor type. The I-V curves were measured at approximately 20 °C and a current limit of −10 µA was used to protect the modules. The FE-I4B chips were not powered. (b) The breakdown voltage ($V_{bd}$) distributions of the tested IBL modules (313 planar, 128 3D CNM and 93 3D FBK modules). The solid vertical lines indicate the maximum measurement point of −400 V for the planar modules and −120 V for the 3D CNM and FBK modules. The $V_{bd}$ acceptance criteria of below −150 V (blue) for the planar modules and below −30 V (red) for 3D modules are also indicated as dashed lines.

As shown in figure 14b, $V_{bd}$ depends on the module type. The $V_{bd}$ of planar modules was required to be less than −150 V, 70 V below the nominal bias voltage, $V_{op}$ = −80 V. Only four of the dressed planar modules failed the sensor breakdown voltage criterion. The $V_{op}$ of the FBK and CNM modules is −20 V, and for this reason all 3D modules having a $V_{bd}$ above −30 V at the final performance test were rejected. As already noted (section 3.1.3), the sensor test procedure at wafer level was significantly different for the CNM and the FBK modules. For the 3D FBK modules, only one module was rejected. However, for CNM modules, the correlation between $V_{bd}$ at wafer level and for dressed modules was poor. For this reason, the wafer-level criteria were relaxed and 27 of the dressed CNM modules failed the $V_{bd}$ requirement. Furthermore, in some cases, the early soft breakdown is thought to originate in the p-stop region around the n-columns. After radiation, the leakage current due to radiation damage in the silicon bulk dominates.

### 3.4.2 Module time-walk and threshold tuning

During detector operation, the IBL modules digitise the measured hits with respect to the master clock, which is synchronised to the LHC clock. Only hits that are recorded within one clock cycle, i.e. within a sensitive time of 25 ns, can be assigned to the correct bunch crossing of the LHC. The in-time hit detection probability is significantly influenced by the time-walk effect of the charge sensitive amplifier. Small signal charges at the input of the amplifier cross the discriminator threshold with some time delay with respect to a large reference charge and therefore the knowledge of this time-walk is important for the IBL operation.

To measure the time-walk, the time difference between the arrival time of the signal charge at the input of the amplifier and the time at which the amplifier output voltage crosses the discriminator threshold needs to be determined. During this measurement, the charge is generated by the on-



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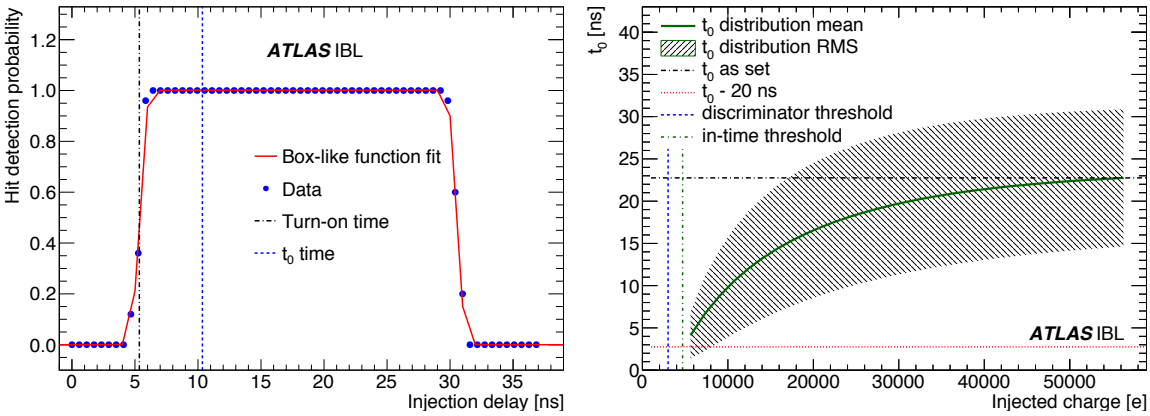
chip charge injection circuitry and thus the signal charge arrival time is determined by the charge injection time, which needs to be precisely measured and adjusted. The FE-I4B chip has adjustable on-chip chip-level injection delay circuitry that is used to tune the charge injection timing. The circuitry delays the injection timing globally with respect to the chip master clock, thus decreasing the time difference between the charge injection and the digitisation time window. The injection delay is scanned and the hit detection probability is measured as a function of the delay setting for a large injected charge, using a single clock cycle digitisation window. This results in a box-shaped function as shown in figure 15a for a single pixel, in this case for an injected charge of approximately 10 ke$^-$. The time difference between the master clock and the charge injection (i.e. injection delay) for a 50 % hit detection probability is defined to be the hit detection time. The difference between the hit detection time for two consecutive digitisation windows is known to be 25 ns (one bunch crossing) and this is used to calibrate the step-width of the delay circuitry. The step-width of this particular FE-I4B chip is 0.58 ns. The mean hit detection time of the full pixel array is measured and the time $t_0$ is defined to be the mean hit detection time of the chip plus a safety margin of 5 ns to ensure that early pixel timings are not excluded.




(a) (b)

**Figure 15.** (a) The single pixel hit detection probability of one pixel of a typical chip during a $t_0$ scan with a high injected charge (approximately 10 ke$^-$), and (b) the measured mean $t_0$ as a function of the charge of the entire chip. Analog injections with high charge are performed as a function of the on-chip injection delay. Hits are digitised during a single cycle of the master clock of the chips. The hit detection time is determined using a box fit convoluted with a Gaussian shape (box-like). The $t_0$ is set to the hit detection time plus a safety margin of 5 ns. For the full pixel matrix the measured mean $t_0$ is shown as a function of the injected charge. The effect of the time-walk is visible for small charges.

The calibration of the internal injection timing was verified with reasonable agreement using charge pulses induced in a planar sensor using a picosecond 671 nm laser. The scanning procedure measuring $t_0$ is similar to that based on internal injection but with the injection time being controlled outside the FE-I4B chip, thus providing an important cross check.

As shown in figure 15b the value of $t_0$ measured as a function of the injected charge reveals the effect of time-walk. For high charges the mean $t_0$ saturates at a fixed delay. For small charges, closer to the discriminator threshold, $t_0$ is smaller, i.e. the time between charge injection and the digitisation time window is larger. Given the 5 ns safety margin added for early signals, the time-walk must not



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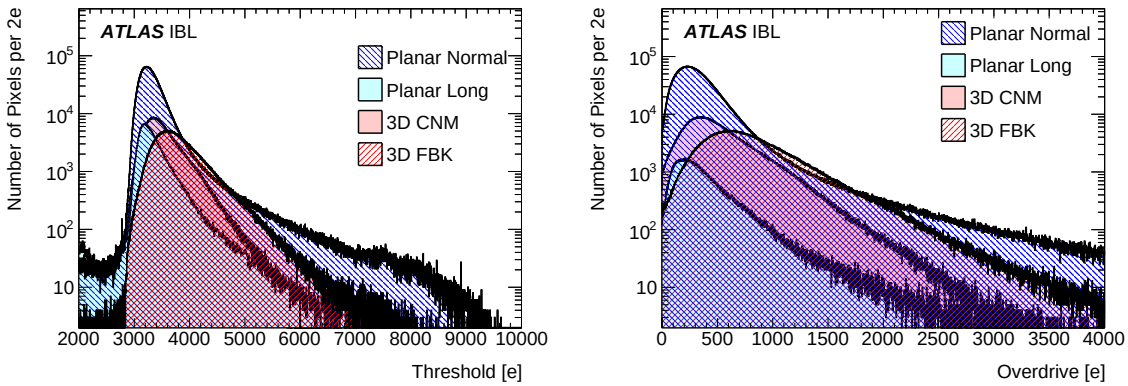
exceed 20 ns for an injected charge to be detected in the correct digitisation window, i.e. the correct bunch crossing. The time-walk can be related to the input charge in electrons using figure 15. The charge corresponding to 20 ns time-walk is called the overdrive, and the in-time threshold is the sum of threshold plus overdrive. Injected charges greater than the in-time threshold will be detected in the correct bunch crossing. Smaller hits will be 'out-of-time'. Out-of-time hits can be recovered with on-chip processing. In the FE-I3 chips of the Pixel detector, there is a function to duplicate all hits below a programmable ToT value to the prior bunch crossing, at the cost of a significantly increased data volume. The FE-I4B chip contains a more sophisticated recovery method that limits the impact on the data volume. Hits with a ToT value of 1 or 2 (optional and programmable) can be replicated in the previous bunch crossing assignment, if they are adjacent to a larger hit. This exploits the fact that low-charge hits are mostly due to charge sharing, since charged particles are unlikely to produce very low-charge single-pixel clusters.




(a) (b)

**Figure 16.** The distribution for individual pixels of (a) the in-time threshold and (b) the charge overdrive above the discriminator threshold needed for the hit to be detected within one bunch crossing. All modules matching IBL quality criteria are shown. The overdrive is measured after tuning the modules to 3000 $e^-$ threshold and 10 ToT counts for a charge injection of 16 $ke^-$ at approximately −15 °C. The mean in-time threshold varies between 3354 $e^-$ for the normal planar pixel and 3820 $e^-$ for the 3D FBK pixel. Pixels failing the measurement are not included in the distributions, and pixel overflows are not shown.

The tuning algorithm used to generate the initial module configurations included a global threshold adjustment, a module feedback current and threshold tuning, and a final iterative pixel-level feedback current and threshold tuning. The threshold was measured using a known injected charge and measuring the 50 % hit efficiency, initially at the global level and then at the pixel level. The mean value for each FE-I4B chip was tuned to be 3000 $e^-$ at a nominal temperature of 22 °C.

The in-time threshold can also be measured using a threshold scan algorithm with a single bunch crossing read-out, following a $t_0$ adjustment. Therefore, the time-walk could be measured during the IBL module production using the so-called overdrive measurement (calculated for each pixel as the difference of in-time threshold and the discriminator threshold). Both the in-time threshold and the overdrive distributions are shown in figure 16. The in-time threshold distributions show the expected dependence on the sensor type; the detector capacitance influences the rise-time of the amplifier and thus the mean time-walk. Similar to the noise distributions for the three module



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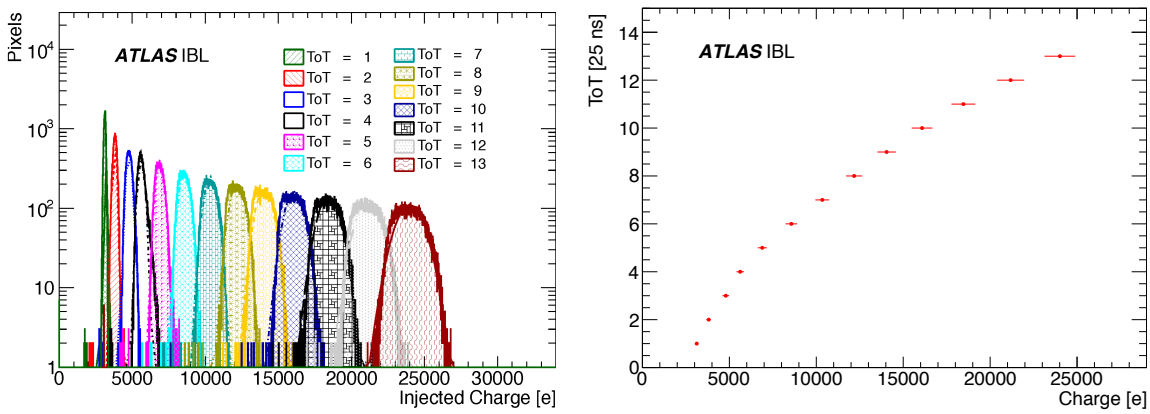
types, the overdrive distribution for planar modules (mean 355 $e^-$, RMS 250 $e^-$) has a lower mean than for CNM modules (mean 530 $e^-$, RMS 351 $e^-$) and FBK modules (mean 828 $e^-$, RMS 478 $e^-$). A small number of pixel channels in the tails of the in-time threshold distribution result from poorly determined threshold fits. These mean time-walk values are well within the out-of-time hit recovery capability of approximately 1500 $e^-$ for the FE-I4B chip [34].

### 3.4.3 Module ToT-to-charge calibration

The ToT is calibrated after the discriminator threshold calibration, as that affects the ToT along with the feedback amplifier current, and vice versa. The limited available charge information due to only four ToT bits complicates the ToT-to-charge calibration. A calibration method was implemented to measure the injected charge histograms for a specific value of the ToT. For each pixel the injected charge value is stored for the pixel that responds with the chosen ToT. This results in charge histograms as shown in figure 17a. The mean values and the widths of the distributions of injected charge are used as a look-up table for the charge-to-ToT calibration function (figure 17b). The measurement was made on each IBL module, initially for a given chip and then at the pixel level, and the result was stored for each pixel. Because of the maximum injected charge, the ToT $\geq$ 14 distributions were biased, and excluded from the calibration.




(a) (b)

**Figure 17.** Calibration function of the Time-over-Threshold (ToT) to charge: (a) for a given ToT value, the mean injected charge of each pixel, and (b) the charge-to-ToT calibration function. Measurements of the charge distributions for ToT $\geq$ 14 were biased by the maximum injected charge and were excluded from the calibration.

### 3.4.4 Module electronic noise

The average noise of a single pixel is measured in units of Equivalent Noise Charge (ENC).[19] The pixel noise is an important figure of merit for the pixel module performance. It is mainly determined by the capacitance at the input node of the preamplifier and by the leakage current. Both depend on the sensor type. In addition, the noise (ENC) can be affected by external parameters such as the module flex hybrid circuit quality and the power supply stability. No influence of the IBL

[19]Noise is usually measured in charge units and is defined as the charge necessary at the input of an amplifier to generate the same output signal as the observed noise. This quantity is called Equivalent Noise Charge (ENC).



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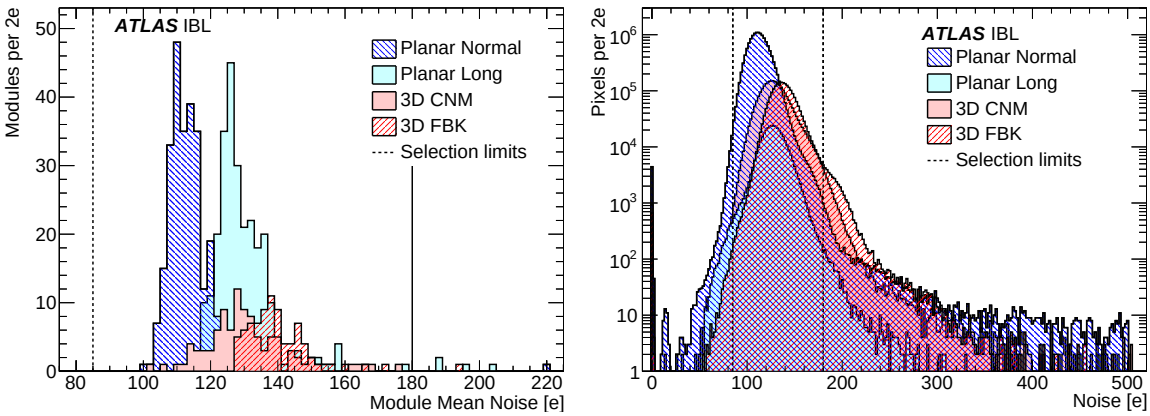
powering mode using the on-chip regulators is expected [37]. The noise (ENC) is evaluated from measurements of the pixel occupancy as a function of injected charge in the vicinity of the threshold value (the so-called S-curve method), using the same injected charge circuitry as that used for the pixel ToT calibration and threshold tuning. Figure 18a shows the mean noise (ENC) measured for each module during the full electrical test. The minimum and maximum selection limits for the mean module noise are shown by vertical lines. Figure 18b shows the noise (ENC) measured for individual pixels. The minimum and maximum selection limits for the noise of individual pixels are shown by vertical lines. Only 0.6 % of the pixels fail this selection and are flagged. The 3D modules have a higher noise (respectively 140 $e^-$ and 131 $e^-$ for FBK and CNM modules) in the same tuning condition as the planar modules (114 $e^-$). This is expected because of the higher pixel capacitance of 3D sensors. The RMS width of all three distributions is comparable and ranges from 30 $e^-$ to 70 $e^-$.




(a) (b)

**Figure 18.** For all modules matching the IBL quality criteria, (a) the module mean noise (ENC) distribution, and (b) the individual pixel noise (ENC) distribution. The modules are tuned to a 3000 $e^-$ threshold, and 10 ToT counts for a charge injection of 16 $ke^-$, at a nominal operating temperature of −15 °C. The minimum and maximum selection limits for the mean module noise (a module selection criterion), and for the noise of individual pixels (a bad pixel criterion), are shown as vertical lines in each figure. Plot overflows are not shown.

### 3.4.5 Module bump-bond connectivity and individual pixel failures

Scans to reveal possible bump failures were made at the level of individual pixels. These scans included threshold and noise measurements without the sensor bias applied, crosstalk measurements and $^{241}$Am source measurements.

As noted in section 3.5, the initial production batches suffered from a very high bump-bonding failure rate, as determined during threshold and noise measurements at the initial test phase. Production was halted until the problem was solved.

An $^{241}$Am source scan was made on each IBL module in the final test sequence and proved to be the most reliable test for open bump-bond detection. Based on the individual pixel hit rate with respect to the average hit rate per pixel for each module type, noisy pixels could be identified. Remaining bump-bonding failures could also be identified as resulting from shorts (or high electronic coupling) or open bumps. Figure 19 shows the fraction of failed pixels for each module in the



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final source test. Pixels with less than 5 % or more than 450 % of the mean pixel occupancy were considered as failing. A total of 19 modules had more than 1 % of bad pixels and were rejected.

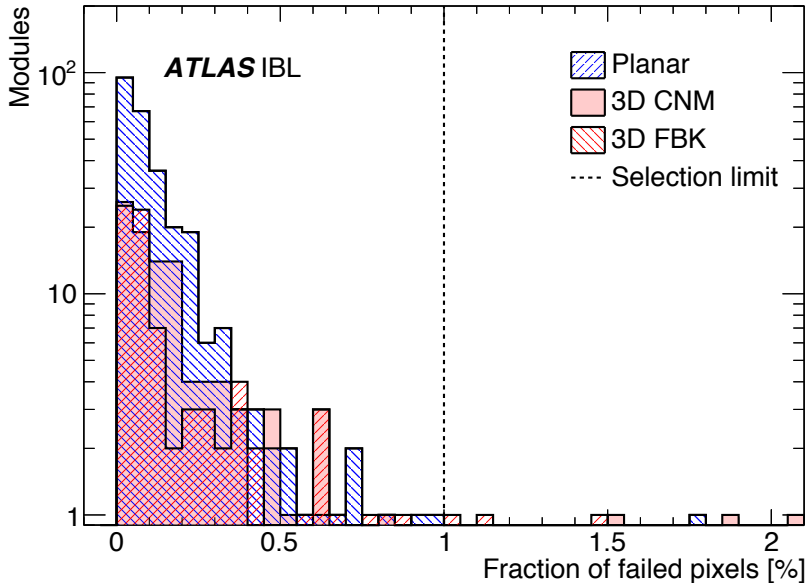


**Figure 19.** The distribution of the fraction of pixels failing the occupancy criteria in a $^{241}$Am source scan. Only modules otherwise accepted for stave loading are included. The modules are tuned to a 3000 $e^-$ threshold, and 10 ToT counts for a charge injection of 16 $ke^-$, at a nominal operating temperature of −15 °C. A pixel is counted as failing if it has less than 5 % or more than 450 % of the module's mean pixel occupancy. The selection limit is shown as a vertical line. Overflow entries are not shown.

After each test of an individual failure mode, failing pixels were counted (with no double counting for multiple failures). The fraction of pixels that failed in any test is shown in figure 20 for all modules. This fraction was required to be less than 1 % during the module production QA and was used as a basis for the final module selection. The mean fraction of failing pixels for accepted planar modules was 0.56 %. The mean fraction of failing pixels for CNM (0.44 %) and FBK (0.68 %) modules is comparable to the planar module distribution.

Occupancy distributions, measured using a $^{90}$Sr source after the loading of modules onto staves, are shown for each sensor type in section 5.2.5.

### 3.5 Module production and yield

The IBL module production was started in July 2012 and completed in April 2014. Bare modules were delivered in batches of about twenty modules for each module type. Fully dressed modules were then assembled, tested in detail and selected according to the quality criteria described in section 3.4. Accepted modules were then sent to be loaded on staves as described in section 5.

After the production of the first module batches, a high bump-bonding failure rate was observed and the module production was halted for approximately four months until the problem was understood and improved procedures were implemented. Two types of bump defects were identified: large areas of disconnected bumps and a small number of isolated bumps electrically shorted to a neighbour. During the production stop, both bump-bonding defects were investigated



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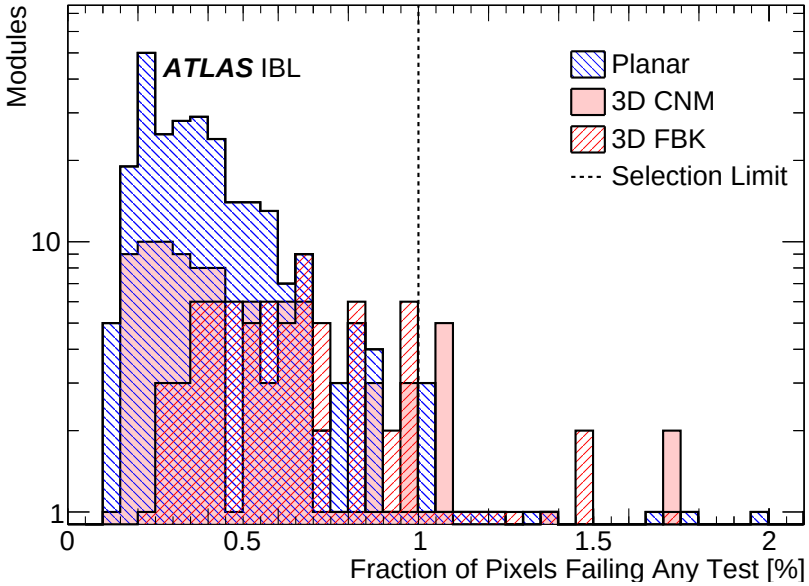


**Figure 20.** The distribution of the fraction of pixels failing in any test. Only modules otherwise accepted for stave loading are included. The modules are tuned to a 3000 $e^-$ threshold, and 10 ToT counts for a charge injection of 16 $ke^-$, at a nominal operating temperature of −15 °C. A pixel is counted if it fails any one of the tests as described in the text. The selection limit is shown as a vertical line. Overflow entries are not shown.

in detail in close collaboration with the bonding vendor. Both problems were traced to the usage of a flux during the soldering process: the disassembled sensors and FE-I4B chips of defective modules showed polymerised flux residuals that acted as a spacer during the reflow, preventing a proper bump connection between the sensor and the FE-I4B pixel. For shorted pixels the results were less conclusive but flux residuals in areas with larger number of shorts were also found. The solder flux applied to the FE-I4B chip prior to the flip-chip and reflow was replaced by glycerin as the new tacking media. With this new flip-chip method neither problem recurred.

Figure 21 summarises the IBL module production yield including the first batches where the bump-bonding problems were identified. In the figure the yield is expressed in terms of rejected modules, separately for planar, CNM and FBK modules. The yield is divided into different production batches (L1 to L5) with similar laser de-bonding and flip-chip methods applied. All modules assembled with the initial flip-chip method using solder flux are grouped in L1.

Another change during the module assembly concerned the laser de-bonding of the glass carrier. The initial vendor was replaced by a second vendor, which was qualified during the production; the first modules from this vendor are in batch L3 for the planar modules, and L4 for the FBK and CNM modules.

The production yield of the first batch L1 was poor for all module types because of the bump-bonding problems. Respectively 40 %, 20 % and 35 % passed the acceptance criteria for planar, CNM and FBK modules. For batches L2-L5, the yield improved to an average of 75 %, 63 % and 62 %, respectively. The initial modules coming from the second laser de-bonding vendor showed a higher rate of bump-bonding defects, mainly due to problems with the handling of the thin modules during and after the glass carrier removal. The bump-bonding failures result mainly from mis-



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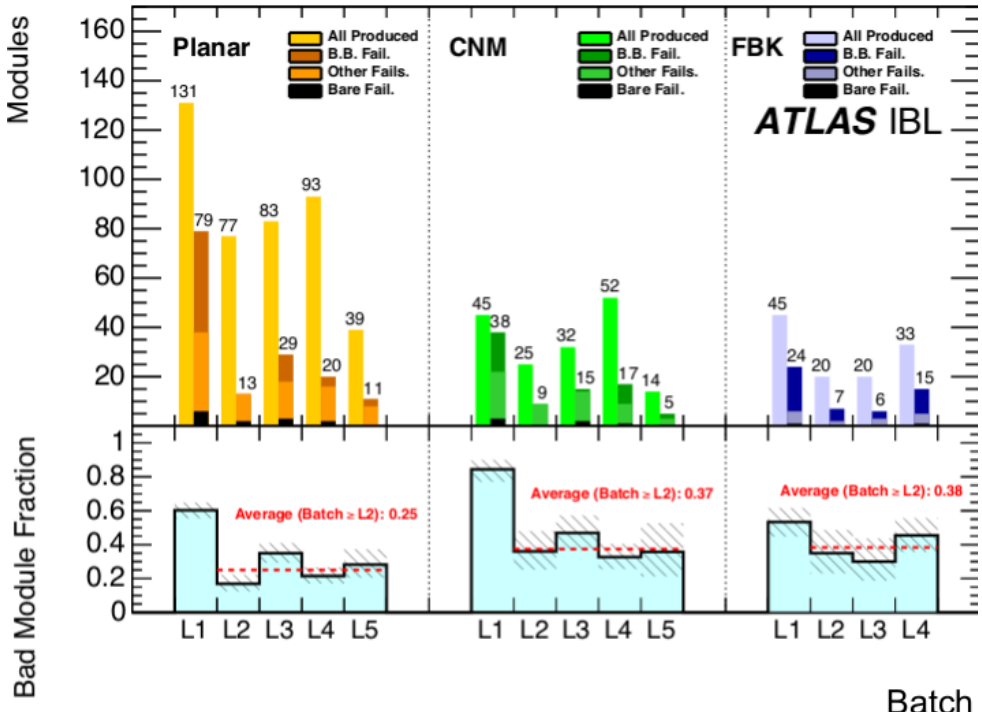


**Figure 21.** Fraction of rejected planar and 3D (CNM, FBK) IBL modules for the five production batches L1–L5. Within a given batch, a similar configuration of the laser vendor and the bump-bonding was applied. In the upper panel, *B.B. Fail.* denotes bump-bonding failures, *Bare Fail.* denotes modules that were not assembled due to (mainly) mechanical damage, and *Other Fails.* includes both electrical and sensor failures identified after assembly. In the lower panel, batch L1 was excluded from the mean rejected module fraction because of bump-bonding problems that were corrected in batches L2–L5. Including L1, the mean rejected module fraction for respectively planar, CNM and FBK modules was 0.36, 0.50 and 0.44.

handling during the laser de-bonding, and not on the sensor type. The mean failure rate was less than 10 % for planar and CNM modules, and 25 % for FBK modules. A summary of the failure rates, separately for the batches L1 and L2 –-L5 , is reported in table 8.

Other defects observed during the module production were mainly of mechanical or electrical nature. During the production a constant electrical failure rate of approximately 15 % was observed, mainly from the on-chip regulators, which were not tested during wafer probing of the FE-I4B wafers. Other electrical problems included failing double columns of the FE-I4B chip, and communications issues, but the rates were low. Several CNM modules in L2 and L3 showed problems with a low sensor breakdown voltage, due to insufficient testing procedures during the sensor wafer QA (section 3.1.3). CNM sensors used for the batches L4 and L5 were re-tested after UBM deposition and dicing and the yield improved slightly. However, this re-testing introduced new defects on the sensors' pixel side, increasing the bump-bonding failure rate.

The quality of each accepted module was characterised on the basis of:

- The number of bad channels, based on source scan results, digital tests and other analog measurements at the operating temperature;

- Electrical measurements such as the mean noise, threshold, noise dispersion, and the regulator voltages;



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**Table 8.** IBL module failures and the failure rate as a percentage of the bare modules delivered to the assembly sites. Failure modes are the same as figure 21. The failure rate is significantly larger for the first batch, as explained in the text.

| | Planar | 3D CNM | 3D FBK |
|---|---|---|---|
| Batch L1 | | | |
| Delivered bare modules | 131 | 45 | 45 |
| Bare module failures | 6 | 3 | 1 |
| Delivered dressed modules | 125 | 42 | 44 |
| Accepted modules | 52 | 7 | 21 |
| Bare module failures [%] | 5 | 7 | 2 |
| Bump-bonding (B.B.) failures [%] | 31 | 36 | 40 |
| Other failures [%] | 24 | 42 | 11 |
| Total failure rate [%] | 60 | 84 | 53 |
| Batches L2 –-L5 | | | |
| Delivered bare modules | 292 | 123 | 73 |
| Bare module failures | 7 | 3 | 1 |
| Delivered dressed modules | 285 | 120 | 72 |
| Accepted modules | 219 | 77 | 45 |
| Bare module failures [%] | 2 | 2 | 1 |
| Bump-bonding (B.B.) failures [%] | 6 | 9 | 25 |
| Other failures [%] | 16 | 26 | 12 |
| Total failure rate [%] | 25 | 37 | 38 |

- Mechanical anomalies or damage including non-conformal glue distribution, invisible alignment marks and reworked wire bonds.

The highest quality modules were placed closest to the interaction region.

## 4 Stave components

The IBL modules are supported and cooled by 14 staves, cylindrically arranged around the beam pipe axis, as described in section 2.1. Two symmetric multi-layer flexible circuits, the stave flexes, are glued on the back of the mechanical stave structure and route electrical services between individual modules and the EoS region. The design, production and QA of the bare staves and stave flex components, and their assembly until the loading of modules on the stave, are described.

### 4.1 The bare stave

The bare stave should satisfy several important design criteria: a low material budget to improve physics performance; an excellent module thermal performance to optimise the pixel signal-to-noise



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and to prevent thermal runaway; good mechanical stability for efficient tracking performance; and a low Coefficient of Thermal Expansion (CTE) of component materials to reduce the mechanical stress.

### 4.1.1 Bare stave material

The constraints of low material budget and high structural reliability for the bare stave has resulted in specific design and material choices. The stave is assembled from four main components (figures 22 and 23), together with thermally conducting epoxy:[20] a 1.7 mm external diameter titanium T40 cooling tube; a carbon foam section[21] to drain the heat flux; carbon fibre laminates[22] to reinforce the stave stiffness; and PEEK[23] elements to fix the stave on the IBL support.

Each of the stave components requires special manufacturing and precise machining techniques. For example, the carbon laminates require fabrication in an autoclave to obtain the required transverse thermal conductivity ($\kappa$). Because of the high critical pressure (73.8 bar at 31 °C) of the bi-phase $CO_2$ cooling system, the titanium cooling pipes must fulfill stringent pressure requirements, with a minimal 0.11 mm wall thickness. The total material budget of the bare stave is 0.62 % $X_0$. The contribution of each component is detailed in table 9 and the main properties of the materials used are summarised in table 10. Each stave has a length of 724 mm, measured between the end block fixation points, and a width of 18.8 mm.

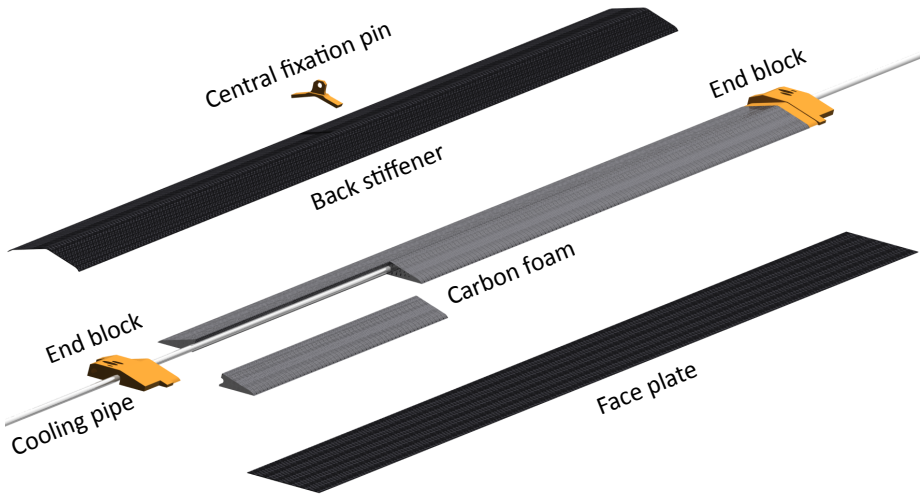


**Figure 22.** Exploded view of the bare stave with its main components: the cooling pipe, the carbon foam, the two carbon laminates (the face plate where modules are loaded and the back stiffener on the opposite side) and the PEEK elements (the central fixation pin and the end blocks).

### 4.1.2 Bare stave quality control and production

The bare stave production is a 13-step process that requires careful QA to ensure a uniform quality. The QA included a visual inspection to check for cracks or mechanical non-conformities, a weight

[20] Stycast 2850FT thermally conducting epoxy encapsulant, see http://www.henkel-adhesives.com/electronics.htm.
[21] K9 Carbon Foam, Allcomp Inc., see http://www.allcomp.net.
[22] RS-3/K13C2U uni-directional prepress, Tencate Advanced Composites, see https://www.tencate.com.
[23] Polyether-ether-ketone, VIRTEX® PEEK 450CA40, Victrex plc., see https://www.victrex.com/en/.



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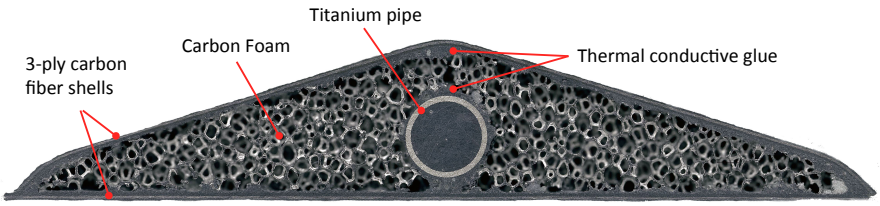


**Figure 23.** The transverse section of a bare stave.

**Table 9.** Properties and radiation length ($X/X_0$) of the bare stave components.

| Component | Material | Volume/stave ($cm^3$) | Equiv. Thickness (mm) | $X_0$ (cm) | $X/X_0$ (%) |
|---|---|---|---|---|---|
| Back stiffener | RS-3/K13C2U prepreg | 2.020 | 0.144 | 21.1 | 0.068 |
| Epoxy layers | Stycast 2850FT | 3.290 | 0.234 | 8.97 | 0.261 |
| Carbon foam | K9 | 21.600 | 1.536 | 213 | 0.072 |
| Cooling pipe | Titanium T40 | 0.411 | 0.029 | 3.56 | 0.082 |
| Face plate | RS-3/K13C2U prepreg | 1.903 | 0.135 | 21.1 | 0.064 |
| End-of-Stave fixation | PEEK 450CA40 | 2.510 | 0.178 | 25 | 0.071 |
| Central fixation | PEEK 450CA40 | 0.075 | 0.005 | 25 | 0.002 |
| Total: | | | | | 0.621 |

**Table 10.** The mechanical and thermal properties of the materials as used in finite-element modelling of the bare stave. The x-coordinate for the uni-directional RS-3/K13C2U fibre is along the fibre. The properties of the 0°/90°/0° fibre layup (not shown) are calculated from the input of uni-directional fibres, for a given fibre fill factor.

| Component | Density ($g/cm^3$) | Thermal Conductivity ($\kappa$) (W/mK) | CTE@20 °C (ppm/°C) | Young's modulus (GPa) | Tensile Strength (MPa) | Compressive Strength (MPa) |
|---|---|---|---|---|---|---|
| Titanium T40 | 4.51 | 16.4 | 8.6 | 102 | 430 | 340 |
| K9 carbon foam | 0.20 | 28.3 | < 1 | 0.293 | 3.6 | 1.8 |
| RS-3/K13C2U prepreg | 1.73 | ($x$) 96 | ($x$) -0.7 | ($x$) 410 | | |
| | | ($y/z$) 0.5 | ($y/z$) 15 | ($y/z$) 5.6 | | |

and metrology control, and a 150 bar pressure test and helium leak test for the cooling tubes. A total of 33 bare staves were produced, and a similar number of prototypes were built to verify the design performance and to tune the production process. Table 11 summarises the yield of the bare stave production.

The stave weight was systematically checked to control the manufacturing uniformity. The average stave weight of the 33 produced staves is (26 ± 1) g.

Given the very tight envelope requirements of the IBL, the bare stave planarity, ΔR, is an important factor that was controlled during the metrological survey. Deviations from planarity



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**Table 11.** The number of bare staves produced, and bare stave failures during QA.

| Bare stave characterisation | Quantity |
|---|---|
| Bare staves produced | 33 |
| Staves used as prototypes | 2 |
| Staves rejected after visual inspection | 7 |
| Staves rejected after metrology | 0 |
| Staves rejected after high pressure and He leak test | 0 |
| Staves accepted for stave flex assembly | 24 |
| Bare stave failure rate during QA | 27 % |

impact the module loading activity and the minimum gap between two adjacent staves around the beam pipe. The design specification required ΔR to be less than 0.25 mm along the stave length. Figure 24 shows the mean planarity on all produced staves, measured at 34 points along the stave profile and in three azimuthal positions as indicated in the stave profile shown in the figure ($\phi^-$ and $\phi^+$ at the stave edges, and $\phi^0$ at the centre of the stave). The staves have a slight undulated profile.

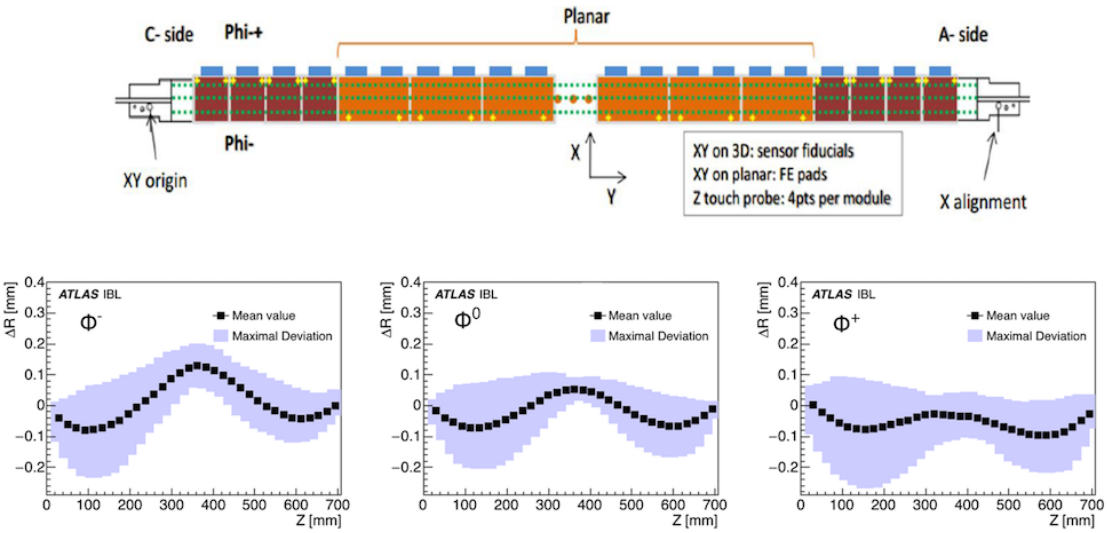


**Figure 24.** Summary of the planarity, ΔR, for the 33 production bare staves in three azimuthal positions as defined in the text: (a) $\phi^-$; (b) $\phi^0$; and (c) $\phi^+$.

### 4.2 Stave flex

The on-stave electrical service lines (the stave flex) connect each module of a stave to the Type 1 internal services at the EoS. The stave flex design presented unique mechanical and electrical challenges including:

- Space limitations force the services to be tightly integrated with the stave itself, with a 0.2 % $X_0$ design specification for the maximum amount of material averaged over the stave width;



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- High-quality transmission of 160 MBit/s data is required along the stave to the EoS, and subsequently 6 m from the EoS to the optical module (opto-board) at PP1;
- The operability of the FE-I4B over the full range of drawn currents requires that the round-trip low-voltage drop is less than 400 mV;
- Via interconnections are required between the Al and Cu layers.

#### 4.2.1 Stave flex layout

A single stave is served by two stave flexes, one from each side (A and C, see figure 3) and symmetric about the stave centre. The stave flexes run along the back-side of the stave, facing away from the interaction point. Each stave flex serves 16 FE-I4B chips and includes:

- 4 low-voltage (LV) supply lines, each serving 4 FE-I4B chips in parallel;
- 4 high-voltage (HV) supply lines, each serving either 2 double-chip planar or 4 single-chip 3D modules;
- 16 pairs of LVDS output lines;
- 8 pairs of LVDS data input and clock lines, each connected to 2 FE-I4B chips in parallel;
- 8 lines reading out 4 equidistant NTC (Negative Temperature Coefficient) sensors located on the module flexes.[24]

The stave flex, shown in figure 25, consists of a longitudinal section, a dog-leg part and a connector region, with a total length of 528.4 mm. The longitudinal section, approximately 350 mm long and 11.5 mm wide, is equipped with 16 identical wings that provide electrical and mechanical connections to the FE-I4B chips. The wing pitch of 20.75 mm corresponds to the inter-distance between FE-I4B chips in the planar modules, but is approximately 100 µm too short for 3D modules; this mis-alignment is corrected using angled wire-bonding between the wing flex and the module flex (section 3.3.2). Each wing is 17.5 mm long and 12 mm wide. Two ears at the edge of the wing ease the gluiing of the wing flex to the module during the integration phase. As the wing needs to be bent by 180° to be glued on the module, a row of small holes are drilled between the metallic lines to make the polyimide (Kapton®) more flexible. The dog-leg region creates a shift in both the radial and azimuthal directions, allowing services to be positioned in the correct location between cooling pipes in the EoS region. The connector region at the end of the stave is equipped with eight Panasonic AXT540124[25] SMD sockets.

The stave flex has six metal layers of which two are 50 µm thick Al traces used for the power and ground, and four have Cu traces; the stack-up is shown in figures 26 and 27. The total thickness is approximately 500 µm. Routing between layers is achieved using vias, which are described in section 4.2.2. Thin stiffeners are glued on the bottom under the connectors to ensure good connector

[24] All 3D (planar) modules carry one (two) NTC sensors mounted on the module flex hybrid. However, only four of the 16 NTC sensors are read out, to reduce the number of lines on the stave flex.

[25] Narrow 0.4 mm pitch 40-pin connectors AXT540124 (socket) / AXT640124 (header) from Panasonic Electrical Works, https://www.panasonic-electric-works.com.



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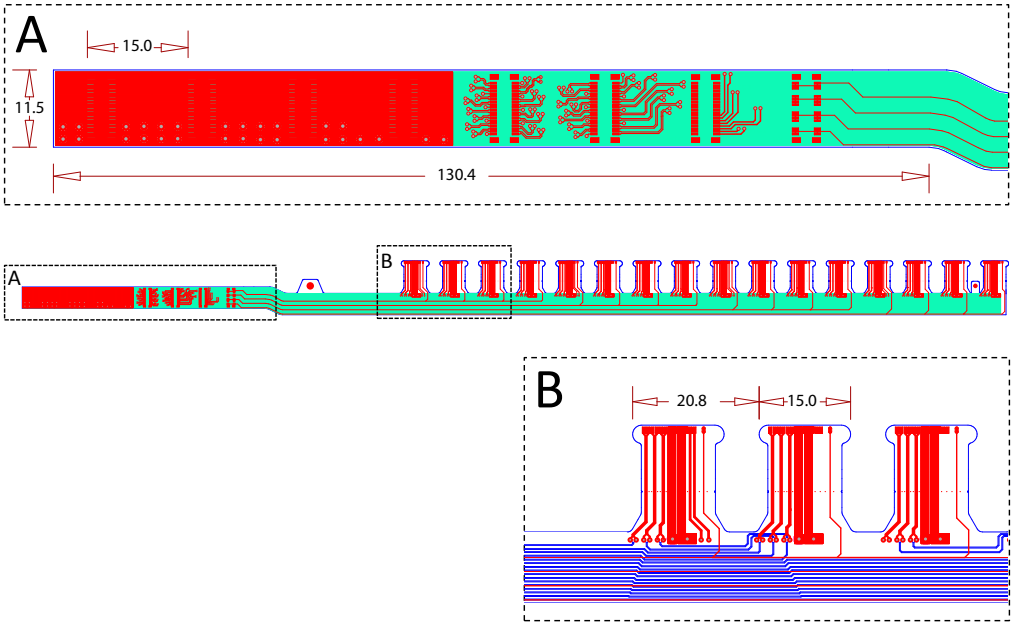


**Figure 25.** The layout of the stave flex: a zoom of the connector region (detail A) and part of the longitudinal section (detail B). The dog-leg section can be seen in between the regions A and B. All units are in mm.

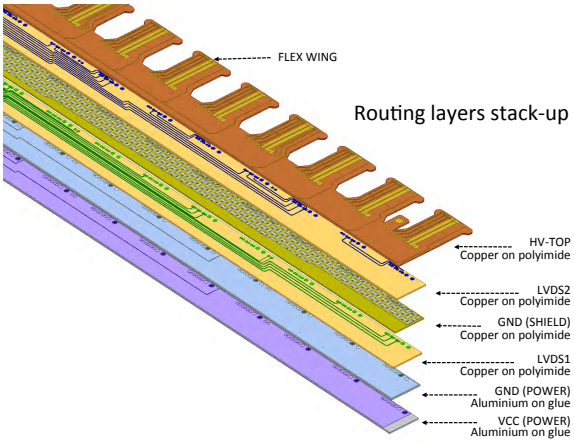


**Figure 26.** An expanded view of the overlapping layers in the stave flex.

insertion and removal reliability. The top metal layer is only used to route the HV signals, in order to maintain sufficient distance between the HV traces to guarantee 1.5 kV isolation. The signal and NTC lines are distributed on the LVDS1 and LVDS2 layers, but the layout differs for the A- and C-sides to ensure the same layout for the signal connectors at the EoS. The routing of LVDS traces has been optimized to avoid cross-talk and to have a controlled differential impedance of 80 Ω. To better control the impedance of the signal traces on the LVDS2 layer, a Cu ground shield is added below it. This 5 μm thick ground shield has a meshed structure optimised to maintain good electrical performance while minimising the additional material budget. The stave flex thickness



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averaged over its length and width is approximately 0.26 % $X_0$ with contributions from Al, Cu, polyimide and epoxy glue. The Cu contribution increases along the stave towards the EoS while the Al is almost constant along the stave length. The quoted material does not include the average ~0.034 % $X_0$ wing contribution. The contribution of the stave flex and the wings to the IBL material budget is approximately 0.21 % $X_0$, once smeared over the azimuthal angle. Details of the material contribution of the stave flex and wings are reported in table 12.

**Table 12.** Properties and radiation length ($X/X_0$) of the stave flex components, separately for the longitudinal section and the stave flex wings. *Thickness* is the effective thickness of the material layers for normal incidence; *Equiv. Thickness* and *Average* $X/X_0$ are respectively the thickness and $X/X_0$ normalised to the stave flex length; *Central* $X/X_0$ is the value of the material budget close to the central region, averaged over the stave width but without averaging along the stave length; *Smeared* $X/X_0$ is the *Average* $X/X_0$ smeared over a cylinder at the mean radius of the stave flex.

| Component | Material | Thickness (µm) | Equiv. Thickness (µm) | Average $X/X_0$ (%) | Central $X/X_0$ (%) | Smeared $X/X_0$ (%) |
|---|---|---|---|---|---|---|
| Stave Flex | Cu | 61 | 7 | 0.041 | 0.011 | 0.029 |
| | Al | 100 | 92 | 0.104 | 0.101 | 0.072 |
| | Polyimide | 163 | 163 | 0.057 | 0.057 | 0.040 |
| | Glue | 173 | 173 | 0.060 | 0.060 | 0.042 |
| Total Stave Flex | | 497 | | 0.262 | 0.230 | 0.182 |
| Wings | Cu | 19 | 3.8 | 0.024 | | 0.026 |
| | Polyimide | 38 | 21.4 | 0.007 | | 0.008 |
| | Glue | 10 | 5.6 | 0.002 | | 0.002 |
| Total Wings | | 67 | | 0.034 | | 0.036 |

The CTE of the stave flex is approximately 27 ppm/°C, which is significantly different from the almost zero value of the carbon stave structure. To ensure the mechanical integrity of assembled and loaded staves during thermal cycling, the stave flex is glued to the carbon structure (section 4.3.1).

### 4.2.2 The process flow

The stave flexes were produced at the CERN PCB workshop. The Cu and Al stacks (figure 26) were processed separately. The material used for the four Cu layers were two double-sided Cu-clad laminates on polyimide substrates, one used for the TOP/LVDS2 and the other for the GND/LVDS1 routing layers. The Cu and Al stacks are then laminated together.

A feature of the stave flex is the use of low-resistivity vias joining the GND/VCC Al layers to the TOP Cu layer. Following successive etching and deposition steps to create the Al/Cu vias, there is a deposition of 0.2 µm of Cr and 2 µm of Cu in the location of the power vias. The stave flex process is completed by:

- pressing together the Cu and aluminum stacks and drilling the power vias;
- 25 µm Cu electroplating of the power vias to connect the TOP layer with GND/VCC, followed by polyimide cover layers on the two stave flex sides;
- gold plating the bonding and soldering pads and cutting the stave flex to its final shape.



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The power and signal vias are shown in the cross-sectional view of the stave flex in figure 27. The final power vias have a typical resistance of 3-4 mΩ.

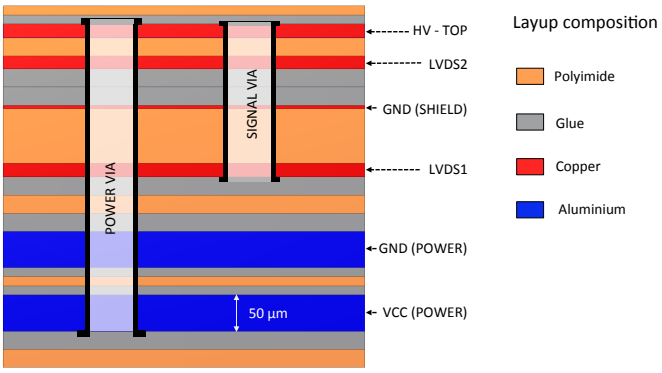


**Figure 27.** Cross-section of the stave flex showing the signal and power vias.

### 4.2.3 Quality control and production

The stave flex production was organised in batches of up to 4 sheets with three stave flexes each, all of the same type, either for the A-side or the C-side. After being diced and mounted with connectors, the flexes were cleaned and shipped to the qualification laboratory. The qualification consisted of:

- a visual inspection to identify mechanical damage and surface anomalies, and a first electrical test to check resistance measurements, continuity or shorts;
- the bending of the 16 stave flex wings on themselves (to allow later connection to the module flexes), with Araldite 2011 gluing on the back-side, followed by mechanical measurements and an electrical continuity test for possible broken lines, at room temperature;
- ten thermal cycles between −40 °C and 40 °C;
- an extended (one day) HV test at 1500 V with a current limit at 0.1 µA and a final electrical verification of resistance, continuity and shorts;
- a final visual inspection and sign-off for delivery.

Table 13 reports the stave flex yield. Six stave flexes were rejected during production by the vendor because of electrical or mechanical non-conformity, mainly at the beginning of the production. Two stave flexes were rejected because of a high resistivity of the LV via connection to the stave flex wings. The resistivity of the LV lines determines the round-trip voltage drop and a high inter-wing resistivity indicates a possible weak via connection. The voltage drop was uniform and typically ~320 mV for I = 2 A in the last batches, well within the 400 mV specification. Two staves were rejected because of non-conformities identified during the visual inspection, and one stave was rejected because of HV non-conformities. Finally, electrical tests were repeated at CERN before and after gluing the stave flexes on the stave. A small HV resistivity change was observed on one stave, but the stave flex was not rejected.



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**Table 13.** Failure rate of stave flexes during QA.

| Stave flexes | Number |
|---|---|
| Produced | 72 |
| Rejected during production | 6 |
| Rejected after visual inspection | 2 |
| Rejected after the electrical test | 2 |
| Rejected after the HV test | 1 |
| Rejected after the thermal cycles | 0 |
| Rejected due to mishandling | 0 |
| Accepted for loading | 61 |
| Total failure rate | 15% |

### 4.3 Bare stave and stave flex assembly

#### 4.3.1 Stave flex gluing

A pair of stave flexes is directly glued on the stave back stiffener with a procedure that was developed to meet stringent mechanical and thermo-mechanical constraints, for example the constraint of the stave envelope with an assembly accuracy of ±300 µm in the longitudinal direction and ±100 µm in the transverse direction, the thermo-mechanical characteristics of the two different materials and the minimisation of the material budget. Furthermore, the flexes must meet a radiation hardness requirement of 250 Mrad.

Following validation of the glue deposition process, radiation hardness and mechanical stiffness, Araldite 2011 glue, together with a polyimide wet etching for the stave flex surface, were chosen. Based on these tests, a Pyralux LF111[26] bond ply was added as a flex bottom layer in order to apply the glue to a 12.5 µm acrylic layer after surface treatment, rather than to the polyimide directly.

The above choice was validated with an ageing test using a production IBL stave glued with production stave flexes according to the final gluing procedure. Both thermal and radiation loads were applied to the assembly during the test while using a 10 MeV electron source. After approximatively 380 Mrad and 110 thermal cycles between 40 °C and −40 °C, no critical damage was observed on the stave-flex glue joint [40].

#### 4.3.2 Quality control of stave assembly components

During prototyping, one stave flex started to delaminate after several thermal cycles. A carbon clip was added to the design in order to prevent this problem. Out of 22 production assemblies built for the IBL, only one stave encountered a critical problem due to the glue mixture mistake, which led to a polymerisation failure. The remaining assembled staves underwent a QA procedure to fully

[26]Pyralux® is a DuPont Corp. trademark of a polyimide (Kapton®) substrate with a laminated or cladded layer of metal/adhesive, used for flexible PCBs, see http://www.dupont.com. In particular, Pyralux® LF111 coverlay is a polyimide film coated on one side with a proprietary acrylic adhesive.



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qualify the assembly before module loading. A summary of the assembled staves and their usage is detailed in table 14.

**Table 14.** Accounting of the produced and qualified bare staves.

| Staves | Number |
|---|---|
| Staves accepted for stave flex assembly | 24 |
| Staves used for system test prototypes | 2 |
| | |
| Staves assembled with stave flex | 22 |
| Staves rejected after stave flex assembly | 1 |
| Staves qualified for module loading | 21 |
| Staves loaded with modules | 20 |

As a first qualification step, the staves were visually inspected and the stave flexes were electrically tested to verify that the services were not damaged during the assembly process. The staves were then thermally stressed: an initial phase at 35 °C for 1 h was followed by 10 cycles of 1 h from 40 °C to −40 °C and finally a stabilisation phase of 3 h at 20 °C [41]. A metrology survey was made before and after thermal cycling to measure deformations of the mechanical supports by the flex gluing and to verify that the assembly still respected the required envelope. The stave planarity measurements, before and after thermal cycling, are summarised in figure 28 [41]. The planarity of one typical stave before and after flex gluing, and after thermal cycling, is shown in figure 29. As expected, due to the different CTE of the materials and the stave flexes being glued on just one side of the back of stave, the shape of the mechanical supports is affected by the assembly of the flexes and by the thermal cycling. Before thermal cycling, only four staves exceeded the specified bare stave envelope of 250 µm. After thermal cycling, the planarity is slightly deteriorated, but remains less than 340 µm and within the clearance after integration in the IST of ∼2 mm.

## 5 Stave loading and quality assurance

Twenty staves were loaded with qualified good modules. Details are provided in reference [41]. The QA procedure [42] provided a detailed characterisation of the stave including calibration in cold conditions and data taking with radioactive sources. Pixel defects were classified according to the type of failures observed in the FE-I4B chip, in the sensor and in the bump bonding. Two staves were accidentally damaged by an excess of humidity during the QA procedure (section 5.4). Of the 18 remaining staves that satisfied the QA procedure, the best 14 were selected for assembly in the IBL detector.

### 5.1 Stave loading and rework

Qualified modules were loaded on the staves following the procedure described below and sketched in figure 30. Each qualified stave was installed in a loading tool where a 70 µm thick thermal grease[27]

[27] HTCP, Electrolube, see https://www.electrolube.com/core/components/products/tds/044/HTCP.pdf.



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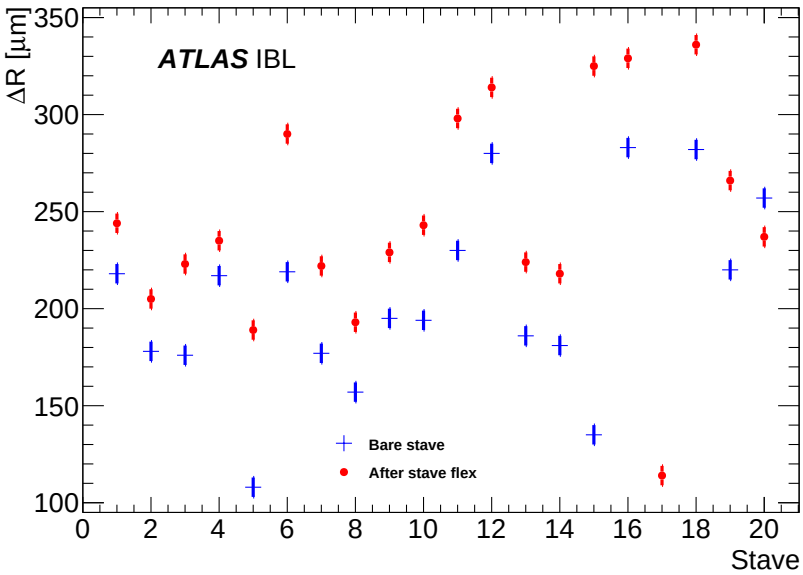
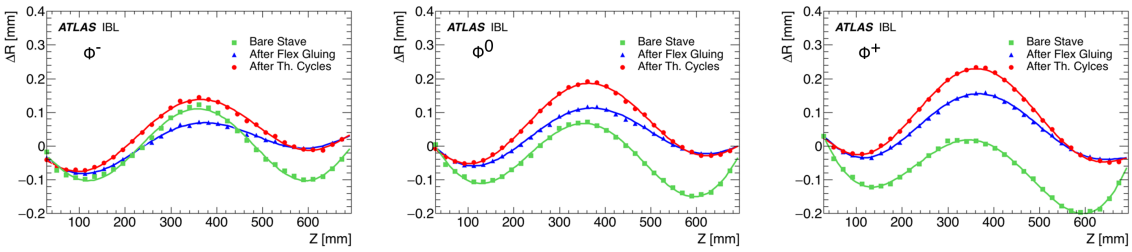



**Figure 28.** The planarity, ΔR, of each production stave, before and after thermal cycling. There is a 5 μm uncertainty on all measurements. No measurement exists for the planarity of stave 17 before thermal cycling.




(a) (b) (c)

**Figure 29.** Stave planarity, ΔR, in three azimuthal positions for a single stave, showing the planarity before stave flex gluing (red), after flex gluing (blue) and after thermal cycling (green): (a) $\phi^-$; (b) $\phi^0$; and (c) $\phi^+$, as defined in the text.

layer was applied to half of its surface using a stainless steel template shim. After removing the template, the positioning tools were installed, and two Araldite 2011 glue drops per FE-I4B chip were applied with a needle on the thermal grease template openings to later fix the modules on their position. The modules were then installed, one at a time, using spacers to achieve a precise 200 μm gap between neighbouring modules. A load of ~20 g per FE-I4B chip was placed on the modules during the glue-dot curing period. After the removal of weights and positioning tools, an optical inspection was performed before repeating the process on the other half of the stave.

After loading, the modules were connected to the stave flex following the procedure sketched in figure 31. First a layer of Araldite 2011 was deposited on each of the stave flex wings using a mask. A tool constrained the wings to stay in their nominal position. A load of ~16 g per FE-I4B chip was applied during the glue curing period. A ~100 μm-thick Kapton® insulator was then inserted between each powering sector. Finally, wire-bonds were added to connect the modules to the wings of the service flex, enabling the stave powering and data transmission. As a last step, the stave envelope was checked to ensure that the mechanical constraints of the IBL were fulfilled.



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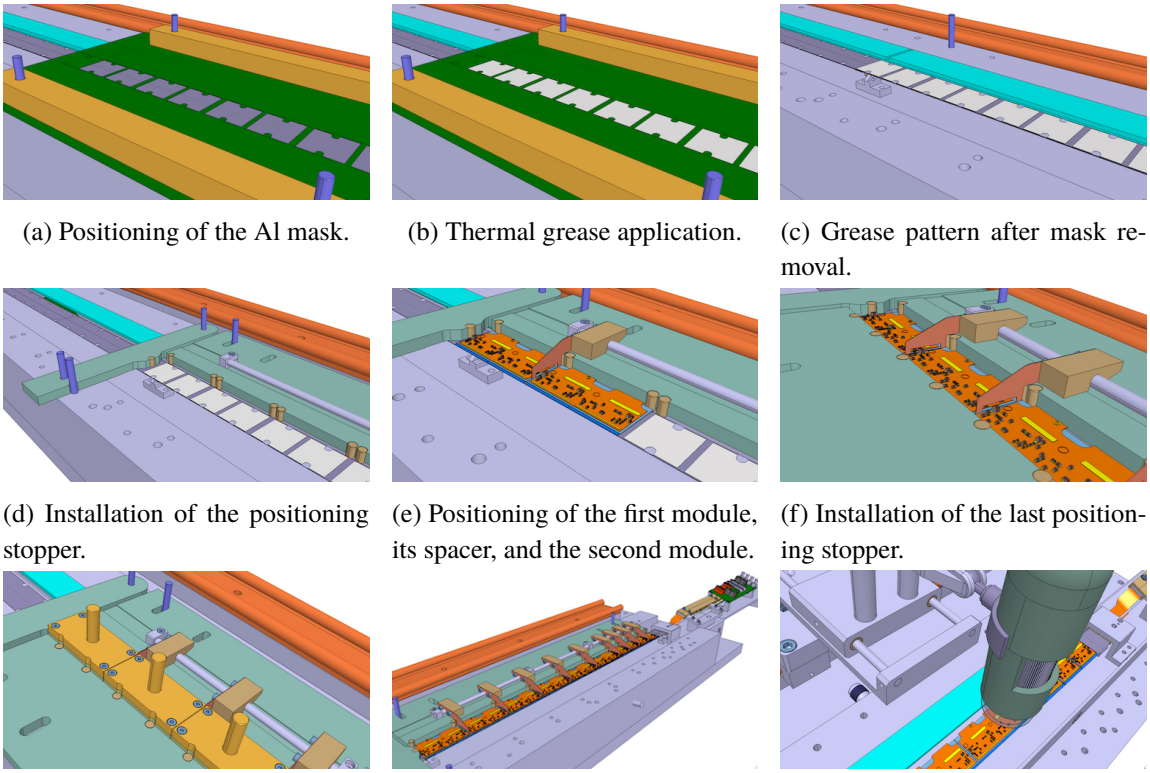

(a) Positioning of the Al mask.

(b) Thermal grease application.

(c) Grease pattern after mask removal.

(d) Installation of the positioning stopper.

(e) Positioning of the first module, its spacer, and the second module.

(f) Installation of the last positioning stopper.

(g) Installation of the module weights.

(h) Tooling dismounting after glue curing.

(i) Optical inspection.

**Figure 30.** Three dimensional renditions of the main stave module-loading steps.

A module re-work procedure, sketched in figure 32, was established to replace modules if required as a result of mechanical damage or functional issues. A ~100 µm-thick Kapton® spacer and holders were installed at each side of the module to be replaced, protecting the neighbouring modules. The module was removed using a spatula and the stave face plate was cleaned from grease or glue. A new module was then loaded following the procedure described above, using a set of dedicated tools. In total, twenty-two modules were re-worked: fifteen modules were replaced due to module damage during the module loading procedure that compromised the integrity of the sensor, the FE-I4B chip or the module flex; five modules were replaced because of failures of the FE-I4B chip after loading; and two modules were replaced because they failed the QA tests made before final integration. In addition, due to the cleaning and re-bonding intervention performed (section 5.4), six modules were replaced on the twelve re-bonded staves.

## 5.2 Quality assurance of the stave assemblies

### 5.2.1 Stave cooling performance

An essential aspect of the stave design is the removal of heat from the IBL modules, under any foreseeable environmental and running condition. The sensor temperatures must be controlled, as an increasing sensor temperature will result in an increased sensor leakage current that may lead to thermal runaway [43], damaging the module. To minimise the effects of reverse annealing and



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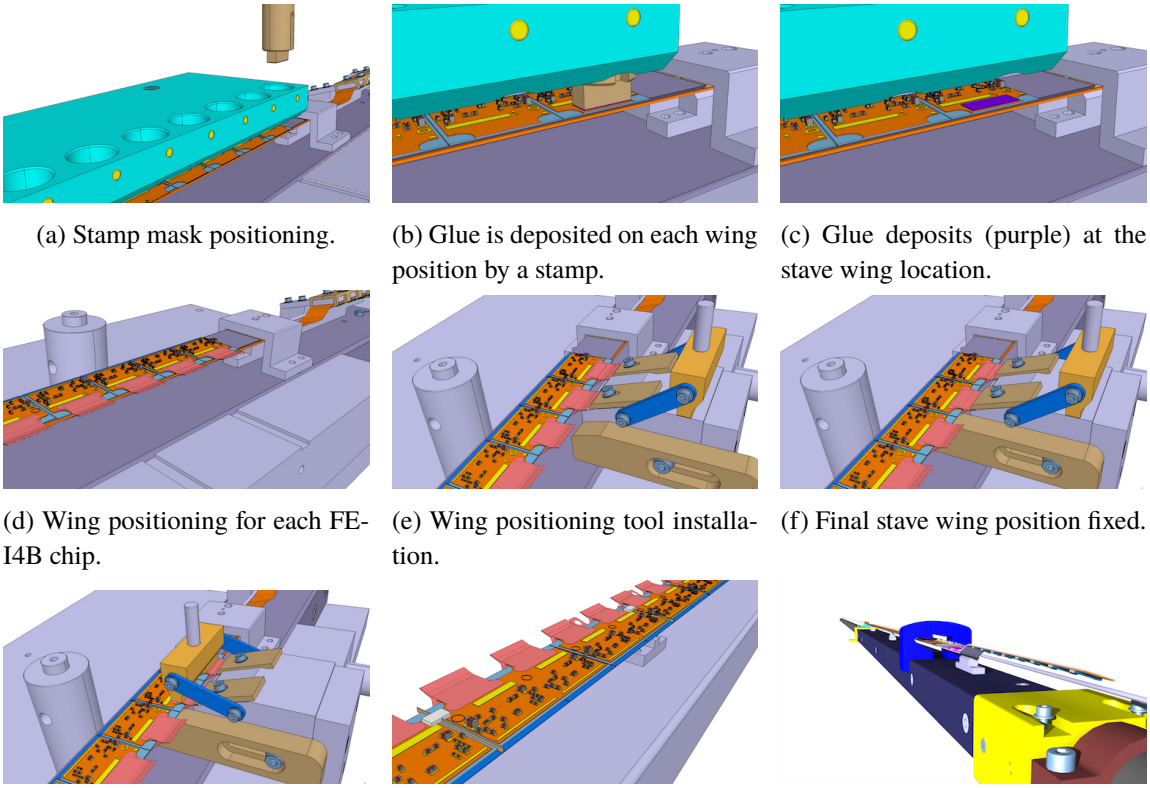


(a) Stamp mask positioning.

(b) Glue is deposited on each wing position by a stamp.

(c) Glue deposits (purple) at the stave wing location.

(d) Wing positioning for each FE-I4B chip.

(e) Wing positioning tool installation.

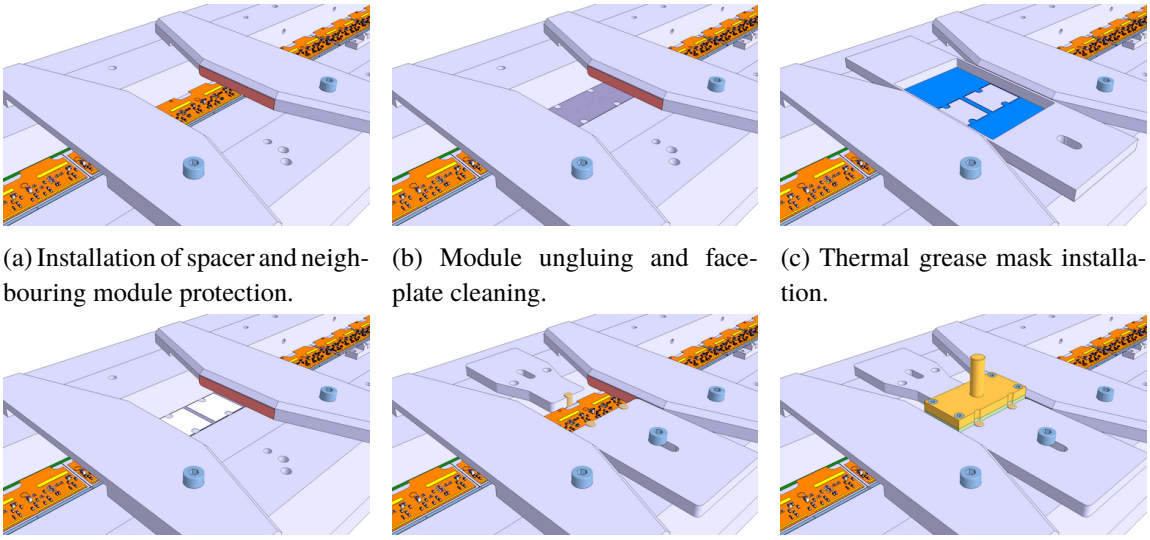
(f) Final stave wing position fixed.

(g) Weight on stave wings during glue curing.

(h) HV insulator placement and bridge gluing.

(i) Stave envelope check.

**Figure 31.** Three dimensional renditions of the main stave-flex wing gluing steps.



(a) Installation of spacer and neighbouring module protection.

(b) Module ungluing and face-plate cleaning.

(c) Thermal grease mask installation.

(d) Thermal grease pattern and glue dots.

(e) Module placement using positioning tools.

(f) Weight positioning and glue curing.

**Figure 32.** Three dimensional renditions of the main re-work steps for replacement of modules.

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thermal runaway in the sensors, the target temperature of IBL modules during operation is below −15 °C. Furthermore, the modules must remain cool during beam-pipe bake-out procedures when the beam pipe at the IBL contact points reaches 110 °C.

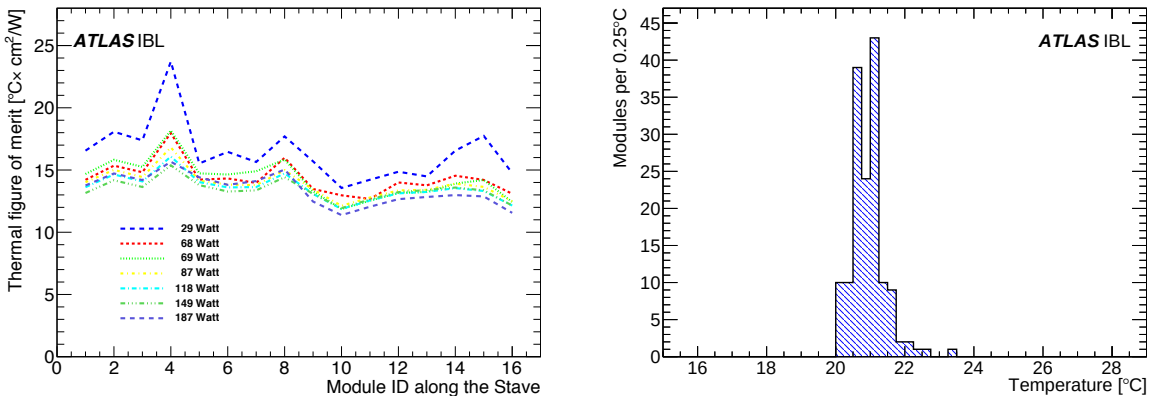
The bi-phase $CO_2$ cooling system (section 7.5) was chosen to achieve the required low temperature module operation while minimising the pipe diameter and the associated radiation length [44]. The 1.7 mm external diameter titanium T40 cooling tubes have a 0.11 mm wall thickness to meet the $CO_2$ critical pressure (73.8 bar at 31 °C) requirements.

Several simulations were performed to estimate the stave thermal performance, quantified by the Thermal Figure of Merit (TFoM), i.e. the thermal resistance between the cooling fluid and the sensor surface. Considering the various heat sources and an active sensor area $A_{\text{sensor}}$, the sensor temperature can be expressed as:

$$T_{\text{sensor}} = T_{\text{coolant}} + \frac{TFoM}{A_{\text{sensor}}} \times (P_{\text{chip}} + P_{\text{flex}} + P_{\text{sensor}})$$

where $P_{\text{chip}}$ is the power dissipated in the chip; $P_{\text{flex}}$ is the power dissipated in the module flex; and $P_{\text{sensor}}$ is the power dissipated in the sensor. In worst-case conditions for $P_{\text{chip}}$, $P_{\text{flex}}$ and $P_{\text{sensor}}$, the thermal runaway was estimated to occur for the TFoM > 30 °C cm$^2$/W.

Figure 33a shows the measurement for a prototype stave during the final design qualification. The measured TFoM is 14 °C cm$^2$/W for $T_{\text{coolant}} = -22$ °C, conservatively a factor two below the TFoM value at thermal runaway. To qualify the thermal performance of the stave during production, the temperature uniformity was measured for each stave after module loading. All of the installed staves show a temperature dispersion within 0.5 °C, as shown in figure 33b, which is a good indication of the production uniformity.




(a) (b)

**Figure 33.** (a) Measured Thermal Figure of Merit (TFoM) for modules along a stave, with a 1.7 mm outer diameter titanium cooling tube. (b) The module temperature distribution on produced staves, with configured read-out electronics and a cooling tube temperature of 19 °C. The histogram has 152 entries, a mean value of 20.9 °C and an RMS of 0.5 °C.

### 5.2.2 Metrology survey

An optical survey of the stave assemblies was made using the four fiducial marks placed on each module. The error distributions of the module loading position are shown in figure 34 for the $\phi$



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and $z$ axes:[28] an RMS precision of 50 µm is measured for planar modules in both directions, and for 3D modules an RMS precision of 56 µm in $z$ and 33 µm in $\phi$ is achieved.

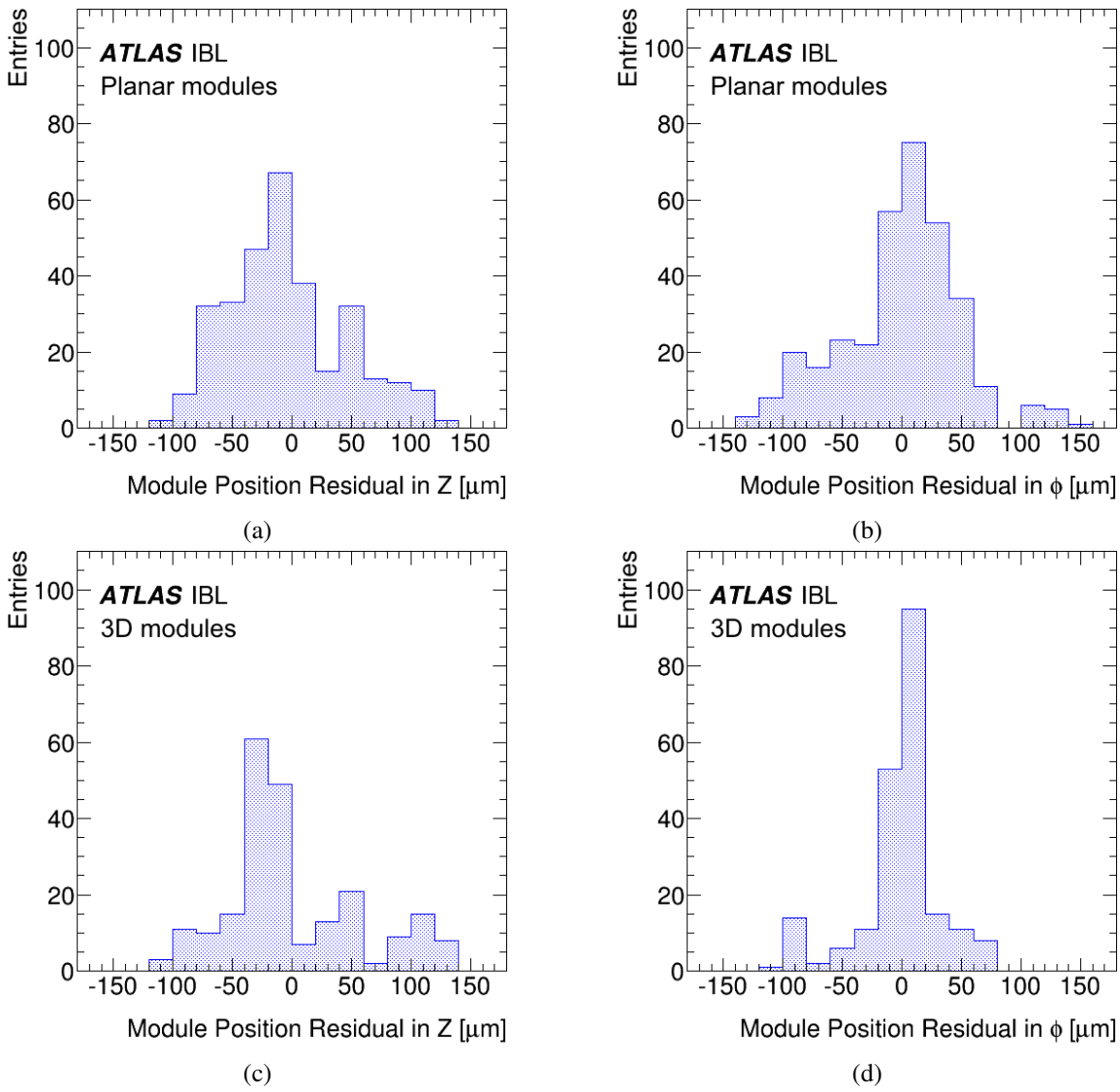


**Figure 34.** Fiducial mark residuals in the directions $z$ and $\phi$ for (a,b) double-chip planar modules and (c,d) single-chip 3D modules.

### 5.2.3 Functional qualification

Following the metrology survey, the staves were transported to CERN where the final stave qualification was carried out. Results from the electrical qualification [42] were an important input for the selection of the 14 staves that were integrated in the final detector.

The electrical QA test stand could operate two staves simultaneously. The staves were installed in an environmental box, which was flushed with dry air to maintain the humidity below 3 %, cor-

[28]For the definition of the $\phi$ and $z$ directions refer to figure 24.



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responding to a dew point of −53 °C for the minimum box temperature of −20 °C. The temperature on the staves was controlled by a TRACI[29] $CO_2$ cooling plant.

The Detector Control System (DCS) and the Data Acquisition (DAQ) for the test stand emulated the DCS and DAQ of the installed IBL detector, described in sections 6.2 and 6.3. They were connected to the stave using custom EoS PCBs. The read-out system used the Reconfigurable Cluster Elements (RCE) architecture based on ATCA technology [45]. As for the installed IBL detector, the DCS granularity was a group of four read-out chips; it was not possible to record and control individual modules. The nomenclature of the FE-I4B chips as used for the stave QA, and of the DCS read-out for a stave, are shown in figure 35.

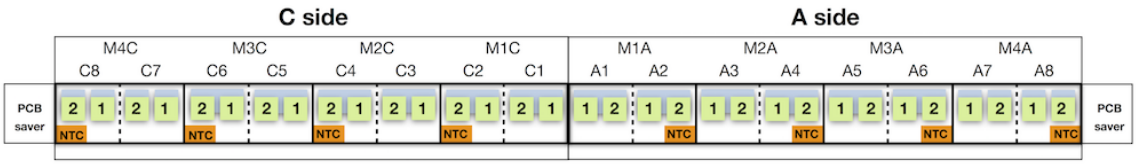


**Figure 35.** Schematic for a full stave of the module and FE-I4B layout, as well as the DCS and powering modularity. The FE-I4B chips are labelled for the stave and integration QA as A(C)X-Y where X runs from 1 to 8 towards the PCB cards, and Y is 1 or 2. A(C)7 and A(C)8 are single-chip 3D modules. The DCS modularity is shown as M1A(C) through M4A(C). The NTCs measure the temperature of each module group.

A detailed optical inspection of each stave was made before and after the QA procedure. Photographs of each chip were taken with a high resolution camera to identify any major damage to the chip, as well as debris that might have been left on the stave during assembly or wire bonding. A detailed microscope inspection of the stave was then made.

The electrical functionality of each stave was next verified, before making calibration measurements. This included power-up studies, the verification of set voltages and currents in un-configured and configured FE-I4B chip states, and I-V characteristics of the sensors. The powering behaviour of the modules was verified during ten LV power cycles. The time dependence of current and voltage from this test are shown for stave ST12 in figure 36a. Most modules show a stable current consumption for every cycle; current fluctuations can be explained by improperly reset chip registers. After a first successful power-up of the stave, the temperature, the set voltage reading, and the currents before and after read-out configuration of each DCS group, were recorded. The expected values during the stave QA are listed in table 15. An I-V scan was performed to characterise the sensor quality. The sensor HV was ramped in 20 steps from 0 to 100 V for 3D sensors and from 0 to 200 V for planar sensors. The I-V characteristics of the DCS module group of four read-out chips was required to be compatible with the measurements performed on modules before the stave loading. Results for stave ST12 are shown in figure 36b. For this particular stave, one DCS group (M4C) indicated a 3D sensor I-V breakdown, above the operating voltage and still within the QA specification.

A series of basic functionality tests, including the digital functionality, the $t_0$ calibration and threshold, ToT and crosstalk scans, were also made, using the module configurations recorded at previous module QA testing sites (section 3.4.2). This allowed a direct comparison of the stave

[29]Transportable Refrigerator Apparatus for $CO_2$ Investigation, https://ep-dep-dt.web.cern.ch/co2-coolingplants/traci-geneve.



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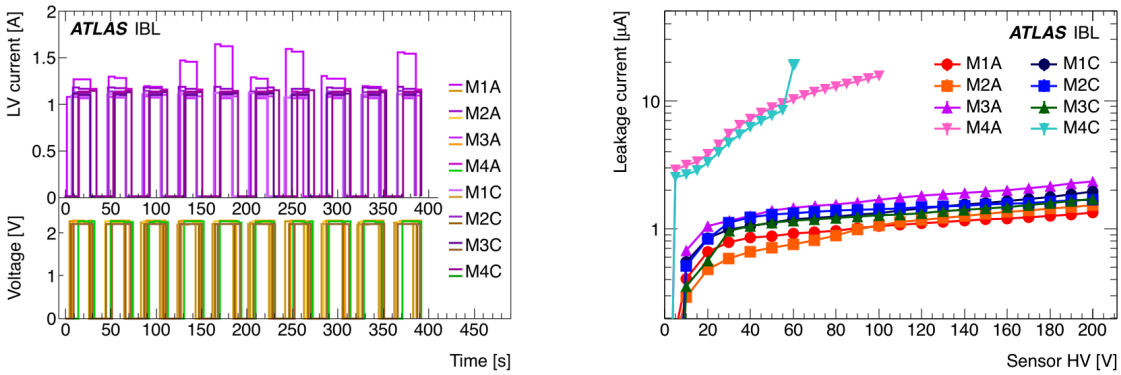
**Table 15.** Quantities recorded for each DCS group (four read-out chips) and their nominal expected values in the QA qualification of loaded staves after their reception at CERN.

| Quantity | Expected Value |
|---|---|
| Temperature | 22 °C |
| Voltage | 2.1 V |
| Unconfigured current | 1.1 A |
| Configured current | 1.5 A |
| Leakage current | Compatible with module QA |




(a) (b)

**Figure 36.** (a) LV cycles and (b) sensor I-V characteristics for the 8 DCS groups of stave ST12. The DCS granularity is a group of four read-out chips (two planar modules or four 3D modules).

functionality, and discrepancies indicating possible damage induced during module loading or transportation to CERN.

A comparison of threshold scans with and without HV allows the identification of areas of disconnected bumps, since a pixel that is no longer connected to the sensor is not affected by the higher noise present when the sensor is not fully depleted. Nevertheless, a source scan is needed to fully identify all disconnected bumps as described in section 5.2.5.

### 5.2.4 Stave calibration

Following a $t_0$ calibration, the discriminator threshold and the ToT parameters of the FE-I4B chips must be calibrated and tuned to distinguish charged particle signals from electronic noise, and to ensure that the charge determination is uniform over all IBL pixels. The selected threshold should be as low as possible to ensure maximal detector efficiency for charged particles (especially when the charge is shared between pixels), and to ensure the best possible ToT tuning. It should also be sufficiently high to discriminate against electronic noise.

During the module QA (section 3.4), a mean module threshold of 3000 $e^-$. To compare with those results, the same calibration working point was retained. A more realistic operating condition is to use a lower pixel threshold as noted above. A second calibration working point of 1500 $e^-$ at



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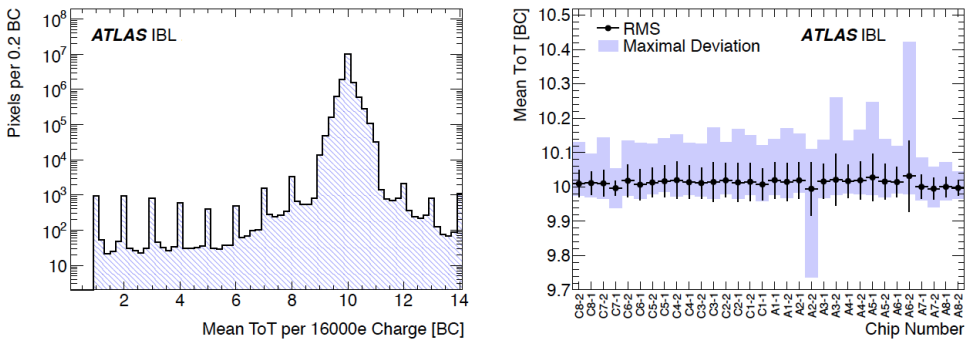
an operating temperature of −12 °C was chosen [42]. The mean threshold can be tuned for each FE-I4B chip using charge injection circuitry. As for the QA of individual modules, the pixel noise (ENC)[30] is evaluated from a measure of the pixel occupancy as a function of injected charge, using the FE-I4B charge injection circuitry (the S-curve method).

In each case the ToT was tuned to 10 units of 25 ns for a charge of 16 000 $e^-$, corresponding to a minimum ionising particle at normal incidence. Figure 37 shows the one-dimensional ToT distribution for all pixels when tuned to 10 ToT, and the mean ToT as a function of chip number along the stave. The data are shown for a mean module threshold of 1500 $e^-$ at −12 °C.

The threshold calibration results for the complete set of staves are summarised in table 16. The pixel-to-pixel RMS of the threshold distribution (threshold RMS), of approximately 40 $e^-$, is compatible with the accuracy of the injection circuit. Figure 38 shows the threshold and noise (ENC) distributions for individual pixels, in the case of a 3000 $e^-$ threshold tuning at 22 °C. Figure 38a indicates that all of the modules could be tuned to a mean threshold of 3000 $e^-$, with only a few individual pixels that could not be tuned to that value.




(a) (b)

**Figure 37.** (a) One-dimensional Time-over-Threshold (ToT) distribution for all pixels when tuned to 10 ToT, using an injected charge of 16 000 $e^-$. The spikes result from injection failures where the selected ToT value is not 10. Non-integer mean ToT values result when successive injections to evaluate the mean select differing ToT values. (b) The average ToT distribution as a function of the chip number (position) on the stave. The data are from all 18 qualified staves using a mean module threshold of 1500 $e^-$ at −12 °C.

The threshold-over-noise distributions for 3000 $e^-$ and 1500 $e^-$ tunings are shown in figure 39; this quantity is the key parameter in determining the quality of the IBL modules with respect to their operability at a given discriminator setting. The physics occupancy in the ATLAS Pixel B-Layer was approximately $5 \times 10^{-4}$ hits per pixel per bunch crossing unit of 25 ns at the end of Run 1 and that for the IBL was expected to be approximately $10^{-3}$ hits per pixel per bunch crossing unit at the beginning of its operation. Pixels with a noise occupancy rate higher than $10^{-6}$ hits per pixel per bunch crossing unit were considered to be noisy and were disabled from data taking. A threshold-over-noise value larger than 5 ensured a noise contamination in IBL physics hits of less

[30]ENC is defined in section 3.4.4.



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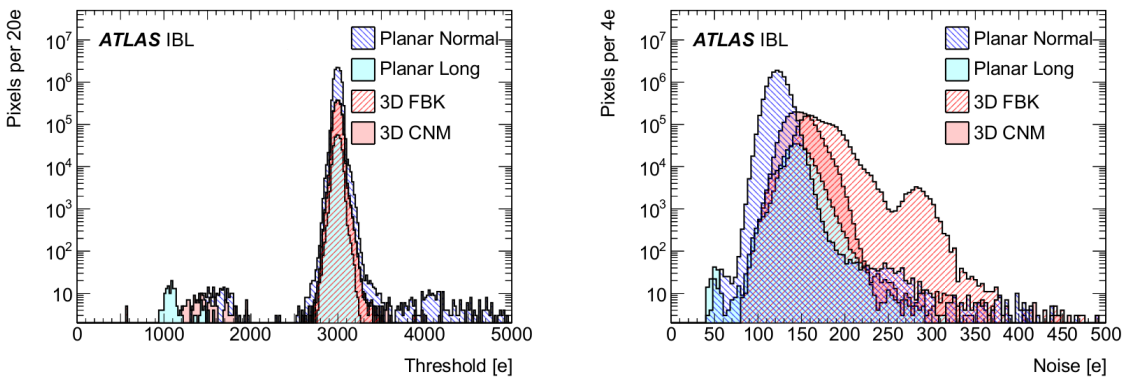
**Table 16.** Calibration summary for the 18 qualified staves. Long pixels of planar sensors are listed separately to indicate a higher noise because of their larger pixel size.

| Tuned Threshold | Pixel Type | Threshold RMS [e$^-$] | ENC [e$^-$] | Threshold-over-Noise |
|---|---|---|---|---|
| 3000 e$^-$ at 22 °C | Planar Normal | 37 | 123 ± 10 | 25 ± 2 |
| | Planar Long | 58 | 146 ± 15 | 21 ± 2 |
| | 3D FBK | 39 | 171 ± 25 | 18 ± 2 |
| | 3D CNM | 40 | 149 ± 15 | 20 ± 2 |
| 1500 e$^-$ at −12 °C | Planar Normal | 42 | 129 ± 13 | 12 ± 1 |
| | Planar Long | 47 | 149 ± 16 | 10 ± 1 |
| | 3D FBK | 46 | 171 ± 25 | 9 ± 1 |
| | 3D CNM | 41 | 146 ± 16 | 10 ± 1 |




(a) (b)

**Figure 38.** (a) Threshold and (b) noise (ENC) distributions of individual pixels for a 3000 e$^-$ threshold tuning at 22 °C. The threshold width is primarily determined by the injection circuit, and only a few individual pixels were badly tuned.

than 0.1 %. For the 1500 e$^-$ reference tuning at −12 °C module temperature, the observed fraction of noisy IBL pixels was less than 0.03 %.

Figure 40 shows the threshold and noise distributions averaged over all 18 qualified staves as a function of chip number for the 1500 e$^-$ reference tuning. Figure 40a shows that it was possible to tune all production staves to 1500 e$^-$ within 40 e$^-$. The average noise was approximately 130 e$^-$ for planar sensors and less than about 170 e$^-$ for 3D sensors. Slightly higher noise was observed on the A-side of the setup: this was due to a combination of increased noise on the HV lines of the setup and the fact that FBK modules, which are more sensitive to external noise, represented the majority of the 3D sensors on this side.



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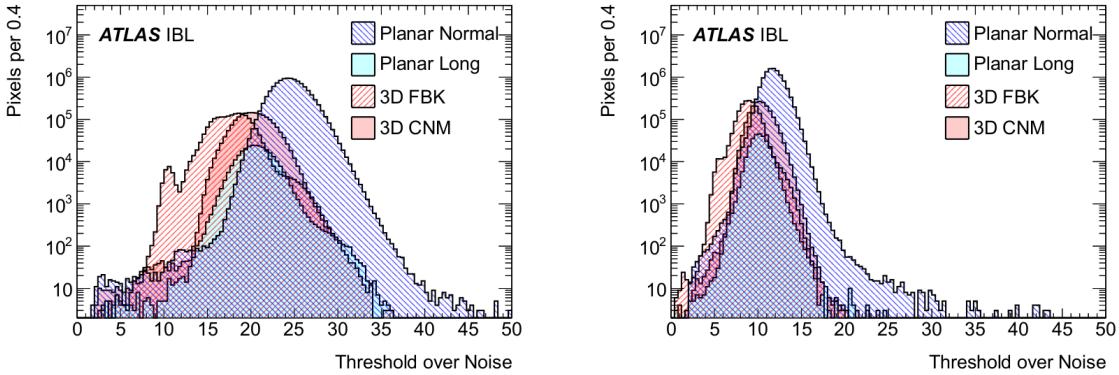
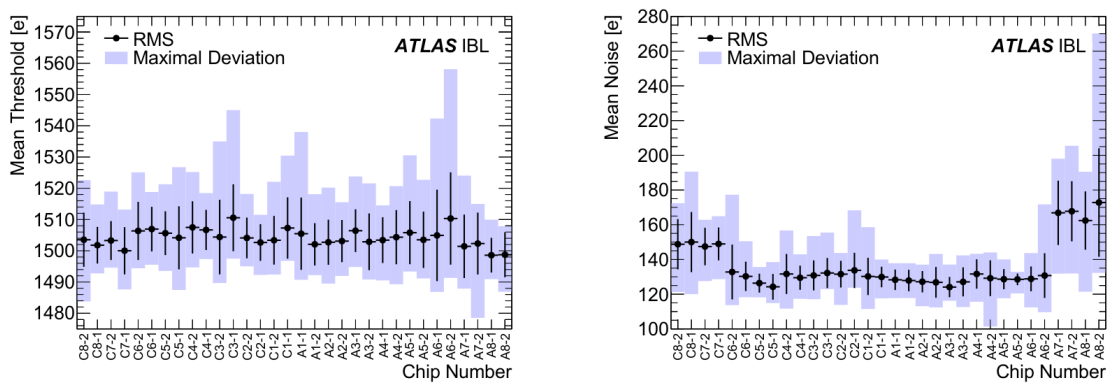



(a) (b)

**Figure 39.** Threshold-over-noise distribution of pixels for threshold tunings of (a) 3000 $e^-$ at 22 °C and (b) 1500 $e^-$ at −12 °C.




(a) (b)

**Figure 40.** (a) Mean threshold and (b) mean noise (ENC) distributions for all 18 qualified staves as a function of the chip number (position) on the stave, for a 1500 $e^-$ threshold tuning at −12 °C . The error bars represent the RMS value accounting for the differences between staves whereas the solid colour describes the full range covered by data.

### 5.2.5 Source scans

Source scans were performed with a 3000 $e^-$ threshold configuration using a $^{90}$Sr source and an internal self trigger mechanism. An example of a source scan hit map for a single 3D FBK module is shown in figure 41. Regions with a lower number of hits are clearly visible and match the passive components mounted on the module flex. Each normal pixel collected approximately 150 – 200 hits. An increased hit occupancy in the edge columns and the edge rows is due to an increased active area for FBK pixels resulting from the fence structure at the edge. Figure 42a shows the hit occupancy for planar pixels, separating the categories of normal pixels and long pixels. The mean hit occupancy is less than that for 3D modules because of the reduced sensor thickness (200 µm instead of 230 µm). Figure 42b shows the occupancy for normal and edge pixels of CNM and FBK modules. Because of their guard-ring design CNM sensors do not show an excess in the edge rows



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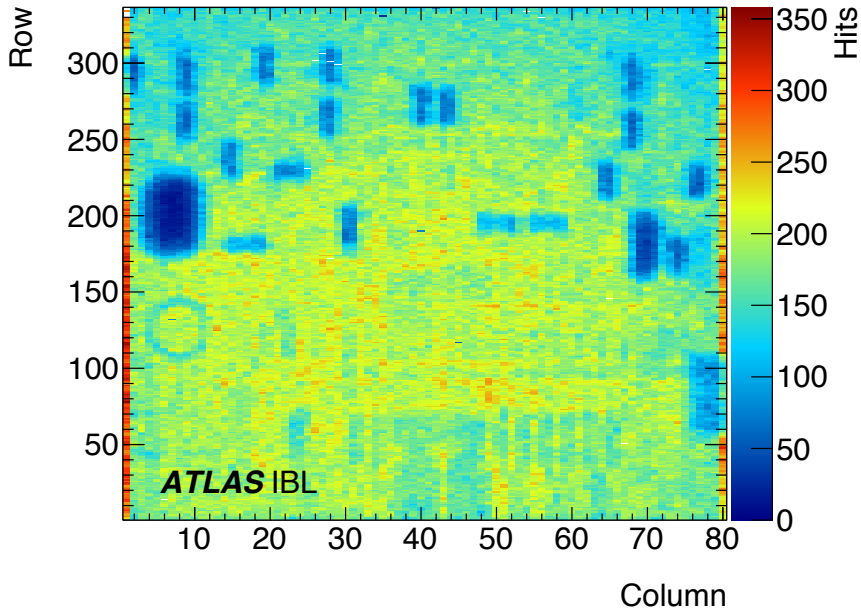
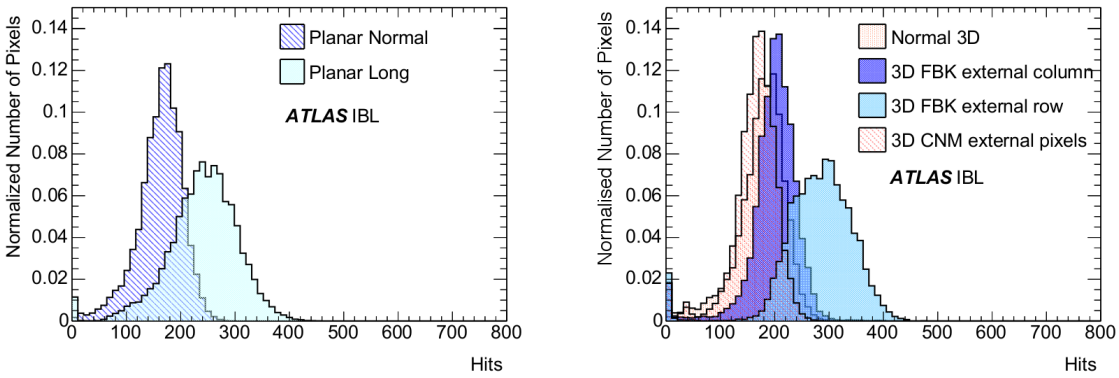



**Figure 41.** Typical source scan hit map of a 3D FBK module during the stave QA. Regions with a lower number of hits match passive components mounted on the module flex. The module threshold is tuned to 3000 $e^-$ at an operating temperature of 22 °C.




(a) (b)

**Figure 42.** Occupancy distributions for (a) planar modules and (b) 3D CNM and FBK modules collected using a $^{90}$Sr source and an internal self trigger mechanism during IBL stave QA. The content of each category of source measurement is normalised to unity in the figures. The module threshold is tuned to 3000 $e^-$ at an operating temperature of 22 °C.

and columns. Although not shown, CNM sensors also have a slightly lower occupancy than FBK sensors for normal pixels because of the smaller depth of their columnar electrodes.

Source scans were mainly used to identify disconnected bumps, but it was also possible to check the average charge using the $^{90}$Sr source. This used the ToT distribution of all clusters with more



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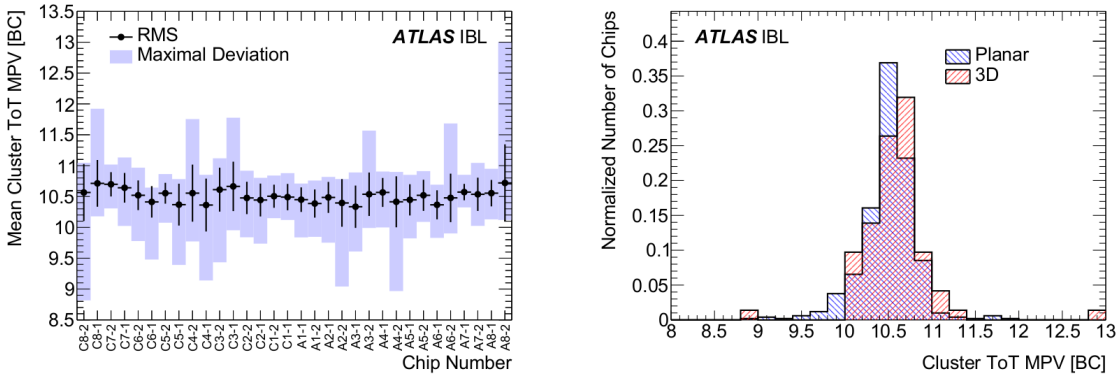
than one hit.[31] Figure 43a shows the most probable value (MPV) of the Landau-Gauss fit of such distributions as a function of FE-I4B position, averaged over all staves; the MPV distribution of each chip is shown in figure 43b. The different behaviour between 3D and planar modules is due to their different sensor thickness. The difference with respect to the calibrated mean of 10 ToT is small.




(a) (b)

**Figure 43.** Most probable value (MPV) of the Time-over-Threshold (ToT) distribution for all clusters with more than one hit, fit with a Landau-Gauss function: (a) the mean MPV as a function of chip number (position) on the stave and (b) the distribution of the mean MPV for all chips. In (a) the error bars represent the RMS value accounting for the differences between staves whereas the solid colour describes the full range covered by data. The module threshold is tuned to 3000 $e^-$ at an operating temperature of 22 °C.

### 5.2.6 Pixel defects

Faulty pixels were classified on the basis of calibration and source scan results and assigned to a single category listed in table 17. This table indicates the failure type, the method used to identify the failure, and the detailed selection criteria.

Most of the failures relied on the module showing an excess or deficit of the hit rate. The digital and analog functionalities can be directly tested with respectively digital and analog scans. Dead digital and analog pixels are common electronic failures. However, the digital and analog bad categories only appear in high numbers for the case of a low ohmic connection between pixels or the identification of a merged bump as occurred in early production batches (section 3.4). The merged bump category exists when two solder bumps connecting the sensor to the read-out chip are merged and manifests itself in an analog failing pixel which still gives a response in a crosstalk scan. A pixel is classified as untunable if the threshold or ToT cannot be tuned at all; nevertheless a high discrepancy from the tuning target is accepted as these pixels can still be used for operation. The noise occupancy, which indicates how many hits per BC are produced due to noise, is a very important diagnostic and operational quantity. The easiest way to identify a disconnected bump is to analyse the response from a source scan. If a pixel shows zero or only very few hits in the source scan data, the bump is assumed to be disconnected (section 3.4). The high crosstalk pixel category is not directly related to the performance of the pixel but if a sensor pixel shows significant charge sharing with a neighbour, this can influence the precision of the offline reconstruction.

[31] Clusters are formed by groups of hits collected by adjacent pixels.



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**Table 17.** Classification of pixel failures.

| Failure Name | Scan type | Criteria | |
|---|---|---|---|
| Digital dead | Digital scan | Occupancy | <1 % of signal injections |
| Digital bad | Digital scan | Occupancy | <98 % or >102 % of signal injections |
| Merged bump | Analog scan | Occupancy | <98 % or >102 % of signal injections |
| | Crosstalk scan | Occupancy | >80 % of 25 ke$^-$ signal injections |
| Analog dead | Analog scan | Occupancy | <1 % of signal injections |
| Analog bad | Analog scan | Occupancy | <98 % or >102 % of signal injections |
| Tuning failed | Threshold scan | s-curve fit | Fit failure |
| | ToT test | ToT response | 0 or 14 ToT units of 25 ns |
| Noisy pixel | Noise scan | Occupancy | >$10^{-6}$ hits per 25 ns bin |
| Disconnected bump | Source scan ($^{90}$Sr) | Occupancy | <1 % of mean occupancy |
| High crosstalk | Crosstalk scan | Occupancy | >0 with 25 ke$^-$ signal injection |

The total fraction of bad pixels, averaged over all modules, is shown in figure 44. No clear correlation was found between the chip topology (other than edge regions) and the measured disconnected bumps. There was a clear increase in the number of bad pixels towards the stave ends because of the choice to load the best modules into the central region of a stave. The number for each bad pixel category is collected for each stave in table 18.

A production cut of 100 bad pixels per chip was initially applied after the module assembly. This cut was relaxed at the end of the production because of a shortage of 3D sensor assemblies; 73 % of all chips loaded onto staves had less then 0.1 % bad pixels.

The total number of failing pixels per stave is shown in figure 44d. The dashed lines indicate the 0.1 % and 0.2 % marks; the specification required a stave to satisfy < 1 %. All staves were well within the specification; 80 % of the staves had < 0.2 % failing pixels and 50 % of those staves had < 0.1 %. Approximately 50 % of all failures were due to disconnected bumps, the other 50 % were distributed between a pixel with failing analog functionality, or a bad ToT tuning.

Correlations between the defects observed at this stage and in the module production were extensively studied [42]. Although similar selections to classify a pixel were used in the two test stages, a more intense test procedure was applied during module production and more bad pixels were detected per FE-I4B chip. However, there was a good correlation between the number of bad pixels per FE-I4B chip in the two tests. Moreover it was verified that there was no significant increase of bad pixels in specific geographical areas, for example the chip edges, thus excluding damage resulting from the module transport, handling and stave loading.

### 5.3 Stave ranking and layout assignment

Of the 18 qualified loaded staves, 14 staves were selected for integration as part of the IBL. The stave quality was scored by a geometrical inefficiency based on a $\eta$-weighted bad pixel fraction, together with an algorithm developed to minimise the clusterisation of bad pixels in $\eta - \phi$. In addition, two



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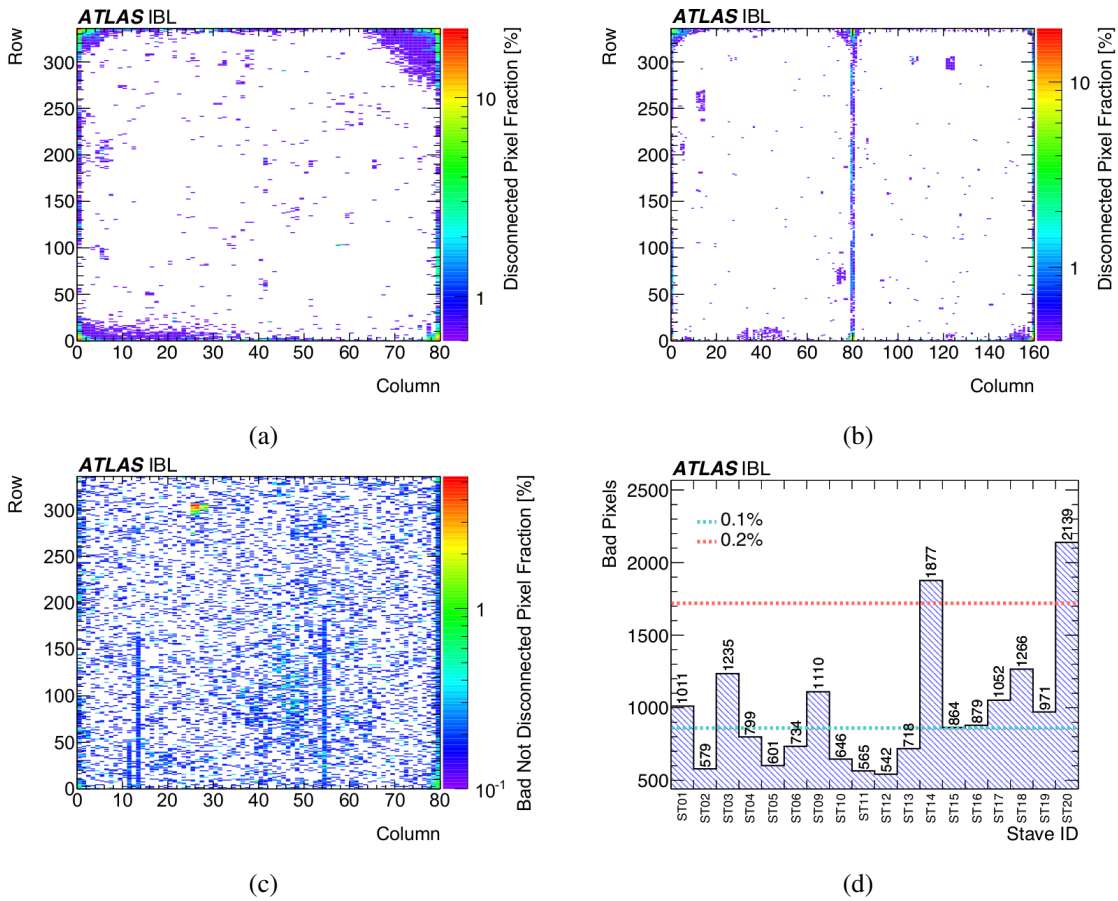


**Figure 44.** Map of the fraction of disconnected pixels for (a) 3D modules and (b) planar modules . (c) Map of the total fraction of bad but not dis-connected pixels (both module types). (d) The total number of bad pixels per stave for all 18 qualified staves. The horizontal bars in (d) indicate the 0.1 % and 0.2 % bad pixel levels.

artificial constraints were applied: the first and the last integrating staves were required to have the best planarity in order to simplify assembly; and staves that were re-worked as a result of corroded wire bonds (section 5.4) were loaded alternately.

Table 19 summarises the position of each stave in the IBL loading map, and other characteristics of the staves considered in the selection. Figure 45a compares the average bad pixel fraction for the 14 installed staves with the four non-installed staves, as a function of $\eta$. The average bad pixel fraction for the integrated IBL staves is 0.07 % for $|\eta| < 2.5$ and 0.09 % over the full $\eta$ range. The corresponding fractions for the four non-installed staves are respectively 0.16 % and 0.18 %. Figure 45b shows the distribution of bad pixel fraction as a function of $\eta$ and $\phi$. The stave overlap is taken into account in this figure.

### 5.4 Wire bond corrosion

During the IBL production, two production staves were damaged during testing inside the QA environmental box. While the staves were in operation and cooled at −20 °C, ice was identified around the coldest part of the staves. The two staves were carefully inspected under a microscope and it was discovered that most of the aluminium wire bonds were corroded (figure 46), with a few



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**Table 18.** Overview of the number of different bad pixel categories for the 18 qualified staves. Digital and Analog failure modes include both dead and bad categories as defined in table 17.

| Stave | Digital fault | Analog fault | Disconnected pixel | Merged bump | Untunable | Noisy pixel | High crosstalk | Total |
|---|---|---|---|---|---|---|---|---|
| ST01 | 6 | 389 | 272 | 3 | 232 | 11 | 98 | 1011 |
| ST02 | 10 | 255 | 54 | 3 | 117 | 15 | 125 | 579 |
| ST03 | 6 | 375 | 473 | 0 | 182 | 21 | 178 | 1235 |
| ST04 | 2 | 201 | 254 | 0 | 275 | 8 | 59 | 799 |
| ST05 | 2 | 207 | 172 | 0 | 183 | 4 | 33 | 601 |
| ST06 | 6 | 206 | 337 | 0 | 147 | 9 | 29 | 734 |
| ST09 | 8 | 360 | 476 | 3 | 167 | 8 | 88 | 1110 |
| ST10 | 16 | 179 | 304 | 0 | 141 | 3 | 3 | 646 |
| ST11 | 10 | 196 | 159 | 0 | 155 | 8 | 37 | 565 |
| ST12 | 15 | 172 | 169 | 0 | 166 | 7 | 13 | 542 |
| ST13 | 9 | 127 | 205 | 0 | 336 | 6 | 35 | 718 |
| ST14 | 4 | 161 | 1364 | 0 | 330 | 7 | 11 | 1877 |
| ST15 | 5 | 222 | 350 | 0 | 259 | 20 | 8 | 864 |
| ST16 | 1 | 237 | 414 | 1 | 187 | 15 | 24 | 879 |
| ST17 | 2 | 214 | 598 | 0 | 229 | 5 | 4 | 1052 |
| ST18 | 13 | 161 | 902 | 1 | 178 | 2 | 9 | 1266 |
| ST19 | 10 | 163 | 543 | 0 | 228 | 11 | 16 | 971 |
| ST20 | 14 | 224 | 1051 | 0 | 535 | 13 | 302 | 2139 |

broken. A white residue around the bond foot could be easily identified with ring lighting. The other staves were re-inspected and, of the 12 staves already produced, 11 staves were identified to suffer from bond corrosion.

Production was halted until the problem was understood. A number of successive actions were taken:

- Identify the origin of the corrosion and identify corrective actions such as to improve the QA procedure, before resuming the production;
- Investigate the evolution of the corrosion and identify possible preventive actions, for example cleaning and coating;
- Organise a re-work centre to clean all the wires and to re-bond the 11 defective staves;
- Launch an additional module production with remaining components to ensure a sufficient number of IBL staves for the integration.



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**Table 19.** Loading order overview of the 14 IBL staves. The position is sequential around the beam pipe. The cooling pipe of the stave in position 01 is at $\phi = -6.1°$, subsequent staves are displaced by 25.7° in $\phi$. The planarity shows the difference between the minimum and maximum height of a stave. The last column indicates whether a stave has been reworked at the CERN wire bonding laboratory because of the corrosion issue. For completeness, the last four lines show the same parameters for those staves that were not selected for installation.

| Position | Stave | Number of bad pixels | Planarity [μm] | Reworked because of corrosion |
|---|---|---|---|---|
| 01 | ST17 | 1052 | 114 | no |
| 02 | ST02 | 579 | 205 | yes |
| 03 | ST19 | 971 | 266 | no |
| 04 | ST09 | 1110 | 229 | yes |
| 05 | ST18 | 1266 | 336 | no |
| 06 | ST04 | 799 | 235 | yes |
| 07 | ST13 | 718 | 224 | no |
| 08 | ST10 | 646 | 243 | yes |
| 09 | ST11 | 565 | 298 | no |
| 10 | ST12 | 542 | 314 | yes |
| 11 | ST16 | 879 | 329 | no |
| 12 | ST06 | 734 | 290 | yes |
| 13 | ST15 | 864 | 325 | no |
| 14 | ST05 | 601 | 189 | yes |
| n/a | ST01 | 1011 | 224 | yes |
| n/a | ST03 | 1235 | 223 | yes |
| n/a | ST14 | 1877 | 218 | no |
| n/a | ST20 | 2139 | 237 | no |

The investigation initially considered the possibility of humidity in the QA environmental boxes, and it was found that 2 setups were concerned. The first concerned the 1.6 $m^3$ climate chamber used to qualify loaded staves by temperature cycling in the range −40 °C to 40 °C. As shown in figure 47, the dew point was reached for a few minutes in the proximity of the stave modules during the fast temperature ramp-up because of local restrictions to the dry air flow, even though the volume was flushed with dry air and the chamber humidity control was activated [41]. The stave electrical and mechanical integrity was not affected by the corrosion: this was confirmed by electrical characterisations and metrology surveys. For the remainder of the production, the newly loaded staves were not thermally cycled. The second problematic environmental box was that used for the stave electrical qualification at low temperature. Upgrades to improve the stave dryness and the reliability of the environmental control were made by adding dedicated interlock actions on the cooling and the power supply.



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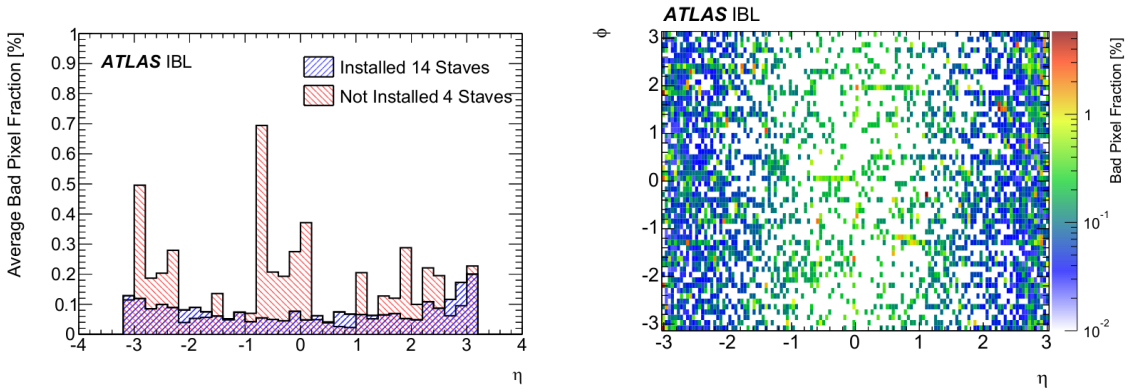
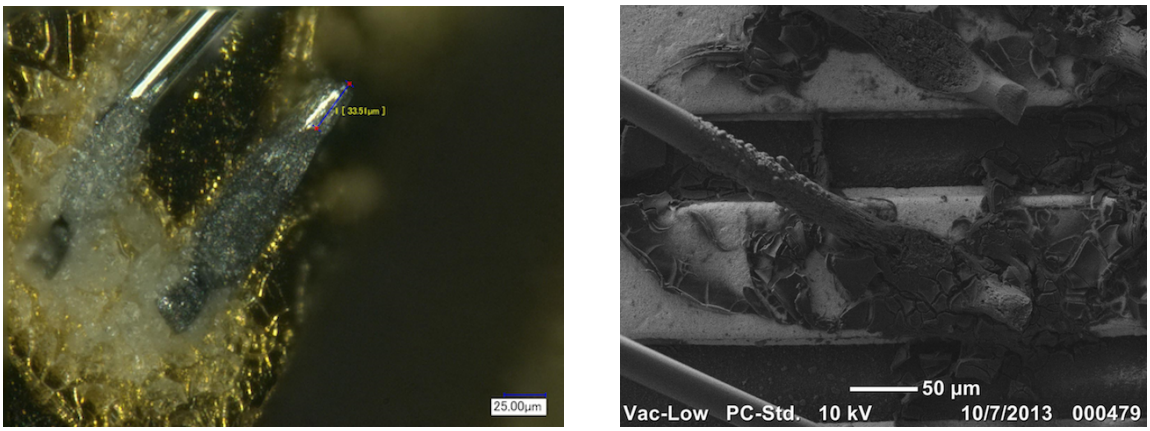



(a) (b)

**Figure 45.** Average bad pixel fraction (a) as a function of $\eta$ for installed and non-installed production staves, and (b) in the $\eta - \phi$ plane for the 14 selected staves. The stave overlap is taken into account and the fraction is computed as the number of bad pixels divided by the total number of pixels in a given bin.




(a) (b)

**Figure 46.** (a) White residue of corrosion on staves as observed under a microscope. (b) A Scanning Electron Microscopy (SEM) image of corroded wires and the corrosion residue at the foot of the bond.

### 5.4.1 Investigations of the Al wire corrosion process

The interconnection of Al wires with the Ni/Au bonding pads remains an issue even at room temperature, because of the galvanic coupling between Au and Al. During the ultrasonic wire bonding the Au layer is locally removed and the final metal contact is between Al and Ni. In addition the Al wire is normally protected by a thin oxidation layer that is formed in a few hours and that stabilises at a thickness of about 5 nm. This protective layer can be damaged in the presence of water or because of mechanical or chemical attack. If this occurs, as during the stave cold test, a corrosion process will be initiated.

The corrosion residues and Al wires were analysed (figure 48) with an Energy Dispersive X-Ray Spectroscopy (EDS) technique and the presence of C, O, Ca, Na, Cl, F at a level of up to a few percent was detected. The presence of ionic compounds indicated that the cleaning of the module flex after



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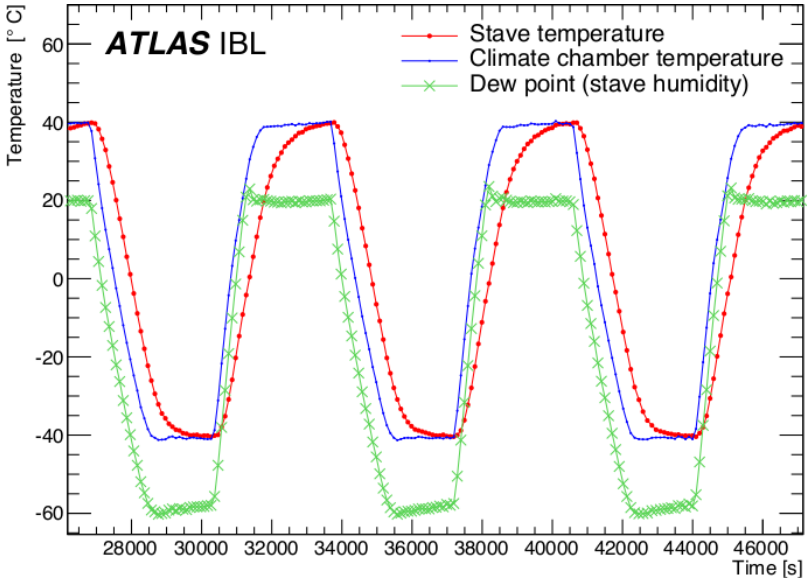
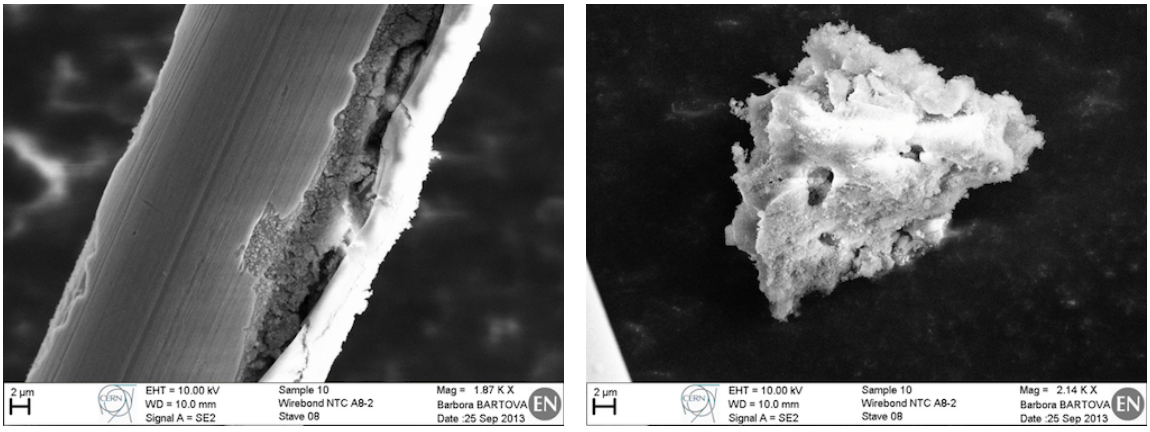



**Figure 47.** Temperature and dew point monitoring in the vicinity of stave modules during thermal cycling in the 1.6 $m^3$ climate chamber. When increasing the temperature the dew point (green curve) rises faster than the stave temperature and surpasses it for a few minutes.




(a) (b)

**Figure 48.** Images of (a) a corroded Al-wire and (b) residue taken from an affected stave. The images were taken with an Energy Dispersive X-Ray Spectroscopy (EDS) analysis setup.

SMD assembly should be improved. The corrosion process was easily reproduced in the laboratory, even in presence of de-ionised water on wire bonded samples. However, further investigations revealed that the process was even observed on ultra-clean bare flex assemblies. Additional cleaning procedures such as plasma cleaning proved ineffective in stopping the occurrence of corrosion, although its effect could be mitigated.

A sample analysis was also performed with an X-ray Photoelectron Spectroscopy (XPS), alternating the measurements with the sputtering of the Au layer with Ar ions. This probed the atomic spectrum at the Au surface while removing subsequent layers until reaching the Ni interface.



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The procedure was applied to several flex circuits delivered by two different producers.[32] On one sample fluorine was detected at a significant level (up to 14 % at a depth of 7 nm). This presence could not be understood nor reproduced in other flex circuits from the same producer.

Options considered to protect against corrosion included the potting of the bond foot and the use of spray coating such as polyurethane, but neither were possible because of the tight production and integration schedule. All wire bonds showing signs of corrosion were replaced. It was decided to leave the wire bonds unprotected, but to ensure that a safe humidity level would always be maintained during production, testing, integration and operation. Tests of the susceptibility of bond pads to corrosion are recommended before and during the production process, for all future projects.

## 6 Off-detector electronics and services

Beyond the EoS cards located at the end of the detector, off-detector electrical and optical cabling connects each half-stave to the off-detector electronics in the USA15 electronics cavern (see figure 5). Similarly, power to the module sensor and read-out electronics is routed via electrical cables from power supplies in USA15. This section summarises the off-detector read-out, control and service components of the IBL.

### 6.1 Off-detector electrical cabling

The IBL off-detector cabling consists of two parallel paths originating from the EoS region: one path is dedicated to data with a signal bundle that includes the clock and commands; the other path concerns the power distribution, including the LV, HV and DCS lines. Together, they define the Type 1 cables. The data path terminates at an opto-box that contains the opto-boards [46] at the outer edge of the ID end-plate region, while the power bundle is routed to the patch panel PP1 and then to a second patch panel PP2 located at the ATLAS periphery, as illustrated in figure 5.

As also noted in sections 2.2 and 7.3, the data and power lines are initially routed from the EoS to a cable board by a set of six intermediate flexes (2 LV, 1 clock/commands , 1 data, 1 DCS, 1 HV) that are stacked vertically. These flexes are pre-shaped into a corrugated form to partially compensate for the thermal mismatch of the cables and the supporting carbon fibre structure, given temperature excursions of up to 80 °C, from cold operation and the beam-pipe bake-out. The intermediate flexes connect to the Type 1 cables at the cable board.

The signal transmission in the data bundle uses LVDS data transmission over twisted pair cables with radiation hard polyimide insulation. The control lines, feeding the command signals and the 40 MHz clock, rely on a twisted pair of thin AWG36 copper wires each serving two FE-I4B chips. The 160 MBit/s read-out lines use one twisted pair of AWG28 copper wires per FE-I4B chip. Both the control and read-out twisted pairs adopt double quad insulation to better match the stave flex impedance and a tight twist of 4-5 twists/inch is used for better transmission quality. The data bundle runs for approximately 5 m directly to the opto-box with no intermediate junction, again to avoid transmission degradation. Due to this relatively long distance, an LVDS common-mode reference voltage control is necessary.

[32] Laboratory studies showed that the susceptibility of the flexes to corrosion was vendor dependent. In particular, the flexes used for the Pixel detector were much less sensitive to corrosion.



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Each Type 1 power bundle is split into two parts: an inner cable running for approximately 3.5 m to PP1 and a 9 m length outer cable leading to PP2. Custom 67-pin AXON[33] connectors of 21 mm diameter are used at PP1 to join the two sections.

The LV is delivered to the stave via a dedicated regulator located at PP2. These LV supply wires dominate the service material, because of the low resistance required to avoid an excessive voltage drop. FE-I4B Shunt-LDO regulators (section 3.2.1) are used, with an input voltage range of 1.8 V to 2.5 V. The resistance and voltage drops for a single LV channel serving four FE-I4B chips are shown in table 20. A minimum shunt current of 270 mA per FE-I4B chip is set to prevent excessive transient over-voltage due to a sudden current drop. The inner HV section shares a common ground return with the LV to reduce the number of EoS connectors.

Each Type 1 power bundle includes fourteen or fifteen lines for seven DCS signals. For each group of four FE-I4B chips one NTC is read out (that is 4x2 lines per half-stave). These signals are routed via the intermediate flex to the cable board. Three more signals originate from the cable board region: one NTC near the cable board itself; one NTC on the cooling pipe next to the cable board; and either a third NTC or a humidity sensor. The humidity sensor is mounted on the cable board itself and requires three lines. In the case of a third NTC, this is placed to measure the temperature of the cable bundle upstream of the cable board.

**Table 20.** Room temperature resistance and voltage drop for a single LV channel serving four FE-I4B chips at the maximum current of 0.56 A per chip (2.24 A per LV channel).

| Section | Resistance (Ω) | Voltage Drop (V) |
|---|---|---|
| Module | 0.017 | 0.038 |
| Stave flex | 0.170 | 0.381 |
| Intermediate flex | 0.035 | 0.078 |
| Cable board | 0.033 | 0.074 |
| Type 1 inner cable | 0.139 | 0.311 |
| Type 1 outer cable | 0.091 | 0.204 |
| LV regulator crate | 0.046 | 0.103 |

### 6.2 The detector control, interlock and power supply systems

A schematic of the IBL Detector Control System (DCS) and interlock hardware and functionality [14] is shown in figure 49. The inputs to the DCS and interlock systems from the power supplies, the cooling plant and the environmental monitoring are also shown.

#### 6.2.1 The DCS and interlock systems

The DCS has three main functions: to control the detector, the opto-board and the power supply operation; to monitor all operational and environmental aspects of the detector system; and to provide inputs to the power supply and interlock systems as needed for detector and operational

[33] Axon' Cables, see http://www.axon-cable.com.



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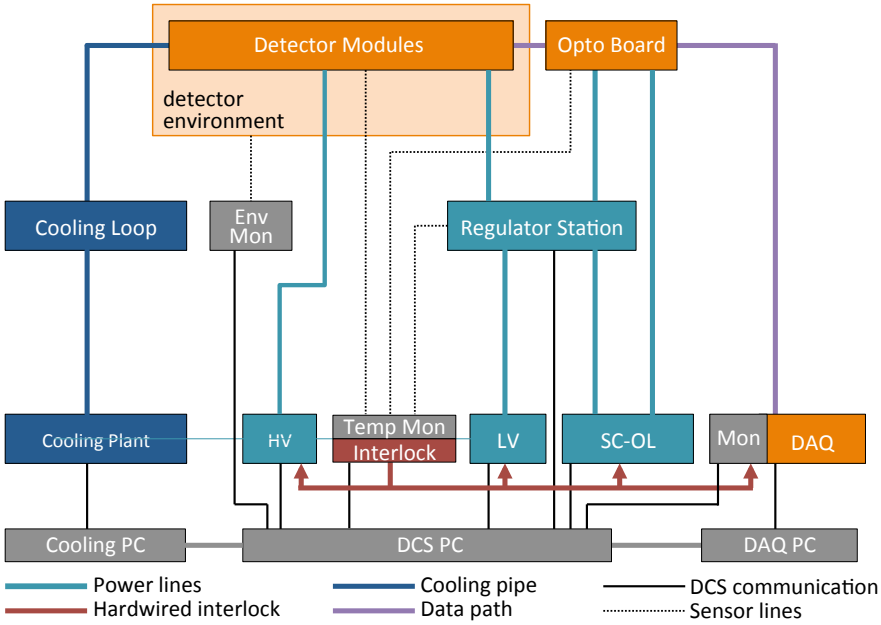


**Figure 49.** Schematic of the DCS control and monitoring functions on the sensor (HV), front-end electronic (LV) and opto-board (SC-OL) power supplies, as well as temperature and humidity monitoring. The schematic also indicates an independent hardware interlock system used for detector and operational security.

security. Most parts of the DCS are provided by dedicated PCs located in the counting room, about 100 m from the ID. The regulator station at the PP2 panel and selected monitoring units are installed inside the detector cavern.

The main component of the IBL DCS software is a Finite State Machine (FSM) that is fully integrated into the DCS of the Pixel detector and ATLAS. The tree structure of the ATLAS FSM nodes reflects the structure of the detector. Commands are sent from the top node to its children, then the status information is sent back to the top node and informs the operator about the success of a command. As all modules of a half-stave are read out through a single opto-board, the half-stave is the key element of the IBL FSM. Because of the service modularity, four FE-I4B chips with their two (planar) or four (3D) sensors are the smallest units that can be separately steered by the DCS.

The interlock system is an independent hardware implementation complementary to the DCS. The core component of the interlock system is a flash FPGA with an internal Electrically Erasable Programmable Read-Only Memory (EEPROM) . This avoids the need of a program loading at power-on. A negative logic is implemented, which means that a missing cable or lost power causes an interlock automatically. Power supply and environmental (temperature and humidity) data are fed to the DCS, and the temperature data are independently fed to the interlock system. Additional information from the laser protection system, the cooling system, the LHC or other external systems is included into the interlock matrix. As this system is completely hardware based, maximum safety is provided.



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### 6.2.2 The IBL power supplies

The detector modules and the opto-boards require dedicated powering, well adapted to the corresponding electrical loads. Common to all components is the use of floating power supplies with variable output voltages. The power supplies are controlled and monitored by the DCS, but essential security data such as over-current or high-temperature alerts are also transferred to the interlock system.

To deplete the sensors an HV power supply is required. While the planar sensors will require up to 1000 V after irradiation, the 3D sensors can be operated with significantly lower voltages of a few hundred volts.

The FE-I4B chips are powered by the LV power supplies. Because of the large currents in the FE-I4B chip, the voltage drops on the services are non-negligible. The FE-I4B chips themselves require a nominal input voltage of 1.8 V, however the LV supply is able to deliver up to 15 V. Since the FE-I4B chips would be destroyed by voltages of greater than 2.5 V, a voltage regulator close to the detector is installed to protect the chips against transients. The output voltage of each regulator can be remotely programmed to deliver precise voltages to the FE-I4B chips, via a Controller Area Network (CAN) bus in 100 steps between 1.2 V to 2.2 V. The maximum deliverable current per channel is approximately 3.4 A and each channel is protected against sense line interruption compatible with the maximum voltage drop allowed in the system. The IBL regulator station is based on the design used in the other layers of the Pixel detector [4].

The Supply and Control of the Opto Link (SC-OL) is used to power the opto-boards and requires three different low voltages. For the main supply voltage, $V_{VDC}$, the SC-OL provides a maximum voltage of 10 V at a maximum current of 800 mA. As the chips on the opto-board must also be protected, $V_{VDC}$ is routed through the regulator station in the same way as the LV. The second supply voltage, $V_{pin}$, biases the receiver PiN diodes. The supply voltage of up to 20 V provides a normal operation voltage of $V_{pin}$ of 5-10 V. The third supply voltage, $V_{Iset}$, with a maximum of 5 V, controls the current in the Vertical-Cavity Surface Emitting Lasers (VCSEL). Additionally, a reset signal is provided, which can be sent to the opto-board in case the decoder is stuck.

### 6.2.3 Temperature and humidity monitoring

The environmental monitoring is handled independently of the other monitoring tasks. Temperature sensors (NTCs) are installed in many different locations to protect detector components that might be damaged by overheating. Each Type 1 power bundle, serving a half-stave, includes fourteen or fifteen lines sending seven DCS signals to both the DCS monitoring units and the interlock system. Since the FE-I4B chips and silicon sensors can be permanently damaged by the overheating of detector modules, each sensor is also equipped with an NTC. A comparator sets a logical signal in case of overheating. In the same way, the opto-boards and the regulator station are equipped with NTCs. NTCs are also mounted on the cooling pipe and near the cable board. Finally, either a humidity sensor mounted on the cable board, or an NTC mounted on the cable bundle, is read out.

Several voltage and current diagnostic measurements as well as temperature sensors (diodes) are also built into the FE-I4B chips. An on-chip 10 Bit Analogue to Digital Converter (ADC) associated to an 8-to-1 analog Multiplexer (MUX) can be used to select and read out the temperature, power supply voltages, voltage references, detector leakage current, and other DCS analog voltages. On demand in calibration mode, this information can be sent to the DCS or through the standard



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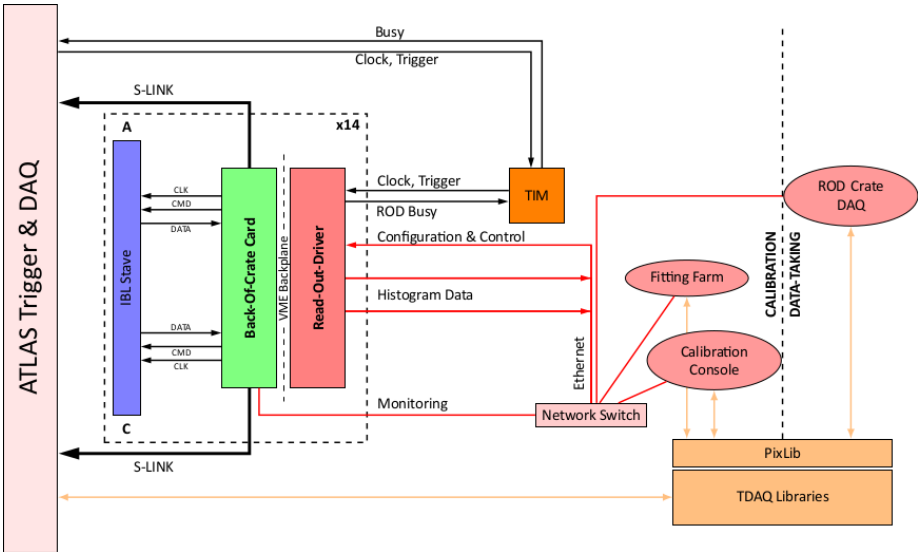


**Figure 50.** Schematic of the IBL read-out system.

data path. This monitoring strategy is not fully implemented for the IBL but remains a promising approach for future DCS developments, to reduce the material inside the detector volume.

### 6.3 Data Acquisition System (DAQ)

The IBL read-out system [15], shown in figure 50, is based on the Pixel detector read-out [4]. Each IBL half-stave is connected via the opto-board [46] and a fibre bundle to the off-detector electronics boards: the Back-Of-Crate card (BOC) [12, 13] and the Read-Out-Driver (ROD) [11].

#### 6.3.1 Optical link

The opto-board, shown in figure 51, is connected to the counting room via approximately 80 m of optical fibre. On the BOC card clock and data signals are encoded into one Bi-Phase-Mark (BPM) signal, running at 40 MBit/s, which is sent to the opto-board via a single optical link serving as TTC link. At the same time, the detector modules generate data streams at 160 MBit/s using 8b/10b encoding. The data are then sent by the opto-board via one optical link per FE-I4B chip to the BOC card.

The opto-board handles data in both directions and provides eight receiver and 16 transmitter channels. Hence, each opto-board serves a half-stave (six planar modules and four 3D modules). Each opto-board therefore contains one PiN diode array and two VCSEL arrays, with each array containing 12 channels but only the inner 8 channels are used. The PiN diode array is paired to two 4-channel Digital Optical Receiver Integrated Circuits (DORIC). The PIN diode converts an optical signal into an electrical signal that the DORIC decodes the into clock and data signals. Both signals are then transferred in LVDS format to the module. Two 4-channel VCSEL Driver Chips (VDC), driving one VCSEL array with tunable current levels, are used to route the signals via the VCSELs to the BOC card. While the DORIC is a self-adjusting chip, the VDC requires an externally tunable voltage to steer the drive current and hence the optical output power of the VCSEL. The IBL uses 28 opto-boards and two additional boards are used for a Diamond Beam Monitor (DBM) [47].



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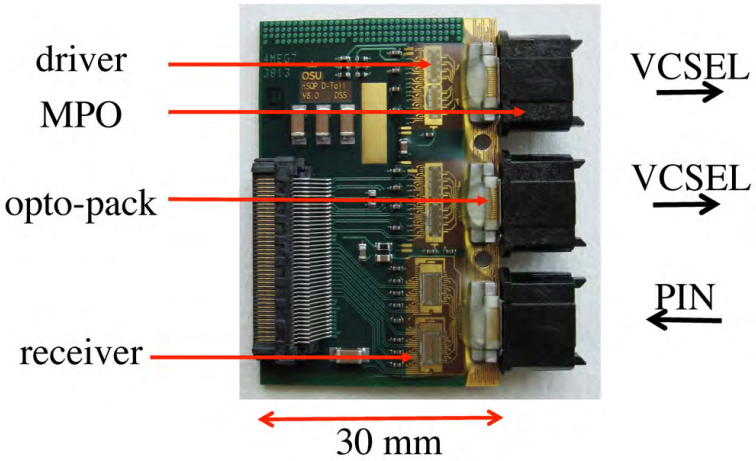


**Figure 51.** Photograph of the IBL opto-board.

### 6.3.2 Off-detector read-out electronics (ROD/BOC)

A ROD/BOC card pair is shown in figure 52. As shown in figure 50, data communication between the detector and the ROD/BOC cards is bi-directional: one control and two parallel data processing paths link the ROD/BOC pair to an IBL half-stave.

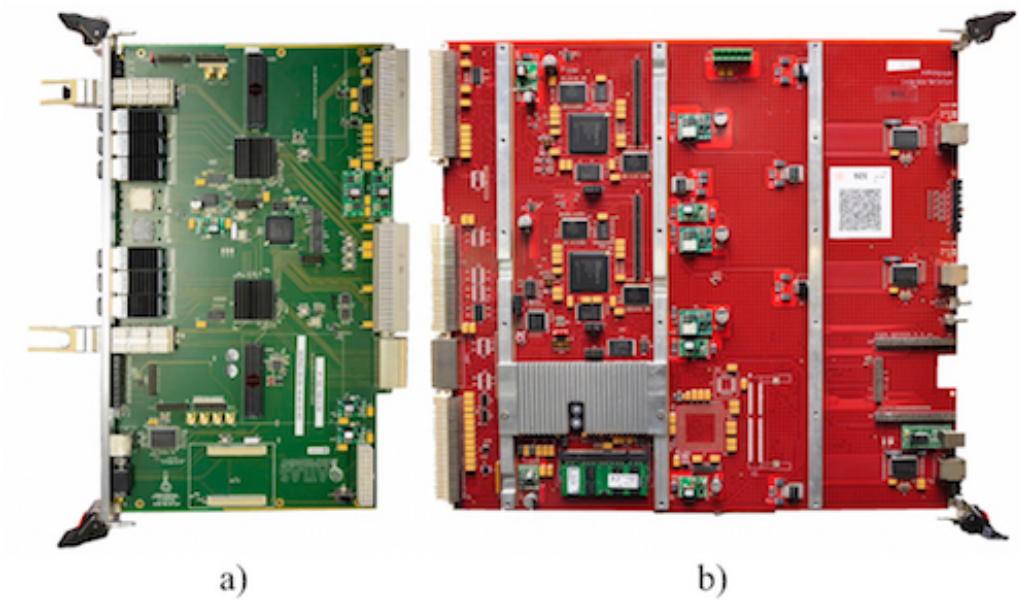


**Figure 52.** The IBL read-out cards located at the off-detector side of the optical link. (a) The BOC card and (b) the ROD card are paired in a VME crate via its back-plane.

The ROD controls the detector operation for both the calibration and data-taking modes. All of the front-end commands, including the trigger and clock signals, are generated in the ROD using a Virtex-5 FPGA with an embedded PowerPC (PPC) processor. The trigger and clock signals are



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distributed to the ROD by the Trigger Timing Control (TTC) link from the TTC Interface Module (TIM). The ROD control signals are transmitted to the detector via the BOC. An FPGA running a MicroBlaze processor on each of the ROD and BOC cards handles the Ethernet connection between them. The BOC card is interfaced to the detector and to the ATLAS read-out system: the detector interface uses commercial SNAP12 optical transmitters and receivers;[34] the read-out interface is via S-LINK connections.[35]

Each data processing path handles 16 FE-I4B chips and contains two FPGAs:[36] one on the BOC card, responsible for synchronising, decoding and processing the signal coming from the FE-I4B, and one on the ROD, which builds event fragments and packages them for transmission to the ATLAS read-out via QSFP transceivers[37] on the BOC card. The FPGA on the ROD card is also responsible for generating the histograms used to calibrate the detector. These histograms are transmitted using the Ethernet protocol to a fitting farm that uses commercial PC processors. The boot and reset of the ROD is controlled by the Program Reset Manager (PRM) FPGA, directly mounted on the ROD.

A total of 15 ROD/BOC card pairs, 14 for the IBL staves and one for the DBM, are installed in a VME crate together with the TIM module which distributes the LHC clock and the ATLAS trigger signals. The loading of the ROD firmware and software as well as the transmission of control signals and data between the ROD and BOC is performed via the VME back plane; contrary to the Pixel detector read-out, the configuration of the cards and the transmission of calibration data are performed via Ethernet. As noted above, the fitting of calibration histograms is performed using a farm of PCs instead of the on-ROD Digital Signal Processors (DSPs) used for the Pixel detector read-out. This solution provides the scalability that is required to deal with the higher bandwidth of Run 2.

The IBL read-out hardware and system architecture is being implemented in stages to read the other Pixel detector layers because of the higher allowed bandwidth. The readout of the Pixel B-Layer is equipped with twice the number of optical links, and the upgrade of Pixel Layer 1 was made at the end of Run 1.

## 7 Interfaces and integration

The insertion of the IBL pixel layer was made possible by the reduction of the ATLAS beam-pipe diameter [6]. The inner radius was reduced from 29 mm to 23.5 mm, allowing sufficient radial space for the IBL and its mechanical support structure. The new beryllium beam pipe is described in section 7.1, and the support structure is described in section 7.2. Prior to insertion in the ATLAS experiment, the full IBL as well as its services were assembled around the beam pipe on the surface (section 7.3) and electrically tested (section 7.4) at room temperature. Once installed in the ATLAS cavern, electrical and environmental connections were made. In particular, the 2-phase CO2 cooling system as well as its connection to the IBL package and its subsequent performance is described in sections 7.5 and 7.6.

[34]The SNAP12 Multi-Source Agreement (May 2002) outlines specifications for the mechanical, electrical and optical interfaces of 12-channel pluggable parallel optical transmitter and receiver modules.

[35]S-LINK, for simple link interface, is a high-performance data acquisition standard developed at CERN.

[36]Unless otherwise specified, all FPGAs are from the XiLinx Spartan-6 family.

[37]The Quad Small Form-factor Pluggable (QSFP) is a hot-pluggable transceiver allowing data rates of 4x10 Gbit/s.



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### 7.1 The beryllium beam pipe

The new beam pipe was designed and fabricated with a length of 7300 mm, including the flanges (which were unchanged). The beryllium section is 7100 mm long with a nominal wall thickness of 0.8 mm. It is installed symmetrically with respect to the interaction point. At each end of the beam pipe, split aluminium flanges of 100 mm are welded, compatible with an insertion inside the IBL Inner Positioning Tube (IPT). The inner surface of the beam pipe is treated with a Non-Evaporable Getter (NEG) thin film coating to optimise the vacuum quality. The NEG coating is activated by heaters that are wrapped along the beam-pipe length for the bake-out. A bake-out is made each time the ultra-high vacuum is established. The heater temperature is monitored and controlled by thermo-couples installed along the beam pipe. To reduce possible damage to the IBL layer, the infra-red emissivity of the beam pipe is reduced by a surface layer of aluminium.

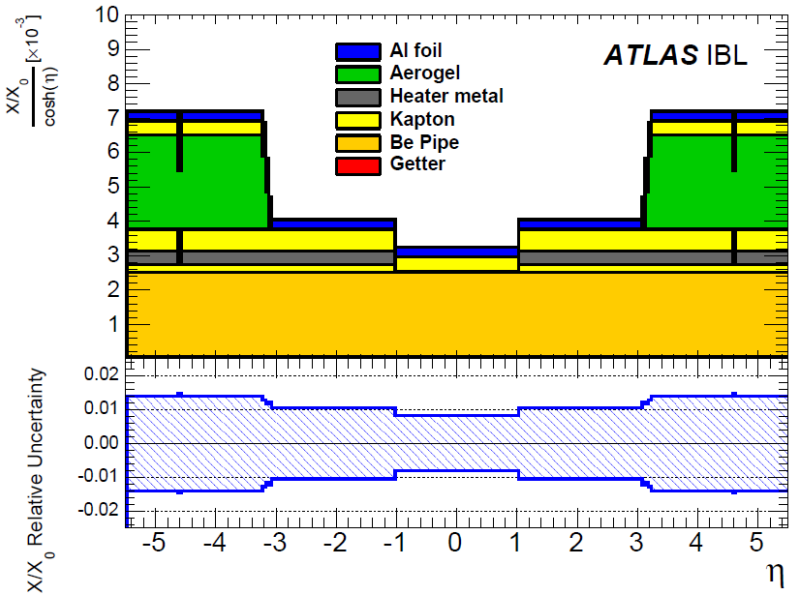


**Figure 53.** The calculated radiation length $X/X_0$ of the new beam pipe normalised by $\cosh^{-1}(\eta)$ as a function of $\eta$. The lower plot shows its relative uncertainty. The Getter (NEG) contribution is small and is not visible.

The composition and radiation length of the new beam pipe were both carefully validated. The thickness of the beryllium pipe was measured with a precision of ±2.5 µm for eight positions along each section of the pipe, and the average thickness was measured to be (0.8683 ± 0.0032) mm. The other components of the beam pipe (Kapton®, heater metal, aerogel, aluminium foil) were individually measured by $^{109}$Cd (22 keV) X-ray absorption and their nominal composition and thickness were confirmed to within a few percent precision. The total uncertainty of the radiation length considers not only the material composition, but also fabrication details such as wrinkles of the Al foil.

As a result, the total thickness of the beam pipe was calculated to be 0.32 % $X_0$ at the centre of the beam pipe and up to 0.72 % $X_0$ at 1.5 m from the centre, as shown in figure 53. The main reduction of material thickness was the removal of the aerogel insulating layer over a length of 622 mm at the centre of the beam pipe.



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As a cross-check, the fabricated beam pipe was scanned using X-rays at $z$ positions of 2.2 cm, 25 cm, and 90 cm along the beam pipe. The scanning equipment, shown in figure 54, was mounted on a multi-purpose container (MPC; see section 7.3) supporting the beam pipe. The X-ray assembly

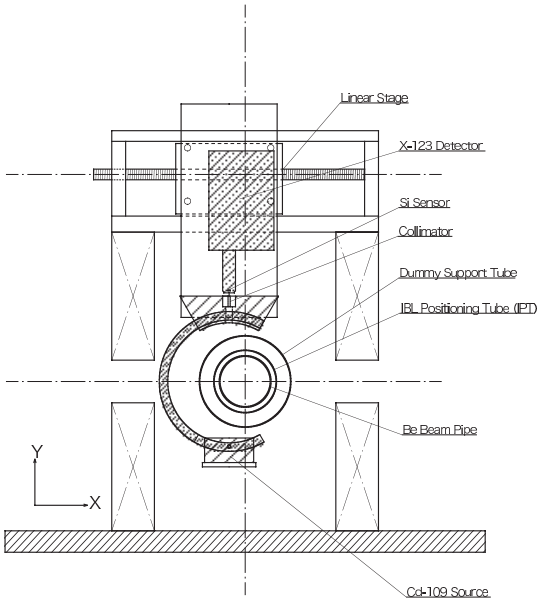


**Figure 54.** Beam pipe X-ray scanning equipment.

included a fully-depleted Si-PIN X-ray counter (Amptek X-123[38]) and a vertically collimated $^{109}$Cd source. The source and detector could slide together horizontally, maintaining a constant X-ray flux. The relative X-ray absorption at $z = 2.2$ cm is shown in figure 55 as a function of the horizontal position. An X-ray absorption model, parameterising the absorption coefficient of the layers and the absolute X-ray flux, is in good agreement with the data. Similar validation results were obtained for $z = 25$ cm and $z = 90$ cm.

### 7.2 The inner mechanical structure of IBL and its external envelope

As shown in figures 2 and 3, the IBL volume for the stave and services is delimited by the Inner Support Tube (IST), which is fixed on the Pixel structure, and by the IPT, which is a precision mechanical support to hold the staves and the services. A schematic and photograph of the IPT are shown in figure 56.

The IST is a 6600 mm long tube with an inner diameter of 85 mm and 0.455 mm wall thickness, containing the full IBL package and the central portion of the beam pipe. It is secured to each end of the Pixel detector frame in the PP0 area and to the pixel cruciforms in the PP1 region, located at respectively 728 mm and 3241 mm from the interaction point along the beam axis. Given the clearance of only ~2 mm with respect to the Pixel B-Layer, the IST is designed to have a minimal deflection during its lifetime. It was therefore manufactured using very high modulus carbon fibre

[38] Amptek X-123 Si-Pin X-ray counter, see www.amptek.com.



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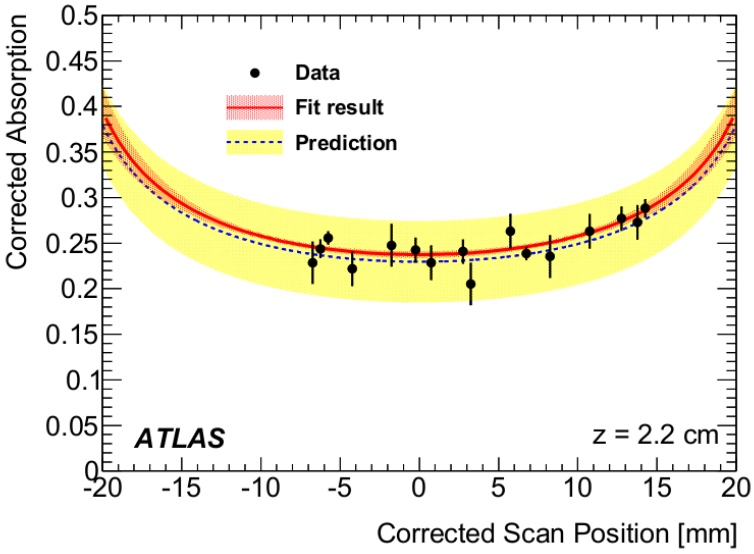
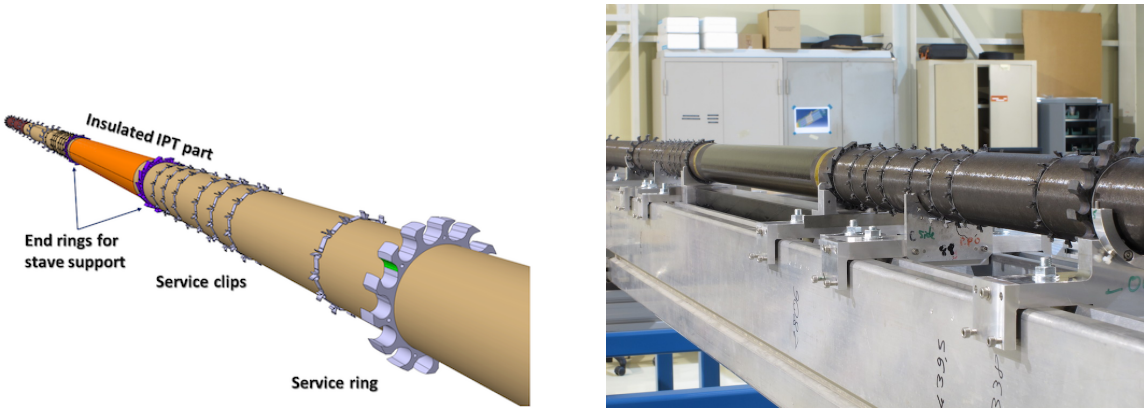



**Figure 55.** Relative amount of X-ray absorption in the beam pipe as a function of the corrected transverse scan position, at $z = 2.2$ cm.




(a) (b)

**Figure 56.** (a) Sketch and (b) photograph of the Inner Positioning Tube (IPT) assembly before the integration of staves and services.

(K13), coupled with cyanate ester resin (RS3). The carbon-fibre material consists of seven 65 µm-thick plies oriented in different directions to minimise the tube deflection. The thermo-mechanical behaviour of the complete package was precisely predicted by finite element analyses and validated with experimental data.

The IPT is a precision assembly of carbon fibre tubes and rings (figure 56a) that aligns the 14 staves with high precision. The five carbon-fibre segments use the same carbon fibre material as the IST, but the central segment uses five plies to minimise the material budget; the resulting thickness is 0.355 mm. In addition, to ensure electrical insulation with respect to the stave module HV, this central segment is co-cured with a 25 µm-thick polyimide film. The service rings, each with 14 radial grooves for the stave services, are precisely positioned every 50 cm along the IPT. A small



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extra length, estimated to be ~3 mm, compensates for the service cable contraction and extension during temperature excursions.

A key feature of the IPT design is the ability to perform a fast insertion or extraction of the IBL and of the beam pipe independently of the rest of the ATLAS ID. The IPT is locked in z with respect to the Pixel structure at a distance of 3241 mm from the interaction point on the C-side, and is positioned radially within the limited clearance to the IST, which is fixed to the Pixel frame. The beam pipe is positioned in z with respect to the LArg Cryostat at PP1, 3426 mm from the interaction point. It is positioned radially within the limited clearance to the IPT and the Liquid Argon cryostat at PP1.

Two titanium terminals are positioned at the IPT extremities. Their function is to provide shielding from electromagnetic interference, strain relief for the cooling fittings, space for cable bundle integration and mechanical stability during installation. The gluing of components on the IPT was performed using epoxy glue (Hysol 9394[39]) that can cure at room temperature and has a maximum service temperature of 177 °C. This guarantees the integrity of all the parts, even during the beam-pipe bake-out when the maximum temperature is expected to reach 110 °C at the contact points with the beam-pipe rings.

Two units were manufactured for each of the IST and the IPT and were surveyed in a metrology laboratory to check for geometrical defects and qualification. The best assemblies with respect to geometrical specifications were used for the IBL integration.

### 7.3 Surface integration and installation

The elements to be integrated can be grouped in three independent sets: the IPT with the support rings, the staves with their cooling pipes and the services.

The Multi-Purpose Container (MPC), the mechanical support for the IBL integration, was designed to allow secure and precise stave integration, and to transfer the IBL package to the experimental cavern. Initially, the beryllium part of the beam pipe was inserted inside the IPT. A precision tool was then used to transfer the staves from their holding jigs to the IPT, preserving the tight clearances with respect to the surrounding structures. After each stave was connected to the cooling extension (section 7.6), it was fixed to the integration tool of the MPC (figure 57). Using adjustable screws on the stave integration arm, and IPT rotations referenced with precision pins, each stave could be installed and transferred from the handling frame to the support ring of the IPT with a precision of ~50 µm over the ~724 mm length.

Once the 14 staves were loaded, a central ring consisting of seven parts was installed and clipped to the central stave support feet, providing an additional stiffening. However, because of stringent construction and thermal fixation constraints, it did not eliminate all possible detector degrees of freedom. It radially stiffens the 14 staves at the centre, while leaving free movement in the azimuthal direction and along the beam axis. Operationally, this resulted in an R-$\phi$ distortion of the staves at the level of a few µm/°C (section 8.2).

The services that connect the staves to each ID end, ~3.5 m from the interaction point, were installed after the integration of each stave. The service installation consists of eight intermediate flex circuits linking Type 1 cables to the stave flex in the PP0 region (section 6.1). The Type 1 cables service the HV and LV power, the read-out and the DCS signals and are laced in a single bundle that

[39] Hysol® is a trademark of Henkel Corporation, see www.henkel.com.



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**Figure 57.** Integration of a stave mounted on a handling frame and the integration arm which is mechanically aligned to the Multi-Purpose Container (MPC).

splits just before exiting the IBL volume into separate data and power bundles. After the installation of each stave and their services, electrical qualification tests were performed, before proceeding to the next row. All the staves were successfully integrated without rework or re-installation.

The next operation consisted of inserting soft sealing rings at the two extremities ~3 m from the interaction region to guarantee a proper environment for the IBL. The IBL is flushed with dry nitrogen gas at a flow rate of up to 450 $\mathrm{l\,h^{-1}}$. This ensures a dew point below that of the minimal foreseen coolant temperature of −40 °C, keeping the detector dry under all operating conditions. The sealing ring core is moulded as a ring from polyurethane, with holes for electrical and cooling services. During cavern commissioning, the full dry nitrogen circuit, including sealing rings, was leak checked. At the nominal running parameters (80 $\mathrm{l\,h^{-1}}$ at 20 mbar at maximal overpressure), the measured outlet flow was 75 $\mathrm{l\,h^{-1}}$, equivalent to a nitrogen circuit tightness of better than 90 %.

Once the integration was completed, the services (including an additional length of 1 m for the power bundle and 2.6 m for the data bundle) were packed to ensure the IBL envelope for installation in the ATLAS cavern. In particular, the Type 1 bundles from PP1 to PP2 were wrapped by a spiral wrapping tool around the beam pipe (figure 58) until the IBL package was inserted inside the IST.

### 7.4 Electrical tests after stave integration

The purpose of the stave electrical test after integration of the staves onto the IPT, cabling of the Type 1 cables and insertion inside the IST, was to verify the electrical and functional integrity of the stave components and to test the service chain. The stave test included threshold scans with and without sensor bias, a validation of the time-over-threshold (ToT) setting, and an I-V scan. The tests were directly compared to results obtained during the stave QA. A sample of these comparisons is shown in figures 59, 60 and 61. Noise and threshold values are larger than in the stave QA because the detector was not cooled during the stave loading. This is especially true for 3D modules, which are more sensitive to temperature. With that caveat, no performance degradation was measured.



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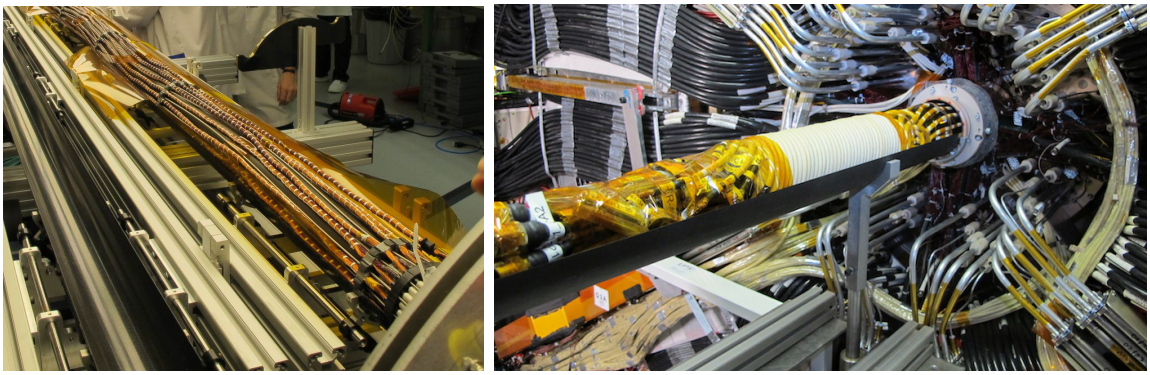

(a) (b)

**Figure 58.** (a) Type 1 services integrated on the Inner Positioning Tube (IPT) and Z-stopper locked into the service rings. (b) Spiral wrapped Type 1 cables that take up the excess length of the IBL envelope and limit the radial envelope with respect the Inner Support Tube (IST) for the insertion.

The tests also revealed several hardware problems (e.g. broken or shorted lines in the Type 1 cable or in the intermediate flex) that were repaired. The tests were repeated after sealing the IBL volume with two soft polyurethane disks, to check the correct functionality of all modules before wrapping the services and lowering the detector in the cavern of the ATLAS experiment. No changes with respect to previous tests were measured.

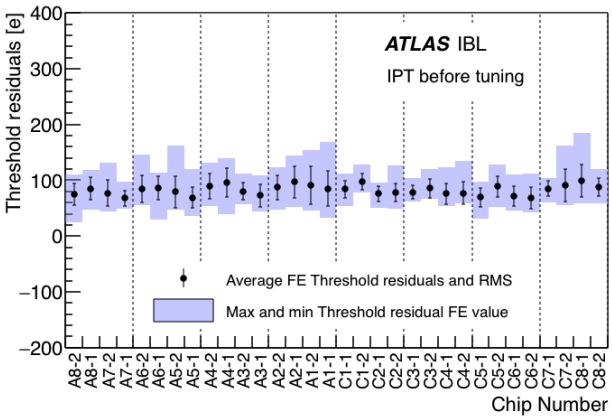


**Figure 59.** Average and RMS of the chip-to-chip FE-I4B threshold difference between the results of the connectivity test after integration around the IPT (IBL positioning tube) and the individual QA values for the 14 staves. The QA configuration setting targeted 3000 $e^-$ and 10 ToT at 16 $ke^-$. Maximum and minimum FE-I4B threshold mean values of the 14 staves are represented for each chip number (position on stave) by the filled area.

In parallel to the stave integration and test, a system test was prepared using two prototype IBL staves and either production or pre-production detector services, the full power and DCS chain, but mono-phase cooling. The measured noise, threshold and ToT performance were in excellent agreement with the QA. Scans were made using $^{241}$Am and $^{90}$Sr sources, as well as cosmic rays, with satisfactory results. The system test also confirmed the functionality of the interlock system. The system test setup continues to be used as a test-bench for operational maintenance and upgrades.



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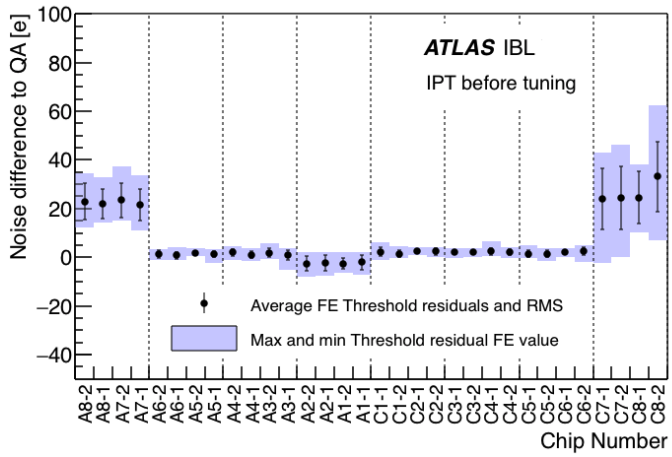


**Figure 60.** Average and RMS of the chip-to-chip FE-I4B noise difference between the results of the connectivity test after integration around the IPT (IBL positioning tube) and the individual QA values for the 14 staves. The QA configuration setting targeted 3000 $e^-$ and 10 ToT at 16 $ke^-$. Maximum and minimum FE-I4B noise mean values of the 14 staves are represented for each chip number (position on stave) by the filled area (the four outer chips on each side, using 3D sensor technology, show an increased noise behaviour).

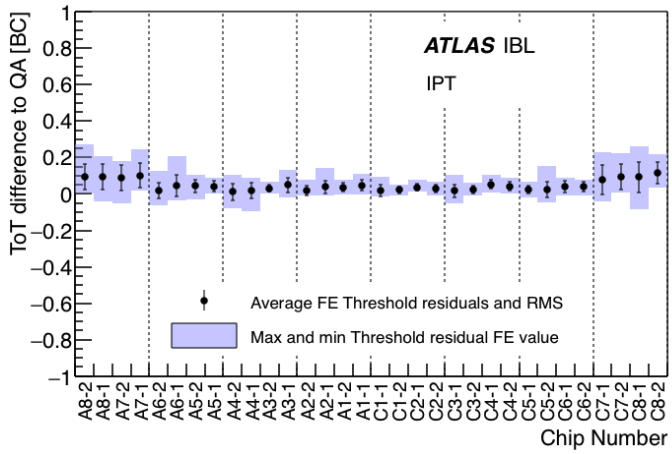


**Figure 61.** Average and RMS of the chip-to-chip FE-I4B ToT mean values between the results of the connectivity test after integration around the IPT (IBL positioning tube) and the individual QA values for the 14 staves. The QA configuration setting targeted 3000 $e^-$ and 10 ToT at 16 $ke^-$. Maximum and minimum FE ToT mean values of the 14 staves are represented for each chip number (position on stave) by the filled area.

### 7.5 $CO_2$ cooling system

The cooling of the IBL detector is based on $CO_2$, which is circulated in a closed system through the detector with an overflow where part of the liquid is evaporated (approximately 30 % at 1.5 kW) [44]. The two-phase liquid-vapour mixture is returned to the cooling plant, which is located in the USA15 service cavern and easily accessible. The cooling plant condenses the returning two-phase $CO_2$ using a commercial chiller. The liquid $CO_2$ is pumped back to the manifold system near the IBL detector via a concentric transfer line that bridges the distance between the cooling plant in USA15



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and the manifold in the UX15 service cavern. Figure 62 shows a simplified schematic of the IBL cooling system with the main components of the cooling system highlighted.

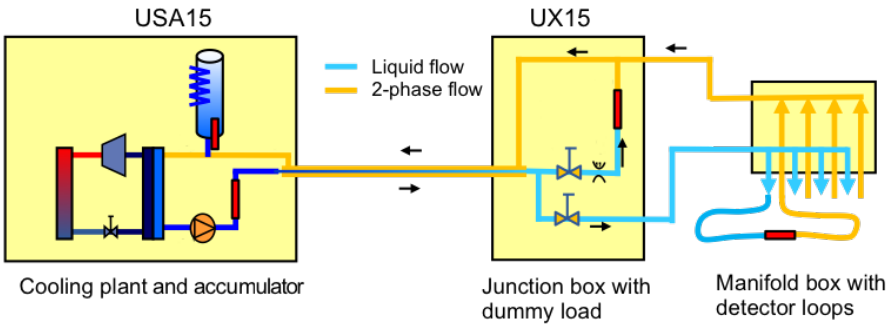


**Figure 62.** Simplified scheme of the IBL cooling system. USA15 and UX15 refer to the service caverns where the equipment is installed. The junction and manifold boxes are separated from the cooling plant by approximately 80 m.

### 7.5.1 Cooling system operation

The $CO_2$ arriving in the detector is a saturated liquid, which means that it evaporates directly when heat is applied. The temperature of the arriving saturated liquid is a function of the pressure, which is controlled by the cooling plant in U.S.A.-15. Changing the temperature of the two-phase mixture in the accumulator will change the pressure in the system and allows operation with an evaporation temperature between 15 °C (used for commissioning) and −40 °C.

The pressure can also be increased to fully liquify the system. This is used at start-up to prevent thermal shocks. The cool-down temperature ramp is controllable and can be set to 2 °C per minute, or to a lower rate. The preferred inlet condition of the cooling is that the liquid is saturated in the IBL stave region, so that heat needs to be applied to the cold liquid. This heat is taken out of the returning two-phase mixture by a constant thermal contact of the liquid inlet and the two-phase return. The inlet and outlet fluids circulate in concentric tubes (the inlet liquid in a 10 mm inner diameter tube, and the outlet fluid circulating in a 21 mm outer diameter tube). The actual system allows having the same temperature at the detector and at the two-phase temperature controlled by the accumulator. The higher pressure on the inlet keeps the $CO_2$ liquified at the inlet to the cooling tubes. It starts boiling in the cooling tubes of the IBL staves once powered. This liquid temperature condition works over a large range of operational temperatures and makes the control of the system, without active elements inside the ATLAS detector, very reliable in a hard-to-access region. The first tests allowed the system to reach stable temperatures for various heat loads and was tested up to a thermal load of 3 kW and down to −40 °C (figure 63).

### 7.5.2 Redundant system

Once irradiated, the IBL must remain cold at all times to limit the radiation damage in the silicon sensors. To guarantee a fail-safe solution for the $CO_2$ cooling a redundant system has been developed. There are two identical plants where one serves as a full back-up of the running plant. Each plant has its own control and sensor system with a dedicated Programmable Logic Controller (PLC) and



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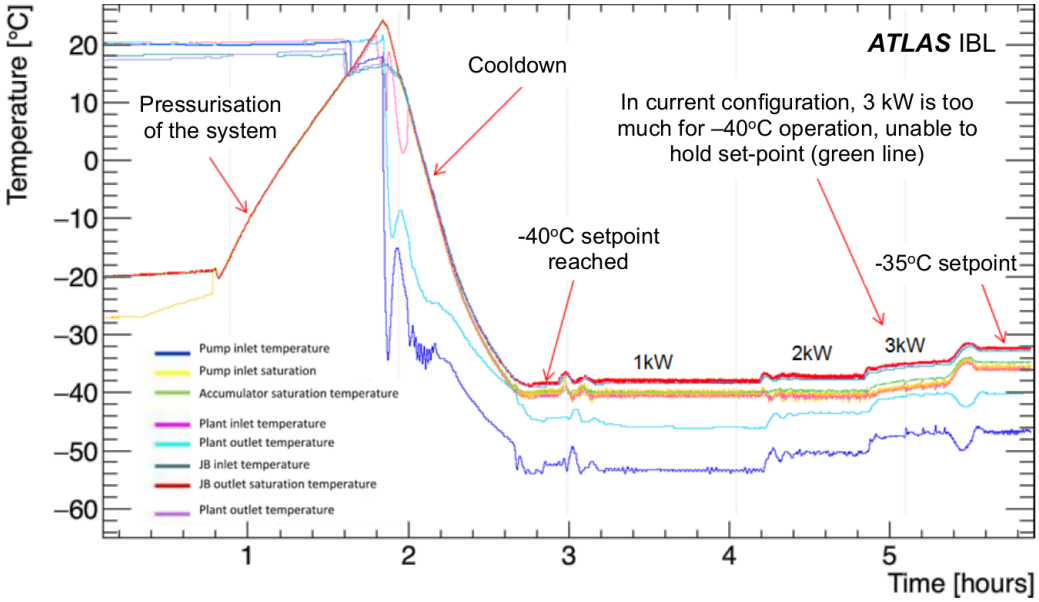


**Figure 63.** Temperatures measured at start-up and cold operation of the $CO_2$ cooling system with various thermal loads applied at the junction box located several meters from the IBL.

power source. The transfer lines and the accumulator are shared with respect to the $CO_2$ volume. A plant can be disconnected from the main system for interventions. Both chillers are cooled by water provided from the central ATLAS water system. An integrated air cooling condenser is present in each chiller unit to back-up the single source water cooling. During operation, one system can remain on standby for a fast switch-over in case of a system failure. In addition, for greater safety, the two plants can operate in parallel increasing the cooling capacity, but this operational mode is mainly foreseen for the beam-pipe bake-out.

### 7.5.3 Detector distribution

A homogeneous $CO_2$ flow distribution to the 14 IBL staves is achieved by 11 m long lines and 1 mm inner diameter capillaries (figure 64). These capillaries are routed inside the return tubes of the IBL to be shielded from ambient heating. The manifolds are located in the muon detector area. The total tube length from manifold through the IBL and back to the return manifold is approximately 32 m ($2 \times 11$ m concentric tubing, $2 \times 4$ m connection tube and 1 m stave tube). The inlet tubes, the boiling channels and outlet tubes have nominal inner diameters of 1.5 mm, 1.5 mm and 2 mm respectively. The innovative vacuum isolated flexible lines were used for the fluid transfer on long distances [44]. The concentric return tubes in the flexible transfer line have a diameter of 3 mm. The 11 m concentric line is outside of the ID volume and is insulated by multilayer insulation inside a 16 mm diameter vacuum metallic tube. This triple concentric assembly is flexible and is routed similarly to the electrical cabling, through the ID end plate region towards the manifold. The flex lines inside the ATLAS ID end plate up to the splitter box are shown on figure 64(b).



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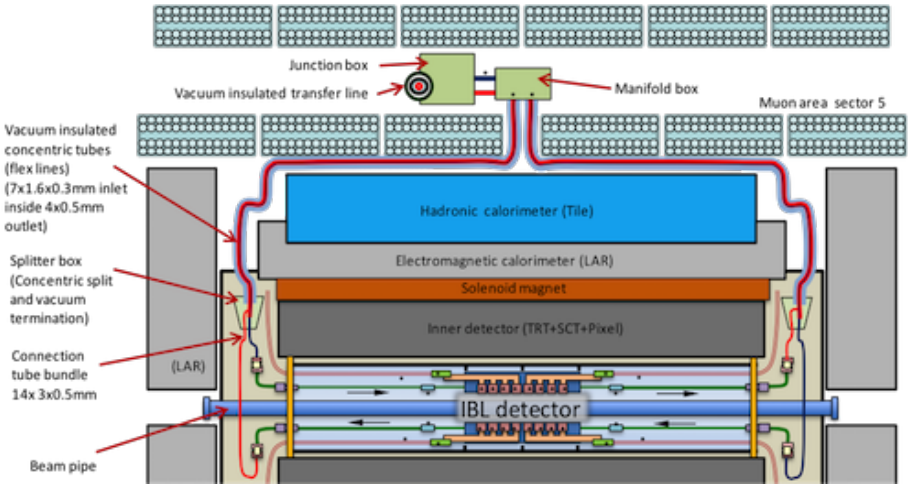
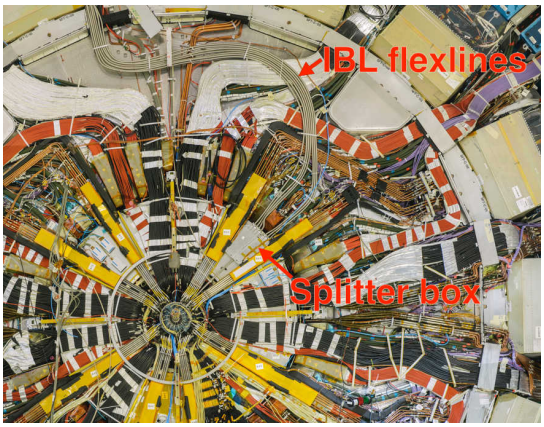



(a)




(b)

**Figure 64.** (a) $CO_2$ distribution concept inside the ATLAS detector. (b) Flex cooling lines integrated inside the ID flange and connected to one end of the IBL detector package via Splitter box.

### 7.5.4 Commissioning

The commissioning of the system started in January 2014 with local circulation of $CO_2$ using the plant internal dummy load. Near the manifold the so-called junction box is present (figure 64) where the flow can be by-passed through a 3 kW dummy load. The system commissioning was made using this dummy load with a restriction valve having a similar flow resistance to that of the detector loops. One of the main challenges for the IBL cooling was related to the colder temperatures compared to previous cooling systems. The requirement of cooling to −40 °C brings the margin close to the $CO_2$ freezing point (−56 °C) and hence a very stable primary cooling was needed. In the early phase the system was tuned such that under extreme conditions it remained within safe operational boundaries. The measured heat load was approximately 2 kW at −40 °C and 3 kW at −35 °C. The IBL detector was also successfully tested during the commissioning at various temperatures with the nominal power load expected during operation. The boiling onset inside the IBL cooling loops sometimes had problems to be correctly initiated. In this case, super-heated liquid, that is warmer



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than the boiling temperature and has a worse heat transfer than the desired two-phase flow, could be present in the detector. As a result, the temperatures of the first modules of a stave were sometimes a few degrees higher. To mitigate this problem, flow restrictions were applied in the inlet manifold to reduce the flow and to keep the inlet pressure high [44].

### 7.6 On-detector cooling branch and interfaces

The on-detector cooling branches consist of a 7 m length straight section of titanium pipe with two brazed junctions at each side of the stave and a dis-mountable fitting at each end (figure 65). As for the rest of the IBL services, the detector side of the fitting must respect the insertion envelope. The branch is connected on each side to a short 90 °-bend section of Ti pipe, which is brazed to an electrical break and to a stainless steel pipe at the other end. The stainless steel pipes are then routed on a path specific to each stave to a splitter box where the transition is made to 16 mm flexible vacuum transfer lines of 11 m length connected to a manifold box further out from the ID.

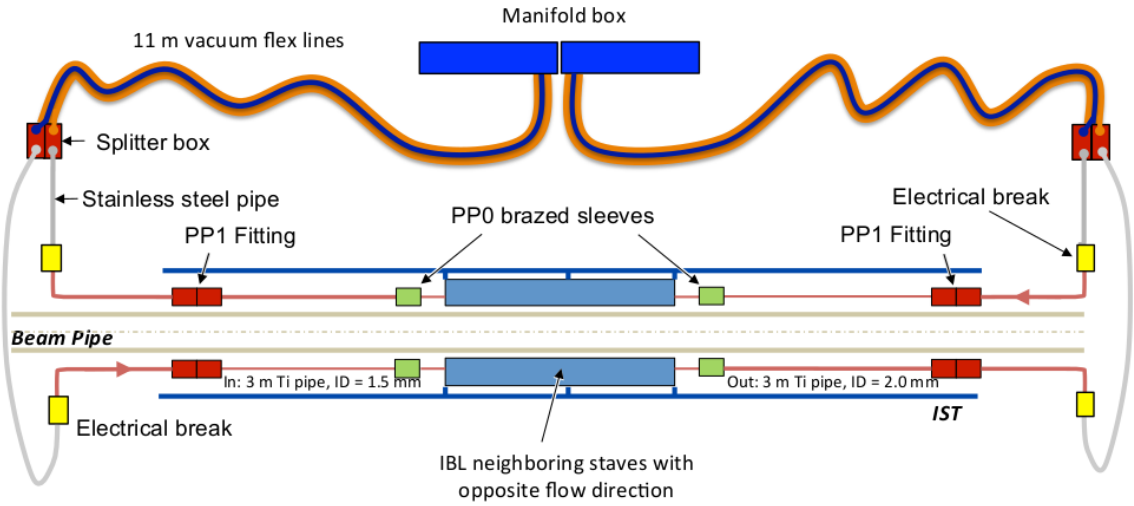


**Figure 65.** Not-to-scale schematic view of the IBL cooling distribution line inside the ID volume.

#### 7.6.1 Fittings outside the IBL volume

Because of space constraints for the insertion of the IBL inside the IST, the electrical and cooling service envelope is restricted to a maximum external radial space of 4 mm. An industrial fitting of such a small size compatible with the pressure, the radiation hardness, and the reliability requirements of the IBL does not exist; therefore a custom fitting was developed.

The use of the $CO_2$ evaporative system (section 7.5) together with titanium as a selected material for both the tube and the fitting required a special engineering and design development to maximise the reliability. The extreme radiation environment excludes the use of organic joints, leading to a metal-to-metal contact solution. The requirement led to the selection of a hard titanium alloy (TA6V, or grade 5) to guarantee the sealing. The tightness is ensured by a cone-sphere junction, with strict requirements on the surface quality.

Prototype fittings were assessed with several batches of ~10 fittings machined in-house and tested to qualify the final design. The final production batches were manufactured in industry



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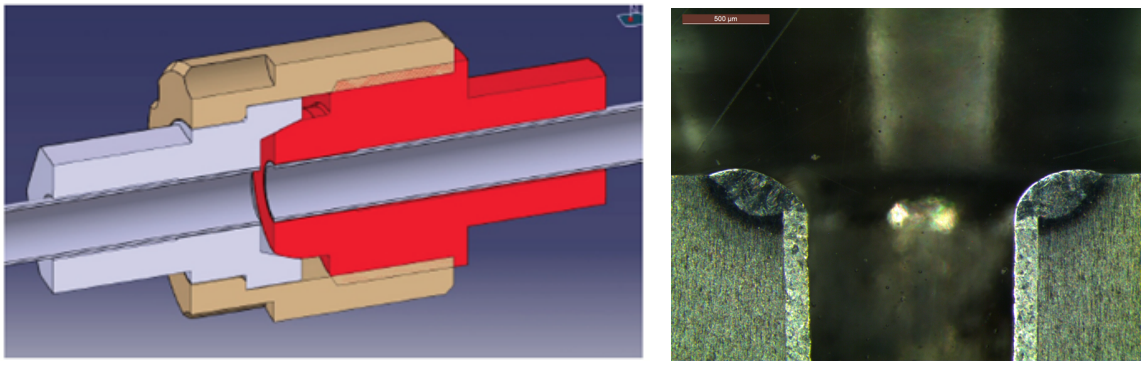

(a) (b)

**Figure 66.** (a) Cross-section drawing of the PP1 fittings and tubes. (b) Cross-section photograph of the electron beam welding of the titanium pipe with the fitting gland.

and qualified in-house on a large number of test samples. The fitting is connected to the thin titanium pipe (0.11 mm wall thickness) by electron beam welding at the front face (figure 66). This welding requires high quality vacuum and was performed in industry. The method imposes strict requirements on the reliability of the fitting which can not be repaired. A large-scale qualification and validation campaign was carried out, with ~100 fittings leak tested, some of them mated and de-mated tens of times. An industrial qualification procedure was applied to fulfil the standard requirements with large statistics pressure cycling. A set of ten fittings, electron-beam welded to short-pipe sections and connected in series, was tightened by the collaboration and sent to a certified ISO qualification lab to perform the pressure cycling (one million water cycles with 1 bar to 100 bar at ~1 Hz). The entire set successfully passed the leak tests. The minimal torque required for reliable tightening was determined during the qualification campaign. A 2 N m torque was sufficient to guarantee the success of tests like fast temperature cycling or thermal shocks using a $CO_2$ blow-off system. A small subset of fittings was tested at higher torque up to 6 N m without visible damage. The final torque used for installation in the cavern was 2.5 N m for which all the 28 IBL connections passed the pressure tests at 100 bar.

The pre-series consisted of producing approximately 100 samples for qualification. The 28 fittings selected for installation were visually inspected for scratches and dust, and individually leak-tested.

### 7.6.2 The cooling line electrical break

The grounding and shielding scheme of the IBL requires using electrical breaks on the cooling pipes at the PP1 area (figure 67) and in the ID end-flange region. Because of space constraints the closest possible location was just after the 90 °-bend of the radial section of the pipe. The mechanical stress in this section is significant; a relatively large diameter (8 mm) ceramic electrical break was chosen for robustness. At this location it is also necessary to make the transition from titanium pipes, which are difficult to bend, to stainless steel pipes, which are easily routed. After testing several options for the titanium to stainless steel transition the most reliable solution found was to braze in the same processing step a stainless steel sleeve on the external side of the ceramic of the electrical break (the detector side of the ceramic being brazed in a titanium sleeve). Due



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to the mismatch of the thermal expansion coefficient between the ceramic and the stainless steel material the brazing is a delicate process. A full qualification in collaboration with industry was performed to design and produce a reliable junction. The qualification process was the same as for the fitting and a number of destructive tests were made to evaluate the mechanical robustness and the capillary penetration of the brazing material. All the tests were passed successfully and the tensile tests at the electrical break junction revealed that the pipe was weaker and that the junction withstands at least 640 bar internal pressure (limited by the test setup). In addition, a few electrical break samples were irradiated to 250 Mrad with a 10 MeV electron beam, corresponding to the expected maximum end-of-life IBL ionising dose, and found to be leak-tight.

**Figure 67.** The cooling line electrical break in the ID end flange service region.

### 7.6.3 The brazing junction of the stave inside the detector volume

At PP0, the cooling junction connects the staves to the cooling extension running from 705 mm to 3366 mm (PP1 region) from the interaction point. This junction was designed such that the stave production could be made with 1500 mm long objects, easing the module loading task, the testing tool, the handling and the shipment. Due to the limited space around the beam pipe in the PP0 region, and the high level of reliability required inside the detector volume, the use of fittings was not possible.

One major impact of this design choice was to develop a thin wall (0.11 mm) titanium pipe joining technique between the extension and the stave pipe which could be easily connected after module loading and before integration of the staves around the IPT. When such an operation is performed after the module loading, the requirements are not only based on the quality of the welded junction but also the risk of damage to electrical or mechanical components (that should be negligible). Therefore techniques that require excessive heat spread, such as oven brazing, or high and fast current spikes such as orbital welding, were prohibited. With such a thin wall thickness, titanium is not an easy material to weld or braze. Since it is highly sensitive to oxygen, welding or brazing requires an inert environment, e.g. argon, or vacuum. Induction welding was the only technique (figure 68) found that uses local heating, does not involve current spikes on mechanical structures, and has a reasonably sized tool that does not risk damage to the front-end electronics.

The brazing compound or filler used was Palcusil-5 (Ag 68 %, Cu 27 %, Pb 5 %). The brazing process was performed at 820 °C to 825 °C in vacuum ($<8.1 \times 10^{-6}$ bar ) for several seconds, with



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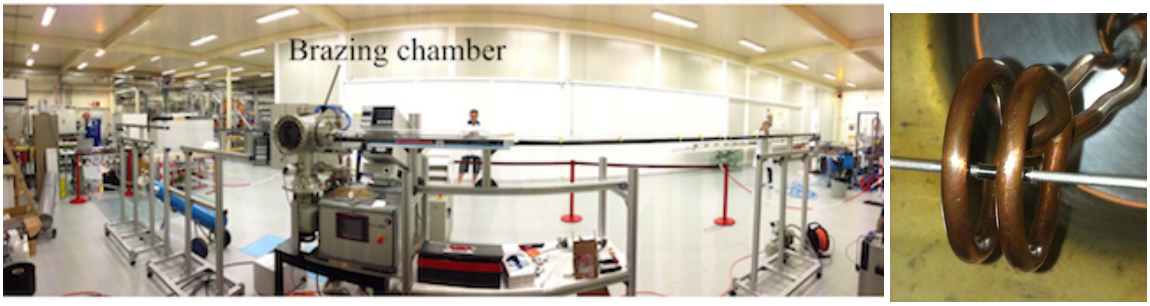


(a) (b)

**Figure 68.** (a) Brazing setup for the extension of the cooling pipe from 1.5 m to 7 m. (b) The inductor head located in the vacuum chamber.

a well defined ramp-up (figure 69). Prior to the chamber and the pipe vacuum pumping, argon is flushed to minimise the presence of oxygen around the brazing point.

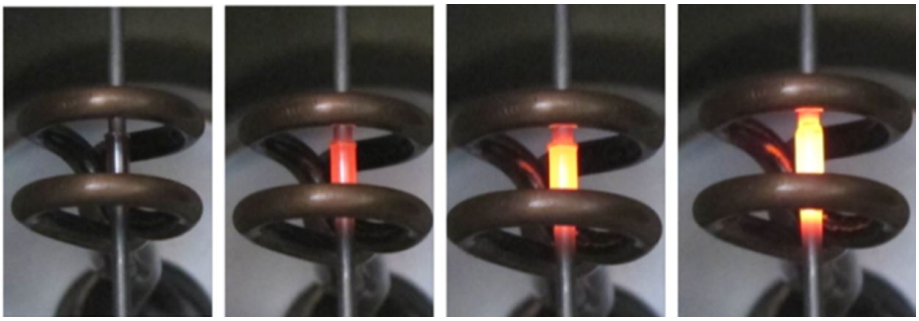

**Figure 69.** Brazing sequence: local heating of the titanium by an induction head located inside a vacuum chamber, at a temperature of 825 °C for approximately 3 minutes.

Qualification tests were performed to fine-tune the parameters and to check the quality and reliability of the braze. All test samples underwent visual inspection, leak tests, thermal shocks, metallographic inspection, tensile tests and thermal cycling. The 14 IBL staves were successfully brazed on both sides and no damage was detected on any of the modules loaded on staves. The most delicate part of the process was to design and manufacture the feedthrough and sealing parts on the vacuum brazing chamber, given such thin pipes and the high level of vacuum required to complete the junction.

## 8 Final remarks and conclusion

The construction of the IBL detector started in mid-2012 and the completed detector was installed in May 2014. Because of the demanding detector constraints, and the hostile radiation and operational environment, R&D programs relevant to the IBL started in 2008. IBL commissioning in the ATLAS cavern started in June 2014 and the IBL was fully commissioned from November 2014.

### 8.1 The IBL challenges

Key challenges of the IBL project included:



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- The R&D, industrialisation and integration of two sensor technologies (planar and 3D) on one single-stave layout, capable of surviving integrated radiation doses of up to $5 \times 10^{15}$ $n_{eq}/cm^2$, and with inactive edges of order 200 µm. The successful development of planar sensors with small inactive edges capable of reliable and efficient operation at full depletion after large radiation doses was an essential requirement for IBL operation. The new 3D sensor technology is being used for the first time in a tracking detector. The radiation tolerance of 3D sensors has been demonstrated, and their reliable and efficient operation in the IBL is a major milestone because of their reduced operating voltage (and power consumption) after high radiation doses;

- The bump-bonding of thinned FE-I4B chips to the planar and 3D sensors. This requirement was met by gluing a sapphire glass substrate to the FE-I4B wafer for all the processing steps and later detaching it using a laser de-bonding technique after the bump-bonding and before further module assembly;

- The development of the FE-I4B front-end read-out chip, the largest front-end design in radiation hard 130 nm CMOS technology for a tracker in particle physics. Its large area maximises the active area and reduces the bump-bonding cost;

- The global IBL envelope of less than 10 mm between the Pixel detector and the beam pipe was a challenge for integration, installation and the beam-pipe bake-out. As a result, innovative and custom-made mechanical supports, services and fittings were developed.

- The aggressive design minimisation of the stave material budget, and the space constraint above, required that the service bus was tightly integrated with the stave (with implications for thermal expansion mismatches that are noted below). An on-stave flex having two aluminium layers for power and four copper layers for service lines was developed;

- The development of Type 1 electrical services for the power distribution, and long (~4 m) data transmission wires, because of the tight space requirements and the hostile radiation environment. The high-density pin connectors were designed and fabricated specifically to match the limited space for integration;

- The optimisation of the thermo-mechanical interface between the module and the local stave support to guarantee the interface reliability and reproducibility, radiation hardness, and the replaceability of a module without damaging neighbouring modules, the stave itself or the service flex integrity;

- The design, development and qualification of cooling pipe connections and electrical insulation for proper grounding and shielding;

- The development of reliable $CO_2$ cooling in the detector region while satisfying the space and thermal insulation requirements. This required the R&D, design and fabrication of flexible vacuum transfer lines; these could not be transferred to industry for logistic reasons and were produced in-house;

- Extreme sealing and insulation capabilities, given the low dew-point temperature inside the detector volume, with $CO_2$ cooling close to the $CO_2$ freezing point (−55 °C);



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- Installation of the cooling plant and the long vacuum transfer line (~100 m) to the junction box and a dummy load installed close to the IBL and inside the Muon detector. Two cooling plants, each with a 3 kW maximum load, are installed and independently controlled such that they can run either in complementary operational mode, one in standby while the other is operational, or in parallel which was mainly used during the bake-out of the beam pipe.

The successful development of both the planar sensor technology and the new 3D sensor technology, capable of reliable and efficient operation in the IBL after high radiation doses, is a major milestone in the demonstration of their suitability for tracking detectors at the HL-LHC. The lower operating voltage of 3D sensors after high radiation doses is a significant potential advantage for HL-LHC operation.

During the IBL production and integration, two major issues affected the schedule. The first issue concerned the bump-bonding yield for the initial production batches. An excess of merged and open bumps (section 3.5) was identified to result from the solder flux used for bump bonding. The problem was resolved after a change of the tacking material and of the flip-chip machine. The second issue concerned wire-bond corrosion [42], which was identified on most staves mid-way during the production (section 5.4). This resulted from a combination of extreme susceptibility to corrosion and accidental exposure to humidity during the temperature cycling tests after stave loading, and all but two staves could be fully repaired. Two options were considered to protect against potential future corrosion: the potting of the bond foot or the use of spray coating such as polyurethane, but neither were possible because of the schedule. It was decided to leave the IBL detector with unprotected wire bonds and to guarantee at all stages of the integration, installation and operation phases a safe humidity level.

### 8.2 IBL in ATLAS

The commissioning of the IBL as part of the ATLAS experiment closely followed the on-surface QA procedure. Initially, the integrity of the LV sense lines for each module group was ensured. The modules were then powered with their nominal supply voltage. At each step, voltage and current readings were compared to the measurements on-surface QA. After verification of the expected DCS measurements, configuration commands were sent to the FE-I4B chips to establish communication with the modules. These powering and configuration tests were followed by digital, analog, threshold and ToT scans, and finally re-tuning of the threshold and the ToT. The RCE read-out system was used for this initial commissioning in the cavern, to ensure a consistent comparison with the on-surface QA. The results confirmed 100% damage-free transportation and installation of the IBL before the sealing of the inner detector volume at the end of July 2014.

The commissioning of the ROD/BOC read-out system started in August 2014. Nine of the 14 IBL staves were integrated in the ATLAS experiment for the collection of cosmic ray data in October 2014. Subsequently, the new beryllium beam pipe was heated to 230 °C to activate the NEG coating necessary to achieve the high vacuum levels required for LHC operation. The $CO_2$ cooling system ensured the safety of the IBL during this bake-out. From November 2014, the IBL was fully integrated as part of the ATLAS experiment.

Details of the ATLAS commissioning, data taking and performance are beyond the scope of this paper [48]. However, four detector issues related to the design and construction of the IBL are briefly noted below. None have affected the quality of data from the IBL, nor the physics performance.



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- Since the wire bonds were not encapsulated, and the IBL operates in a 2 T magnetic field, current changes during the read-out may risk damage from bond oscillations [49]. To avoid oscillation frequencies a Fixed Frequency Trigger Veto was implemented at the DAQ level in the range 3 to 40 KHz;

- As noted in sections 5.4 and 8.1, wire bond corrosion was identified on most staves during mid-production, because of accidental exposure to humidity at low temperature during temperature cycling. Because of schedule considerations, it was decided to ensure that the staves remain at low humidity. The performance of the staves has not deteriorated following this precaution;

- An increase in the current consumption of the FE-I4B chip at low total ionising dose was identified to result from N-MOS transistor leakage currents after the build-up of charge at the $SiO_2$ interface in the 130 nm CMOS process [50]. The evolution of this current was evaluated at different temperatures and annealing procedures were introduced by operating the detector at temperatures around 10 °C;

- Distortions resulted from the R-$\phi$ twisting of staves at the level of a few µm/°C, due to the mismatch of the thermal expansion coefficient between the stave and the stave flex, and the asymmetric attachment of the flex that was made necessary by mechanical constraints [51]. The impact of this is minimised by ensuring a temperature stability of less than 0.2 °C and by the development of in-run alignment correction procedures.

### 8.3 Conclusion

The fabrication and integration of the ATLAS IBL detector is described in this paper. A fully working detector with only 0.09% of dead channels was successfully installed in ATLAS in May 2014 and fully commissioned as part of the ATLAS detector in November 2014. The addition of this innermost pixel layer, very close to the interaction point and with a smaller pixel size than other Pixel layers, provides additional redundancy and significantly improves the ATLAS tracking and vertexing performance.

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