High-Speed Signal and Power Distribution of a Digital Tracking Calorimeter for Proton Computed Tomography

A thesis by

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Abstract

Radiation therapy for treating cancer generally uses photons to damage the diseased cells. However, the radiation deposited to the healthy tissue can be significantly reduced by employing protons (or other charged particles) instead. The dose planning of the charged particles is currently estimated by using a conventional photon-based Computed Tomography. Nevertheless, this method introduces errors that can be limited by implementing proton-based imaging.

The proton Computed Tomography prototype is under development by a team established at the University of Bergen. It is based on multiple layers of pixel sensors that need steady power distribution and reliable high-speed connection to the readout unit. Taking into account that the readout unit contains radiation sensitive components, it cannot be placed in close vicinity to the detector.

This thesis solves this obstacle by designing a Printed Circuit Board labeled as the Transition Card. A significant portion of the work is dedicated to developing the card to fit onto the detector frame without significantly changing the prototype's existing design. The result of this thesis is a fully functional and suitable card that needs some simple modifications. Besides that, the work estimates the power consumption and the heat dissipation of the TCs to ensure proper power distribution and cooling systems.

During this time, several suggestions were issued on how to ease the installation and testing methods. The work includes a proposal on the safety and the control system that will monitor and control the power and the temperature of the detector.

Every suggested change and decision taken along the development is well documented. Besides, this work contributed to gain a clearer picture of the different detector elements. This is relevant for troubleshooting and further development of the pCT prototype.

Acknowledgments

First and foremost, I would like to thank my supervisor, Professor Kjetil Ullaland, who gave me highly appreciated guidance not only in academic life but also in professional and personal. A big thanks to my co-supervisor, Associate Professor Johan Alme, who taught me a great deal about radiation effects in electronics. I will always be thankful to Ola Slettevoll Grøttvik for seeing the potential in me and not running away whenever I started the conversation with "Ehm, I have a question".

The rather broad scope of this work involved to collaborate with different working groups within the pCT Bergen team, which was intimidating at times but simultaneously enlightening. For that, I want to thank Professor Dieter Röhrich and the pCT team, especially Shruti, Viljar, Jarle, and Ihor. I wish to express my gratitude to Ton van den Brink for his quick response and valuable advice, no matter what day of the week. I appreciate every tip and trick offered by our engineers, Shiming Yang, and Bilal Hasan Qureshi.

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I would also like to thank my fellow students but Alf Kristoffer Herland, in particular. You have been a good friend these past five years, and I will be forever grateful for that.

Finally, I thank my parents and family, who have patiently supported me on this long journey. I hope you know that my success is the reflection of your hard work as well. I would like to thank Daniel for accompanying me on this journey and showing me that everything is possible, particularly when you own a 3D printer.

Contents

Acronyms

ALICE A Large Ion Collider Experiment.
ALPIDE ALICE Pixel Detector.

BOM Bill of Materials.

CentOS Community Enterprise Operating System.
CERN European Organization for Nuclear Research.
CMOS Complementary Metal Oxide Semiconductor.
CT Computed Tomography.

DAQ Data Acquisition.
DCH Direct Connect System.
DTC Digital Tracking Calorimeter.
DTU Data Transmission Unit.
DUT Device Under Test.

EMI Electromagnetic Interference.
ESD Electrostatic Discharge.

FF FireFly.
FPC Flexible Printed Circuit.
FPGA Field Programmable Gate Array.

GPIB General Purpose Interface Bus.
GUI Graphical User Interface.

I2C Inter-Integrated Circuit.
IC Integrated Circuit.
IDC Insulation-Displacement Connector.
IPC Institute of Printed Circuit.
ITS Inner Tracking System.

LET Linear Energy Transfer.
LVDS Low-Voltage Differential Signaling.

MAC Media Access Control.
MAPS Monolithic Active Pixel Sensor.
MLVDS Multipoint Low-Voltage Differential Signaling.
MPSoC Multiprocessor System on a Chip.

PCB Printed Circuit Board.
pCT proton Computed Tomography.
PCU Power Control Unit.
PHY Physical Layer.
PLA Polylactic Acid.
PLL Phase Locked Loop.
PRBS Pseudorandom Binary Sequence.
pRU pCT Readout Unit.
PSU Power Supply Unit.
PTB Production Test Box.

RCBO Residual-Current Circuit Breaker with Overcurrent Protection.
RCU2 Readout Control Unit Version 2.
RS-232 Recommended Standard 232, serial communication transmission of data.
RTD Resistance Temperature Detector.

SOBP Spread-Out Bragg Peak.
SPI Serial Peripheral Interface.
SRAM Static Random Access Memory.

TC Transition Card.
TID Total Ionizing Dose.

UDP User Datagram Protocol.
UiB University of Bergen.
UPS Uninterruptible Power Supply.
USB Universal Serial Bus.

VISA Virtual Instrument Software Architecture.

ZIF Zero Insertion Force.

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CHAPTER 1

Introduction

1.1 Background and Motivation

Cancer is amongst the top causes of death. There are several cancer treatments, such as surgery, chemotherapy, radiation therapy, and immunotherapy. In radiation therapy, high doses of radiation are used to damage the diseased cells. Photon beams are commonly applied during cancer treatment. This method, however, introduces doses of radiation to the healthy tissue as well. Beams with charged particles, on the other hand, reduce this problem significantly. Even though this technique has been used in radiation treatments since the 1950s, its popularity has started to grow only in the last two decades [1]. There exist about 40 photon therapy clinics in Norway but no particle therapy centers [2]. In 2017 the government decided to change that and build two particle clinics in Oslo and Bergen, specifically proton clinics.

Every radiation treatment requires a scan of the cancer-affected part of the body before the actual procedure. In proton therapy nowadays, this is generally completed by a conventional Computed Tomography (CT) machine that uses low-dose X-rays for imaging. The data collected from the imaging are further used to estimate the desired dose of protons. Nevertheless, this method brings up uncertainties, which can be reduced by utilizing CT imaging with the same type of charged particles i.e., protons. For this reason, a team based at the UiB is currently developing a prototype of a proton Computed Tomography (pCT) machine.

1.2 About this Thesis

The pCT prototype requires a complex system of electronics. The front-end electronics consist of multiple layers of pixel sensors developed by CERN that detect

the incoming particles. These chips need stable power distribution and high-speed interface with the readout system. This system contains components that are sensitive to radiation. The chips are bonded to a flexible cable whose length can't exceed a certain limit to preserve good signal quality. For these reasons, an intermediate element is needed.

There are nine chips bonded to the flexible cable. This arrangement is referred to as a 9-chip string. One sensor layer is built out of twelve such strings covering an area of 27×15 cm. These strings are further mounted on aluminium plates that also serve as an absorbing medium to slow down the particles. All layers are fixed onto a frame that holds the cooling system for the chips as well. Therefore, one of the requirements for this intermediate element is to fit onto the frame so that no additional structure will be necessary. It is desirable that the solution is easy to assemble and reliable to use in the high radiation zone. This thesis analyzes the possible options to solve this problem.

This solution is built on the fact that the flexible cable is very fragile, and no other components can be mounted directly onto it. This is why a PCB called Transition Card (TC) is developed to make this conversion possible. A significant portion of the work was dedicated to transfer the TC design into a 3D model and match it with the available 3D model of the detector. In this way, it was verified that no spatial restrictions were violated.

When designing the TC, particular layout rules were followed to preserve good quality signal. This is documented in detail to make the troubleshooting easier if an issue occurs. The radiation tolerance of the chosen components is documented as well.

A significant effort was made to explain the different elements and the design decisions of the power distribution. This thesis is not only expected to define a stable power supply system but also evaluate how much power the detector consumes. This is essential for further development of the facility where the prototype will be tested. It is also emphasized that the length of the power cables contributes to the stable power distribution and power consumption and must always be reevaluated when changed.

Due to the delicate electronics i.e., the strings, solutions on the most secure handling when connecting them to the TC are examined. Consequently, various tools were created for this purpose.

Given that the TC will be used by different people with different backgrounds, a manual was written to provide a simple guide on how to use the card (available in Appendix D).

Finally, Chapter 7 presents a proposal on the safety and the power control system. It is intended that these systems will monitor and control the power and the temperature of the detector to protect it in case of an emergency. Besides, the Power

Control Unit (PCU) will give the functionality to control the power for each string.

1.3 Chapter Overview

Chapter 2 – Radiation Therapy and Computed Tomography This chapter describes the different interactions of photons and protons with the matter, and how this is implemented in radiation therapy. It further explains why the conventional and the proton CT is employed along with the cancer treatment.

Chapter 3 – Proton Computed Tomography at University of Bergen This chapter presents the current design and the workings of the pCT prototype being developed by the Bergen pCT team. It gives a brief section on the radiation effects on semiconductor devices.

Chapter 4 – Transition Card This chapter starts with the requirements and restrictions of the TC. The chapter further continues to justify the choice of components and the design. There is also a section on how much radiation the card will receive and tolerate. A brief section in this chapter provides the theory on transmission lines, differential signaling, and the adequate layout. This chapter also offers the estimated power consumption of the detector, as well as how much heat will be dissipated. The chapter ends with recommendations for changes in the next TC version.

Chapter 5 – Testing and Verification of Transition Card This chapter outlines the different tests applied to confirm the functionality of the TC. It also provides several suggestions on how to make the process of testing and assembly easier.

Chapter 6 – Remote Control of Power Supply Unit This chapter begins by explaining the need for controlling a power supply unit remotely. It then presents a Python code based on the power supply unit available in the laboratory.

Chapter 7 – Power Control Unit This chapter presents the requirements and the proposal of a control unit that would monitor the power consumption and the temperature of the detector.

Chapter 8 – Safety System This chapter explains what safety measures must be taken to protect the equipment when failures in different stages of the circuitry occur.

Chapter 9 – Conclusion and Future Work This chapter evaluates the work done in the period of this thesis. It also gives a discussion on the future work needed.

Appendices The two first appendices contain the schematics and the layout of the TC V1.0. All technical drawings of the 3D printed tools and additional figures of the detector are presented in the following appendix. There is also an appendix that serves as a manual to the TC. It explains the features of the card and how to connect it. It also gives a list of available test points as well as a list of possible issues and how to fix them. The last appendix contains the Python code discussed in Chapter 6.

CHAPTER 2

Radiation Therapy and Computed Tomography

This chapter is an introduction to ionizing radiation, radiation therapy, and medical imaging. The following sections explain how photons and protons interact with a matter to understand the advantages and disadvantages of either photon or proton therapy. The next section shows various imaging techniques used along with radiation therapy used to locate the tumor and calculate the dose required in the treatment, so-called dose planning. The last section briefly explains the various effects of radiation on semiconductor devices.

2.1 Radiation

Radiation is an energy that is traveling through space and material in the form of waves or particles. We distinguish between ionizing and non-ionizing radiation. Ionization occurs when the energy emitted by atoms as electromagnetic waves (gamma or X-rays) or particles (alpha, beta, protons, or neutrons) removes electrons from the atom. This is harmful in high doses or long-term exposure. Ionizing radiation is further categorized into direct and indirect radiation. For direct ionization, charged particles such as protons, alpha, beta, or heavy ions (e.g., carbon ions) interact multiple times straight with the atoms. Indirect ionization happens when non-charged particles such as neutrons or photons (from gamma and X-rays) set free a single electron, thus creating by-products, which can cause the secondary ionization. On the other hand, non-ionizing radiation like radio waves, microwaves or ultraviolet rays has insufficient energy to ionize atoms. However, they can damage the molecular level when tissue is overexposed to these types of radiations, e.g., a sunburn from UV radiation caused by the Sun.

2.1.1 Interaction of Photons with Matter

Photons don't have an electric charge, but they carry momentum and a certain amount of energy. When a photon interacts with a material, three primary mechanisms occur. The photon can be scattered in the medium (Compton scattering), absorbed by the medium (photoelectric absorption), undergo a conversion with the medium (pair production), or it can simply penetrate the medium without interaction.

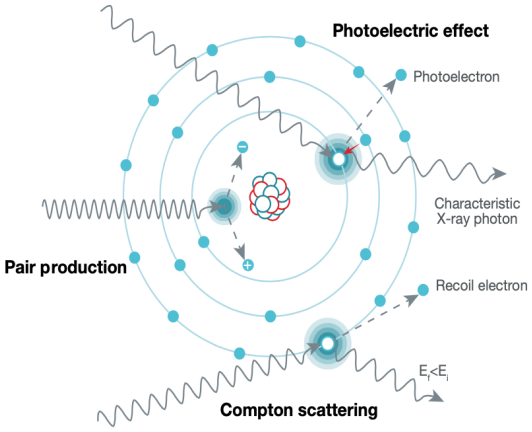


Figure 2.1: Three main photon interactions with matter: Photoelectric effect, Compton scattering and pair production [3, Figure 2-7].

The photoelectric effect occurs when a photon transfers its energy to an electron in one of the atomic shells. This is only possible when the photon energy is slightly higher than the electron's binding energy. When this is the case, the photon is absorbed in the interaction, and the electron is removed from the atom creating an excited photoelectron. This leaves a positively charged vacancy, which is filled by another outer-shell electron. The difference in energy between the removed electron and the substituting electron produces a characteristic X-ray photon.

Compton scattering is an interaction where a photon with significantly higher energy than the binding energy of the atomic electron collides with the electron. The photon transfers some of its energy, which results in freeing the electron. This recoil electron can cause further interactions with other electrons and nuclei. In this process, the photon loses some of its energy, and its trajectory is shifted. This shift in direction is called scattering.

Interactions of photons with energy higher than 1.02 MeV may lead to pair production. The outcome of the collision between a high-energy photon and an electron or a nucleus is the production of an electron and a positively charged positron, each with the energy of 511 keV.

Attenuation of the Photon Beam Intensity

These interactions reduce the number of photons as a beam of photons traverses the medium. Thus, we look at the intensity of the photon beam (the number of photons traversing an area per second) rather than at the energy of the photons. This attenuation of the beam intensity is defined as:

$$I(x) = I_0 \times e^{-\mu x} \tag{2.1}$$

where I_0 is the intensity of the incident beam, μ is the linear attenuation coefficient, and x is the traveled distance in the medium. Equation 2.1 represents that as the medium gets thicker, the intensity of the beam decreases exponentially.

The linear attenuation coefficient is given by the cumulative cross-section of the different photon interactions (σ_{tot}) and the number of atoms per unit of mass:

$$\mu = \sigma_{tot} \times \eta_A \tag{2.2}$$

where σ_{tot} is the sum of cross-sections of the different photon interactions, and each σ presents the probability of a interaction to happen:

$$\sigma_{tot} = \sigma_{Photoelectric\ effect} + \sigma_{Compton\ scattering} + \sigma_{Pair\ production} \tag{2.3}$$

The linear attenuation coefficient, μ, is often converted into the mass attenuation coefficient, μ_m (cm^2/g), which is a ratio of the linear attenuation and the density of the medium (μ/ρ). The total mass attenuation presents how much the medium attenuates the penetrating photon beam. This is essential when estimating what material should be used for shielding in the radiation environment. Figure 2.2 shows the total mass attenuation coefficient in iron as the function of photon energy. The probability of penetration plateaus as the photon reaches incoming energy of more than 10 MeV. In this higher photon energy region, the pair production is the most dominant interaction. At the lower energies, the photoelectric effect will dominate, and to some extent Compton scattering as well.

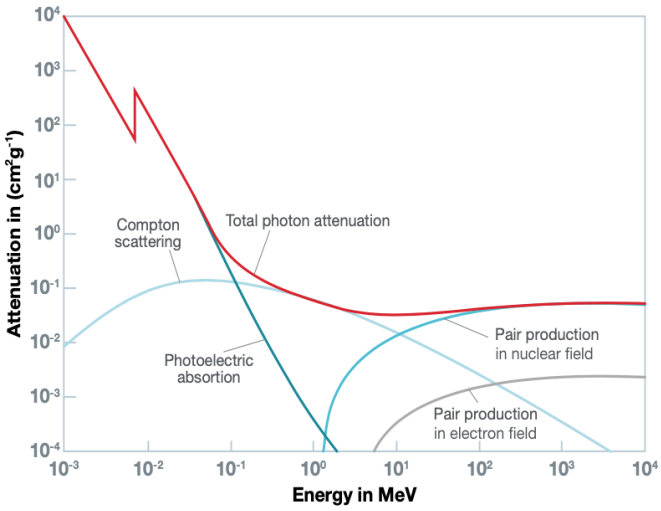


Figure 2.2: The mass attenuation coefficient of Fe as a function of photon energy [3, Figure 2-8].

2.1.2 Interaction of Protons with Matter

Protons and other charged particles are surrounded by the Coulomb field, and they thereby interact with either electrons or the nuclei of an atom. These interactions can be elastic or inelastic collisions. There are three main ways protons can interact with matter:

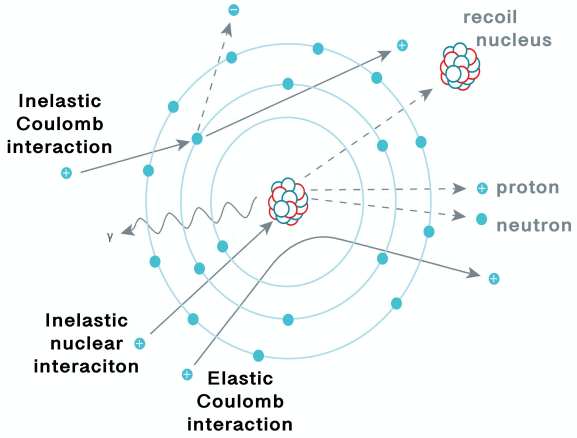


Figure 2.3: Three main proton interactions with matter: inelastic nuclear interaction, inelastic and elastic Coulomb interaction.

Elastic Coulomb interactions (also called Multiple Coulomb scattering) occur between the proton and the atomic nuclei, where the nuclei only divert the proton.

In inelastic Coulomb interactions (also called stopping interactions), the proton collides with the atomic electrons. Since the proton's mass is bigger than the mass of the electron, it takes several collisions before the proton stops.

Inelastic nuclear interactions (also called hard scatters) are single collisions of a proton and a whole nucleus. The proton is absorbed, and secondary particles (e.g., protons, alphas, neutrons, and others) are created in the process. This interaction happens rarely.

Energy Loss in Proton Interactions

As the protons traverse a medium, they lose energy because they interact with matter. The Linear Energy Transfer (LET) estimates the average energy transferred to the medium per unit length. The Bethe-Bloch formula calculates the energy loss (also known as stopping power) as well, but it includes all energy-loss mechanisms, and because of that, it is more accurate. Both methods depend strongly on the material and type of particles, and both state that as the velocity of proton decreases, the energy loss increases. In other terms, when the proton starts to slow down in the medium, it deposits more energy because it has more time to interact with the medium. Figure 2.4 demonstrates this mechanism of protons in water. As the stopping power increases and the energy of protons decreases, it creates a peak where all remaining energy is deposited. This peak is known as the Bragg peak.

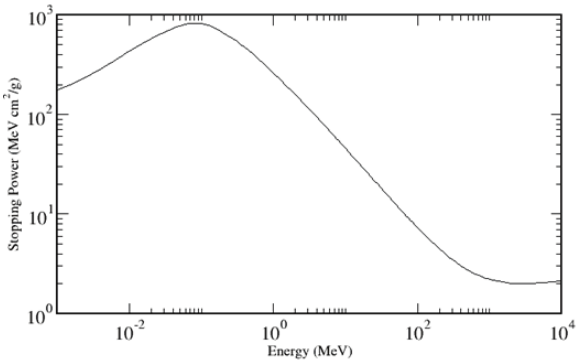


Figure 2.4: Stopping power of protons in water [4].

2.1.3 Radiation Therapy

Radiation therapy makes use of the ionizing radiation to damage a malignant tumor. A beam of either photons or heavier particles (mainly protons or carbon ions) targets the affected area and damages the DNA, so that it is unable to replicate later. Traditionally, photon radiation treatment has been the main type of radiation therapy, but only a small number of proton treatment centers operate nowadays (around 90 proton therapy facilities in clinical operation worldwide as of 2020 [5]).

These two methods primarily differ in how the energy is deposited in the tissue. Figure 2.5 portrays this process. The photon beam (in blue) delivers most of its energy straight after it penetrates the body. Thus, the tumor is radiated from various angles to achieve the accumulative dose affecting the target area. However, the ionizing radiation impacts the adjacent healthy tissue as well, which can later lead to secondary cancer. The proton beam (in yellow) deposits a major part of its energy (the Bragg peak) directly to the tumor, reducing secondary cancer's probability. The Bragg peak is, however, too narrow to cover the range of a tumor. A modified beam is created for clinical applications when a broader range is needed by using different thicknesses of absorbers or altering the beam's energy [6]. This adjusted beam is referred to as Spread-Out Bragg Peak (SOBP).

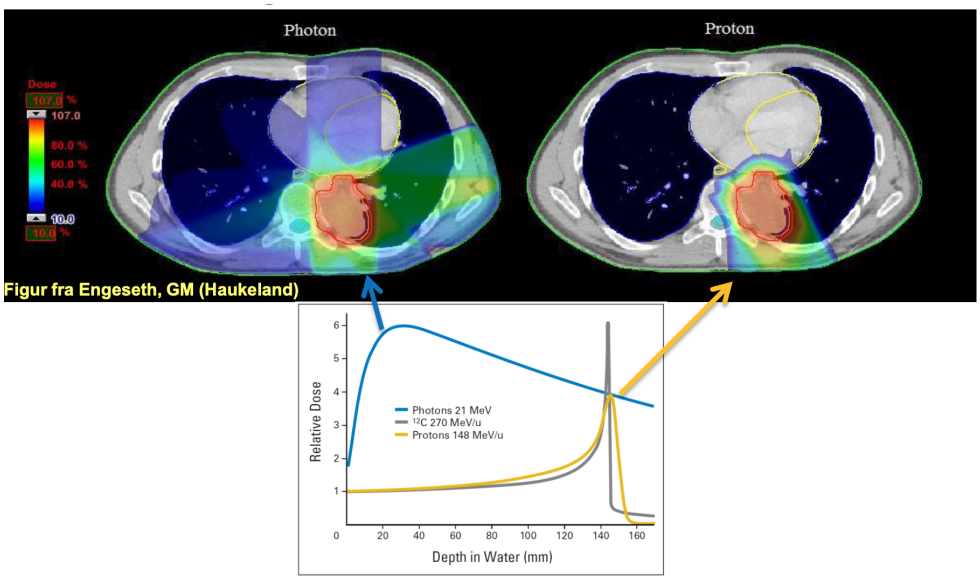


Figure 2.5: Graphical illustration of how the dose is delivered to the tissue (source: top figure from G. M. Engeseth ved Haukeland Universitetssykehus, bottom figure [7]).

2.2 Computed Tomography (CT)

Medical imaging is the method of creating a scan of a section in the human body. Techniques as X-ray radiography, magnetic resonance imaging, ultrasound, computed tomography, and others are used to achieve this. Medical imaging is associated with radiation therapy because the patient is scanned before every treatment to establish the position and contour of the tumor as well as to estimate the beam energy used during the treatment. Figure 2.6 presents one of the general configurations where a beam is projected toward a target and afterward measured by the detector.

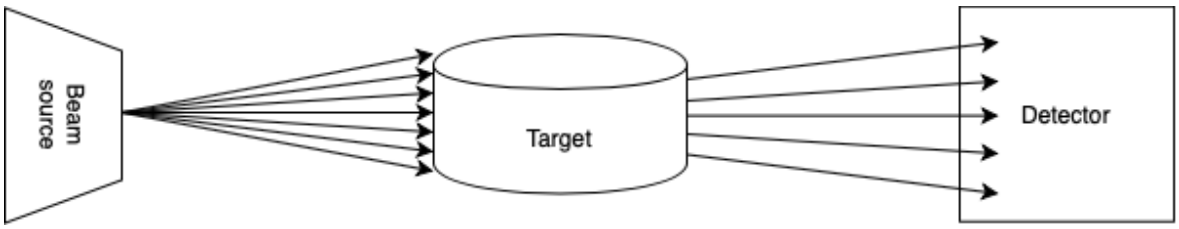


Figure 2.6: General configuration of scan imaging.

The standard CT machine employs an X-ray (photon) beam, which is quickly rotated around the target creating cross-sectional images. The target is also moved in a horizontal direction to acquire a three-dimensional image. The attenuation of the beam is proportional to the tissue density, and thus the attenuation is measured to reconstruct the image qualitatively. The X-ray attenuation is expressed in Hounsfield units, which converts the image into a gray scale, i.e., black and white image. The denser structures in the body (e.g., bones) have very high attenuation, and this high reduction in beam intensity will be detected and reconstructed in white color. In contrast, air only attenuates the beam intensity slightly, so it is displayed as black.

2.2.1 Proton Computed Tomography (pCT)

As the name indicates, the pCT uses protons instead of photons. The setup corresponds to the one shown in Figure 2.6 with the modification that there are generally tracking planes before and after the target. In the pCT, the proton beam is modified to reach the Bragg peak in the detector rather than in the target. The protons must have enough energy to penetrate the target, but the interaction with the target will cause them to scatter (inelastic and elastic Coulomb interactions) and to escape the target at different angle than the incident angle. The most-likely-path of the protons is then reconstructed from the tracking layer data [8] and the remaining energy is measured by the detector.

The pCT has two major advantages. The first advantage is that the patient obtains lower amount of ionizing dose than in the CT imaging. The second advantage concerns the accuracy of the measurement of the stopping power of the target. Currently, the stopping power is estimated by the Houndsfield units data from traditional CT imaging. However, the relationship between Houndsfield units and stopping power is not linear. Thus, the estimation causes an error of 2-3 % [9]. By measuring the stopping power directly, i.e. by using protons for imaging, this error might be significantly reduced.

2.3 Radiation Effects in Electronics

This section presents briefly the different effects of radiation on semiconductor devices. It is important to address these since the radiation present during radiation therapy and imaging can seriously degrade or even damage semiconductor components. After sufficient radiation exposure the insulating and conductive materials lose their characteristics and start to be uncontrollable. Similarly, a particle with high enough energy can initiate various errors both in analog and digital ICs [10].

The radiation effects are categorized into two main groups: Single-Event Effects and Cumulative Effects.

2.3.1 Cumulative Effects

These effects are caused by the accumulation of the deposited energy from incoming particles. Each device has its threshold of how much dose it can receive before it starts to malfunction. There are two major dose-effects [11]:

Total Ionizing Dose

The ionizing radiation creates excess charge in the insulating layers which, when accumulated, leads to leakage current and degrades the device. The primary source of TID are electrons and protons. The dose is often expressed in rad.

Displacement Damage Dose

The displaced atoms in the crystal lattice by non-ionizing radiation create permanent damage in the device. The accumulation of these microscopic defects lead to decrease of the electrical properties of a device. It is common to express the dose in relation to particle fluence (particles/cm^2).

2.3.2 Single-Event Effects

As the name suggests, these effects are result of a single particle interacting with the device. The particle can cause many different effects, such as [3]:

Single-Event Upset

The particle changes the data state of a memory cell, register, latch, or flip-flop. The device itself is not permanently damaged.

Single-Event Functional Interrupt

The particle flips the bit of a memory in a critical control system of the device. This error causes the device to fail.

Single-Event Transient

The particle creates an instantaneous current spike in combinational circuits. If this error propagates through the circuit, a wrong value can be latched or stored causing single-event upset.

Single-Event Latchup

The particle forms a low resistance path between power and ground. If the current flowing through this region is high enough, it can produce permanent damage to the device.

Single-Event Burnout and Single-Event Gate Rapture

The particle deposits high enough energy creating high current that is further amplified by the device. This failure causes irreversible damage by melting the device.

CHAPTER 3

Proton Computed Tomography at University of Bergen

This chapter gives an overview of the proton Computed Tomography (pCT) prototype being developed at University of Bergen (UiB) by the Bergen pCT collaboration. It gives a detailed summary of the current detector design. It also provides a brief outline of the electronics system and the readout system.

3.1 Digital Tracking Calorimeter Prototype

The pCT prototype follows the principle build-up as shown in Figure 3.1. In nuclear and particle physics, a calorimeter refers to an apparatus which detects particles and measures their energy. In our case, the protons are detected by several layers of ALPIDE sensors (ALICE Pixel Detector). The two first layers are used for tracking and the rest for measuring the protons' energy and range. The data acquired by the detector are then reconstructed into an image. This multilayer structure is referred to as Digital Tracking Calorimeter (DTC).

The ALPIDE chip is a CMOS (Complementary Metal Oxide Semiconductor) MAPS (Monolithic Active Pixel Sensor) composed of 512×1024 pixels that can detect particles that deposit energy over a specific threshold. It was originally developed for the Inner Tracking System (ITS) in the ALICE experiment at CERN [12]. The relatively high granularity of the ALPIDE gives a high spatial resolution, thereby making it possible to distinguish individual particles. This, in turn, allows for increasing the particle rate, reducing the time needed for a single 2D projection. The chips can also process data at the required readout speed, and are therefore a good option for the pCT prototype. This is important for the fast reconstruction of the image.

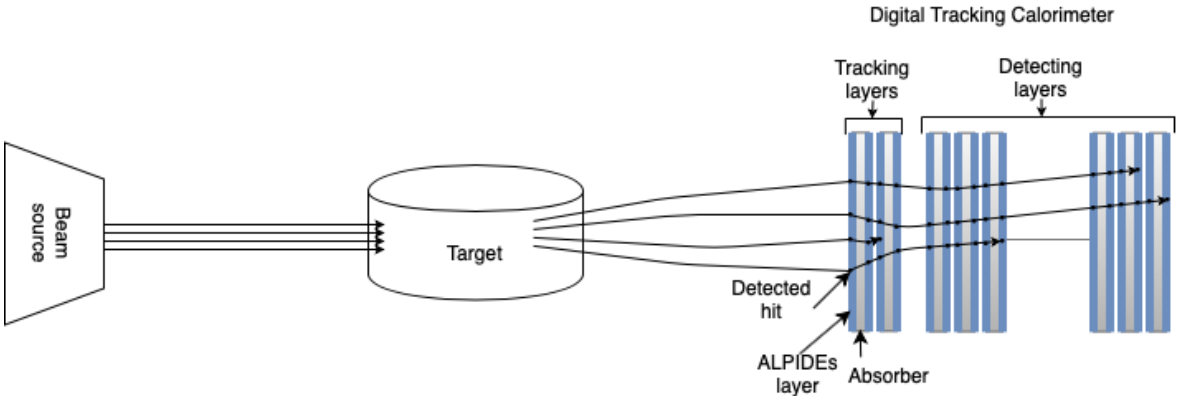


Figure 3.1: The principle build-up of the pCT system with two tracking layers.

Each ALPIDE is bonded to an aluminium-polyimide Flexible Printed Circuit (FPC), from here on called a chip cable, using Tape-Automated Bonding [13]. The chip cables are further connected by the same bonding method to a longer FPC, simply named as a string flex. In the pCT system, nine ALPIDE chips are mounted on one flex. This configuration is defined as a 9-chip string. Three strings are further glued next to each other into a slab on a 1 mm thick aluminium plate (carrier for the slab). The plate is part of the absorber layers between each layer.

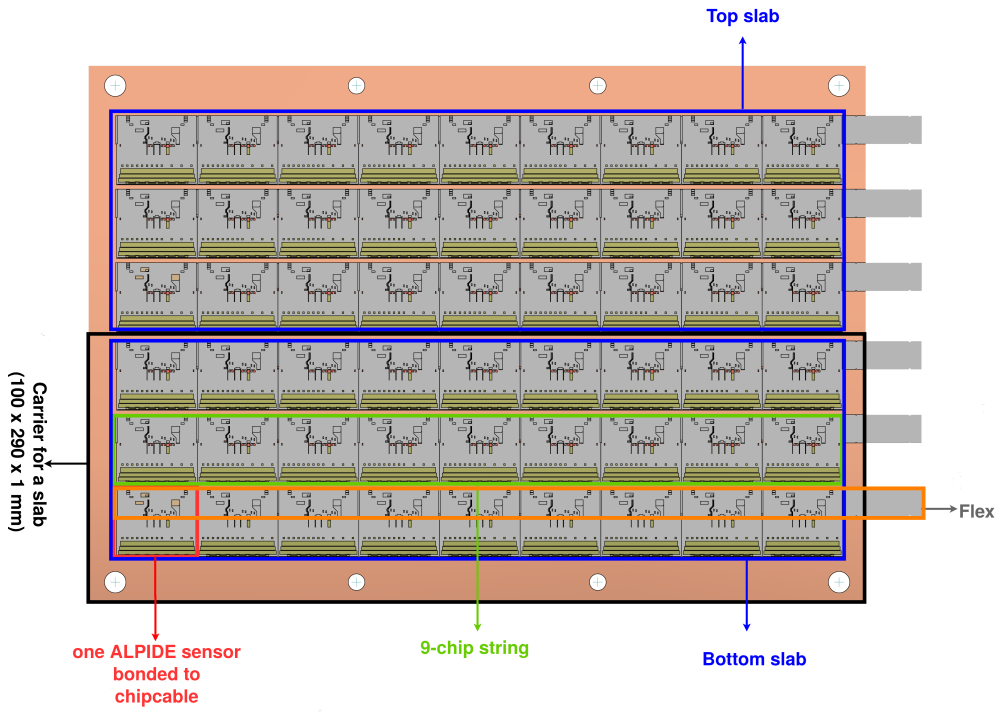


Figure 3.2: Half sensor layer and the related glossary.

Figure 3.2 shows one half sensor layer consisting of two carriers for the top and bottom slabs, and the terms that describe the different components of the half layer. In addition to the 1 mm aluminium carrier, there is a 1.5 mm thick aluminium plate between each half sensor layer [14]. These aluminium layers absorb proton energy and, hence, reduce the protons' velocity as they traverse trough the DTC. The part of the flex cable that sticks out of the carriers is called flex end or flex tail.

The other half sensor layer is flipped horizontally (180 degrees) to face the first half. This arrangement secures that the ALPIDE chips cover the whole area of one sensor layer. Figure 3.3 shows this overlap on the four bottom strings where the green strings are part of one half layer, and the blue strings are part of the other half layer. However, there is a gap between the slabs that must be taken into account during image reconstruction.

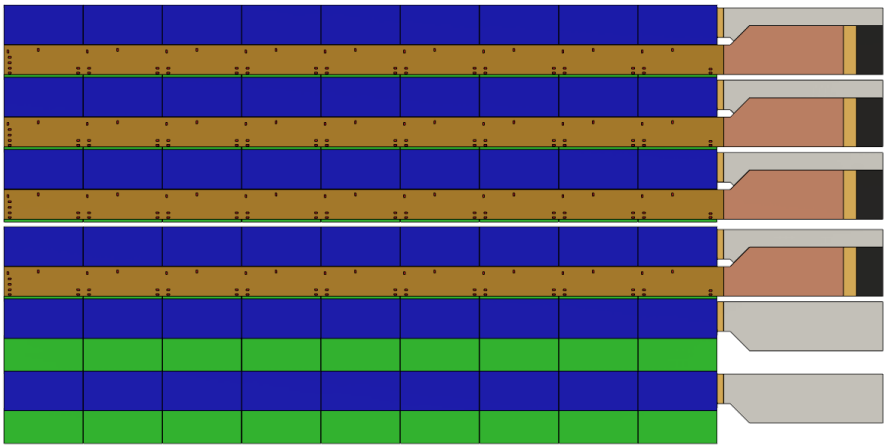


Figure 3.3: One sensor layer without aluminium carriers.

A PCB is developed to make the transition between the flex cables and the pRU, titled as the Transition Card (TC). This card serves two purposes; the first is to connect the high-speed ALPIDE communication links with the pRU, and the second is to provide stable power for the ALPIDE chips (see Chapter 4).

Figure 3.4 shows the 41 layers and two tracking layers in the front. The carriers in the tracking layers are made of thinner carbon-Epoxy sheets due to the low thermal conductivity of carbon [14]. Each of these layers is connected to the Transition Card that is mounted to the main frame. The dimensions of the detector as shown in the Figure 3.4 are approximately $28 \times 60 \times 24$ cm (depth x length x height) and $39 \times 60 \times 24$ cm with two front tracking layers. However, it is expected that the new iteration of the Transition Card will be longer by 2.5 cm, which will make the detector longer by 5 cm.

The DTC has three different types of cooling systems: closed-loop liquid-cooling for ALPIDEs in the calorimeter, a combination of air- and liquid-cooling in the tracking layers and forced air cooling for the Transition Cards. Two aluminium plates on the top and the bottom of the calorimeter are part of the closed-loop liquid-cooling system. The air ducts that are wrapped around the whole detector maintain the flow of forced air. On each side of the DTC is a framework that supports the power cables and the data cables. This relieves the tension on all connectors on the TC, and it helps to keep the cables organized. More figures in Appendix C.

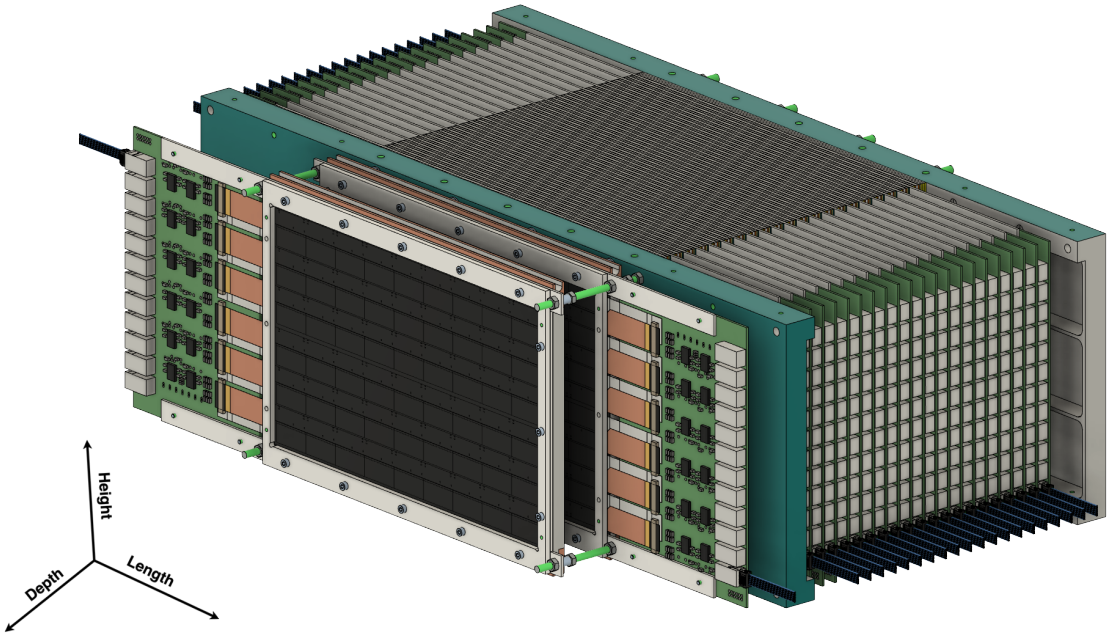


Figure 3.4: 3D design of the Digital Tracking Calorimeter including TC V1.0 (3D design of the detector provided by Anthony van den Brink (a.vandenbrink@uu.nl))

3.2 pCT Electronics System Overview

The data acquisition (DAQ) system is composed of the front-end electronics (ALPIDEs), the Transition Card (TC) and the pCT Readout Unit (pRU). The temperature and power consumption will be monitored by the Power Control Unit (PCU), which is defined in Chapter 7. The whole system will be powered by several Power Supply Units (PSU), and protected by overcurrent safety circuits (fuse boxes, more about safety in Chapter 7.2). Figure 3.5 suggests how the electronics system of the pCT prototype could look like in the final version, and how the separate elements are interconnected with each other.

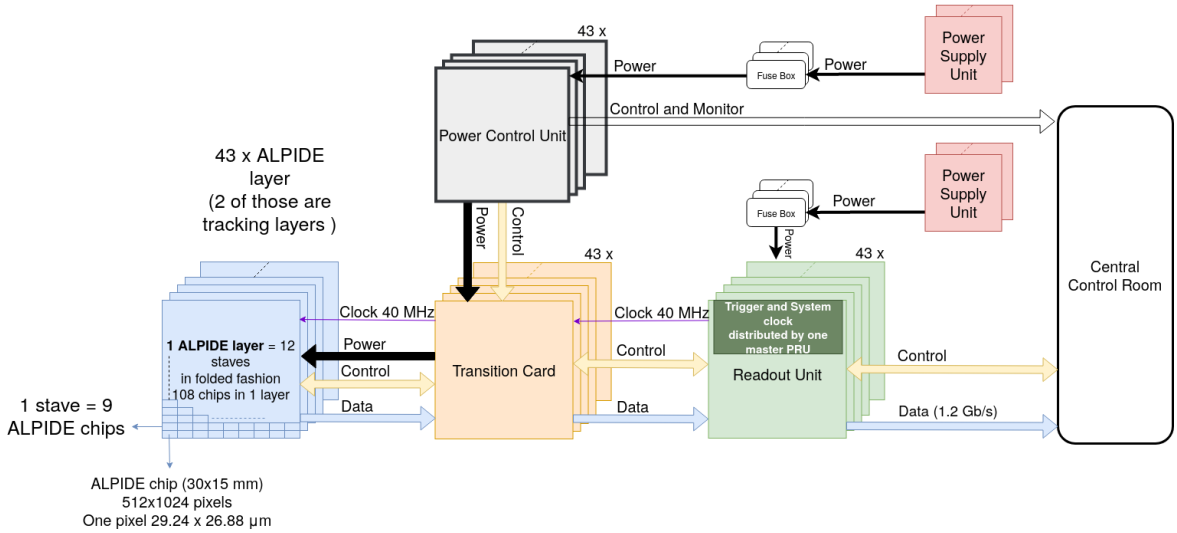


Figure 3.5: Current diagram of the pCT system.

3.3 pCT Readout System

The main component of the pRU is a Field Programmable Gate Array (FPGA) that takes care of the data processing and various control and monitoring tasks. One pCT Readout Unit (pRU) processes one detector layer with 108× high-speed data links, 12× 40 MHz clock link and 12× control link shared between ALPIDEs on each string.

The pRU employs a Xilinx Kintex Ultrascale FPGA (XCKU085-FLVA1517) that can handle the accumulated data rate of a single detector layer [13]. The data is packed in a special data format containing both spatial hit information and the timing information before it is multiplexed and transmitted with a custom UDP-protocol over a copper network layer. The pRU design was first introduced in 2017 by Ola Slettevoll Grøttvik (former M.Sc. student and later Ph.D. candidate at UiB). Most of the tests and the development of the readout electronics have been performed on the VCU118 evaluation board from Xilinx utilizing a Virtex UltraScale+ FPGA.

An SRAM-based FPGA is sensitive to ionizing radiation, especially single-event effects (see Section 2.3), and it must be situated at minimal 2 m distance from the center of the DTC to avoid the high radiation zone [15]. On the other hand, it is not desirable that the thin flex end is more than 50 cm long. High-speed signal simulations showed that the string flex significantly attenuates the signal, thus complicates the data recovery and increases errors.

These constraints are the main requirements for an additional board between the front-end electronics and the pRU that can securely carry the data from the DTC to the pRU, and that will fit into the main frame.

CHAPTER 4

Transition Card

This chapter describes the approach to solve the connection between the chips and the readout unit. The Transition Card is designed just for this purpose. This chapter starts with gathering the functional and spatial requirements, then the design process. The chapter contains also estimates on power consumption, heat dissipation, and radiation tolerance regarding the TC. The last section outlines the necessary changes for the next iteration of the card.

4.1 Method

There is a need for reliable conversion from the flex cable to another type of cable with low attenuation. The FireFly cable assembly from Samtec has been previously tested and verified as an acceptable option. However, it is not possible to make this transition directly, i.e., to mount the FireFly connector on the flex cable, since the flex cable is very delicate.

This is why the TC is considered to have the appropriate connectors to make the transition and a set of voltage regulators to provide stable power. It is also connected to Power Control Unit (PCU), which will control and monitor the power and temperature of the TC.

Even though, a similar board was previously developed for the 9-chip string with different layout (by Ing. Jody A. Wisman from Utrecht University), this work looks closely into the design and other possible solutions.

4.2 Requirements

The initial requirements for the TC are listed below:

1. TC must handle 12× 9-chip strings (108 ALPIDE chips per TC).
2. TC must provide 1.9 V and 1.1 A (0.2 A for AVDD, 0.9 A for DVDD [1]) to each 9-chip string. The required voltage can change; thus it must be an option to alter it.
3. TC must provide a connector for the flex cable. There are 36 contacts on the flex end with a 0.5 mm pitch. The flex has Nickel-Tin-Bismuth plating. The connector must have 0.5 A rated current.
4. TC must have proper layout design for 11 differential links per string (132 links per TC). The differential impedance of these links must be in the range of 100 $\Omega \pm 10\%$.
5. TC must only contain radiation tolerant components.
6. TC is considered to have testing points for easier troubleshooting.
7. TC considered to have universal design i.e., only one version of the TC (no left and right configuration).
8. TC considered to fit onto the main frame of the DTC.

4.3 Spatial Restrictions

The design of the DTC has evolved throughout this thesis work. The mechanical team and the microelectronics team have been working consistently together. No significant change could be done on the TC before discussing it with the mechanical team and vice versa.

The primary focus when designing the TC has been on the signal integrity to minimize the attenuation and mismatch of the transmission lines. It is also desirable that the TC is as close as possible to the ALPIDE chips. However, the main frame of the detector has its space limitations, which pose a challenge to find connectors of smaller proportions to fit into the design since these components are, in general, the largest on a PCB.

[1] Current consumption has been measured by ALICE ITS team at CERN. However, the report is still in progress and hence confidential. It is measured that an ALPIDE chip with GOLD classification will draw a maximum of 16 mA for analog part and maximum of 50 mA for digital during the simple powering test (only the clock is on, no data transfer), so around 150 mA and 650 mA respectively for a 9-chip string. When chips were tested with high-speed data transfer at UiB, higher digital current consumption was experienced (880 mA, never over 900 mA).

Figure 4.1 displays the restrictions between four sensor layers. It is important to notice that the TC is mounted on every other layer on each side of the detector to gain more space. In this way, half of the cards will be on the right side of the detector and the other half on the left side. That is why one of the requirements is to keep the full sensor layer together with the TC universal, meaning that there won't be any special right or left arrangement to keep track of. This would otherwise introduce complexity to the entire design.

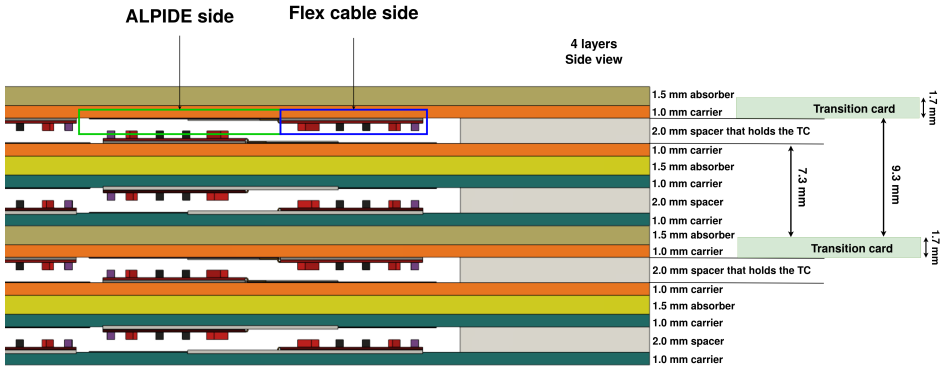


Figure 4.1: Spatial restrictions shown on 4 layers from the side view.

The TC can't exceed the height of 198 mm to keep it in the same height as the detector. The flex is mounted on a fixed position on the carrier, and connectors must align with the flex in order not to bend and not to damage the traces. The TC is attached by screws to aluminium spacers, and therefore, no components are allowed in this area.

4.4 Power, Ground and Bias Nets

This section describes the different nets that power both ALPIDE chips and the Transition Card. Table 4.1 gives a short overview of these nets. These net names are being used throughout the whole thesis.

The front-end electronics does not only contain a matrix of pixel sensors. It is a complex, mixed-signal system that includes memory blocks, registers, analog-to-digital, and digital-to-analog converters and other electronics [16]. A mixed-signal system is an Integrated Circuit (IC) that has two domains: digital and analog. The digital circuitry is, in general, very noisy with fast-switching signals that can interfere with the quiet analog circuitry. Therefore are these environments kept separated. Also, the digital circuitry supply is kept separate from the PLL supply as well, which requires a very stable voltage to behave optimally.

Table 4.1: Power, ground, and bias nets definitions.

	Net names	Type	Comment
ALPIDE	AVDD	SUPPLY	Analog domain supply; currently set to 1.9 V
	AVSS	GROUND	Analog domain ground
	DVDD	SUPPLY	Digital domain supply; currently set to 1.9 V
	DVSS	GROUND	Digital domain ground
	PVDD	SUPPLY	PLL supply; DVDD and PVDD connected together on TC
	PVSS	GROUND	PLL ground; DVSS and PVSS connected together on TC
	PWELL	SUBSTRATE	Substrate bias; currently connected to AGND on TC
	SUB	SUBSTRATE	Substrate bias; PWELL and SUB connected
TRANSITION CARD	AVDD/AVDD_IN	SUPPLY	Analog domain supply; AVDD = 3.0 V, AVDD_IN= 1.9 V
	AGND	GROUND	Analog domain ground
	AVDD/AVDD_IN	SUPPLY	Dnalog domain supply; DVDD = 3.0 V, DVDD_IN= 1.9 V
	GND	GROUND	Digital domain ground
	PWELL	SUBSTRATE	Substrate bias; currently connected to AGND on TC

Analog domain: The power and ground nets that supply the analog part of the ALPIDE have the names AVDD and AVSS. However, the power net on the TC that provides 1.9 V to the ALPIDE is called AVDD_IN. This name is only visible in the schematics of the TC. The power net that supplies the TC (the voltage regulators) is also called AVDD, and it is recommended to be 3 V. The ground net is called AGND on the TC.

Digital domain: The power and ground nets that supply the digital part of the ALPIDE have the names DVDD and DVSS. However, the power net on the TC that provides 1.9 V to the ALPIDE is called DVDD_IN. This name is only visible in the schematics of the TC. The power net that supplies the TC (the voltage regulators) is also called DVDD, and it is recommended to be 3 V. The ground net is called GND on the TC.

PVDD/PVSS: The power net PVDD supplies the Phase Locked Loop (PLL) of the Data Transmission Unit (DTU). PVDD and DVDD are separated on the flex cable but reconnected on the TC. This means that PVDD is currently set to 1.9 V as well. The ground net is called PVSS.

PWELL: Bias of the p-type wells in the pixel region. The purpose of the PWELL is to regulate the intensity of the sensing diode of the pixels. The TC does not control the PWELL net. The current design suggests that the PCU will regulate the PWELL. It is currently connected to the analog ground net (AVSS) via an 0 Ω resistor, i.e., it is set to 0 V.

SUB: Bias to the substrate contacts in the seal ring and the periphery region.

The PWELL and SUB nets are electrically connected through the conductance of the die substrate.

4.5 Design of Transition Card

This section proposes which components should be used on the TC. All restrictions and requirements are taken into consideration when choosing the components.

Table 4.2 shows the suggested components, and the following subsections explain the reason and the function of each component.

Table 4.2: Reduced BOM of Transition Card V1.0 (resistors and capacitors not included).

Component	Amount	Part number
Linear Voltage Regulator	12	MIC29302AWD
FireFly connector part 1	12	UCC8-010-1-H-S-1-A
FireFly connector part 2	12	UEC5-019-1-H-D-RA-1-A
ZIF connector	12	541323633
Power connection	1	172249-0100

The complete schematics regarding TC V1.0 are presented in Appendix A.

4.5.1 Linear Voltage Regulator

One of the requirements states that ALPIDEs must be supplied with a constant voltage of 1.9 V and with current up to 1.1 A. For this, the MIC29302 linear voltage regulator from Microchip was chosen. It can deliver up to 3 A, and the output voltage can be adjusted by means of two external resistors from 1.24 V to 15 V. It has a protection circuit against overcurrent faults, reversed input polarity, reversed lead insertion, and overtemperature operation [17].

As previously mentioned, the analog and the digital environment should be supplied separately. A good circuit design needs to be deployed with respect to keep the analog environment clean from the noise. Each string is powered by two voltage regulators to filter this noise and keep the power rails isolated.

The schematics in Figure 4.2 shows the two voltage regulators, where one regulates the AVDD net and the other the DVDD net for one 9-chip string. The required output voltage is 1.9 V. Two external resistors must be connected to the output and the adjustable pin to achieve this.

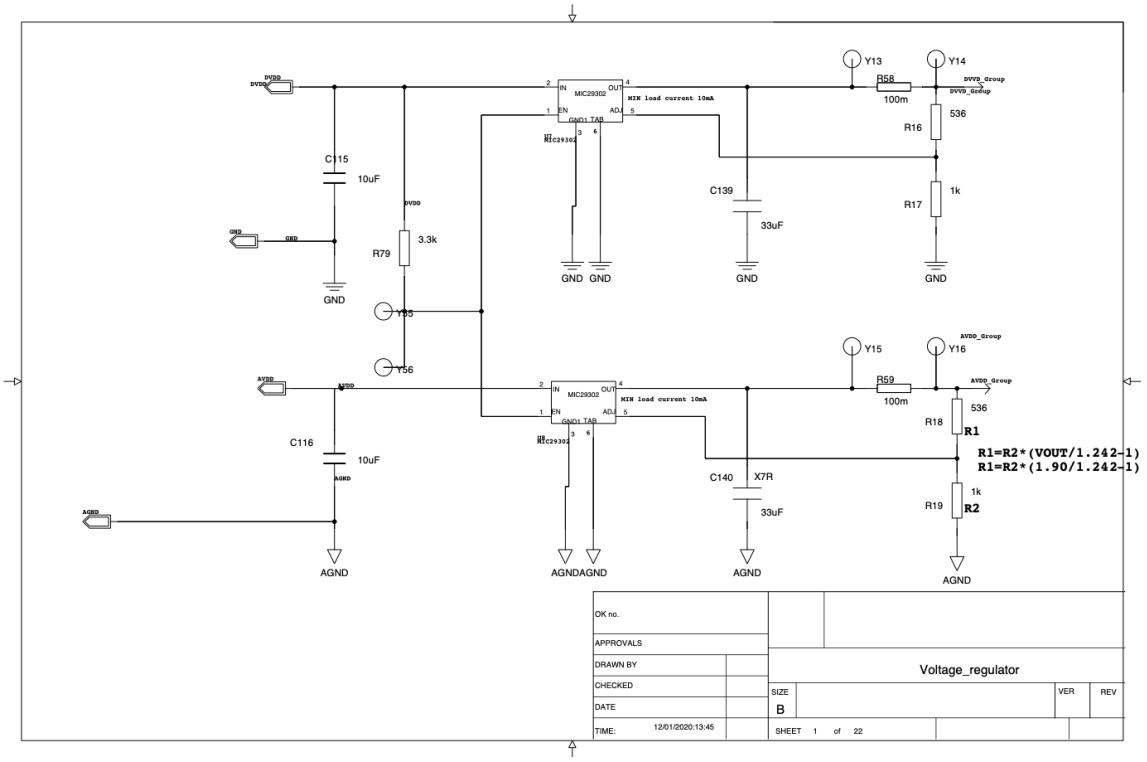


Figure 4.2: Schematics of the voltage regulators part.

The R2 resistor is selected to be 1 kΩ and R1 is calculated according to the equation 4.1 to be 530 Ω. The closest standard resistor value is 536 Ω. This makes the output voltage to be 1.91 V (see Equation 4.2). The reference voltage for MIC29302 is 1.242 V [17].

$$R1 = R2 \times \left(\frac{V_{out}}{V_{ref}} - 1\right) = 1000 \times \left(\frac{1.9}{1.242} - 1\right) = 530\ \Omega \tag{4.1}$$

$$V_{out} = V_{ref} \times \left(\frac{R1}{R2} + 1\right) = 1.242 \times \left(\frac{536}{1000} + 1\right) = 1.91\ V \tag{4.2}$$

It must be taken into account that the voltage regulator and resistors are not ideal and that they have their inaccuracies. Both resistors have 1% tolerance, and the voltage regulator has 2% accuracy.

$$V_{out\_min} = V_{ref\_min} \times \left(\frac{R1_{min}}{R2_{min}} + 1\right) = 1.215 \times \left(\frac{530.64}{990} + 1\right) = 1.87\ V \tag{4.3}$$

$$V_{out\_max} = V_{ref\_max} \times \left(\frac{R1_{max}}{R2_{max}} + 1\right) = 1.267 \times \left(\frac{541.36}{1010} + 1\right) = 1.95\ V \tag{4.4}$$

Equations 4.3 and 4.4 estimate the range of the output voltage. This range is within the accepted values for recommended operating conditions for the ALPIDE chips (1.62 - 1.98 V [16]).

The regulator has an active-high enable pin, which is set high by default (pulled up by a 3.3 kΩ resistor), but it can be set to low by connecting it to the ground. The enable pins of the two regulators for each string are connected, and this connection is extended onto the Power Control Unit. In this fashion, the regulators are in operating mode, and if needed, the enable pin can be switched to ground and thus disabling the regulator for each string individually. The regulator can indeed power several strings with its ratings; however, we will lose the possibility to control and monitor the power delivered to an individual string. This is useful for cutting off the power for the distinct string in case of emergency, troubleshooting, or testing.

Decoupling Capacitors

Figure 4.3 shows the power distribution structure of a system containing a model of a voltage regulator, power and ground planes, a chip package, and a chip. This figure is a suitable representation of the power system between the TC and the ALPIDE as well. The voltage regulator is presented as an ideal voltage source with small resistance and inductance of its pins. The power and ground planes add some further resistance and inductance into the system. All capacitors are modeled as ideal capacitors with an effective series resistance and an effective series inductance, except the on-chip capacitor, which has insignificant inductance because it sits very close to the switching loads [18].

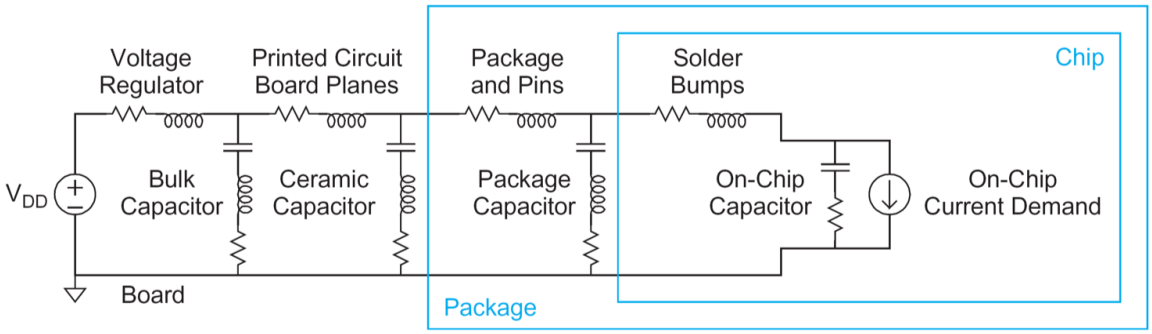


Figure 4.3: Power distribution model in a system [18, Figure 12.20].

These capacitors are called a bypass or decoupling capacitors, which act as power storage. Every time there is an instantaneous current spike on the power network, the voltage regulator cannot respond quickly enough to the change due to the resistance and inductance of the power lines (i.e., the copper traces). That is why the decoupling capacitors are placed on the power lines to compensate for this delay. Decoupling is essential because ICs are sensitive to ripples and noise occurring on

the power lines. The performance of ICs can degrade over time if the power supply variations are left untreated [19].

There are two 22 µF capacitors on AVDD power line, two 22 µF capacitors on DVDD power line, and two 10 µF capacitors on PWELL power line per ALPIDE chip on the flex cable. A 10 µF capacitor is placed by the input pin of the regulator. This helps to rectify the transient response of the input voltage line. The output pin has a 33 µF capacitor as well in case of sudden current spikes in the power lines. The manufacturer [17] recommends these values. In addition, there are three capacitors with different values (0.1, 1, and 10 µF) located by the ZIF connector for each power line, i.e., AVDD, DVDD, and PWELL.

Radiation Distribution

As discussed in Section 2.3, the Total Ionizing Dose (TID) accumulated by protons can seriously damage a semiconductor device. The only semiconductor component on the TC is the voltage regulator, and it must be radiation tolerant. MIC29302 has been used in ALICE experiment at the Readout Control Unit Version 2 (RCU2) for several years now. Since it has been proven to withstand the radiation in ALICE experiment and in various beam tests, it is deemed safe to use it in our experiment where smaller doses of radiation will be present. It was also tested successfully to a total dose of 10 krad [20].

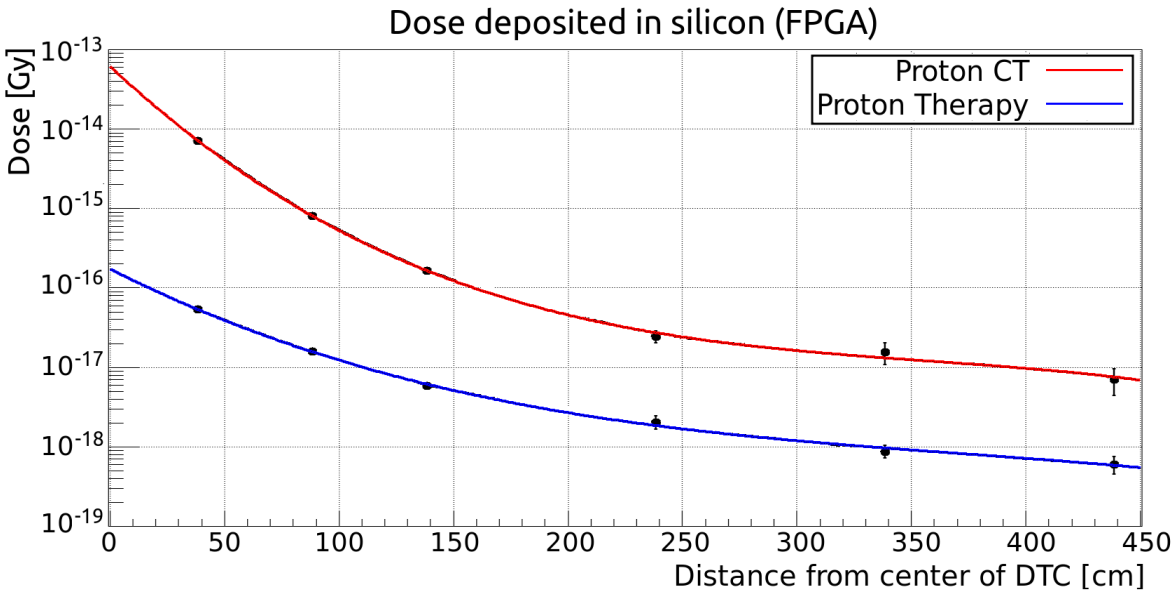


Figure 4.4: Dose deposition in silicon [Gy per proton][21].

The red curve in Figure 4.4 shows the third-order polynomial that demonstrates how much dose will be deposited in a silicone block, e.g., voltage regulator or

FPGA, as a function of distance during proton CT scanning. The regulators are about 20 cm away from the center of the DTC. Thereby, the deposited dose in the silicone will be:

$$\begin{gathered} y(x) = -13.20691 - (0.02698075x) + (0.00006945826x^2) - (6.452336 \times 10^{-8}x^3) \\ y(20\ cm) = -13.72 \\ Dose(x) = 10^{y(x)} \\ Dose(20\ cm) \approx 10^{-13} Gy\ per\ proton \end{gathered} \tag{4.5}$$

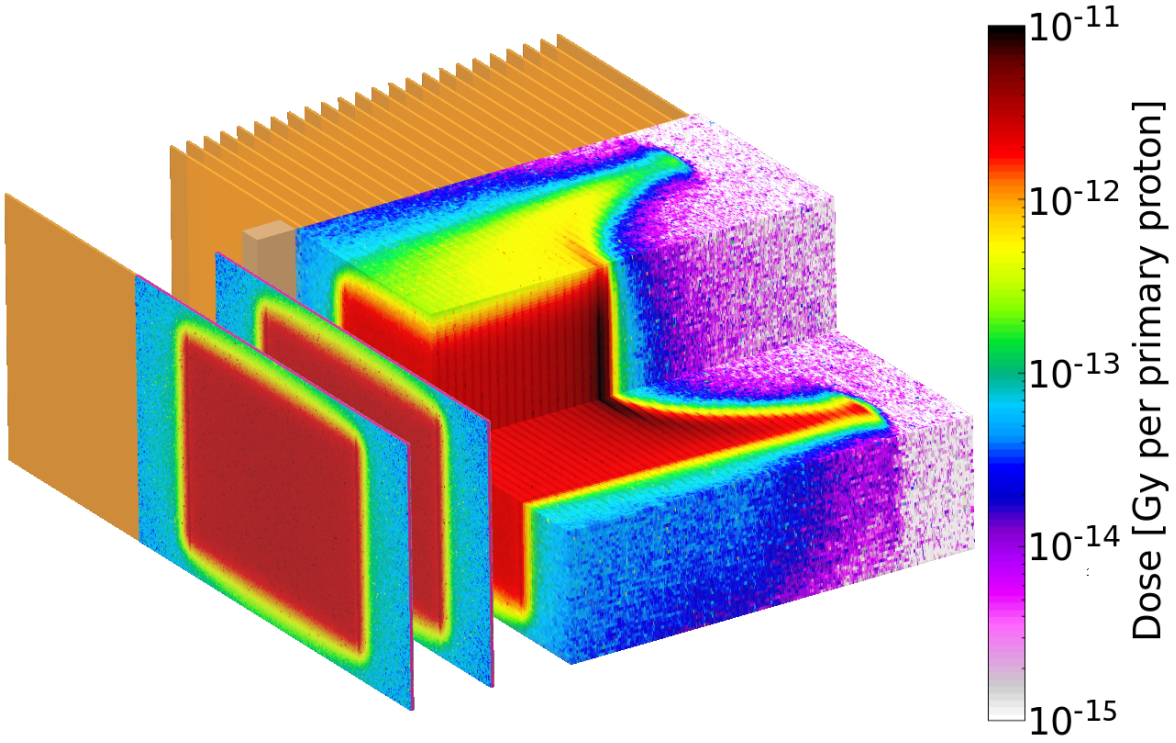


Figure 4.5: Dose deposition in DTC [Gy per proton] [21].

Simulation in Figure 4.5 also confirms that the dose at the edge of the DTC is approximately 10^{-13} Gy per proton. If we assume that the proton beam intensity is 10^7 protons per second, then the total dose in silicon will be:

$$\begin{gathered} Dose(silicon) = 10^{-13}\ Gy/proton\ \times 10^7\ protons/s\ = 10^{-6}\ Gy/s \\ = 10^{-6}\ Gy/s\ \times 100\ rad\ = 10^{-4}\ rad/s \end{gathered} \tag{4.6}$$

Since it is proven that the voltage regulator can tolerate up to 10 krad, the time before this dose is reached will be:

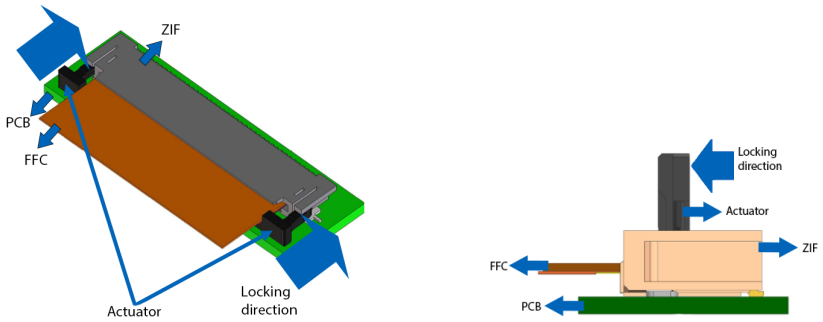
$$\frac{10^4\ rad}{10^{-4}\ rad/s} \approx 3\ years \tag{4.7}$$

Simply put, it takes little over 3 years of continuous radiation with the intensities and energies required for pCT imaging, before voltage regulators start to malfunction. If we conclude that the radiation will be present only during pCT imaging and that it takes 240 seconds to acquire one pCT scan, the regulators will withstand around 410 000 scans.

4.5.2 ZIF Connector

The connection between the flat flex cable and the TC is secured by a Zero Insertion Force (ZIF) connector. This connector is also referred to as Flexible Flat Cable or Flexible Printed Circuit connector. The selected ZIF connector, manufactured by Molex, meets both electrical and mechanical requirements.

It has 0.5 mm pitch, 36 contacts, bottom contact position, and 0.5 A rated current. The connector comes with two different plating options: Tin-Silver-Bismuth and Gold plating. The Sn-Ag-Bi plating is more preferable because it is almost identical to the plating of the flex cable used with the ALPIDEs (Tin-Nickel-Bismuth).



(a) Slider (b) Flip

Figure 4.6: Different types of actuators for a ZIF connector. [2]

Molex provides two types of actuators on the connector: flip and slider. The slider type of actuator (see Figure 4.6a) opens and closes in the same direction as the flex cable, and it keeps the flex cable fixed by blocking it into the ZIF connector. The advantage of the slider is that if it breaks, another piece of non-conductive material can be used to wedge the cable into the connector. The disadvantage is that it is often difficult to insert the cable into the connector and align the traces on the flex cable with the contacts of the connector. Another disadvantage specific for our model is that the minimum gap between the two connectors is about 4 mm, which is a quite narrow space. The flip type (see Figure 4.6b) opens all the way up so that the contacts of the ZIF connector are left exposed. In this manner, it is easier

[2]Figures obtained from different Molex datasheets.

to insert the cable and close the flip actuator. The common issue with this type is that when the actuator breaks, it cannot be repaired. This would mean that the connector must be resoldered.

The latter reason has been the deciding factor to use the slider type of actuator. Since the TC V1.0 has been in use, the experience was that it is possible to open and close the actuator despite the tight gap. However, a special tool would make the process easier and faster. A flat-head screwdriver made of ESD material (see Chapter 5) is suitable for this purpose.

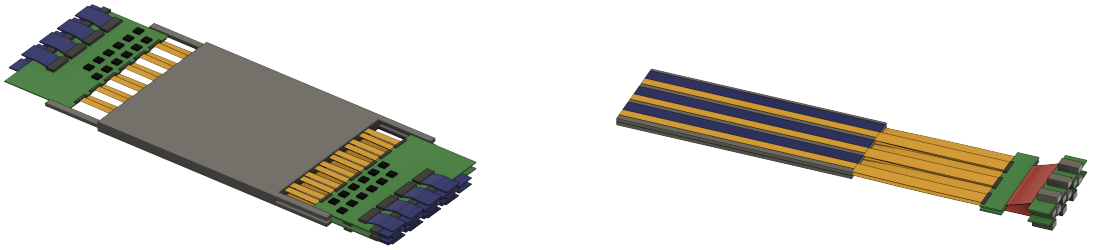
A general disadvantage with ZIF connectors is that they have low durability. Every time the flex cable is pressed into the ZIF connector (also called a mating cycle), the connector wears out. The Molex connector can withstand 20 cycles. This should be taken into consideration during testing, assembly, and maintenance of the prototype.

4.5.3 High-Speed Signal Connection

The TC and the pRU are linked together through Samtec's FireFly cable assembly system. This system is a series of interchangeable copper or optical cables and connectors with a small footprint that offer high data rates and different cable configuration [22]. This type of cable assembly has already been used for Inner Tracking System and the VCU118 evaluation board in the pCT project.

The space restrictions were stricter in the initial design of the detector than they are now. The air gap or the gap between two half sensor layers was meant to be 1 mm. This means that the space between two Transition Cards was 8.3 mm while the FireFly cable and the FireFly connector built up to 8 mm height. This made the clearance to be 0.3 mm, which was not approved by the mechanical team.

Two alternatives were suggested to resolve this problem. The first suggestion was using an alternative cable assembly provided by Samtec. The Direct Connect System (DCH) is similar to the FireFly system with the difference that it has fewer differential pairs available per assembly, and it is connected straight to a PCB so that no extra connector is needed (press-fit connection) [23]. This DCH solution would need 17 connectors per DTC layer (see Figure 4.7a). The second option was to keep using the FireFly system connected to the rest of the circuitry by a Flexible Printed Circuit (FPC) allowing the PCBs with FireFly connectors to fan out, and thereby fit into the design (see Figure 4.7b; FPC is marked as red). This approach is feasible but requires a rigid-flex PCB system, which is relatively complicated and more costly than a standard rigid PCB.



(a) DHC solution (b) combined rigid-flex PCB and FF solution

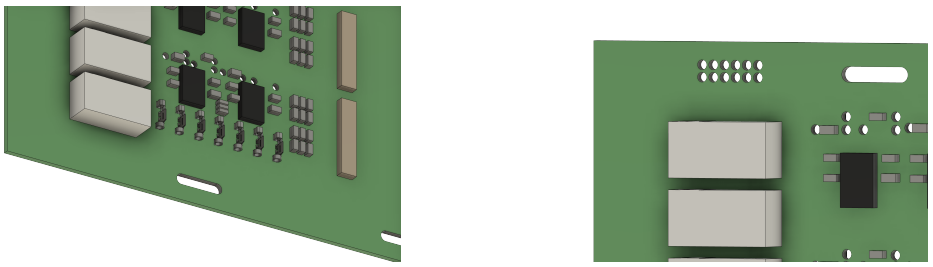
Figure 4.7: Different solutions for the FPC-TC connection.

In the recent design, the air gap has been luckily increased by 1 mm, thereby increasing the clearance and allowing us to go back to the initial plan utilizing the FireFly system. However, the different strategies mentioned above are included in the thesis in case the space constraints change again.

4.5.4 Power and Enable Signals Connection

The power connection must be compatible with the 1.5 mm^2 copper cables, and it must withstand current up to 6 A. There are two approaches to connecting a cable to a PCB, either solder them directly to the board or joining them via a connector. The first approach has been used for TC V1.0, where crimp terminals are first crimped around the wire and then soldered directly to the board. The height of the terminals is 3.3 mm when inserted to the board, which is the deciding factor for using them since the size doesn't collide with the space restrictions (see Figure 4.8a). The terminals are right-angled, and they provide good strain relief for the cables and the terminals as well. The current rating is also kept within the range; crimp terminals are rated for currents up to 14 A [24].

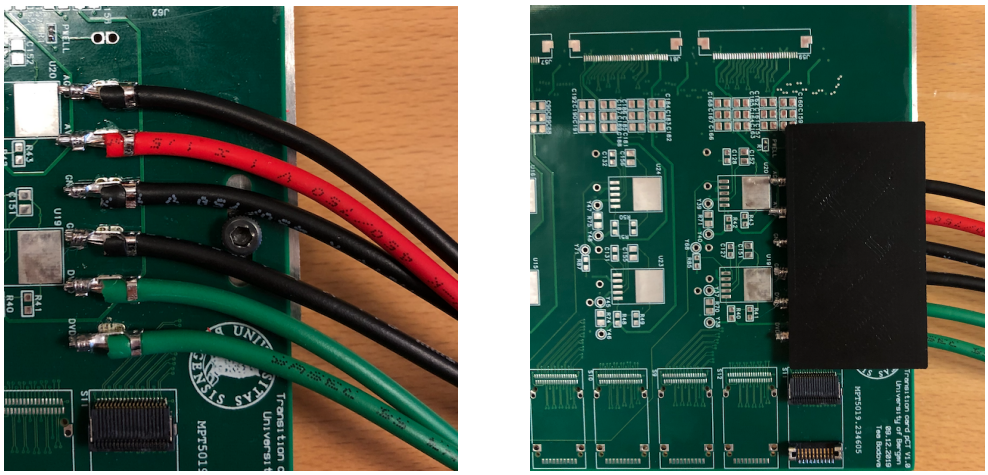
The enable signals connection is kept simple. The signals are only routed to plated holes, to which thin, flexible cables can be soldered (see Figure 4.8b).



(a) crimp terminals (b) plated holes

Figure 4.8: Crimp terminals and enable signals connection on TC V1.0.

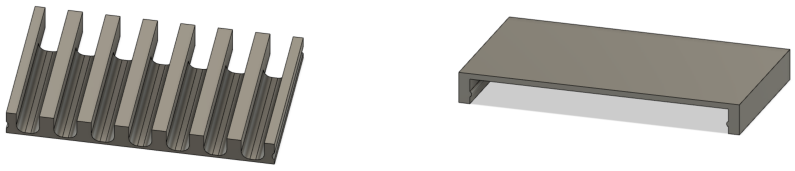
Figure 4.9a shows the soldered crimp terminals with power cables. As long as the cables are kept in a straight position, there have been no problems with the connection. However, when the cables were bent, the crimp terminal started to break off. As a result, cable support was designed to reinforce the connection. The structure holds the power cables in a straight position, and the bending starts rather outside the TC (see Figure 4.9b).



(a) soldered crimp terminals (b) cable support

Figure 4.9: Power connection on TC V1.0.

The support consists of two parts: the bottom and top (see Figure 4.10). The bottom part can be glued to PCB, but from experience, it is enough to slide the part in between the terminals. In this way, the support prevents a possible short circuit between crimp terminals or cracks in solder joints since the bending point is shifted further from the crimp terminals. The top part is removable.



(a) bottom (b) top

Figure 4.10: 3D design of the cable support.

Two main issues have emerged after the completion of the TC V1.0 design. The first issue is that air ducts have been introduced into the DTC design (see Appendix C). This structure hinders that the power cables are routed on the top or bottom

of the TC as initially intended. The best strategy is to route the cables in the same direction as the FireFly cables. The second issue is that it is planned to place temperature sensors on the string carriers and one on the TC to monitor the temperature of both. This implies that the sensors are connected to the TC, and the signals are routed further with the enable signals to the Power Control Unit.

For this purpose, the TC should be made wider to create space for the connection. It is suggested to extend the card by 25 mm on the FireFly side and place the new power connector in the center of the edge. In this way, the position will be universal, so there won't be any right or left configuration. The new power connector is shown in Figure 4.11, and it meets all requirements:

- It must have 7 contacts.
- It must have maximum height of 8.5 mm.
- It must have current rating $\geq$ 6 A.
- It must be detachable.
- It must be right angle.
- It must be suitable for 1.5 mm^2 cables.

It is a two-part connector from Weidmüller, where one part (the male header [25]) is soldered to the PCB and the cables are attached to the second part (female plug [26]), which can be disconnected at any time. The second issue is that the power cables will be as long as 4 m, and for this reason, it is cumbersome to solder seven long cables to the board without the option to disconnect them at any time. This would make assembly or service of the DTC very complicated.

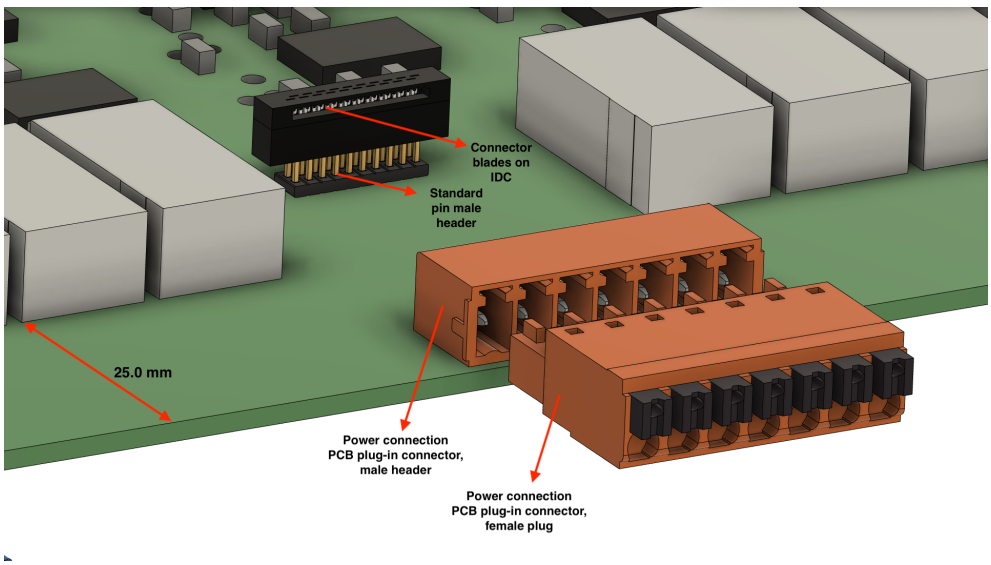


Figure 4.11: Detailed 3D design of the power and the temperature sensors and enable signals connection on TC V2.0.

A new pin male header connector is placed behind the power connector and between the FireFly connectors. It has 20 contacts dedicated to twelve enable signals and the rest to temperature signals. One contact should be dedicated to the ground net for reference. The second part of the connector is an Insulation-Displacement Connector (IDC) that has inbuilt sharp blades, which cut through the insulation of a flat cable when inserted. This connector offers a smooth and swift installation and is compatible with the standard pin header. Therefore the cable used with IDC must be flat at the end. However, no cable can go over the power connector since there is limited space. Figure 4.12 presents how this problem can be resolved by using a flat cable that is compressed into a round shape. In this manner, only the flat part is connected to IDC, and the round cable runs easily past the power connector.

These updates will be part of the second iteration of the TC.

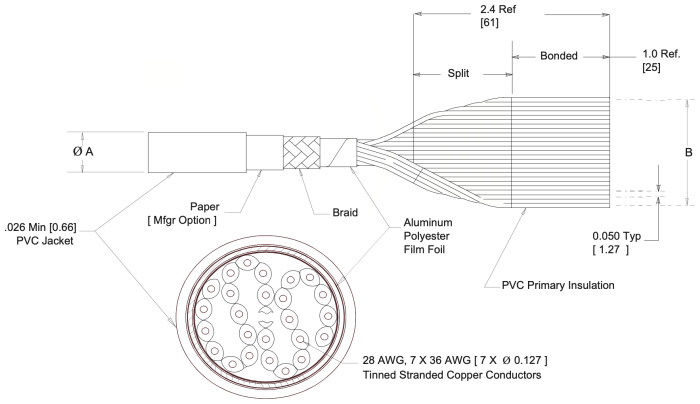


Figure 4.12: Drawing of the cable used for the temperature sensors and the enable signals connection [27].

4.6 Signal Integrity

Technology advancement keeps pushing the boundaries on how fast data is transferred in the electronic systems. It has become a standard that electronics work in the 1 GHz and higher frequencies range. When designing systems in this high-speed domain, the physical traces cannot be treated as standard traces but rather as transmission lines. Traces carrying fast-switching signals have a characteristic impedance that influences the signal in a significant way. This must be taken into account, and careful design rules must be applied for the PCB to work properly.

4.6.1 Transmission Lines

The term transmission line is used to describe a conductor with uniform cross-section that carries voltage and current as waves. The conductor can either be a cable (usually coaxial cable) or e.g. a trace on a PCB (microstrip or stripline; see Figure 4.13). The conductor can't be treated as a simple static wire anymore when its length is greater than one-fourth of the signal wavelength [28]. For example in case of ALPIDE chip, the clock frequency is 40 MHz. The wavelength is then:

$$\lambda = \frac{speed\ of\ light\ in\ transmission\ line\ (km/s)}{frequency\ (1/s)} = \frac{0.7 \times 300\ 000(km/s)}{40\ 000\ 000(1/s)} = 5.25 \times 10^{-3}\ km \tag{4.8}$$

One-fourth of that is about 1.3 m. The length that the clock signal must propagate through is greater than that since the distance between ALPIDEs and the pRU is at least 4 m. The threshold of the propagation length is even lower for the data signal operating in the GHz range.

The most important property of the conductor is then its impedance, also called characteristic impedance Z_0. Z_0 is determined by the width of the trace, its thickness, and the constant of the dielectric surrounding the trace. If the trace is routed on the dielectric, i.e., microstrip, the Z_0 is also influenced by the space between the trace and the next plane. If the trace is routed inside the dielectric, i.e., stripline, the height between the plane above and below the stripline is also accounted into the Z_0 calculation. The equations presented below are approximations for the Z_0 recommended by the IPC [29].

Z_0 approximation for microstrip:

$$Z_0 = \frac{87\ \Omega}{\sqrt{1.41 + \varepsilon_r}} ln\left(\frac{5.98\ h}{0.8\ w + t}\right) \tag{4.9}$$

Z_0 approximation for stripline:

$$Z_0 = \frac{60\ \Omega}{\sqrt{\varepsilon_r}} ln\left(\frac{2\ b + t}{0.8\ w + t}\right) \tag{4.10}$$

where: Z_0 = characteristic impedance, in Ohms
h = dielectric thickness below the signal trace to the plane, in mils
w = trace width, in mils
b = plane-to-plane spacing, in mils
t = trace thickness, in mils
ε_r = dielectric constant

(a) microstrip (b) stripline

Figure 4.13: Transmission lines represented as traces on a PCB [29, Figure 7-30].

4.6.2 Differential Signaling

An electrical signal is traditionally transmitted through a single wire. This method is called single-ended signaling. It is widely used for its simplicity and low cost.

The alternative method is differential signaling. It uses a pair of transmission lines where one line carries the signal, and the other line carries the inverted signal. The receiver then compares both lines, and the difference between them is the data, hence the name differential signaling (see Figure 4.14).

The advantage of differential signaling is that it is less susceptible to noise, EMI (Electromagnetic Interference), and ground bounces than single-ended signaling. The disadvantage is double the amount of conductors and more complex design rules.

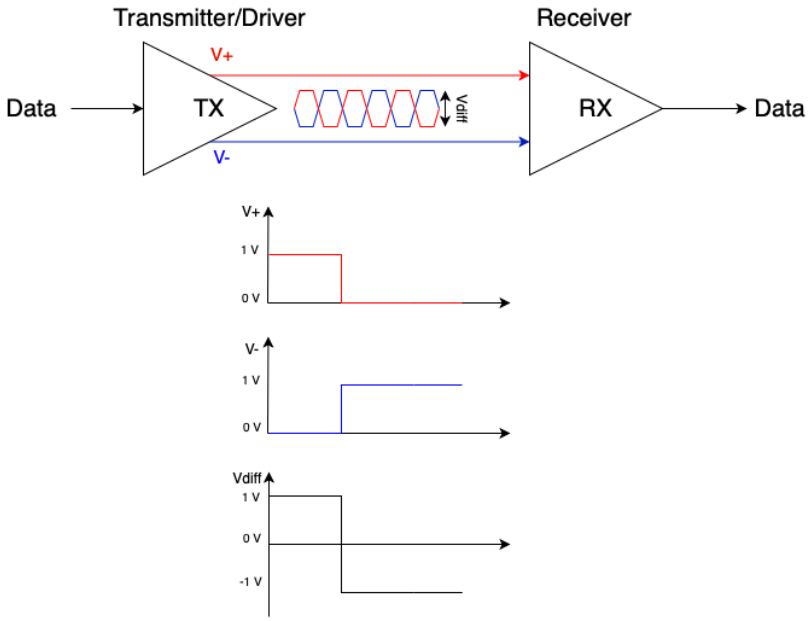


Figure 4.14: Differential signaling.

Impedance in Differential Signaling

As previously described, the impedance of a trace is called characteristic impedance, Z_0. The impedance between the traces in differential signaling is called equivalent or differential impedance, where:

$$Z_{equivalent} = Z_{diff} = 2 \times Z_0 \tag{4.11}$$

(a) Characteristic impedance, Z_0 (b) Differential impedance, Z_{diff}

Figure 4.15: Impedance in differential lines [29, Figure 11-8].

Nevertheless, this is only the simplified estimate, and Z_{diff} varies for different types of traces.

Z_0 approximation for microstrip in FR4 dielectric [3]:

$$Z_{diff} = 2 \times Z_0 \left[1 - 0.48 \exp\left(-0.96 \frac{s}{h}\right)\right] \tag{4.12}$$

Z_0 approximation for microstrip in FR4 dielectric:

$$Z_{diff} = 2 \times Z_0 \left[1 - 0.37 \exp\left(-2.9 \frac{s}{b}\right)\right] \tag{4.13}$$

where:
Z_{diff} = differential impedance, in Ohms
Z_0= the characteristic impedance, in Ohms
s = edge-to-edge separation between the traces, in mils
b = total dielectric thickness between the planes, in mils

(a) microstrip (b) edge-coupled stripline

Figure 4.16: Different types of differential lines.

[3]The FR4 is commonly used type of dielectric. FR4 is used in Transition Card as well.

Coupling

As current runs through a conductor, fringe magnetic fields and fringe electric fields arise around the conductor. In the case of differential signaling, where two conductors are in close proximity, electromagnetic fields interact with each other. This EMI produces coupling. Figure 4.17 shows the coupling in differential lines. If the current runs in one direction across the wire and in the opposite direction across the other wire, the magnetic fields have opposite polarity and will cancel each other out. The electric fields of these two conductors will couple. The coupling is thus set by the mutual capacitance and inductance per length [29, Chapter 11].

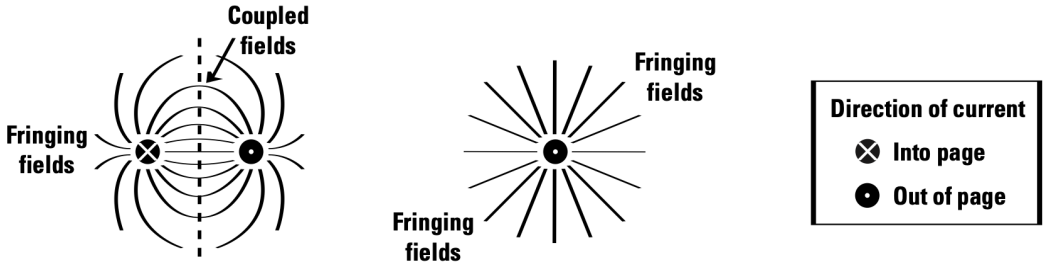


Figure 4.17: EMI in differential (left) and single-ended (right) signaling [30, Figure 3.4].

Outside PCBs, twisted pair cable is used, where two wires are wrapped around each other to keep the two conductors in the immediate vicinity to achieve the coupling. This is, however, not the case for pCT prototype. The FireFly High-Speed I/O assembly from Samtec incorporates ultra low skew twinax cable technology with 100 Ω impedance configuration achieving data rate up to 28 Gb/s. This technology is based on two copper wires surrounded by a dielectric and shielded by other insulating materials representing one differential line [31]. This gives us improved coupling and better controlled impedance than in twisted pair cables.

Within PCBs, the differential lines are also routed adjacent to each other. It is important to underline that the coupling and the impedance of the differential lines are entirely dependent on the shape of the conductors and the material properties, i.e., dielectric, rather than other factors such as voltage, current or data rate.

Differential Signaling in pCT

The Data Transmission Unit (DTU) is the block that is in charge of the data transmission on the ALPIDE chip. The data is transmitted over one differential pair per chip with a line rate of 1.2 Gb/s to the pCT Readout Unit. However, the line combined with 8b/10b encoding provides a data throughput of 960 Mb/s. The 8b/10b encoding is employed to achieve DC-balance by encoding an 8-bit word

into a 10-bit symbol. The DTU is designed to be compatible with the Low-Voltage Differential Signaling (LVDS) standard [16]. This is essential because the FPGA that acquires the data uses the LVDS standard [32].

Figure 4.18 shows the diagram of the ALPIDE DTU. The driver outputs current between 0 and 5 mA, which then propagates through the differential pair. This is different from the driver in the LVDS standard that applies 3.5 mA. The current can be changed by modifying register settings via the ALPIDE control interface. Furthermore, the DTU can also provide pre-emphasis that can neutralize some of the detrimental effects of the transmission line.

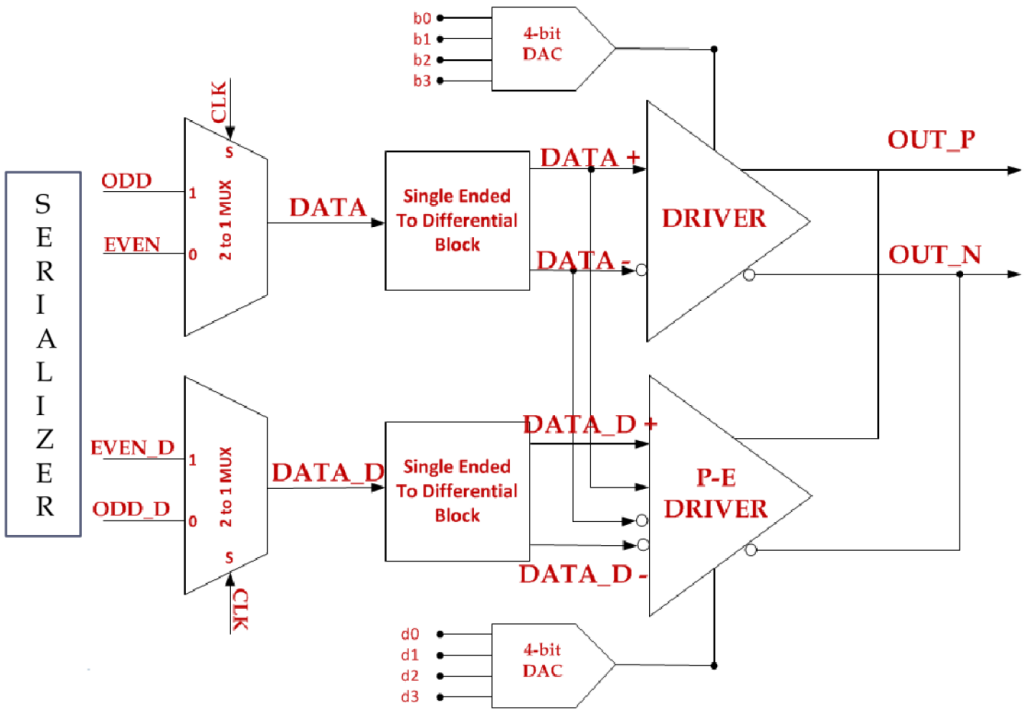


Figure 4.18: Functional diagram of the DTU [16, Figure B.1].

Figure 4.19 shows the circuitry of a LVDS standard with a controllable current source. The input of the receiver typically has a high impedance, and for this reason, most of the current flows across the 100 Ω termination resistor and creates current-to-voltage conversion. This results in low drop-out voltages along the termination resistor sensed by the receiver, hence the name Low-Voltage Differential Signaling. The termination resistor also matches the differential impedance, Z_{diff}, to prevent reflections. The output common-mode voltage is set to 0.9 V to reduce the power consumption compared to the LVDS standard that uses 1.2 V [16]. The low voltage swings further reduce crosstalk and EMI.

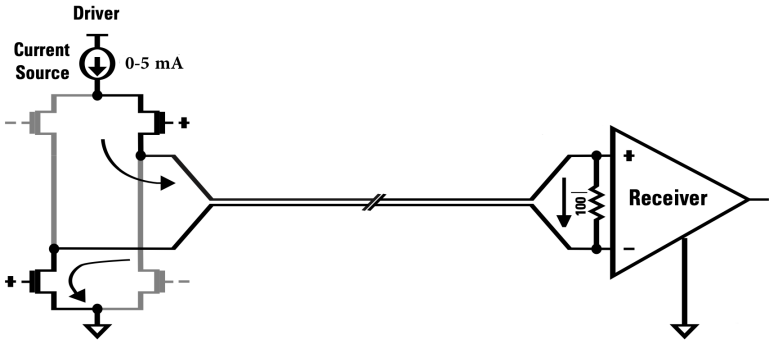


Figure 4.19: Modified circuitry of the basic Low-Voltage Differential Signaling [30, Figure 1.1].

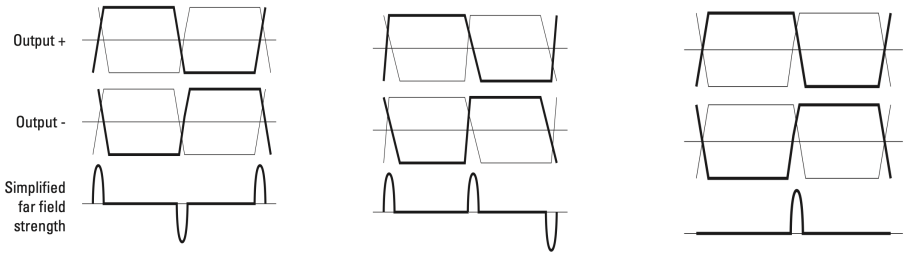
Challenges in Differential Signaling

Differential signaling in the high-speed domain will work correctly only if the properties of the differential lines are thoroughly followed and controlled. If this is not the case, issues such as crosstalk, EMI, and reflections occur and corrupt the signal. If an external noise affects a balanced differential pair, the disturbance will appear as common-mode noise, and the receiver will reject it.

This can be expressed as:

$$V_{diff} = (V_+ + V_{noise}) - (V_- + V_{noise}) = V_+ - V_- \tag{4.14}$$

Improper and unbalanced driving of the signal can cause skew, unbalanced edge rates, and pulse widths (see Figure 4.20). The electromagnetic fields around the traces no longer have the same strength and will not cancel each other out. The stray fields can escape the coupling and propagate to the far field (further from the source/driver) increasing EMI. In other words, the differential pairs' waveforms must be balanced to benefit from the differential signaling [30].



(a) skew within pair (b) unbalanced edge rates (c) unbalanced pulse widths

Figure 4.20: Disturbances in far field when differential pair is unbalanced [30, Figure 3.10].

As the signal reaches the receiver, and the impedance does not match, part of the signal will be reflected in the transmission line (see Figure 4.21). The reflection will interfere with the incoming signal since the signal is transmitted at a high rate, and the reflection will not have time to propagate through the line without disturbing it. For the same reason, it is important to keep the transmission line's impedance constant to avoid reflections on the line as well.

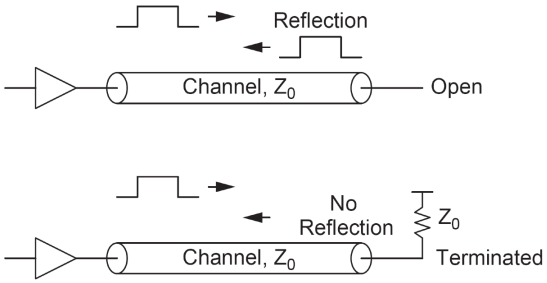


Figure 4.21: Unterminated (top) and terminated (bottom) channel [18, Figure 12.57].

The impedance of the differential receiver is usually very high. Therefore, a terminating resistor is placed between the pair that matches the Z_{diff}. In the 9-chip string, the control and clock signals are shared between the ALPIDEs, i.e.; they are Multipoint Low-Voltage Differential Signaling (MLVDS). They are also bidirectional and must be terminated by a 100 Ω resistor on both ends. The data signals are transmitted from the ALPIDEs and received by the FPGA on the pRU. The 100 Ω termination value is set internally in the FPGA [32]. Figure 4.22 represents how the interconnects between the 9-chip string and the off detector electronics work.

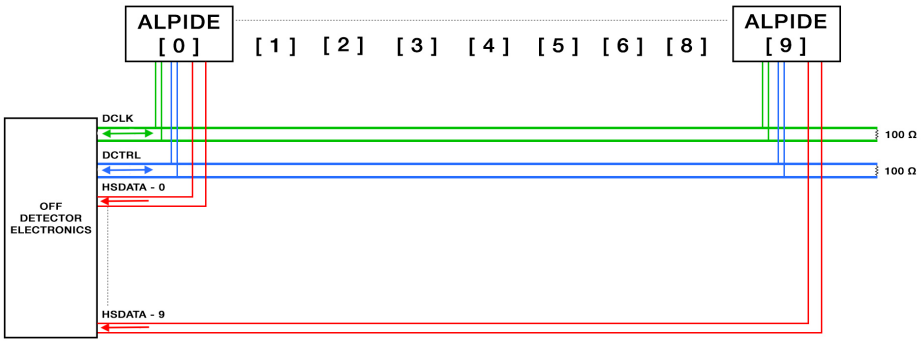


Figure 4.22: Simplified schematic diagram of the interconnections between the 9-chip string and the off-detector electronics [16, Figure 12.62].

4.6.3 Layout

The rules for designing a PCB that includes differential pairs and high-speed links must be closely followed to achieve good signal integrity. These rules include [29]:

- Matching the characteristic impedance (Z_0) and the differential impedance (Z_{diff}).
- Keeping the same length of both differential pairs.
- Keeping the differential pairs close for better coupling.
- Having a continuous ground plane adjacent to the differential pair.
- Avoid using vias with differential pairs.

The Transition Card was designed in Mentor Graphics software, which contains tools (such as Constraint Manager and Stackup Editor) that automatically calculate the space and the width of the differential pairs based on the thickness of each layer in the PCB and the required impedance.

The required differential impedance is 100 Ω. Thereby, the number and the thickness of the PCB layers must be defined first to determine the differential further pairs properties.

Multilayer PCB

This section explains the approach and reasoning when selecting the configuration of the multilayer PCB for the Transition Card. The amount of various connectors and voltage regulators requires that the top and the bottom layers, i.e., outer layers, are reserved for these components and their interconnects. The differential pairs must be consequently routed in another inner layer as striplines. Besides, the restricted card size and a large number of via holes dictate that more than one layer is needed for routing the 132 differential pairs, as shown in Figure 4.23. The pairs are connected to the board by the ZIF connectors and then routed through the inner layers to the FireFly connectors. The signals are further carried from the Transition Card to the pCT Readout Unit by the FireFly cable. It is a good designing practice that the stripline layer is embedded between two continuous planes, ideally ground planes [30]. These planes provide additional shielding from external EMI radiation. Even though it is not recommended to use via connections on the differential pairs traces, it is inevitable in this project.

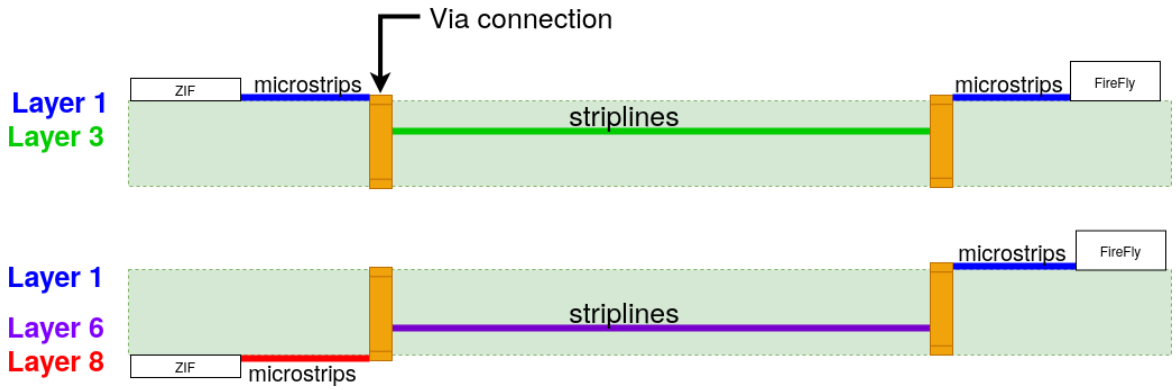


Figure 4.23: Simplified representation of how differential pairs are connected through the layers in the PCB.

Figure 4.24 shows the stackup of the card. A PCB stackup describes the order and the usage of the various copper layers and the thickness of the insulation layers, i.e., dielectric. The top and bottom layers of the stackup are reserved for the physical components (voltage regulators, connectors, passive components). As established before, the differential pairs (as striplines) need two separate layers with four additional shielding layers. In conclusion, the Transition Card needs eight layers in total.

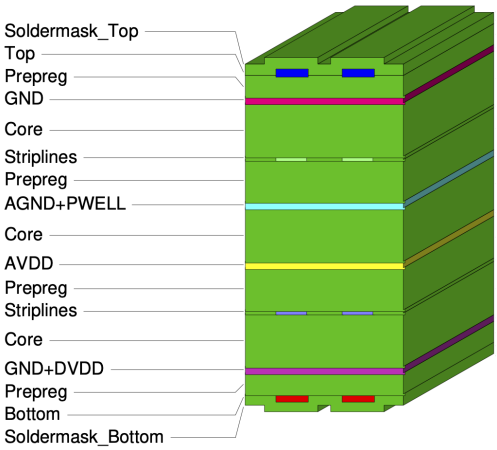


Figure 4.24: Stackup of the Transition Card (V1.0).

A layer in a PCB is the copper plane that is etched with track and pad patterns during the manufacturing process based on the layout. These conductive copper layers are separated by dielectric (insulating) layers of FR-4 material with specified dielectric constant. These dielectric materials between copper layers are called core and prepreg. Both materials are made of fiberglass. The difference between them is that the core is already cured with epoxy resin, and it has copper layers on either

side. The prepreg is used to connect two core layers. The material is only impregnated with the epoxy resin, which hardens when it is heated, thereby connecting the cores [33].

The PCB is finished off with a solder mask on the exposed (top and bottom) layers. The solder mask is a thin protective layer applied to the copper to avoid oxidation and short circuits between traces.

Table 4.3 presents the stackup of the multilayer Printed Circuit Board and the properties of each layer. The original stackup was selected based on the available configurations by the PCB provider. The width and the spacing of differential pairs were estimated accordingly.

Table 4.3: Stackup of Transition Card V1.0 and its layer properties.

			Differential pairs		**Original stackup**			**Updated stackup**			
Layer	**Type**	**Material**	**Spacing mm**	**Width mm**	**Thickness mm**	**Zdiff Ω**	**Dielectric constant**	**Thickness mm**	**Zdiff Ω^a**	**Zdiff Ω^b**	**Dielectric constant**
1	**signal & microstrip**	**copper**	**0.127**	**0.140**	**0.035**	**100**		**0.035**	**97**	**106**	
	prepreg	dielectric			0.1		4.6	0.109			3.8
2	plane	copper			0.035			0.035			
	core	dielectric			0.25		4.6	0.229			4.3
3	**stripline**	**copper**	**0.175**	**0.130**	**0.018**	**100**		**0.035**	**92**	**96**	
	prepreg	dielectric			0.2		4.6	0.300			4.05
4	plane	copper			0.035			0.035			
	core	dielectric			0.25		4.6	0.229			4.3
5	plane	copper			0.035			0.035			
	prepreg	dielectric			0.2		4.6	0.300			4.05
6	**stripline**	**copper**	**0.175**	**0.130**	**0.018**	**100**		**0.035**	**92**	**96**	
	core	dielectric			0.25		4.6	0.229			4.3
7	plane	copper			0.035			0.350			
	prepreg	dielectric			0.1		4.6	0.109			3.8
8	**signal & microstrip**	**copper**	**0.127**	**0.140**	**0.035**	**100**		**0.035**	**97**	**106**	

[a] Calculated by the manufacturer.
[b] Calculated by our design tools.

Once the constraints, the routing, and the layout were finalized, the whole design was submitted for production to the PCB provider. At that time, the provider could not ensure the original stackup and suggested to change mostly the thickness of the stripline layers from 0.018 mm to 0.035 mm. As seen from the last columns in Table 4.3, the dielectric constants for the insulating layers were modified as well. As explained in the previous section, the thickness of the traces and the dielectric constant are some of the variables that define the impedance of the differential pairs. Therefore, the impedance changed with the new stackup. The new impedance was calculated by the manufacturer to be 97 Ω and 92 Ω for microstrips and striplines, respectively. Our design tools determined the impedance to be 106 Ω and 96 Ω when using the updated stackup. Despite the differences in estimates, they are both within the 10% error. The TC V1.0 was therefore fabricated based on the updated stackup. The overall thickness of the PCB is 1.7 mm, which meets the spatial requirements.

One of the design rules states that both traces of the differential pair must have the same length. The driver ideally sends the signals across the pair at the same time. The receiver expects that both signals arrive simultaneously. For this to happen, the length of the traces must be maintained equally. The length typically does not match when the ends of the differential pair do not match, as seen in Figure 4.25. A technique called trace tuning adds a serpentine-like pattern to the shorter trace to match the length. As a result, the signals travel the same length and arrive synchronously at the receiver.

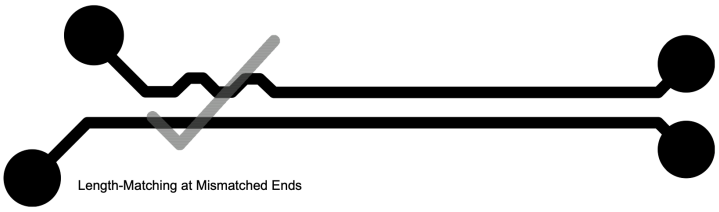
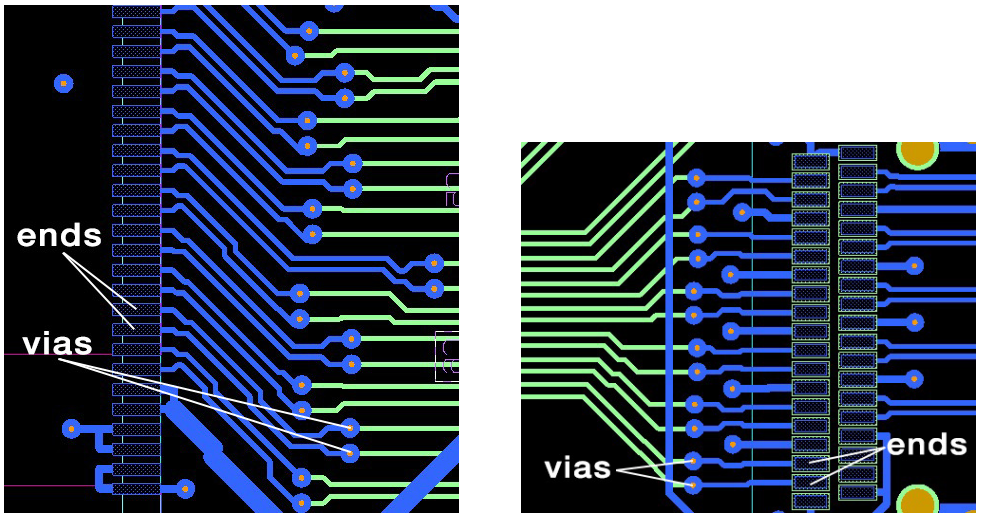


Figure 4.25: Length matching [34, Figure 5].

Figure 4.26 demonstrates that there are no mismatched ends on the TC. This rule was simple to follow in our design because both ends, i.e., ZIF and FireFly connectors, have matched ends. Hence, it was simple to keep the length matched, and the trace tuning technique was not required.



(a) ZIF connector (b) FireFly connector

Figure 4.26: Example of matched ends on both sides of differential pairs.

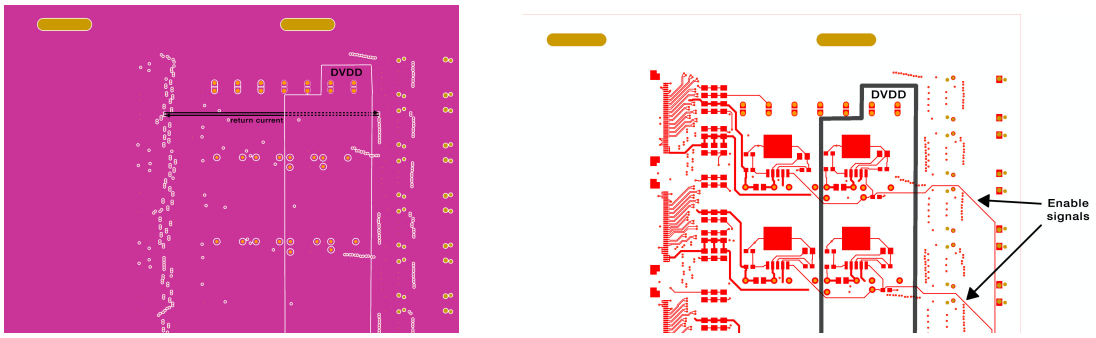
It is important to note that there are open vias on all differential pairs near two ZIF connectors (J54 and J60; see Appendix D). An open via does not have a solder mask on it, and a differential probe can be placed on them to test the signal quality.

The probe should be treated as a receiver, and the signals should arrive at the same time to these test points. Hence, they must be matched accordingly, as well.

The probe available in the laboratory is a TDP4000 4 GHz differential probe from Tektonix. The probe head has two tip pins that are 2.54 mm apart, and the vias on the TC are spaced 0.65 mm apart. Despite that, the probe comes with various adapters. One of them is the variable spacing adapter, where the tips can be adjusted in the range from 0.51 mm to 4.57 mm. The inconvenience with this adapter is that it can only sustain between 50 and 75 insertion cycles [35].

Power and Ground Planes

According to the design rules for good signal and power integrity of a PCB, it is preferable to have unbroken ground and power planes if possible. The low impedance of the continuous plane enables the currents and the return currents to achieve the shortest paths and to avoid creating current loop areas that can further generate noise into other parts of the circuitry. As for differential signaling utilized in our system, the ground planes will allow the common-mode current to return directly under the differential pairs [29]. This rule is, however, violated in the current design (TC V1.0). The violation occurs between layer 6 (striplines) and layer 7 (GND+DVDD).



(a) current layout (GND + DVDD) (b) proposed layout

Figure 4.27: DVDD and GND plane layout.

Figure 4.27a presents how the copper layer is divided into the GND plane and DVDD plane. The DVDD plane provides power for voltage regulators on both the top and the bottom layers through several via connections. A via is a copper-plated hole in the board to interconnect two or more layers. In all layout figures, the vias are displayed as orange circles with the smallest diameter. When a white ring encloses a via, it means that it does not connect to that specific layer. The figure also shows a representation of a differential pair routed on the adjacent layer. In this layout, the common-mode return current will not flow right under the differential

pair since the GND plane is interrupted by the digital plane. This is not directly an issue for the differential signals, but it should be taken into consideration when designing the second iteration of the card. The signal measurements in Chapter 5 confirm this assumption since they did not show any excessive distortion of the signal. Nevertheless, the TC has been tested only with one string.

Figure 4.27b offers a possible solution. The same shape of the DVDD plane can be moved to the bottom layer. The constraint with this arrangement is that the enable signals cut through this plane. This can be resolved by routing sections of the enable signals on the top layer to omit the DVDD plane.

A similar problem appears on the layer 4 (AGND + PWELL). Layer 4 is dedicated to AGND apart from a small portion that is specified for the PWELL net. Again, the current from vias on the left side has to flow around the PWELL. This issue can be corrected by moving the PWELL plane slightly to the left together with its vias, and by relocating the AGND vias to the right side of the PWELL plane.

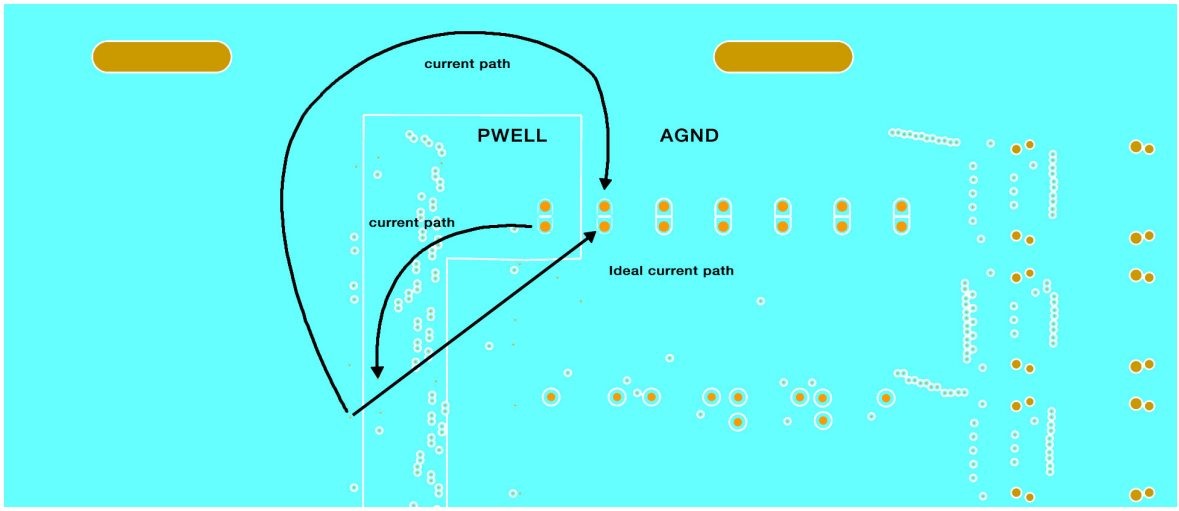


Figure 4.28: Current paths on PWELL and AGND plane.

These suggested changes are regarding the first version of the TC. The next version is going to have the power connector on another position. Since the direction of the current flow is strongly related to the connector, it is likely that these issues might get solved in another way.

The complete layout is available in Appendix B.

Common Point for Digital and Analog Ground

All signals must be referred to a common ground, i.e., to the same voltage potential, but our mixed-signal system has separate digital and analog ground planes. That

is why the common point is created at the power supply unit by connecting the digital and analog ground terminals with a cable (see Appendix D). This method prevents that the noisy digital signals couple into the quiet analog circuitry [36].

The common point can be created on the TC as well by linking the grounds by the power connector with a zero Ω resistor. This approach gives us the option to choose where the common point will be.

4.7 Power Consumption and Heat Dissipation

It is essential to keep in mind that not only ALPIDE chips generate heat, but voltage regulators as well due to the relatively big voltage drop over the regulator (in the range from 1 V to 1.3 V). It is, therefore, essential to calculate the heat dissipation of the regulators and handle it accordingly. This determines if the TC needs to be cooled down during operation. Moreover, this section estimates the ideal voltage drop over the power cables and the length of the power cables.

Foremost, the input voltage for the voltage regulator must be selected. The MIC29302 is a low-dropout voltage regulator with a 560 mV dropout voltage at the full load. The current setup of the voltage regulator will yield an output voltage range from 1.87 V to 1.95 V. So the possible input voltage range is:

$$\begin{aligned} V_{in_{min}} &= V_{out_{min}} + V_{DO} = 1.87\ V + 0.56\ V = 2.43\ V \\ V_{in_{req}} &= V_{out_{req}} + V_{DO} = 1.90\ V + 0.56\ V = 2.46\ V \\ V_{in_{max}} &= V_{out_{max}} + V_{DO} = 1.95\ V + 0.56\ V = 2.51\ V \end{aligned} \tag{4.15}$$

For the current application, V_{out} is required to be 1.9 V. However, none of the input voltages is reasonable since the minimum operating input voltage for this component is 3 V. So, despite the theoretical low dropout voltage, the operating input voltage needs to be 3 V, making the dropout voltage around 1.1 V. This increases the power consumption together with the heat dissipation.

Following equations show how to calculate voltage drop over the power cables between the TC and the Power Control Unit (or power supply unit), the power dissipation of the voltage regulators and the estimated junction operating temperature of the voltage regulators:

$$\begin{aligned} Cable\ voltage\ drop\ (V) &= Cable\ current\ (A) \times Cable\ resistance\ (\Omega/m) \\ &\quad \times Cable\ length\ (m) \\ V_{D_{cable}}\ (V) &= I_{cable}\ (A) \times R_{cable}\ (\Omega/m) \times l_{cable}\ (m) \end{aligned} \tag{4.16}$$

$$\begin{aligned} \textit{Power dissipation } (W) &= \textit{Current } (A) \times \textit{Voltage drop regulator } (V) \\ P_D\ (W) &= I\ (A) \times V_{D_{regulator}}\ (V) \end{aligned} \tag{4.17}$$

$$\begin{aligned} \textit{Junction operating temperature } (°C) &= \textit{Thermal resistance } (°C/W) \\ &\times \textit{Power dissipation } (W) + \textit{Ambient temperature } (°C) \\ T_J\ (°C) &= \theta_{JA}\ (°C/W) \times P_D\ (W) + T_A\ (°C) \end{aligned} \tag{4.18}$$

Table 4.4: Estimate of power consumption for power cables, Transition Cards and strings.

	IDLE STATE [a]			**DRIVE STATE** [b]		
	AVDD	DVDD	DVDD/2	AVDD	DVDD	DVDD/2 [c]
Power consumption of power cables l_{cable} **= 4.00 m (1.50 mm^2 copper cable);** R_{cable} **= 0.0133 (Ω/m)**						
I_{cable} **(A)**	1.56	1.92	0.96	2.40	10.80	5.40
$V_{D_{cable}}$ **(V)**	0.08	0.10	0.05	0.13	0.57	0.29
P_{cable} **(W)**	0.13	0.20	0.05	0.31	6.21	1.55
$P_{43\ layers}$ **(W)**	5.57	8.43	4.22	13.18	266.83	133.41
Power consumption of Transition Cards						
$I_{9\text{-chip string}}$ **(A)**	0.13	0.16	0.16	0.20	0.90	0.90
$V_{TC_{input}}$ **(V)** **(3.0-**$V_{D_{cable}}$**)**	2.92	2.90	2.95	2.87	2.43	2.73
$V_{TC_{input}}$ **(V)** **(3.3-**$V_{D_{cable}}$**)**	3.22	3.20	3.25	3.17	2.73	3.01
$V_{D_{regulator}}$ **(V)**	1.32	1.30	1.35	1.27	0.83	1.11
$P_{D_{regulator}}$ **(W)**	0.17	0.21	0.22	0.25	0.75	1.00
$P_{D_{TC}}$ **(W)**	2.04	2.52	2.00	3.05	8.96	12.00
$P_{D_{43xTC}}$ **(W)**	87.72	108.36	111.46	131.06	385.45	516.00
Power consumption of 9-chip strings						
$V_{9\text{-chip string}}$ **(V)**	1.90	1.90	1.90	1.90	1.90	1.90
$I_{9\text{-chip string}}$ **(A)**	0.13	0.16	0.16	0.20	0.90	0.90
$P_{12x\ string}$ **(W)** **(one sensor layer)**	2.96	3.65	3.65	4.56	20.52	20.52
$P_{43x\ sensor\ layer)}$ **(W)**	127.45	156.86	156.86	196.08	882.36	882.36
Operating temperature of regulators θ_{JA} **= 35.00°C/W;** $T_{J_{max}}$ **= 125.00°C**						
T_A **(°C)**	119.05	117.65	117.44	116.11	98.86	90.00

[a] Minimum current drawn by the ALPIDE chips.
[b] Maximum current drawn by the ALPIDE chips.
[c] DVDD/2 means that the power net is split in two.

It is proposed to use a 1.5 mm^2 copper cable. This type is usually used for a current of 10 A, but it can tolerate up to 18 A. This is also dependent on the voltage drop and the length of the cable. A copper 1.5 mm^2 cable has resistance of 0.0133 Ω/m. The minimal expected length of the cable is 4 m as a consequence of keeping electronics out of high radiation zone.

As seen from Table 4.4, if the DVDD power net is split in two, the biggest voltage drop will be around 0.29 V. This means that if the voltage on the Power Control Unit is kept at 3.3 V, the recommended input voltage on the voltage regulators on TC will remain intact. This is not the case when DVDD is not divided (voltage drop over cables would be 0.57 V) or when the voltage on the Power Control Unit would be maintained at 3 V. This would result in lower input voltage at voltage regulators then desirable.

The DVDD/2 + AVDD configuration will cause the power dissipation of the regulators on one Transition card to be approximately 15 W and 650 W for all 43 layers in the drive state (maximum current state). The mechanical team evaluated this as serious power dissipation and proposed a cooling system that is based on air being driven between the cards through air ducts (see Figure C.1). The table also estimates that 43 sensor layers in the DTC will consume over 1000 W. The loss in power cable will be around 150 W. This sums up to approximately 1800 W for the whole DTC with 1.9 V operating voltage, including Transition Cards and 4 m long power cables.

The last row in the table points out that if the ambient temperature on the TC near the regulators exceeds 90°C in the drive state or 117°C in the idle state, the junction temperature inside the regulators will be 125°C. This is the threshold value for the regulators, and it can cause the regulator to fail. These temperatures, therefore, represent the worst-case scenario. For this reason, a temperature sensor will be placed in the middle of the TC, where temperature accumulates the most so that the airflow can be adjusted accordingly.

In summary:

- The DVDD power line must be partitioned in two between the TC and the PCU.
- The voltage on the PCU must be set to 3.3 V.
- The temperature on TC must be monitored and must not pass 90°C.

Every modification (e.g., cable length, cable cross-section, cable resistance, the voltage on the Power Control Unit) should be reevaluated based on the calculations presented in this section.

4.8 TC V2.0

Given the reasons presented throughout this chapter, a new iteration of the TC is necessary. The list below summarizes the additional changes and requirements. Some of them were suggested as a result of the testing and verifying the TC. This is further discussed in Chapter 5. Table 4.5 gives the overview of the new components.

List of required and suggested modifications:

- TC must be extended by 25 mm on the FireFly side.
- TC must have new enable signals and temperature sensors connection.
- TC must have new power connection.
- TC must include a temperature sensor.
- TC must have connection for external temperature sensors.
- TC is considered to include common point to connect the ground nets.
- TC is considered to have open vias for all differential pairs by the ZIF connectors for easier troubleshooting.
- TC is considered to have modified FireFly connector pads (extended from 0.85 mm to 1.1 mm; explained in Chapter 5).
- TC is considered to have labeled differential pairs on one channel for easier troubleshooting.
- TC is considered to have continuous planes if possible.

Table 4.5: Reduced BOM of Transition Card V2.0 (resistors and capacitors not included).

Component	Amount	Part number
Linear Voltage Regulator	12	MIC29302AWD
FireFly connector part 1	12	UCC8-010-1-H-S-1-A
FireFly connector part 2	12	UEC5-019-1-H-D-RA-1-A
ZIF connector	12	541323633
Power connector (header)	1	1942120000
Power connector (plug)	1	1969140000
Additional connector (header)	1	M50-3501042
Additional connector (plug)	1	M50-3301042

CHAPTER 5

Testing and Verification of Transition Card

This chapter describes different tests performed on the Transition Card as well as tests that should be executed in the future. The different challenges with assembly and testing are introduced across the entire chapter but also the possible solutions to handle them. It also presents issues with the string cables discovered during testing.

5.1 Continuity Test

One of the biggest challenges is to verify that the FireFly- and ZIF-connectors are correctly soldered before connecting the strings. The continuity test is applied in this work, verifying if there is a complete current path between two points, and the following subsections indicate how this test can be performed. This is important during the commissioning. Commissioning is a systematic procedure to verify the functioning of each separate section of a project to provide hassle-free equipment installation.

5.1.1 Manual Continuity Test

An external company fabricated the first batch of the Transition Cards. The components have been mounted and soldered in-house at UiB by Bilal Hasan Qureshi[1]. The in-house assembly is preferred in the development period to save time and money. It also enables us to gain better expertise in soldering techniques.

[1]Chief Engineer at Department of Physics and Technology; Bilal.Qureshi@uib.no .

Firstly, the FireFly connectors were soldered in the vapor reflow phase oven (Asscon VP310; available at UiB). The oven benefits from boiling perfluoropolyether, which creates a vapor layer that has a higher density than air. This provides a uniform atmosphere around the PCB and the components with good and even heat transfer. This is why the vapor reflow phase oven is suitable for densely populated PCBs or components with dense footprints, i.e., FireFly connector [37]. The distance between two pads of the footprint is only 0.08 mm, and one pad is 0.42 mm wide and 0.85 mm long. A small amount of solder paste was applied on the pads, and then the FireFly connector was placed on the pads and reflowed.

Following this, the pins were examined under the microscope for potential solder bridges or cold solder joints. A solder bridge (unwanted bond between two or more pins through an excessive amount of solder) is often easy to spot under a microscope. However, it is likely to overlook a cold solder joint (not properly formed bond; see Figure 5.3). The continuity test was employed to locate the cold solder joints on FireFly connectors. Most of the digital multimeters nowadays have the continuity test mode. The advantage of this testing is that the Device Under Test (DUT) does not need to be powered. Figure 5.1 demonstrates two probes of the multimeter placed on the two points of our DUT. On the left are pads of the ZIF connector, and on the right is the end of the FireFly cable connected to the FireFly connector under test. The benefit of the FireFly cable is that it has a small PCB on each end with exposed pads. In this manner, each differential link's electrical connection is verified, and thus the soldered bond as well.

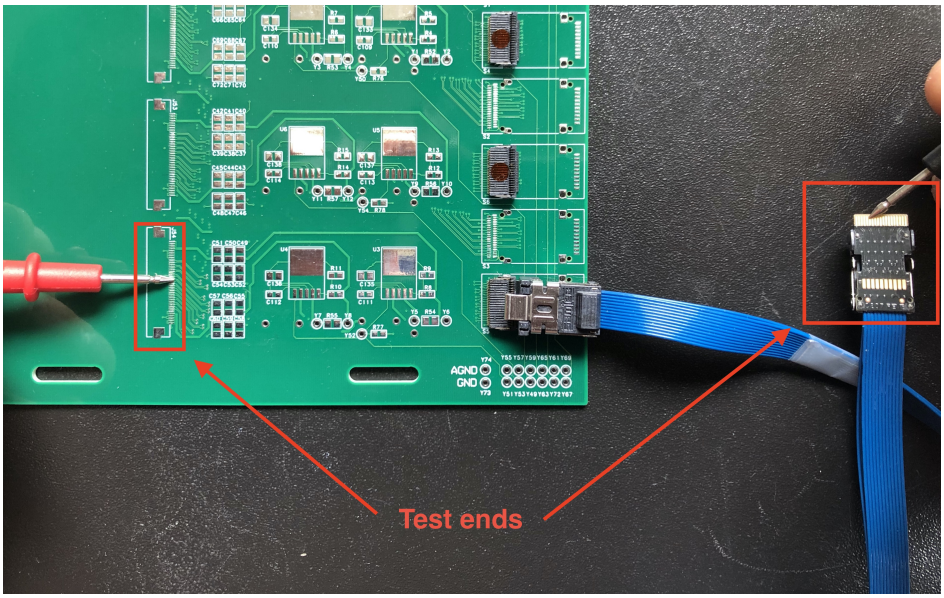


Figure 5.1: The manual continuity testing with digital multimeter.

During the first period of testing and soldering, a simple PCB was designed to serve as some sort of extension to the FireFly assembly (see Figure 5.2). The intention was

that it is easier to place probes on the extended board than on the small integrated FireFly PCB. However, this concept failed because it was even more problematic to solder the FireFly connector on the extension board properly. The PCB consisted only of the core and the copper sheet, which was milled as specified by the layout. As a consequence of densely populated pins and the absence of a soldering mask on the copper layer, the soldering paste spread to the adjacent pins creating short circuits. This was not anticipated before, and this quick prototype was dropped during testing altogether.

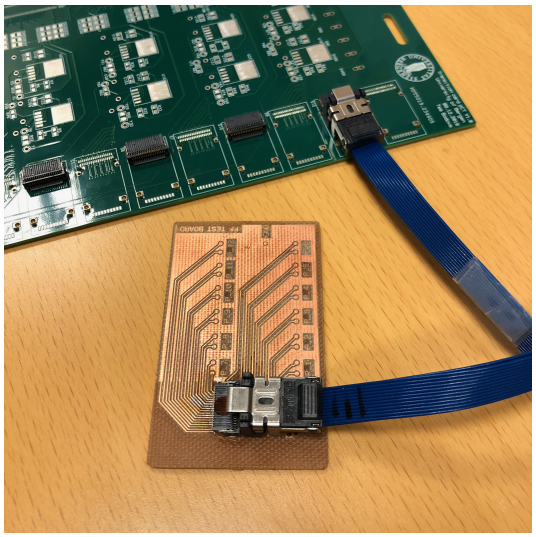


Figure 5.2: Extension board to the FireFly assembly for easier probing.

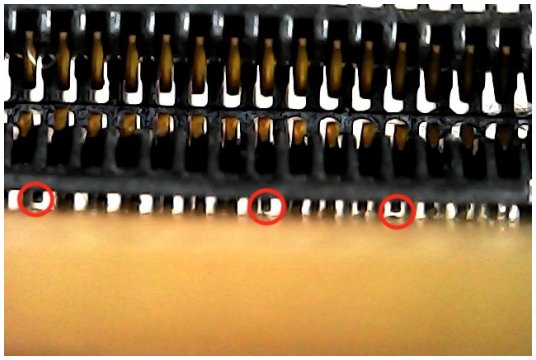


Figure 5.3: Cold solder joints.

When a cold solder joint was detected on the outer side, it was easy to repair under the microscope with the soldering iron. However, when a cold solder joint was identified on the inner side, the FireFly connector needed to be removed with the hot gun and reflowed again. This often led to destroying the connector with the hot gun. It has also been experienced that some other pins of previously working FireFly connectors got defective after the second or several reflows. Thus, the reflow machine was omitted, and the hot gun has been used for soldering the FireFly connectors. Hot gun has been proven to be as effective as the reflow machine but more time- and manpower-consuming. Figure 5.3 shows three cold solder joints inspected under a microscope. The possible cause of these cold joints may be an insufficient amount of solder paste. Luckily, the second part of the FireFly connector serves as a mechanical support and does not need to be tested (see Figure 5.4).

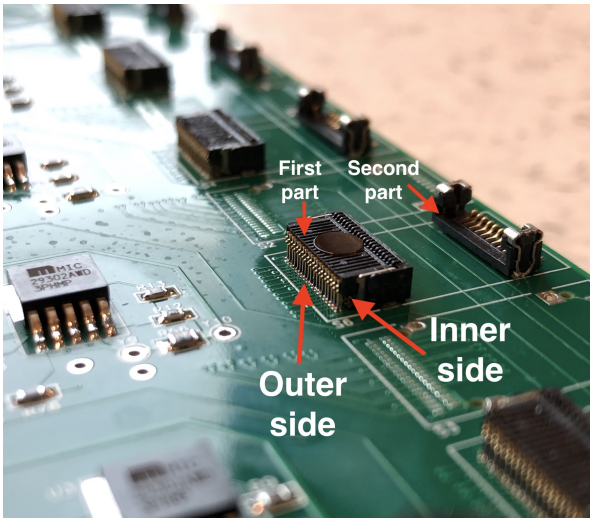


Figure 5.4: The different parts of the FireFly connector.

Once all needed FireFly connectors were verified, the rest of the components were soldered by hand. The learning outcome of soldering the connectors was that the yield of correctly soldered connectors on the first attempt is low. Therefore, two precautions have been decided. The first is to make the footprint of each FireFly connector pad longer by 30% (length of 1.1 mm) to ensure a bigger soldering area. The second is to use a stencil to apply an even layer of the solder paste onto the pads. If this will be confirmed to be effective, then the reflow oven should be considered again to save time.

Flux is used as a cleaning medium to remove oxidation from the metals whenever a component is soldered. After all components are soldered onto the board, the most important thing is to clean the connectors thoroughly. The problem occurs when there is an excessive amount of flux, and it solidifies and creates an adhesive layer on the board. Several problems can occur:

- Traces of the flex cable can stick to the flux on the board and get damaged.
- Actuator of the ZIF can get stuck.
- Pins of the FireFly can get insulated or stuck.

This means that whenever it appears that the FireFly connector does not work during testing, there may be a layer of flux on the pins. Because of this, the first step of troubleshooting should be to clean the connectors with isopropyl alcohol.

5.1.2 Semi-Automated Continuity Test

The final version of the Transition Card will be fabricated and assembled by an external company, and more than 43 ready-to-use cards need to be verified before

the final DTC assembly. There are 264 connections per Transition Card. This entails a considerable amount of work if each connection is tested with the same method as outlined in the previous section. The manual test is time-consuming, laborious, and not suitable for a large number of boards.

The semi-automated test concept shown in Figure 5.5 is based on the continuity testing with a LED used instead of a digital multimeter to check the continuity. In other words, when the LED is on, the connectors are soldered correctly. For this semi-automated test, two test boards and a FPC must be designed. The Test Board Source has one FireFly connector, where each differential pair is connected to a voltage source.

One end of the differential pair is connected to positive and negative voltage on the Test Board Source. The other end is connected to a LED on the Test Board LED. The Test Board LED needs a ZIF connector to link to the Transition Card via the Test FPC.

The Test Board Source includes the same connection for the enable signals. In this way, the signals can be connected to the ground at once, and the voltage regulators will not output any voltage.

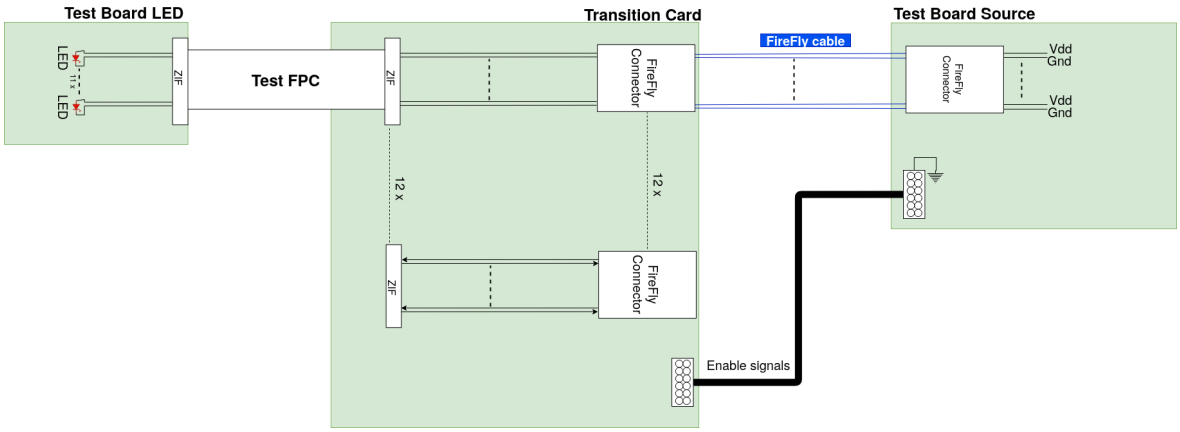


Figure 5.5: Simplified diagram of the semi-automated test.

However, if the yield of the soldered FireFly connectors is resolved, it may be considered to omit this type of testing. Nevertheless, this concept can still be used for troubleshooting.

5.2 Voltage Regulator Verification

The objective of these following tests was to verify the function of the voltage regulators under different conditions.

5.2.1 Output Voltage

After all components were successfully soldered on and verified, the TC was connected to a power supply. The input voltage was set in a range from 2.6 V to 3.3 V in 0.1 V increments, and the output voltages were measured without and with load (in this case, the load was the 9-chip string). Appendix D shows the test points available on the card.

It is expected that the input voltage will be changing during the operation because of the varying current consumption of the chips and the resulting voltage drop over the cables. Therefore, this test's purpose was to see if the regulators will still output stable voltage even when the input voltage is changing.

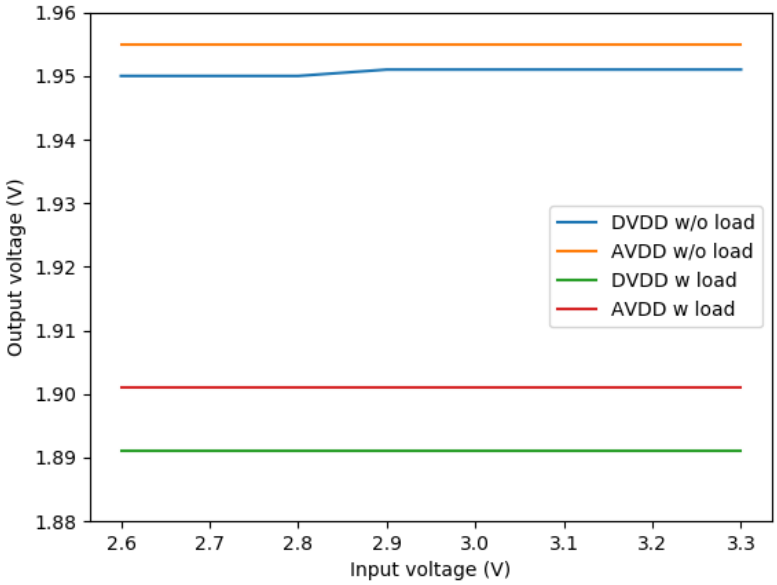


Figure 5.6: Measured output voltage on MIC29302 with varying input voltage.

Figure 5.6 gives the results of this testing on one channel with a 9-chip string. The output is steady for a wide range of voltages. Nevertheless, it is still recommended that the input voltage is 3 V (see Chapter 4). These results are essential and must be taken into consideration when choosing the power cable's length, given that there will be a voltage drop over the power cables.

When the load current is less than 10 mA, leakage currents start to dominate, and the output voltage increases [17]. This behavior is confirmed with this testing as well. The output voltage is slightly higher when no string is connected. This is not a concern but rather explains why the voltage is higher than designed for, i.e., 1.9 V.

5.2.2 Enable Signals

As described in Chapter 4, each voltage regulator has an enable pin. All pins were connected to the ground, and the output voltages were measured to confirm the correct functionality and design of the circuit. The regulators did not output any voltage or current, which means that the test was successful.

5.3 Signal Integrity Test of Differential Transmission Lines

In the interest of verifying the high-speed data signal quality on the TC, eye diagram measurements were employed on some of the differential pairs. An eye diagram visualizes the quality of the high-speed digital signal [38]. The measurements were completed with an oscilloscope and a 4 GHz differential probe.

To do that, the PRBS (Pseudorandom Binary Sequence) pattern was sent from the ALPIDE. The propagation scheme was as followed: through the flex cable, the Transition Card, a 5 m long FireFly cable, to the VCU118 Evaluation Board, where it was measured over the two AC-coupling capacitors with a differential probe and displayed on the oscilloscope as shown in Figure 5.7.

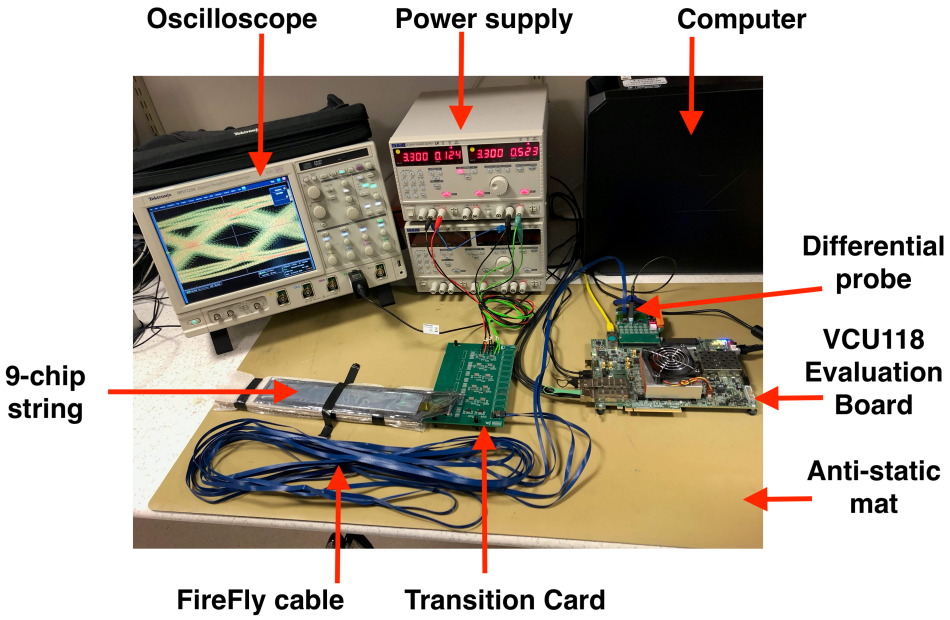
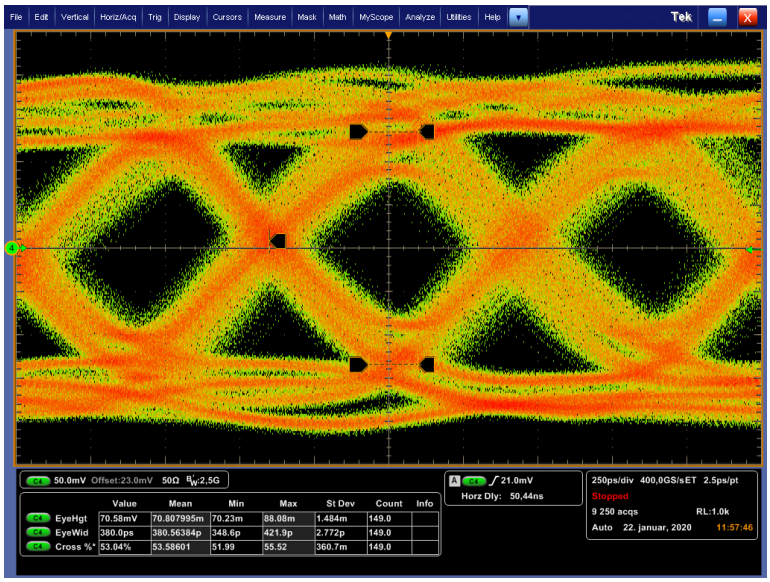
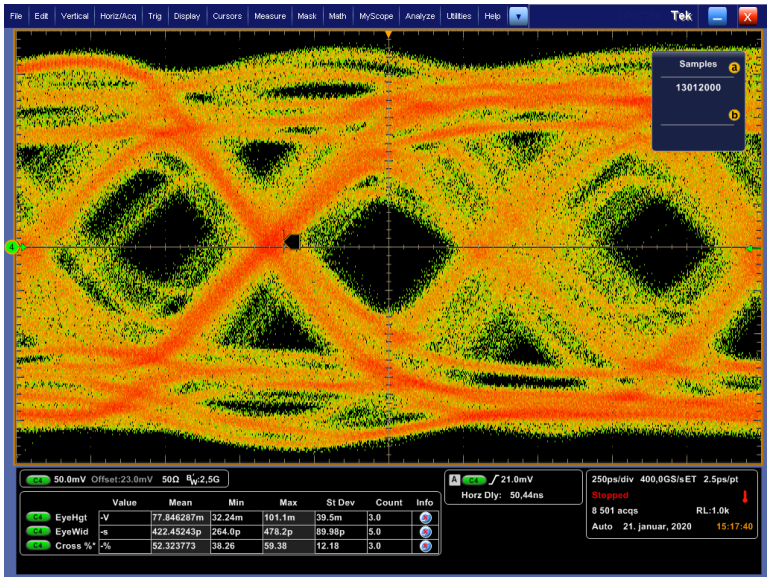


Figure 5.7: Testing setup at the laboratory.

Considering that only two strings are currently available, the TC is not fully populated with components. However, one full channel on the top and the bottom layer is populated to evaluate the signal integrity of both striplines layers.



(a) 9-chip string



(b) ITS stave

Figure 5.8: Eye diagram of the differential link attached to ALPIDE chip.

One of the eye diagram measurements is shown in Figure 5.8a. The eye diagram has good enough quality to be adequately sampled. This means that the eye diagram's width and height are big enough so that it is possible to distinguish between the digital zero and one on the signal. Similar results were obtained from the other

eye diagrams. Thereby, it is reasonable to assume that the card's signal integrity is sufficient even if the quality was not tested directly on the card but rather on the whole transmission chain.

For comparison, the 9-chip stave from ITS was tested as well. Both the 9-chip string (pCT) and the 9-chip stave (ITS) use 9 ALPIDE chips, but the layout of the flex cable is different. Moreover, the stave is directly linked with the FireFly connector, so the TC is omitted. The sampling settings of the oscilloscope were the same for both. It is evident from Figure 5.8b that there is a bigger magnitude of the noise that distorts the signal. This again reassures the assumption that the Transition Card was designed correctly.

5.4 Assembly Tools and Testing Apparatus

During this thesis, several tools and apparatus have been designed to ease the assembly and testing processes. It also presents some of the challenges experienced when handling delicate strings. Appendix C provides all detailed technical drawings and figures.

5.4.1 Holders

The first apparatus is a holder design to keep the string and the Transition Card in an upright position. In this setup, there is easy access to the passive components (terminating resistors and capacitors) on the string. It is possible to place the probes on the components to perform measurements (e.g., the voltage drop of the power lines on the flex cable). This holder was also intended to be utilized during the radiation beam test (see Section 5.6). The beam is directed horizontally along with the room. Hence, the string must be positioned perpendicular to the beam. The inconvenience with this setup is that only one string can be connected to one of the ZIF connectors at the bottom of the card. However, the advantage is that it is locked in the same position as the TC. This prevents the flex cable from accidentally bending.

The second apparatus is based on a standard vise, where one of the sides is movable by a screw with the allen bolt head (size M6). There are narrow cuts to hold the string both in the vertical and the horizontal positions on the inner sides. It is possible to use the vise for the Transition Card as well. The advantage of this type in comparison with the holder is that it is universal, and several ZIF connectors are accessible. This concept has been designed by the end of this thesis and has not been produced yet. However, it is included since it is a more flexible solution than the current holder available at the laboratory. The disadvantage with this solution is that the string is not in a locked position with the TC.

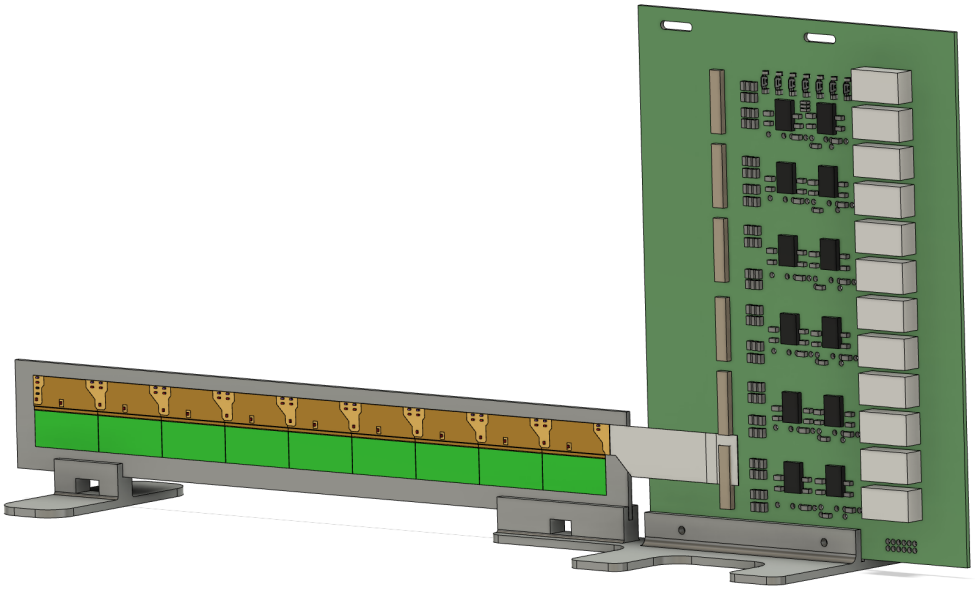
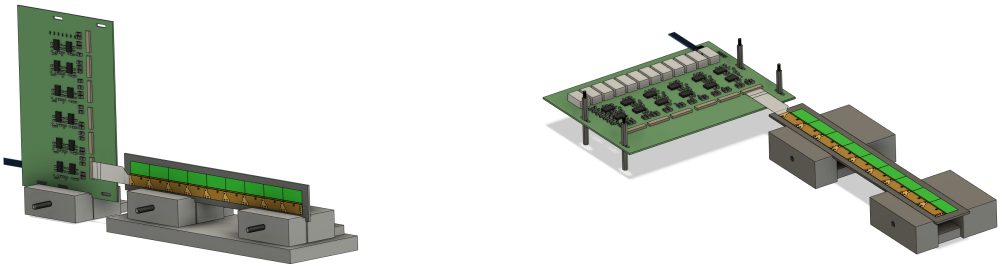


Figure 5.9: 3D design of the holder.



(a) vertical position (b) horizontal position

Figure 5.10: 3D design of the vises.

5.4.2 Tweezers

The end of the flex cable has a thin but rigid piece called the ZIF-stiffener, making it easier to insert to the ZIF connector. Usually, this is enough for effortless insertion, but only when the ZIF connector is placed at the edge of the PCB. The ZIF connector at Transition Card sits 3.5 cm from the edge (see Figure 5.11). This limitation makes the insertion and removal challenging. It is common to use a pair of metal tweezers to help with this problem. Nevertheless, the ZIF-stiffener has a smooth surface, which makes it often slip from the tweezers.

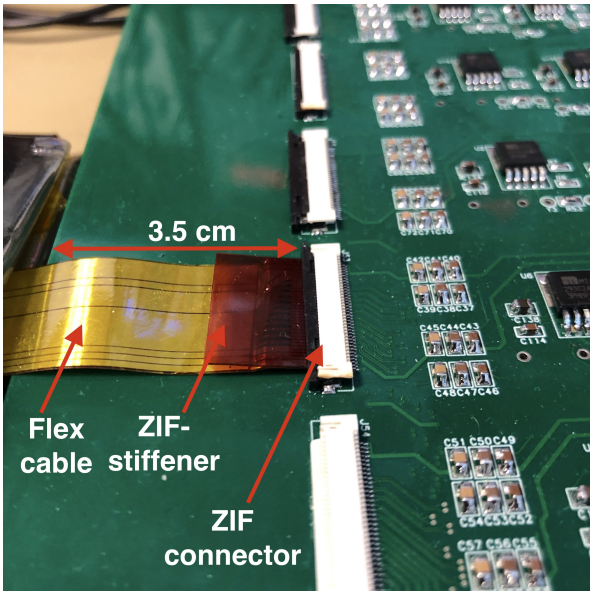


Figure 5.11: Flex cable and ZIF connector connection.

The initial idea was to create two holes into the ZIF-stiffener and a pair of tweezers with two pins to grab the stiffener easily (see Figure 5.12). The stiffener is composed of two Kaptons (polyimide films) with different thicknesses glued together to obtain the desired thickness, and it is partially glued to the flex cable (see Figure 5.13). It was advised from the flex cable's fabricator not to make holes into the stiffener as it can delaminate. Therefore a new pair of tweezers was designed where both ends are flat and have the same width as the stiffener (180 mm). For better grip, a layer of liquid tape with rubber texture (from Performix) was applied on the inner side of the tweezers. For even better grip, the ZIF-stiffener will be prolonged by 5 mm on the next string prototype. The current dimensions of the stiffener are roughly $145 \times 185 \times 0.275 - 0.295$ mm. Approximately 110 mm of the stiffener sticks out from the ZIF connector.

(a) with pins (b) flat

Figure 5.12: 3D design of tweezers.

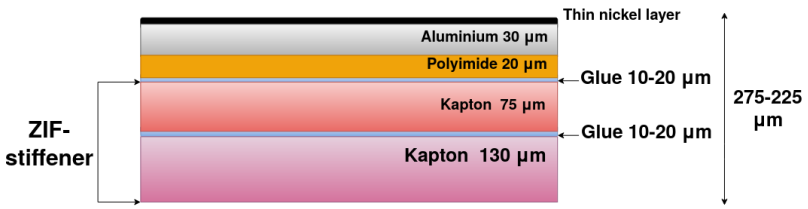


Figure 5.13: Cross-section of the flex cable end.

5.4.3 ESD Safety

An electrostatic charge is an imbalance of electrons on a surface. The charge will dissipate, and a transient current occurs when two imbalanced surfaces meet. This incident is called ESD (Electrostatic Discharge), and it is of high risk for sensitive electronics, i.e., the ALPIDE chip. According to the data sheet for the MIC29302, the voltage regulator is ESD sensitive as well [17]. The ESD can degrade or even destroy a semiconductor device. Every equipment and person that comes to contact with the chips must be either grounded or use ESD safe materials [39].

The holder and the tweezers were 3D printed with a Polylactic Acid (PLA) filament (bio-based plastic) with non-conductive properties. This material was used mainly to prove the concept and for its inexpensiveness. However, PLA material isn't ESD safe, and it represents a potential risk for the chips. Nonetheless, the cable support was 3D printed with the PLA filament since it is also intended as insulation.

There are several possible solutions to this challenge. The first is to use an ESD safe PLA filament (e.g., from 3DXSTAT™) to print out the tools. The other solution is to use the licron crystal coating (from TechSpray) that creates a conductive layer on the surface. According to both manufacturers, the materials have high surface resistivity (10^6 to 10^9 Ω), and they are static dissipative [40] [41]. In other terms, they prevent no or low charge from building up on the surface, and they should be additionally grounded for safety. The alternative possibility is to produce these tools with a CNC machine from metal (e.g., aluminium) and ground them.

Every solution mentioned above has the disadvantage that they require extra equipment to manufacture the tools. For the ESD PLA filament, any standard 3D printer can be used (one 3D printer already available at UiB). For the licron crystal coating, a spray gun and the already 3D printed tools are required. For the CNC machined tools, metal material, CNC machine, and a skilled operator are needed. For these reasons, the ESD PLA filament was considered as a good option since it has short manufacturing time and an easy manufacturing process.

The ESD PLA filament is based on a multi-wall carbon nanotube and the state of art compounding technology. The carbon nanotubes provide good electrical properties, which, when integrated with an insulating polymer (e.g., PLA), create

required surface resistivity. This compound makes a good ESD protection even in space application [42].

A simple option in the laboratory during regular testing is to utilize an air ionizer (e.g., 99110 Benchtop Air Ionizer is available in the microelectronics laboratory). This ionizer also eliminates static charge from building up on the surfaces.

5.5 String Design Remarks

Parallel to the design and production of the TC, a new design of the 9-chip string has been developed. Two strings were delivered to UiB, one with four chips and one with nine chips. Several issues have been observed during the testing.

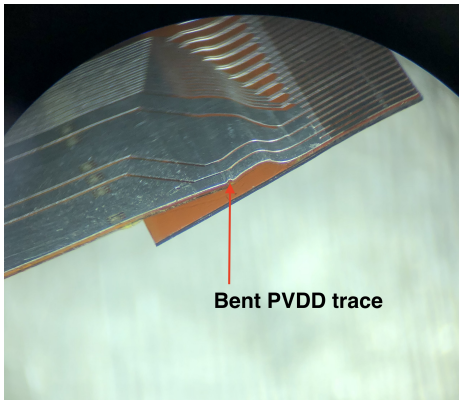
Whenever the digital or the analog voltage dropped on the power supply unit that was connected to the TC, it was usually because the contacts on the flex end were misaligned with the contacts in the connector. The flex needed to be reinserted until it was aligned correctly to solve this. Since it is the ZIF stiffener that indicates the position of contacts in the connector, it should be manufactured carefully. The data sheet for the Molex ZIF connector provides the required dimensions of the stiffener. Another update regarding making the stiffener longer has been suggested during this thesis (see Section 5.4.2).

It was also experienced that the flex cable bends on a particular location, and the thin aluminium traces can brake. This happened on both strings during testing, and they had to be repaired. When the flex was inspected under a microscope, two different polyimide thicknesses were detected, which the traces are glued to. This bending point was about 1 cm from the flex end, and precisely on this transition between the thicknesses.

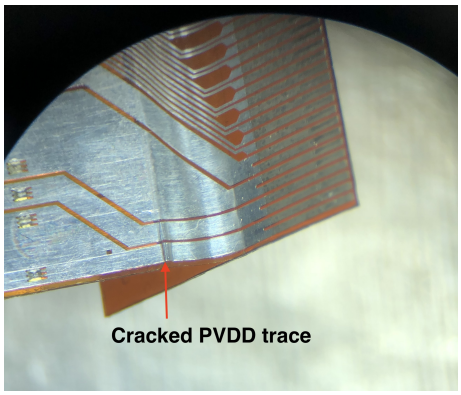
The traces are made of aluminium even though a standard FPC usually uses copper, which has better electrical and thermal conductivity and better mechanical strength. Regardless of these reasons, aluminium is preferred before copper in the pCT. It is due to several factors: aluminium is lighter, less expensive, and has high corrosion resistance. Another deciding factor is that it is easier to bond the aluminium pads on the chip with the aluminium-polyimide than with copper-polyimide cable because it requires additional nickel and gold layers [43]. Aluminium also has lower Z number than copper, which reduces the scattering and keeps the DTC homogeneous (aluminium absorbers and carriers).

Figure 5.14a shows the bent PVDD trace on the 9-chip string, the cracked PWELL and AVSS traces are not shown (on the other edge of the string). The PVDD line on the 4-chip sting is bent and cracked as well (see Figure 5.14b). It is visible from Figure 5.14c that the material on the left part of the string is different; it is thicker than the rest of the flex end. The last 1 cm of the end is thinner and thus more

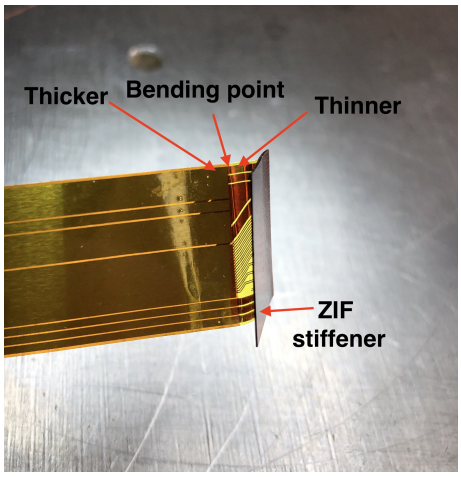
flexible. It is therefore concluded that the thin part of the flex bends more easily on the sharp edge of the thicker part, causing the aluminium traces to break.



(a) bent PVDD trace (9-chip string)



(b) bent and cracked PVDD trace (4-chip string)



(c) bending point (9-chip string)

Figure 5.14: The bending point on the flex cable.

Figure 5.15 displays the current thicknesses of the different layers in the flex cable along with suggestions on how to fix the bending issue. The first alternative purposes of making the gap between the edge and the stiffener longer. The second alternative indicates to extend the thicker 75 µm Kapton entirely to the end of the flex cable. The manufacturer did not approve of these suggestions. The first alternative was rejected because it only shifts the bending point but not solve the issue. The second alternative with the flex cable having a thicker layer of Kapton all the way is not desirable because it would be hard to align it with the ZIF connector. This is one of the reasons for the thinner layer. The other reason being to compensate for the length inaccuracy and the narrow placement of the ZIF connectors, so it is easier to handle the flex cable. It is thus concluded that the design remains the

same and more careful handling will prevent these issues.

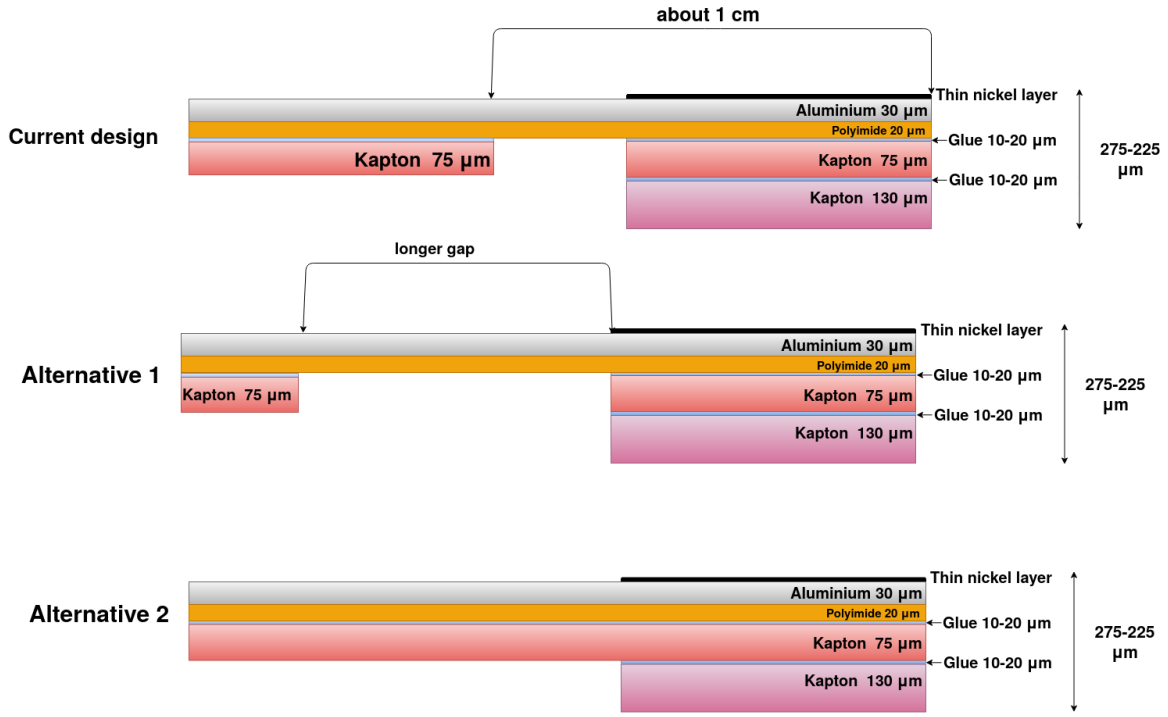


Figure 5.15: Cross-section of the current and alternative flex tail.

5.6 Radiation Test

It was planned to test the Transition Card and one 4-chip string and one 9-chip string in a beam test at DESY (German Electron Synchrotron) in April 2020. However, the tests were canceled due to the COVID-19 pandemic. Although it is documented that the voltage regulators can withstand the planned radiation, it would be interesting to see how the regulators behave when irradiated.

5.7 Remaining Tests

As for the period of this thesis, there have been only two strings available for testing. This means that the Transition Card has not been tested with a full load.

The new iteration of the card will have new updates and more functions: temperature sensors, common ground point, new FireFly connector footprint, that need to be verified and tested. Besides, this thesis also presents some changes in the string design, so there is not a final version yet. If necessary, the TC must be adjusted, and so this needs to be verified as well.

CHAPTER 6

Remote Control of Power Supply Unit

This chapter outlines another option of easing the testing process. It is separated from the previous chapter since it is software related and it explains the motivation for controlling a power supply remotely. It also gives a detailed description of the method used to achieve this.

6.1 Motivation

Over the past three years, the pCT prototype has been actively developed, the code base for automated testing of ALPIDE chips has grown quite large. One of the reasons for automation is to save time and complexity during development and quality assurance during production. Considering that the Transition Card is now part of the testing setup and is powered by a power supply, a code implementing remote control and the automated start of the power supply whenever other tests are performed is therewith in order. This also applies for when the ALPIDE chips are tested in a beam test, which radiates the chips with charged particles. In such testing conditions with radiation being present, users must avoid entering the beam room. In case of an emergency, the power supply needs to be able to be controlled and shut off remotely.

This code was later proven beneficial during the COVID-19 outbreak when universities closed down, and the pCT testing setup was controlled remotely, allowing the work on the ALPIDE chips to be continued.

6.2 Approach

As mentioned above, the approach should save time and complexity. This, in turn, needs a Graphical User Interface (GUI) that is both simple and intuitive. GUI is essentially a software application that converts command-line interfaces into graphical icons that the user can interact with. To make the software portable, the PyQt5 framework has been selected, which is also easy and fast to use in development. PyQt5 is being utilized for this goal, which is a module that helps build GUI application in Python programming language. It is a binding between Python and Qt cross-platform C++ framework. This GUI runs on Community Enterprise Operating System (CentOS) in our lab.

The power supply that the code is based on is the MX180TP Triple Output Multi-Range DC Power Supply from Aim TTi. This power supply is a switching power supply with linear final regulation. This combination is called mixed-mode regulation and gives excellent noise and transient characteristics while maintaining power efficiency. According to the technical specification from the Instruction Manual [44], all outputs have typical noise < 2 mVrms. If tests require lower noise than the values above, the QL355TP linear power supply (available in the microelectronics laboratory at UiB as well) from Aim TTi should be considered. It has almost six times lower noise, < 0.35 mVrms. The remote commands to control the power supply are the same for both models; this entails that the same code can be used in both cases.

6.2.1 Architecture

When developing software applications like this, with many different interacting components, there is a need to ease the process and make the software more flexible and robust in an already proven way. The pattern used for the desktop application that remotely controls the power control is a Model-View-Controller architecture [45]. This architecture partitions the application into three interlinked sections. The strategy is to isolate the internal commands and functions (Model) from the user (View). Figure 6.1 shows this chain of commands. The View is the user who has the right to only communicate and call functions from the Controller. The same holds for the Model, and the Controller is the interlink between these two. There is no direct connection between the View and the Model. The following subsections provide more accurate insight into these three sections.

The code is written in Python3 and is available in Appendix E or here: `https://git.app.uib.no/Tea.Bodova/production_tests/tree/powersupply/tests_ptb`

Figure 6.1: MVC architecture.

Model

The Model (power_supply.py) is the direct link to the power supply. In order to communicate with the power supply a communication protocol (e.g.USB,RS-232, GPIB) must be implemented. When using devices for measuring and testing in the industry (e.g., digital multimeters, power supplies, oscilloscopes), a Virtual Instrument Software Architecture (VISA) has been developed for communication between the instrumentation and a computer. There is already a Python package (PyVISA [46]) available for VISA communication that the Model imports to speed up the development and uses to communicate with the power supply. This introduces a dependency, and pyvisa needs to be installed (**$ pip install -U pyvisa**).

The Model builds on a class (PowerSupply) that contains various functions defined upon the remote commands from the Instruction Manual [44]. This class can read current and voltage from all three outputs of the power supply. It can set the voltage and current limit as well. Some functions can turn on or off individual outputs or all of the outputs at the same time. The read, set, and on/off commands are sufficient for this application even though there are many more available.

6.2.2 Controller

The Controller (supply_controller.py) is an interface between the View and the Model. It manages the output from the View and updates the variables for the Model.

When the user from the GUI calls the *on* function, the Controller sets the voltage to the desired value and the desired channel. A separate thread is spawned to monitor if the current on the output channel goes over the limit set by the user. The power supply has overcurrent protection, and it will decrease the voltage when the load connected to the output of the power supply starts to draw more than it is the set current limit. That is why the thread checks if the voltage is less than its set value every 2 seconds. If this occurs, the Controller turns off all outputs on the power supply. This is a safety feature that protects the tested equipment. The thread also reads and saves voltage and current readings into a queue. The central logging then reads the queue in the View.

This entire logic is run in a daemon thread. This means that while the main program (the View) runs, this task runs parallel to other threads or other processes. However, when the main program terminates, all daemon threads also abort.

6.2.3 View

The View (pt.py) is the GUI that is initiated from the terminal and controlled by the user. Figure 6.2 shows the GUI window for the power supply that the user interfaces with. The user is not allowed to turn on the power supply before the correct power supply is connected. After the connection is established through the PyVISA, the user can set the output voltage and current limit for output 1 and 2 on the power supply. The MX180TP power supply provides a third output as well. This is not covered in this setup because only two outputs are needed for the TC.

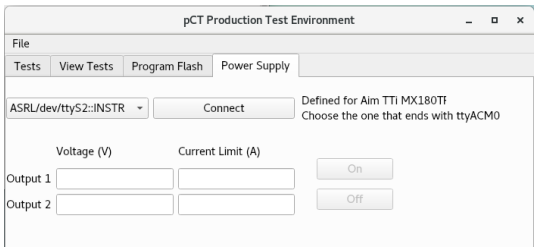


Figure 6.2: GUI window.

6.2.4 Code Verification

In software development, it is a good practice to write an additional code that tests it. Unit tests are used in the Python environment where these tests help verify if the code works as intended. The unit test examines one section of the code independently from the rest of the code. Given that all commands used in the code can actually be observed on the power supply, unit testing was not required in this application.

A simple test to verify the over-current thread was carried out before using the code with the Transition Card and ALPIDE chips. The power supply's voltage output was set to 5 V, and the current limit was set to 0.040 A. After that, a 150 Ω through-hole resistor was connected to the output drawing 0.033 A. When the resistor was switched to a 100 Ω resistor, the current consumption increased to 0.050 A forcing the power supply to drop the voltage. The thread detected this change and all outputs on the power supply were turned off.

CHAPTER 7

Power Control Unit and Equipment Protection System

This chapter describes the different elements of the pCT prototype that help to control and monitor the power and temperature. Moreover, the chapter introduces how the equipment can be protected from technical failures.

The first element is the Power Control Unit board. It can be employed as a main switch, as well as it can monitor the temperature and power consumption of the DTC. The readings are then forwarded to the Central Control Room for evaluation. It is possible that several PCUs are needed due to multiple layers in the DTC. The second element is the Equipment Protection System that will shut off the DTC during critical conditions as high temperature and current leakage. It is desirable that this system is independent of the pCT Electronics System, and powered by the Uninterruptible Power Supply.

7.1 Power Control Unit

This section presents the requirements and suggestions for the Power Control Unit design that can monitor and control power, as well as measure the temperature of the detector. The reason why the PCU monitors the temperature as well is because of the convenience. In the interest of simplifying the system, the enable signals from voltage regulators of the TC and the temperature signals are routed through one connector and one cable. It is then evident that it is easier when they are connected and processed by the same unit, i.e. PCU.

Figure 7.1 shows the diagram of the TC (based on the V2.0) and the PCU. The four main components of the PCU are a processor, power control and monitoring, PWELL regulation and resistance-to-voltage conversion. The processor controls the

other three components, processes data and sends it further to the Central Control Room via Ethernet protocol. The resistance-to-voltage component converts the resistance to voltage of the temperature sensors positioned on the aluminium carriers and on the TC. The PWELL regulation will control the voltage in the negative domain for the PWELL net of the ALPIDE chip. The power control and monitoring circuitry is in charge of monitoring the power of the analog and digital domain of the chips. It can also regulate if the power delivered to the TC is on or off.

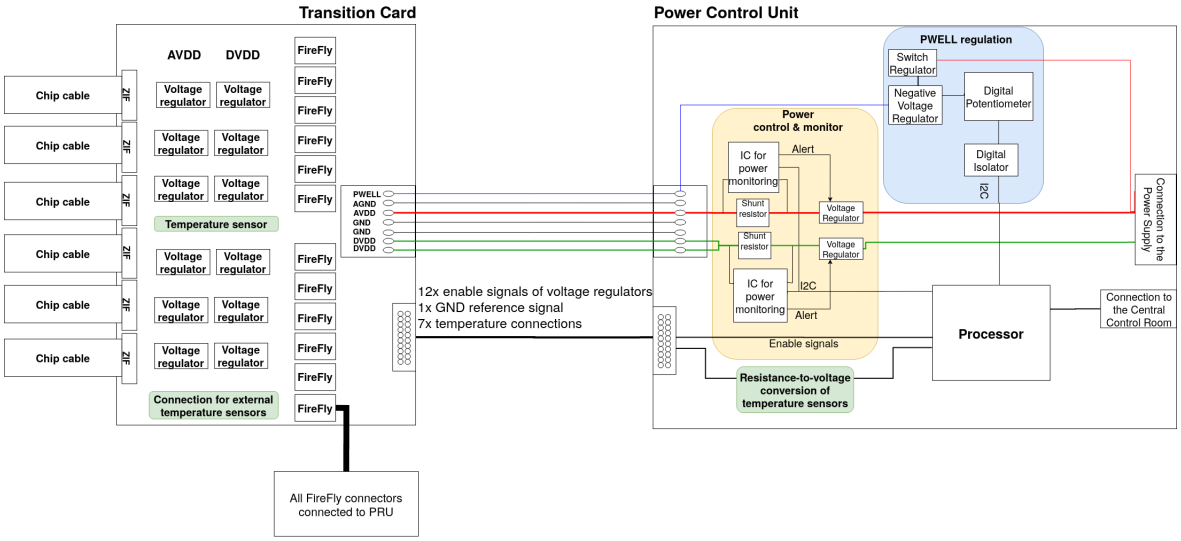


Figure 7.1: Transition Card and Power Control Unit diagram.

7.1.1 Requirements

The initial requirements for the PCU are listed below:

1. PCU must control PWELL voltage in the range from 0 to minus 6 V.
2. PCU must monitor, control and deliver power to the TC.
3. PCU must read out the temperature of the TC and the external sensors.
4. PCU must communicate with the Central Control Room via the Ethernet protocol.
5. PCU must handle 12× enable signals, 2× temperature and 1× ground reference signal per TC.

7.1.2 Design Proposal

This section contains design suggestions on the various elements of the PCU considering the requirements.

Power Control and Monitoring Circuit

One part of the circuitry is intended to monitor the power supply lines per TC. INA226 from Texas Instruments can sense the power supply voltages over a shunt resistor, and can report the drawn current, voltage and power. It is compatible with the I2C communication interface [47].

The second part of the circuit will control the power distribution. There are two possible methods how to achieve this. The processor will manage the enable signals to the voltage regulators on the TC. In other words, it can switch on and off each individual set of regulators (one regulator controls the DVVD line and the other the AVDD of one string) as required. The other method is to use two additional voltage regulators on the PCU that will manage the DVDD and AVDD power lines. INA226 has an alert pin that is asserted when the voltage or the power is under or over a certain programmed threshold. Thereby, the INA226 can shut off the power distribution for the whole TC before the processor receives and evaluates the data from INA226. This can be valuable as a safety system feature. The alert can be of course linked directly to the processor as well.

The reason for monitoring DVDD and AVDD seperatly is because they don't behave similarly. The AVDD is generally very stable. On the other hand, DVDD changes according to what operation are the ALPIDE chips performing.

PWELL Regulation Circuit

The PWELL substrate net is currently connected to the AVSS ground net via an 0 Ω resistor on the TC.

It is desirable to control the voltage of the PWELL which in return regulates the threshold of the sensing diode in the ALPIDE [16]. The voltage regulation must be adjustable from 0 to minus 6 V. It is clear that there must be a switch voltage regulator that would first shift from positive to negative voltage domain. The negative voltage regulator can then regulate this voltage to the required negative value. As on the TC, the output voltage is set by a pair of external resistors. The digital potentiometer can be used to have the ability to change the values of the resistance, and thus changing the output voltage. The suggested potentiometer supports I2C communication interface. Because these components are in the negative domain they must be isolated from the rest of the circuit. For this a digital isolater can be used with the same type of communication protocol.

The PWELL doesn't draw much power and for that the PCUs can be connected in the daisy chain scheme. This way, one pRU will regulate the PWELL net of several detector layers.

Processor

The initial idea was to use the MSP432E401Y microcontroller mostly because of the integrated PHY and MAC Ethernet connectivity. This was on of the requirements

since the communication between pRU and the Central Control Room is built on the same principle. However, there is a workable solution available (the PTB board used during testing the ALPIDE chips) that incorporates the INA226 and a MPSoC module from Xilinx integrating Zynq UltraScale+ FPGA. For this, the possibility to use this module needs to be considered.

Temperature Readout Circuit

It has been decided that the temperature sensors used will be of the RTD (Resistance Temperature Detector) type, i.e. either a Negative Temperature Coefficient thermistor or a PT100 (platinum sensor that has 100 Ω at 0°C). With this type of sensors, the resistance changes according to the temperature.

The resistance must be, however, first converted into voltage, and then processed by the processor. There are several options how to preform this. One can use an Operational Amplifier that will sense the change in resistance, and the output voltage will change accordingly. One can also use an IC (e.g. MAX31865) that converts the resistance into a digital value, and sends it to the processor. The MAX31865 RTD-to-digital converter is compatible with the SPI communication interface, and is optimized for platinum RTD [48].

Others

The PCU needs several connections. The first is for the enable and temperature signals, which can be the same as used on the TC (see Section 4.5.4). The PCU needs also connection to the power supply unit. This can be kept simple with a standard power connector. It is required that the connection between the PCU and the Central Control Room is realized via the Ethernet protocol, and for that the Ethernet connector and cable is needed.

7.2 Equipment Protection System

The pCT prototype will be used to confirm the proof of concept. This is why no patients will be screened during testing of the prototype. The only safety features employed must regard the equipment. These types of safety systems are usually complex and require a lot of analysis. A standard list of the different process steps can be divided into three main phases [49]:

1. Risk analysis.
2. Design and implementation.
3. Operation and maintenance.

Once the risks operating the pCT are analyzed, the safety system to protect the equipment can be designed and verified. It must be also estimated what type of maintenance the prototype needs and how often it must be performed.

Figure 7.2 shows the power distribution chain in the pCT where high current power supply units will power several detector layers. The fuse box then contains several Residual-Current Circuit Breaker with Overcurrent Protection (RCBO) that protect PCU, TC and lastly the ALPIDEs.

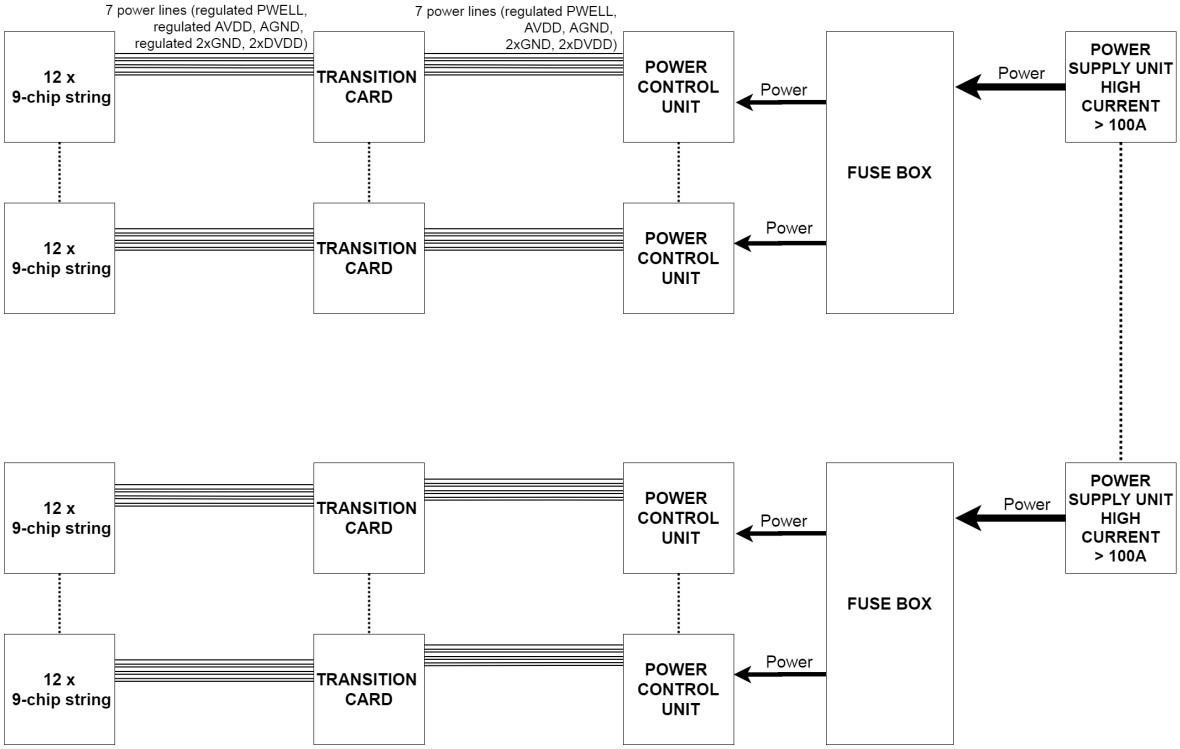


Figure 7.2: Power distribution chain scheme.

The RCBO, often called only circuit breaker, has two safety features. The first is monitoring of the current going out and in of the RCBO. If the difference is more than 300 mA (the threshold can be lower in better RCBO; 50 mA), it means that current is leaking into some other parts of the system, and the RCBO breaks the circuit. This protects people as well if the current starts to leak outside beyond the detector. The second safety feature is monitoring of current consumption. If the system suddenly draws more current than it should, it will again break the circuit. This happens when the circuit is in overload due to many connected devices. This isn't an issue when the power consumption is analyzed correctly because no additional equipment will be connected to the detector once it is assembled. These circuit breakers prevent possible overheating of cables and damaging the detector or other part of the system.

Another concern regarding equipment protection is the temperature of the detector. If the cooling systems fail or there is other cause of overheating, it needs to be detected as quick as possible. It is planned that the TC V2.0 will have a temperature sensor placed in the middle of the card on one side. The same type of the

temperature sensor will be then located on one of the aluminium carriers. Both temperatures will be processed and readout by the PCU. The PCU will then send warnings and status to the Central Room, and it can be programmed to shut down the layer if temperatures reach critical values.

It is discussed that there will be an external back-up safety system that will monitor the temperature in case some of the PCUs stop working and it won't be noticed by the Central Control Room. However, the room can communicate with the PCU and ALPIDE chips consistently. This means that a non-working PCU can be detected in this fashion, i.e. when the Central Control Room isn't getting signal from the PCU. It is up to the operator of the detector to determine what to do next. There should be always a main manual switch that would shut down the whole system immediately. This emergency switch can be located prior to all the high current power supplies. On the other hand, it is easy to overlook a failed unit in such a complex system.

CHAPTER 8

Conclusion and Future Work

8.1 Summary

The primary objective has been to design the power distribution to the ALPIDE chips and a reliable transfer of data, control, and clock signals between the chips and the pRU. For this purpose, the TC was developed and produced. The signal quality has been maintained by designing a multilayer PCB with impedance controlled differential transmission lines. Consequently, particular design rules were followed to achieve good signal integrity.

The card delivers stable power to twelve 9-chip strings. There are two low-dropout voltage regulators for each string. The MIC29302 regulator can deliver up to 3 A and the desired voltage of 1.9 V. The power circuitry has been laid out in a way that the power to each string can be switched on or off as desired. It has been estimated that 43$\times$ detector layers will consume about 1000 W, 43$\times$ TCs about 650 W, and the power cables about 150 W in the current setup. The total power consumption of the DTC sums up to approximately 1800 W. This work also evaluates the power delivery system to TCs, such as the length and the cross-section of the power cables, and the voltage required in the interest of properly working regulators.

When choosing the components for the card, it was taken into account that the TC will be positioned in the high radiation zone (dose of 10^{-4} rad/s). The only radiation sensitive component on the card is the voltage regulator. Therefore, the MIC29302 has been selected that has been previously used in the ALICE experiment, and it was tested to withstand the TID of 10 krad. This yields that the voltage regulators are reliable up to 410 000 scans, which is significantly more than necessary.

Over the testing period, several solutions were developed for easing the testing and the assembly processes. For example, different apparatus was designed and

3D printed with ESD safe material. One component of these solutions is a Python code that can control remotely most of the Aim TTi power supply units (but based on MX180TP). This power supply unit is employed to provide power to a single TC during testing in the laboratory or the beam tests.

Along with designing the TC, the requirements for a control system were gathered and specified as outlined in Chapter 7. Chapter 7.2, on the other hand, describes a potential safety system that should be applied when operating the DTC.

A few elements, such as the spacers that hold the TC and the cable rack, were added to the DTC. This was anticipated, and it did not pose enormous challenges for the mechanical team.

8.2 Future Work

The tests of the TC have not revealed any functional error, and the signal quality is acceptable. Nevertheless, there is a need for an iteration of the TC. The next version will include a temperature sensor on the card and the option to connect external temperature sensors to the card. Due to this and some additional modifications in the DTC design, the power and enable-temperature signals connection has to be changed.

One of the biggest challenges has been to correctly and quickly solder the FireFly connector in-house. The reason for in-house assembly is to save time and cost during the development phase. The FireFly assembly connects the TC and the pRU. However, the connector has a high pin density, and it was not easy to mount it on the PCB. This work suggests to redesign the pads on the PCB and to apply even layer of the solder paste using a stencil.

All aforementioned changes are necessary, and they should be included while re-designing the TC. Section 4.8 sums up these changes along with some less critical adjustments to the card that can improve it.

This work also presents findings of some critical issues with the flexible cable, which links the ALPIDE chips and the TC. The flexible cable is very delicate, and it must be handled accordingly. A simple tool was designed and manufactured to help with inserting and removing the cable in and from the TC. This tool has been tested to some degree. Still, the manufacturer of the flexible cables will provide some test cables, i.e., no mounted chips, so that this installation method can be verified.

The remaining work includes the power control unit that needs to monitor and control the power and the temperature of each layer in the DTC. It is also necessary to decide if this unit will serve as a safety system or if there is a need for an independent one.

8.3 Conclusion

This thesis covers various subjects regarding the pCT prototype. Even though the TC V1.0 isn't the definitive version, it is fully functional and reliable to use during the remaining development period. Besides, the changes required for the next iteration are properly documented.

In conclusion, the work gives solutions and suggestions on improving several aspects of the testing and installation procedures. It also clearly states the obstacles when handling the fragile electronics applied in this project and how to avoid them.

Appendices

APPENDIX A

Transition Card V1.0 Schematics

This appendix presents the schematics of the TC V1.0. Full schematics are available here \\felles3\ift-kjernefys1\pCT\TC. Schematics were done in Designer VX.2.4 from Mentor Graphics.

The schematics are divided into blocks which are later reused. This is applied for FireFly connector, voltage regulators and ZIF connector schematics.

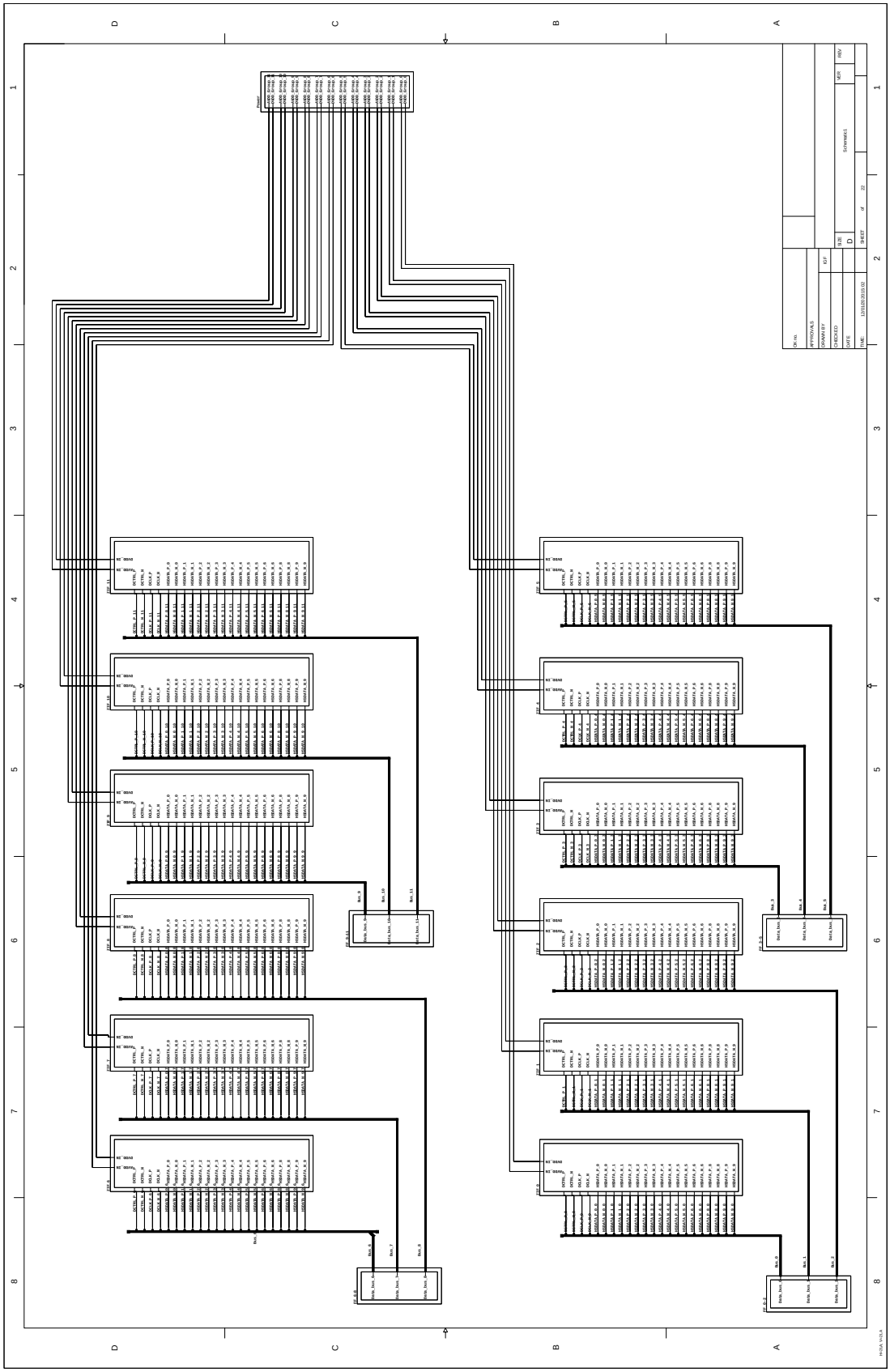
The first page of the schematics shows how all ZIF and FireFly connectors are connected as well as the regulated power (AVDD_Group and DVDD_Group) coming out of voltage regulators into the ZIF connectors.

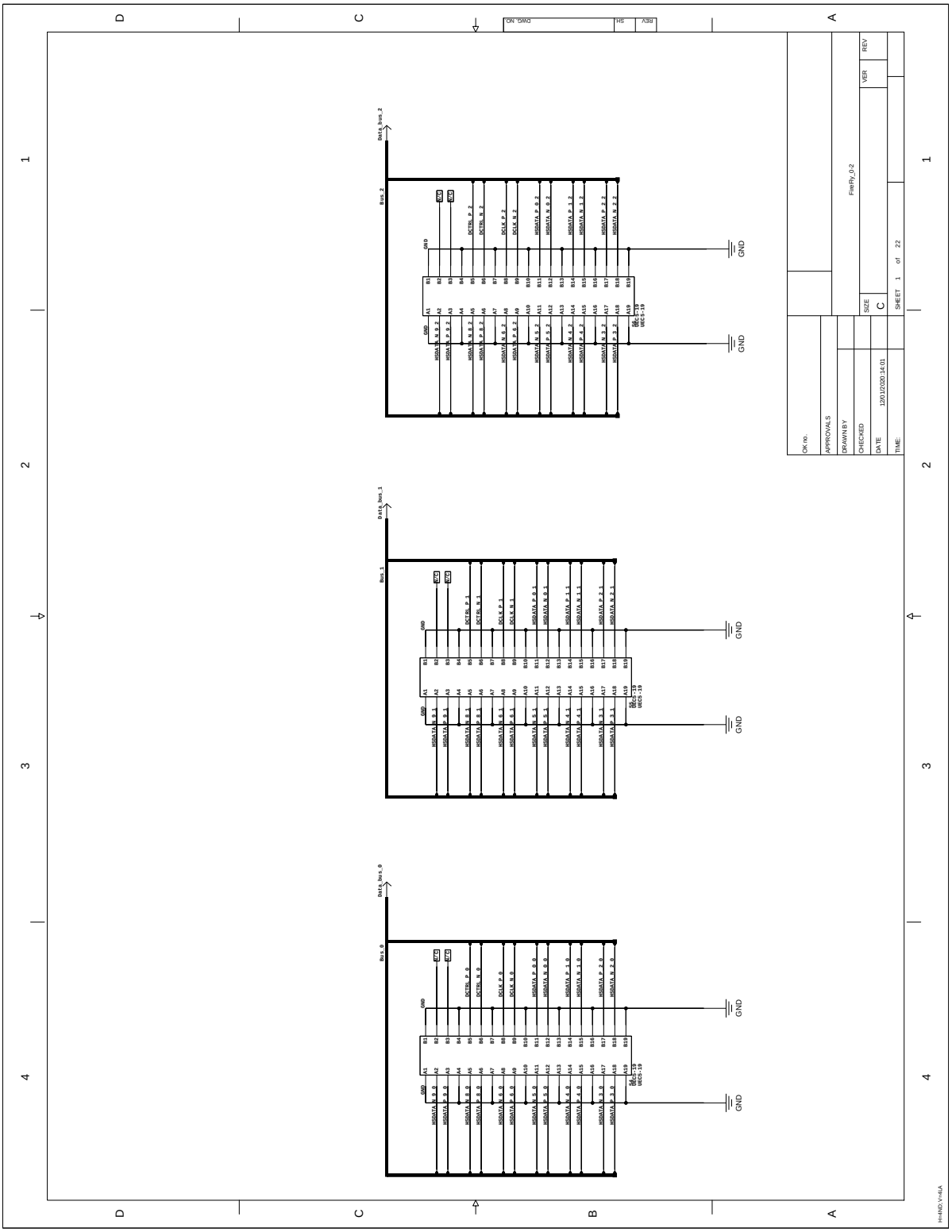
The second page shows pinout for 3 separate FireFly connectors. This is block is then reused 4 times to cover all 12 FireFly connectors.

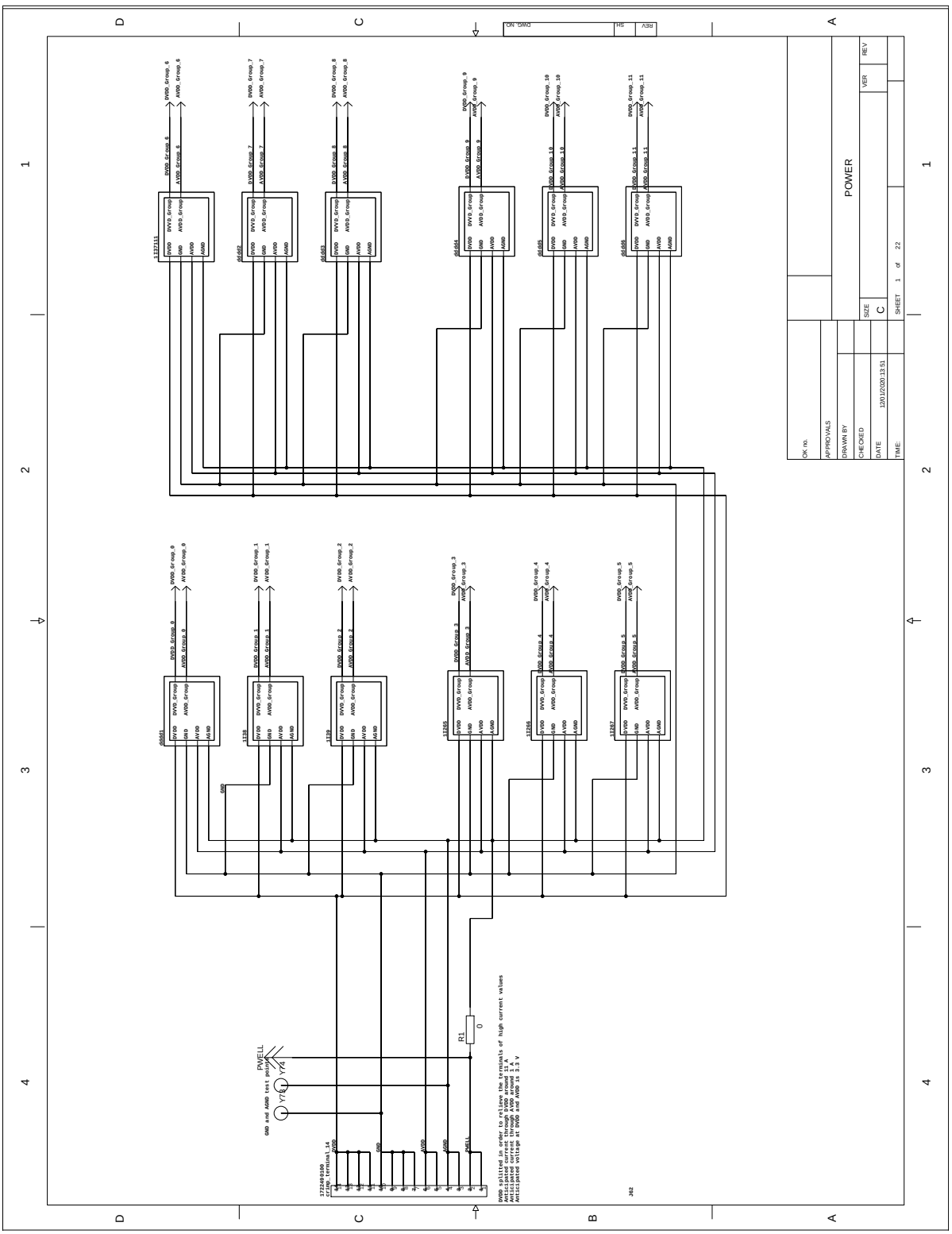
The third page shows the power distribution on the TC. The power (AVDD and DVDD) coming from the power connector (crimp terminals in this case) into voltage regulator blocks and then regulated power going out.

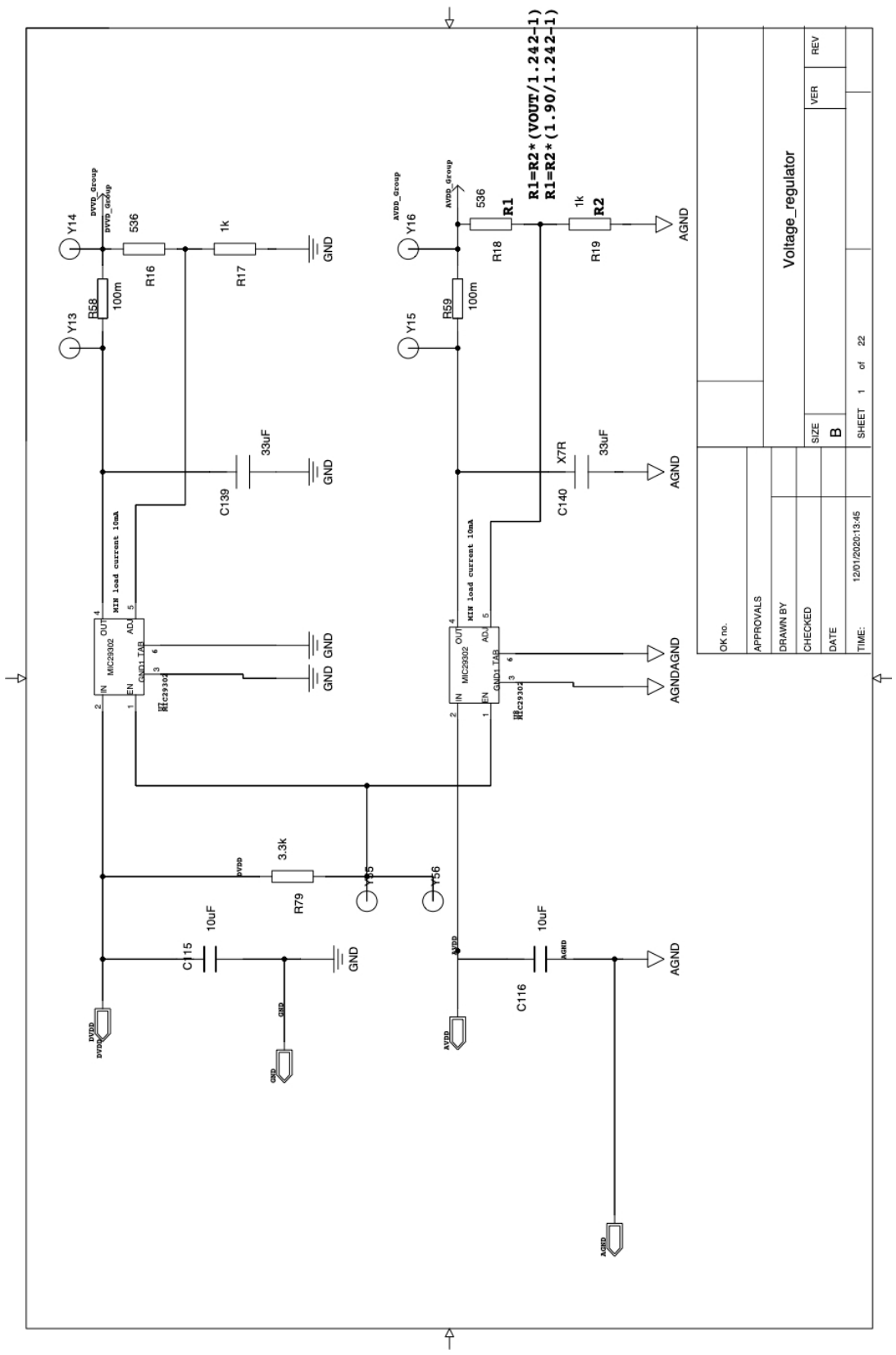
The fourth page shows the schematics for the voltage regulator block. This is later reused 12 times.

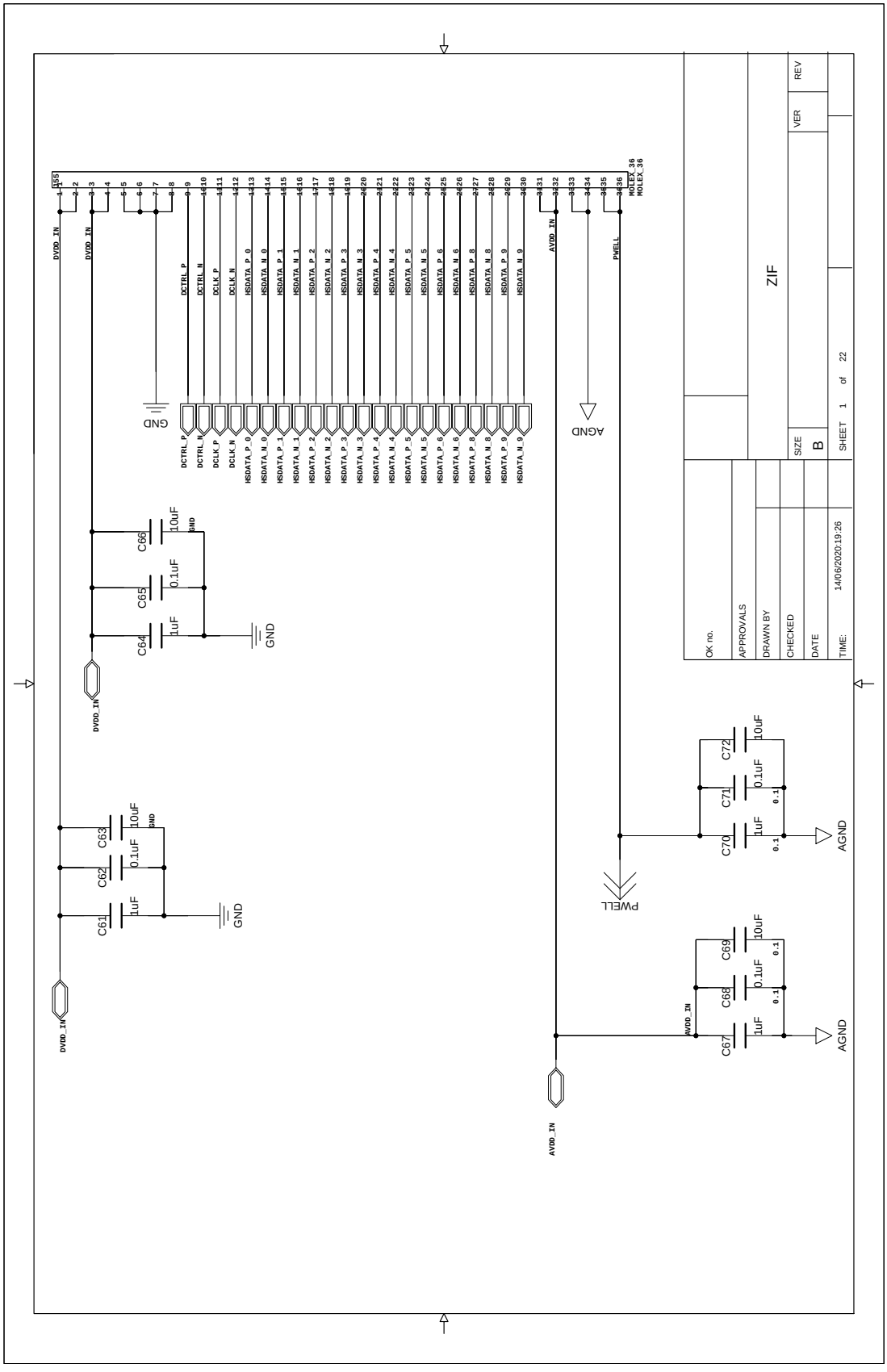
The last page shows pinout of the ZIF connector. This is later reused 12 times.




FireFly_0-2
SHEET 1 of 22
GND
Data_bus_2
Data_bus_1
Data_bus_0


POWER
SIZE
C
SHEET 1 of 22
DRAWN BY
CHECKED
DATE
TIME:
APPROVALS
DWG NO
REV
PWELL
R1
0
DVDD splitted in order to relave the terminals of high current values
Anticipated current through DVDD around 11 A
Anticipated current through AVDD around 4 A
Anticipated voltage at DVDD and AVDD is 3.3 v


R1=R2*(VOUT/1.242-1)
R1=R2*(1.90/1.242-1)
Voltage_regulator
SIZE
B
VER
REV
SHEET 1 of 22
TIME: 12/01/2020:13:45
DATE
CHECKED
DRAWN BY
APPROVALS
OK no.
DVDD_Group
AVDD_Group
Y14
Y13
Y15
Y16
536
100m
1k
R16
R17
R58
R59
R18
R19
R1
R2
GND
AGND
33uF
C139
C140
X7R
MIC29302
MIN load current 10mA
OUT
ADJ
GND1_TAB
IN
EN
AGNDAGND
3.3k
R79
Y55
Y56
10uF
C115
C116
DVDD
AVDD
AGND


ZIF
SIZE
B
REV
VER
SHEET 1 of 22
TIME: 14/06/2020:19:26
DATE
CHECKED
DRAWN BY
APPROVALS
OK no.
MOLEX_36
MOLEX_36
DVDD_IN
DVDD_IN
DCTRL_P
DCTRL_N
DCLK_P
DCLK_N
HSDATA_P_0
HSDATA_N_0
HSDATA_P_1
HSDATA_N_1
HSDATA_P_2
HSDATA_N_2
HSDATA_P_3
HSDATA_N_3
HSDATA_P_4
HSDATA_N_4
HSDATA_P_5
HSDATA_N_5
HSDATA_P_6
HSDATA_N_6
HSDATA_P_8
HSDATA_N_8
HSDATA_P_9
HSDATA_N_9
AVDD_IN
PWELL
GND
AGND
C61
C62
C63
C64
C65
C66
C67
C68
C69
C70
C71
C72
1uF
0.1uF
10uF
0.1
DVDD_IN
AVDD_IN

APPENDIX B

Transition Card V1.0 Layout

This appendix presents the layout of the TC V1.0.

Full layout is available here `\\felles3\ift-kjernefys1\pCT\TC`.

Schematics were done in Layout VX.2.4 from Mentor Graphics.

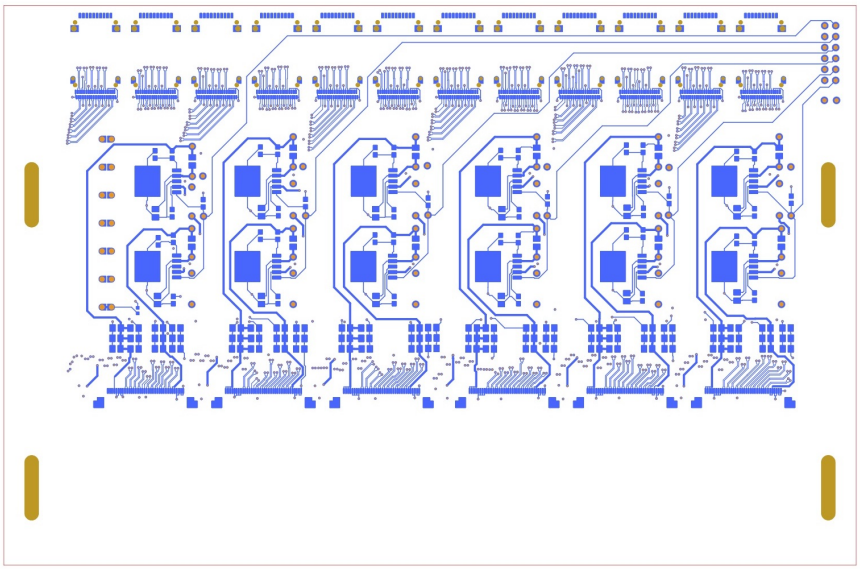


Figure B.1: Layer 1, Top.

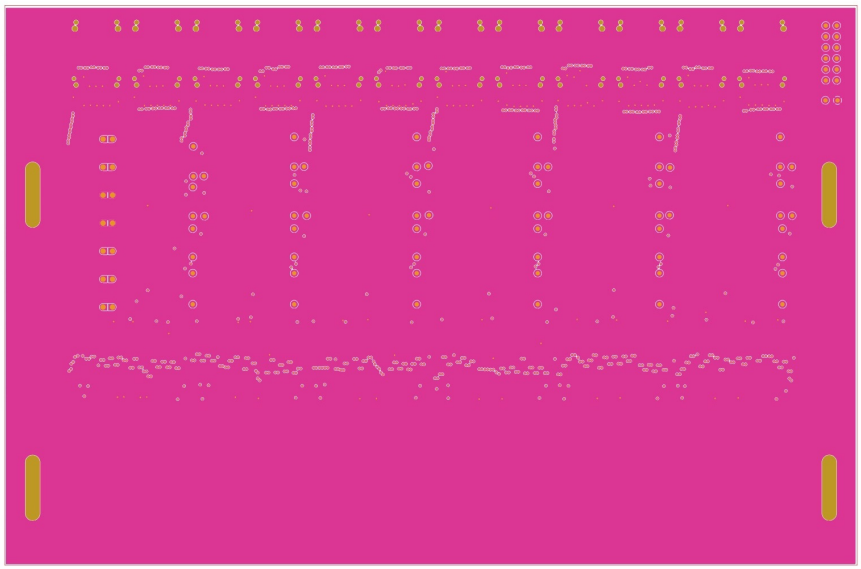


Figure B.2: Layer 2, GND.

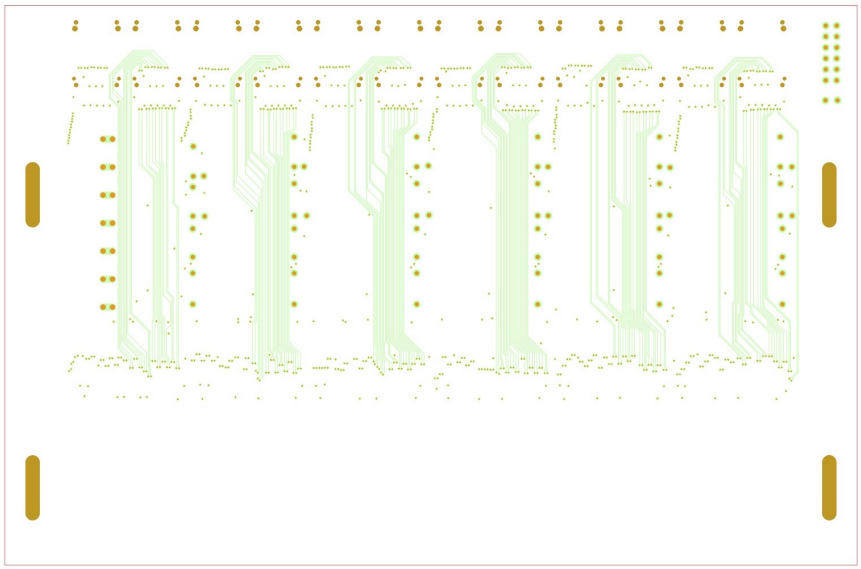


Figure B.3: Layer 3, Striplines.

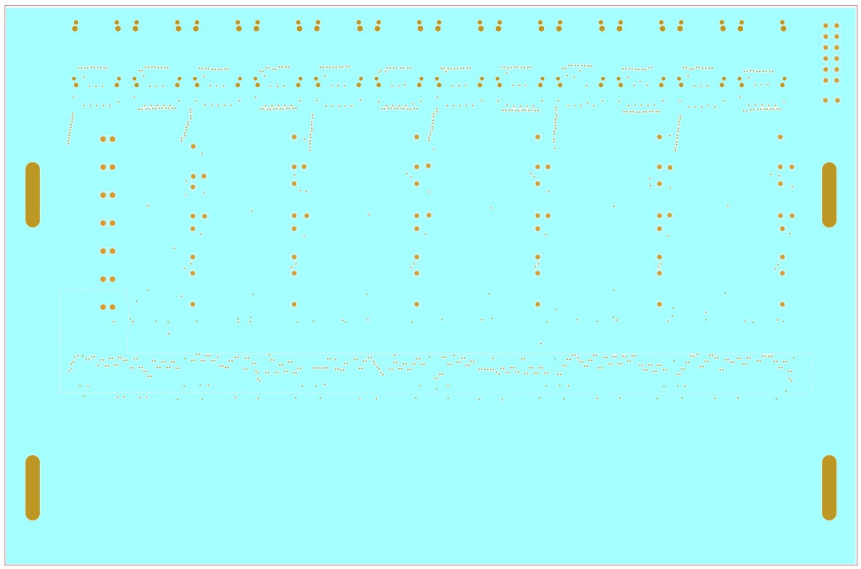


Figure B.4: Layer 4, AGND + PWELL.

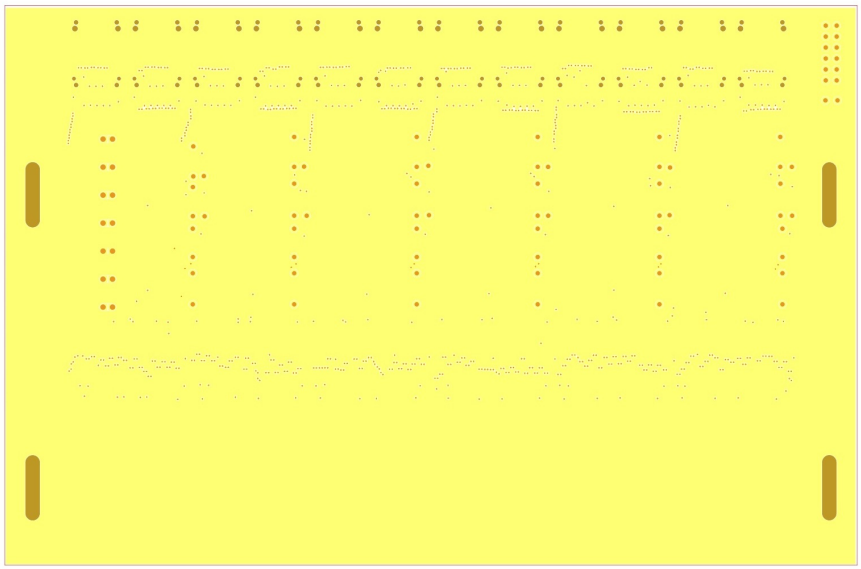


Figure B.5: Layer 5, AVDD.

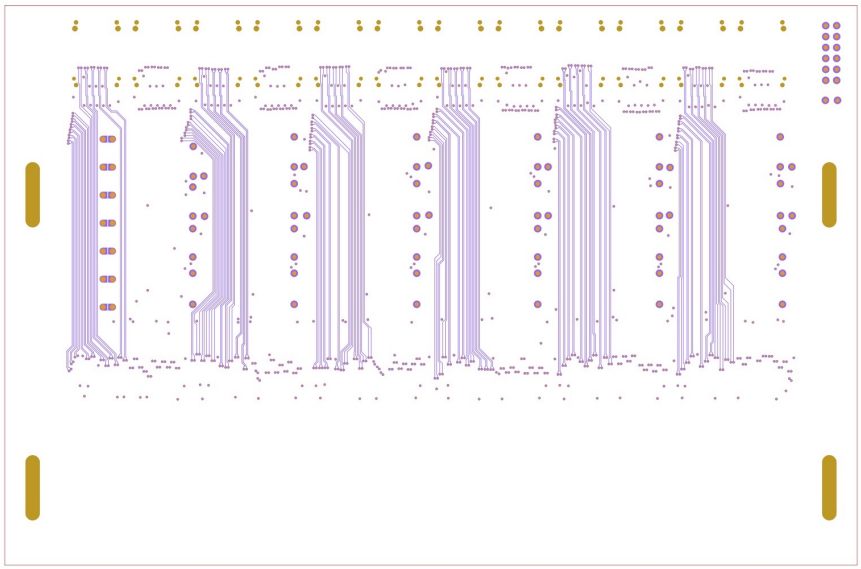


Figure B.6: Layer 6, Striplines.

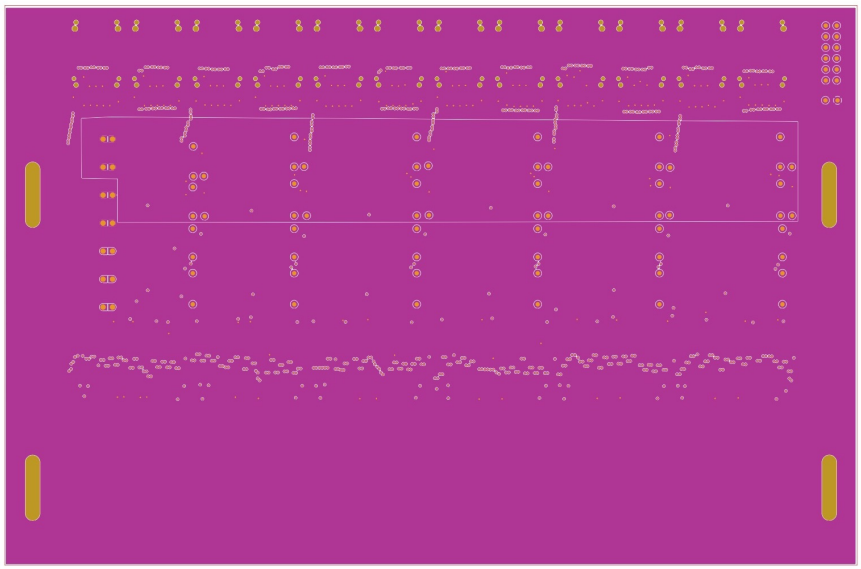


Figure B.7: Layer 7, GND + DVDD.

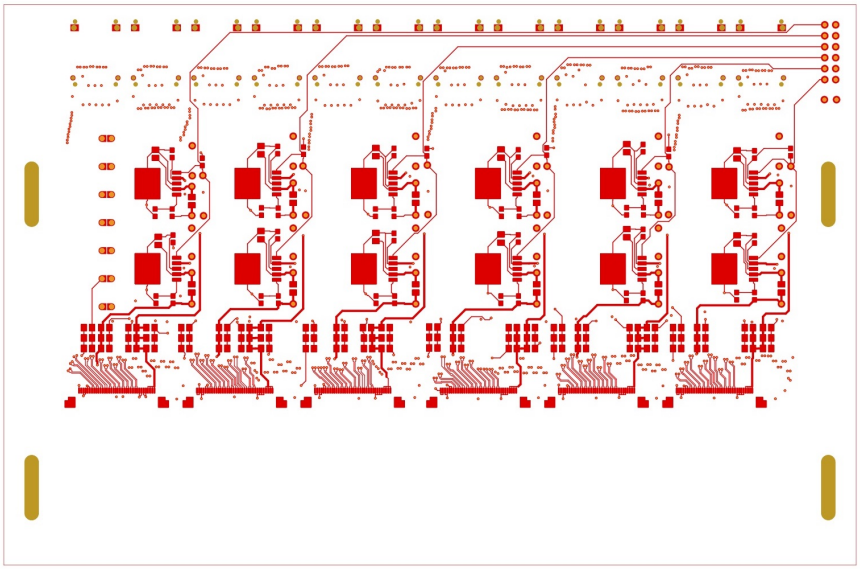


Figure B.8: Layer 8, Bottom.

APPENDIX C

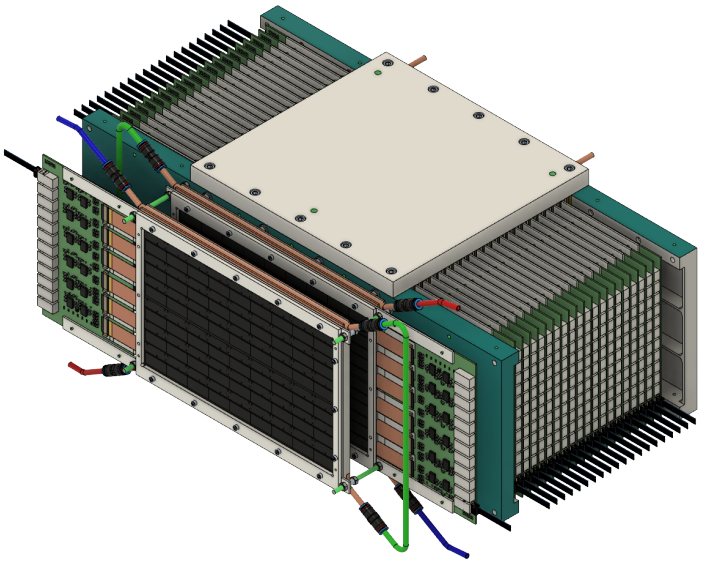
Technical Drawings and Figures

This appendix contains some additional figures of the detector that were not directly needed to introduce in the main text of this thesis. They are included for better understanding how the whole structure of DTC looks like. The 3D design of the detector was made by Anthony van den Brink (a.vandenbrink@uu.nl) in Solid Edge.

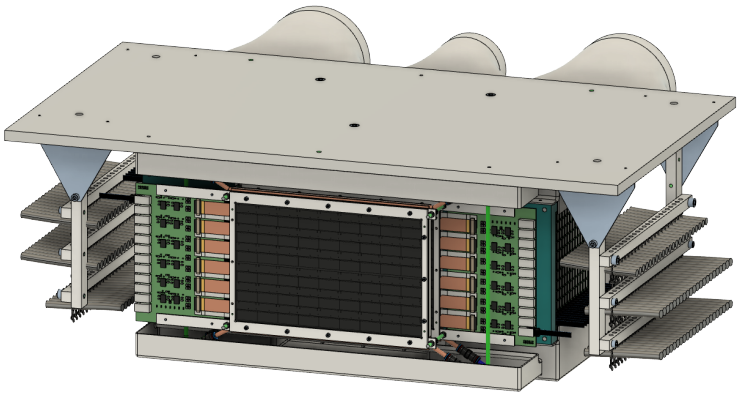
It also contains all technical drawings of the different tools and apparatus designed in this thesis. The dimensions used in the drawings are in mm.

Full layout is available here `\\felles3\ift-kjernefys1\pCT\3D_designs`. Designs were done in Autodesk Fusion 360.

Layout VX.2.4 The designs were made in Autodesk Fusion 360 and are available in .step file at a dedicated server for pCT (felles3).



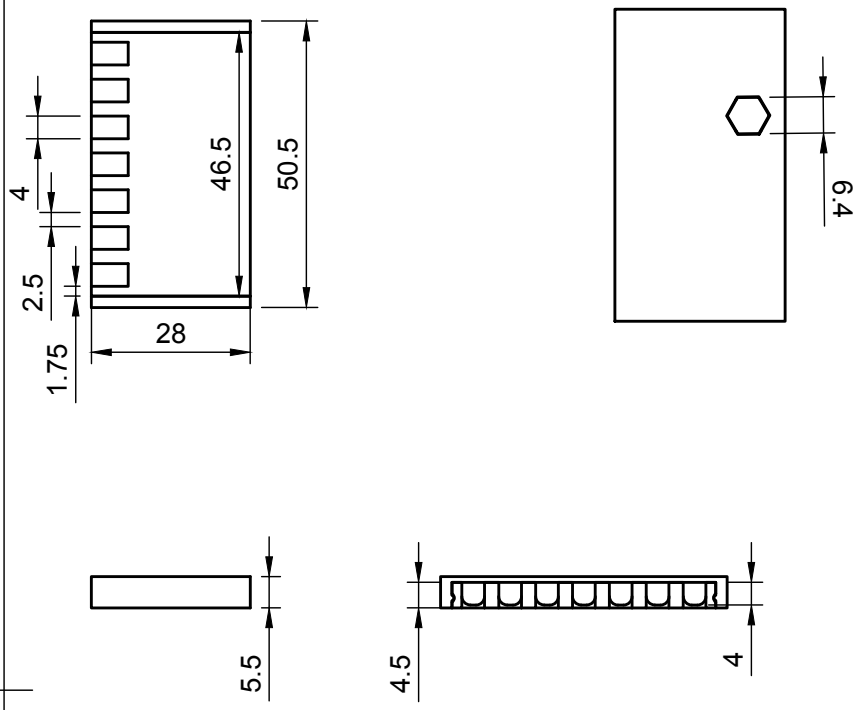
(a) including water cooling and cold plate on the top and bottom

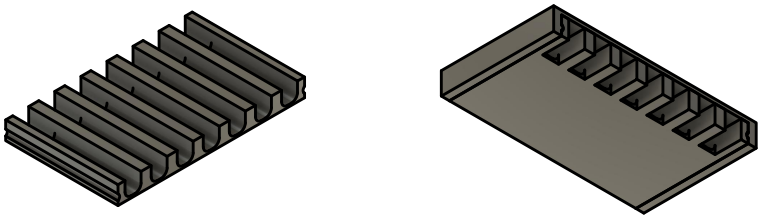


(b) including base plate with cable frame and air ducts

Figure C.1: Digital Tracking Calorimeter with TC V1.0.

Second version with
hole for the PCB pillar





Dept.	Technical reference	Created by Tea Bodova 31/01/2020	Approved by
in mm		Document type	Document status
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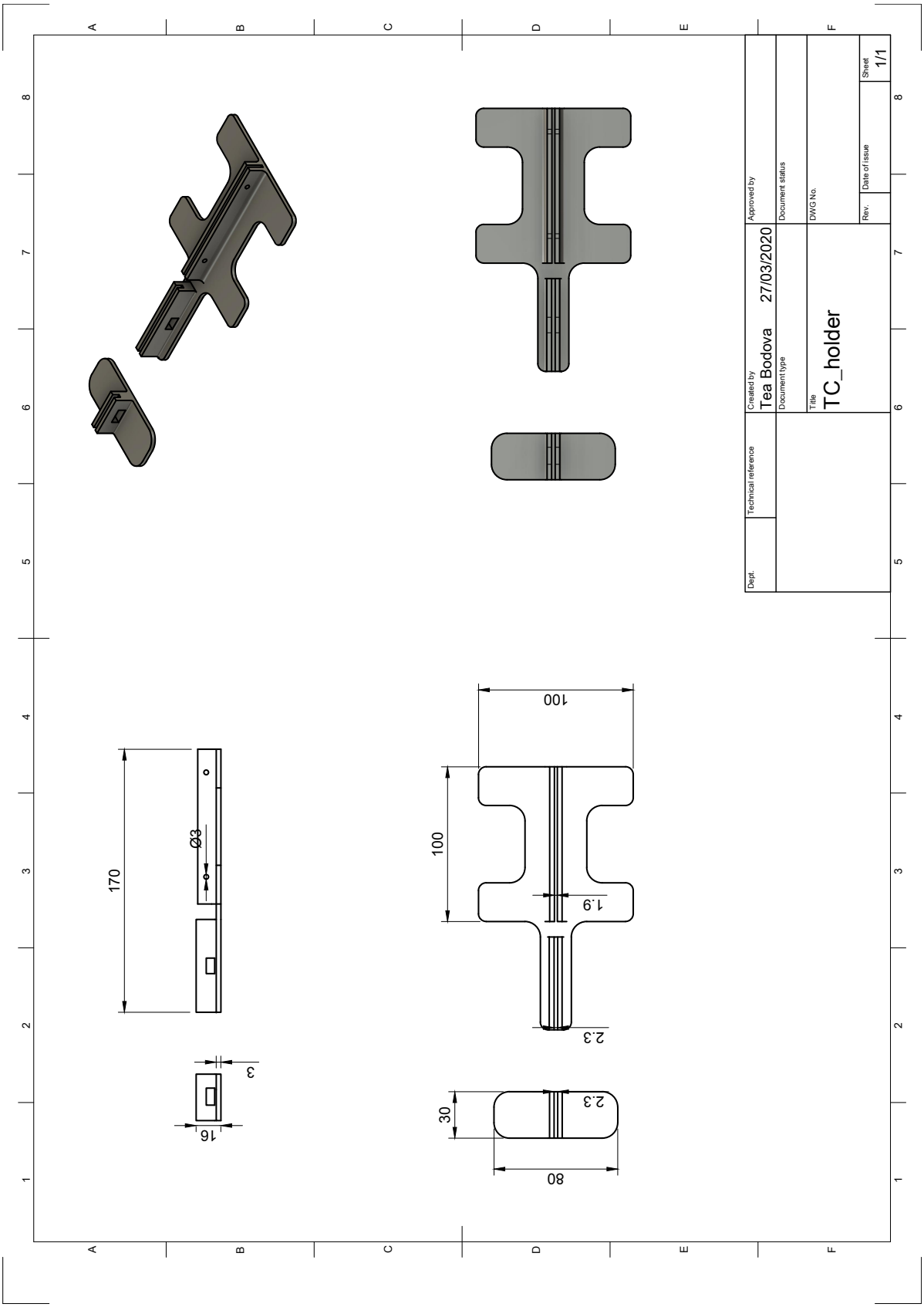
			Rev. / Date of issue / Sheet 1/1


Approved by
Document status
DWG No.
Sheet 1/1
Rev.
Date of issue
Created by Tea Bodova 27/03/2020
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Dept.
Technical reference
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100
1.9
2.3
2.3
30
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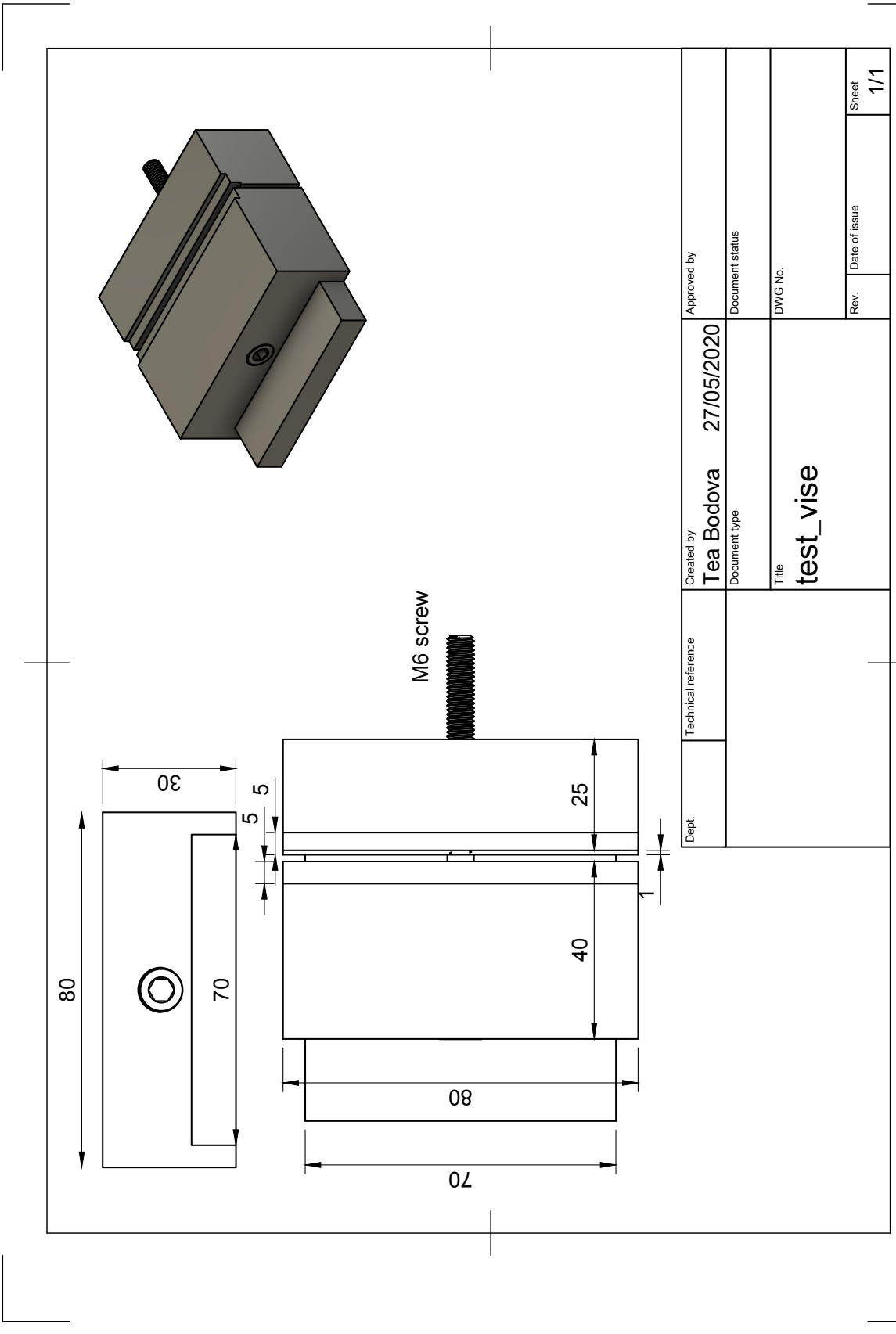
170
Ø3
3
16


M6 screw
30
5
5
25
1
40
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Tea Bodova
27/05/2020
Approved by
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Document status
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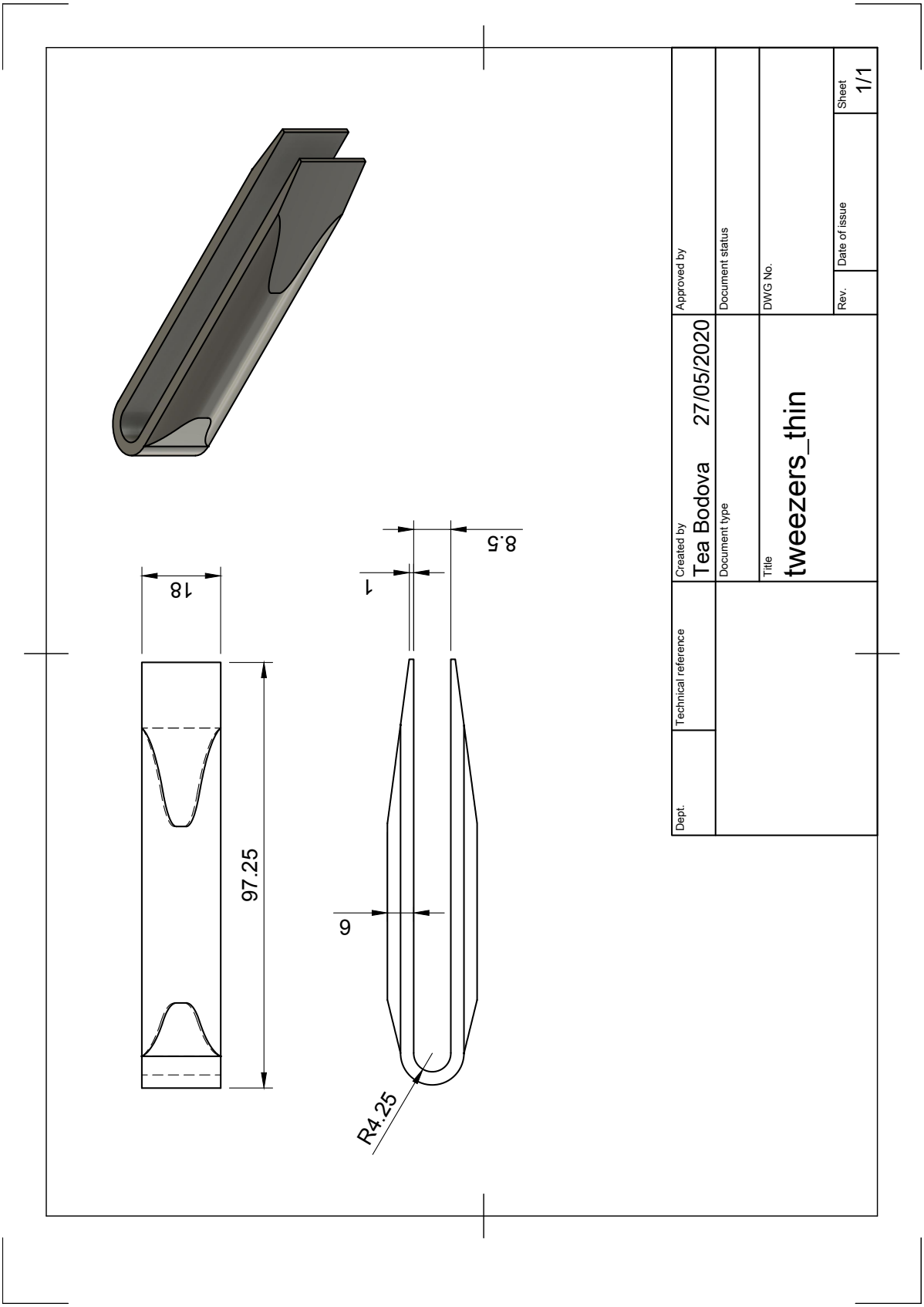
DWG No.
Rev.
Date of issue
Sheet
1/1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8.5
6
R4.25
Dept.
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Created by
Tea Bodova 27/05/2020
Document type
Approved by
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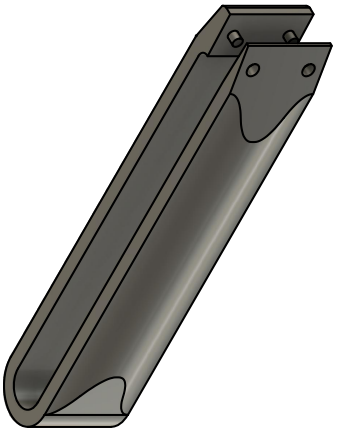
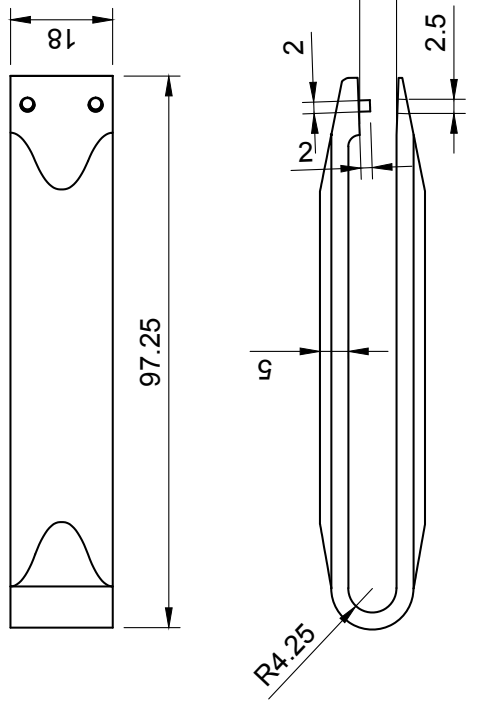
tweezers_thin
Rev.
Date of issue
Sheet
1/1





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		Document type	Document status
		Title: tweezers_pins	DWG No.
			Rev. / Date of issue
			Sheet 1/1

APPENDIX D

TC V1.0 Manual

Transition Card V1.0 for pCT
Manual
University of Bergen
February 2020

D.1 Introduction

TC is a Transition card designed for Proton Computed Tomography at University of Bergen. It provides power to twelve 9-chip strings. Each string channel consists of a ZIF connector, one voltage regulator for DVDD, one for AVDD and a FireFly connector. There are 11 differential pairs between ZIF and FF (controlled impedance of the traces is 100 Ω). Both regulators output 1.9 V. Firefly connectors are positioned on the TOP of the PCB. ZIFs and voltage regulators are on both sides.

D.2 How to Use

1. Assure that the board is clean from the flux. Especially the Firefly and ZIF connectors. The area before the ZIF connectors (the string side) must be clean as well. Clean with isopropyl alcohol if possible.
2. Use 3 V for both DVDD and AVDD on the power supply.
3. Set current limit on the power supply according to how many 9-chip strings are connected to TC. The current limit for AVDD is 0.2 A and for DVDD is 1 A of one 9-chip string.

4. TC V1.0 is missing a common ground point that would connect AGND with GND. Connect these on the power supply. See Figure D.1.

5. It is recommended to first measure the output voltage of the regulators before connecting the rest when TC is used for the first time. See Section D.3.

6. Connect FireFly cable to the designated FireFly connector. See Section D.5 on which FireFly connector belongs to which ZIF connector.

7. Turn the power off when connecting the string.

8. Connect flex end of the string to the ZIF connector. The ZIF has **BOTTOM** connection! Contacts on flex must face the PCB. The cable is very fragile! The ZIF connector can be mated only 20 times. This means that once the string is connected and working, don't disconnect it again for no reason.

9. Turn the power back on and check if the voltage is stable (1.9 V). The current should be around 0.125 A for the AVDD and around 0.400 A for DVDD when the clock and data transfer is not initiated. When the clock and data transfer is on, the DVDD current will increase to about 0.900 A. The DVDD current when chips are idle will also increase because of the increasing temperature to about 0.550 A. If the current or voltage isn't stable, the flex end can be misaligned with the ZIF contacts. Try to disconnect and connect the flex again.

10. If PWELL connection is needed, solder an extra cable to the power connection. Use crimp terminal from Molex (part number 1722490100) and a 1.5 mm^2 cable. Remove resistor R1. This resistor is mounted by default to AGND. It is positioned right next to the PWELL input on the TOP side (side with UiB logo on) of the TC.

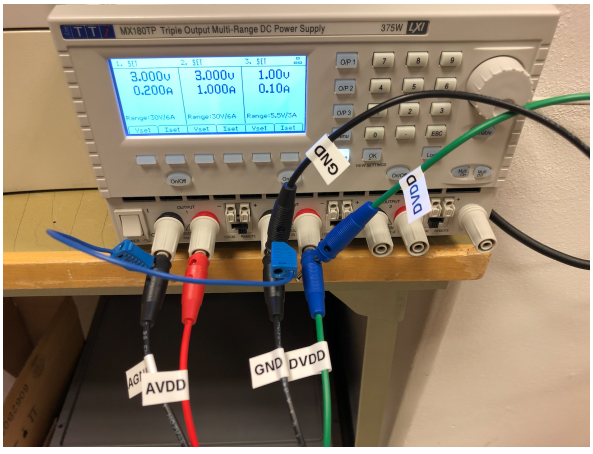


Figure D.1: Power supply setup.

D.3 Test Points

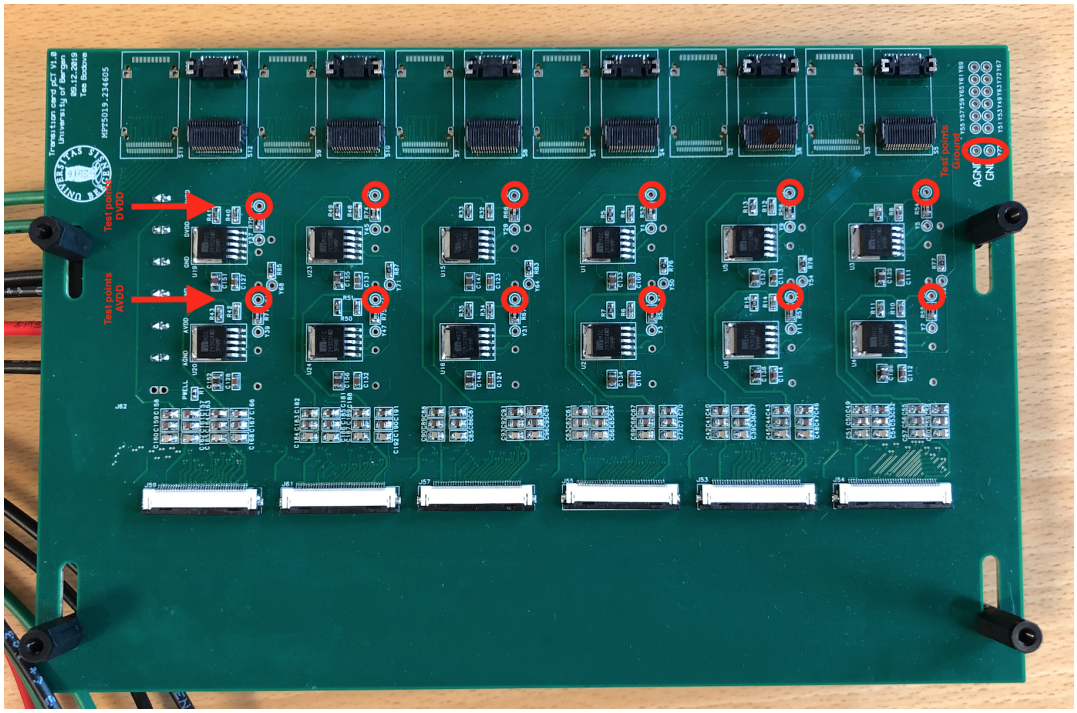


Figure D.2: Test points for output voltage from voltage regulator on the TC.

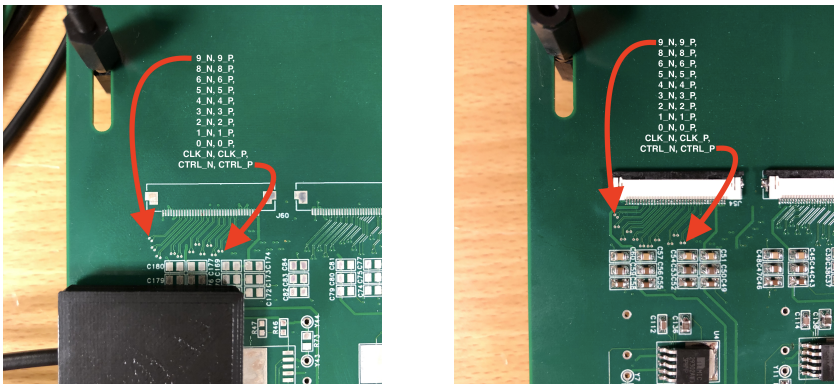
There are several test points on the TC. Every voltage regulator has a 100 mΩ resistor in series with the output pin. On both sides of the resistor are two test points. These can be used to measure the current. The test points on the right side of the resistor can be used to measure the output voltage of the regulator (see Figure D.4). There are also ground reference points in the bottom right corner. The output voltage is usually 1.97 V (ranges between 1.95V to 2.00V) when no load (so no chip string) is connected to the ZIF connector. When the load is connected, voltage drops to approximately 1.91 V (this also varies, but it shouldn't be less than 1.90 V).

D.4 Other Remarks

The voltage regulators draw very little current. However, if there is need to disable some of the channels, it can be done so by connecting the designated through-hole contact to the ground. These contacts are in the bottom right corner by the ground reference points. First row belongs to the BOTTOM side of the TC and the second row is connected to the regulators on the TOP side. It is easy to follow the trace from the contact to the designated channel.

Some of the PCBs have a 3D printed box covering the power cables. This is to help reinforce the cable's position. It also prevents short circuits. This box has to parts and they are not attached to the PCB in any way. Both parts can be removed at any time.

ZIF J54 and J60 have open vias on the differential pairs that can be probed. See Figure D.3 for the pinout.



(a) (b)

Figure D.3: Pinout for the differential pairs.

D.5 FireFly-ZIF Connection

Table D.1 shows which FireFly connector is associated with which ZIF connector.

Table D.1: FireFly-ZIF connection labeling.

	Channel	FireFly	ZIF
TOP	1	S12	J59
	2	S10	J61
	3	S8	J57
	4	S4	J55
	5	S6	J53
	6	S5	J54
BOTTOM	7	S11	J60
	8	S9	J56
	9	S7	J58
	10	S1	J50
	11	S2	J51
	12	S3	J52

D.6 Troubleshooting

If TC doesn't work, here are some possible solutions:

- Check power supply. Is the output on? Is the AGND and GND connected at power supply? Is the current limit and voltage set to the right values?
- Check if the output voltage from voltage regulators is around 1.9 V.
- Check if FireFly cable is inserted all the way into the connector on both sides of the cable.
- Check if FireFly is connected to the right channel.
- Check if the flex is inserted all the way to the ZIF connector.
- Keep the connectors (ZIF, FireFly) and flex cable clean. Use isopropyl alcohol to clean the contacts.
- Inspect if the flex isn't damaged.
- Check if the through-hole contacts by the ground reference points (bottom right corner) aren't connected to ground. This disables the voltage regulators.

D.7 Bill of Material

#	PART	VALUE	GEOMETRY	QTY	REFERENCE NAME	Manuf. Nr.	Farnell nr.	COMMENT
1	CAP	1 uF	C0805	48	C1,4,7,10,13,16,19,22,25,28,31,34, 37,40,43,46,49,52,55,58,61,64,67,	GCM21BR7YA105KA55L	2494199	
2	CAP	10uF	C0805	48		GCM21BR70J106KE22L	2470434	
3	CAP	0. 1uF	C0805	48	21,23,24,26,27,29,30,32,33,35,36, 38,39,41,42,44,45,47,48,50,51,53,	GCM21BR72A104KA37L	2470440	
4	CAP	10 uF	C0603	24	C109-C132	ZRB18AC81A106KE01L	2990841	
5	CAP	33 uF	C0805	24	C133-C156	C2012X5R1A336M125AC	2525132	
6	crimp_terminal		crimp_terminal	7	J62	172249-0100	2454266	
7	MIC29302		SOT252	24	U1-U24	MIC29302AWD	2774962	
8	MOLEX_36		MOLEX_ZIF_BOTTOM_36	12	J50-J61	54132-3633	3215815	
9	RES	0 Ohm	R0402	1	R1	ERJ2GE0R00X	2059190	
10	RES	3.3k Ohm	R0603	12	R76-87	CRCW06033K30FKEA	1469793	
11	RES	536 Ohm	R0603	24	R4-R50 (only even numbers)	WR06X5360FTL	2670838	
12	RES	1k Ohm	R0603	24	R5-R51 (only odd numbers)	CRGCQ0603F1K0	2861461	
13	SHUNT_R805	100m Ohm	R0805	24	R52-R75	CRM0805-FX-R100ELF	1865233	
14	UEC5-19		UEC5-19-1	12	S1-S12	UCC8-010-1-H-S-1-A	2856850	this component has 2 parts
				12		UEC5-019-1-H-D-RA-1-A	2856133	

Figure D.4: Bill of Materials for the TC.

APPENDIX E

Power Supply Python Code

The Model (power_supply.py)

```
"""
Python class that implements functions based on the manual
    for Aim TTI MX180TP power supply

$ pip install -U pyvisa)
"""

import pyvisa


"""
!!!
Run this first if pt.py GUI is not used to find the res

run this to find res:
import pyvisa
rm = pyvisa.ResourceManager('@py')
print(rm.list_resources())
"""

class PowerSupply(object):
    def __init__(self, timeout=2500):
        self.timeout = timeout
        self.rm = pyvisa.ResourceManager('@py')
        self.instr = None

    def openResource(self, res):
        self.instr = self.rm.open_resource(res)
```

```
        self.instr.read_termination = '\r\n'
        self.instr.write_termination = '\n'
        self.instr.timeout = self.timeout
        self.reset()


    def reset(self):
        self.instr.write('*RST')

    def get_id(self):
        return self.instr.query('*IDN?')

    def output_on_all(self):
        self.instr.write("OPALL 1")

    def output_off_all(self):
        self.instr.write("OPALL 0")

    def output_on(self, channel):
        output = "OP" + str(channel) + " 1"
        self.instr.write(output)

    def output_off(self, channel):
        output = "OP" + str(channel) + " 0"
        self.instr.write(output)

    def set_voltage(self, channel, voltage):
        output = "V" + str(channel) + " " + str(voltage)
        #print("setting " + str(output))
        self.instr.write(output)

    def set_current(self, channel, current):
        output = "I" + str(channel) + " " + str(current)
        #print("setting " + str(output))
        self.instr.write(output)

    def read_voltage(self, channel):
        output = "V" + str(channel) + "O?"
        #print("setting " + str(output))
        return self.instr.query(output)

    def read_current(self, channel):
        output = "I" + str(channel) + "O?"
        #print("setting " + str(output))
```

```
        return self.instr.query(output)
    class OutputCurrentTooLargeException(Exception):
        """Raised when output current is too high"""
        pass
```

The Controller (supply_controller.py)

```
"""
Python class that remotely controls and monitors power supply
Implements also another class (PowerSupply)

This class contains an thread that checks every 2 sec if the
    voltage is different than the setup voltage for output 1
    and 2
The reason behind is that if load connected to the power
    supply exceeds the set current limit, the output voltage
    decreases
The thread also puts readings of output voltage and current
    for both outputs into a queue
The data from queue is then sent to a log
Logging should be confgured in the main workflow!
Example:
logging.basicConfig(filename='data.log',filemode='w', level=
    logging.DEBUG, format='%(asctime)s %(message)s %(
    threadName)s')

!!! you should call output_off_all() from the main workflow
    after finishing all the tests !!!

Code based on MX180TP power supply
Change the values for the output error if different power
    supply in use!

"""


from power_supply import PowerSupply
import time
import logging
from queue import Queue
from threading import Thread

class SupplyController(object):

    #q = Queue(maxsize=0) ## maxsize = 0 means infinite queue
```

```
    hence full() never returns True
     inThread = None
31   #_tti = PowerSupply()

33   def __init__(self, inThread = True):
         self.inThread = inThread
35       self._tti = PowerSupply()

37       self.voltage_1_plus = 0
         self.voltage_1_minus = 0
39       self.voltage_2_plus = 0
         self.voltage_2_minus = 0
41
     def setOn(self, res):
43       self._tti.openResource(res)

45   def on(self, voltage_1, voltage_2, current_1, current_2):
         #Turns on the power supply
47
         self._tti.set_voltage(1, voltage_1)
49       self._tti.set_current(1, current_1)
         self._tti.set_voltage(2, voltage_2)
51       self._tti.set_current(2, current_2)
         """Treated for power supply error
53       Output1: Voltage   0.05% of reading + 3mv
         Output2: Voltage   0.1% of reading + 10mv"""
55       self.voltage_1_plus = float(voltage_1) + 0.005
         self.voltage_1_minus = float(voltage_1)   0.005
57       self.voltage_2_plus = float(voltage_2) + 0.01
         self.voltage_2_minus = float(voltage_2)   0.01
59


61       self._tti.output_on(2)
         time.sleep(3) ##AVDD/channel(1) will be turned 3
    seconds later
63       self._tti.output_on(1)

65       if self.inThread:

67           th = Thread(target=self._check_power_output)
             th.daemon = True ## define if process should be a
     deamon   deamon processes shut down abruptly when main
    program ends
69           th.start()
```

```
        else:
71          self._check_power_output()

73  def off(self):
        ## Turns off the power supply
75      self._tti.output_off_all()


77
    def _end_execution_with_error(self):
79      self._tti.output_off_all()
        print('Exceeded current limit')
81      #logging.error('Exceeded current limit')
        raise PowerSupply.OutputCurrentTooLargeException()
83
    def _check_power_output(self):
85
        while True:
87          time.sleep(2)
            # data_current_1 = self._tti.read_current(1)
89          # data_current_2 = self._tti.read_current(2)
            # data_voltage_1 = self._tti.read_voltage(1)
91          # data_voltage_2 = self._tti.read_voltage(2)
            #data = ['Ch_1',data_current_1,data_voltage_1,'
    Ch_2',data_current_2,data_voltage_2]
93          #self.q.put(data)
            #logOut= self.q.get()
95          #logging.debug(logOut)

97          if float(self._tti.read_voltage(1)[0:5]) < self.
    voltage_1_minus  or float(self._tti.read_voltage(1)[0:5])
    > self.voltage_1_plus or float(self._tti.read_voltage(2)
    [0:5]) < self.voltage_2_minus or float(self._tti.
    read_voltage(2)[0:5]) > self.voltage_2_plus :
                self._end_execution_with_error()
99              #self.q.task_done()
```

The View(pt.py)

```
"""
2 part of the pt.py GUI code that is connected to the power
    supply code

4 """
def resources(self):
6       res = self.cb_resources.currentText()
```

```
            self.supplyController.setOn(res)
8           self.btn_connect.setEnabled(True)
            self.btn_power_supply.setEnabled(True)
10          self.btn_power_supply_off.setEnabled(True)


12
    def ps_ON(self):
14          V_1 = self.line_voltage_1.text()
            V_2 = self.line_voltage_2.text()
16          I_1 = self.line_current_1.text()
            I_2 = self.line_current_2.text()
18          self.supplyController.on(V_1, V_2, I_1, I_2)
            self.btn_power_supply.setEnabled(True)
20
    def ps_OFF(self):
22          self.supplyController.off()
            self.btn_power_supply_off.setEnabled(True)
```

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