

Paper V

The Detector Control System of the ATLAS SemiConductor Tracker during Macro-Assembly and Integration

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Abstract

The ATLAS SemiConductor Tracker (SCT) is one of the largest existing semiconductor detectors. It is situated between the Pixel detector and the Transition Radiation Tracker close to one of the four interaction points of the Large Hadron Collider (LHC). During 2007 the installation inside the TRT will be completed and the detector lowered into the ATLAS cavern and installed in its final position.

The SCT consists of 15 392 silicon wafers containing around 6.3 million readout channels which are assembled into 4088 detector modules. These modules are mounted on four barrel cylinders and 2×9 end-cap disks and are read out via optical links. For the assembly, commissioning and integration phase, a complete Detector Control System was developed to ensure the safe operation of the tracker. This included control of the individual powering of the silicon modules up to 500 V bias voltage and 30 kW low voltage power, its bi-phased cooling system together with various types of sensors monitoring the SCT environment and the surrounding test enclosure. The DCS software architecture, performance and operational experience will be presented in the view of a validation of the DCS for the final SCT installation and operation phase.

1. Introduction

The ATLAS detector is a multi-purpose detector currently being constructed at one of the four interaction points along the 27 km circumference

LHC accelerator. The detector will study p-p collisions with 14 TeV centre-of-mass energy at a design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and with a 25 ns bunch crossing time. Three main layers of trackers, calorimeters and muon chambers are centred

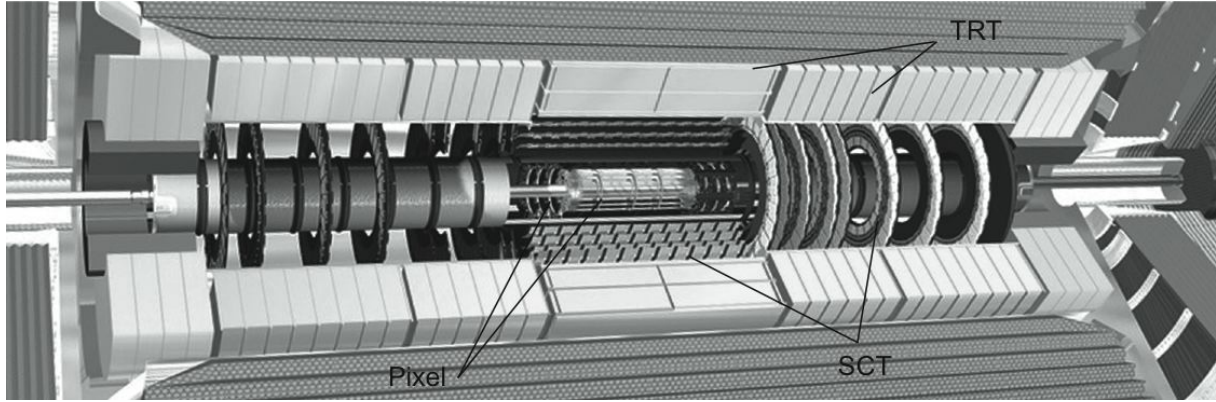


Fig. 1. The ATLAS Inner Detector. The SCT can be seen in the middle consisting of 4 cylindrical barrels and 18 disks, 9 at each end. Between the SCT and the TRT the thermal enclosure protects the SCT and Pixel environmental conditions.

around the interaction point. The central tracker, the Inner Detector (ID), is situated inside a 2 T central superconducting solenoid magnet (see figure 1). It consists of the Pixel detector (Pixel) closest to the beam, surrounded by the SCT detector and the outer Transition Radiation Tracker (TRT). During the envisaged 10 years of operation the total particle fluence is expected to be of $2 \cdot 10^{14} \text{ cm}^{-2}$ 1-MeV neutron equivalent, resulting in a continuous degradation of the detectors.

The SCT will provide at least four space points per track and will have a pseudorapidity coverage up to $\eta = 2.5$. To achieve this, the detector consists of one central barrel, where 2112 barrel modules have been mounted to cover the full outer surface of four cylinders, and one end-cap in each forward region, where the 1976 end-cap modules have been mounted on 18 disks.

The barrel detector modules [1] are identical and made of two single-sided p-on-n microstrip sensors with $80 \mu\text{m}$ pitch bonded together and glued back-to-back at 40 mrad stereo angle to provide two-dimensional track reconstruction. Both sides have each 768 strips of 12 cm total active length which are read out by 12 ABCD3TA [3] radiation hard ASICs, mounted on a copper/kapton hybrid located at the module centre. The end-cap modules [2] have four different radial geometries depending on their position relative to the collision centre and their readout hybrid is mounted at the sensor edge. A binary architecture has been chosen, being the most cost-effective implementation

meeting the performance requirements.

Parallel to the detector construction a DCS system has been developed to ensure the safe and reliable operation and control of the SCT. The high hardware requirements and extreme environmental conditions of the SCT detector are two of the main challenges faced by the SCT DCS system. Preliminary DCS results have been presented in [4–6]. Currently, the SCT DCS is in its final development stage, after being extensively tested and validated during detector assembly, integration and commissioning. A summary of these results, focusing on the validation of the safe operation and control of the SCT, is presented in this note.

2. SCT Detector Control System

Several power lines are needed to operate a single SCT module: bias voltage for sensor operation, several low voltages for the readout electronics and for the conversion of optical signals into electrical. They are all provided by the DCS system, which also provides several slow commands for basic configuration of the SCT detector modules. Due to the large heat dissipation and to the increasing damage due to the radiation, the modules need to be cooled and to be in a dry nitrogen atmosphere. The cooling is provided by a bi-phase C_3F_8 cooling system [7] running at -25°C which cools the detector modules to the operating temperature of -7°C . The

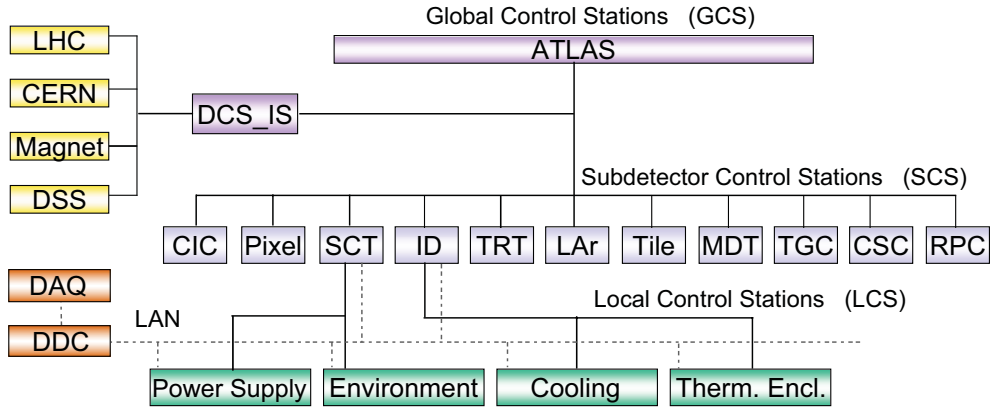


Fig. 2. Overview of the ATLAS DCS structure. Both the SCT and the ID DCS are managed by separate Subdetector Control stations (SCS) which each controls several independent PVSS projects.

Pixel and SCT detectors are also surrounded by a thermal enclosure, which permits cold operations, while the TRT is maintained at $+25^{\circ}\text{C}$.

In addition, the radiation results in increased sensor leakage current, type inversion, increasing depletion voltage and signal degradation due to charge trapping. It is expected that for the worst affected detector modules the bias voltage needs to be raised from the nominal value (150V) up to a maximal value of 500 V. After 10 years of operation it is foreseen that one module will dissipate 10 W (7.4 W from the hybrid) in the worst case. In comparison, unirradiated modules produce initially 5.6 W (5.4 W from the hybrid).

The main goal of the SCT DCS is to provide the detector with power, cooling and necessary control signals as well as to protect the detector from any failure or error conditions. If any situation occurs where the detector is in danger the DCS system should provide a rapid response, either by software actions (if possible) or by hardware interlocks. The SCT DCS also needs to provide a safe communication between the subsystems, with the ATLAS DCS as well as with the SCT data acquisition system (DAQ). Both state transitions and errors need to be propagated to the ATLAS DCS and to the SCT DAQ in an unambiguous way.

2.1. DCS Overview

The ATLAS DCS is based on a custom solution developed for the LHC experiments. The subdetector hardware equipment is read out by a standard Controller Area Network (CAN) fieldbus [12] and a custom developed OPC CANopen server. A custom Embedded Local Monitor Board (ELMB) [8] has been developed, to provide an interface between the subdetector equipment and the readout system where this is needed. A Supervisory Control and Data Acquisition system, PVSS II [9,10], controls the data communication, alarm handling and data display. The core of the software is provided by the subdetectors individually, whereas the CERN Joint Controls Project (JCOP) [11] has developed several software tools to provide interfaces to the most common hardware. JCOP also provides the top layer solution for the overall control of ATLAS based on a Finite State Machine (FSM) written in SMI++ which interacts with the subdetector DCS via state transitions and error messages.

The main aim of the common ATLAS DCS is to make it as homogeneous as possible, with rapid communication, without compromising the functionality of the subdetector DCS. The overall architecture of the ATLAS DCS, including the SCT DCS and the ID DCS, for the part which is relevant to the SCT detector, is shown in figure 2.

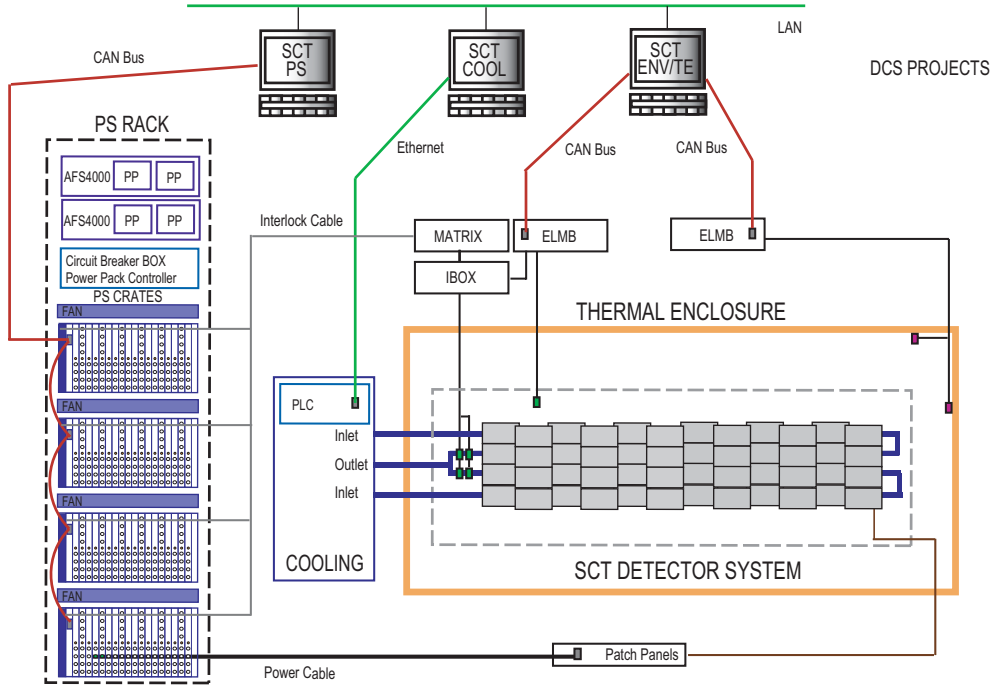


Fig. 3. The SCT DCS configuration used during surface tests. The Power Supply, Cooling, Environmental and Test Enclosure projects are shown, as well as their connection to the hardware.

2.2. SCT Software Architecture

The core SCT DCS is divided into two subsystems, each controlling and monitoring a part of the detector system: the Power Supply system and the Environmental monitoring. In addition, several DCS systems common for the ID system has been developed by the SCT group and are essential to the operation of this detector, notably the Cooling System and the Test Enclosure (monitoring an early prototype of the Thermal Enclosure). Figure 3 shows a subset of the hardware controlled by the four SCT and ID DCS systems. All systems were linked together as distributed PVSS projects to allow DCS to DCS communication.

A. Power Supply DCS

The largest part of the SCT DCS system is the Power Supply (PS) system [13]. Each detector module is powered and controlled by two completely independent and floating power supplies. The high voltage supplies provide the 150

V nominal bias voltage necessary to deplete the sensor and the low voltage supplies provide digital and analogue voltages to the ABCD3TA chip, the opto-communication drivers [19], such as the DORIC4 chip, the VCSEL drivers circuit and the VDC chip as well as the VCSEL control voltage and the PIN photo diode bias voltage. In addition to power, each module is also provided with two signal lines for Reset and Clock select, four sense wires which probe remotely the low voltages and several parameters permit to set limits on the currents and to tune and control the power supply cards. Finally, there are two current sources on each Low Voltage (LV) power channel supplying the Negative Thermal Coefficient (NTC) ($R_{25} = 10 \text{ k}\Omega \pm 5\%$) thermistors mounted on the SCT detector module, two for the barrel modules (one on each side) and one for the end-cap module, which permit to read the hybrid temperatures. An overview of all readout and set parameters associated with one module is found in table 1.

In order to assure safe operation of the detector modules several safety mechanisms are imple-

Param.	Typical	Hard. Trip	Firmware	CC
V_{bias}	150V	500	set value	10 V^1
V_{cc}	3.5V	10V	-	-
V_{ccPS}	3.6V	10V	-	-
V_{dd}	4.0V	10V	-	-
V_{ddPS}	4.4V	10V	-	-
V_{VCSL}	1.6V - 6.6V	9.6V	-	-
V_{PIN}	5-10V	13 V	-	-
I_{bias}	$0.3\mu\text{A}$	5mA	$5\mu\text{A}$	$3\mu\text{A}$
I_{cc}	900mA	1300mA	-	-
V_{ccRET}	0.08V	10V	-	-
I_{dd}	579mA	1300mA	-	-
V_{ddRET}	0.08V	10V	-	-
I_{VCSL}	4mA	10mA	-	-
I_{PIN}	0.5mA	2.0mA	-	-
$T1_{module}$	0°C	38°C	35°C	33°C
$T2_{module}$	0°C	38°C	35°C	33°C

Table 1

The 16 power supply readout values per module and their hardware trip limits, programmable firmware trip limits and the Crate Controller limits.

mented in the power supply system. Each High Voltage (HV) channel has an absolute (hardware) over-current and over-voltage protection which automatically trips the voltage in case any of these parameters exceeds the limits. The LV channel has a limit on the maximum output current and detector module temperature. The hardware trip values are given in table 1. In addition the PS channels handle the firmware programmable limits which, during stable operation of the system, will be set to values that are lower than the hardware limits for: hybrid temperature, bias voltage and over-current trip reaction time for I_{cc} and I_{dd} .

The PS system has a hierarchical structure. The highest level in the hardware hierarchy is the power supply crate which contains 12 LV cards with four output channels each and six HV cards with eight output channels each. The crates are equipped with a Crate Controller (CC) board built upon the ELMB card. The CC is an interface between the power supply boards and the

higher levels of the control system. It handles multiplexed commands from the supervisory DCS application, translates it into sequences of single commands and propagates them to the PS boards using a custom communication protocol. This custom communication protocol uses an 8-bit parallel address/data bus and several control signal lines, physically located on the backplane of the crate. The communication with the DCS computer is done by means of a CAN bus network, according to the CANopen [14] communication protocol.

The power supply crate is also connected to the hardware interlock system via a System Interlock Card (SIC), which distributes interlock signals through the backplane to the LV cards.

The *Monitor Power Supply* (MoPS) project provides a graphical user interface for monitoring online parameters and sending commands to the hardware. A large effort has been put to build a project architecture with navigation possibilities which permits both access to the hardware structure (e.g. crate, channel) as well as the detector structure (e.g. barrels, disks, cooling circuits).

Given that many parameters of the Power Supply project are crucial for the data quality it is natural for the SCT detector to have the DAQ as the main center of control and the DAQ should be able to control the power supply. This is implemented via a Distributed Information Management (DIM) system [16] which is enabled through the PVSS-DIM toolkit. It provides the DAQ-DCS Communication (DDC) [15] enabling the DAQ to both monitor PVSS parameters and send commands to the power supply system. Thus it is possible to control and monitor the power supply hardware using either the DCS interface or the DAQ.

Operating the power supply system is not a trivial task due to the high number of PS channels and the corresponding monitoring and control parameters. In total, one power supply crate needs to handle around 2500 different variables. Of those, around 1000 are purely readout values for the modules and they are updated every 15 seconds to ensure fast detection of any alarm state in the system. Another ~ 1000 are used to configure the modules while the rest of the parameters are mainly used to configure and control the power supply cards.

Due to the size and complexity of the system

¹ Applied only for PS channels in OFF state

it is challenging to have a high readout frequency, required for detector safety, and at the same time keep the CAN bus occupancy below 65% as required by ATLAS DCS. Sending the configuration parameters (14 CAN frames for one PS channel) significantly increases the bus occupancy and slows down the data handling in the OPCserver and the MoPS project. Hence, in order to comply with the system readout and setup time, as requested by ATLAS DCS, and at the same time respect the CAN bus occupancy bounds, three sets of configuration parameters with associated alarm limits for each PS channel are stored in the non-volatile EEPROM memory on the CC board. The EEPROM memory also stores the mapping between PS channels and DAQ groups. Using the stored mapping the custom command format allows for configuration and passing of commands to individual DAQ groups. Each group action requires only one frame sent over the CAN bus, which significantly reduce the CAN bus occupancy.

The configurations are written to the EEPROM by the MoPS project, typically before running the detector, using standard CANopen SDO data transfer and handshaking mechanism between the MoPS and the CC. The EEPROM can be overwritten every time new detector settings are defined, and has an endurance of at least 100 000 write/erase cycles.

The PS system needed for the complete SCT detector comprises 88 power supply crates connected to 8 CAN bus branches (11 crates per branch). Each CAN bus branch is supervised by a separate PC. Such granularity of the system assures a satisfactory performance and a reasonable number of computers on the network. A subset of 11 power supply crates was used during integration of the SCT detector and tests with cosmics.

B. Environmental DCS & Interlock

Environmental monitoring is needed to supervise the running conditions for the SCT detector. Four quantities are read out to monitor the detector: the temperature of the carbon fiber structure of the detector (mechanical temperatures), the temperature of the air inside the detector volume, the temperature of the cooling pipes (sensors

Part	Cooling	Monitored	Mechanical	Air	Humi
	Cooling				
Barrel 3	36	0	9	32	3
Barrel 4	44	0	9	32	4
Barrel 5	52	0	11	32	4
Barrel 6	60	0	14	32	4
External	0	0	0	8	0
Total Barrel	192	0	43	136	15
Disk 1	16	4	4	9	1
Disk 2	24	6	4	9	1
Disk 3	24	6	4(2)	9	1
Disk 4	24	6	4	9	1
Disk 5	24	0	4	9	1
Disk 6	24	6	4	3	1
Disk 7	16	0	4	3	1
Disk 8	16	0	4	3	1
Disk 9	8	2(0)	4	6(7)	0
Cylinder	0	0	0	29(27)	10
Total EC A	176	30	36	89	18
Total SCT	544	58	113	313	51

Table 2

The number of environmental sensors and their physical distribution. Numbers in parentheses are for End-Cap C. The total number for SCT takes into account that there are two end-caps.

located at the exhaust of the pipe) and the relative humidity. See table 2 for sensor figures.

The environmental conditions were monitored by two different systems during reception and combined tests. The *Environmental DCS* project, called the Envr project, handled the temperature and humidity sensors located inside the detector volume while the test enclosure project took care of extra sensors placed inside a temporary thermal enclosure (the test box) which provided thermal isolation from the outside. The test enclosure was used at the time since the final thermal enclosure was not ready for assembly. After installation of the thermal enclosure, the sensors from the test enclosure project were used to read out dew point at the exhaust air line of the detector.

The Envr project displays the monitored value for the different sensors and calculates alarms and

warnings that are propagated to the MoPS project if the values are outside a safe range (see section 2.6 for more details). The separate test enclosure project has the same functionalities for the sensors inside the test enclosure, as well as calculating the dew point using the temperature and humidity readings.

The main purpose of the interlock system is to protect the silicon detector modules from overheating if the cooling stops. The system is also designed to offer protection against laser light coming from the optical readout system and to integrate general safety measures from the ATLAS central Detector Safety System (DSS). During macro-assembly, the cooling interlock and a general safety interlock (panic button) were implemented.

To achieve a reliable and predictable system, the interlock is built using the redundant temperature sensors located at the end of a half cooling loop for 24 silicon detector modules in the barrel. The system is fully implemented in hardware without microprocessors or software needed for the system to be operational. The main components of the interlock system are the IBOX [17] which converts the analogue signal from the temperature sensor to a binary signal, the IMatrix [18] that associates power supply channels to cooling loops and the SIC that interfaces the interlock system to the power supply system. One channel from the interlock system, built upon two temperature sensors, acts on 24 channels for both LV and HV power supply cards. The interlock logic in the IMatrix is written in VHDL and programmed into LC5768VG Complex Programmable Logic Device (CPLD) from Lattice. If the interlock is triggered by high temperature on the cooling loop then the associated power supply channels are switched off in about 1 s.

C. ID Cooling DCS

The Inner Detector Cooling System [7] will cool down the SCT and Pixel detectors to the needed operational temperature for irradiated detectors of -7°C . For initial testing, warm runs of $+15^{\circ}\text{C}$ are permitted. The total system must remove 60 kW of heat from the Inner Detector and have a stability better than $\pm 2^{\circ}\text{C}$ in order to avoid thermal

Plant Parameters	Type	Nb
Global PLC status	R	1
Condensation Buffer Temperature	R/W	1
Condensation Buffer Pressure	R/W	1
Storage Tank Weight	R	1
Storage Tank Temperature	R	1
Storage Tank Pressure	R	1
Chilled Water Pressure	R	1
Input Liquid Flow	R	1
Output Liquid Flow	R	1
Distribution Rack Temperature	R/W	Nx1
Distribution Rack Pressure	R/W	Nx1

Table 3

The number of monitored parameters from different parts of the cooling plant. Eight distribution racks were used during testing. Typical values are taken during stable running.

shocks and cycles. To achieve this the detectors will be cooled using an evaporative fluorocarbon cooling system with C_3F_8 running in thin wall CuNi (SCT) or Al (Pixel) cooling tubes through the detectors with good thermal contact to each module. The cooling process is controlled by an independent Programmable Logic Controller (PLC) which is read out by a PVSS project via ethernet and a Schneider OPC server. The monitored parameters from different parts of the cooling plant are listed in table 3.

2.3. Power Supply State transitions

Safe operation of the SCT detector requires several intermediate states when the detector power is ramped up or down. The intermediate states prevent channels (modules) from tripping due to too high ramping current, but is also needed when the LHC refills and it is desirable to turn the bias voltage down (but not off) to prevent detector damage in case of accidents.

Each module of the SCT detector has three different predefined operational states for HV and LV independently. They are OFF, STANDBY and ON and each state is defined by a set value for each parameter and associated alarm threshold. Typical

ON set-values are given in table 1 and STANDBY is derived from these settings with reduced high and low voltage levels ($V_{bias} = 50V$, $V_{dd} = 3.0V$ and $V_{cc} = 2.5V$). The set-values and firmware programmable alarm limits are uploaded to the EEPROM as explained above.

When the detector is being prepared for a run it is first cooled to a temperature well below the working one under close supervision from the environmental project. Once a stable condition is obtained the detector is ready for power and DAQ. The two systems are mutually dependent on each other, hence the following switch on sequence is used:

- (1) Power crates, start MoPS project and upload latest DCS configurations to EEPROM, all channels in OFF state.
- (2) Start, boot and configure DAQ.
- (3) Ramp power to STANDBY, then to ON, and recover channels which tripped or missed a command.
- (4) DAQ configures and probes modules.
- (5) Start run.

During a run it is occasionally needed to perform MANUAL adjustments, i.e. not use the predefined set-values, to a HV or LV channel in order to tune module performance or to understand problems. From the MoPS project (either DCS or DAQ interface) it is possible to write directly to the RAM values of the Crate Controller and later command the Crate Controller to apply the RAM values to the channel. Once optimal settings have been found using manual intervention the set-values for the state in question (ON, OFF or STANDBY) should be updated and the EEPROM likewise.

An important principle during running is that working modules should not be modified if avoidable. Thus an implementation is in place to be able to perform state transitions only to channels in a given state. This allows for easy recovery of groups of modules without interfering with working modules.

At any time when the detector is powered (independent of the module power state) it is protected by the interlock system. It will turn off both the HV and LV channel associated with a module if the temperature of the cooling pipe which cools that particular module is too high. The interlock sys-

tem also provides protection against laser light in the event of an open ROD rack back door. This is done by interlocking the VCSEL line which powers the on-detector opto package for optical readout. When a temperature interlock is released both the HV and LV channels return to their OFF state and user action is needed in order to bring the module back into an operational state. For a VCSEL interlock the module returns to the same state as before the interlock.

2.4. DCS configurations

The configuration of the DCS system is the set of operating values and the corresponding four alert levels (warning low, warning high, alarm low, alarm high) for each of the detector states. The operating values are sent to the controlled hardware, while the majority of alert thresholds are used by the project. For the PS, the “alarm high” alert level for the module temperature, the bias voltage and the HV current are also sent to the Crate Controller, which will act by tripping the channel when at least one of the limits is passed (see section 2.6). Therefore, one never expects to observe any “alarm high” condition on module temperature or HV. As explained in section 2.3, for the MoPS project, the state transitions do not involve loading new configurations to the crates, being already preloaded. A set of parameters and alerts, grouped per crate and per state makes a PS DCS configuration unit, or “recipe”. The configurations are stored in an Oracle database, using the schema created with the JCOP framework functions [11]. Each configuration unit has an identifying “tag”, or name, and a version. During the tests only the most recent version of a configuration set was available for loading and editing. In addition, each tag-version pair of a configuration is associated with a text, indicating the author of the change and a short comment, and with an unique identifier, which is also written to the Crate Controller EEPROM. This feature will enable a quick test on the presently loaded configuration, to avoid reconfiguring if no change is made. To complete a configuration process three basic steps are needed: first the configuration is

loaded from the Oracle database to the memory of the project, then the relevant values are sent to the Crate Controller and finally the new values are stored in the EEPROM.

Datapoint: CrateXX.ChannelYY
Alias: Barrelxx-Rowyy-Modulezz or Endcapxx-Quadrantyy-Ringab-Modulezz
Datapoint: CrateXX.ChannelYY.Status
Alias: <i>off-line ID</i>

Table 4
Datapoints and their aliases used during tests.

During the end-cap tests the configurations for all crates were written to the Oracle database from ascii files, which had been used during the previous tests. The tag names were of the type *Crate<number>_<state>_ECtestSR1*. Only one configuration per crate per state was used; the option of storing different sets of operating conditions (e.g. for stable beam, cosmics etc..) was available, but there was no immediate use for it. The configuration values could be changed by using the editor windows, which are available within the MoPS project. All changes are recorded to the database before being applied to the hardware, which takes place upon an operator’s request. A direct connection to the Oracle database was used, while the other option of using local cacheing was available, but awaited a synchronization mechanism to be in place. The internal variables (datapoints) of the MoPS project refer to the “hardware” view of the power supplies, which are addressed by crate-channel numbers. The “logical view” is obtained by using the PVSS *alias*. During the tests two types of aliases were set: one to address the modules in the form Barrel-Row-Module or Endcap-Quadrant-Ring-Module, one to address the modules with their offline identifier as in table 4. The primary source of the aliases was an ascii file that was generated by the DAQ and loaded to the MoPS project.

For the Envr project, two complementary configuration methods are applied. First, the connection from the hardware channels to the project datapoints needs to be established. This is done using a text file, which associates an ELMB channel to a sensor, prepares the OPC server configuration file

Param.	Datapoint	Deadband	COOL folder
V_{cc}	LVch_Vcc	30 mV	/MPS/LV
V_{dd}	LVch_Vdd	30 mV	/MPS/LV
V_{ccPS}	LVps_Vcc	70 mV	/MPS/LV
V_{ddPS}	LVps_Vdd	70 mV	/MPS/LV
V_{ccRET}	LVretVcc	70 mV	/MPS/LV
V_{ddRET}	LVretVdd	70 mV	/MPS/LV
I_{cc}	LVch_Icc	15 mA	/MPS/LV
I_{dd}	LVch_Idd	15 mA	/MPS/LV
V_{VCSL}	LVchVCSV	70 mV	/MPS/OPTO
I_{VCSL}	LVchVCSI	50 mA	/MPS/OPTO
V_{PIN}	LVchPINV	70 mV	/MPS/OPTO
I_{PIN}	LVchPINI	50 mA	/MPS/OPTO
Status LV	LVchStat	none	/MPS/CHANSTAT
$T1_{module}$	MOch_Tm0	0.2 °C	/MODTEMP
$T2_{module}$	MOch_Tm1	0.2 °C	/MODTEMP
V_{bias}	HVchVolt	0.8 V	/HV
I_{bias}	HVchCurr	40 μ A	/HV
Status HV	HVchStat	none	/MPS/CHANSTAT
T_{mech}	—	0.2 °C	/ECCMECH
T_{air}	—	0.2 °C	/ECCAIR
T_{cool}	—	0.2 °C	/ECCCOOL
T_{mcool}	—	0.2 °C	/ECCMCOOL
Humi	—	0.2 %	/ECCHUMI
Humi $_{Cyl}$	—	0.2 %	/ECCHW
$T_{dewpoint}$	—	0.2 °C	/ECCDEWP

Table 5
Parameters and their correspondent datapoints and archive parameters, as used for the last part of the end-cap testing. The COOL folder are subfolders of /SCT/DCS/

and sets an alias to the datapoint in the project. Secondly, a set of four alert thresholds, each corresponding to an alert level, are inputted by the user in the software. Each type of sensors (see table 2) has its own set of alert thresholds.

2.5. Conditions Archiving

For all the projects, the data specifying the DCS conditions are stored into an Oracle database using the Oracle RDB manager. A reduction of the

data volume is necessary, to avoid filling the disk space with values due to noise fluctuations. During the end-cap test a deadband was specified for all relevant datapoints and values were written to the database only when significant changes from the previous value were measured. The deadbands were all specified in absolute values and those used during the end-cap test are reported in table 5. The parameters for archiving can be set globally or individually for a single channel using panels within the projects. The data from all the archived datapoints were then copied every 15 minutes to the COOL conditions database, using the CondDB program [20] running on a separate linux machine. The COOL folder used for the end-cap tests are also shown in table 5. The DCS data are available from the offline Oracle production database, with schema ATLAS_PVSS_SCT_SR1, while the data are available in COOL, from the schema ATLAS_COOL_SCT, which also belongs to the offline production database ATLPDOD. No reduction of data was used going from Oracle to COOL, but all the time stamps were rounded to the second. This is about the time resolution which is available from the DCS, although a better synchronization of the distributed systems, and a precise measurement of all the delays which are involved may allow for a better precision, if required. During the combined tests all the DCS data were written to the offline database. For the barrel tests the DCS data were initially stored in the internal PVSS database and then copied to the COOL database COMPROD. A copy of these data is also available from the CERN Advanced STORAGE manager (CASTOR) area of the user *sctdcs*. In both cases the *Channel_ID* corresponding to a datapoint was the *offline identifier* of the corresponding module. Datapoints which are related to the same module and are stored in different folders have the same *Channel_ID* as the module.

2.6. Systems Safety Actions

An important aspect of the DCS is to ensure the safe operation of the detector. This implies that whenever a fault occurs, the necessary action is taken either by the user or by the system itself. In

Case	Action
$T_{module} > T_{alarm}$	Switch off LV and HV
$I_{bias} > I_{alarm}$	Switch off HV
Off state: $V_{bias} > 10\text{ V}$	Switch off HV
Off state: LV output on	Switch off LV
CC $< - >$ HV/LV communication lost	Send emergency message to MoPS
CC $< - >$ MoPS communication lost	Reset Communication
$T_{cool} < T_{dewpoint} + 10^{\circ}\text{C}$	Pop up messages
$T_{cool} < T_{dewpoint} + 5^{\circ}\text{C}$	Switch off LV/HV
$T_{cool} > 22^{\circ}\text{C}$	Switch off LV/HV
$T_{air} > 30^{\circ}\text{C}$	Switch off LV/HV
$T_{mech} > 30^{\circ}\text{C}$	Switch off LV/HV
Bad status for cooling	Switch off LV/HV
Communication loss between projects	Pop up messages, operator to reestablish communication. Interlock to ensure safety.

Table 6
The DCS alerts and their associated safety action

addition, useful information must be transmitted between DCS projects to trigger the appropriate actions. The information also has to be transmitted to the DAQ, where the decision about whether to stop a physics run will be taken. Within the ATLAS DCS terminology the names *Alert* describes any alarm or warning which are due to detector problems. The name *Errors* describes the incorrect functionality of the DCS system itself. When an alert is triggered in either the environmental, the cooling or the test enclosure DCS, information about the alert is passed on to the MoPS project which will warn the user about change of condition and if needed automatically take the appropriate action. Depending on the cause and severity of the alert, action will be taken by either the power supply hardware, as explained in section 2.2, or by the MoPS project.

For the Envr project, an alarm high value on any temperature (mechanical, air or cooling) would initiate the MoPS project to perform a controlled emergency shutdown of all powered modules. The

cooling pipe temperatures were also compared to the dew point provided by the test enclosure project, which results in the same action as for the temperatures themselves. The same mechanism also prevents the module power from being ramped on if such an event occur. For the cooling project, a global software interlock prevents the MoPS from turning on the modules if no cooling is present. All projects are connected to each other (see section 2.2) and thus a loss of communication causes a software interlock in the MoPS project (much like for the cooling one).

Table 6 describes the alerts and the automatic safety actions. The alerts have their assigned priority within the projects, the highest priority corresponds to the most dangerous conditions for the detector. The alarm limits are put on parameters which are considered the most critical to the SCT system. For these parameters in the MoPS project, the CC provides an extra protection, checks them against the safety limits and performs an automatic power ramp down if necessary. Typical high alerts occur at over-temperature of the module or when the bias current goes over safe operation limit. All other alarm states are currently used purely for information and the user must take an action if considered necessary.

3. Results and Performance

The data which was archived during the different test phases that the SCT went through can be used to validate the DCS system for the final installation of ATLAS. The results for two running conditions, stable and interlocked, are presented here.

3.1. Stable running of the detector

Figure 4 shows all the environmental cooling pipe temperatures on the first layer of silicon modules in the SCT barrel (called barrel 3) as measured by the Envr project during reception testing at CERN (April 7th, 2005). The full cooling cycle is visible with the start up of the cooling followed by the ramping up of the modules power and the inverse sequence for the end of run. At around

17h00, one can notice a dip for all sensors. This corresponds to a change in back pressure settings on all pipes connected to this barrel. The individual sensors show an acceptable level of stability throughout the whole run and the spread of the temperatures is low (~ 2.5 °C).

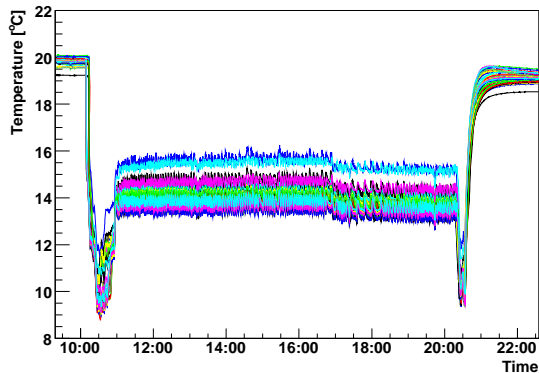


Fig. 4. Evaporative cooling cycle as measured by the environmental cooling pipe temperature sensors on barrel 3.

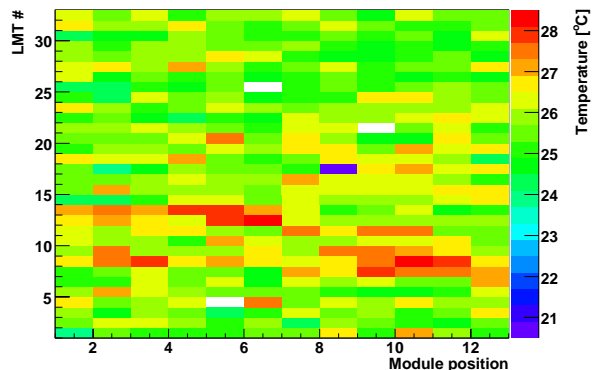


Fig. 5. Module temperature distribution for barrel 3. The temperature shown is the mean of the two temperature sensors on a module.

The temperature uniformity of the detector modules can be seen in figure 5. Each square corresponds to a single SCT module, where the mean of the two thermistor values has been calculated. Except for one cooling loop which was showing a higher temperature, the modules have a good overall uniformity [22]. Three modules were miss-

ing in the run where the data was taken, due to temporary power problems.

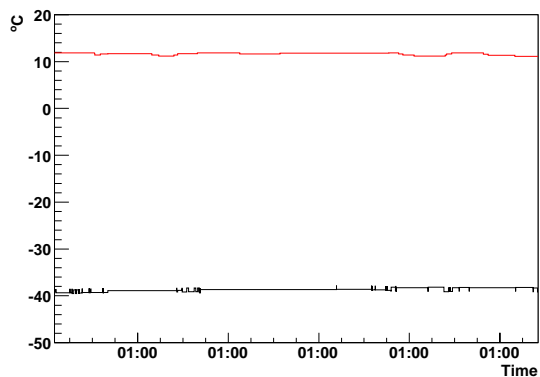


Fig. 6. Dew point calculation (black line) and monitored cooling temperature (red line) over 5 days of data taking for EC C cosmics tests.

Only one of the SCT end-caps (End-Cap C) underwent combined testing on surface. During this run, the dew point calculation was done using non-radiation hard Honeywell sensors mounted on the cylinder. Figure 6 shows the dew point calculation for one of these sensors over a five day period. The value for the dew point is low (around -39°C) and the stability is good. The value of one of the monitored cooling temperature (located in the same region on the end-cap cylinder) is high compared to the dew point, indicating that there was no risk of condensation.

The complete temperature profile for the SCT barrel during a cooling cycle can be seen in figure 7. The environmental temperatures are rising when the module power is ramped up and are decreasing when power is ramped down. The variation is more visible on the cooling pipe temperature, as these are more closely related to the modules. The air temperatures show a smaller fluctuation while the mechanical temperatures have a stable behaviour within a 5°C margin.

Figure 8 shows the humidity trend recorded by the Xeritron humidity sensors when the test enclosure is flushed with dry air. The humidity was monitored both in the test enclosure by a non-radiation hard IST humidity sensor and by radiation hard Xeritron humidity sensors mounted on

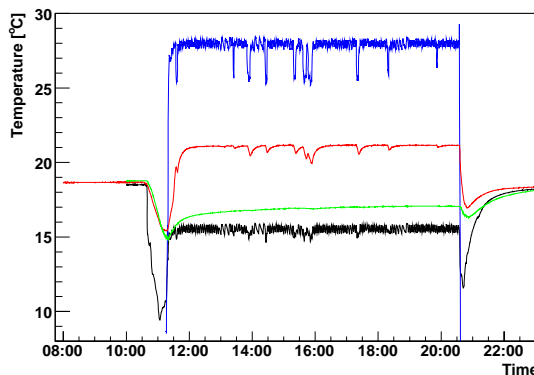


Fig. 7. A view of all temperatures for a cooling cycle on the SCT: cooling pipe (black line), air (red line), mechanical (green line) and module temperatures (blue line) are shown for the data from May 10th 2006).

the SCT end flanges. The non-radiation hard sensor showed that the test enclosure dried out in a few hours while the Xeritron sensor shows a much slower trend. The slow response of the Xeritron sensors at low humidity is a known feature which details can be found in [21]. The slow response is amplified if there is poor air circulation around the sensor.

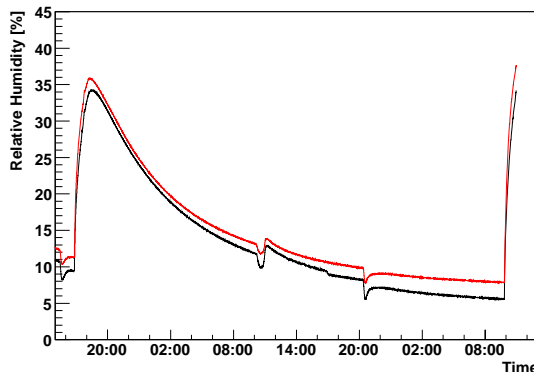


Fig. 8. Relative humidity readings from the Xeritron sensors inside the detector volume (barrel 3) during reception testing over 46 hours.

Another feature of the sensor is a slight sensitivity to temperature which can potentially be a problem since the temperature of the SCT is very different if the detector modules are switched off, powered or clocked. The humidity trend shown in fig-

ure 8 shows two glitches corresponding to changes in temperature of SCT. Fortunately the humidity can be easily corrected for temperature in the OPC server by a correction function based on the individual resistances and total resistance of the Xeritron sensor.

To ensure a minimum number of noise hits in the detector, the power supply hardware and software needs to deliver bias voltages (HV) which are stable and reliable over time. When the high voltage is ramped to its nominal working point the bias leakage current rises to a level about 10 times higher than those observed during stable operation, due to charging currents. Figure 9 shows such a behaviour where the bias leakage current peaks at about $\sim 3 \mu\text{A}$ before settling to 300 nA.

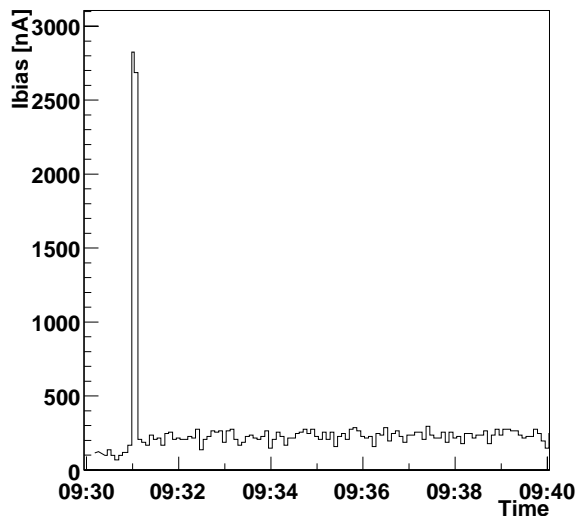


Fig. 9. When the high voltage is ramped from 0V to 150V the bias leakage current increases significantly due to charging currents.

After ramping has been completed the bias leakage current should remain essentially stable, subject only to small changes due to variations in module temperature, which can in turn be influenced by DAQ activity. Figure 11 (see next page) shows the current for one hour of cosmic data taking, during which ~ 7000 cosmic events were recorded. The fluctuations around the mean value of 258 nA are in agreement with the readout resolution which,

summing the contributions from ADC and noise of electronic elements, account to about 100nA. A detailed study of the data recorded shows only 37 entries of the 660 readings yield a $\Delta I_{\text{bias}} > 100 \text{ nA}$. The weak dependence on DAQ actions is shown in figure 10 where both module bias and pin current are plotted together. When the module is not clocked and configured (Pin I $\sim 40 \text{ nA}$) the module temperature falls by a couple of degrees Celsius and this can be seen in the bias current which slightly decreases during the same time.

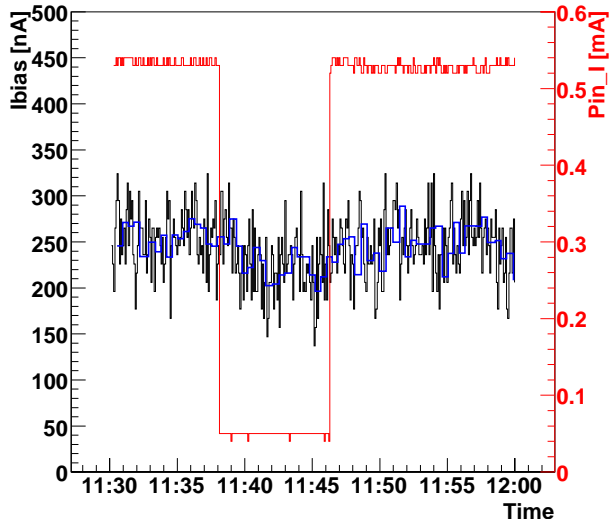


Fig. 10. The dependence on DAQ activities can be seen as a slight reduction in the leakage current (best seen by the bold blue line which is the mean of the preceding 10 I_{bias} readouts) when the module is not clocked and configured (Pin I $\sim 40 \text{ nA}$).

The SCT detector is ramped on in three stages (OFF, STANDBY and ON as discussed in section 2.3). During these steps the detector module gradually heats up from the the OFF condition where the temperature is mainly that of the cooling alone. Figure 12 shows the temperature development as the module moves through the following stages (see figure for details):

- (1) From OFF to STB. HV is ramped to 50V and the LV voltages are set to reduced levels ($V_{\text{dd}} = 3.0\text{V}$ and $V_{\text{cc}} = 2.5\text{V}$). The voltages VCSEL and PINV, related to the opto elec-

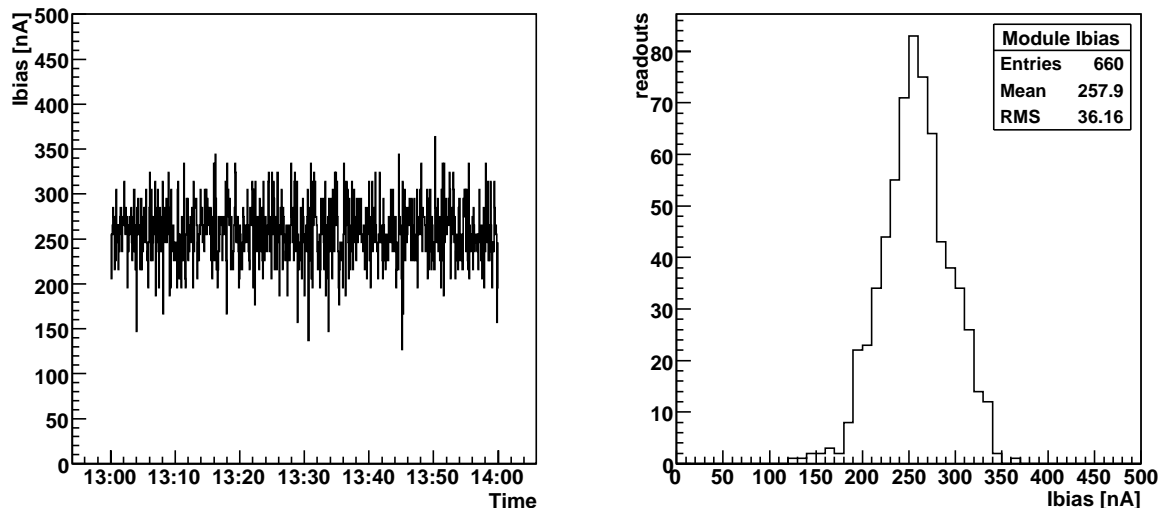


Fig. 11. The bias leakage current during one hour of cosmics data taking. Left hand plot shows the Ibias as function of time, while the right hand plot shows a projection of this data onto the y-axis.

tronic readout hardware, are set directly to their nominal values

- (2) From STB to ON. HV is ramped to 150V and LV voltages are set to nominal levels ($V_{dd} = 4.0V$ and $V_{cc} = 3.5V$. The module is ready to be configured.
- (3) Module configuration. At power up, various registers of the ABCD chips used on SCT detector modules come up in an undefined state. It is only after the chips have been configured, by the DAQ sending a serial bit-stream to the modules, that the power dissipated by each module reaches the nominal value. The module is now ready for physics.
- (4) Temperature stabilized. The module runs in physics mode and data is read out. Heat dissipated by the module is being removed by the evaporative cooling system.

During barrel and end-cap reception and later combined testing the SCT detector was run in "warm mode" meaning that the hybrid temperature was kept at $27\text{ }^{\circ}\text{C}$ ². Figure 13 shows the module temperature as measured by the ther-

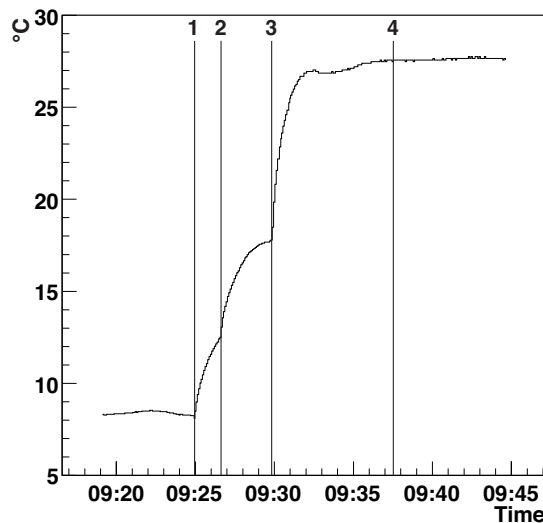


Fig. 12. Module switch on and preparation for data taking involves several steps during which the temperature of the module gradually rises.

mistor mounted on the hybrid upper side for the same module and same physics run as presented in figure 11. The temperature readings show a nice regular pattern where the temperature oscil-

² Contrary to operation within the ATLAS where the SCT detector will run in "cold mode" with hybrid temperatures at 0°C

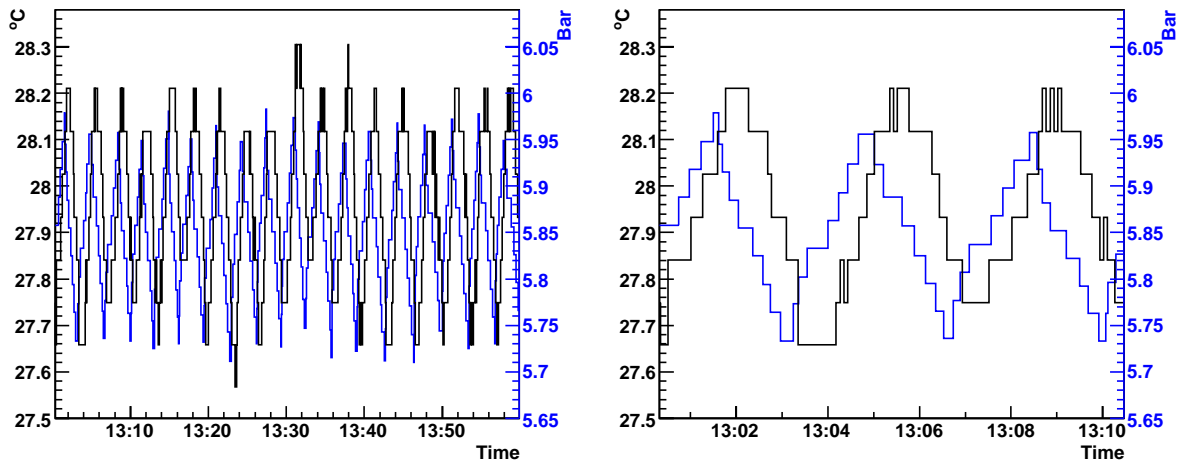


Fig. 13. Module temperature fluctuations (black line) and the corresponding back pressure readings (blue line). The right hand plot shows a ten-minute blown up view of the left hand plot which extends over an hour.

lates with an amplitude of $\sim 0.2^\circ\text{C}$ and period of ~ 5 min. This is found to coincide with the same oscillations in the back pressure of this loop, as seen on the same figure. This shows that the modules are closely coupled to the cooling pipe, and hence sensitive to variations in its temperature.

3.2. Interlock event in the detector

On the 4th of April 2006 there was an unfortunate accident where the capillary feeding a cooling half loop on barrel 6 became partially blocked by debris present in the cooling system as a result of an earlier pump failure. In the absence of the heat load produced by the modules, the loop appeared to be behaving normally. When the modules were powered, there was insufficient fluid flow to cool them: the module temperatures rose quickly until the safety interlock activated to cut the power off. This event is shown in figure 14: the temperature of module Z=-3 never reaches a stable value and is interlocked while still showing a steep gradient.

The interlock system worked reliably throughout the tests. In the early phase of the macro-assembly, several high temperature interlocks were triggered due to a blocked inlet to cooling loops, a problem that was later solved by inserting proper

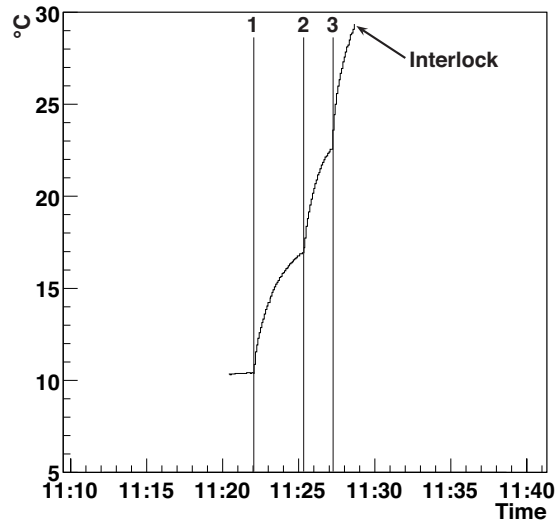


Fig. 14. The temperature of module Z=-3 on the blocked cooling pipe when the module is switched on and there is an insufficient flow of cooling fluid. The temperature rises steeply and does not stabilize before the modules is interlocked by the interlock system.

filters for the coolant. The sensors on the cooling loops responded faster to the cooling problem than the overheating protection programmed into the microprocessors in the power supply crate. The

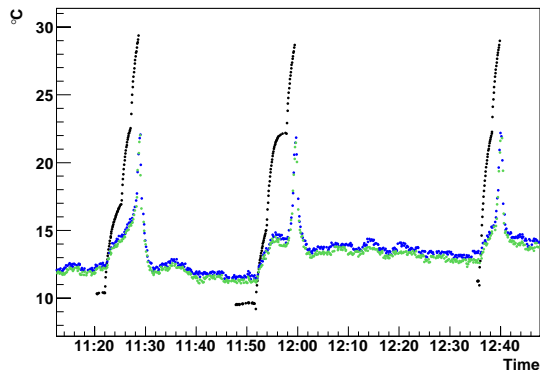


Fig. 15. Module temperature (black dots) and cooling pipe temperature (blue and green dots) showing the interlock incident

probable reason is that the low mass of the cooling pipe give a more rapid temperature rise than on the silicon detector module. Figure 15 shows a series of overheating incidents where temperature rise rapidly when cooling fails; when interlock is activated the temperature returns to normal.

3.3. DCS Performance

Running 1/8 of the detector together with all services during the commissioning and the cosmic tests allowed for studying the performance of the DCS. CAN bus performance was evaluated separately for the different projects as the data traffic varies substantially between the them.

For the ELMB, sending one message on the CAN bus at a baudrate of 125 kbits/s takes 0.7 ms. Hence, a delay between two messages of 0.9 ms leads to 100% occupancy. However, for safe operation the occupancy should be less than 60%. The maximum number of ELMB nodes on each bus at a baudrate of 125 kbits/s will be of 32 [23]. For the Envr project, the number of ELMBs was never higher than 6, with a baudrate of 250 kbits/s resulting in a good performance of the system and allowing a 5 seconds delay only between readings.

For the power supply project the maximum bus load of 60% is generated by 4 crates sending data simultaneously. When there is more than 4 CC nodes, the high rate of data transmission causes a 'traffic jam' on the CAN bus. To prevent this situ-

ation, an inhibit time parameter was implemented in the CC. This is a counter with a 100 ms resolution, which inhibits the next readout transmission for a period of time. Optimal settings of the inhibit times for nodes connected to one CAN bus were sought and found to be 0 ms delay for crates 0-4, 1000ms delay for crates 4-8, 2000ms delay for crates 9-11 etc. Taking into account time needed for sending data from one crate (800 ms) and inhibit times set in the system, it was found that for a minimum readout time of 4 - 5 seconds no more than 11 CC nodes could be connected to the same CAN bus.

A separate issue of the system performance was the huge CPU consumption on the DCS computer. The CPU usage raised rapidly when collecting the data after a SYNC message. This effect was mainly related to the PVSS internal archiving and also due to the alert archiving. The problem of the internal archiving was later solved for the end-cap tests while the alerts were simply not used (see below). On the figure 16 the periodic spikes on CPU related to SYNC are shown for the OPCserver and for PVSS plus the OPCserver.



Fig. 16. CPU consumption of the MoPS project PC during barrel cosmics run. The plot shows regular peaks at 100% with a period corresponding to the MoPS reading rate (15 seconds).

Usage of alerts within the MoPS project was not possible during the macro-assembly phase. This was due to an internal mechanism of the software which tried to save all alerts to an archive file. The number of alerts being active at the same time in the MoPS project being large, the archive file size would eventually increase enough to make the

project crash. As this was a severe performance issue, the alerts were not used for this period.

The PS hardware performance can be discussed in terms of the switching on/off speed and the trip rate. The ramp down speed of one crate is defined by the ramping speed chosen by the user and by the time it takes the CC to send the commands to all the channels. It takes 6 seconds from the first channel starts ramping until the 48th channel starts. Since the crates are all independent, this value does not vary with the number of crates on the bus. For this reason the total time to shut down all crates on one bus is not much more since the total amount of messages will be equal to the number of crates, which gives a maximum of 11 messages. Cosmic runs allowed for studies of low level hardware trips, which typically occurred after long period of running the PS system. Occasional LV and HV trips not related to the detector conditions were solved in the PS firmware. The intercommunication between the different DCS projects is defined by the ethernet speed. Since the SCT DCS will be on a dedicated local network there should be no reason for this to be slow or fail.

Combined tests were an excellent opportunity to develop and test more efficient data handling strategies. The volume of DCS data was also to be evaluated. As explained in section 2.5, no deadband was used for the barrel tests. This resulted in a tremendous amount of data stored in the offline database (18 GB for 3 months of data taking). For the end-cap tests, the deadbands were enabled and the improvement is clearly visible: 2 GB of data stored for 1.5 month of data taking. The data removed in the smoothing process is due to noise fluctuations in the readings from the hardware and is therefore not desirable.

4. Conclusion and Outlook

The first large scale test of the DCS for the SCT was done during the macro assembly and commissioning phase prior to installation into the ATLAS detector. The highest priority for the system was to secure safe operation of the SCT but the assembly and commissioning phase was as well an ideal

test bed to study the architecture and performance of the DCS.

The tests show architecture of the system meet the requirements in speed and configurability. The concept of loading settings and alarm levels from the database to the memory of the crate controller of the large power supply system before operation through state transition proved to operate well. The response time to complete a state transition was only a few seconds and because of the distributed architecture insensitive to upscaling of the system. The DCS system was partitioned to give an update rate for the future full SCT system with around 100 000 monitoring parameters of less than 10 seconds.

The functionality of the database was studied. The use of condition database was tested and used for regular running. The parameters were throughout the tests archived either in the local PVSS database and later to an Oracle database and transferred to the central conditions database COOL at CERN. The conditions database was only tested in view of an implementation in the final system.

The DCS system provided the needed protection for the detector. In addition of the safety protection supplied by the software and firmware a fully hardware based interlock system provided the ultimate protection against fatal overheating of the detector. The interlock system was activated a few times during the commissioning due to blockage of the cooling system and was correctly turning off the power to the silicon detector modules before overheating. The monitoring of the SCT environment for temperature and humidity functioned without interruption throughout the commissioning phase.

At the time of the test no Finite State Machine was implemented which is needed for running the full SCT DCS. The development of the FSM was started during the tests and will be finalised in parallel with the commissioning of the SCT in the ATLAS detector. The SCT DCS will be split in 11 partitions: two for the environmental project, eight for the power supply project and one sub-detector control station. The designed DCS system will provide a fast and reliable system for a safe operation of the SCT in ATLAS.

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