A setup for electronic tests of ATLAS silicon strip detectors

Candidatus Scientiarum Thesis

by

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September 2001

Preface

The main purpose for this thesis was to build up a readout system for silicon microstrip detectors, used for the evaluation and testing of single detectors, and the functionality of the SCTA128HC readout chip.

I found this project very interesting during the entire process, due to the constant increase of knowledge and learning. As work progressed during this year, I have gained experience in: Making engineering drawings for metal framework, using huge LabVIEW programs, understanding of VME and NIM modules, making double-layer PCBs, onboard soldering, using the PCI-MXI/VME-MXI (the interface between the VME crate and the PC terminal), sending and receiving signals to the SCTA128HC readout chip, reading out silicon detectors, getting help form the web, but most of all searching for errors in software and hardware by using different programs, writing debugging programs, and actively use of the oscilloscope for debugging.

While travelling five times to CERN, I found myself hurled into a huge, ongoing project with participants from all over the world, where I learned about a broad range of topics concerning the project of this thesis. I learned about the technical details, requirements, limits and methods to overcome these limits. I also gained a lot of experience about the administrative side, about the never-ending stream of suggestions, decisions, meetings and comparisons necessary to keep such a huge project moving along the right path.

I wish to thank my supervisor and spellchecker Bjarne Stugu for his guidance and direction, and for making this thesis possible, and Lars G. Johansen for helping me with all the how, why and where's. Furthermore I would like to thank Dave Robinson for answering 23 extensive mails concerning his LabVIEW program and setup. I also want to thank my Rannveig for her care and understanding.

Bergen, September 2001

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Bjørn Pommeresche

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List of abbreviations, acronyms and terminology

ADC	Analog to Digital Converter, a device for converting an analog electric signal to digital form, so it can be subsequently stored and processed by the computer.
ALICE	A Large Ion Coillider Experiment
ATLAS	A Toroidal LHC ApparatuS, one of the general proton-proton detectors for the Large Hadron Collider
BCO	Bunch Cross-Over
CERN	Organisation européenne pour la recherche nucléaire
CMS	Compact Muon Solenoid
ECL	Emitter Coupled Logic circuit. ECL circuits use bipolar transistors biased in the active region. They are a very fast high-power digital technology commonly used in logic circuits.
EEPROM	Electronically Erasable Programmable Read Only Memory
Fan-in	The number of electrical loads present by an input pin to the driving device. Applies to macros within an array or to discrete devices.
Fan-out	The number of components to which a signal is connected.
LEP	Large Electron Positron collider
LHC	Large Hadron Collider
MITE	A National Instrument custom ASIC, a sophisticated dual-channel DMA controller that incorporates the Synchronous MXI and VME64 protocols to achieve high-performance block transfer rates.
MXIbus	Multisystem eXtention Interface Bus; a high-performance communication link that interconnects devices using round, flexible cables
PCB	Printed Circuit Board
Pedestal	In a detector element, a value measured when no signal is present. Must be subtracted from the raw reading to get the true signal.
PMT	PhotoMultiplier Tube
SCT	Semi Conductor Tracker
SIROCCO	SI-strip Read Out Camac Controller.
SNR	Signal to Noise Ratio
TDC	Time to Digital Converter
VXIbus	VMEbus eXtensions for Instrumentation

1 Introduction and Overview

1.1 CERN

In the middle of the twentieth century, the European physicists understood that they had to follow the US path to get back their leading position in basic science research. No countries in Europe had the money or expertise to do this, so they had to cooperate to reach this goal. In 1953, 12 countries of the multi-international and European organisation called "Conseil Europeen pour la Recherche Nuclaire" signed a convention to together build a laboratory called CERN.

CERN, the European Organisation for Nuclear Research, is an organisation for research mainly targeted at sub-nuclear physics. It is situated on the border between Switzerland and France, approximately 10 km outside the city of Geneva. CERN will celebrate its 50^{th} anniversary in the autumn of 2004. From the very beginning, it has had a leading edge in the field of experimental particle physics, and there have been many industrial and technical offshoots from these activities over the years: Cancer therapy, medical and industrial imaging, radiation processing, electronics, measuring instruments, new manufacturing processes and materials, food preservation techniques, destruction of toxic products, and not to forget the World Wide Web which is one of the more recent, well known examples.

The core of the CERN activities is, and always has been, the particle accelerators and their detectors. One of the first experimental machines built at CERN was the Proton Synchrotron (PS). It accelerated and provided protons for fixed target experiments at a beam energy of 26 GeV. Over the years several accelerators and detectors have been built. As old accelerators have become outdated, they have frequently been transformed into pre-stages of newer, more powerful accelerators. The PS is thus a pre-stager for the SPS and the LEP accelerators. With a centre of mass energy up to 900 GeV, the W and Z bosons of the weak interaction were discovered at the SPS, thus giving important confirmation of the electroweak theory and a Nobel Prize.

The planning of another new machine started as early as 1977, i.e. before the SPS was in operation. This machine was called LEP, the Large Electron Positron accelerator. The reason for choosing $e^{\pm}$ as the accelerated particles was mainly to be able to study the production of the Z boson (with a mass of approximately 90 GeV) from electron-positron annihilation. The need for high beam energy dictated a large-radius accelerator, especially since electrons and positrons were to be accelerated. A charged particle in a circular orbit radiates energy according to the energy-loss equation:

$$\Delta E \propto \frac{E^4}{r \cdot m^4} \tag{1-1}$$

where r is the radius of the orbit, and m is the particle mass. With their low mass, electrons loose a large fraction of energy per turn, and to compensate a big radius is needed.

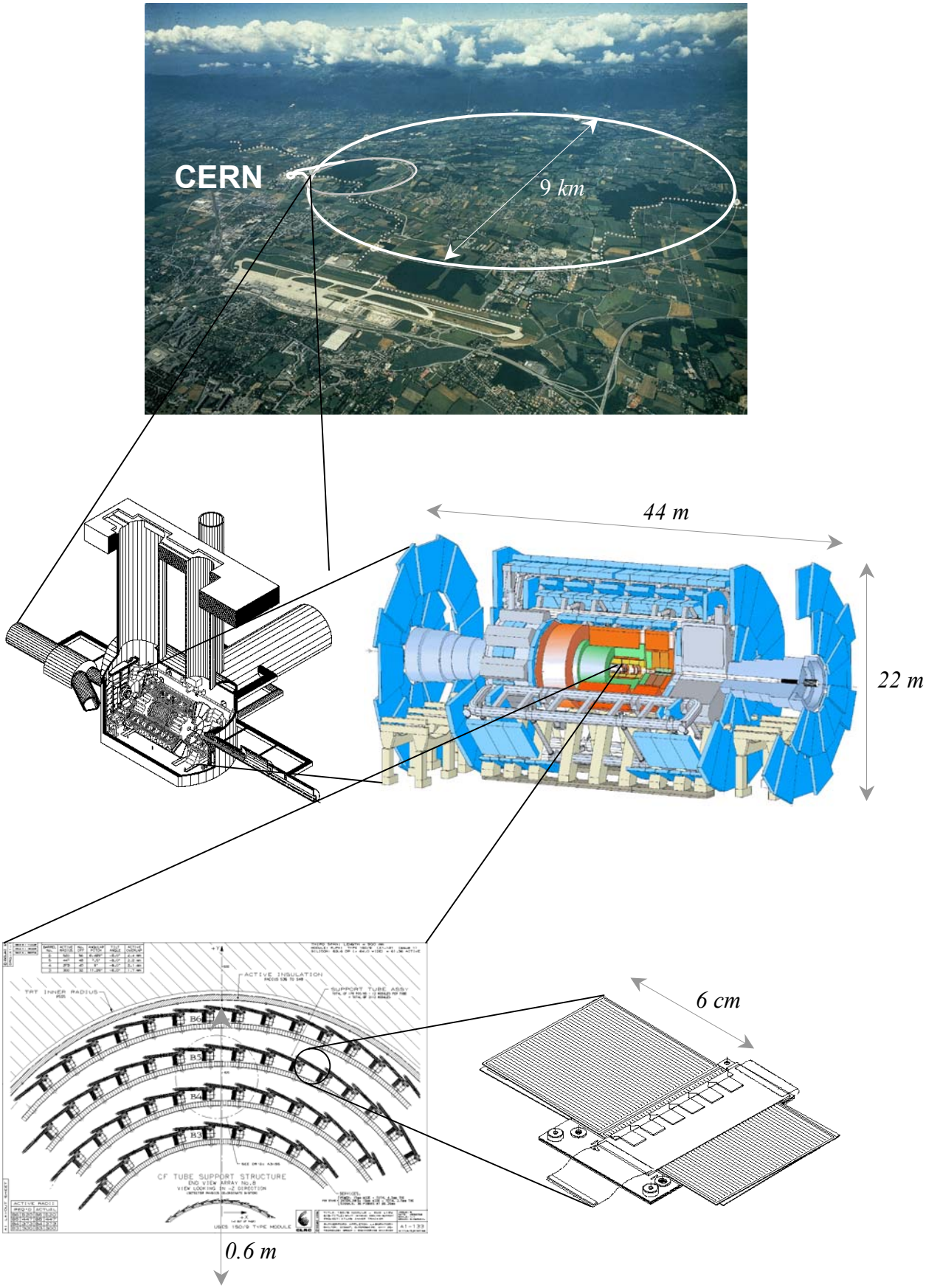

Figure 1 Introduction and Overview

To house the LEP, a circular tunnel, 3.8 m wide and 27 km long, was drilled. The tunnel is situated 100 m below French and Swiss countryside, and took 8 years to complete. Following the philosophy of re-use and cost efficiency, space was provided for two accelerators inside the LEP ring when it was built (LEP itself and a future accelerator, not yet planned at the time) [1].

LEP has proved an invaluable source of experimental data to test the Standard Model to very high precision. It has successfully searched for particles in the energy range up to approximately 115 GeV. While 209 GeV (i.e. 104.5 GeV/beam) represented a substantial leap in beam energy and thus "exploration potential", it is still not enough to exhaust the Standard Model. Now LEP has closed down for good, and is being dismantled. The last beams were dumped at 8 a.m. on the 2nd November 2000.

Even higher energies are needed to search for heavier particles. This includes the search for the Higgs boson, which is predicted by the Standard Model, but still remains undetected. Other topics of interest in the energy-regime of 1 TeV would be the search for particles predicted by Grand Unification Theories and supersymmetry. The Large Hadron Collider LHC is the machine designated to undertake these jobs.

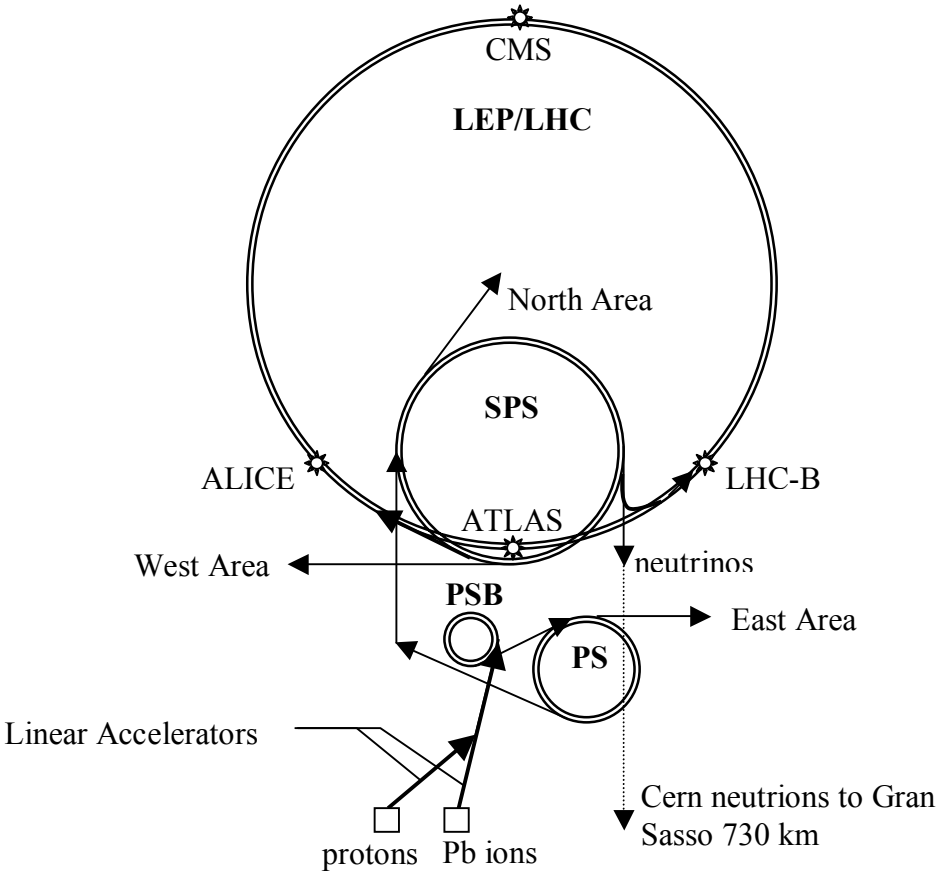

Figure 2 Schematic diagram of the CERN accelerator complex

1.2 LHC

The Large Hadron Collider (LHC) is a proton-proton collider with 14 TeV centre of mass energy, and design luminosity of $10^{34}cm^{-2}s^{-1}$. Beam crossing are 25 ns apart, and at design luminosity there are 23 interactions per crossing. Because the charged particles used in the LHC are protons instead of electrons, the LEP tunnel is sufficiently large enough to accelerate the particles to the required energy. Existing particle sources will be used as preaccelerators. To build LHC one has to use very advanced existing technology, and new technology must be developed. LHC will use the most advanced super-conducting magnet and accelerator technologies ever developed.

There are four detectors proposed for the LHC project, these are:

- ATLAS, A Toroidal Large hadron ApparatuS. High luminosity proton-proton detector.
- CMS, The Compact Muon Solenoid. High luminosity proton-proton detector.
- ALICE, A Large Ion Collider Experiment. Study the ion-ion collisions.
- LHC-B, Serve B-physics studies.

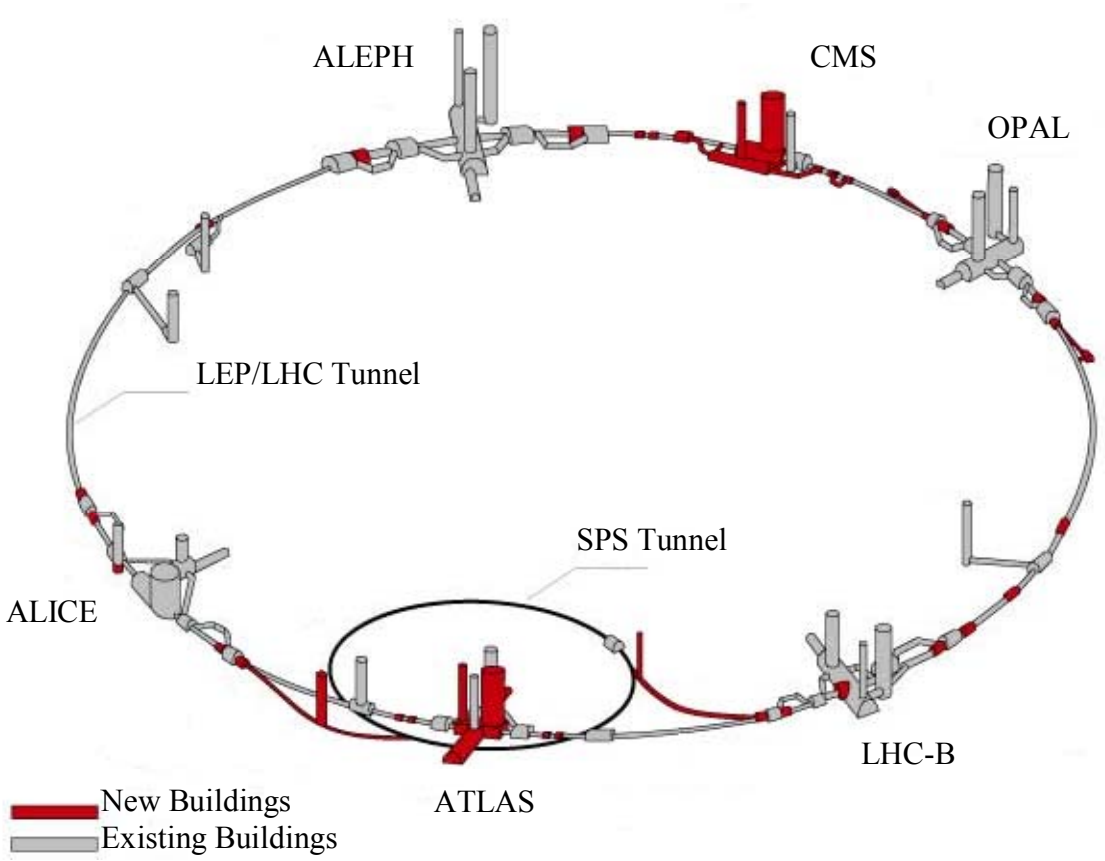

Figure 3 Schematic overview of the LHC Accelerator

LHC will occupy the same tunnel as LEP presently occupied, but with its own beam pipes and detectors. The idea originally was to put LHC on top of the LEP beam-pipe. However, this turned out to be too expensive. This removes the option of e - p collisions, which originally were planned. Instead, enough room is kept free over the LHC installation that a lepton ring can be installed there in the future, possibly using LEP components.

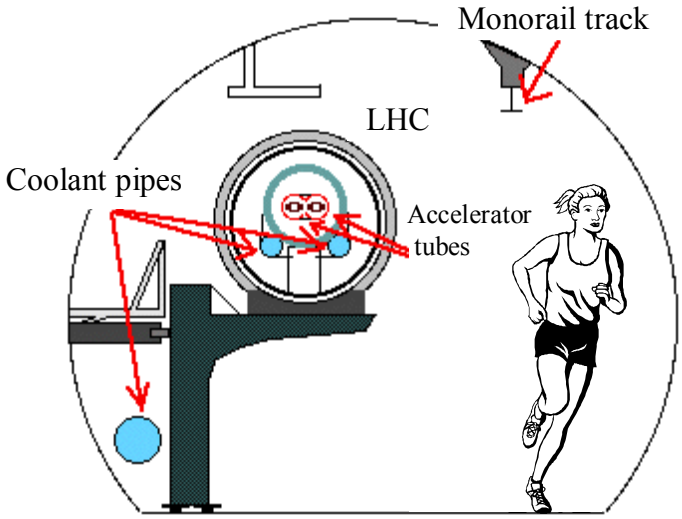

Figure 4 Inside the 27 km long LHC tunnel

Physicists have high hopes for interesting new physics at energies around 1 TeV. Therefore, a centre-of-mass energy sufficiently high to produce particles in that range is planned for LHC. Furthermore, very high luminosity is needed. When looking for new particle interactions, it is important to be able to extract very subtle effects for the data, effects that may only occur seldom and /or produce a small signal over a large noise-background. The higher the luminosity, the more data can be gathered in a given time. Basic design parameters for the LHC machine are listed in Table 1 [2].

Specification	Value	Unit
Energy per beam	7,0	TeV
Dipole field	8,38	T
Luminosity	10^{34}	$cm^{-2}\ s^{-1}$
Bunch spacing	25	ns
Bunches per beam	3600	
Particle per bunch	1×10^{11}	
Stored beam energy	332	M Joule
Beam life time	22	H
Radiated power per beam	3.7	KW

Table 1 Basic design parameters for the LHC machine

Experiments at high energies are necessary to make advances in particle physics. In this century, development in physics has followed a path were theorists and experimentalists have taken turns pushing our understanding of the processes we study into deeper levels.

One of the main reasons for this is probably that experiments are built to test the predictions of theories, and that theories often are constructed to explain some unexpected results from an experiment. LHC is the most powerful experimental machine yet to emerge from this interplay between theory and experiment.

1.2.1 LHC Magnets

The proton bunches circulate through the rings (beam pipes) in opposite directions. The purpose of the ring is to keep the particles on a circulating path, providing multiple accelerations of the same particles. Protons circulating around the pipe radiate energy. The reason for this is the change in the velocity due to the bending of the path. The amount of energy lost in this manner increases both with the energy of the particle, and the curvature of the beam pipe according Eq. (1-1).

The LHC accelerator operates with two kinds of electromagnets. Super conducting magnets will be used to guide the particles around the ring. The super-conducting magnet technology has allowed us to obtain higher magnetic fields than in conventional magnets, and thus higher particle energies. When a proton has the energy of 7 TeV, its fraction of speed of light 0.999 999 991, which means only 9,71 km/h from the speed of light.

In order to keep the 7 TeV protons in the ring, the LHC dipole magnets must produce a magnetic field of 8,36 Tesla. In order to obtain superconductivity, the LHC magnets will be operated at 1.9 above absolute zero (1.9K). The numbers of dipole magnet will be 1,296 each of 14.2m. The other magnet type is quadrupoles that focus the particles along the beam and prevent them from straying [3].

1.2.2 LHC Cooling

It is very important to keep the system at low temperature. The cryogenic system choosed for LHC is foreseen to use super-fluid helium, which has unusually efficient heat transfer properties, allowing kilowatts of refrigeration to be transported over more than a kilometre with at temperature drop of less than 0.1 K. The LHC's super-conducting magnets will sit in a 1.9 K bath of super-fluid helium, flowing in heat exchanger tubes threaded along the string of magnets. The reliability and efficiency of this sophisticated cryoloop are key factors in achieving the required magnet performance.

The magnet coil is indirectly cooled with forced flow of two phases helium through a single pass cooling tube. The coil can be cooled down to 4.5 K in 100 hours with a helium mass flow of 20 g/s, by keeping the maximum temperature difference in the coil below 40 K. The LHC cryogenic system is very large as well as very cold. Refrigeration power equivalent to over 140kW at 4.5 K is distributed around the 27 km ring. During the initial cool-down of LHC 12 million liters of liquid nitrogen will be vaporised to cool-down 31,000 tons of material. And the total inventory of liquid helium will be 700 000 liters [4].

2 ATLAS

ATLAS is an achronym for A Toroidal Large Hardon collider ApparatuS. The experiment is being constructed by 1850 collaborators in 150 institutes around the world. The installation of Apparatus is expected to start in the beginning of 2003, and data taking will begin with a four-week pilot run in April 2006, followed by a seven months physics run starting August 2006. ATLAS is designed to improve our fundamental understanding of matter and forces. (A prime physics goal of ATLAS is to understand the nature of mass.)

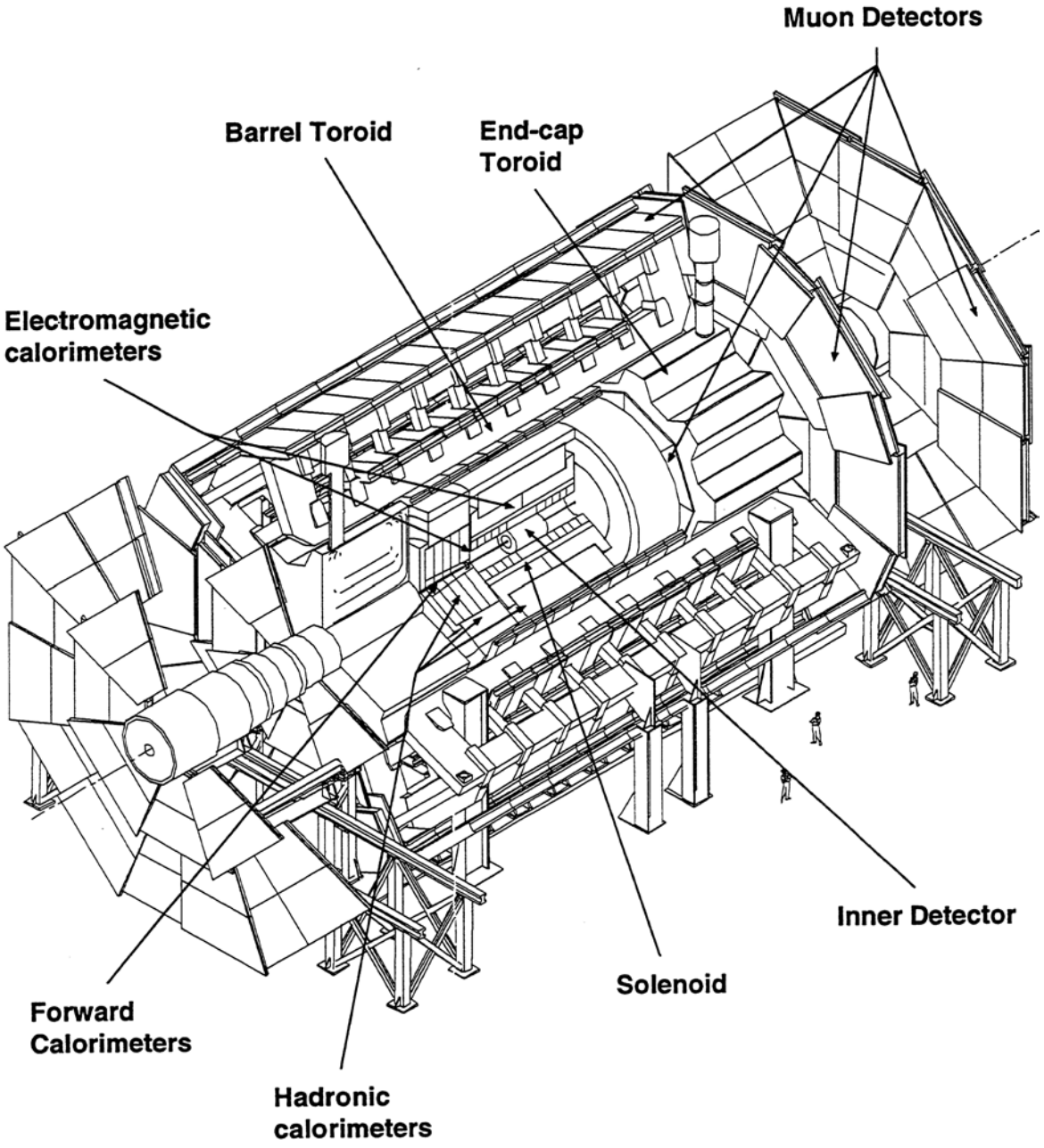

Figure 5 The ATLAS detector for LHC

The ATLAS detector consists of four major components:

- Inner detector - measures the momentum of each charged particle
- Calorimeter - measures the energies carried by the particles.
- Muon spectrometer - identifies and measures muons.
- Magnet system - bending charged particles for momentum measurement.

The interactions in the ATLAS detectors will create an enormous dataflow. To digest this data we need:

- Trigger system- selecting 100 interesting events per second out of 1000 million others.
- Data acquisition system- channeling the data from the detectors to the storage.
- Computing system- analyzing 1000 Million events recorded per year.

The LHC offers a large range of physics opportunities, among which the origin of mass at the electroweak scale is a major focus of interest for ATLAS. Physics issues such as sensitivity therefore guide the detector optimisation to the largest possible issues such as sensitivity to the largest possible Higgs mass range. Other important goals are the searches for heavy W- and Z-like objects, for supersymmetric particles, for compositeness of leptons and quarks, as well as the investigation of CP violation in B-decays, and detailed studies of the top quark. The ability to cope well with a broad variety of possible physics is expected to maximize the detector's potential for the discovery of new, unexpected physics. The physics potential for ATLAS can be summarized as follows:

- Higgs particle
- New Gauge bosons
- Super symmetric particles
- Heavy ion physics
- New phenomena beyond the Standard Model

See [5] chapter 11 for more details. The total material cost for the detector with the manpower for industrial products and industrial support included amounts to 450 MCHF. The Inner detector system has an estimated total cost of 78 MCHF, and the overall cost uncertainty of adding the cost uncertainties is estimated at 26 MCHF. The support needed for the design, testing, assembly and installation of the detector in terms of engineers, technicians and other staff to be provided by the laboratories has been estimated to about 2500 persons-years [5].

2.1 ATLAS Detector

The purpose of the ATLAS detector is to measure whatever happens after the high energy proton-proton collision provided by the LHC accelerator. Over a large part of the parameters space to be explored at the LHC, the cross sections for the physics processes to be studied with the ATLAS are small. In other words, most of these processes are very rare. For instance, only one proton-proton inelastic interaction in $\sim 10^{13}$ would result in a Higgs boson decaying into 4 leptons. This explains the need of high luminosity. It is also important with a detector providing as many signatures as possible (electron, gamma, muon, jet and missing transverse energy measurements). The wide selection of signatures is important to achieve solid and unambiguous physics results.

Outside the inner detector, which is widely explained in chapter 2.2, there is the highly granular liquid-argon electromagnetic sampling calorimetry, followed by a liquid-argon hadron calorimeter. This is surrounded by the muon spectrometer that defines the overall dimensions of the ATLAS detector. Figure 6 shows the different layers and where the different particles are detected.

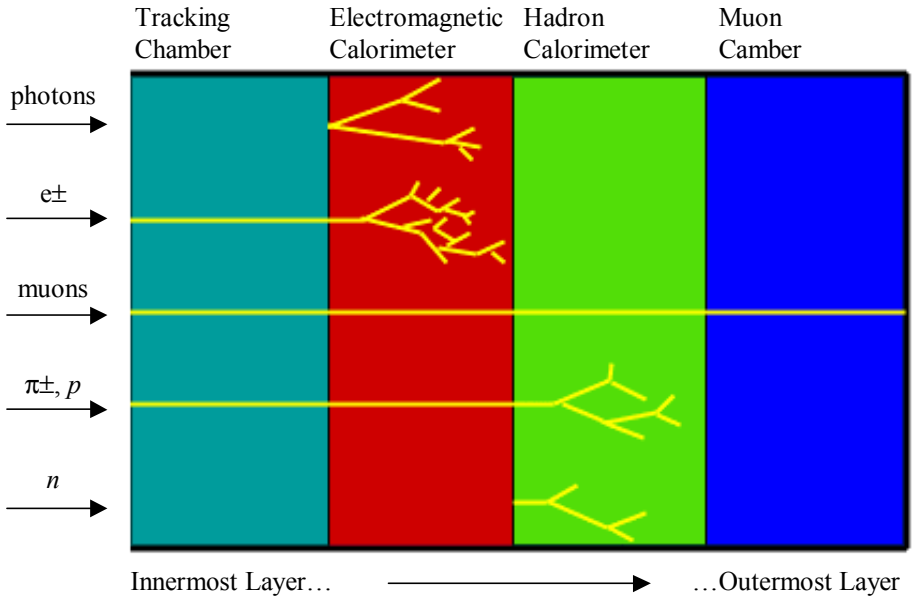

Figure 6 Decay Chart for ATLAS

The outer chambers of the barrel are at a radius of about 11m. The length of the barrel toroid coils is 26 m, and the third layer of the forward muon chambers, mounted on the cavern wall, is located at ±21 m from the interaction point. The overall weight of the ATLAS detector is about 7 000 tons [6].

2.2 Inner Detector

The inner detector is contained within a cylinder of length 7 m and radius 1.15 m, with a solenoidal magnetic field of 2 T. The inner part takes care of pattern recognition, momentum and vertex measurements, and enhanced electron identification are achieved with a combination of discrete high-resolution pixel and strip detectors in the inner part, and continuous straw-tube tracking detectors with transition radiation capability in the outer part of tracking volume. The highest granularity is achieved around the vertex region using semi-conductor pixel detectors. The total number of precision layers must be limited because of the material they introduce, and because of the high cost. Typically, three pixel layers and eight strip layers (four space points) is provided by the Pixel and the SCT systems. The straw tube tracker (TRT) provides continuous track-following with much less material per point, and lower cost. The combination of the two techniques gives very robust pattern recognition and high precision in both φ and z coordinates [6]. The inner detector is divided in three subsystems: Pixel detector, Strip detector (SCT) and Transition Radiation Tracker (TRT), shown in Figure 7.

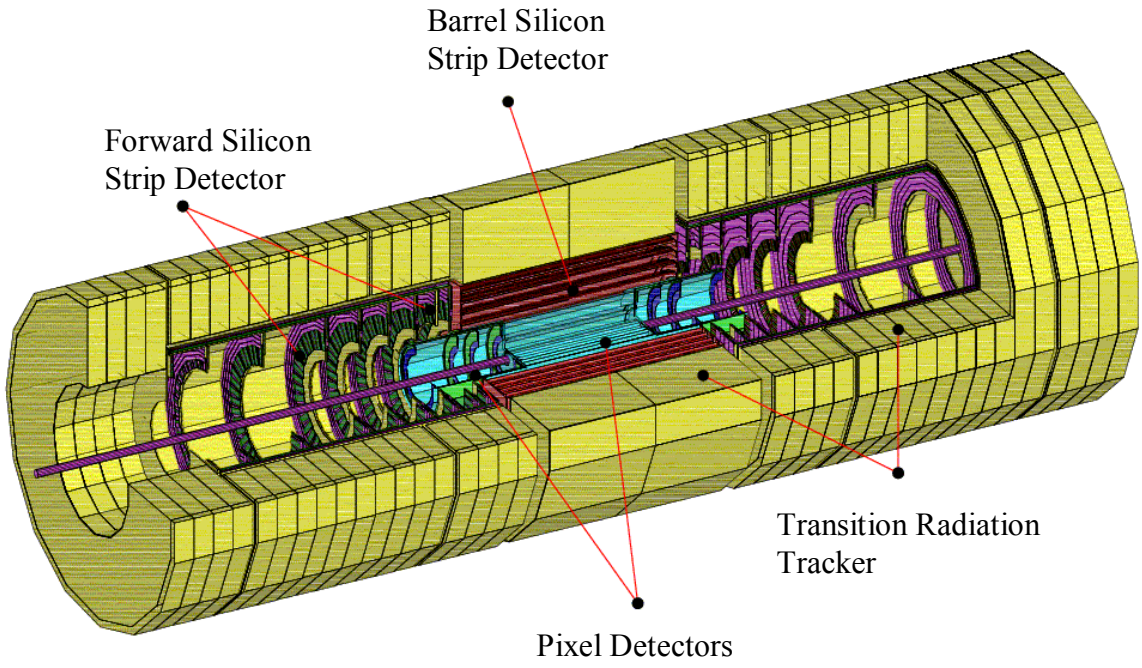

Figure 7 Sketch of the ATLAS Inner Detector

2.2.1 Pixel Detector

The pixel detector is designed to provide a very high-granularity and high-precision set of measurements, as close to the interaction point as possible. The system provides three precision measurements over the full acceptance, and mostly determines the impact parameter resolution, and the ability of the Inner Detector to find short-lived particles such as *B* mesons and τ leptons. The two-dimensional segmentation of the sensors gives space points without any of the ambiguities associated with crossed strip geometries, but requires the use of advanced electronic techniques and interconnections for the readout. The readout chips are of large area, with individual circuits for each pixel element, including buffering to store the data while awaiting the level-1 trigger decision. Each chip must be bump bonded to the detector substrate in order to achieve the required density of connections. In addition, the chips must withstand over 300 kGy of ionizing radiation, and over $5x10^{14}$ neutrons per cm^2 over the ten years of operation. The system contains a total of 140 million detector elements, each 50 μm in the $R\Phi$ direction and 300 μm in z, which are invaluable for the task of pattern recognition in the crowded environment of the LHC.

The detector contains 61 m^2 of silicon detectors, with 6.2 million readout channels. The spatial resolution is 16μm $R\Phi$ and 580 μm in z, per module containing one $R\Phi$ and one stereo measurement. Tracks can be distinguished if separated more than ~200 μm.

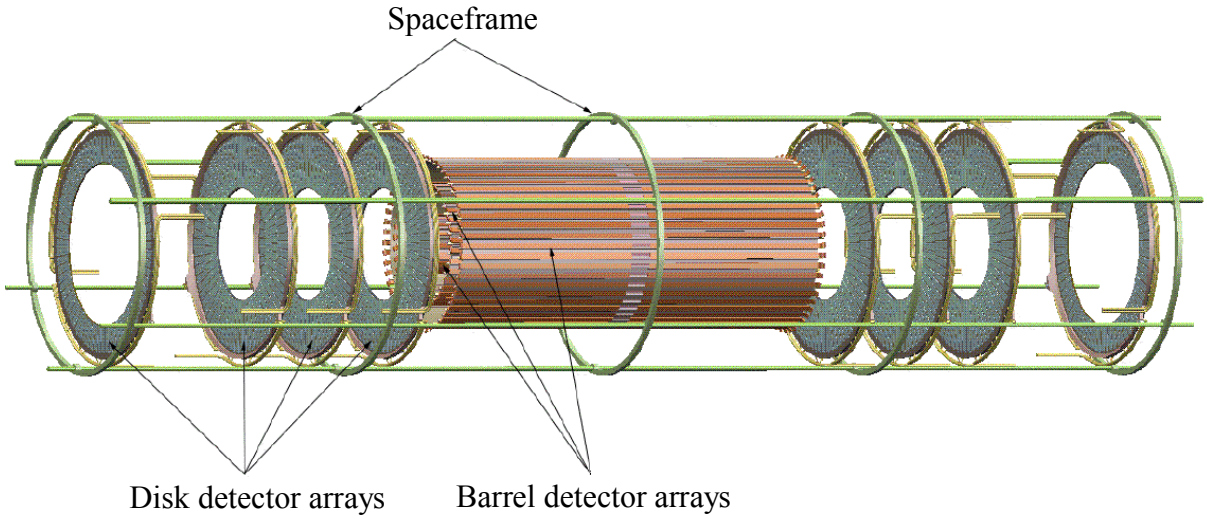

Figure 8 Pixel Detector

The system consist of three barrels at average radii of ~4 cm, 10 cm, and 13 cm, and five disks on each side, between radii of 11 and 20 cm, which complete the angular coverage. The system is designed to be highly modular, containing approximately 1 500 barrel modules and 700 disk modules, and uses only one type of support structure in the barrels, and two types in the disks.

2.2.2 Semi Conductor Tracker (SCT)

Each silicon strip detector is 6.36x6.40 cm^2 with 768 readout strips of 80µm pitch. Each module consists of four single sided p-on-n silicon detectors. On each side of the module, two detectors are wire-bonded together to form a 12.8 cm long strip. Two such detector pairs are then glued together back-to-back at 40 mrad angel, separated by a heat transport plate, and the electronics is mounted above the detector on a hybrid. The readout chain consist of a front-end amplifier and discriminator, for bowed by a binary pipeline which stores the hits above threshold until the level-1 trigger decision. All together summarised in Table 2.

Table 2 Barrel module parameters

Silicon outer dimension	63.56 mm x 128.05 mm (cut edge)
Construction	Four 63.56 x 63.96 mm p-in-n single sided sensors to form back to back glued sensors
Strip length	126.09 mm (2.090 mm dead in the middle)
Thickness	285 ± 15 µm (uniformity required to be ± 10 µm)
Strip directions	± 20 mrad (0, ± 40 mrad on support structure)
Number of readout strips	768 per side, 1536 total
Strip pitch	80 µm
Hybrid	two single side hybrids bridged over the detector
Hybrid power consumption	6.0 W nominal, 8.1 W maximum
Maximum detectors bias voltage	460 V (on the detector), up to 500 V in the module
Operating temperature of detector	- 7 ºC (average)
Uniformity of silicon temperature	< 5 ºC
Detector power consumption	1 W total at - 7 ºC, Heat flux (285 µm): 120 µW/mm2 at 0ºC
Thermal runaway	Heat flux: > 240 µW/mm2 at 0 ºC
Radiation length	< 1.2 % X0

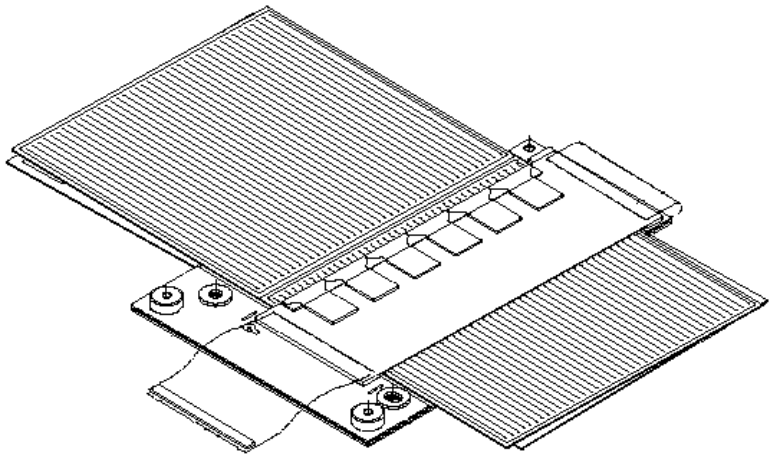

Figure 9 Configuration of the barrel module (consists of four silicon strip detectors)

The SCT modules are aligned in 4 cylindrical central barrels, and 9 forward and 9 backward disks with a total sensitive area of ~ 50 m^2. A total of 11 424 single sided silicon strip detectors are required for the four central barrel layers. A guiding principle has been to make the detector highly modular, and to minimize the number of different components required. All four cylinders are built from identical Rφ modules. In one proposed assembly scheme, 14 modules are first mounted onto a stave and then the staves are assembled into the cylinders. Alternate cylinders are built of *u* - *φ* and *v* - *φ* layers. A total of 2 856 modules will be required for the four barrel layer.

The front-end electronics produce a well localized large power density, which has to be removed before it can heat up the silicon detectors. The available surface area for cooling is less than 1 cm^2 per chip, and it is very delicate. The silicon detectors also dissipate power. This is exponentially dependent on the temperature, and can lead to situation where the silicon detector thermally runs away in a badly cooled area. Thermal expansion for different temperatures can move the detectors out of position, so there seems to be no end of engineering challenges. Figure 10 shows the barrel modules making the four barrel cylinders

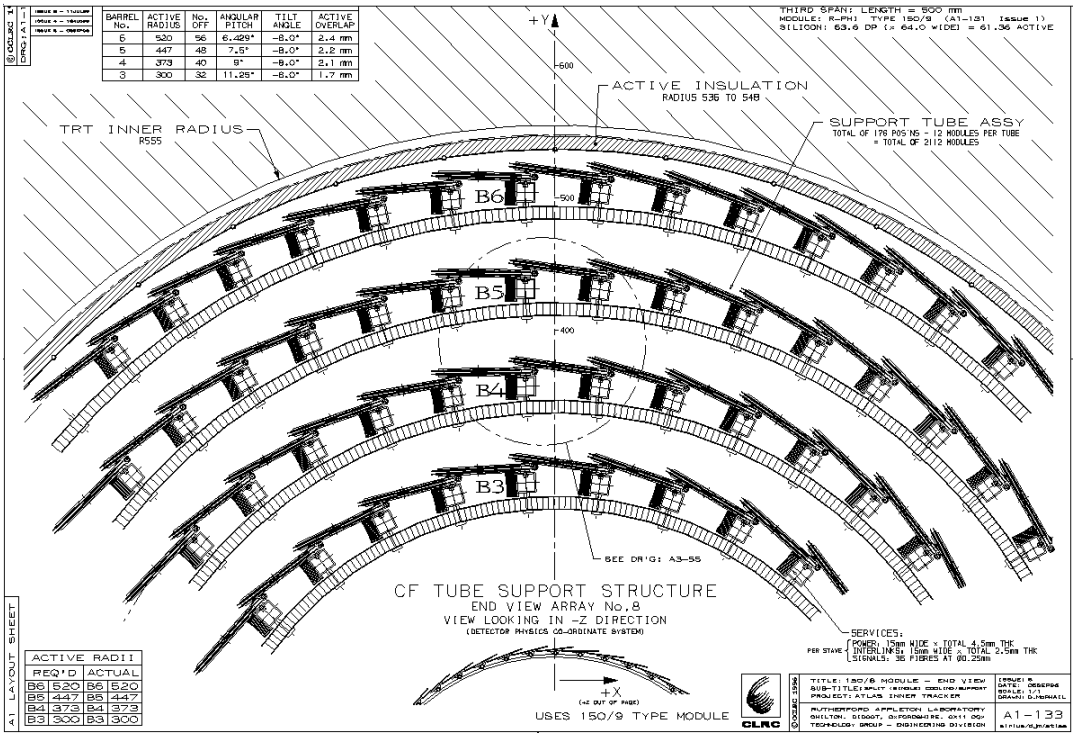

Figure 10 Structure of the SCT Barrel Section

2.2.3 Transition Radiation Tracker (TRT)

The TRT surrounds the pixel and the strip detectors, and are aligned both parallel and perpendicular to the beam direction. It consist of layers of straw detectors where each designed as 1 barrel with 52 544 axial straws of about 150 cm length, and 2 end cap parts with 319 488 radial straws of 39-55 cm length. The intrinsic radiation hardness and the low cost compared to other large volume tracking solutions, made this combined straw tracking and transition radiation detecting system very practical. The price to pay for these advantages is, however, a high detector occupancy with the 370 000 straws and 420 000 electronic channels. This system provides almost continuous tracking at large radii in the Inner Detector, due to its many measurement points. Each particle hits, on the average, about 36 straws [7]. The combined straw tracker and TRT, provides tracking and contributes to the electron identification over the whole inner detector rapidity coverage. Its pattern-recognition capability is strong due to the large number of measurement points, which will be combined to perform the momentum measurement together with the SCT precision detectors. The TRT can also provide an attend-alone momentum measurement, but with a lower precision than the whole inner detector. Layers of 4 mm diameter cylindrical drift tubes (straw detectors) are interleaved with radiators to produce and detect X-ray emission from very relativistic particles. The straw orientations are chosen to make optimal use of the 2 T axial magnetic field. The detector will be built in three different blocks, two end cap TRT's with radial straws and one barrel TRT with axial oriented straws. Hence the barrel TRT measures Rφ, while the end cap TRT measures φ and z [8].

2.3 Calorimeters

Calorimeters are used to determine the energy E of a charged or neutral particle by total absorption. The most important parameters for the calorimeter material are the nuclear absorption length and radiation length. The nuclear absorption length is the mean distance between inelastic collisions of hadrons with nuclei. Radiation length is defined as the distance over which the electron energy is reduced by a factor 1/e due to radiation loss only. Generally calorimeters are composed of heavy metal layers to produce a shower of particles. The metal layers are sandwiched between scintillators to measure the amount of particles that penetrate the metal layer. The interactions in the absorbers will transform the incident energy to a kind of shower of particles that are detected by the sensing elements. Complete calorimeters consist of two sub calorimeters:

Electromagnetic calorimeter EMC: The electromagnetic calorimeter consists of an inner barrel cylinder and two end caps, with the sensing element liquid argon. Because of the showers in the argon, the electrons will be freed and collected. The inner calorimeter is optimized for use in the measurement of electrons, and photons energy. Electrons and photons above 1 GeV interact with matter, principally through bremsstrahlung (energy loss by radiation) and pair production.

These processes create secondary photons and electrons, which interact correspondingly, producing a cascade of secondary particles, whose energies eventually fall below the region dominated by radiation loss, and dissipate their energy primarily through ionization. The signals can be measured in Liquid Argon cells when the shower particles ionize the Argon atoms.

Hadronic Calorimeter: The outer shell is called a hadronic calorimeter and it is optimized for hadroic showers. An outer barrel cylinder and two extended barrel sections makes the hardonic calorimeter. The Hadronic Calorimeter will be of the traditional sampling type, with sandwiched layers of iron and scintillator. The iron is the passive (absorber) material, in which the shower develops, and the scintillators are the active sampling layers measuring the ionization. When hadrons react with the iron layer, hadronic showers will be generated. Particle showers cause the plastic to emit light, which is then detected and recorded, further explained in chapter 4.2.

2.4 Muon Spectrometer

Muon detector is the outermost detector in ATLAS, it consist of a 26 m long barrel part with a inner bore of 9.4 m and an outer radius of 19.5 m, together with two end-caps with length of 5.6 m. The system consists of high precision tracking chambers and separated trigger chambers, operating inside a magnetic field generated by large superconducting air-core toroid magnets. In order to characterize a muon, the deflection of the muon in the magnetic field is measured.

Muons, which are charged leptons, are the “big brothers” of the electrons. While electrons are usually stopped in the electromagnetic calorimeter because they are so light, the 200 times heavier muons are heavy enough to escape the calorimeter. This due to bremsstrahlung being greatly reduced for charged particles with higher masses. Actually the cross-section for bremsstrahlung is inverse proportional to the square of the particles mass, so the radiation loss by muons is about 40 000 times smaller than for electrons. Unlike the τ (tau), which usually decays inside the tracker, the muon lives long enough to escape the calorimeter detector before decaying. Because of these properties, the special muon detector is needed to detect these particles, reconstruct and identify the muon tracks, measure their momenta, and provide information to be matched with data from the inner detector.

Only the neutrinos escape the apparatus without direct detection. But their existence can be deduced. The total energy of the proton proton collisions is known. By adding up all the energy deposited in the various pieces of the apparatus we can calculate, by using the principle of energy conservation, the missing energy. This missing energy will be the undetected neutrinos energy. The direction of neutrinos can be calculated by means of conservation of momentum.

2.5 ATLAS Trigger System

Bunches of particles will collide in the centre of ATLAS every 25 ns, generating a number of new particles. It means that each bunch uses 90 μs to travel around the ring. Thus there will be 3600 bunches in the ring at any instance, and the distance between two bunches with the same direction will be 7.5 m. The particles produced will travel outwards in the detector and interact with the transducer material, producing signals in all the different layers of the detector. As much as 1 000 particles might be produced per event, and these will cause a burst of signals in the detector. Up to 7 Terabyte of raw data per second is foreseen. This is ten times the data which is transferred through the telephone line if all the people in the world speak simultaneously in the telephone. It is of course impossible to continuously store that amount of data for later analysis. The trigger system works in real-time, and aims at filtering away as much data as possible form uninteresting events. The system is divided in three, with each stage working on a bigger part of the data from an event than the previous. The data are taken from evenly distributed locations in the Calorimeters and the Muon Detector. If the data look interesting, the event is kept, and sent to the slower 2nd level trigger. If not, the event is trashed. The idea is that the 1st level trigger (LT) should be a fast, but rather inaccurate judge of whether the event is interesting or not. The decision algorithm should be simple, fast, and conservative. It should keep all interesting events, but will also keep many events that will turn out to be uninteresting. The 1st level trigger also tries to identify so-called Regions Of Interests (RoIs). The system transfers all the events that the 1st level trigger accepts to the 2nd level trigger, together with information about RoIs. The 2nd level trigger extracts a bigger sample of data for the event to work on, and takes the data mostly form the RoIs. It is thus more accurate, but needs more processing time to arrive at a decision. The time it needs is available because the 1st level trigger has filtered away over 99% of the events. The same is repeated with the 3rd level trigger, except that the 3rd level trigger works on the full event, so it needs both much processing time and processing power [1].

3 Theory

3.1 Standard Model

The "Standard Model", a theoretical framework built to explain the properties and behavior of elementary particles, has been enormously successful in predicting a wide range of phenomena. Just as ordinary quantum mechanics fails in the relativistic limit, we do not expect the Standard Model to remain an excellent approximation to nature at distance scales as small as 10^{-18} m. This model describes the current theory of fundamental particles, and how they interact. Both the strong interactions due to the color of quarks and gluons, and the unified theory of weak and electromagnetic interactions (electroweak) are included in the Standard Model, whereas gravitational interactions are neglected.

In the Standard Model there are 12 fundamental particles and their corresponding antiparticles. Particles and antiparticles have identical mass and spin, the only difference is that they have opposite charges. There are two types of fundamental particles in the standard model, matter particles and force carriers. Matter particles are as shown in Table 3 separated in Leptons and Quarks.

Quarks	u up	c charm	t top	γ photon	**Force Carriers**
	d down	s strange	b bottom	g gluon	
Leptons	ν_e electron neutrino	ν_μ muon neutrino	ν_τ tau neutrino	Z Z boson	
	e electron	μ muon	τ tau	W W boson	

Table 3 Fundamental particles

Leptons: Leptons are fundamental particles that are not participating in strong interactions. There are 6 types of these where three of them are negatively charged, the electron (e), muon (μ) and the tau (τ), and the rest are electrically neutral particles, called neutrinos (ν). The best known lepton is the electron, which is stable. The only difference between the electron and the other remaining charged particles (muon, tau) is that they are more massive than the electron is. Neutrinos on the other hand, were until recently believed to be massless, but now experiments indicate non-vanishing neutrino masses. They are also very difficult to detect, because they only take part in weak interactions.

Quarks: We can find 6 types of quarks in the Standard Model. The up and down quarks that make up the proton (uud) and neutron (udd), and the strange, charm, bottom and top quarks that were present at the beginning of the universe, and which are now only produced in particle collisions. The difference between quarks and leptons is that quarks cannot exist alone (confinement), and are therefore found together with other quarks, to form hadrons. Hadrons are divided in baryons and mesons. Baryons are made from three quarks, and both the proton (uud) and the neutron (udd) are baryons. Mesons are made from one quark and one antiquark. Antiquarks have the same masses as the corresponding quarks, but with opposite charge. The electrical charges of quarks are - 1/3 or 2/3 in units of the proton charge (the electrical charge of the proton is 1.6 x 10^{-19} C). Quarks are smaller than the protons and neutrons, in fact only an upper limit can be set on their size. All six quarks have been produced at the accelerators, but the top quark is so massive that it took many years and very high energy accelerators to produce it (Fermilab in 1995) [1].

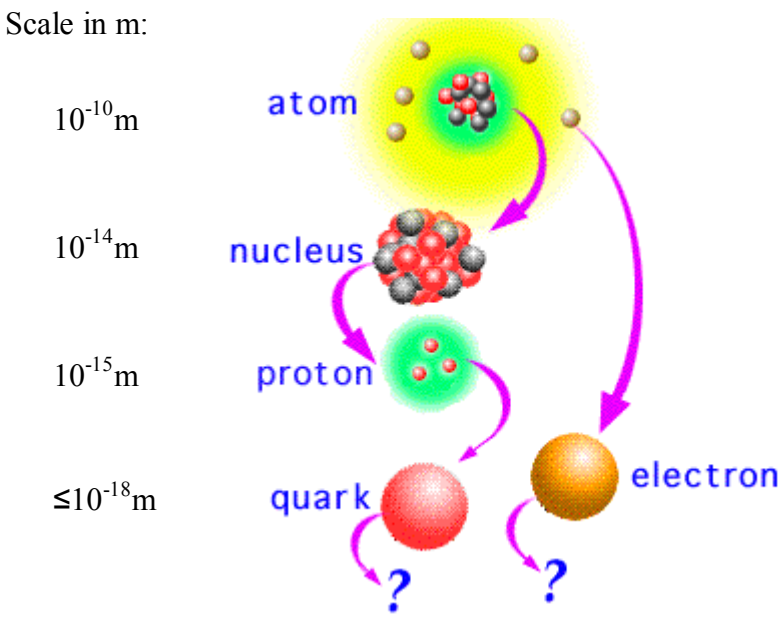

Figure 11 The scale of the different particles within the atom

3.2 Forces and their Particles

In the early 1960s particle physicists described nature in terms of four distinct forces, characterized by widely different ranges and strengths. These are: weak and strong nuclear force, electromagnetic force, and gravitational force. These forces have their own force-carrying particles. The weak force has a range of 10^{-17}m and the strong nuclear force has a range of 10^{-15} m, the electromagnetic and the gravitational forces have infinite range. The gravitational force is too weak to be observed in laboratory experiments, and the physicist have not discovered how to include it in a quantum field theory. Gravitational forces are therefore not yet included in the Standard Model.

Force carriers also called bosons are divided in four different categories, these are:

Gluons: Carriers of strong interactions. Gluons hold quarks in nucleons (protons and neutrons), and bind nucleons together to form nuclei.

Photons: Carrier particles of electromagnetic interactions. The electromagnetic forces binds electrons to the nucleus to form electrically neutral atoms.

W and Z bosons: Carrier particles of weak interactions. These particles are responsible for radioactive decay.

The Standard Model answers many of the questions of the structure and stability of matter with its six types of quarks, six leptons, and the four forces. But the Standard Model leaves many other questions unanswered. Questions regarding the Standard Model are:

- How can the gravitational interaction be included in the Standard Model?
- How can the generation of particle masses be explained?
- Why is there so much more matter than antimatter in the universe?
- Why are there three types of quarks and leptons of each charge?
- Why are the W and Z particles very massive and the photon massless?
- Is there some pattern to the masses of fundamental particles?
- What particles form the dark matter in the universe?
- Are the quarks and leptons really fundamental, or do they too, have substructure?
- Are there more types of particles and forces to be discovered at yet higher-energy accelerators?

In attempts to answer some of these questions, the Standard Model applies the Higgs mechanism. It suggests that particles acquire mass by interacting with a field, the Higgs field, which is present everywhere. If we were able to discover the Higgs boson(s), we would have proved the existence of the Higgs field. The only thing we can say about the Higgs boson today, is that if it exists, it must have a mass greater than about 115 GeV/c^2.

The Standard Model calculations suggest that if the quarks energies reach 1 TeV something has to show up. This is the energy range, which the LHC has been designed to explore.

3.3 Worldwide Discoveries that led to the Standard Model

The current theoretical framework is based on experiments that started in 1897 with the discovery of the electron. Today, we know that there are, as mentioned six leptons, six quarks, together with the force carriers (photon, 8 gluons, Z, W^+, W^- and graviton). The list below gives the dates of the discoveries, the names of scientists and laboratories involved.

Quarks:

Up (u) down (d)	1968	Physicists at the Stanford Linear Accelerator Center (SLAC) observe the first evidence for quarks inside the proton.
Strange (s)	1951	First observation of kaons (particles containing strange quarks) in cosmic-ray experiments.
Charm (c)	1974	Physicists at SLAC and BNL discover independently a new particle that contains a new kind of quark, called the charm quark.
Bottom (b)	1977	Led by Lederman, a group of scientists at Fermilab discover the upsilon, a particle containing a bottom quark and an anti-bottom quark.
Top (t)	1995	The CDF and DØ collaborations at Fermilab announce the discovery of the top quark, an elementary particle as heavy as a gold atom.

Leptons:

Electron (e)	1897	Using a cathode tube, Thomson discovers the electron at the Cavendish laboratory in England.
electron - neutrino (ν_e)	1956	Experimenters led by Cowan and Reines at the Savannah River plant detect the first neutrino.
muon (μ)	1937	Neddermeyer and Anderson discover the muon in a cosmic-ray experiment.
muon - neutrino(ν_μ)	1962	Scientists at BNL discover the muon neutrino.
Tau (τ)	1976	Experimenters at SLAC discovers the tau lepton, the first observation of a third-generation particle.
Tau - neutrino(ν_τ)	2000	Fermilab announces first direct evidence for the interaction of a tau neutrino in a detector. Indirect indications for the existence of this particle existed since more than two decades.

Force carriers:

photon (γ)	1905	Based on Planck's introduction of quanta of energy, Einstein describes the photoelectric effect using light particles called photons. They are carriers of the electromagnetic force.
gluon (g)	1979	At the Deutsches Elektronen-Synchrotron (DESY) in Germany, scientists report evidence for the gluon, the carrier of the strong force.
electroweak bosons (W,Z)	1983	Physicists at the European research laboratory CERN observe the W and Z bosons, the only force carriers with mass.

Antimatter:

Every particle has its own antiparticle. Two major discoveries helped physicists to establish this fundamental principle:

positron (e^+)	1931	Examining cosmic-ray data, Anderson discovers the positively charged electron - later named the positron.
antiprotron (p^-)	1955	Using an accelerator at Berkeley University, Segre and Chamberlain discover the antiproton. (Later, physicists learnt that a proton contains quarks, and an antiproton consists of antiquarks.)

The theory of the Standard Model is intimately connected to the numerous discoveries in quantum physics in the first half of the 20th century. Here the major theoretical breakthroughs of the second half of the 20th century that were honored with Nobel Prizes.

1965 Tomonaga, Schwinger and Feynman receive the Nobel Prize for formulating the theory of quantum electrodynamics, the most precisely tested theory in physics.

1969 Gell-Mann receives the Nobel Prize for his contributions to the classification of elementary particles, and their interactions.

1979 Glashow, Salam and Weinberg receive the Nobel Prize for the unification of the electromagnetic and weak interactions in an electroweak theory.

1999 Gerardus 't Hooft and Veltman receive the Nobel Prize for their quantum formulation of the electroweak theory.

Another major component of the Standard Model, the theory of strong interactions (quantum chromodynamics), also emerged in the second half of the 20th century [9].

4 Particle Detection

4.1 Passage of Ionizing Radiation in Matter

Knowing that charged particles lose their energy in matter, a natural question to ask is: How far will the particles penetrate before they lose all their energy? Moreover, if we assume that the energy loss is continuous, this distance must be a well defined number, which is the same for all identical particles with the same initial energy in the same type of material. This quality is called the *range* of particle, and depends on the type of material, the particles type and its energy.

Experimentally, the range can be determined by passing a beam of particles at the desired energy through different thickness of the material in question, and measuring the ratio of transmitted to incident particles [10].

For equivalent energy, the specific energy loss of electrons is much lower than that of heavy charged particles, so their path length in typical absorbers is hundreds of times greater. As a very crude estimate for energies between 1 and 10 MeV, electron ranges tend to be about 1 mm per MeV in low-density materials, or about 2 mm per MeV in materials of moderate density [11].

The range of beta particles in absorbers would seem to be quite complex in view of the many interactions that are possible, as inelastic collisions with atomic electrons and inelastic/elastic collisions with atomic nuclei. Actually, complexities of the beta spectra and the multiple interactions of these beta particles may be combined to give a relatively simple relation. This relation is the analog to Beer's law for light absorption. If I(x) is the intensity with no absorber, x is the absorber density thickness in g/cm^2 , and μ is the linear absorption coefficient in reciprocal units of density thickness, then

$$I(x) \cong I(0)e^{-\mu x} \tag{4-1}$$

or

$$x \cong -\frac{1}{\mu}\ln\frac{I(x)}{I(0)} \tag{4-2}$$

The relation of Eq. (4-1) is accurate over a wide range of density thickness. The absorption coefficient of the equation is inversely dependent upon energy. An empirical formula relating the absorption coefficient in units of square centimetres per gram to the maximum energy of the beta particles in units of MeV, is

$$\mu = \frac{22}{(E_{max})^{1,33}} \tag{4-3}$$

This empirical relation is valid for E_{max} values between 0.5 and 6 MeV [12].

Bethe, Bloch and other authors first preformed the correct quantum-mechanical calculation. The formula is commonly known as the Bethe-Bloch formula, and is the basic expression used for energy loss calculations.

At non-relativistic energies dE/dx is dominated by the overall $1/\beta^2$ factor in Bethe-Bloch formula, where $\beta = v/c$, and decreases with increasing velocity until about $v \cong 0.96c$ which corresponds to energy of about 300 MeV, where a minimum is reached. Particles with this energy are known as minimum ionizing (MIP). The minimum value of dE/dx is almost the same for all particles of the same charge. As the energy increases beyond this point, the term $1/\beta^2$ becomes almost constant, and dE/dx rises slightly again.

For energies below the minimum ionizing energy value, each particle exhibits a dE/dx curve, which, in most cases, is distinct from those of the other particle types. This characteristic is often exploited in particle physics as a mean for identifying particles in this energy range.

Since the setup is using a β source, it is worth mentioning how to shield electrons. High-Z materials, where Z is the number of protons in an atom, should be avoided because of bremsstrahlung production. Instead, low-Z materials, e.g., polystyrene of lucite should be used. For intense electron sources, a double layer shield consisting of an inner layer of low-Z material followed by a layer of Pb (or some other high-Z material) to absorb bremsstrahlung should be used. The inner layer should, of course, be sufficiently thick to stop the electrons while the outer layer should provide sufficient attenuation of bremsstrahlung [10].

4.2 Scintillator

The scintillation detector is undoubtedly one of the most often, and widely used particle detection devices in nuclear and particle physics today. It makes use of the fact that certain materials, when struck by a nuclear particle or radiation, emit a small flash of UV or visible light. This is called scintillation. The incident ionizing radiation interacts in the scintillator material and produces secondary electrons (δ-rays). These electrons excite the scintillator atoms, and flashes of light (UV or visible) are produced when the atoms de-excite.

The scintillator material is covered by a reflective material, and coupled to the read-out device by some optical compound. This is done to minimize the loss of scintillation light and thereby achieve an optimal signal to noise ratio (SNR). When coupled to an amplifying device such as a photomultiplier, these scintillations can be converted into electrical pulses, which can then be analysed and counted electronically to give information concerning the incident radiation [10].

When evaluating a scintillation detector, it is convenient to consider its two components, the scintillator and the read-out detector, separately. There are two types of scintillator materials: Organic materials (plastic or liquid scintillators) and inorganic materials. Inorganic scintillators are usually called scintillation crystals. The stopping efficiency of a scintillation crystal is determined by its density and size. Increasing the crystal thickness will, however, increase the loss of scintillation light by self-absorption in the crystal, and thereby reduce the output signal and the SNR. Hence it is preferable to use small, dense crystals, which also allow tight stacking. The light output, i.e. the efficiency with which e.g. beta-ray energy is converted to scintillation light energy, is another important crystal property as this also directly affects the signal and thereby the SNR. The speed of response of a scintillation crystal is determined by the decay time of the scintillation signal (flash).

The read out of the scintillation light may be done in many different ways, by using photomultiplier tube (PMT), channeltron (operates the same way as the PMT with the difference that the dynode chain is replaced with a continuous, resistive channel), micron channel plate (MCP which is several, microscopic channeltrons stacked together in a two-dimensional array), hybrid photomultiplier tube (where the dynodes and the anode of the PMT are replaced with an energy sensitive solid state detector) or photodiode (either a standard silicon photodiode or an avalanche photo diode which has internal gain). The conventional PMT has been, and still is, the standard read out detector for scintillation light, and is further described in the next chapter.

By handling of unprotected plastic, it is advisable to wear cotton or terylene gloves as the acids from hands can cause a cracking of the plastic (often referred to as craze) after a period of time. Organic solvents such as acetone and other aromatic compounds easily attack plastics. They are, however, resistant to water, pure methylal (dimethoxymethane), silicon grease and lower alcohols.

We used a plastic scintillator, which after cleaning was packed in aluminium foil. The amount of aluminium foil must be enough to stop the light from reaching the scintillator, but thin enough to let the β particle through. (Since we have a strong β source, (100kBq) it is not so critical with the foil thickness). The size of the scintillator we used was 2,2 cm wide, 1,2 cm high and 3,5 cm long.

4.3 Photomultiplier

Photomultipliers are electron tubes, which convert light into a measurable electric current. When a photon strikes the photocathode, it may eject an electron. It is difficult to measure the effect of a single electron using standard laboratory instruments such as oscilloscopes and voltmeters. To have a measurable effect, the initial electron needs to be converted to between 10^4 and 10^5 electrons. This is done with amplification, using tubes which contain a chain of dynodes. Outside the PM tube there is a voltage divider circuit that gives different voltage to the dynodes inside the tube.

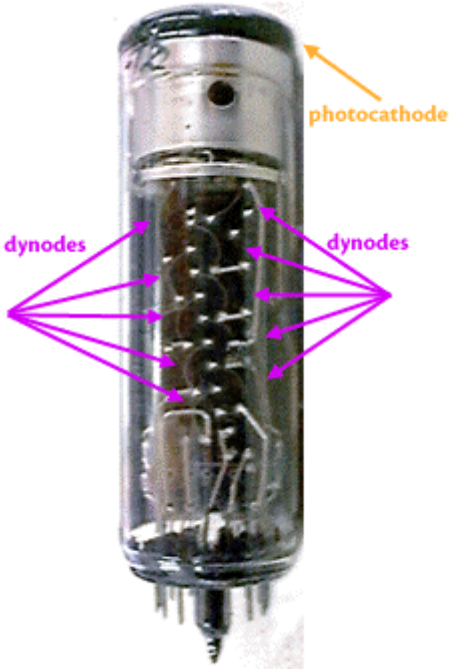

Figure 12 Photo multiplier vacuum tube

Each dynode in the chain is held at a slightly higher potential relative to the next, and is coated with secondary emissive material. Secondary emission is the process by which an electron strikes a metal, and ejects other electrons from the metal by transferring some of its kinetic energy to them. These secondary electrons are accelerated from dynode to dynode, and each electron causes the emission of several new electrons. See Figure 13. After about 8-10 dynodes there are enough electrons (current) for detecting them with a scoop or a discriminator [13].

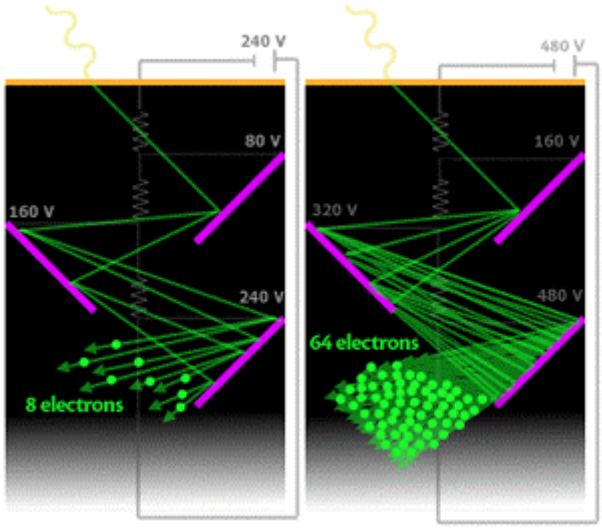

Figure 13 Dynodes inside a photomultiplier tube

The average number of electrons emitted by a dynode is linearly proportional to the potential difference between dynodes. This means that if one were to double the voltage between two dynodes, the average number of secondary emission electrons from that stage would double as well. For this particular photomultiplier tube, the average number of secondary electrons emitted per incident electron is about 0.025·(voltage between dynodes).

The relationship between the gain of a photomultiplier tube, the supply voltage and number of stages of the tube is then given by

$$g = \left(\frac{c \cdot V}{n} \right)^n \tag{4-4}$$

where g is the gain, c is a constant specific to the individual photomultiplier tube (e.g. 0.025), V is the supply voltage (e.g. 1 500 V) and n is the number of dynodes (e.g. 8).

It is very difficult to shield the photomultipliers for light, since it is so extremely sensitive. We had to make connections for the high voltage, and lemo cable at the end, because it was impossible to get out the cables without letting in some light. Gland plate was used at the end of the photomultiplicator tube, even though using black tape between the scintillator and the tube, and at the back of the tube decreased the noise considerably. The inside of the tube can be painted dark to absorb the photons instead of reflecting them.

For optimal contact between the photomultiplicator and the scintillator, a soft optical lens was used (optical grease could also be used). Since it is high voltage inside the tube, it is important to give the electronic and the cabling good distance from the tube. The scintillator was packed in with a thin film of aluminium paper to let through β particles, but not photons from the light, and then wounded with black tape.

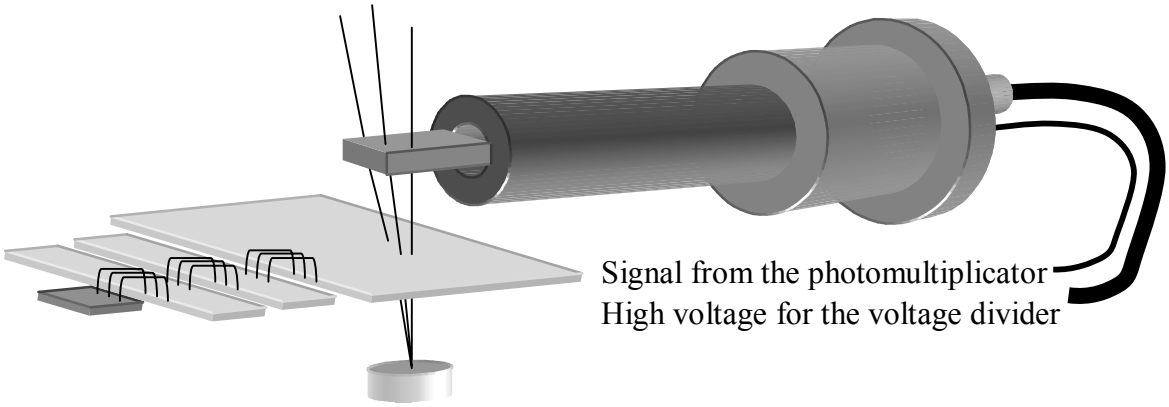

Figure 14 Drawing of the photomultiplicator tube

Figure 14 shows beta particles going through the detector and into the scintillator. The photomultiplicator is used as a trigger in the setup, and tells the system when there has passed a particle through the detector.

4.4 Silicon

Silicon is a material of the IV group of the periodic system. The p- and n-type silicon are obtained by doping the silicon substrate with atoms of the III and V group. The number of these atoms in the substrate decides the density of holes or electrons. Holes and electrons are respectively called majority carriers in p-and n-type silicon.

If we have two crystals, one n-doped and the other p-doped, and bring these together to form a p-n junction, there will be a diffusive migration of carriers across the junction. The initial migration of the carriers will set up a potential barrier, which stops the further migration of majority carriers. The area around the p-n junction, where the carrier density is almost zero, is called the depletion region. In particle detectors the depletion region is the matter of interest, because it is in this area where the particles leave their tracks. In order to expand this area in the detector, a reversed bias voltage will be applied across the detector. We used bias volts between 0-200 in our set up.

4.5 Silicon Microstrip Detectors

There are several reasons why the silicon detectors have become important for particle detection. They have good spatial and energy resolution, fast response time, and a good signal to noise ratio is easily obtained. The output signal is also directly proportional to the energy deposited by the particle. In silicon, one gets an electron-hole pair for every 3.6 eV released by a particle crossing the medium. This is very low energy compared to the 30 eV required to ionize a gas molecule in a gaseous detector, or about 300 eV to extract an electron from a photocatode coupled to a plastic scintillator. The high density of the medium reduces the range of energetic secondary electrons, allowing good spatial resolution.

Another positive effect of the high density of silicon is the high specific energy loss. The average energy loss in silicon is about 280 eV/μm. Strip detectors are widely used for reconstructing the particle paths in the particle detectors. The ATLAS experiment will include a large microstrip tracking detector. This detector must operate in a high radiation environment for at leas 10 years, maintaining a satisfactory detector performance despite the resulting severe changes in the material properties of the silicon and dielectric. The ATLAS tracker has one “barrel” detector design, and five slightly different designs for the “forward” detectors, which are to be built into disks. The same specifications apply to all designs except for the geometric differences. The final overall production requirement for the ATLAS will be about 20 000 detectors [14].

The spatial accuracy of silicon microstrip detectors depends on effects that can be divided into two categories. First category contains physical processes such as statistical fluctuations of the energy loss, diffusion of carriers during the energy loss and diffusion of carriers during the drift. External parameters like strip, readout pitch and electronics noise belong to the second category.

4.6 Silicon Microstrip Detector Operational Principles

The silicon microstrip detector consists of diodes (readout strips) arranged as thin lines. As mentioned a reverse biased voltage applied across the wafer depletes the bulk of the detector. When a charged particle passes through the matter, electron-hole pairs will be created. Because of the electric field, the electrons will move to the backplane, while the holes will accelerate towards the readout strips (p-on-n detectors). This provides the signals that are amplified and used to determine the track of the particle. In Atlas, p-on-n detectors (p+ strips on a n-type substrate) will be used.

The bulk material used is a 285 μm thick resistively n-type silicon. This bulk has strips of p+ silicon on one side and a layer of highly doped n+ on the other. The p+ layers serves to reverse polarize the junction, and the n+ to ensure a good ohmic contact to the external world. The signals from the detector are collected on the p+ strips (readout strips) that are implanted with 1 μm thick aluminium contact. A coupling capacitor created by separating the diode strip from the metal by an insulating layer. Silicon dioxide is used as insulator because it has a good electrically permittivity (0.34 pF/cm).

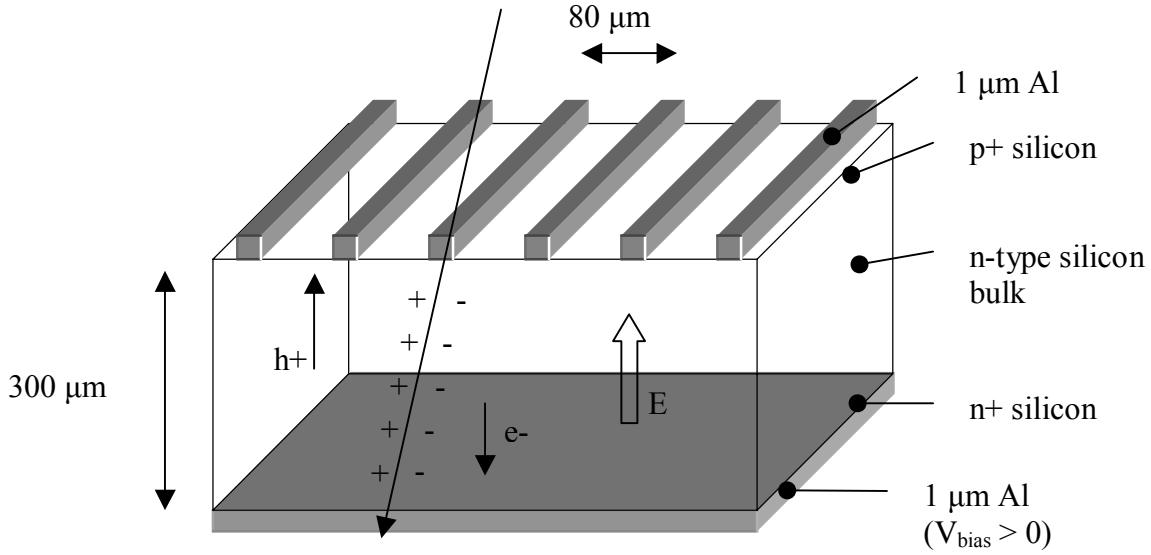

Figure 15 p-on-n type silicon micro-strip detector

Guard rings are also added at the edges of the detector to avoid breakdown, which can be caused by the increased depletion voltage after irradiation. The damage to the detector at breakdown is due to the avalanche of electrons that flow across the junction, with the results that the diode overheats. The large current can cause destruction of the detector if excessive heat builds up. These guard rings will decrease the high voltage performance.

The energy lost by a particle which is passing through a 300 µm thick silicon is about 84 keV. This value is calculated from the Bethe-Bloch formula (a formula used to give a description of the energy loss for charged particles.) The average energy needed to create an electron-hole pair is also known. Then we can find how many electrons that are set free:

$$N = \frac{84keV}{3.662eV} = 22600 \ electrons \tag{4-5}$$

and the charge freed by passing on one ionizing particle through the silicon detector is:

$$MIP = 22600 \cdot 1.6 \cdot 10^{-19} C = 3.6 fC \tag{4-6}$$

Where MIP means Minimum Ionizing Particle. Detector pitch is the distance between the centres of any two strips. It could be favourable to have a very dense readout, in order to measure the signal on several strips, and reconstruct the shape of the charge distribution to find the centre. We know that amplification of the signal in semiconductors is low because of capacitive noise in strip detectors. Because of this noise the, charge should be collected in just a few strips. Table 4 shows the detector electrical properties [15].

Table 4 Strip detector electrical properties

Specification	Value	Unit
P-implant Resistivity	<200	kΩ/cm
Aluminium strip Resistance	< 15	Ω/cm
Bias resistors (polysilicon)	1.5 ± 0.5	MΩ
Load capacitance per strip	<1.2	pF/cm
Coupling capacitance	> 20	pF/cm
Depletion voltage	<100	V
Initial leakage current at 20ºC	<6	µA at 150V
(no irradiation)	<20	µA at 300V
	<100	µA at 500V
Leakage current after irradiation	<1.2	mA at 150V

4.7 Radiation Damage in Silicon Detectors

The radiation doses at LHC, will cause some problems for the silicon microstrip detector. The system has to be cooled down to very low temperatures to decrease the leakage current. This, because an increase in temperature also will increase the leakage current, and then the noise also will increase. We can roughly say that one gets a three-fold increase in the leakage current for each 10º C. Another disadvantage is its sensitivity to radiation damage because of its crystalline structure. Damage on the crystal will cause a decrease in charge collection efficiency. This damage will be reduced at lower temperatures. The main reason of radiation damage is the incoming particles, which collide with the lattice atoms. During these collisions a movement in the lattice will occur. The radiation can also change the resistivity of the base material. An increase of problems will be the result of radiation damage. The high radiation levels will cause the n-type bulk to go over to p-type bulk. This is known as type inversion. Therefore it is important to always operate the detectors overdepleted since a partially depleted detector will have the un-depleted zone on the p-side of the detector. These problems will together limit the useful lifetime of the semiconductor. For use of radiated detectors, it is worth to notice, that capacitance changes drastically as a function of the absorbed radiation dose, much more than the mentioned temperature dependent part.

The results after 10 years of operation at full luminosity, will be a type inversion for all detectors and bias voltages up to ~450 V. The reason why a p-on-n detector (p+ strips on a n-type substrate) was chosen is because this detector had showed that efficient partially depleted operation is possible after type inversion, due to its fast signal collection and limited charge diffusion.

4.8 Noise

The bias voltage determines the thickness of the depletion layer, and also the capacitance of the detector. High voltages thus reduce the noise by increasing the depletion thickness, however, a greater risk of breakdown is also induced. When voltage is applied, this should be done slowly, raising the voltage a few tens of volts at a time and allowing the detector to "settle" for a few seconds after each step. A good procedure is to observe the noise signal on the oscilloscope as the voltage is raised. Immediately after each increase in voltage, the signal may disappear from the oscilloscope display, but should reappear after a second or two. If there are any sudden, very large intermittent increases in noise, breakdown has occurred, and the voltage should be removed immediately to prevent irreversible damage. After the desired voltage has been reached, it is a good idea to allow the detector to stabilize for a few hours, especially if it has not been used for a long period. In some cases, the noise level will also diminish further.

Particular care should be taken with very thin detectors as small increases in voltage correspond to large increases in the electric field.

Because of the small signal obtained from semiconductor detectors, care must be taken to use low-noise electronic for signal processing. In particular, a preamplification is necessary before any further processing. Because the capacitance of semiconductors changes with temperature, charge-sensitive preamplifier preforms this, which apart from the detector itself, is the most important part of a semiconductor detector system. This type of preamplifier is preferred because of its insensitivity to changes in capacitance at its input. To ensure stability, it is necessary for the preamplifier capacitance to be much larger than all the other sources of capacitance at the input, i.e., the detector, cables, etc. Since typical capacitances are of the order of tens of picofarads, preamplifier dynamic capacitances are generally of the order of a few tens of nanofarads.

The noise of the preamplifier is particularly important as it affects the ultimate resolution of the detector. Since the signal from the detector appears as electrical charge, electronics noise is usually quantified by giving its Equivalent Noise Charge (ENC). If V_{rms} is the average voltage noise level appearing at the output,

$$ENC = e\frac{V_{rms}}{w}C \qquad (4\text{-}7)$$

where C is the total input capacitance of the detector and preamplifier, e the neutral logarithm base 2.718…, and w the average energy required to cerate an electron-hole pair [10]. From (4-7), it is clear that minimizing noise requires minimizing the input capacitance of the preamplifier. For this reason the preamplifier is generally mounted as close as possible to the detector, in order to reduce capacitance from cables, etc.

The main contribution to noise in silicon detectors comes from the capacitive coupling of one strip being read out, to its neighbours and to the backplane. It causes a signal smearing and acts as a load capacitance of the preamplifier. Load capacitance gives the main contribution to noise for most readout systems. This noise is known as series noise.

4.9 Analog versus Binary Readout

Analog readout means that pulseheight information from each strip is preserved through the readout chain. Another alternative is binary readout in which only a single bit from each microstrip, “hit yes” or “hit no”, is transferred over the readout chain. Each solution has its advantages and its disadvantages. The position ambiguities are in favour of analog readout. Space and resolution can also easily be improved with analog readout. This is because the pulseheight information can be used to calculate the position at which the particle passed.

In fact, with analog readout of the strips, it is not even necessary to connect each strip to the readout channel. For each strip that is read out there can be one or more in between that are floating. In such a capacitive charge coupling scheme, the floating strips are connected to the p implant over a capacitor.

If a particle passes through the transducer, the charge building up on the two nearest p-implants will couple to the next strip because of the silicon interstrip capacitance. These charges will again couple to the read out electronics. The model of the coupling is the one used to calculate the position of the backplane. This leads to the obvious advantage, the need for fewer readout channels. Capacitive charge coupling is all in all a very attractive scheme.

Analog readout is to a large extent immune to external electromagnetic pickup (common mode), since common mode noise can be can be fully eliminated with software. The price to pay for this safety is a heavier load on data transmission for the detector over optical links, both in bit rate and in the required number and quality of the links.

The ATLAS Semiconductor Tracker has adopted a binary scheme for the readout of silicon strip detectors as the baseline. The binary architecture allows a more compact design, and has the advantage of a much reduced data transfer rate with more chips using a single optical link. This architecture is, however, not immune at all to common mode noise and so it is very sensitive to external electromagnetic interference.

The capacitive coupling readout scheme is only possible if analog readout is used. Binary readout and binary electronics, on the other hand, have a number of advantages, including less power consumption, ease of manufacturing and design. In a binary readout scheme, a digital level 1 buffer storage can be used, something which relaxes the space-requirements, as well. Furthermore, no potentially complicated capacitive model for the silicon transducers is needed, because in the binary scheme all the strips will have to be read out. The resolution is clearly worse than for analog readout, but the other arguments do weigh heavily in favour for the binary readout system because they all relax the demands on other components of the detector system. And there is of course a question of what resolution is actually needed. Overspecifying the resolution is only a waste of time and money [1].

Due to multiple scattering in the material which the particle must transverse (beam pipe, pixel layers, silicon detectors and so on), the particle have a tiny varying deviation from the original path. This is brought into calculations when the resolutions of the detectors for the different layers are decided.

5 The Setup

In our setup the particles starts form a nuclear β source (Ru160). The β particle goes out of the source, through the air, and straight through the thin detector. The detector is reversed biased, and has therefore a strong electrical field in the n-type silicon bulk. By passing the silicon bulk, the β particle creates electron hole pairs. The electrons are accelerated by the electrical field, and goes towards the bias. The holes drift in the opposite direction and are collected on the nearest strip.

All the holes on the strip together make a signal. This signal follows the bonded connection to the glass pitch, over to the pitch adapter, and finally to the SCTA128HC chip, see Figure 27. Here it goes through the front-end amplifier to get a higher signal. The distance between the strip and the front-end amplifier has to be as short as possible, in order to minimize the noise. Then the signal is sampled together with all the other 127 connected strips, by charging capacitors inside the SCTA128HC chip. A 40 MHz multiplexer is then used to put the 128 analog samples with physical data in a line. Putting on a header and some high low transitions at the end of the readout train makes it possible to find the start and end of the readout train outside the chip. The readout train now looks like channel 1 , Figure 62. This signal is transferred through a lemo cable into the analog to digital converter called SIROCCO (also known as VFAS or VFAS3). Often the signal is split, so it can be viewed on an oscilloscope. The SIROCCO uses the CLK input from the NIM logic to know where to trig on the readout train.

After being converted into digital values, the values are transferred through the MXI-2 cable, and into the data acquisition program using VISA session. The DAQ program can analyse and store all data from each single run. These data and history files can be analysed and further studied using the programs readData.vi and readHistos.vi.

The setup is shown in Figure 16 with all the necessary hardware, except form all the lemo cables needed to make the NIM logic for the trigger part and the SIROCCO CLK part. Including all these cables would make the drawing look like a pot of spaghetti, so two connection diagram, Figure 40 and Figure 41, shows the rest of the cabling. The readout PCB has a more detailed view shown in Figure 22, including the supply voltages. All the VME modules, the MXI-2 cable and PCI-MXI-2 board are explained separately in chapter 5.7.

The trigger part: The β particle goes further on the other side of the detector, and then hits the scintillator. Inside the scintillator the β particle hits or almost hits atoms, resulting in photons coming out. What happens inside the photomultiplicator is widely described in chapter 0. The output of the photomultiplicator, the trigger, is sent via a lemo cable and into a discriminator. In the discriminator the signal is converted from a short 10 ns 200 mV pulse to a 20 ns 700 mV pulse, which then is used in the NIM logic, for trigging the system every time there is a particle going through the detector.

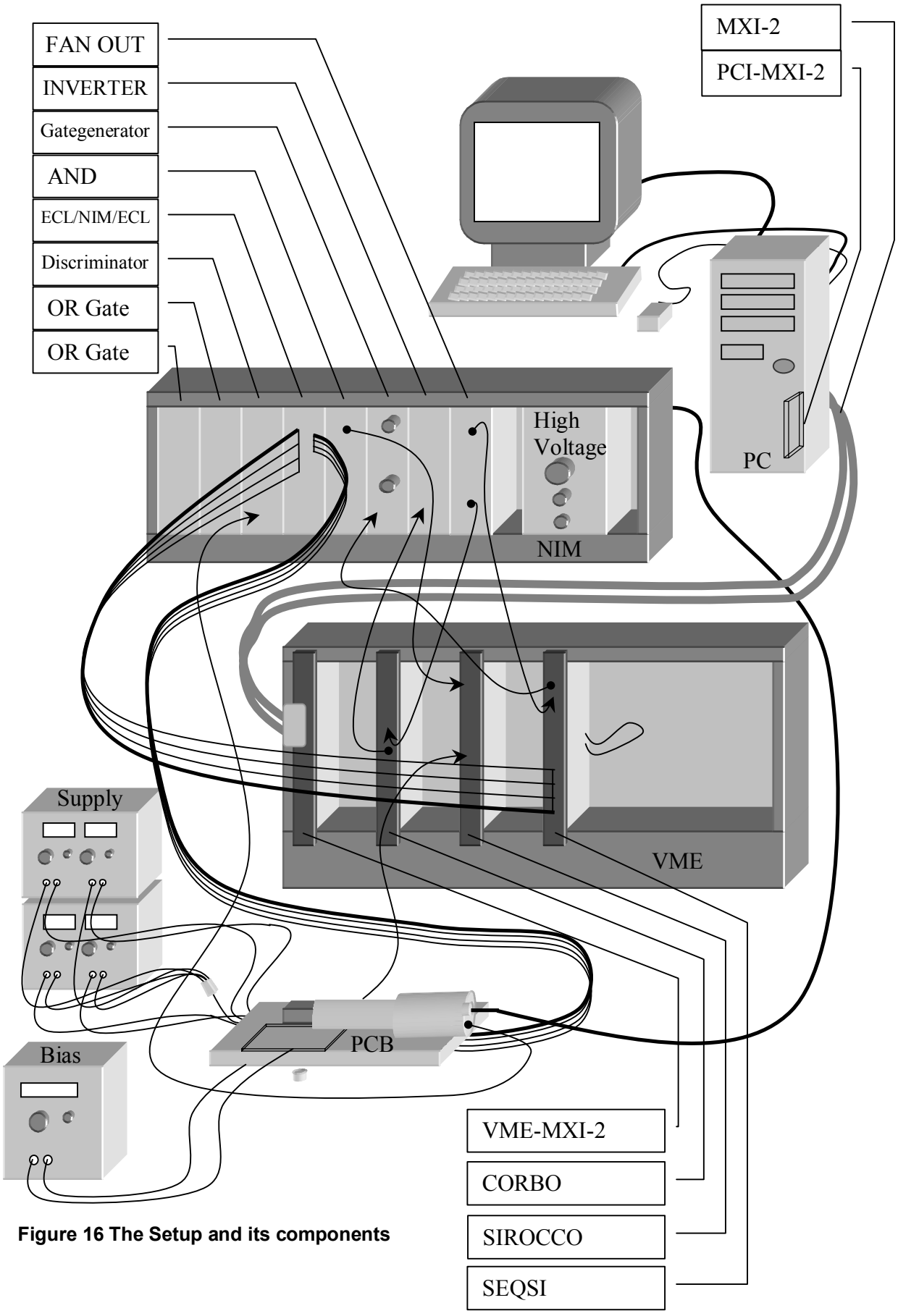

Figure 16 The Setup and its components

5.1 Introduction to LabVIEW

As programming languages have evolved, the power of the languages has also grown, from Pascal's mechanical calculator in 1642, to FORmula TRANslation (FORTRAN) in 1957 and National Instruments in 1986 with LabVIEW 1, (Laboratory Virtual Instrument Engineering Workbench). The ease of writing and compiling the codes has improved significantly as well.

In contrast to text-based programming languages, where instructions determine program execution, LabVIEW is a graphical programming language that uses icons to create applications. LabVIEW uses dataflow programming, where data determine execution. In LabVIEW, the user interface is build by using a set of tools and objects. The user interface is known as the front panel. The codes are then added using graphical representations of functions to control the front panel objects. The block diagram contains this code. If organized properly, the block diagram resembles a flowchart.

One can purchase several add-on software toolsets for developing specialized applications. All the tools integrate seamlessly in LabVIEW. Refer to the National Instrument web site [16] for more information about these toolsets. LabVIEW is integrated fully for communication with hardware such as GPIB, VXI, PXI, RS-232, RS-485, and plug-in data acquisition devices. LabVIEW also has built-in features for connecting the application to the Internet, using the LabVIEW web server and software standards such as TCP/IP networking and ActiveX (Version 6i (internet) mostly).

Using LabVIEW, a 32-bit compiled application can be created, that give the fast execution speeds needed for custom data acquisition, test measurements, and control solutions. Stand-alone executables and shared libraries (DLLs) can also be created, because LabVIEW has a true 32-bit compiler. LabVIEW contains comprehensive libraries for data collection, analysis presentation, and storage, it also includes traditional program development tools. It is possible to set breakpoints, animate programme execution, and make single-step through the program, to make debugging and development easier.

LabVIEW enables to build own solutions for scientific and engineering systems. LabVIEW gives the flexibility and performance of a powerful programming language, without the associate difficulty and complexity. If the data acquisition program was written in a text based program language, it would be an enormous amount of source codes, which would be almost impossible to get the overview of. By using LabVIEW to prototype, design, test and implement the instruments systems, the development time can be reduced quite a lot.

5.1.1 How Does LabVIEW Work?

LabVIEW programs are called virtual instruments, or VIs, because their appearance and operation imitate physical instruments, such as oscilloscopes, multimeters, switches and so on. Every VI uses functions that manipulate input from the user interface and other sources, and displays that information, or moves it to other files or other computers.

A VI contains the following three components:

- Front panel: Serves as the user interface, shown in Figure 17.
- Block diagram: Contains the graphical source code of the VI that defines its functionality, shown in Figure 18.
- Icon and connector pane: Identifies the VI so that the VI can be used in another VI, then referred to as a subVI. A subVI corresponds to a subroutine in text-based programming languages, shown with an arrow in Figure 17.

5.1.2 Front Panel

The front panel is the user interface of the VI. It is built with controls and indicators, which are the interactive input and output terminals of the VI, respectively. Controls are knobs, push buttons, dials, etc. Indicators are graphs, LEDs, numerals etc. Controls simulate instruments input devices, and supply data to the block diagram of the VI. Indicators simulate instrument output devices, and displays data that the block diagram acquires or generates. Since it is important to know what is actually a Panel and what is a Diagram, a tiny adding program is shown. Figure 17 shows how the Panel looks like. This is what the user sees.

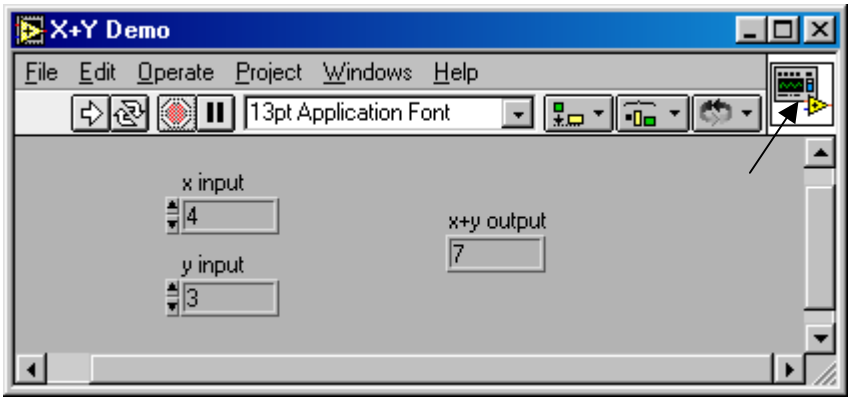

Figure 17 Front Panel with two inputs and one output

5.1.3 Block Diagram

After the front panel is built, the code is generated using graphical representation of functions to control the front panel objects. The block diagram contains this graphical source code. Front panel objects appear as terminals on the block diagram. A terminal cannot be deleted from the block diagram. The terminal disappears only after the corresponding object on the front panel is deleted.

Every control or indicator on the front panel has a corresponding terminal on the block diagram. Additionally, the block diagram may contain functions and structures for built-in LabVIEW libraries. Wires connect the nodes on the block diagram, including control and indicator terminals, functions, and structures. Figure 18 shows the Diagram with the graphical source code, which is the programmer's main window.

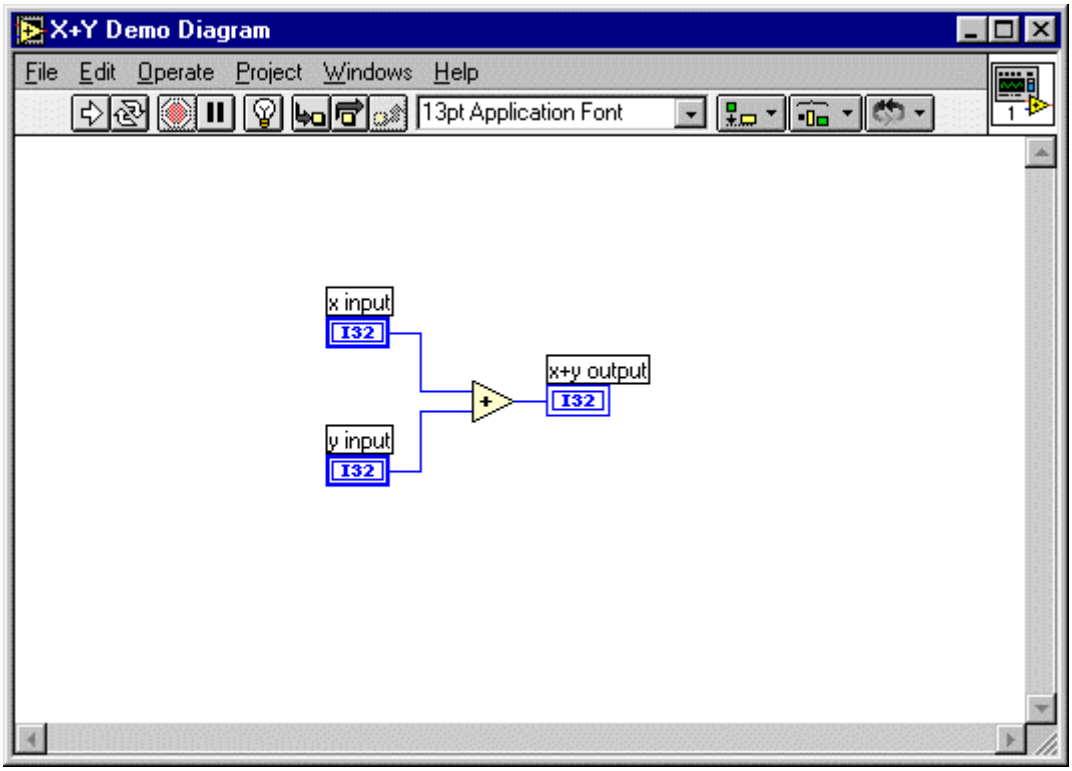

Figure 18 Block Diagram showing the graphical source code for adding to inputs

5.1.4 Palettes

LabVIEW palettes give the user the options needed to create and edit the front panel and the block diagram. There are three palettes:

- The control palette: To create and edit in the front panel.
- The functions palette: To create and edit in the block diagram. Functions are elementary nodes in the G programming language. They are analogous to operators or library functions in text based languages. Functions are not VIs, and therefore do not have front panels, or block diagrams. When compiled, functions generate inline machine code.
- The tools palette: A tool is a special operating mode of the mouse cursor. Tools are used to define the operation taking place when subsequent mouse clicks are made on the panel or diagram.

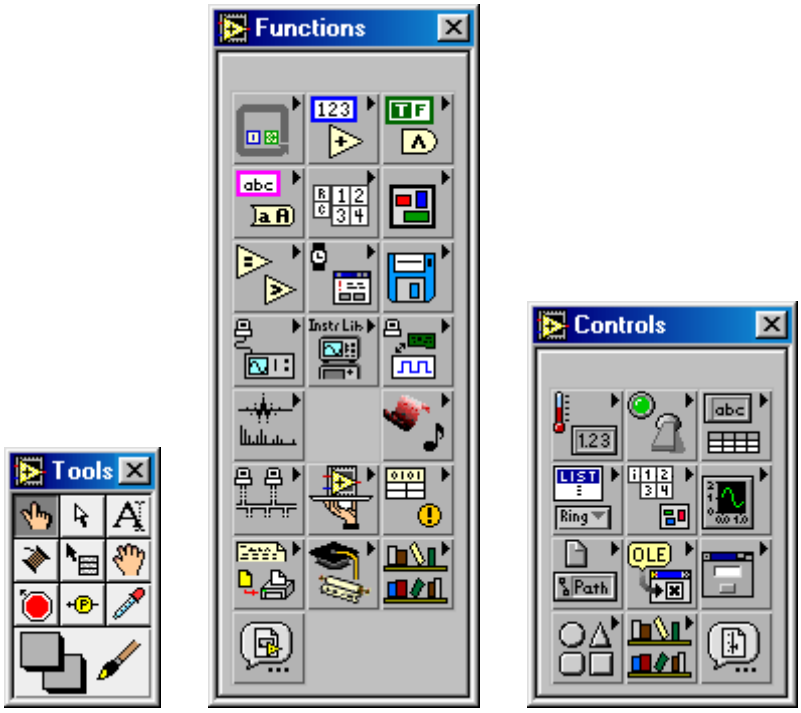

Figure 19 Tools, Functions and Controls palettes, how they look like

5.2 Hardware Description

5.2.1 MXI Multisystem eXtention Interface bus

MXI-2 is the second generation of the National Instrument MXI bus product line. The MXIbus is a general-purpose, 32-bit, multimaster system bus on a cable. MXI-2 expands the number of signals on a standard MXI cable by including VXI triggers, all VXI interrupts, CLK10, and all of the utility bus signals (SYSFAIL, SYSRESET and ACFAIL).

Because MXI-2 incorporates all of these new signals into a single connector, the triggers, interrupts, and utility signals can be extended, not only to other mainframes but also to the local CPU in all MXI-2 products using a single cable. Thus, with MXI-2, CPU interface boards such as the PCI-MXI-2 perform as though it were plugged directly into the VME backplane.

The new synchronous MXI block protocol increases MXI-2 throughput to a maximum of 33MB/s between two MXI-2 devices. All National Instruments MXI-2 boards can initiate and respond to synchronous MXI block cycles.

These interface kits link a PCI-based computer chassis directly to the VXIbus, using the high-speed Multisystem eXtension Interface bus (MXI-2), and can be used on a variety of platforms, including all Microsoft platforms, Macintosh, and Solaris [17].

5.2.2 VMEbus 16 Base Address

This is a 32-bit asynchronous bus developed by Motorola, Signetics and Mostec. In addition to the system bus, the VMEbus consists of extra buses to increase the performance. The VME crate provides power, cooling and mechanical support for the other modules. Backplane buses make connections of the modules in the VME crate. One of its main properties is that it can handle multiprocessing, and has seven interrupt levels. The VMEbus used in the lab-setup, has a non-multiplexed architecture. This means that data and address lines have their own pins. In multiplexed bus architecture both data and address lines use the same pins, in the first part of a bus cycle the address lines use the pins, and in the second part the pins are used by the data lines.

The VME-MXI-2 requires 64 B of A16 memory space for its configuration registers. It uses the logical address scheme of the VXIbus specification, in which each device is assigned an 8-bit value called the logical address. This logical address allocates 64 B of space to the device within the upper quarter of the A16 space. The VME-MXI-2 cannot be configured to locate its registers in the lower three quarters of the A16 space. The A16 base address of the VME-MXI-2 is address lines 14 and 15 high, with address lines 6 through 13 matching the logical address of the VME-MXI-2, and address lines 0 through 5 low. In other words, the A16 space address of the VME-MXI-2 module's 64 B register set is as calculated here: Base address = C000 hex + (logical address) · 40 hex.

The factory-default logical address for the VME-MXI-2 is 1, which locates the register in the range C040 hex to C070 hex. Changing the setting of the 8-bit DIP switch will change the logical address of the VME-MXI-2 (see U21 Figure 34). Be aware that the ON position of the DIP switch corresponds to a logic value of 0, and the OFF position corresponds to a logic value of 1.

5.2.3 Testing and debugging

The nice thing with being a physicist is the possibility to always break the problem into smaller pieces. The physicists have for some reason good correlation between cause and effect. When a biologist hits a dog in head with some special tool, it mostly yelps, but sometimes it runs away, and sometimes it bites, or in worst case, it falls dead. When something is not working for a physicist, it is "just" to start at the beginning where the signal comes from and find out where it is lost. The problem with our rather complex setup is that there are a lot of things happening almost simultaneously, and unfortunately it needs quite a lot of understanding for being capable of breaking the problem into smaller pieces. Missing documentation, and several defect modules has been the main reason for making the work for this thesis difficult.

In debugging, it is necessary to distinguish between hardware and software problems. The first thing to do if the setup doesn't work is to find out if it is the software, or the hardware that fails. The NIM modules can be tested using the oscilloscope, together with other NIM modules checking the logic functionality. The more complex VME modules are harder to give a full check. They have a lot of functionalities and specifications. Some of them have own programmable memory chips (e.g. the SEQSI), and it is impossible to find out if it is set correctly or not. After placing a VME module in the VME crate, hopefully with all the jumpers and DIP switches correctly set, it is recommended to check the access to the memory. The software setting has to match the hardware settings if communication shall be possible. VXI Interactive controller can be used for this purpose, see chapter 5.5. The settings for this setup are shown in Table 6 and Table 7.

Since we hade some trouble with defect VME modules we wrote standalone LabVIEW programs for communicating with each of them. For the CORBO, a program for setting the different LEDs at the front panel was written. For the SIROCCO, a program for starting the sampling was written (which was indicated by a LED). Writing a program for reading and writing to the memory tested the functionality of the SEQSI module.

5.2.4 Debugging Tool

The release of NI-VXI/VISA for Windows 95/NT includes two new utilities to help configure, developing and debug the system, these are T&M Explorer and NI-Spy.

T&M Explorer can be used to view the entire T&M system and configure various components. When launching T&M Explorer, a list of the VXI, GPIB, and serial devices used, appears on the screen. Right-click on the device in the list to view the properties of each device (such as logical address, address space used, primary address).

When viewing the properties of a National Instrument device, the configuration can be done directly from the properties list. T&M Explorer replaces many earlier utilities, such as VXIedit and VISAconf. T&M Explorer also has new features, such as an option to run Resource Manager at start-up, and troubleshooting to guide the user through configuration conflicts and errors.

NI-Spy tracks the calls the application makes to National Instruments T&M drivers, including NI-VXI, NI-VISA and NI-488.2 It highlights functions that return errors, so it is easy to quickly determine which functions failed during the development. NI-Spy can also log the program's calls to these drivers, so they can be checked for errors.

5.2.5 NI-VXI System Level Software

The NI-VXI system-level software is the driver that controls the PCI-MXI-2 interface and VME system. NI-VXI includes a Resource Manager, an interactive configuration and troubleshooting program libraries of software routines for test and measurement (T&M) programming, interactive control programs for both NI-VXI and NI-VISA, and logging utility used for debugging applications. This software can be used to program multiple-mainframe configurations, and have software compatibly across a variety of controller platforms.

Resource Manager must always be running before using the NI-VXI library, otherwise the system may hang, or will not function correctly.

5.2.6 VISA

VISA is a standard I/O Application Programming Interface (API) for instrumentation programming. VISA by itself does not provide instrumentation programming functionality for interfaces other than serial. VISA is a high-level API that calls system-level drivers. As an example, the NI-VISA implementation uses the NI-VXI system-level driver for National Instruments VXI controllers. VISA can control VXI, PXI, GPIB or serial instruments, making the appropriate driver calls depending on the type of instrument being used. VISA uses the same operations to communicate with instruments regardless of the interface type. For example, the VISA command to write an ASIC string to a message-based instrument is the same whether the instrument is serial, GPIB, or VXI. As a result, VISA gives interface independency. This makes it easier to switch bus interfaces, and means that users who must program instruments for multiple interfaces, need to learn only one API. Another advantage of VISA, is that it is an object-oriented API that will adapt to new instrumentation interfaces as they evolve, making application migration to the new interfaces easier.

Virtual instrument software architecture (VISA) is a global set of protocols that can control GPIB, serial and other devices, including VXI. It is a set of protocols agreed upon by more than 40 major instrument companies, so that almost all of the instruments can be controlled by LabVIEW's VISA command functions. The steps of communication using VISA functions are similar to those for data acquisition: VISA Open, VISA Read or VISA Write, and Visa Close. LabVIEW identifies which session is active by the parameter "VISA session" generated by VISA Open. VISA session is similar to the task ID of data acquisition VIs of the reference number of file I/O functions.

Setting up a communication path with instruments, using VISA protocols, is quite straightforward. A set of VIs designated for a specific instrument is called driver, and more than 600 instrument drivers have already been written. Once the driver for the instrument is obtained, the communication cannel can be tested using the Getting Started.vi, which can be found in the driver .llb files. Once the communication path is verified, the rest is LabVIEW programming [18].

5.3 The SCTA128A Chip

The LHC operating conditions presents a great challenge to the front-end electronics of Si trackers, for experiments designed for high luminosity physics. Historically most collider experiments have so far used full analog readout front-ends for Si trackers and vertex detectors. This method allows individual treatment of data in each channel, with optimized and adaptable software, and thereby the most detailed control and monitoring of the whole system. The SCTA chip is an implementation of full analog readout architecture, compatible with the requirements for readout of silicon strip detectors at LHC experiments.

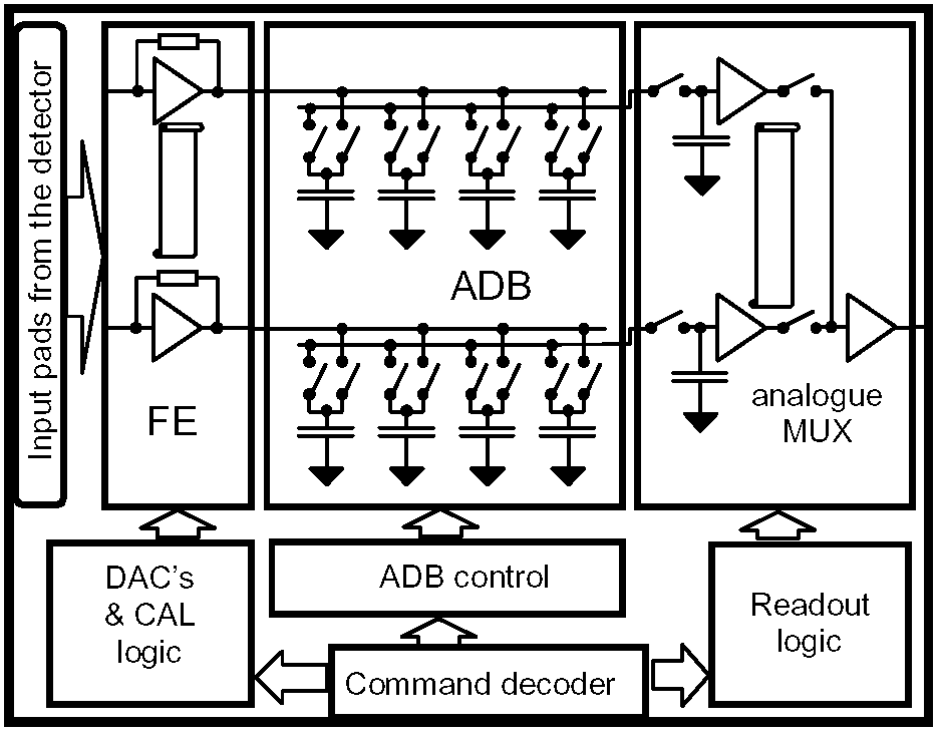

Figure 20 Block diagram for the SCTA128 chip

The SCTA128 chip comprises the following building blocks: 128 channels with front-end amplifiers, Analog Memory (ADB) with the capacity to store 128 analogue samples, control logic providing a derandomizing function (up to 8 events), command decoder and fast analog mulltiplexer to output serial data. In addition to the basic functional blocks, internal calibration circuitry containing an 8 bit DAC to control the calibration level has been implemented to improve the testability of the chip. Four 5-bit DAC's, for the bias of the analog part of the chip, have been implemented in order to compensate the drifts after irradiation, and optimize chip performance for various parameters (noise level for a given detector capacitance, required dynamic range etc.). Except from the front-end blocks, which are different for the two versions, all the other blocks are identical in the SCTA128LC and SCTA128HC.

SCTA128 Semi Conductor Tracker Amplifier is a fast readout chip, first designed as the front end electronics for the ATLAS semiconductor tracker. The SCTA chip is designed with BiCMOS radiation hard technology and consists of 128 parallel channels each with a bipolar front amplifier. It has been designed in two versions, SCT128LC optimized for a low detector capacitance from 2-5 pF, and SCTA128HC optimized for higher detector capacitance from 15-20 pF. The two versions of the front-end (LH and HC) have been designed in order to optimize the noise performance for low and high detector capacitances respectively. The main difference is the gain: 100 mV/fC for the LC and 50 mV/fC for the HC. The designed peaking time for both versions is 25 ns. The front-end circuit is designed in such a way that it can be used with either polarity of the input signal, i.e. for the p-side or the n-side. This is set in the data acquisition program called Hardware setup.

The front-end circuit is a fast transimpedance amplifier followed by an integrator, providing a semi-gaussian shaping with a peaking time of 25 ns, and an output buffer. The peak values are sampled at 40 MHz rate, and stored in a 128-cell deep analog pipeline. Upon arrival of the trigger, the analog data from the corresponding time slot in the ADB are sampled in the S&H buffer, and sent out through the analog multiplexer.

There are two 5 bit DAC's implemented in the chip, which allows to set the bias current in the input transistor, and the bias current in the shaper. These are set by the data acquisition program. In the HC front-end, the current in the input transistor can be set within the range from 0 to 310 μA with a resolution of 10 μA. The nominal setting of about 200 μA is foreseen for a detector capacitance in the range 15-20 pF. In the LC front-end, the current in the input transistor can be set within the range from 0 to 155 μA with a resolution of 5 μA. For a detector capacitance of 2 pF, the nominal current in the input transistor is 50 μA, while for a detector capacitance of 5 pF, the nominal current in the input transistor is 100μA. The actual bias current providing a maximum signal-to-noise ratio for a given detector capacitance depends on the value of the current gain factor β, as well as on the detector leakage and the detector bias resistance. Therefore, for each detector the optimum bias of the input transistor should be found experimentally. Furthermore, the current gain factor β of the input transistor will be degraded after irradiation, which requires readjusting of the bias current to optimize the signal-to-noise ratio. The second DAC provides a reference current which is used to control bias currents in the shaper and the output buffer. The shaper current can be set within the range from 0 to 77.5 μA, with a resolution of 2.5 μA. The nominal value of the shaper current is about 40 μA. The setting of the shaper current is not very critical, however, a setting different from the nominal one may be used in order to compensate changes in the circuit bias, due to possible variation of the process parameters.

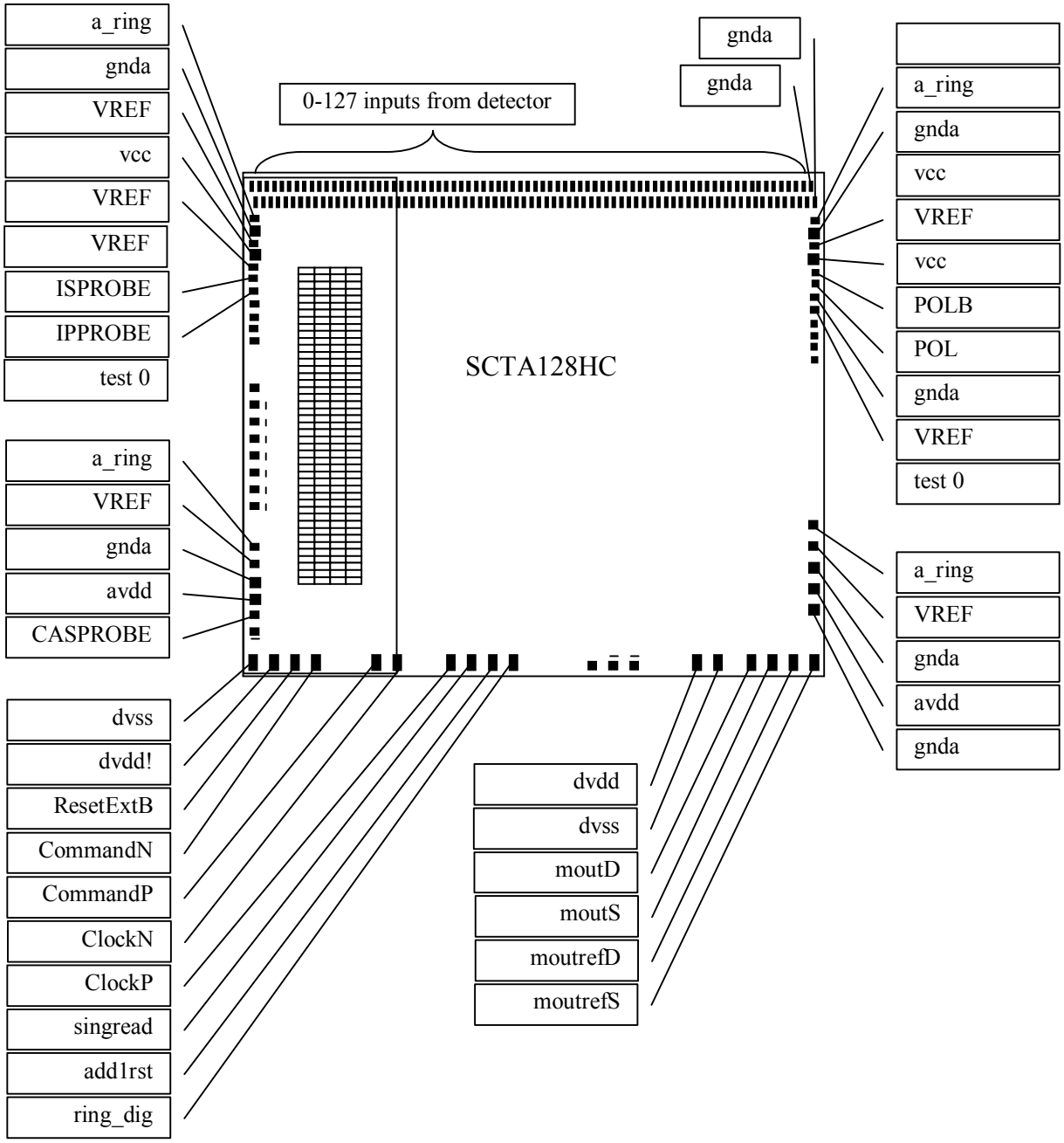

Figure 21 SCTA128HC bonding pad layout

The commands enter the chip via the serial interface as, a serial bit pattern synchronous to the main clock. The data on this line is latched by the rising edge of the BCO clock. The text boxes, that are not connected to any pads on the chip, shows only the PCB layout. The only pad difference between LC and HC versions, is that vcc and VREF pads of the front-end are swapped on both sides. The reference voltages VREF is used in the front-end circuit, as well as in the readout amplifiers, to provide a good tracking of the DC levels in output buffer of the front end, and in the read out amplifier. The bias current in the read out amplifier is controlled by another 5-bit DAC.

Table 5 SCTA128HC Bonding pad list

Pad name	Function	Description
a_ring	ring	Analog guard ring (gnd)
add1rsT	input	Bit to set the first and the second chip on the module. Set to high for the first chip
avdd	supply	Analog power supply (nominal 4 V)
CASPROBE	test output	Test output of ADB read-out amplifier bias DAC range: 0.90 mV corresponding to the current range 0-180 μA Nominal preamplifier current is about 200 μA
ClockP,ClockN	inputs	Clock input
CommandP CommandN	inputs	Command input, can be tested on CommandT pad
dvdd	supply	Digital power (nominal 4 V)
dvss	supply	Digital ground (gnd)
gnda	supply	Analog ground (gnd)
IPPROBE	test output	Test output of ADB read-out amplifier bias DAC HC version range: 0-155 mV corresponding to the preamplifier current range 0-310 μA (Nominal 200 μA)
ISPROBE	test output	Test output of the shaper bias DAC range: 0-387 mV corresponding to the shaper current range: 0-77.5 μA. Normal shaper current about 40 μA
moutrefS moutrefD	outputs	Analog outputs (can be used for differential receiver)
moutS, moutD	outputs	Reference analog outputs, can be used for differential ground (gnd)
POL, POLB	inputs	Selection of the input signal polarity (DC levels) For p-side readout : POL = HIGH, POLB = LOW For n-side readout : POL = LOW, POLB = HIGH
ResetExtB	inputs	Reset input. Exored with internal power-up reset signal
ring_dig	ring	Digital guard ring (gnd)
singread	input	When set to high, only the first chip on the module sends data
vcc	supply	Analog power supply (nominal 4 V)
VREF	supply	Reference ground (nominal 1.6), low impedance

Two SCTA128 chips can be read out via one optical fibre line, but in our setup the chip is readout by a lemo cable, connected to the analog to digital converter called SIROCCO. Programming of the ”add1rst” and ”singread” inputs does the selection of readout mode.

An analog signal train from one chip consists of a four bit header (0101), followed by the three analog samples intended for calibration of the optical links (0 0.8 1), 128 analog samples with physical data from the detector, a one bit buffer overflow flag, a four bit BCO counter, and a four bit T1 counter. This format of the data is independent of mode of readout (single or two chip readout). When the chip is in idle state, a DC level of about 2.75 V appears at moutS and mouterfS, which allows for faster transition when the chip starts sending data for 40 MHz operation. The DC level is for the high state (“1”) about 2.75 V, and for the low state (“0”) about 2.1 V.

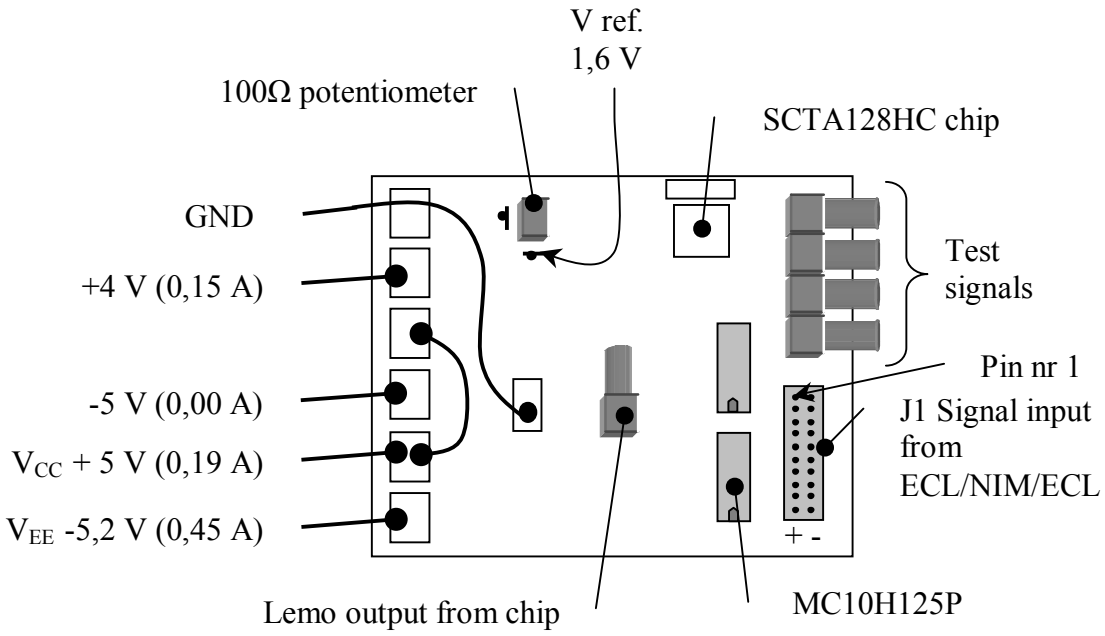

Figure 22 Readout SCTA128HC/LC PCB

Figure 22 shows the readout SCTA128HC/LC PCB board (Mod MPI 3.2.9 9MR). The supplies and the chip is on the backside of the board marked with wite squares. The currents included, are during the data aqusition program running, for knowing the working condition to the PCB. The 100 Ω potensiometer is used set the Vref on the PCB, this is done by measure the point marked V ref., and turn the potensiometer untill it gives 1.6 V. At a setup at CERN we had to set the + 4 V up to + 5 V for getting out signals, since signals were missed when the supply was under 4,2 V. The absolute max for analog and digial supply is 6 Volts.

When no signal is reachable from the chip and the NIM logic seems to work, the TTL outputs from the two MC10H125P chips could be checked. E.g. “Reset” and “Commander” can be found on the output of the MC10H125P chips, using the LabVIEW program SCT128AExerciser.llb, executing the sequences “Reset” and “Chip Setup”, while using the oscilloscope at the right TTL outputs.

To find out where to measure these outputs, Figure 23 to Figure 26 are included. Figure 23 shows the circuit diagram of the PCB, from the connector J1, to the SCAT128HC chip. Figure 24 shows the pin assignment for the HC10H125P ECL to TTL converter, and Figure 25 and Figure 26 show the layout of the PCB. One time we had to replace both the MC10H125P chips, to get out the readout train from the chip.

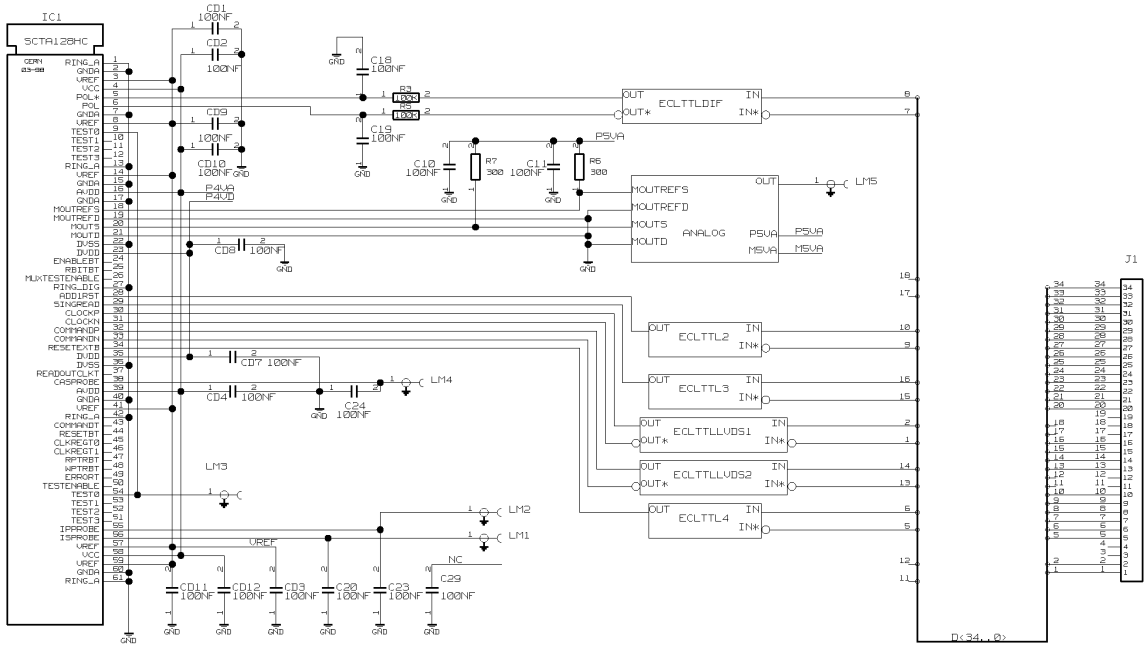

Figure 23 Circuit diagram for the SCAT128HC/LC PCB test board

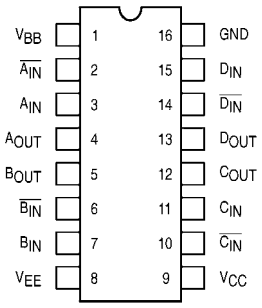

Figure 24 Pin assignment for the HC10H125P ECL to TTL converter

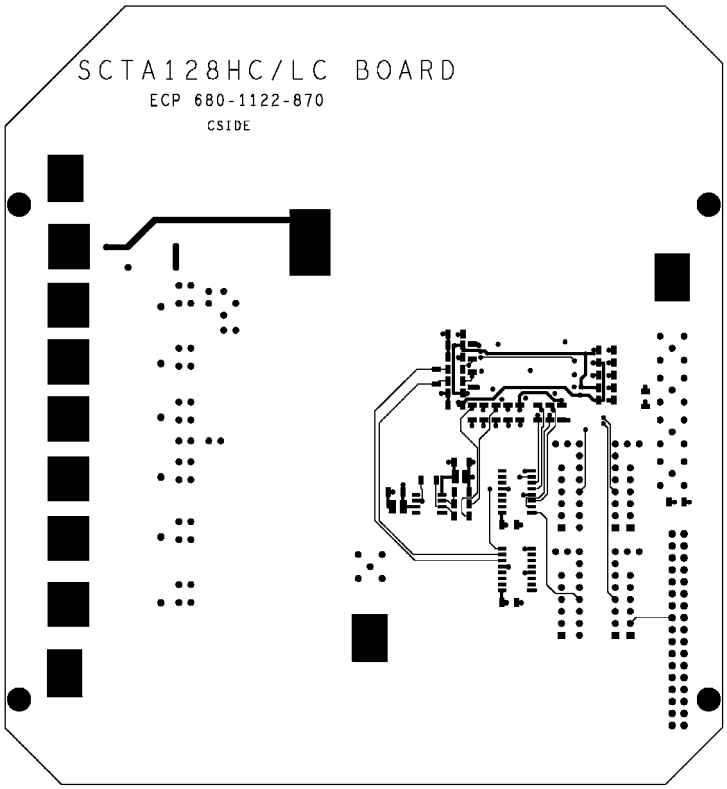

Figure 25 Solder side SCTA128HC/LC PCB

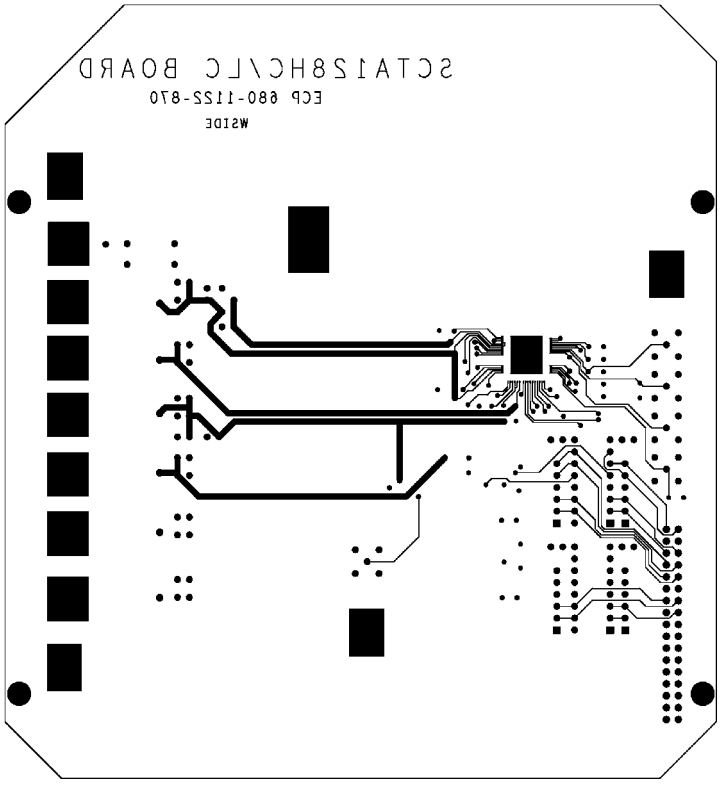

Figure 26 Back side SCTA128HC/LC PCB

5.4 Bonding

The SCTA128 chip occupies an area of 8.1 mm x 8.1 mm, and has to be bonded to the readout PCB and the pitch adapter. To not destroy the expensive SCAT128 chip due to several bondings, a glass pitch adapter is used. The pitch adapter is then bonded to the glass pitch, and then to the detector being measured. Each time a new detector is measured it must be rebonded to the pitch adapter, and after several detector bondings the pitch adapter can be replaced. The bonding description is shown in Figure 27. The figure is not in scale, just for showing where to bond.

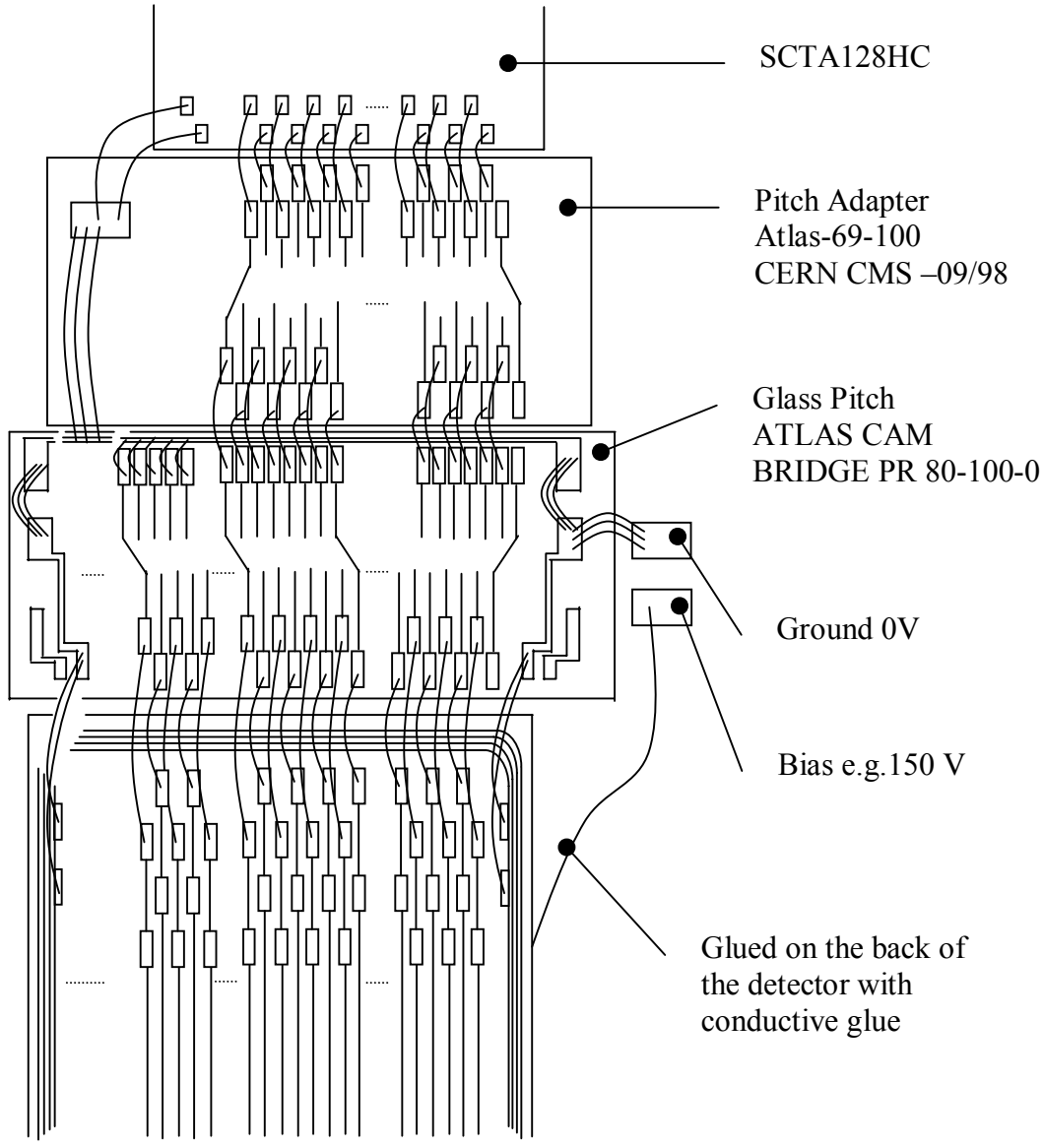

Figure 27 Bonding description from the SCTA128HC chip to the strip detector

5.5 Software settings

For running the SCTA128 setup, the following software is needed:

LabVIEW Version 5.0 or later. We used Version 5.1, and installed LabVIEW as it came with the CD. We only had to add NI-VXI (For VXI control), this was done by marking the tag “install NI-VXI (For VXI control)” during the installation procedure.

National Instrument NI-VXI/VISA for PCI-Based MCI-2 for Windows NT Version 2, which was installed with 8 floppy disks that came with the PCI-MXI-2 PCI Board. It includes Resman, VXI controller and T&M explorer. Be aware of the pdf manuals that are installed, but never mentioned, these are easy found by searching for *.pdf.

Next step is to configure the VME devices in Test & Measurement Explorer, using the add device tab. The Manufacturer and Model Row are not included in the library, so they have to be added. User can choose the slot number arbitrary, but uniform separation is recommended due to cooling reasons, and the noisy fan speed can be reduced.

Table 6 VME module properties in Test & Measurement Explorer Version 1.0

VME module	CORBO	SIROCCO	SEQSI	Old SIROCCO
Device Type	Vme device	Vme device	Vme device	Vme device
VISA Resource Name	VXI0::282:: INSTR	VXI0::256:: INSTR	VXI0::281:: INSTR	VXI0::300:: INSTR
Pseudo Logical Address	282	256	281	300
Manufacturer	Ces	W.Dulinski	M.Morrissey	W.Dulinski
Modell	RCB 8047 (0x1)	SIROCCO (0x2)	PC2935M (0x3)	V-3.0 1992
Frame	VXI Frame 1	VXI Frame 1	VXI Frame 1	VXI Frame 1
Slot	4	8	12	16
Resource type	A24 Address Range	A32 Address Range	A24 Address Range	A24 Address Range
Setting	0xF75A00 - 0xF75AFF	0xDDDD0000 - 0xDDDDFFFF	0xD00000 - 0xD0FFFF	0xC20000 - 0xC22007

After configuring the VME modules, Resman has to be restarted, and the VXI Interactive controller can be used to test if the hardware settings correspond to the software settings. At the Bus Access tab there is a number of parameters that has to be put in to check if the module communicates correctly. These parameters for each VME module are shown in Table 7.

Table 7 VXI Interactive controlling parameters for different VME modules

VME module	CORBO	SIROCCO	SEQSI	Old SIROCCO
Operation	Out	Out	Out	Out
Address Space	A24	A32	A24	A24
Privilege	NonPrivData	NonPrivData	NonPrivData	NonPrivData
Byte Order	Motorola	Motorola	Motorola	Motorola
Address	F75A00	DDDD0000	D00000	C20000
Width	Word	Long	Word	Word
Value	0	0	0	0
Status reach	CMPL	CMPL	CMPL	CMPL

At Status reach: Green light means CMPL (complete), and communication with the module should be possible. Red light means BERR (Bus Error), and indicates that something is wrong. Bus Error is an error that signals failed access to an address. Bus errors occur with low-level accesses to memory, and usually involve hardware with bus mapping capabilities. For example, nonexistent memory, a nonexistent register or an incorrect device access can cause a bus error. Before CMPL is reached on every module, there is no use in running the whole program.

5.6 LabVIEW software for SCTA128A

The software provided comprises 4 programs:

runDAQ.vi - Full DAQ system, with file management, full event analysis and histogramming.
readData.vi - Playback of raw data files, with event-by-event analysis.
readHistos.vi - View and analyse saved histograms.
sct128Tool.vi - Interactive facility to set up and trigger the chip, ideal for debugging observing the data train, setting strobes and so on.

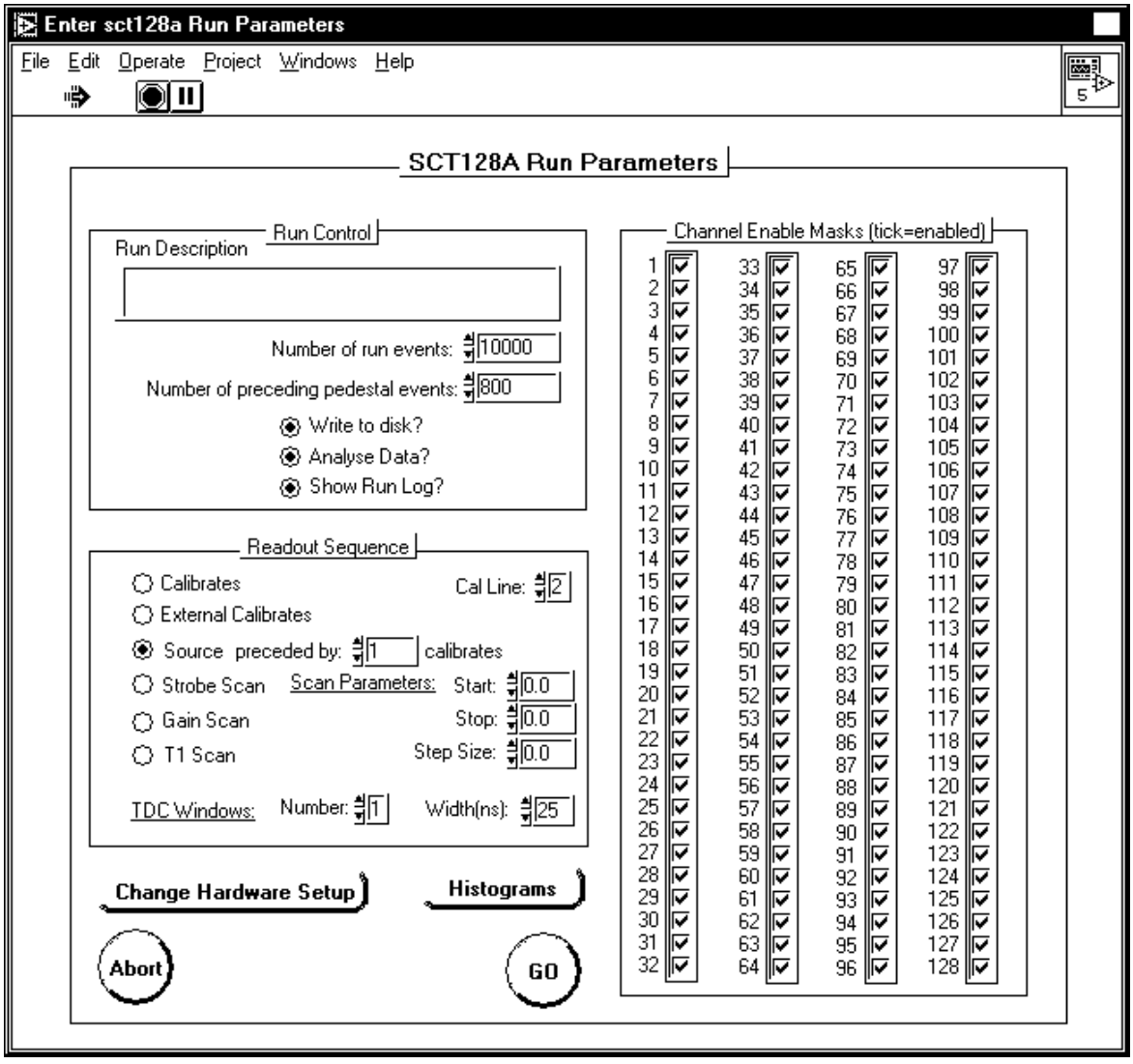

Figure 28 Screen shot of Enter scta128a Run Parameters before starting

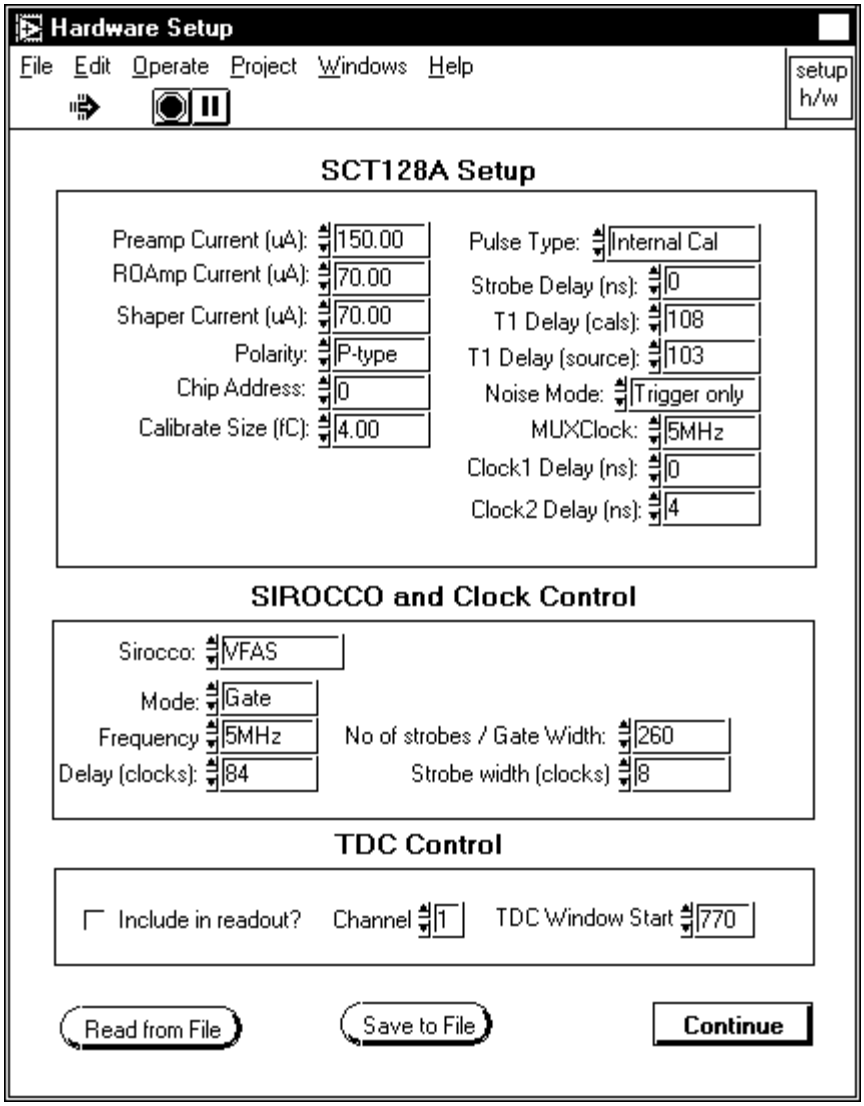

Figure 29 Screen shot of Hardware Setup before running the DAQ program

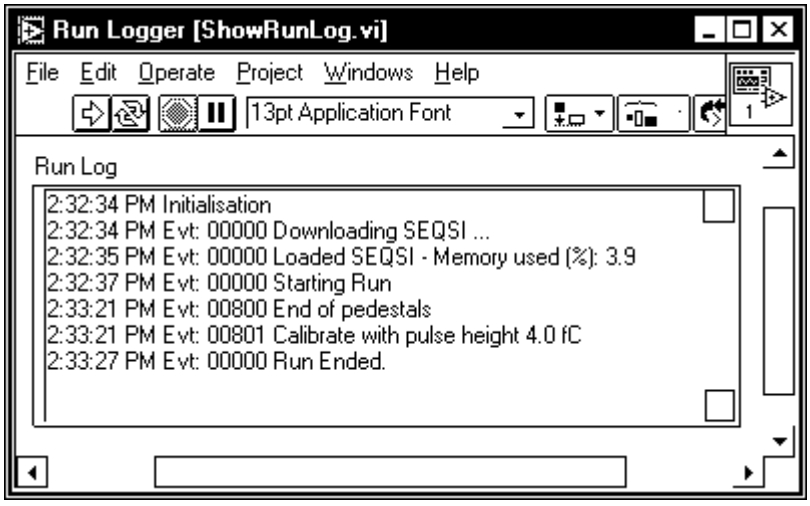

Figure 30 Screen shot of Run Logger after one run of the DAQ program

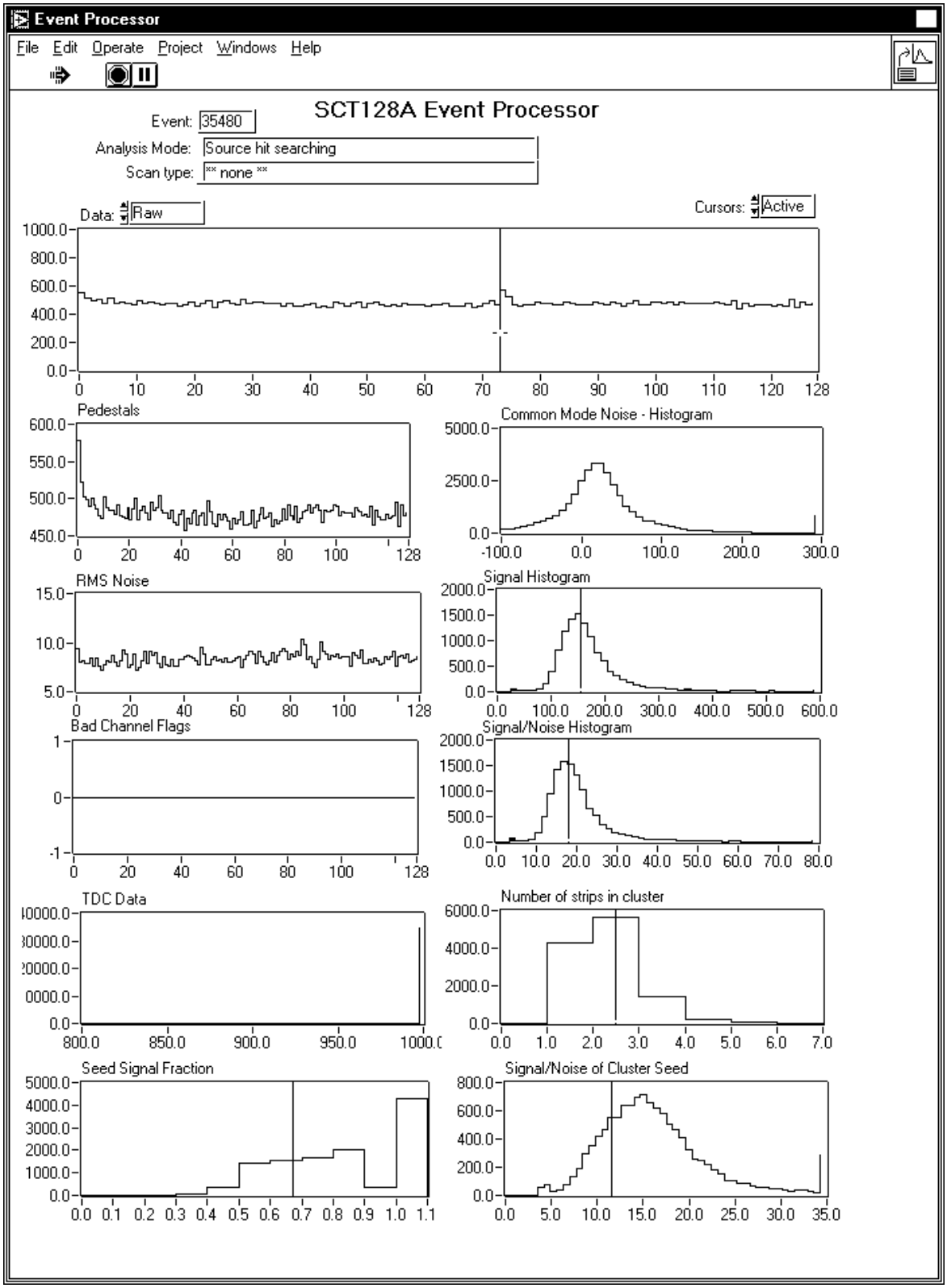

Figure 31 Screen shot of SCT128A Event Processor when running DAQ program

5.7 VME Modules

5.7.1 The importance of documentation

When getting a module, always be sure of getting the documentation for the exact same module. Without the documentation, it is extremely hard to make the module work properly. It is also a good rule to get to know how the module has been used before. Then it may be possible to find out if it is necessary to e.g. reprogram the programmable memory etc. There are so many knots, DIP switches, jumpers and programmable units that it seems impossible to figure out on your own. If just enough documentation is available, further reading and better understanding is always possible. New things can be tried out, and then it is possible to go a little step further in the debugging.

5.7.2 Introduction to VMEbus

The term "bus" is a generic term describing a computer data path, hence the name VMEbus. VMEbus is a computer architecture, and is defined by the IEEE 1014-1987 standard. Actually, the origin of the term "VME" has never been formally defined. Other widely used definitions are VERSAbus-E, VERSAModule Europe and VERSAModule European. However, the term "Eurocard" tends to fit better, as VMEbus was originally a combination of the VERSAbus electrical standard and the Eurocard mechanical form factor.

VME bus (Versa Module Europe) is a flexible open-ended bus system, which makes use of the Eurocard standard. It was introduced by Motorola, Phillips, Thompson and Mostek in 1981. VME bus was intended to be a flexible environment, supporting a variety of computing intensive tasks, and has become a very popular protocol in the computer industry.

The VMEbus architects were challenged with defining a new bus that would be microprocessor independent, easily upgraded from 16 to 32-bit data paths, implement a reliable mechanical standard and allow independent vendors to build compatible products. No proprietary rights were assigned to the new bus, which helped stimulate third part product development. Anyone can make VMEbus products without any royalty fees or licenses.

The bus usage was developed from a computing point of view, which leads to a completely memory mapped scheme. Every device can be viewed as an address, or block of addresses. Under VME, addresses and data are not multiplexed. A block transfer, however, is possible for DMA style applications. The bus allows multiple masters, and contains a powerful interrupt scheme. A resource manager is required to handle the interrupts. The VME bus is a TTL based backplane, which although the system is asynchronous, sets the data transfer speed to approximately 20 Mbytes per second.

A typical transfer consists of an arbitration cycle (to gain bus control), an address cycle (to select the register) and the actual data cycle. Read, write, modify and block transfers are supported.

The VME bus system consists of 4 sub-buses, the Data Transfer Bus, the Arbitration Bus, the Priority Interrupt Bus and the Utility Bus. Data transfer is asynchronous supporting modules with a broad variety of response times.

Since its introduction, VMEbus has generated thousands of products, and attracted hundreds of manufacturers of boards, mechanical hardware, software and bus interface chips. It continues to grow and support diverse applications such as industrial controls, military, medical, aerospace, transportation, telecommunications, office automation, instrumentation systems and high-energy physics [19].

5.7.3 VME Modules

Due to the poor documentation of the modules, we decided to bring some information of the hardware settings. Experience shows that it is almost impossible to write a plain recipe for all the knobs, jumpers and settings. The cards shown with pictures and explanations are the following:

- MXI-2 Cable
- PCI-MXI-2 Card
- VME-MXI-2 module
- CORBO
- SIROCCO
- SEQSI

5.7.4 MXI-2 Cable

The MXI-2 (Multisystem eXtension Interface) is a high speed, 32-bit multimaster system bus, with a cable between the PCI-MXI-2 and the VME-MXI-2 modules. The "2" indicates that the cable is actually separated in two parallel cables. It provides the communication between two physically separated devices, and operates like modern backplane computer buses. By including VXI-triggers, it expands the number of signals on the cable and all of the utility bus signals. Because MXI-2 incorporates all these signals into a single connector, the triggers, interrupts, and utility signals can be extended, not only to other mainframes but also to the local CPU. The MXI-2 products achieve high-performance block transfer rates by integrating the MITE custom ASIC, a sophisticated dual-channel DMA controller with standard interfaces for VXI, VME, MXI, PCI and PXI. By using MITE DMA to transfer data and commands to and from devices, the MITE frees up a computer's microprocessor to perform other tasks, such as data analysis and presentation. In addition to DMA, the MITE incorporates both the new Synchronous MXI protocol and VME64 MBLT (8-byte block transfers in which both the address bus and data bus are used to transfer data directly into the ASIC) to perform the fastest transfers to instruments.

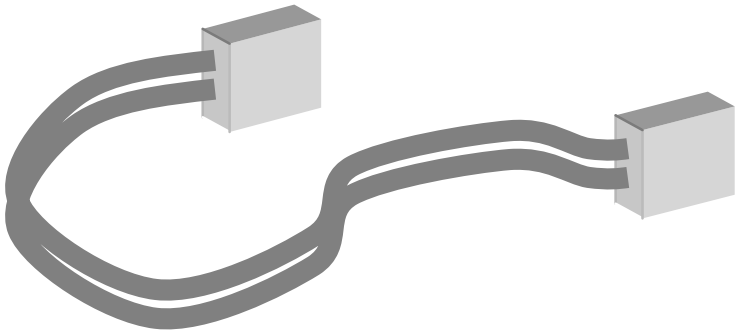

Figure 32 MXI VXI 2 Cable (National Instrument)

It is important to be aware that the cable is directional, one end must be connected to the PC end and the other to the VME end, not the other way around. To find out which end shall be connected to the PC, read on the cable.

5.7.5 PCI-MXI-2 Card

The PCI-MXI-2 is a half-size, PCI-compatible plug in circuit board that goes into one of the expansion slots in the PCI-based computer, and links the computer directly to the MXIbus. Because the PCI-MXI-2 use the same communication register set that other VXIbus message-based device use, other MXIbus devices see the board as a VXIbus device. In addition, it is possible to have up to 16MB of onboard DRAM on the board that can be shared with the MXIbus and VMEbus, and used as a dedicated data buffer. The PCI-MXI-2 has an onboard EEPROM, which stores default register values that are loaded at power-on.

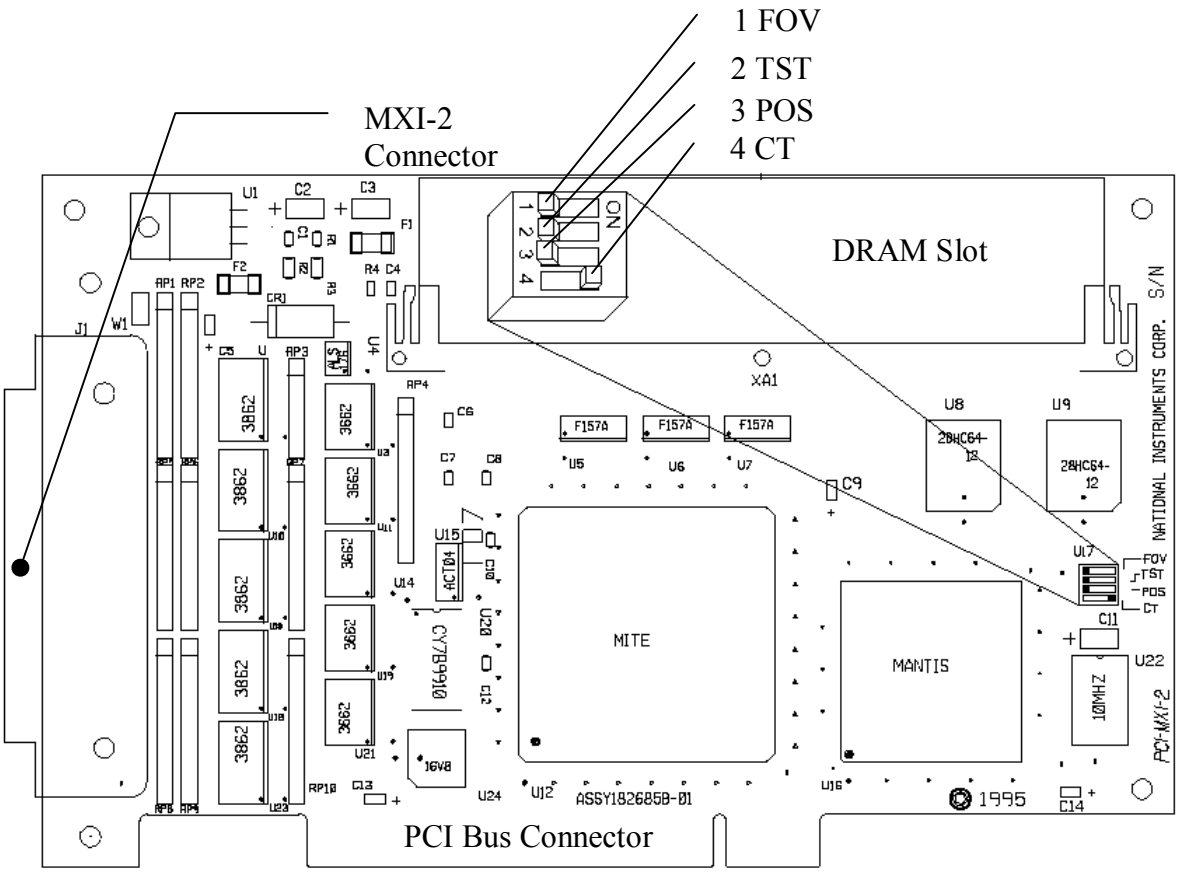

Figure 33 PCI-MXI-2 Card (National Instrument)

Figure 33 shows the default settings of the four-way DIP switch on the PCI-MXI-2 card. Unless problems arises, leave these switches in default position. Certain EEPROM configurations can cause the PCI-based computer to lock up while it is in its boot process. Generally, only the size and location of the memory windows can cause the PCI-MXI-2 to lock up the system. For example, many PCI-based computers will not boot if a board in the system requests more memory space than the computer can allocate. If this situation is reached the size of the PCI-MXI-2 user window should be reduced.

The EEPROM is divided into two halves, so that one half can be modified, while the factory-configured half retains a backup of the default user settings. To fix an invalid EEPROM setting, use switch 1 (FOV) of the four-position switch to control the operation of the EEPROM. Switch 1 determines whether the PCI-MXI-2 boots from the factory-configured half or the user-configurable half. In its default setting, the PCI-MXI-2 boots from the user-configurable half.

The 2 TST switch changes the default factory configuration settings by permitting writes to the factory settings section of the EEPROM. This switch serves as a safety measure, and is not needed under normal circumstances. When this switch is off (its default setting), the factory configuration of the EEPROM is protected, so any writes to the factory area are ignored. The factory area is protected regardless of the setting of switch 1.
Do not alter the settings of switches 3 and 4. Leave these switches as shown unless specifically directed by National Instruments.

5.7.6 VME-MXI-2 module

The VME-MXI-2 module is a single-slot, double-height VMEbus device, with optional VMEbus System Controller functions. It uses address mapping to convert MXIbus cycles into VMEbus cycles and vice versa. By connecting to the PCI-MXI-2, it links the PCI bus to the VMEbus. The VME-MXI-2 can automatically determine if it is located in the first slot of a VMEbus chassis, and if it is the MXIbus System Controller. The VME-MXI-2 requires that the VMEbus chassis comply with the VME64 protocol, to be able to auto-detect Slot 1.

VME-MXI-2 automatically terminates the MXIbus if installed as the first or the last device in the MXIbus. If installed in the middle of the MXIbus, the VME-MXI-2 automatically disables MXIbus termination.

Tree front panel LEDs:

- SYSFAIL LED indicates that the VMEbus SYSFAIL line is asserted.
- MXI LED indicates that the VME-MXI-2 is asserted from the MXIbus.
- VME LED indicates when the VME-MXI-2 is asserted from the VMEbus.

The module is placed in the first slot of the VME crate. Therefore, it is automatically detected by the system, and acts as the VMEbus system controller. Allowable logical addresses for the VME-MXI-2 range from 1 to 254 (hex FE). No other devices can use the A16 address space for the VME-MXI-2 module. The module requires at least 16kB of address space in A24 space, or at least 64kB in A32 space.

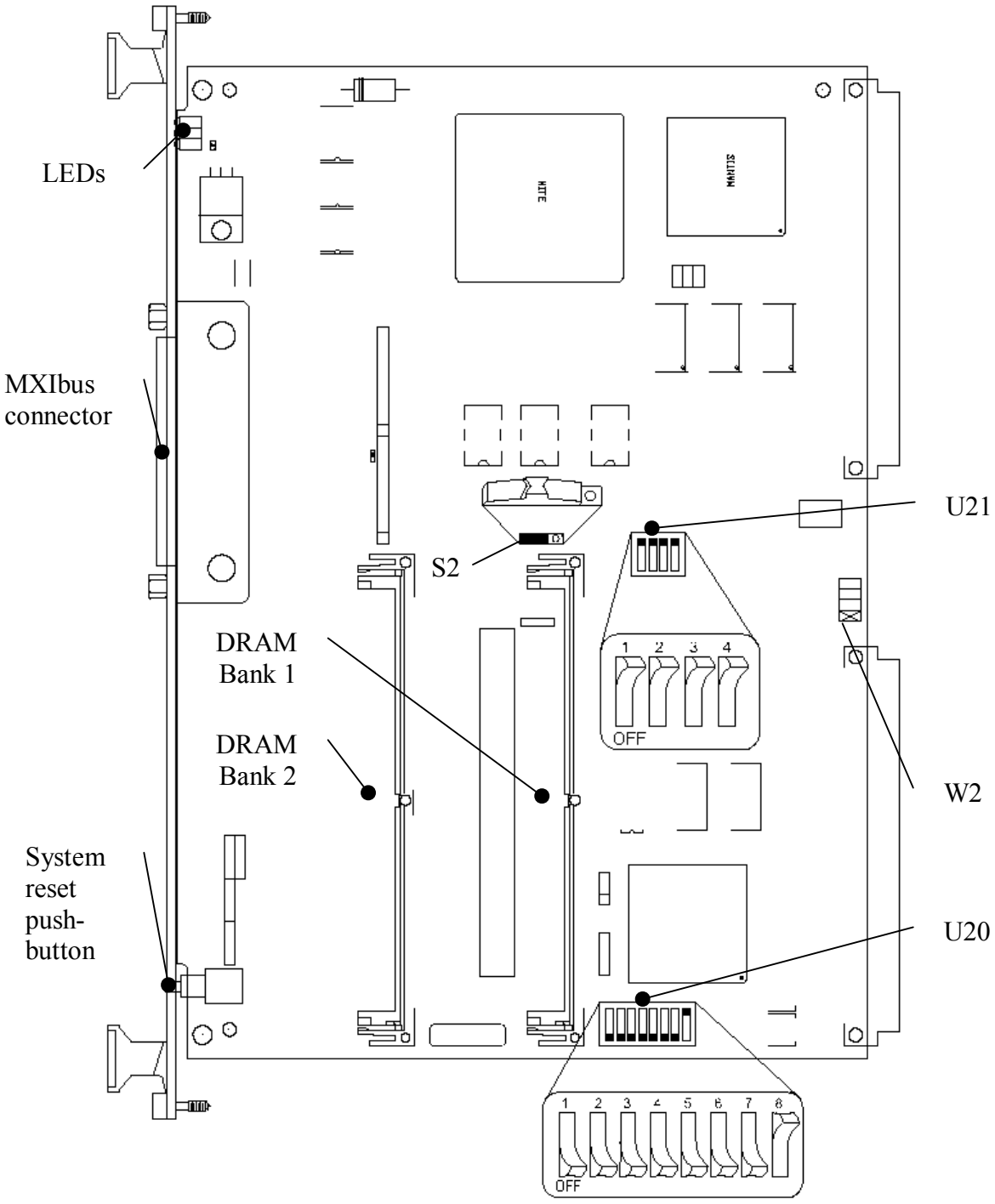

Figure 34 VME-MXI-2 module (National Instrument)

The logical address of the VXI-MXI-2 can be changed by changing the setting of the 8-bit DIP switch at location designator U20, shown in Figure 34.

The ON position of the DIP switch corresponds to a logic value of 0, and the OFF position corresponds to a logic value of 1. The data acquisition system uses the default settings hex 1 that gives binary value 0000 0001, shown in Figure 34.

Verify that the VXI-MXI-2 does not have the same logical address as any other statically configured VXIbus device in the system. Remember that logical addresses hex 0 and FF are not allowed for the VME-MXI-2, it has to be in between.

S2: Used to select the Onboard DRAM SIMM size (SIMM Single In-line Memory Module). No onboard DRAM is needed in this setup, and the S2 switch can stay as default to the left, like S2 in Figure 34.

W2: The fourth position on the jumper is the factory-default setting, which does not connect the VME-MXI-2 to any user-defined pin. Use this option only if a single VME-MXI-2 is installed in a chassis.

U21 (On/Off) respectively:
1. Boot from (User/Factory) configuration
2. Factory configuration (Unprotected/Protected)
3. (Unautomatic/Automatic) MXIbus termination
4. (On/Off) MXIbus termination, (not activated unless switch 3 is in unautomatic position)

The run data acquisition program uses the settings that boots from factory configurations. Factory configuration is protected, and uses automatic MXIbus termination, which is done by setting DIP switch at location designator U21, as shown in Figure 34.

5.7.7 CORBO

We often face the problem of trigger distribution and readout dead time control in data acquisition systems based on VME bus architecture, with either one or more processors scattered in different crates. The CORBO module (CES RCB 8047) has been specially designed to meet those requirements. The CORBO is a VME read-out control board. It has four identical channels containing a trigger input, a busy output, two VME interrupt generators and two counters.

The main use of the module is in the following scenario: A trigger generates a busy signal and a VME interrupt. The event counter is incremented by one, and the dead time counter starts counting the slow clock signal (100 μs period). The busy signal will remain active until it is cleared by a VME access, preventing acceptance of other triggers. The dead time counter gives a measurement of the busy active time. If the busy remains active too long, VME interrupt is sent [20].

The trigger input may be the front panel input, the front panel differential bus input, the front panel push button, or the signal generated by a software access to a VME register. The event counter may count either the busy signal, or the trigger input.

The CORBO features are:

- It handles up to four event interrupt signals.
- Trigger and clear inputs: NIM, TTL or differential.
- Busy output: NIM, TTL or differential signal.
- Slow clock frequency: 10 KHz.
- Slow clock output level: NIM or TTL.
- Four 32-bit fully programmable event number counters.
- Four 16-bit fully programmable dead time measurement counters.

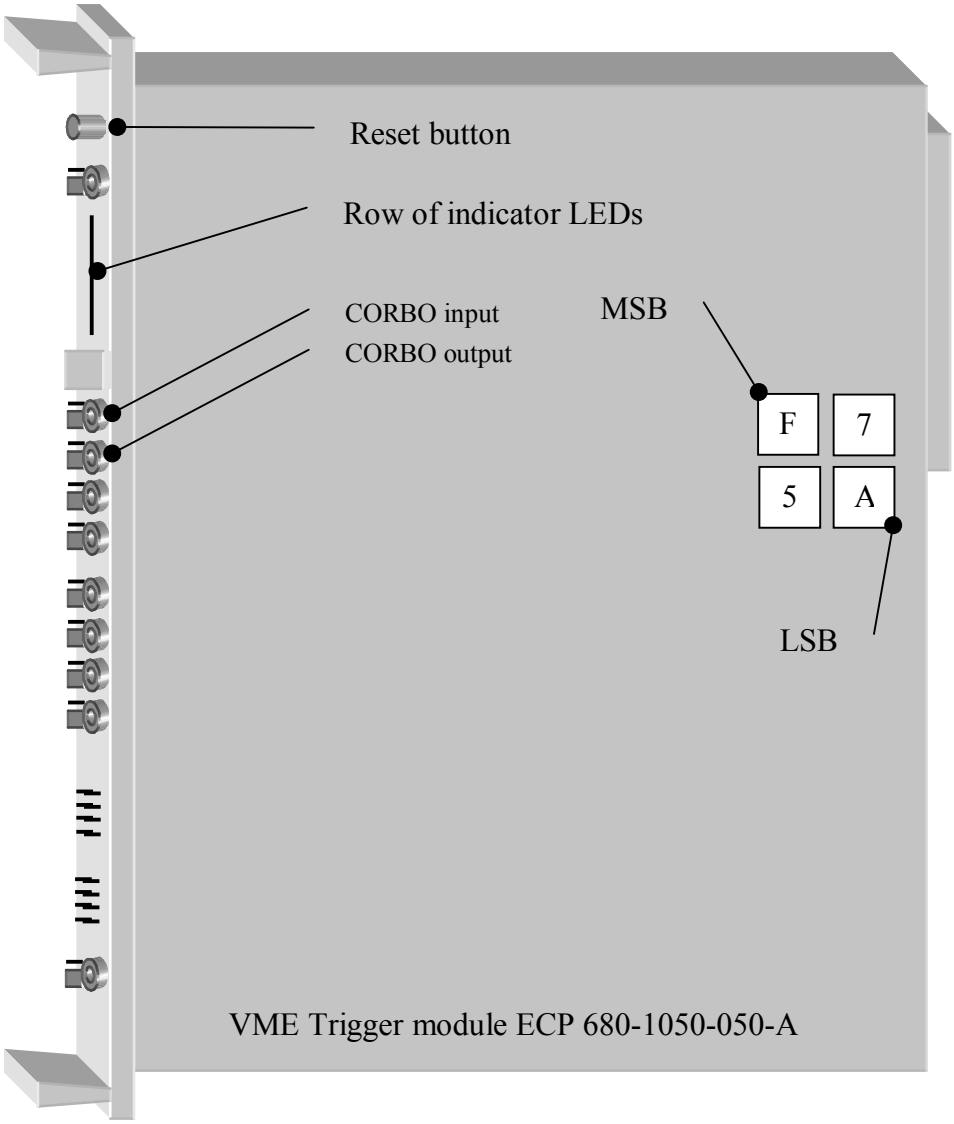

Figure 35 CORBO (CES)

The base address is F75A hex, and is set with rotary switches shown in Figure 35. The most significant bit (MSB) and the last significant bit (LSB) are marked. The hexadecimal F corresponds to the address space <A23:A20>, 7 to <A19:A16>, 5 to <A15:A12> and A to <A11:A08>. There is one input and one output used on this module. The input is the CORBO Trig that trigs the CORBO. This signal comes from the second AND gate at the NIM logic, see Figure 39. The output is the CORBO Not Busy. Here it was said that the CORBO output could go directly into the first input on the second AND gate. This did not work, and to get the system running we had to invert the output from the CORBO with NIM logic. This means that what comes out of the CORBO is the busy signal, and has to be inverted.

Front panel input and output can either be NIM or ECL. NIM is chosen by setting the jumpers beside the lemo connectors downwards, marked whit an N, shown in Figure 35.

5.7.8 SIROCCO / VFAS

The SIROCCO is used to convert analog signals to digital signals. The converted ADC-values are then stored in the SIROCCO's on-board memory, until they are read out and saved to a file through the VME bus. The SIROCCO is a general-purpose ADC converter having (in the basic version) 2 analog channels per VME module, 12 bit resolution, 40 MHz maximum conversion rate and a memory of 8192 samples (strips) per event. The analog input range is of ± 1V (2 V peak to peak), and the baseline position can be adjusted using potentiometers and monitor pins on the front panel. 12 bit resolution gives 2^{12} = 4096 channels. Since we have 2 V peak to peak, this gives 2 V / 4096 channels = 0,49 mV pr channel.

We found problems with our module. The adjustable potentiometer had bad contacts, but after soldering, it looked better. However the monitor pin 1 and 2 gave a continuous 5 V signal, instead of the readout train. The monitor pins shows the last analog readout train of the signal before it goes into the analog to digital converter. As long as we could see our signal at the input but not on the monitor pin, there had to be another hardware failure with the SIROCCO. The most probable was that the input amplifier was broken. After some measurements, we ordered some onboard circuits, CLS428 and AD712. Then we unsoldered the old ones, replaced them with new ones, and a 260 Ω resistor was also replaced. Unfortunately it did not change the strange measurement at the monitor pin, and it turned out that a special fuse had to be replaced. Then finally we could see the readout train at the monitor pin, just before it went into the analog to digital converter. After further tuning, the SIROCCO finally started to sample signals, and the red LED on the upper part of the SIROCCO lit up.

The operation mode includes an acquisition ended by an external stop pulse. In addition to the analog inputs, the module has also two coaxial lemo connectors on the front panel, and each can be configured as a NIM Input or Output for the control/synchronisation signals. It also has 17 hardware-configurable, digital input-outputs, accepting differential TTL and/or ECL standard. The configuration of Digital Inputs/Outputs and the module control logic can be set-up and adopted for the specific application, using straps and/or Xilinx programming. In order to optimize readout speed, data transfers are organised in Long words (32 bits) containing the information of 2 channels per event. The unit is a single width, 6U high, D32 A32 VME module, which uses J1 and J2 connectors. This ensures the compatibility with all standard VME crates [21].

Only few VME commands are required to run the SIROCCO module in the basic application. The Reset Command stops the acquisition cycle at any time, and sets the Status Flag in the Status Register to 0. The Start Command begins the acquisition cycle, or arm the module preparing it to accept an external (front-panel) Clock and/or Startcount Signal. In both cases the Status Flag is set to 1. The Counter Register Read/Write Command reads/sets the acquisition end/start memory addresses. The Status Register Read/Write Command allows to detect the acquisition cycle termination (Status Flag), and to handle Digital I/O Ports. The Memory Read/Write Command is used to read the acquisition results, and to test the memory hardware.

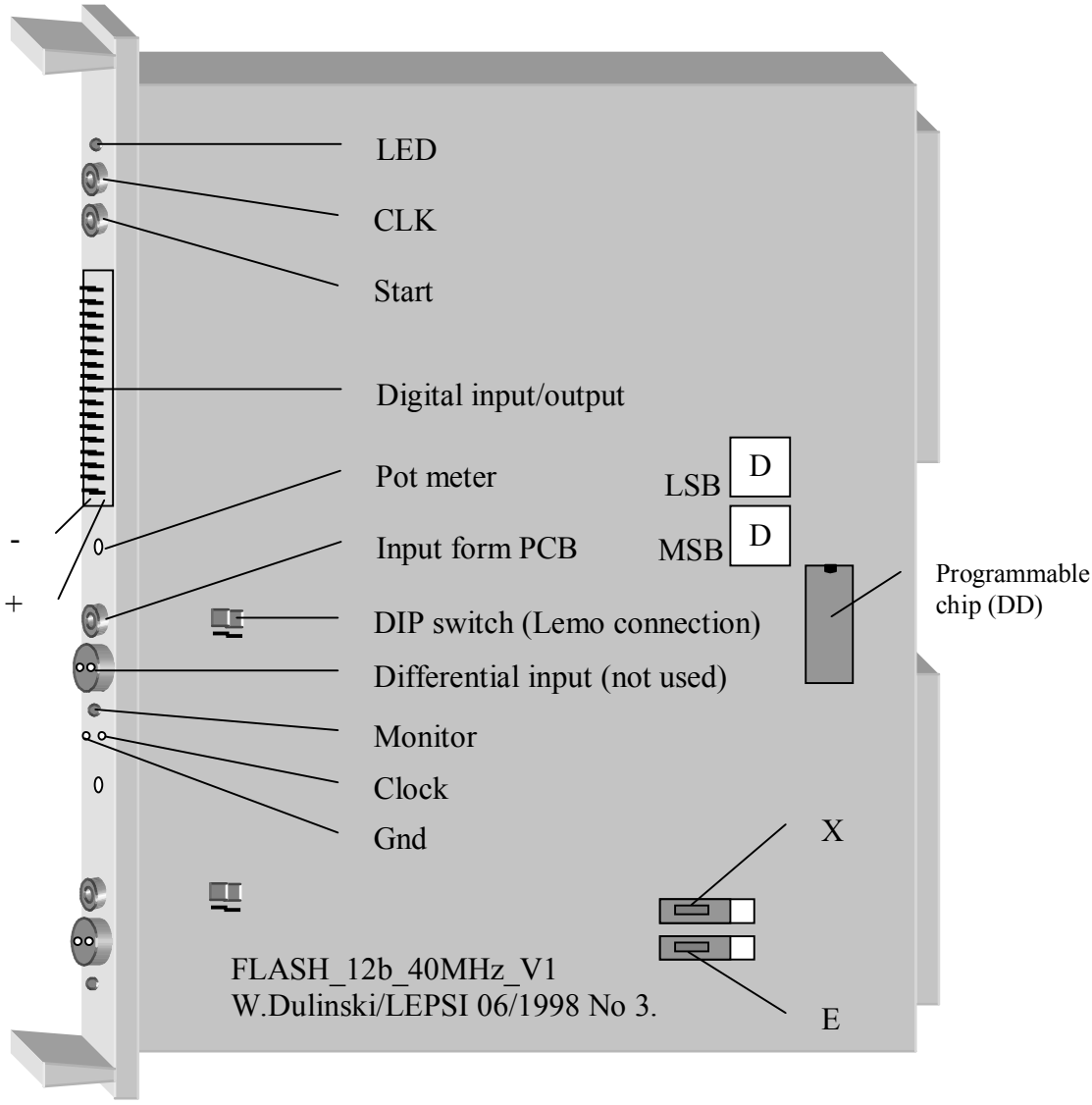

Figure 36 SIROCCO (W.Dulinski) Analog to digital converter

The base address for the old SIROCCO is C2 hex, but for the newer module the base address is DD hex. The most significant bit is marked MSB, and the least significant bit is marked LSB.

Analog signals may be provided either as unipolar (coaxial lemo connector), or bipolar (differential lemo2 connector), selected by jumpers right behind the input from the PCB. For getting the signal into the analog to digital converter through the upper lemo input, the two jumpers have to connect the two uppermost pins vertically.

The switches at the lower right part of the module has to be set in the position shown in the figure above, otherwise the SIROCCO will not communicate correctly with the data acquisition program.

The chip marked on the figure contains a programmed hexadecimal number for the two uppermost 32 bits of the base address. In order to work, this has to be DD hex.

5.7.9 SEQSI

An important part of the test setup is a sequencer board called SEQSI. It is essentially a programmable multi channel pulse generator, which may be used to provide control signals for driving silicon detector front-end readout chips. It is, however, a general-purpose module, and is not restricted to any particular chip or readout system.

The two middle lemo connectors B30 and TR are used. The B30 is an output "sync start" that provides the input to the NIM logic. It is pulsed only at the start of the run (it is used to set a latch in NIM logic, at the start of the run). The TR is an input that comes from the NIM logic called "SEQSI trig" it is provided to allow sequences to be initiated by external random triggers.

B29, CLK and the 34-pins PL1 connector are not used, except from a check that the 40 MHz CLK pulse is present at NIM level. Instead of using the CLK we use the channel one from the ECL/NIM/ECL converter, since this clock signal is sharper and better than the CLK output from the SEQSI.

In our setup, the SEQSI sends signals to the SCTA128 chip through the 50-way PL2 front panel contact. It consists of two vertical columns with 25 pins each, where the pin pair gives a signal and its inverted twin. All these signals are therefore output as differential ECL. A twisted pair cable goes to a NIM module ECL/NIM/ECL converter, where some of the signals from the SEQSI also are connected to the NIM logic. Further from the ECL/NIM/ECL converter there goes another twisted pair cable to the readout PCB, where the upper 16 pins are used.

The format of the sequencer is a single width, U6 high, D16 A24 VME module. Where D16 means a 16 bits data bus, and A24, a 24 bits address bus. The data memory is 32 bits wide, and 64kbits deep. There are 22 output channels for external use, B(0:19) and B(29:30), together with four clock lines. B27, B28 and B31 are used internally [22].

It uses + 5V, and because of its ECL logic, -5.2V. The -5.2 V (not a VME standard supply voltage) can be provided either via the J2 connector (using VXI defined pins), or by using the JAUX connector as used on the CERN type VME crates. Most VME crates other than the CERN type are incompatible with a module fitted with a JAUX connector. Therefore sequencers will be supplied with either JAUX or J2 as specified by the user.

It has been very hard to get the SEQSI working, but it would be rather unnecessary to write about all the problems and how they were solved, since they mostly were hardware failure with the different SEQSI's, and will not be the type of problems that may occur in a normal setup. There were problems with getting access to the memory of the module. Even though three different program packages were tried (LabVIEW, C++ and VIC from National Instrument), noting seemed to work.

Table 8 Memory map for the SEQSI module

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x00						Seq Mem Data <15:0>										
0x02						Seq Mem Data <31:16>										
0x04						JumpAddr Reg										
0x06						Interrupt Addr Reg										
0x08						Clock Control Reg								Clock speed		
0x0A						Polarity Control Reg										
0x0C							Direct Reg									
0x0E						Signal Control Reg										
0x16					Memory Address Counter											
0x18						Memory Date Register										
0x1E								Input								

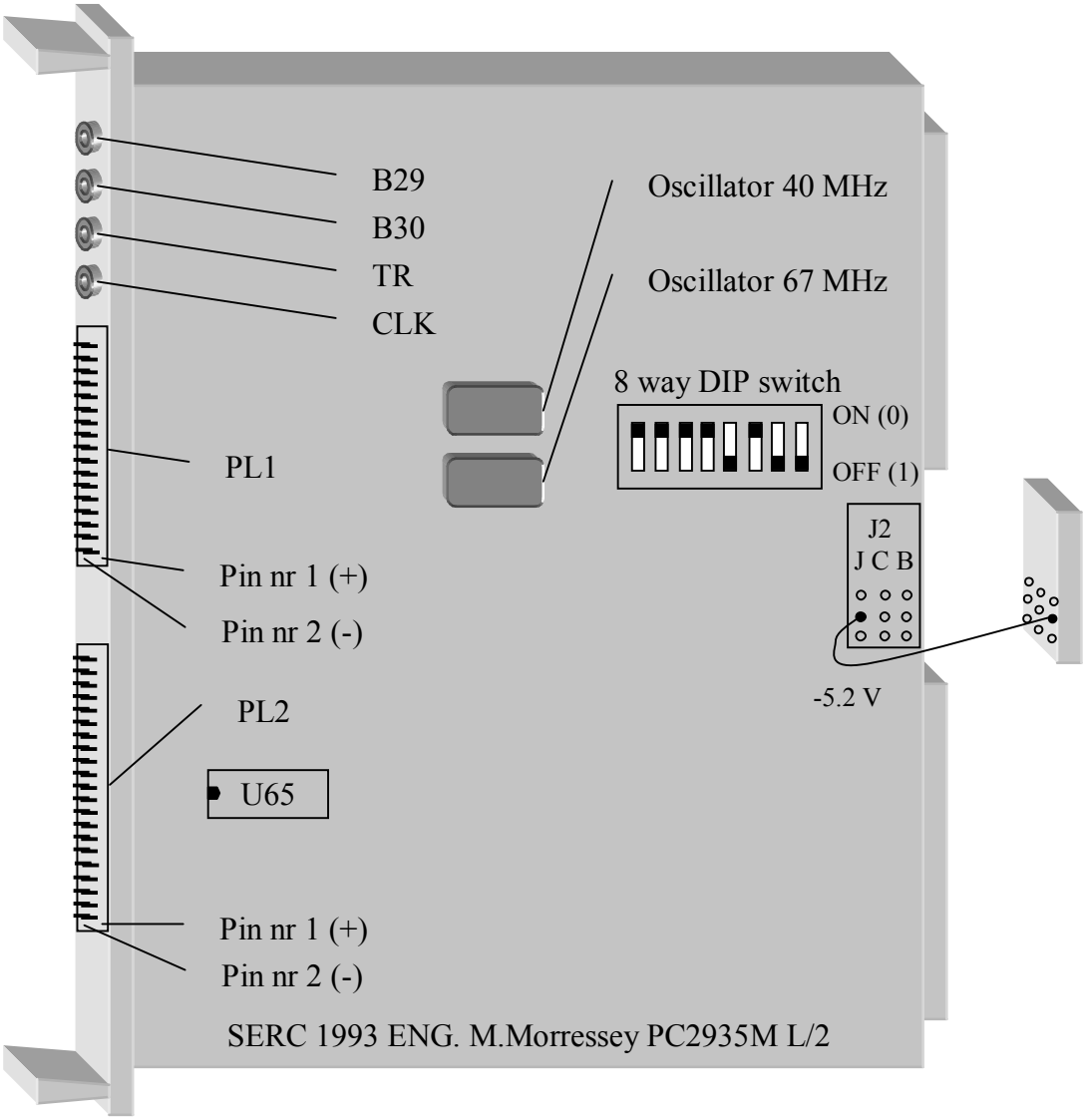

Figure 37 SEQSI (M.Morressey) Sequenser

The VME address in the LabVIEW program was 0xD00000, so the base address to the SEQSI is D0 hex. The most significant bit is marked MSB, and the least significant bit is marked LSB. The hexadecimal D hex is written 1101 binary, and the hexadecimal 0 hex is 0000. This gives 8 binary values 10110000 that are set by the 8-way DIP switch shown in Figure 38.

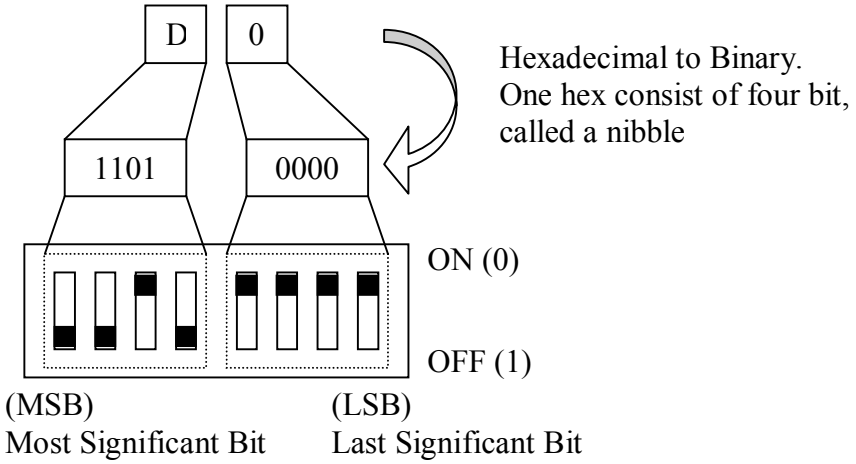

Figure 38 Base address on a 8 way DIP switch

The leftmost switch corresponds to number 1, and the rightmost switch to number 8. For some strange reasons the switch on the SEQSI board is set in the opposite direction and the correct setting of the base address D0 hex is shown in figure Figure 37.

We found out that the ECL circuits on the SEQSI did not get its voltage, so a connection from the VME board to the backplane VME AUX/J2 bus had to be made. Getting the right - 5.2 V can be done by soldering a line on the VME board, and connect the other end into one of the two lowest slots in the AUX/J2 bus at the VME crate, as shown in Figure 37. This should of course be measured before connection, to be sure not destroying the module. To check that the module really gets its - 5.2V, the modules IC U65 pin 8 and 16 should be measuring - 5.2 V and 0 V respectively, (see Figure 36**,** the leftmost sixth IC counted from the bottom).

The cabling between the SEQSI's PL2, and the ECL/NIM/ECL converter was hard to get out of the text. Table 9 shows how to connect the cables. Flat line twisted pair cables are used. Even though it is much work, each connection should be tested, otherwise the error must be found the hard way, and we learned that this takes a lot of time.

5.7.10 TDC

A Time to Digital converter can be used to calculate the time difference between the trigger time, and the BCO clock time. This module is not used in our setup, it is just mentioned since it is included in the data acquisition program LabVIEW program. A TDC is ideal for time measurements of drift chambers, time projection chambers or other detectors requiring time interval measurements with high accuracy, and has been specially designed for high rate environments.

5.7.11 Cabling

Except from the high voltage cable to the photomultiplicator tube, and the two twisted pair cables, all cables used are lemo cables. Lemo cables have been very good and reliable to work with. Even though all of them were used ones, none of the 40 cables has ever failed. A few times some of them have needed to be tightened, which is all.

Two twisted pair cables are needed, one from the SEQSI PL2 connection to the ECL/NIM/ECL converter, and the other from the ECL/NIM/ECL converter to the SCT PCB board J1. These cablings are rather important to get right, and a cabling diagram for these connections are included in Table 9. Column two and three show connections between the SEQSI and the ECL/NIM/ECL module, and column three and four show connections between the ECL/NIM/ECL and the SCT board.

Table 9 Cabling diagram for both SEQSI and PCB to the ECL/NIM/ECL NIM module

SEQSI Chan from 0	Pin Nr. SEQSI PL2 (from 1)	ECL/NIM/ECL LRS4616 Chan No (from 1)	Pin Nr. of J1 Connector on sct board (from 1)	Description outputs(s) used from ECL/NIM/ECL
Clock	45,46	1	1,2	Clock - ECL to chip, NIM to logic
4	9,10	3	5,6	Reset - ECL to chip
5	11,12	4	7,8	Polarity - ECL to chip
6	13,14	5	9,10	Address - ECL to chip
7	15,16	6	11,12	Test enable - ECL to chip, not used
8	17,18	7	13,14	Commander - ECL to chip
9	19,20	8	15,16	Sing read 0 - ECL to chip
10	21,22	9	17,18	Muxtestenable - ECL to chip, not used
11	23,24	10	n/a	SIROCCO strobe (sync stop) NIM to logic
12	25,26	11	n/a	Not used
13	27,28	12	n/a	Trsynchro - not used (historical)
14	29,30	13	n/a	Software trigger - NIM to logic
15	31,32	14	n/a	Enable source trigs - NIM to logic
16	33,34	15	n/a	SIROCCO gate - NIM to logic
17	35,36	16	n/a	TDC stop - ECL to TDC module
30NIM	n/a	n/a	n/a	SIROCCO strobe (sync start) to NIM logic

5.8 NIM Modules

NIM, an acronym for Nuclear Instrument Module, is a standard that was created by a committee in the mid-sixties for a number of reasons. It was found that various circuit elements such as discriminators, logic units, amplifiers etc, were common to most nuclear and particle physics experiments, and a standard that would allow a greater degree of modularity of these devices was desired. A standard would allow greater flexibility, and reduce the cost of producing custom made devices to suit a particular experimental setup, by allowing devices to be reused.

NIM modules are stand-alone modules for basic electronic functions, like discriminators, amplifiers, delay and any type of logic unit (and, or, not etc.). The power supply, which is in general, detachable from the NIM bin, is required to deliver voltages of + 6 V, - 6 V, + 12 V, - 12 V, + 24 V, and - 24 V. Standard NIM modules are required to have a height of 22,2 cm, and must have a width which is a multiple of 3,4 cm.

Two types of standards exist, slow-positive logic and fast-negative logic. In our setup we used fast-negative logic, often referred to as NIM logic. Since these values often are measured for testing and debugging in the system, a table of the defined values is given below [10].

Fast-negative NIM logic (Current into 50 Ω)		
	Output must deliver	Input must accept
Logic 1	- 14mA to - 18mA	- 12mA to - 36mA
Logic 0	- 1mA to + 1mA	- 4mA to + 20mA

Table 10 Fast-negative NIM logic (Current into 50 Ω)

The signals are transferred between the modules with thin lemo cables, for the old modules also with BNC cables, both being coaxial.

TTL and ECL are other logic standards commonly found in NIM systems. The first TTL (Transistor-Transistor Logic) logic family is a positive going logic, which is very often found on NIM electronics modules. The second is a logic family, which is becoming increasingly popular in high-energy physics. This is the emitter-coupled logic (ECL) family that is currently the fastest form of digital logic available. Be aware that NIM and ECL have logic 1 for the lowest voltage, and that the TTL have logic 1 for the highest voltage.

	NIM	TTL	ECL
Logic 1	-0.8V	2-5V	-0.90V
Logic 0	0.0V	0-0.8V	-1.75V

Table 11 Signal levels for NIM, TTL and ECL

5.8.1 NIM Logic

The NIM logic is divided in two main parts. The first one is the triggering part, which generates trigger signals to the CORBO and the SEQSI (also for the TDC for those how use it). The software communicates with the SEQSI through the VME bus, and the SEQSI sends out X14 and X15 through PL2 out to the ECL/NIM/ECL converter via the twisted pair cable. Using lemo cables and some NIM modules, we can build up the NIM logic as drawn in Figure 1. Either X14 and Source Trig, or X13 have to be activated for generating a trigger, then if the CORBO is not busy the signal goes through the AND Gate 2 and sends a CORBO and a SEQSI trigger.

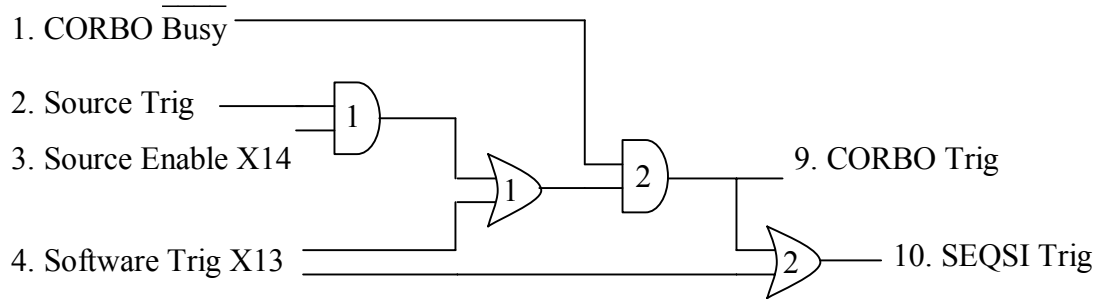

Figure 39 NIM logic for the trigger part

The original NIM logic could not get the system running, probably because of too bad signals from AND Gate 2, going into the CORBO, and from OR Gate 2, going into the SEQSI. Also the CORBO Busy signal had to be inverted. Since the rest of the setup seemed ok, a large number of combinations were tested, and finally the working combination was found, shown in Figure 40

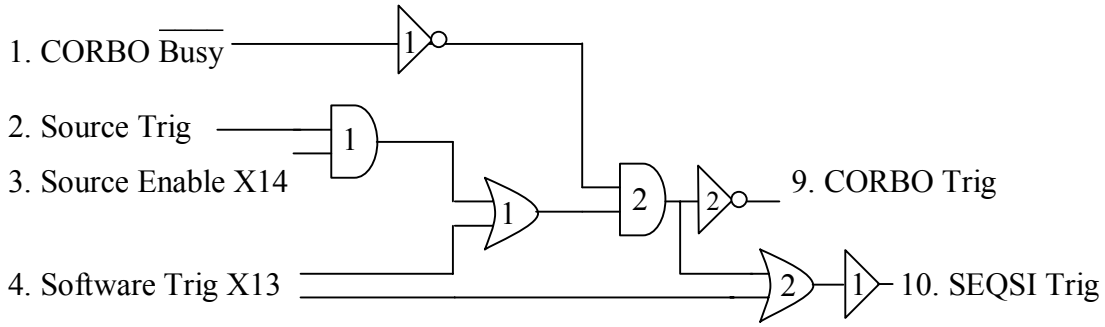

Figure 40 Modified NIM logic for the trigger part

The second part of the NIM logic concerns making the correct pulse for the SIROCCO CLK input. The software allows generating the SIROCCO strobe in two different ways, gate or strobe mode. The strobes can either be generated directly (strobe mode), or they can be generated externally, using the SEQSI to gate the externally generated strobes, so that they are in time with the data train (gate mode). The strobes or gate (depending on which method is used) is available from output X15 from the ECL/NIM/ECL converter. The mode used is selected from "SIROCCO and Clock Control" when clicking on "change Hardware Setup" after starting the runDAQ.vi.

In gate mode, B30 sets the latch high at start-up. X1 starts the gate generator, and the 40MHz clock is then scaled down to 5MHz, and then gated with the output X15 from the ECL/NIM/ECL unit (see Figure 41), so that it is in time with the data train going into the SIROCCO. X15 (SIROCCO gate) then decides the start and the length of the pulse with short continuous 5MHz positive going pulses.

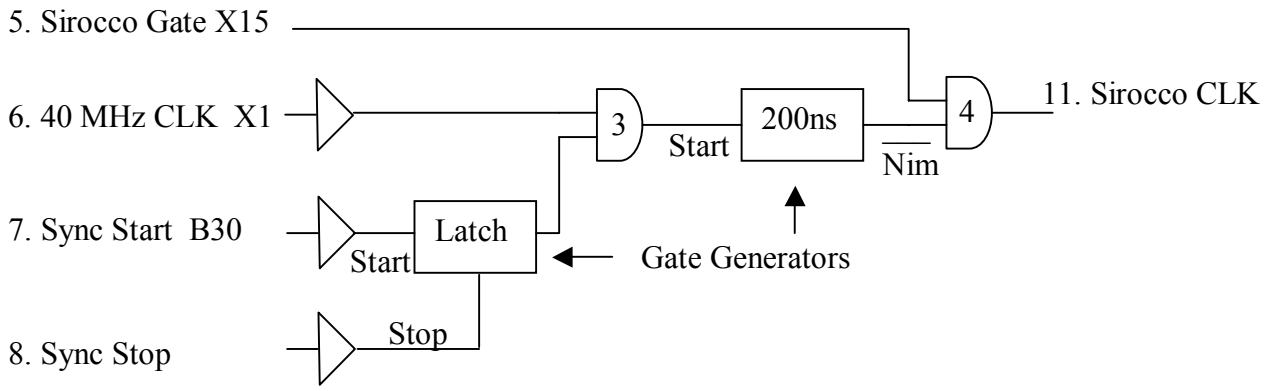

Figure 41 NIM logic for the SIROCCO CLK part

Explanations to Figure 39 and Figure 41.

1. CORBO Busy: Output from the CORBO.
2. Source Trig: Output from the scintillator. Put through a discriminator for getting logic signal.
3. Source Enable X14: Can be set by software to trig on the source.
4. Software Trig X13: Can be set by software to trig by software.
5. SIROCCO Gate X15: Can be adjusted by software.
6. 40 MHz CLK X1: Can be changed by software, also output from the SEQSI module terminal CLK.
7. Sync Start B30: Used when running the setup in strobe mode, in gate mode it is set high at once.
8. Sync Stop: Used when running the setup in strobe mode, for sending syncron stop sign.
9. CORBO Trig: Input to the CORBO (trigs the CORBO).
10. SEQSI Trig: Input to the SEQSI (trigs the SEQSI).
11. SIROCCO CLK: Clock input to the SIROCCO (see Figure 42). The SIROCCO samples the analog values at rising edge of the clock pulses, and converts them to digital bytes.

The big X and the number is output from the ECL/NIM/ECL converter NIM module. When X15 starts is decided in runDAQ.vi, "Change Hardware Setup" under "SCTA128 setup", "No of strobes / Gate Width". When X15 goes high is decided in the same window by "Delay (clocks)". In Bergen the set-up in GATE mode gave the best SIROCCO CLK with:

"No of strobes / Gate Width" = 260
"T1 Delay (clocks)" = 84

Only two things, the "Frequency" and the "No of Strobes/Gate Width", determine the width of the gate. E.g. if the "Frequency" is set to 5 MHz clock, and the "No of Strobes/Gate Width" to 260, the gate width should be 260 · 8 · 25 ns. This means that 5 MHz implies a pulse every 8 · 25ns, so if the 40 MHz clock is prescaled to produce 5 MHz, and this is ANDded with the gate, which is 260 · 8 · 25 ns, this should give ~260 strobes.

In fact, 260 strobes are not needed for the SIROCCO, but at least 140 strobes should be used. The 260 value is completely accidental, it is historical, the old SIROCCO needed 256 strobes, so 260 was used. It has been reduced when changing to the new SIROCCO. For the new SIROCCO is should work with 140.

"No of Strobes/Gate Width" is the number of strobes in strobe mode, and the gate width calculation-factor in gate mode. In gate mode the Strobe width (clocks) is not used, it is ignored.

We use the SEQSI 40 MHz clock (output X1 from ECL/NIM/ECL), and then NIM logic to convert this to 5 MHz. After that, we gate this 5MHz clock with output X15 from the ECL/NIM/ECL unit, so that it is in time with the data train going into the SIROCCO, see Figure 41.

5.9 Readout speed 5 MHz or 40 MHz

It is recommended to start running the setup in 5 MHz, because it is quite difficult to gate the data train with a 40 MHz clock. When the chip runs at less than 40 MHz (e.g. 5 MHz), the readout train is synchronised to an arbitrary pulse in the 40 MHz clock. The synchronisation occurs during the chip setup, before the first readout. Because the 5 MHz strobe is derived from the 40 MHz clock, the strobe relative to the readout train will move horizontal to the strobe, because it becomes synchronised to a different pulse in the 40 MHz clock. The purpose of the latch is to reset the data train. The B30 pulse is generated during the chip setup to pick the correct 40 MHz clock pulse, with which to start generating the 5 MHz clock.

The best way to change the gate frequency is to study the NIM output from the gate generator together with the readout train from the PCB, while running the data acquisition program. Use the readout train to trig the oscilloscope. While the oscilloscope is measuring the frequency, the potentiometer at the gate generator can be turned, until the oscilloscope shows 5, 10, 20 or 40 MHz at the same time as watching the timing. When a frequency is tuned the program should be stopped, and started again with the muxclock and the frequency that is selected. It is important that the frequency is as exact as possible, for getting the best Signal/Noise ratio. If the Signal/Noise ratio suddenly decreases, this frequency should be checked.

Running in 40 MHz without the latch and the gate generator is also possible in the newest versions of the software (version 1.2). The earlier one contained a bug for running in 40 MHz. For running it in 40 MHz, do the following:

- Set the MUXClock to 40 MHz.
- Set to gate mode.
- Set frequency to 40 MHz.
- Set no of strobes/gate width to ~150.
- For the SIROCCO strobe, the 40 MHz clock should be ANDed together with the X15.
- The latch and prescaling are not needed for running the setup in 40 MHz.

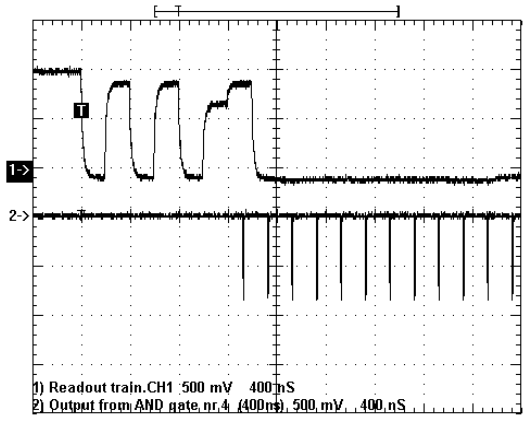

Figure 42 SCTA128HC readout train and X15

Figure 42 shows (1>) the start of the readout channel (the header and the 11 first channels) and (2>) the SIROCCO Gate X15 channel from the ECL/NIM/ECL converter.

5.10 Power supply to the PCB

The readout PCB needs 4 different voltages, these are: + 4V, + 5V, - 5 V and - 5,2 V. Instead of using four different power-supplies, we made an own PCB including all the four voltages. For this purpose we used the monolithic integrated circuit, LM317, for positive going output, and LM337 for negative going output (The following will contain mostly the positive going output, but for negative going output the circuits are mostly the same, only with LM317 replaced with LM337). The nominal output voltages are selected by means of resistive dividers, and for possible adjustments, R_2 is an adjustable resistor.

The LM317/LM337 provides an internal reference voltage of 1,25 V between the output and adjustments terminals, pin 3 and pin 1. This is used to set a constant current flow across an external resistor divider, giving an output voltage V_o of

$$V_o = V_{REF}(1 + \frac{R_2}{R_1}) + I_{ADJ} \cdot R_2 \qquad (5\text{-}1)$$

where V_o is the output voltage, V_{REF} = 1,25 V provided by the LM317, R_1 and R_2 are the V_o deciding resistors. They are designed to supply more than 1,5 A load current, and depending on the resistors R_1 and R_2, the voltage is adjustable over a 1,2 V to 37 V range. The device is designed to minimize the term I_{ADJ} (100µA max) and to maintain line and load changes. Usually, the error term $I_{ADJ} \cdot R_2$ can be neglected

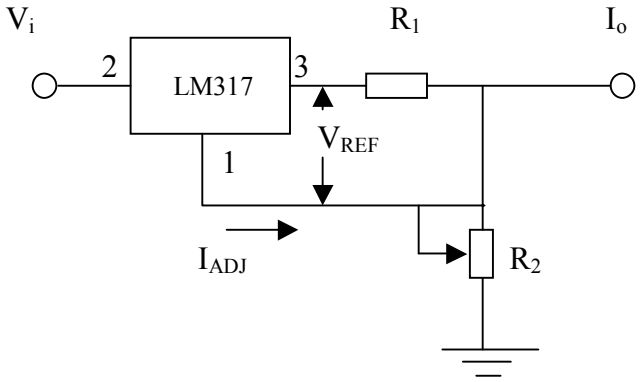

Figure 43 Basic Adjustable Voltage Regulator

The device was designed to minimize the term I_{ADJ} (100µA max), and to maintain it very constant with line and load changes, therefore the error term $I_{ADJ} \cdot R_2$ can usually be neglected. And we get:

$$V_o = V_{REF}(1 + \frac{R_2}{R_1}) \tag{5-2}$$

To avoid overloading the circuit, we also included a current regulator for each of the four voltages. Connecting a fixed resistor between the adjustment and the output of a new LM317 does this. The output current I_o [A] can then be calculated by the formula:

$$I_o = \frac{V_{REF}}{R_3} + I_{ADJ} \approx \frac{1{,}25}{R_3} \tag{5-3}$$

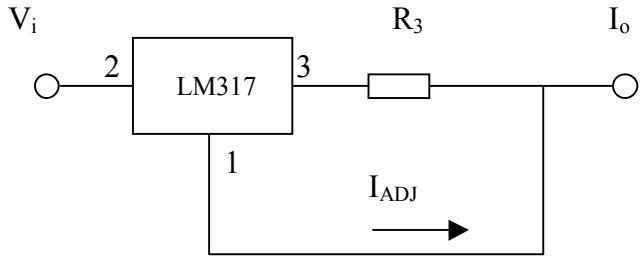

Figure 44 Current Regulator

The voltages are then created by putting a current regulator in series with a voltage regulator, and make four copies on the same PCB where two of them are designed for positive output, and two for negative.

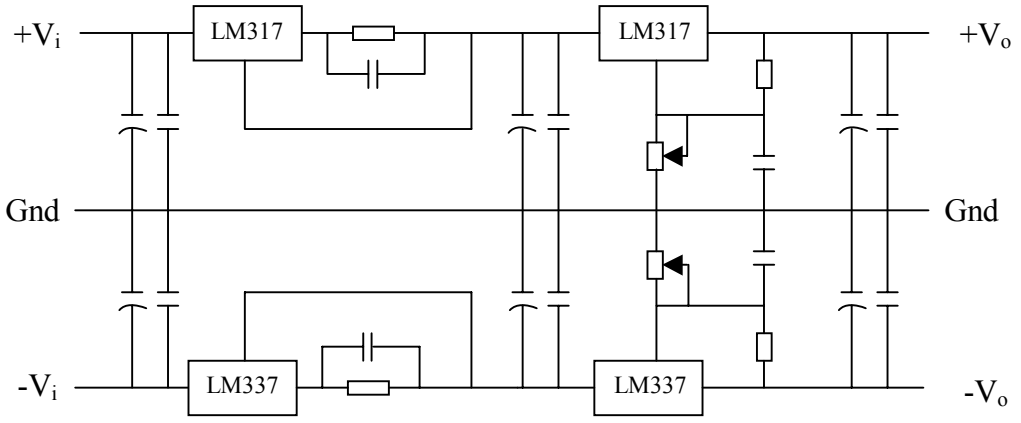

Figure 45 Circuit diagram for positive and negative current and voltage regulator

6 Studies Using the Setup

6.1 Fine Tuning The Settings for the Best Signal/Noise ratio

There are a lot of different quantities to be tuned in the Hardware Setup when starting the run of a measurement. When running the readout in gate mode the interesting settings for the SCTA128 Setup are:

- T1 Delay (cals)
- T1 Delay (source)
- Clock 1 delay (ns)
- Clock 2 delay (ns)

And for the SIROCCO and Clock Control:

- Delay (Clocks)
- No of strobes / Gate Width

6.1.1 T1 Delay (cals)

The "T1 Delay " is the position in the pipeline which is to be read out. This might be a function of the length of the cabling etc. It should become clear which is the correct setting for T1 delay. If the settings were incorrect, the signal would be very small, or completely missing. Different T1 delay for calibrates and source runs are probably needed. To search for the best T1 delay (cals), select " T1 Scan" together with "Calibrates", this will do several runs while changing the T1 Delay between each run. It was found that the optimal gain was obtained with T1 delay (cals) set at 108. For the other values of T1 Delay (cals), the output was always very small, or completely missing. The conclusion is that T1 Delay (cals) does not influence on the S/N ratio for source run, but has to be 108 for making calibration tests in our setup.

6.1.2 T1 Delay (source)

This is the main delay for timing the scintillator trig to the readout train. It is rather critical to get this delay right, otherwise the program will not run, or it will just measure noise. Each measurement contains 10 000 events, and the big difference in uncertainties are due to lower real events number for the "T1 Delay (source)", which gives bad timing. To search for the best T1 Delay (source), select " T1 Scan" together with "Source produced by", this will do several runs while changing the T1 Delay between each run. Our setup gave the best S/N ratio with T1 Delay (source) = 103, as shown in Figure 46.

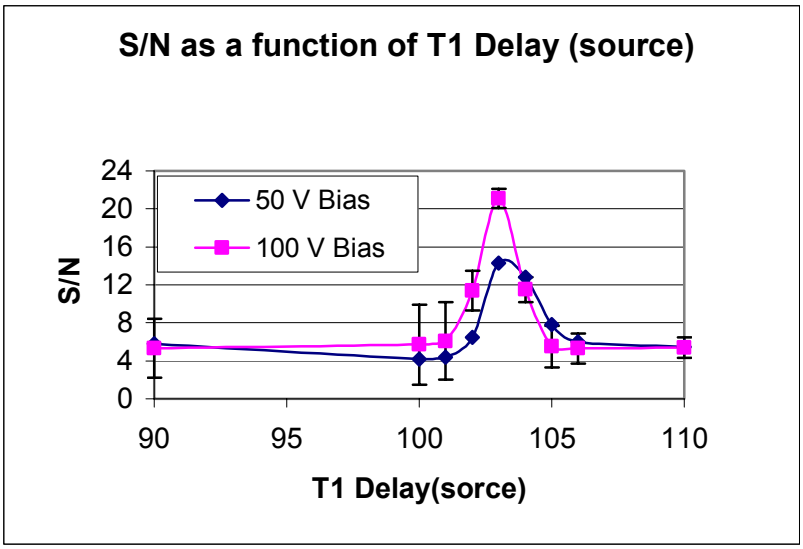

Figure 46 S/N as a function of T1 Delay (source)

6.1.3 Clock 1 delay (ns)

The "Clock 1 delay" gives the possibility to delay the clock 1 line, in up to 7 steps of 2 ns. Lots of measurements were taken with different "Clock 1 delay (ns)", but it had no influence on the measured S/N ratio. Since this delay had no influence of the S/N ratio, the Clock 1 delay was set to zero.

6.1.4 Clock 2 delay (ns)

The "Clock 2 delay" gives the possibility to delay the clock 2 line, in up to 7 steps of 2 ns. Clock 2 delay had a quite strange influence on the S/N ratio. First a tiny increase, then gone for 3 ns, and back with a lower value. To be sure that these measurements were correct, they were repeated for 5, 10 and 40 MHz readout frequencies, with 10 000 events each. The values are plotted in Figure 47 with ± one standard deviation as uncertainties. The biasing was set to 100 V.

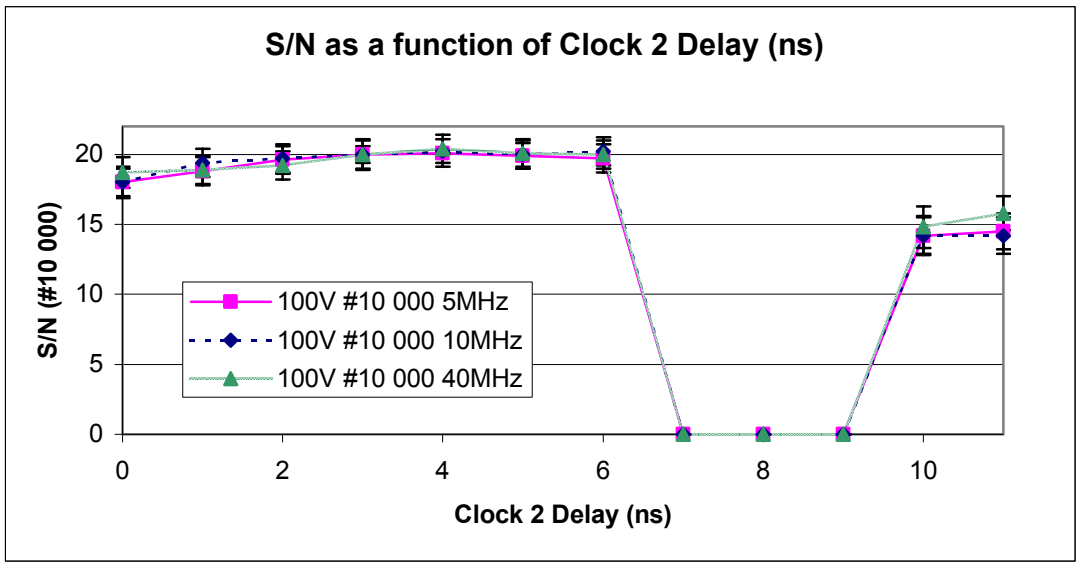

Figure 47 Most Probable S/N as a function of Clock 2 Delay (ns)

When studying the readout train for "Clock 2 Delay (ns)", set to 7, 8 or 9, all the channels decreases approximately 1 V. This is outside the SIROCCO range, and there will be no input, explaining the no S/N value. The Clock 2 Delay (ns) was set to 4, and stored in the default hardware setup file.

6.1.5 No of strobes / Gate Width

No of strobes/Gate Width is the width of the NIM gate that is ANDed with the 5 MHz clock to generate the strobes. This should be wide enough so that the number of strobes to the SIROCCO is larger than 128. We put the value to 260, just to be sure that it was enough, changing this did not change the S/N ratio.

6.1.6 Delay Clocks

"Delay (Clocks)" defines the timing of the first strobe to the SIROCCO, it actually defines the leading edge of the NIM gate that is ANDed with the 5 MHz clock that generated the strobes. Delay (Clocks) is actually best tuned by studying both the readout train and the SIROCCO CLK output from the fourth AND gate, trigging on the readout train with the oscilloscope. The clocks to the SIROCCO should look like the (2>) in Figure 70. This is not enough for fine tuning. Anyway, lots of measurements showed an interesting structure. The apparently random data shows a clear peak value for each 8th delay. This is where the SIROCCO clock fits best to the readout train. Which top to choose can be decided by having a look at the start and end of the Raw Data readout train at the SCTA128 Event Processor. Only the correct delay results in reading out all 128 channels.

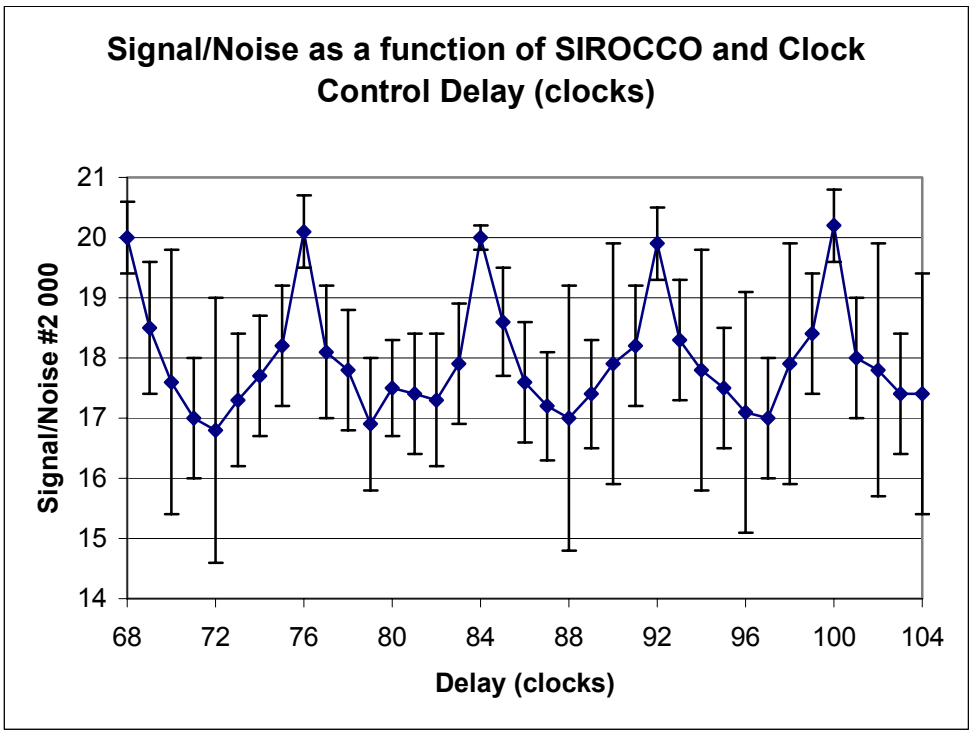

Figure 48 Signal/Noise as a function of SIROCCO and Clock Control Delay (clocks)

The conclusion is to use the oscilloscope to find the approximately right delay, and then make some measurements for some value around that point for finding the peak, and getting the best Signal/Noise ratio.

6.2 Signal/Noise versus Calibrate gain scan point

To check the linearity in the setup, some calibrate gain scan point measurement were done. The detector bonded was the oxyginated detector nr 7 Sintef preseries. The temperature while measuring was 24 ºC, and no datacut was needed. Calibrate gain scan point form 1-10 fC with step on 1 is set as default, when marking the "Gain Scan" tag in the "Readout Sequence" window. Figure 49 shows ten superimposed histograms.

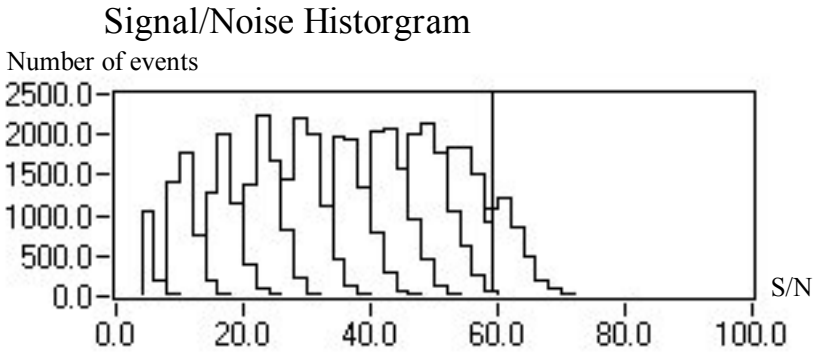

Figure 49 Signal/Noise histogram for calibrate gain scan

The data were saved to file, and the analyse program ReadHistos.vi was used to get the mean value for each scan point. The linearity was very nice, so a best-fit line was added, to see the tiny "S" shape of the Calibrate gain scan line. The equation for the best-fit line is shown in the Figure 50, showing the gradient and the crossover with the y-axis.

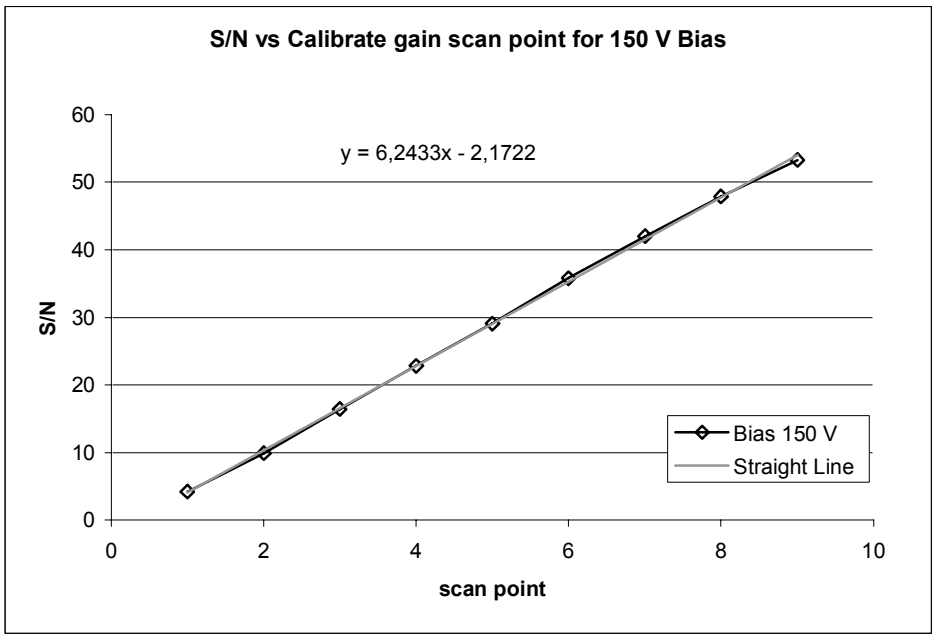

Figure 50 S/N versus Calibrate gain scan point for 150 V Bias

The linearity was also checked for different detector bias voltages, and very nice correlation was achieved. The lines for 50, 100 and 150 V are almost impossible to separate, shown in Figure 51. This is just as expected.

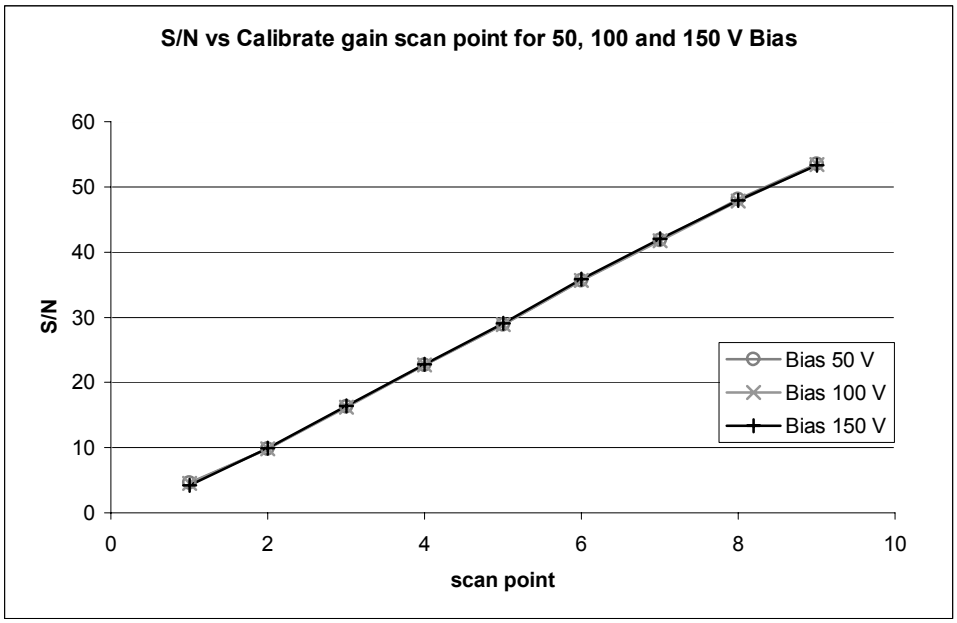

Figure 51 S/N versus Calibrate gain scan point for three different Biases

6.3 Signal/Noise versus Detector Voltage

All the following measurements are done on the oxygenated detector number 108 from Sintef preseries, if not it is specified otherwise. The strip length is 62 mm, and the 128 channels were bonded to strips number 129-256 of the detector. The temperature during the measurements was 25-26°C. The supply voltages to the SCTA128HC Chip is shown in Figure 22. To avoid the inclusion of possible large noise pulses, averages were calculated using only S/N values below 34.5. This makes the Signal/Noise averages a bit smaller than the true average. New measurements were done on the second detector, and it showed up that the peak could be avoided using other values in the histogram window, and the big pulses were due to the Landau tail.

It is known that the Signal/Noise ratio, as function of detector bias will increase until a certain level, and then stabilize. The plot in Figure 52 shows a quite flat line from about 90 V and above. Each measurement is done with 10 000 events, and the uncertainties plotted are ± one standard deviation calculated for each measurement. The readout frequency for this measurement was 5 MHz.

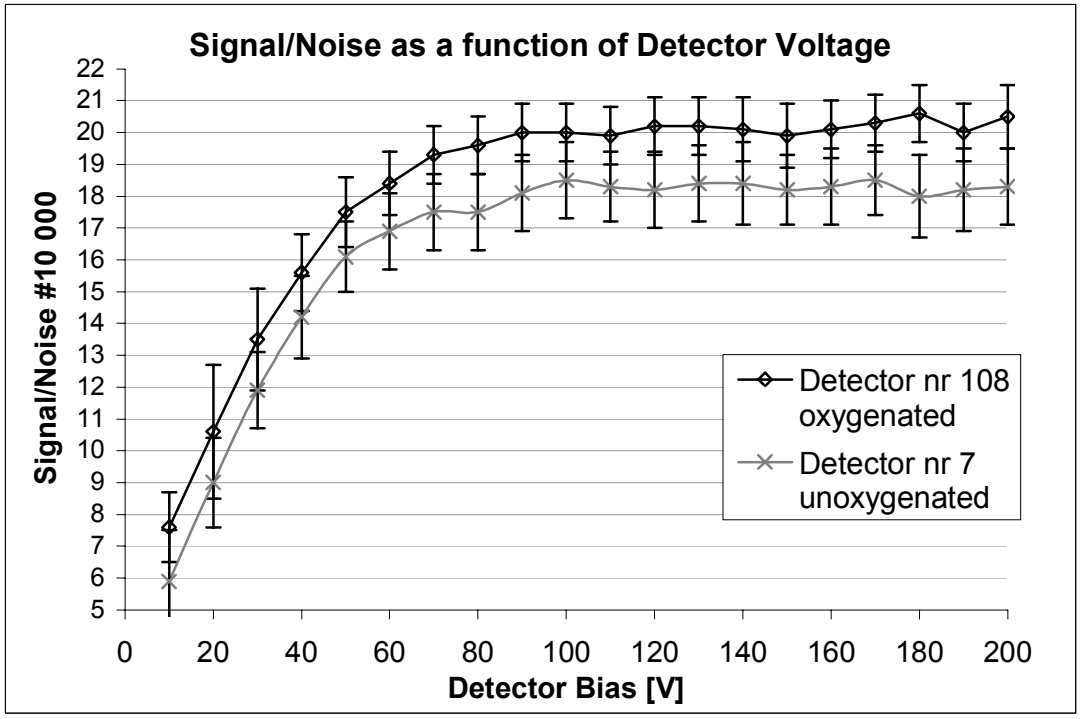

Figure 52 Signal/Noise as a function of Detector Voltage

Figure 52 clearly shows that detector nr 108 has a higher S/N ratio than detector nr 7. This is expected since detector nr 7 is thinner, and therefore gives a slightly lower signal.

The mean S/N ratio averaged over the datapoints from 100 V up to 200 V, is 20.2 ± 0.4 for detector nr 108 and 18.3 ± 0.3 for detector nr 7. The thicknesses of the detectors are 282.5 ± 5 µm and 264 ± 5 µm for detectors 108 and 7, respectively. To check if the difference in S/N ratio corresponds to the difference in detector thickness, Eq. (6-1) and Eq. (6-2) shows the thickness ratio and the S/N ratio, and we find that they are quite equal. Accordingly S/N is proportional to the detector thickness.

$$Thickness\ ratio \Rightarrow \frac{264\mu m}{285.5\mu m} = 0.93 \pm 0{,}02 \tag{6-1}$$

$$Signal/Noise\ ratio \Rightarrow \frac{18.3}{20.2} = 0.91 \pm 0{,}02 \tag{6-2}$$

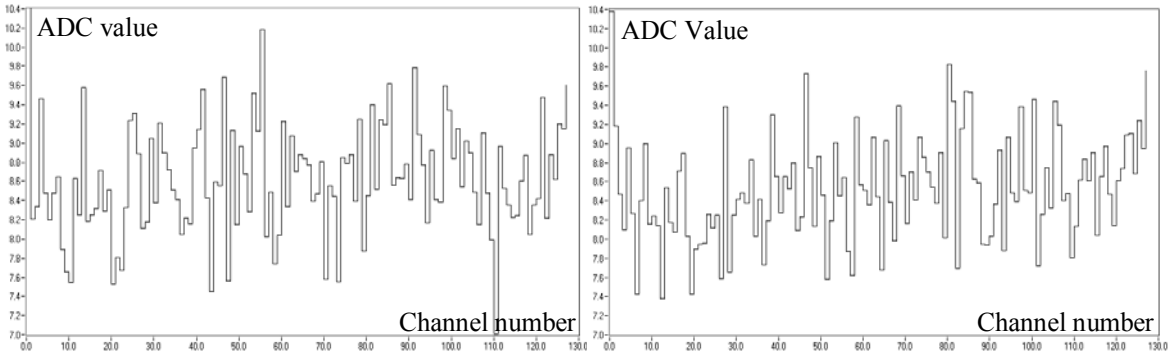

Figure 53 RMS Noise versus channel number for detector nr 108 and nr 7

A study of the RMS (Root Mean Square) noise shows that neither the detector voltage nor the thickness of the detector influenced on the RMS noise value. Without any exceptions the RMS noise level was fluctuating around 8.5. This supports that the higher S/N ratio of the thick detector comes from a higher signal, and not from a lower noise.

As mentioned, 12 bit resolution gives $2^{12} = 4096$ channels, and since we have 2 V peak to peak this gives 2 V / 4096 channels = 0.49 mV pr channel. Figure 53 shows the RMS noise on the detector nr 108 to the left and detector nr 7 to the right, with a mean value around 8.5. The ADC value 8.5 can then be multiplied with 0.49 mV/channel, which gives RMS noise value of 4.15 mV.

The plots in Figure 54 to Figure 59 show the Signal/Noise distribution for some bias voltages. The increase in Signal/Noise for an increase in bias voltage is clearly seen. It is such plots that are used for calculating the mean value and its standard deviation for all the plots with Signal/Noise ratio included.

The number of events decides the amount of data, and thus the standard deviation. For bigger runs the curve gets smoother and smoother. 2 000 events gives approximately a sigma in the S/N of 2, 10 000 events gives approximately sigma = 1, 30 000 runs gives approximately sigma = 0,6, and one million events gives approximately sigma = 0.1.

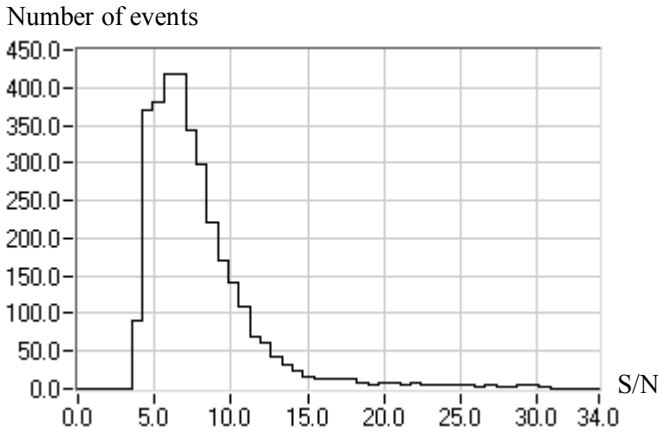

Figure 54 Signal/Noise distribution at a bias of 10 V

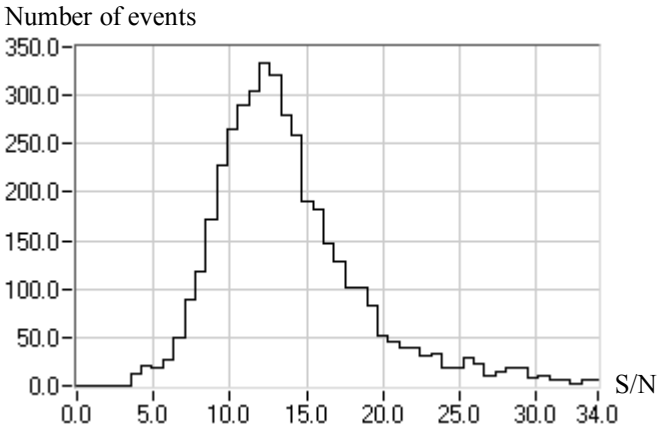

Figure 55 Signal/Noise distribution at a bias of 30 V

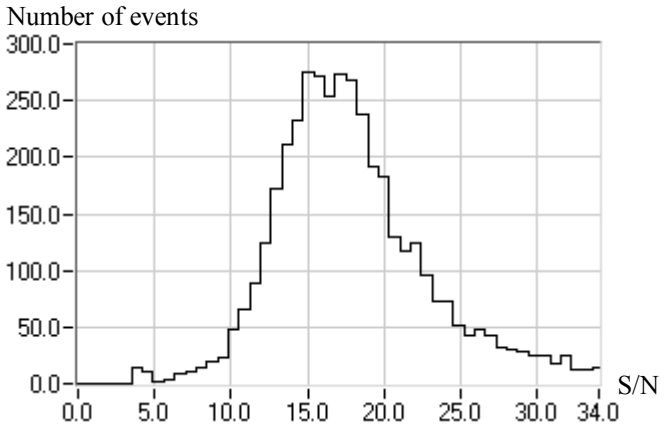

Figure 56 Signal/Noise distribution at a bias of 50 V

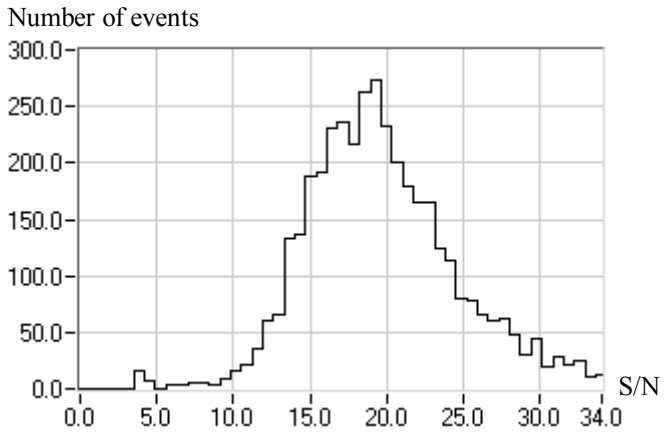

Figure 57 Signal/Noise distribution at a bias of 70 V

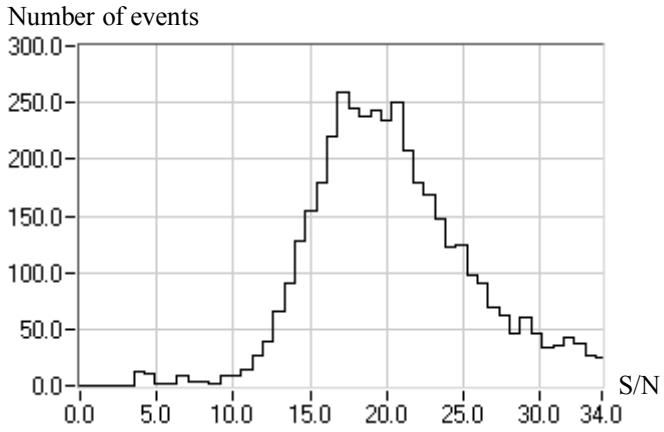

Figure 58 Signal/Noise distribution at a bias of 100 V

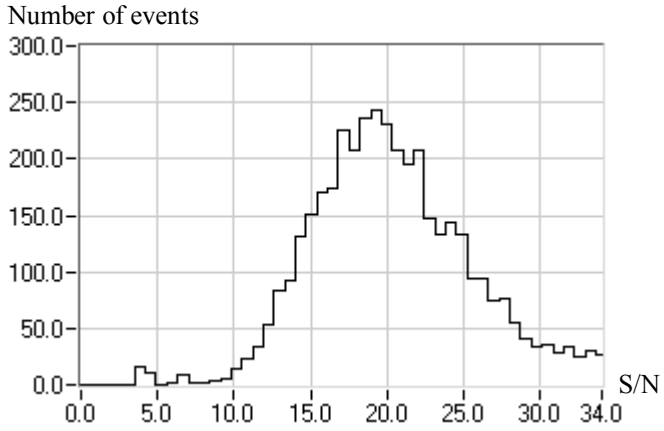

Figure 59 Signal/Noise distribution at a bias of 150 V

6.4 Signal/Noise for Different Readout Frequencies

When finally the setup worked at 40 MHz, some long-term measurements at different readout frequencies were made, for checking if there were variations in Signal/Noise ratio. To ensure no variation with time, we made 18 measurements with 10 000 events. The small fluctuations seemed to be totally random. So for the other frequencies, really long runs, with one million events were taken, to get a low standard deviation.

Table 12 Signal/Noise ratio and the calculated sigma for different readout frequencies

Frequency	Signal/Noise	Standard Deviation
5 MHz	20,1	0,1
10 MHz	20,2	0,1
40 MHz	20,15	0,24

With many measurements, all with the same standard deviation (σ), the standard deviation (σ_m) of the mean value can be calculated by the formula [23]:

$$\sigma_m = \frac{\sigma}{\sqrt{N}} \tag{6-3}$$

where N is the number of measurements. This means that 100 runs with 10 000 events are needed to get the σ_m down to 0.1. We can see from Table 12, that even with very long measurements, the readout frequency does not influence on the Signal/Noise ratio.

6.5 Detector thickness

Controlling the detector thickness was done by measuring the unused parts of the detector (half-moon formed edge wafer, referred to as baby detectors). A micrometer screw attached to the table with a vice seemed to be the best solution. Then it was possible to simultaneously tighten the micrometer screw, and hold the baby detectors. Thicknesses were measured in both ends, so we could find the thickness difference in each wafer. When there where two baby detectors, we took one measurement of each. The measurements are shown in Figure 60 and Figure 61, with some listed values above.

Analysis of variances for thin Detectors (0-100)

Number	*Mean*	*Variance*	*Standard deviation*
36	258,7	45,2	6,7

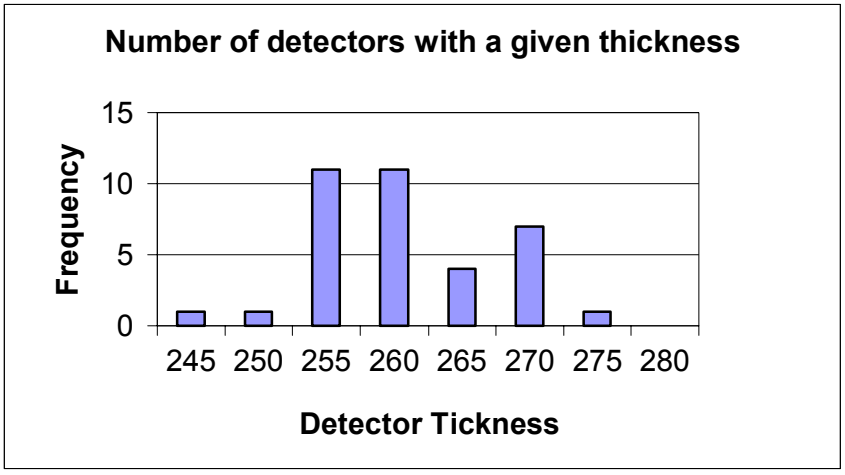

Figure 60 Thickness measurements of unoxygenated detectors

Analysis of variances for thick Detectors (100<)

Number	*Mean*	*Variance*	*Standard deviation*
34	285,7	34,3	5,9

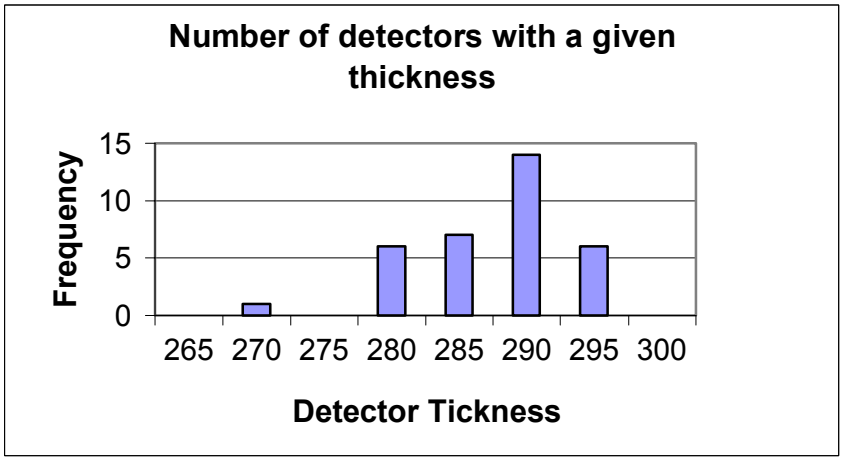

Figure 61 Thickness measurements of oxygenated detectors

6.6 Signal Flow through the Setup

For making debugging and maintenance of the setup easier in the future, some screenshots are included, see Figure 62 to Figure 75. The screenshots are taken with Tektronix oscilloscope together with RS232 cable, and some software for the PC.
Each plot is trigged on the readout train to be able to see the timing of the different plots. The trigger is set on the first negative going pulse of the first three transitions, indicating the start of the readout train, marked with the T. Then comes the 128 channels, and at the end comes some transitions indicating the end of the readout train. Some explanations for some of the figures are listed below:

Figure 66 3) ECL/NIM/ECL Output 15 is the SIROCCO gate (X15). This should go low just before the readout channels, and has to be down until the readout train is finished.

Figure 69 This shows the 40 MHz clock before it goes into the gate generator, which decides which frequency to be used.

Figure 70 This shows the 5 MHz gated clock, ANDed with the SIROCCO gate (X15). The output from AND gate nr 4 is sent into the SIROCCO CLK. These pulses start the analog to digital conversion of the analog signals from the SCTA128 chip. It is a good rule to scoop this channel together with the readout train while making measurements, to see that everything is ok.

Figure 71 2) OR Output nr 1 and 3) OR Output nr 2, have signals that are about 800mV.

Figure 72 FAN OUT Output nr 1 and 2 have signals that are 1400 mV. The setup should work without these to fan outs, but seems to be necessary to get strong enough signals for the SEQSI trigger.

Figure 73 Here the gate generator has scaled down the frequency from 40 MHz to 5 MHz (Compare with Figure 69, output from AND gate nr 3). Important to measure that the frequency is exact the frequency that is wanted. Can be tuned with the potentiometer screw on the gate generator.

Figure 74 Rather bad picture because of the high frequency, showing that the 40 MHz is better at the ECL-NIM-ECL output 1, than the SEQSI output CLK. Due to this the ECL-NIM-ECL output 1 is used in the NIM logic instead of the CLK from the SEQSI.

Figure 75 Output from AND gate nr 4, the same as Figure 70, just with another time scale. To show that it stops some time after the readout train.

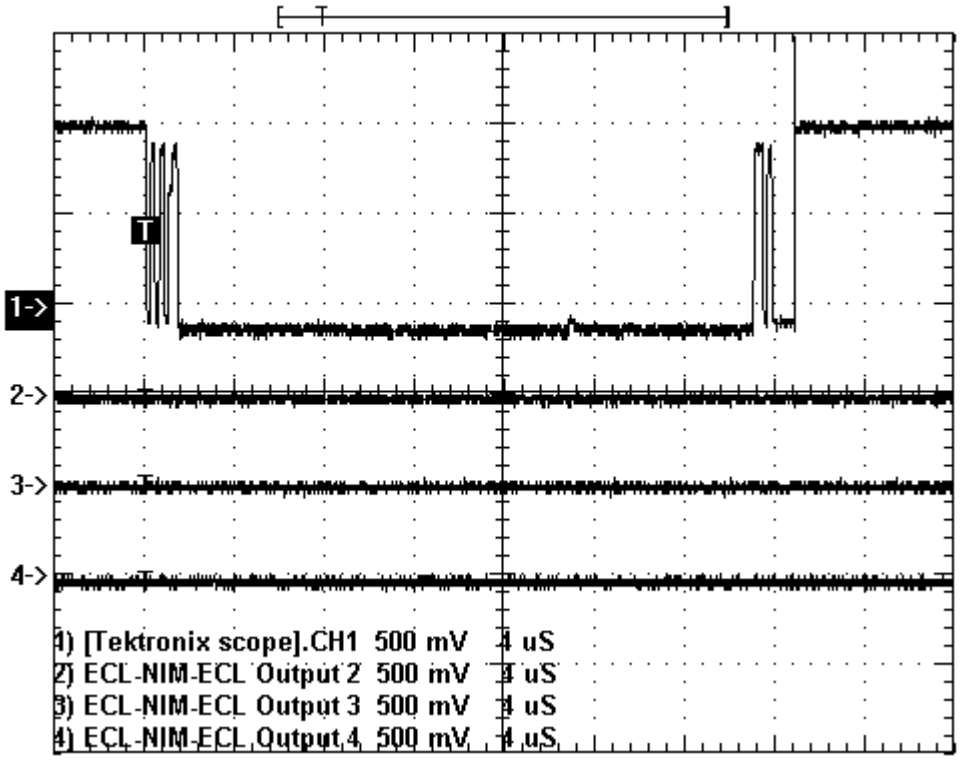

Figure 62 Readout + Output 2, 3 and 4

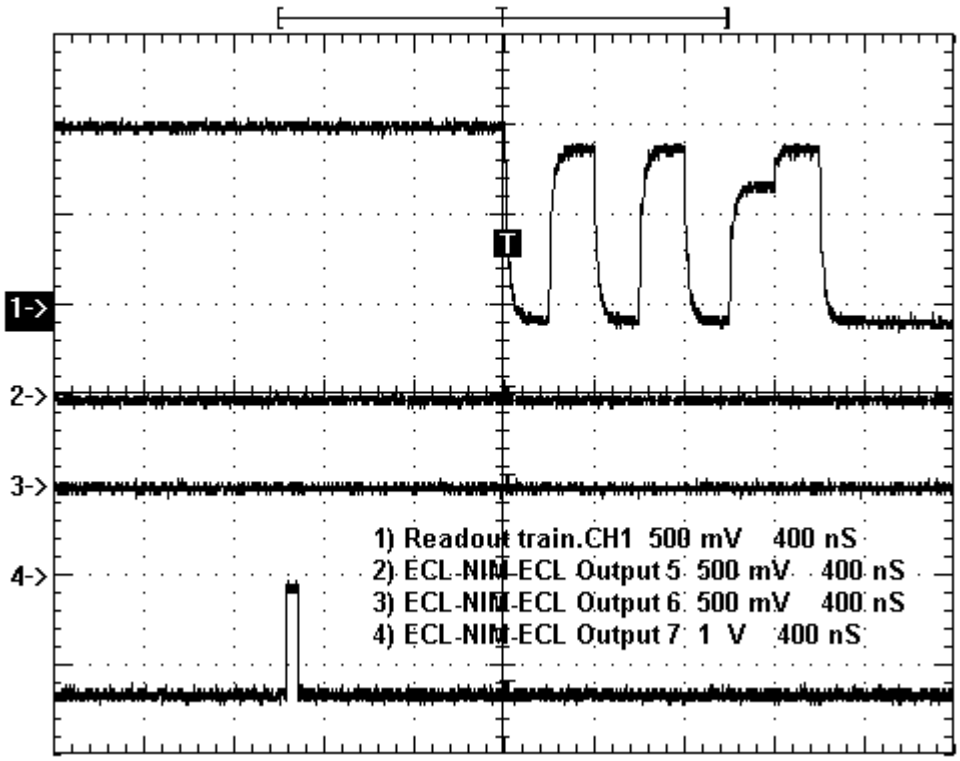

Figure 63 Readout + Output 5, 6 and 7

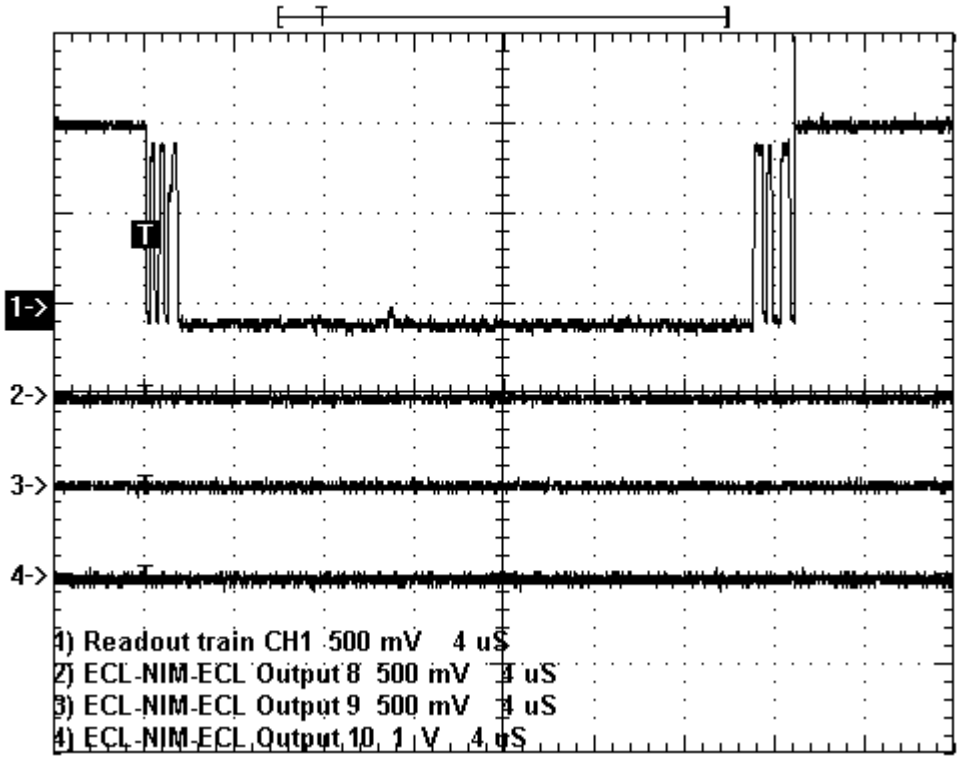

Figure 64 Readout + Output 8, 9 and 10

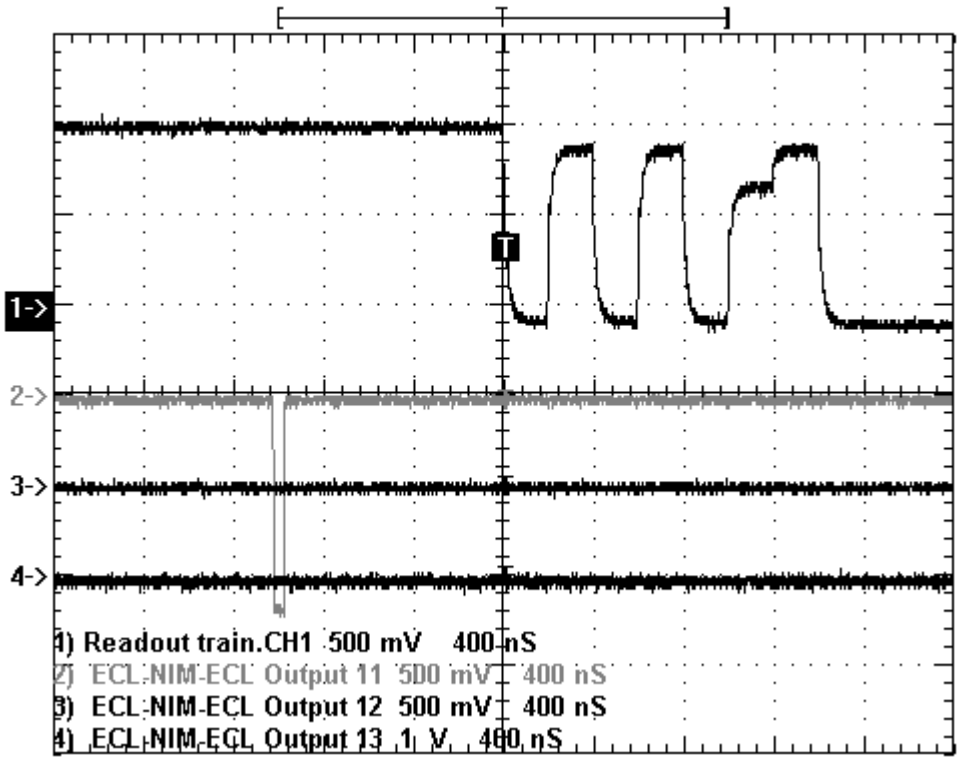

Figure 65 Readout + Output 11, 12 and 13

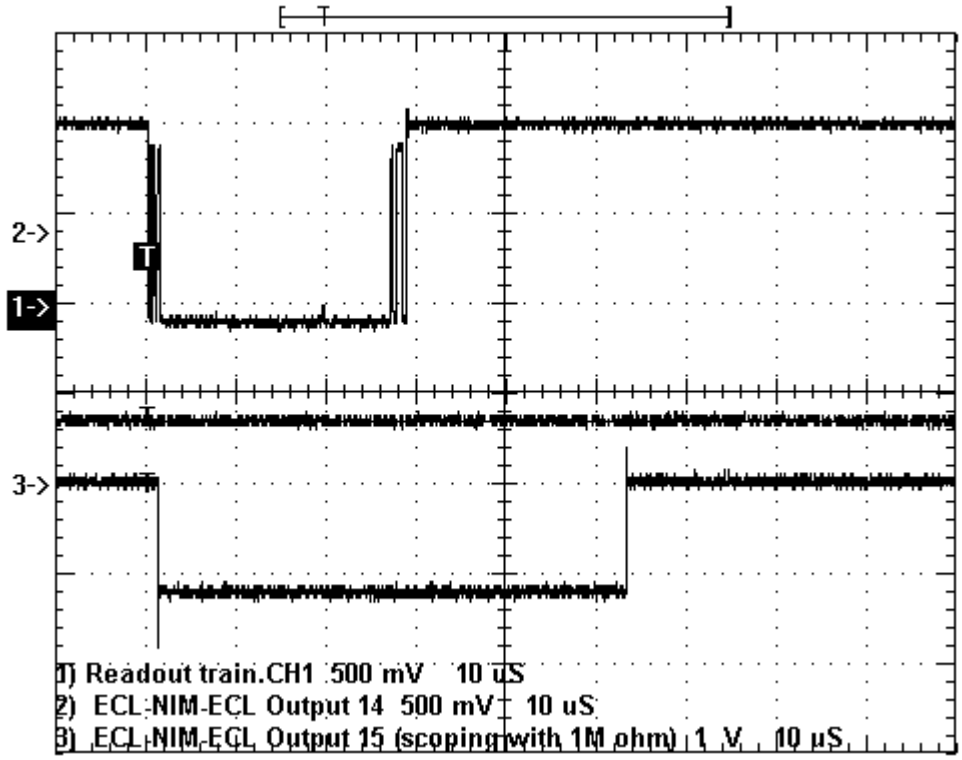

Figure 66 Readout + Output 14 and 15

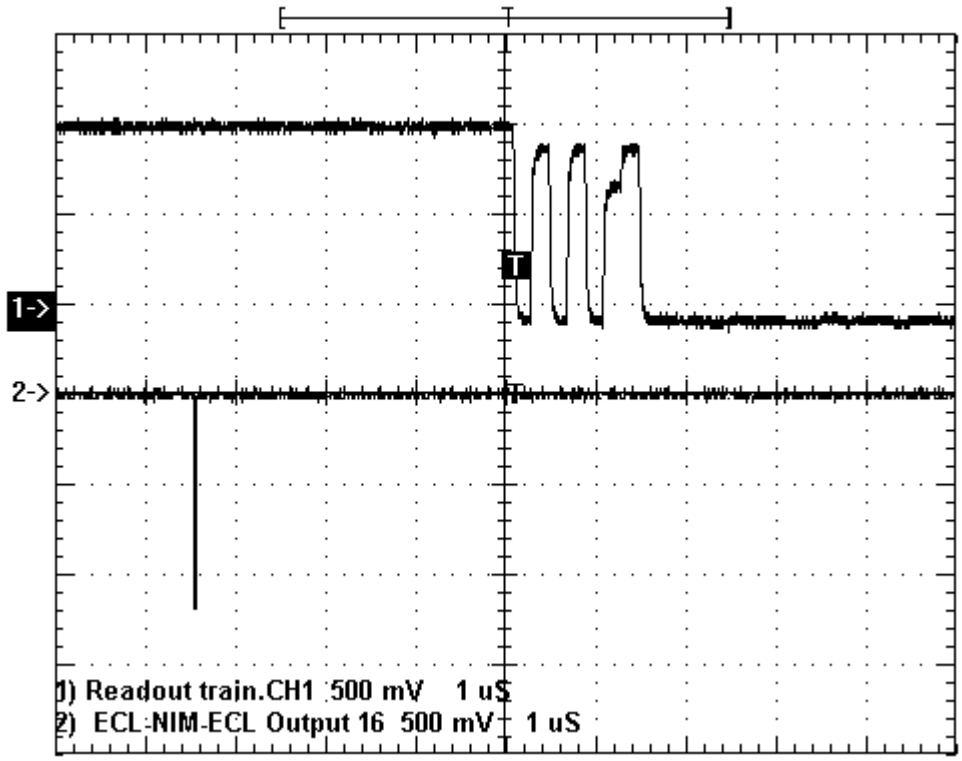

Figure 67 Readout + Output 16

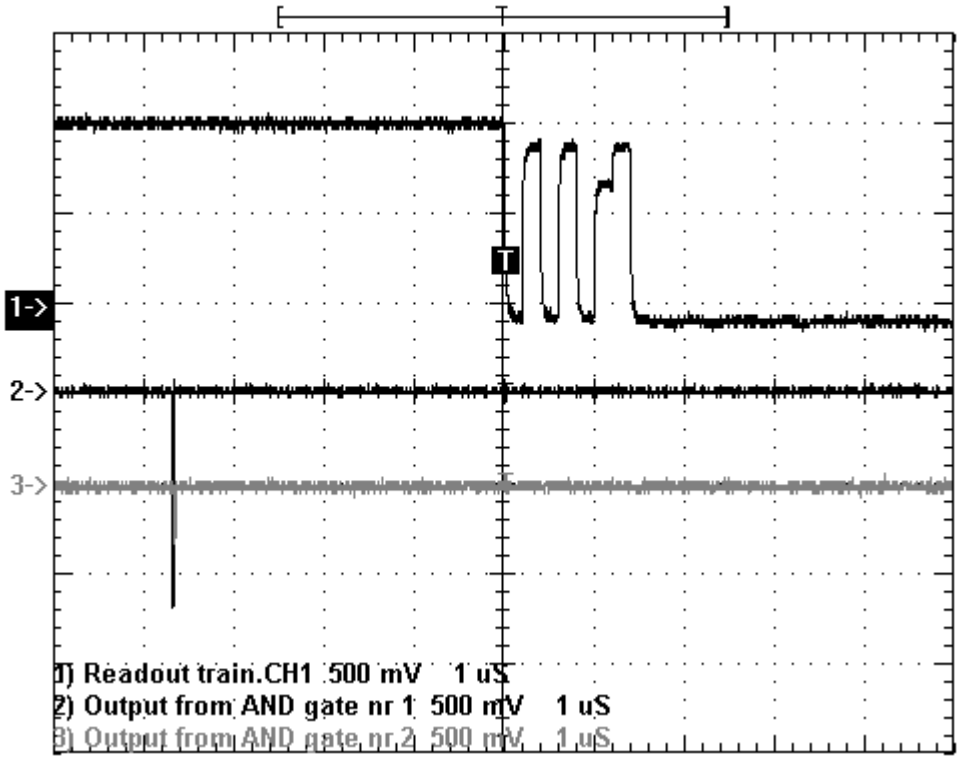

Figure 68 Readout + AND gate 1 and 2

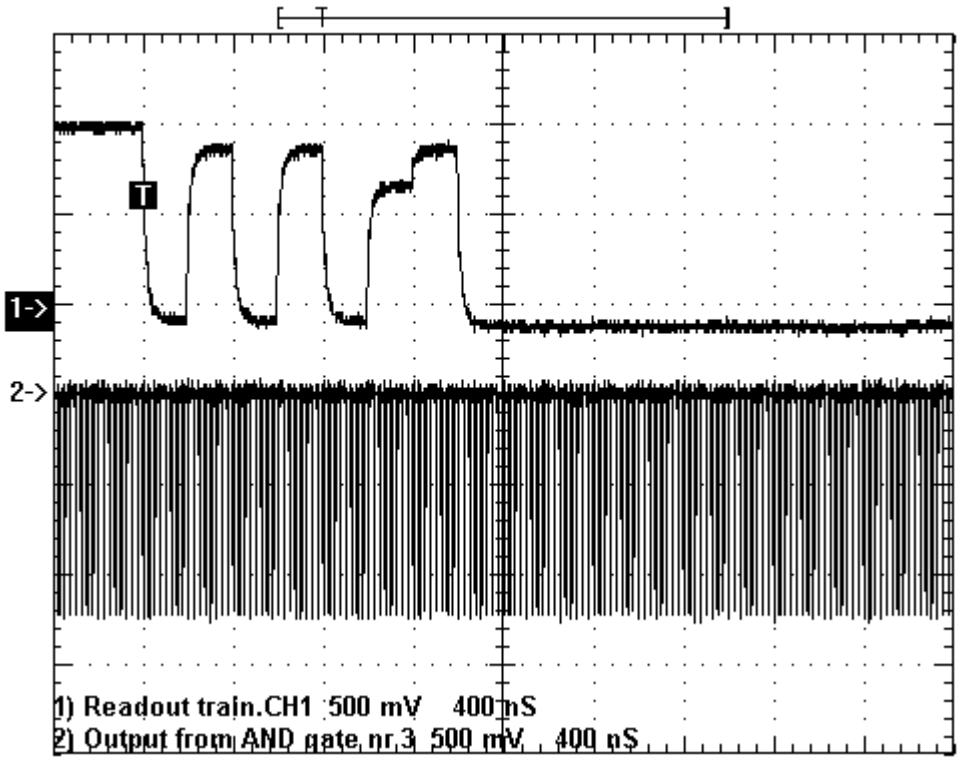

Figure 69 Readout + AND gate 3

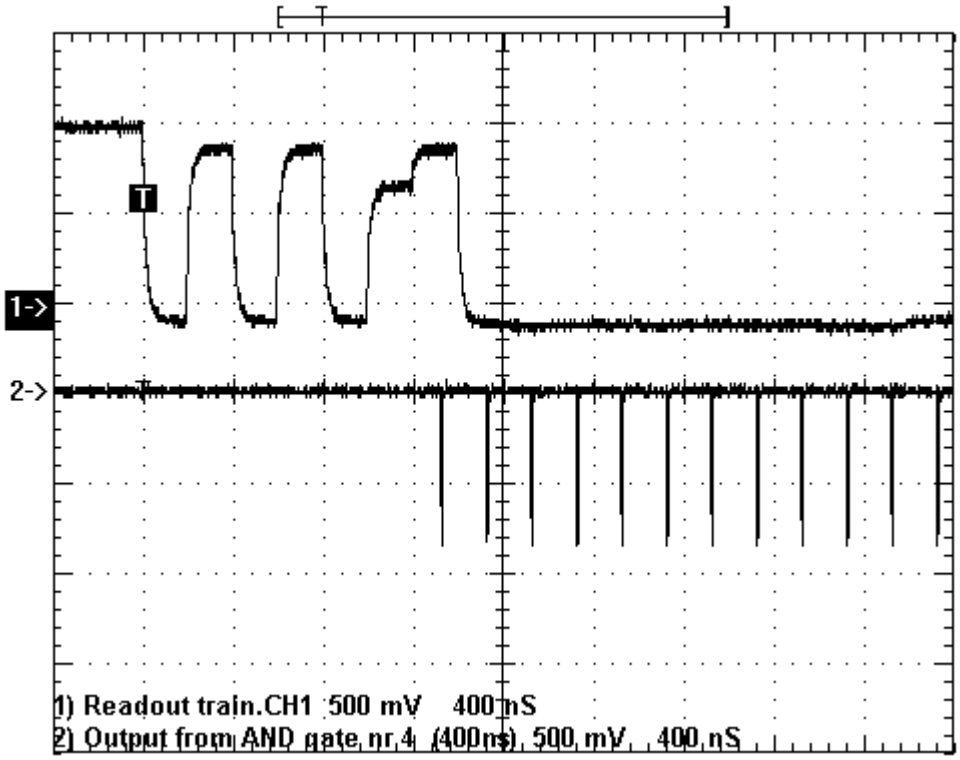

Figure 70 Readout + AND gate 4

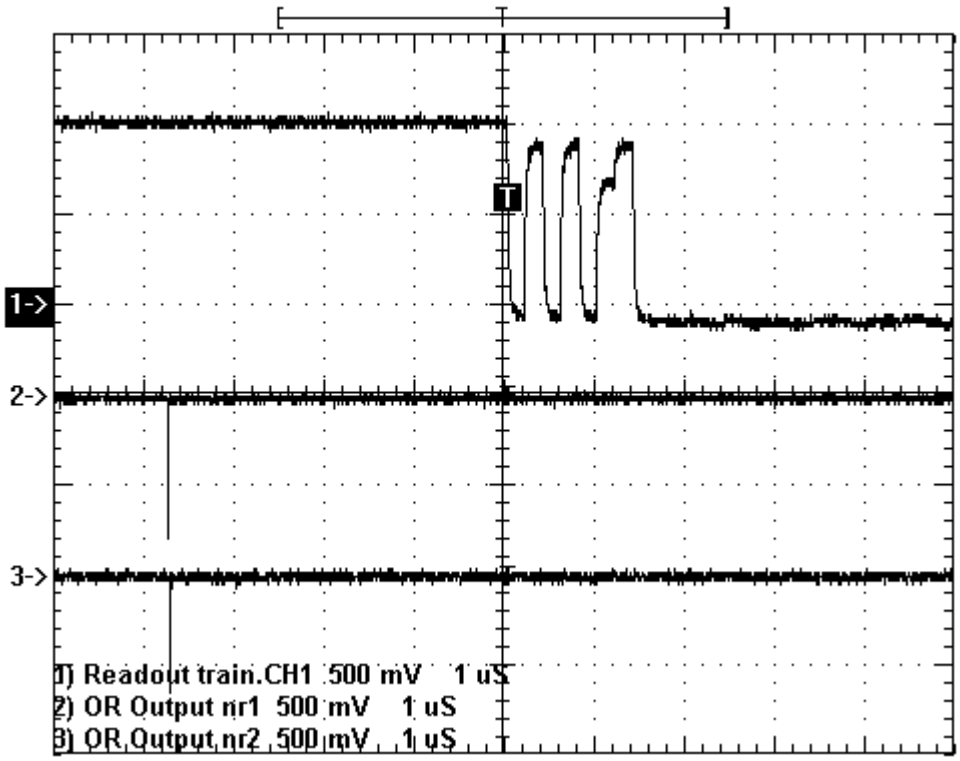

Figure 71 Readout + OR Output 1 and 2

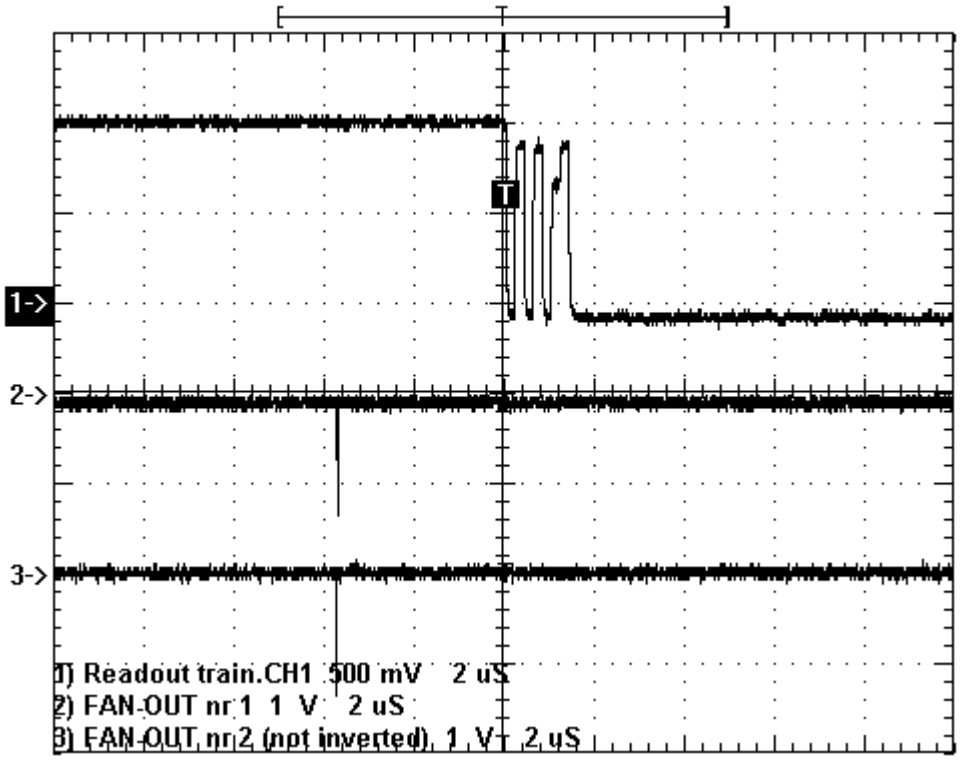

Figure 72 Readout + FAN-OUT Output 1 and 2

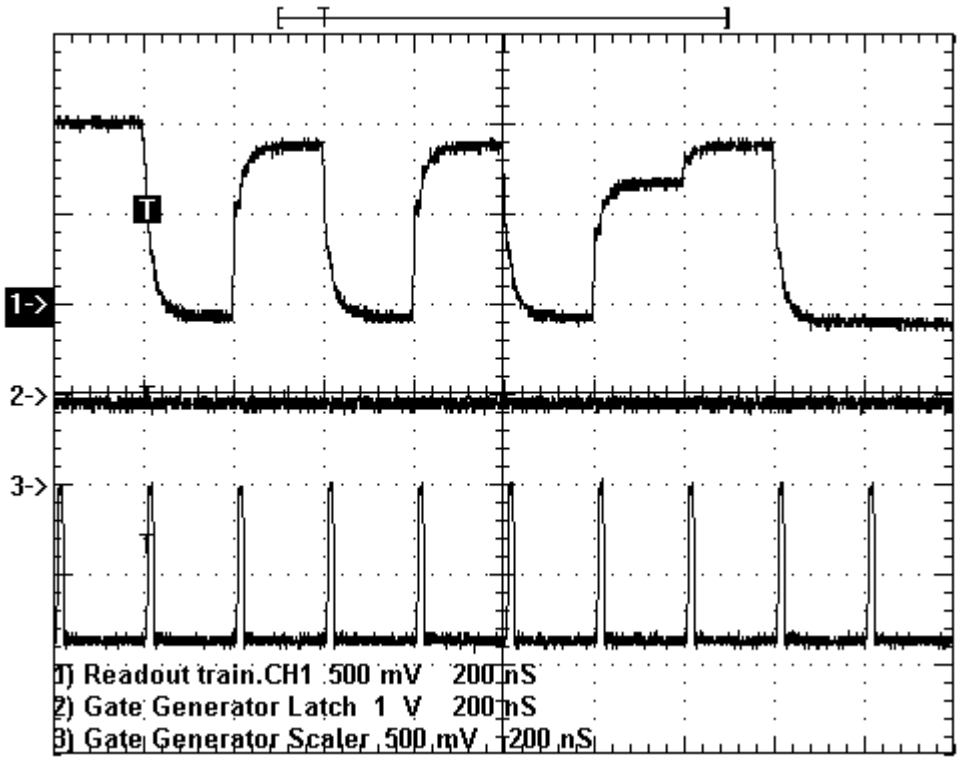

Figure 73 Readout + Gate Generator Latch and Scaler

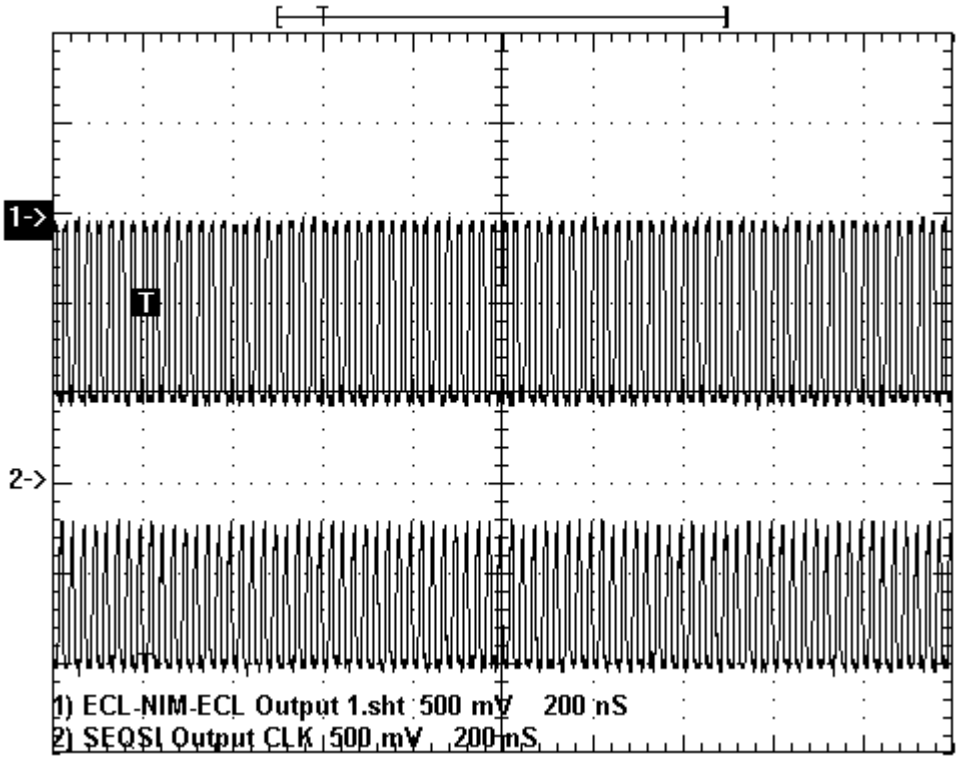

Figure 74 ECL/NIM/ECL Output 1 + SEQSI Output CLK

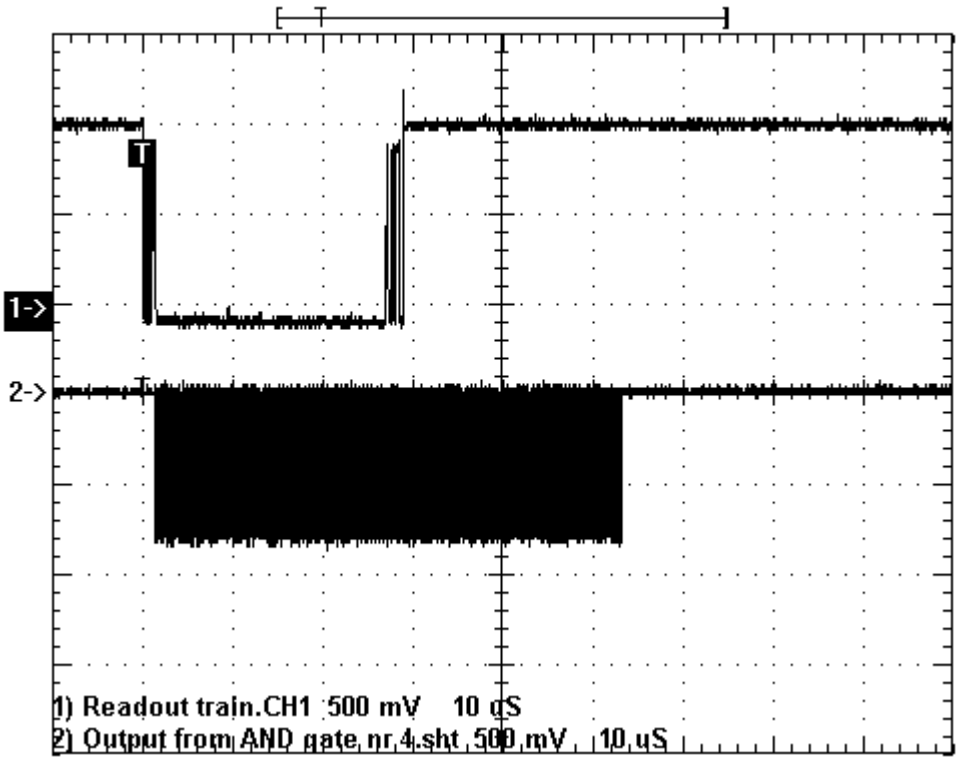

Figure 75 Readout + AND Output 4

7 Conclusion

The goal of this work has been to set up a system to test detectors with fast readout electronics, using a LabVIEW program, and the readout chip SCTA128HC. A lot of time was spent on debugging and replacing faulty modules. In the future, all the hardware trouble we experienced should be unnecessary, and with this documentation it should be possible to build up and maintain the setup rather quickly. The way to do this is to check each module separately and be sure that the communication is working, then build up the NIM logic for the trigger part, and when this is working, finally build the NIM logic for the SIROCCO clock part. How this has been done, is extensively explained in this thesis, together with comments and suggestions. Some modifications on the trigger part had to be made to the NIM logic for the program. Fine tuning of the parameters was performed to increase the S/N ratio. How these parameters are tuned has been explained in the thesis.

The data from the SCTA128HC chip were finally collected successfully for 5, 10, 20 and 40 MHz readout frequencies. We reached our goal which was to get the system running, and we also made some measurements that show a good linearity and a high Signal/Noise ratio around 21. Hopefully this thesis will include enough documentation and explanation for a newcomer to build up and maintain a similar setup, without using too much time.

Appendix A: Search the web

How to get documentation out of the web takes time to learn. The first important thing to learn is how to sort out all the nonsense. Search engines are huge databases of web page files that have been assembled automatically by a machine. When creating a search statement and structuring the query, keep the following in mind:

- Whenever possible, use nouns and objects as keywords.
- Be specific.
- Put most important terms first in the keyword list.
- Use at least three keywords in the query.
- Combine keywords, whenever possible, into phrases.
- Avoid common words, unless they are part of a phrase.
- Think about words that could be expected to find in the body of the page, and use them as keywords.

Type the operators (AND, OR, AND NOT, NEAR or equivalent symbols), and words to define the search. Use parentheses to group complex phrases. An operator must precede all but the first word, or most search engines interpret the words as a phrase. (Use an asterisk to include plurals, and other grammatical variations.)

Basic Search Tips: Use the plus (+) and minus (-) signs in front of words, to force their inclusion and/or exclusion in searches. EXAMPLE: +strip -pixel (remember no space between the sign and the keyword). Use double quotation marks (“ ”) around phrases to ensure they are searched exactly as is, with the words side by side in the same order. EXAMPLE: “Silicon micro-strip” (There is no use in putting quotation marks around a single word). Type keywords and phrases in lower case, to find both lower and upper case versions. Typing capital letters will usually return only an exact match. EXAMPLE: pixel retrieves both pixel, and Pixel.

Use truncation and wildcards to look for variations in spelling. EXAMPLE: “librar” returns library, libraries, librarian, etc.

Combine phrases with keywords, using the double quotes and the plus (+) and/or minus (-) signs. EXAMPLE: +“silicon detector” +strip -pixel (In this case, if a keyword with a +sign is used, the +sign has to be put in front of the phrase as well. When searching for a phrase alone, the +sign is not necessary.)

When searching in a document for a keyword(s), use the “find” command on that page. Ctrl+F is the short key for windows.

Know the default settings the search engine uses (it may be AND or OR). This will have an effect on how to configure the search statement, because if no signs are used (+, - “ ”), the search engine will default to its own settings.

Most search engines have made its own partition for different subjects, sometimes it is smart to follow these, and find a search engine made for a special subject.

Some search engines show the lines where the search string matches, this is a better indication on a good hit than reading all the headlines. The headlines often deal with something totally different than what is searched for.

Tables

Figures

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